A High-Speed CMOS Divide-by-32/33 Prescaler

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***Abstract*—This work compares the design methodologies of four common flip-flop topologies - Transmission Gate (TG), True Single-Phase Clock (TSPC), Source-Coupled Logic (SCL), and Wang - for implementing a divide-by-2 prescaler. Building upon this comparison, a high-speed divide-by-32/33 prescaler design is presented for high-speed applications in 16nm CMOS Technology. This design utilizes cascaded TSPC-based divide-by-2/3 units combined with control logic gates designed using complementary CMOS logic. The prescaler operates at speeds up to 38GHz at 25°C with 0-0.7V full logic swing. At a frequency of 25GHz, the power dissipation is measured at 0.33mW. The paper further delves into a detailed performance analysis of the proposed design.**

***Index Terms*—Frequency dividers, true single phase clock, CMOS prescaler, high speed communication circuits.**

I. Introduction

Modern SoCs often consist of multiple modules that operate in specific clock domains. For example, the clock frequency of each core in multicore processors is dynamically adjusted to improve speed, energy efficiency, and thermal management [1–3]. Thus, Phase-locked loops(PLL) become crucial for synchronizing signals and frequency management [4]. Frequency dividers are used in the PLL loop to reduce the reference frequency. The dual modulus $N/N+1$ ($N = 2^n$) prescaler is used in fractional-N frequency synthesizers [5].

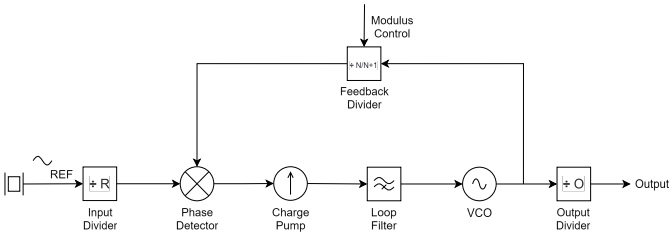

Figure 1: Fractional-N PLL

Flip-flops(FF) and logic gates are used to construct the prescaler. Divide-by-2 circuits can be realised using transmission gates, pass transistors, basic gates, TSPC logic, SCL logic, Wang topology, current-mode logic(CML), or extended TSPC(E-TSPC) [6, 7]. As communication systems push towards ever-higher frequencies, the demand for low-power, high-speed dividers operating in the tens of GHz range is becoming increasingly critical. While different topologies have distinct advantages, optimizing performance and power consumption based on the application is crucial. Power consumption and performance of various divide-by-2 circuits are explored, and a divide-by-2/3 unit is designed using the TSPC approach. The divide-by-32/33 prescaler is designed by cascading five such units coupled with control logic.

II. Analysis of different logic styles for divide-by-2 unit

This work explores the design of a divide-by-2 unit utilizing various logic styles for flip-flops (FFs), which are fundamental building blocks in sequential circuits. The performance of each design is analyzed using simulations in LTSpice with 16nm HP PTM CMOS models from [8]. Rise and fall times are defined as the time taken for the voltage to transition from 10% to 90%(figure 4) and from 90% to 10%(figure 5) of the supply voltage (VDD), respectively, minimizing noise margins. The propagation delay is, $t_d = \frac{t_{\text{rise}}+t_{\text{fall}}}{2}$.

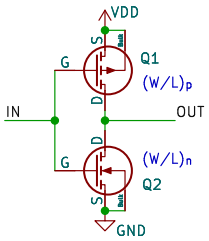

Figure 2: CMOS Inverter

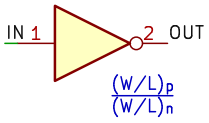

Figure 3: Inverter Symbol

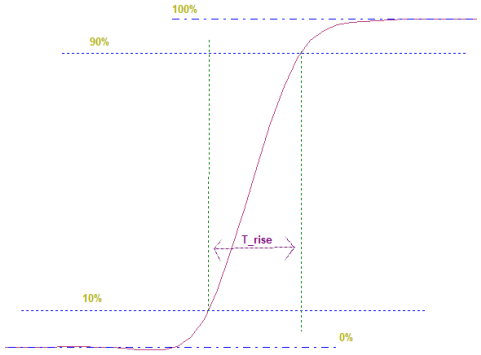

Figure 4: Rise time

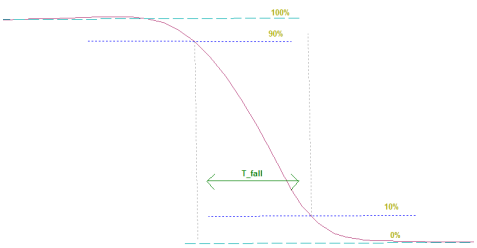

Figure 5: Fall time

A. *Transmission Gate Logic*

Our analysis revealed that the transmission gate-based design (figure 6) achieved a maximum operational speed of 32 GHz at 25°C. It exhibited an average power consumption of 39.9µW at 10 GHz for the mentioned temperature. The input and output waveforms are illustrated in figure 7. The rise and fall times are detailed in table 1.

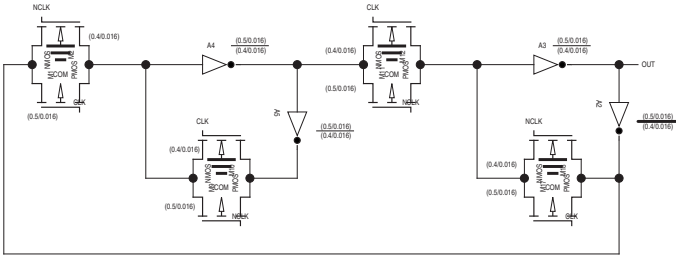

Figure 6: Divide-by-2 using TGs

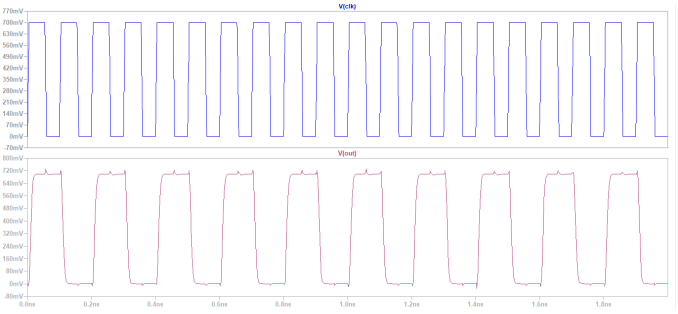

Figure 7: Input and output waveforms

Rise/Fall time	time(ps)
Rise time	9.8
Fall time	9.4

Table 1: Rise and fall time

B. *SCL Topology*

The source-coupled logic (SCL) topology design (figure 8) achieved a maximum operational speed of 11 GHz while consuming an average power of 82 µW at 10 GHz and 25°C. However, this design exhibited a higher rise time (25.6 ps) than other investigated topologies, as shown in table 2. The input and output waveforms at 10 GHz are illustrated in figure 9.

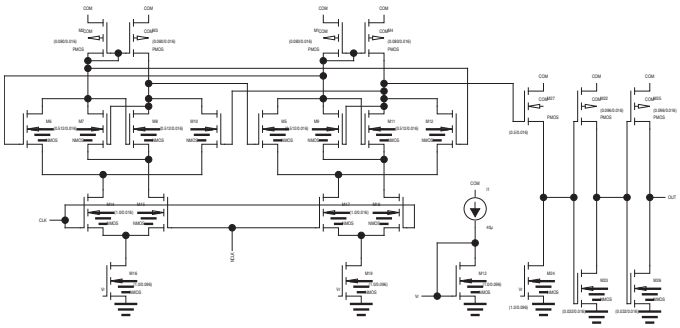

Figure 8: Divide-by-2 unit, SCL topology

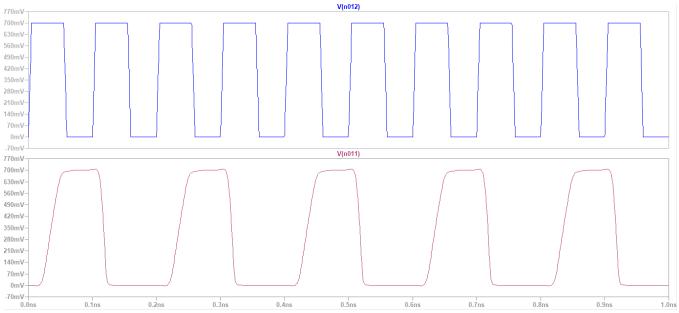

Figure 9: Input and output waveforms

Rise/Fall time	time(ps)
Rise time	25.6
Fall time	9.8

Table 2: Rise and fall time

C. *Wang Topology*

Building upon the Wang topology [9], our design (figure 10) incorporates modifications to reduce power consumption. While this design achieves a higher maximum operational speed of 16 GHz at 25°C compared to the SCL design, it consumes more power (135.5 µW on average at 10 GHz) as shown in table 3. The input and output waveforms at 10 GHz are illustrated in figure 11.

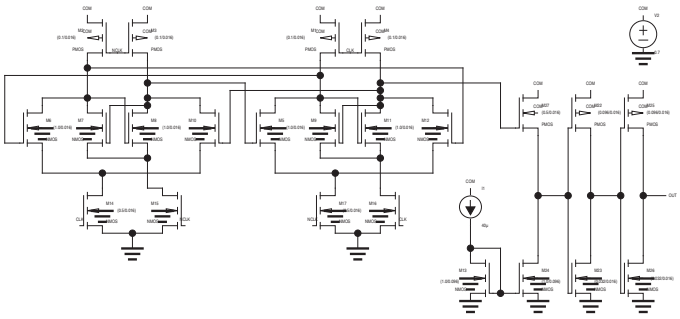

Figure 10: Design prepared analogous to [9]

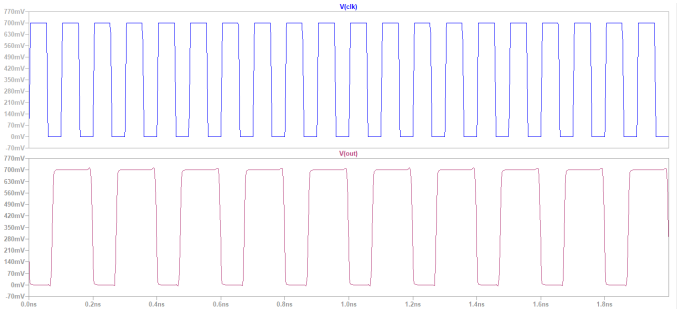

Figure 11: Input and output waveforms

Rise/Fall time	time(ps)
Rise time	11.2
Fall time	7.1

Table 3: Rise and fall time

D. TSPC Topology

The TSPC-based design(figure 14, in divide-by-2 mode) achieved an impressive maximum operational speed of 35 GHz at 25°C while maintaining a moderate average power consumption of 43.9 µW at 10 GHz. This design exhibited the fastest operation among the investigated topologies and offered a good balance between speed and power. The rise and fall times were measured to be 6.6 ps and 5.9 ps, respectively (table 4). The input and output waveforms at 10 GHz are shown in figure 12.

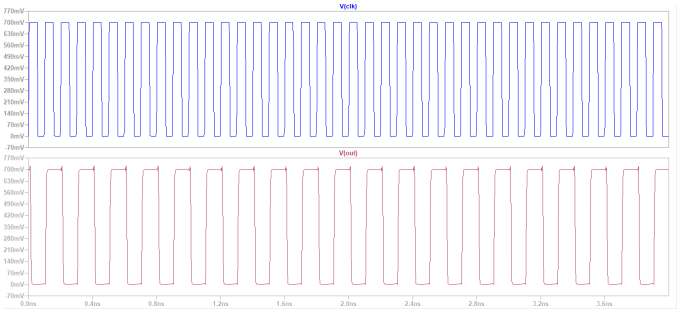

Figure 12: Input and output waveforms

Rise/Fall time	time(ps)
Rise time	6.6
Fall time	5.9

Table 4: Rise and fall time

A graphical representation comparing these logic styles is presented in figure 13.

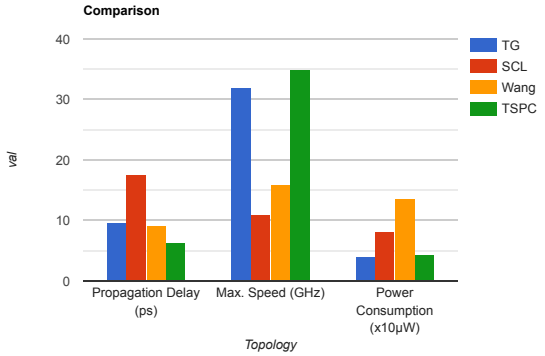

Figure 13: Comparison between the logic styles

III. Analysis of the Divide-by-2/3 Prescaler

TSPC-based flip-flops are preferred due to their smaller area footprint [10], reduced clock skew issues, and lower power consumption The divide-by-2/3 prescaler is realised from [7]. The design (figure 14) operates in either divide-by-2 mode or divide-by-3 mode based on the control input(M). When M is held at logic high, the output frequency is half the input frequency. Conversely, a low M signal sets the output frequency to one-third of the input frequency. The timing diagram in figure 15 illustrates this behaviour.

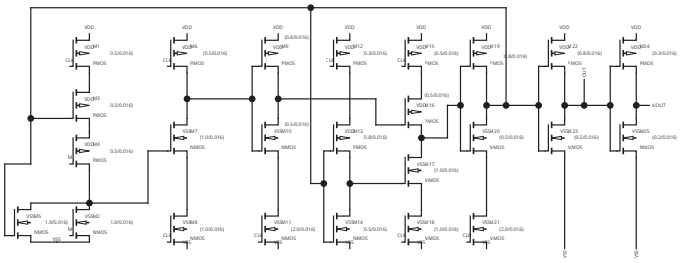

Figure 14: Divide-by-2/3 unit

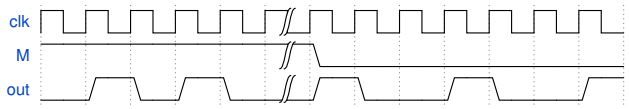

Figure 15: Timing diagram of divide-by-2/3 operation

IV. Analysis of the divide-by-32/33 prescaler

This section explores a divide-by-32/33 prescaler design utilizing five cascaded divide-by-2/3 units (figure 17). The first stage is switchable between divide-by-2 and divide-by-3 modes based on a control signal generated by complementary CMOS logic (figure 16). The remaining four stages operate in divide-by-2 mode continuously.

The operating mode of the entire prescaler is determined by the MODE input signal. A logic high MODE signal sets the prescaler to divide-by-32 mode, while a logic low MODE signal enables divide-by-33 mode. In divide-by-33 mode, the first stage switches to divide-by-3 operation when the control logic circuit (implemented using an OR gate) detects a specific combination of outputs from the flip-flops. This combination includes either a high output from one of the two designated flip-flops (X2 and X3) or a low output from one of the other two flip-flops (X4 and X5).

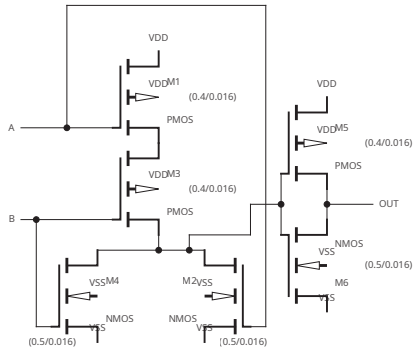

Figure 16: CMOS OR Gate using complementary logic

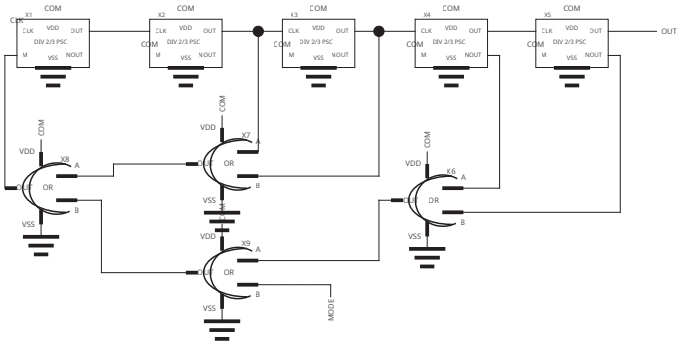

Figure 17: Divide-by-32/33

Performance

Simulations performed in LTSpice at various temperatures (0°C, 25°C, and 80°C) reveal the prescaler's maximum operational speeds (table 5). As expected, the maximum speed reduces with increasing temperature. The design achieves a maximum speed of 38.16 GHz at 25°C and consumes an average power of 0.33 mW under these conditions. The power consumption for both divide-by-32 (figure 18) and divide-by-33 (figure 19) modes is analyzed in separate figures.

Temperature($^\circ C$)	Max. freq.(GHz)
0	45.25
25	38.16
80	24.67

Table 5: Maximum operable frequency

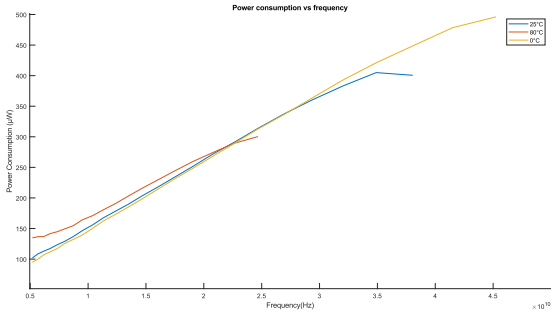

Figure 18: Power consumption in divide-by-32 mode

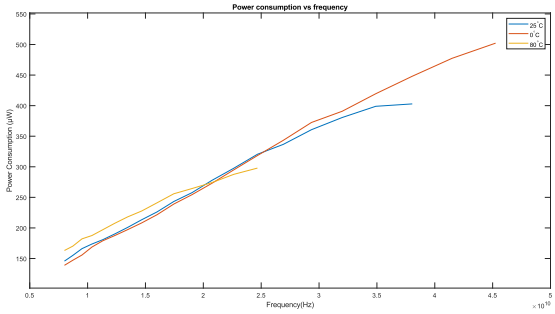

Figure 19: Power consumption in divide-by-33 mode

V. Conclusion

This work investigated the design and performance of a divide-by-32/33 prescaler utilizing various logic styles for flip-flops. The analysis focused on four main designs: transmission gates topology (TGs), source-coupled logic (SCL), a modified Wang topology, and transistor-switching logic (TSPC).

The analysis revealed that the TSPC-based flip-flop offered the best balance between speed (achieving a maximum operational speed of 35 GHz) and moderate power consumption (43.9 μW at 10 GHz). By cascading five divide-by-2/3 units with control logic, the overall design achieved both divide-by-32 and divide-by-33 functionality. Simulations in LTSpice demonstrated a maximum operational speed of 38.16 GHz at 25°C and an average power consumption of 0.33 mW in divide-by-32 mode. The prescaler exhibited the expected decrease in maximum speed with increasing temperatures.

This study successfully designed and analyzed a functional divide-by-32/33 prescaler. The findings provide a foundation

for further development and optimization to achieve even better performance metrics.

REFERENCES

[1] R. S. Peerla, A. Dutta, and B. D. Sahoo, "An extended range divider technique for multi-band pll," *Journal of Low Power Electronics and Applications*, vol. 13, 9 2023.

[2] A. K. Datta and R. Patel, "Cpu scheduling for power/energy management on multicore processors using cache miss and context switch data," *IEEE Transactions on Parallel and Distributed Systems*, vol. 25, no. 5, pp. 1190–1199, 2014.

[3] Y. Xing, F. Liu, N. Xiao, Z. Chen, and Y. Lu, "Capability for multi-core and many-core memory systems: A case-study with xeon processors," 2019.

[4] B. S. Premananda, N. Sahithi, and S. Mittal, "Avls-based 32/33 pre-scaler for frequency dividers," *e-Prime - Advances in Electrical Engineering, Electronics and Energy*, vol. 4, 6 2023.

[5] G. Ghiaasi and M. Ismail, "A cmos broadband divide-by-32/33 dual modulus prescaler for high speed wireless applications," 2005.

[6] J. Kaur and M. Sharma, "A review on various techniques to design 2/3 pre-scaler," *Int J Electric Electron Comp Sci Eng*, vol. 5, no. 1, pp. 115–9, 2018.

[7] J. Wu, Z. Wang, X. Ji, and C. Huang, "A low-power high-speed true single phase clock divide-by-2/3 prescaler," *IEICE Electronics Express*, vol. 10, no. 2, pp. 20120913–20120913, 2013.

[8] A. S. University, "Predictive technology model (ptm): 16nm high performance model card." https://web.archive.org/web/20191221222848/http://ptm.asu.edu/modelcard/HP/16nm_HP.pm 2019. Accessed: 2024-07-15.

[9] H. Wang, "A 1.8 v 3 mw 16.8 ghz frequency divider in 0.25 /spl mu/m cmos," in *2000 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.00CH37056)*, pp. 196–197, 2000.

[10] K. Swetha, K. Syamala, and U. Godugu, "Design of low power d-flip flop using true single phase clock," *International Journal & Magazine of Engineering, Technology, Management, and Research*, vol. 4, no. 4, pp. 370–374, 2017.