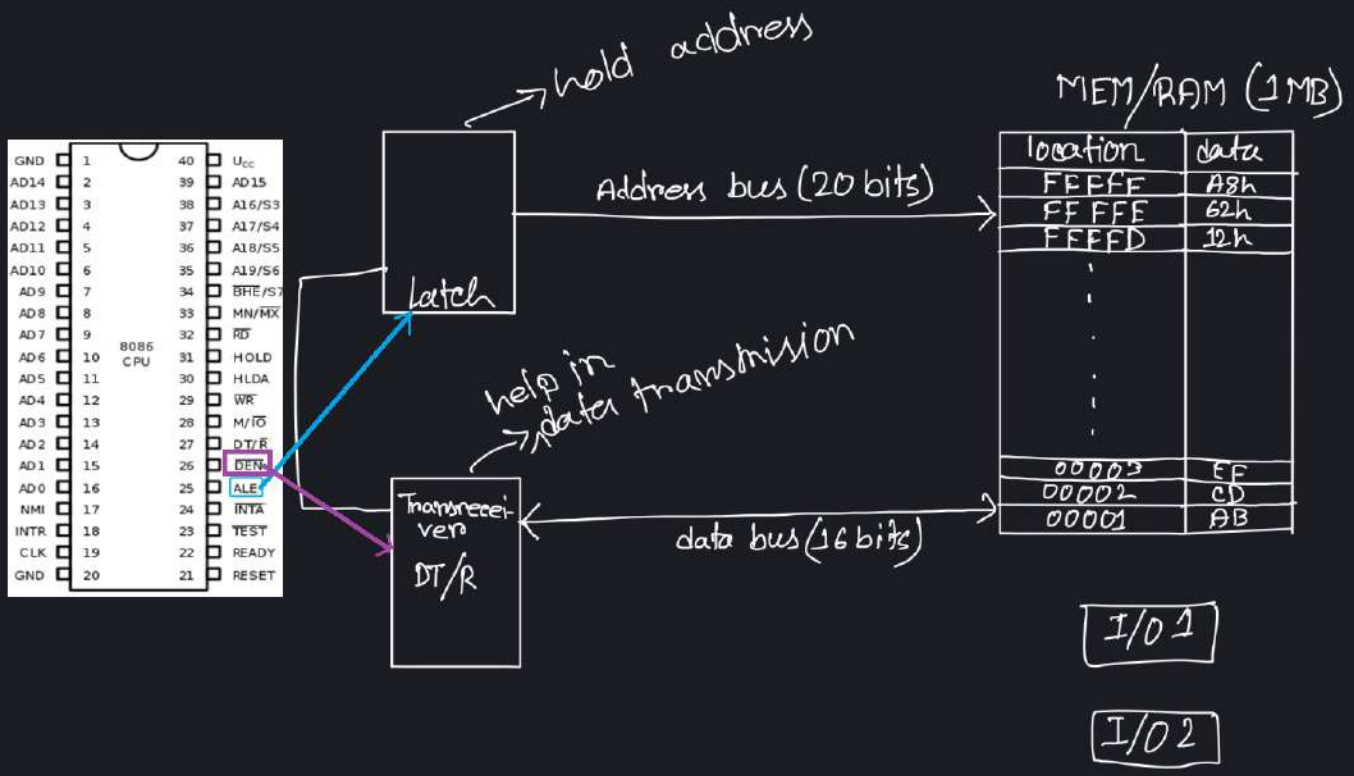


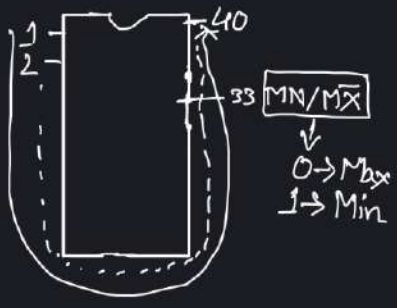

2 Mode

- ① Minimum mode
- ⑪ Maximum mode

Active high { y = 1 → ON ; y = 0 → OFF

Active low { $\overline{x}$ = 0 → ON ; $\overline{x}$ = 1 → OFF

Min mode → Pin 33 → 1

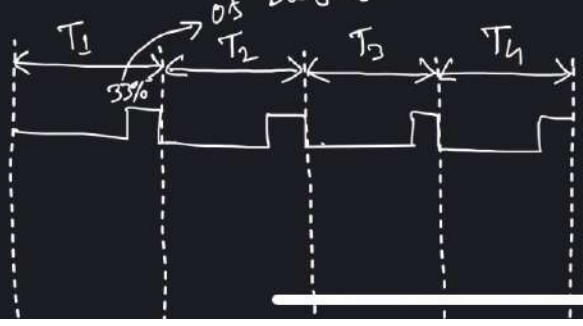


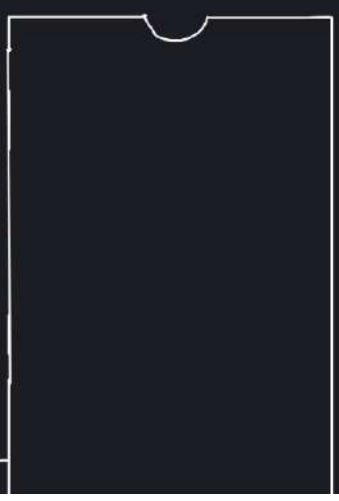

AD0–AD5 & / → Multiplexed



Read data:

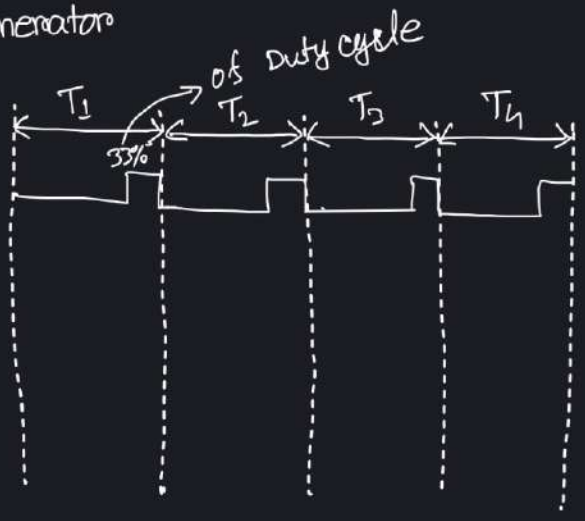
Step 1: Clk generator



## Read data:

Step1: Clk generator




$T_1$:
(i) µp 20 bits address generate करेगा
(ii) ALE=1 (A0-A19)

$T_2$:
Prepares all the control signals
MEM/$\overline{IO}$
$\overline{DEN}$, $\overline{RD}$
$\overline{WR}$, Ready
DT/$\overline{R}$

$T_3$:
Actually reads or writes the data to MEM or I/O (D0-D15)

$T_4$:
All signals go back to default state

Step2: Generate 20 bits address from segment offset.
(S4, S3 → segment Identifier)

Segment Identifier

| MSB S4 | LSB S3 | Segment |
|---|---|---|
| 0 | 0 | ES |
| 0 | 1 | SS |
| 1 | 0 | CS |
| 1 | 1 | DS |

Step3: Now, the address will be placed on the address line (A0-A19) (20 bits)

Step4: ALE=1; actives the latch & stores the 20 bit Address

Step5: The address/Location will be triggered & data communication process will start

Step6: $\overline{DEN}$=0; This will activate the Transreceiver & activate the data lines (D0-D15)

DT/$\overline{R}$
- Data Transfer → µP → (Write)
- Receiver → (Read)

(AD-AD19) DEN, RD WR, Ready DT/R (DO-D15)

Segment Identifier

| MSB S4 | LSB S3 | segment |
|---|---|---|
| 0 | 0 | ES |
| 0 | 1 | SS |
| 1 | 0 | CS |
| 1 | 1 | DS |

Step2: Generate 20 bits address from segment offset:
(S4, S3 → segment Identifier)

Step3: Now, the address will be placed on the address line (AD0-AD19) (20 bits)

Step4: ALE=1; actives the latch & stores the 20 bit Address

Step5: The address/Location will be triggered & data communication process will start

Step6: $\overline{DEN}=0$; This will activate the Transreceiver & activate the data lines (D0-D15)




Step7: All the control signals will be prepared for reading from memory

$\overline{DEN}=0$
$\overline{RD}=0$
$MEM/\overline{I/O}=1$
$\overline{WR}=1$
$DT/\overline{R}=0$
Ready=0 (for slow I/O or memory, the value will be 1)

Step8: Now the actual data (62h) (D0-D7) will be read by the µP through (D0-D15)