Freescale Semiconductor
Application Note

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P2020 QorIQ Integrated Processor Design Checklist

This document provides recommendations for new designs based on the P2020 QorIQ integrated processor. The P2020 combines dual e500v2 processor cores built on Power Architecture® technology with system logic required for networking, wireless infrastructure, and telecommunications applications.

This document may also be useful in debugging newly-designed systems by highlighting those aspects of a design that merit special attention during initial system start-up.

For updates to this document, see the website listed on the last page.

Contents

1 Simplifying the First Phase of Design

This section outlines recommendations to simplify the first phase of design. Before designing a system with a P2020 QorIQ integrated processor, it is recommended that the designer be familiar with the available documentation, software, models, and tools.

1.1 P2020 Block Diagram

Figure 1 shows the major functional units within the device.

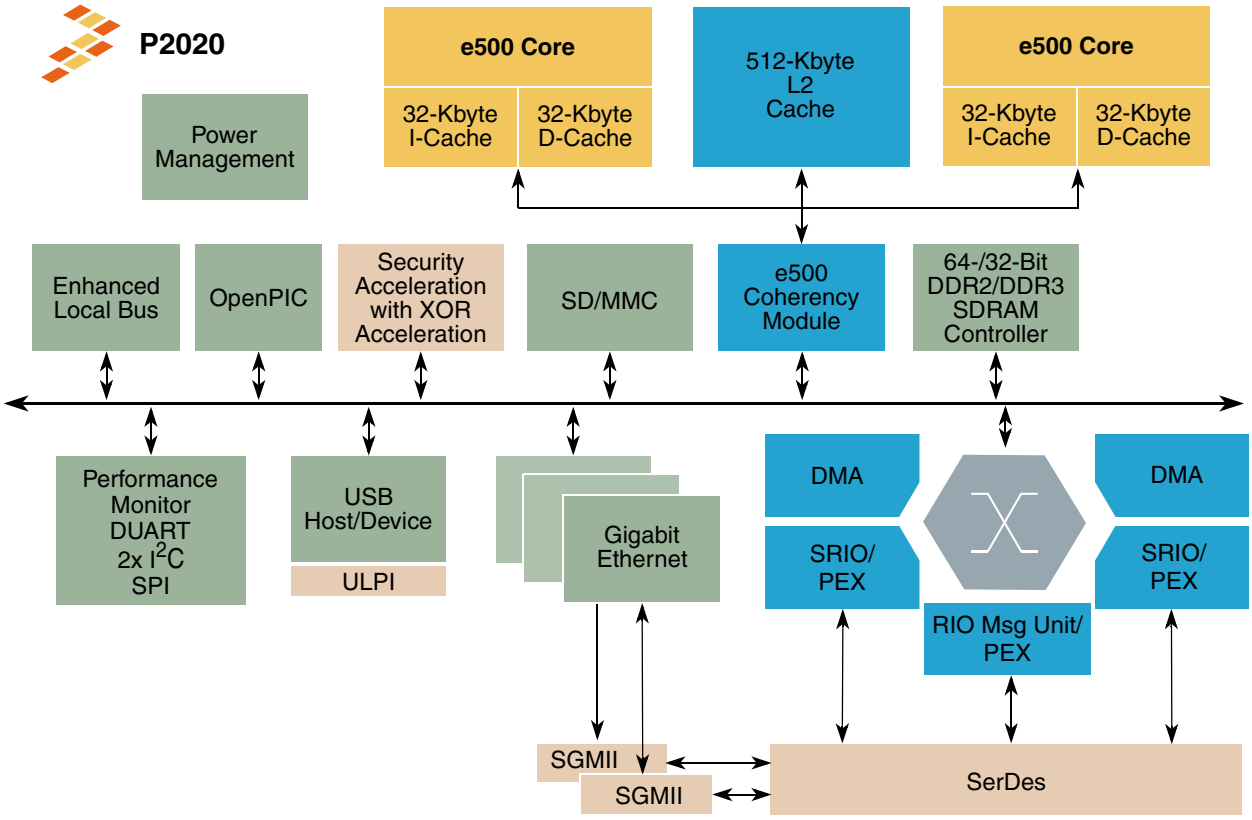


Figure 1. P2020 Block Diagram

1.2 Recommended References

Table 1 lists helpful tools, training resources, and references, some of which may be available only under a non-disclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

Table 1. P2020 Helpful Tools and References

ID	Name	Location
Related Documentation		
P2020RM	*P2020 QorIQ Integrated Host Processor Family Reference Manual*	www.freescale.com

Table 1. P2020 Helpful Tools and References (continued)

ID	Name	Location
P2020RMAD	*Errata to P2020QorIQ Integrated Host Processor Family Reference Manual*	www.freescale.com
P2020CE	*Device Errata for the P2020 QorIQ Integrated Processor*[1]	www.freescale.com
P2020EC	*P2020 QorIQ Integrated Processor Hardware Specifications*	www.freescale.com
AN4309	*PowerQUICC DDR3 SDRAM Controller Register Setting Considerations*	www.freescale.com
AN3369	*PowerQUICC DDR2 SDRAM Controller Register Setting Considerations*	www.freescale.com
AN3939	*DDR Interleaving for PowerQUICC and QorIQ Processors*	www.freescale.com
AN3659	*Booting from On-Chip ROM (eSDHC or eSPI)*	www.freescale.com
AN2910	*Hardware and Layout Design Considerations for DDR2 SDRAM Memory Interfaces*	www.freescale.com
AN3940	*Hardware and Layout Design Considerations for DDR3 SDRAM Memory Interfaces*	www.freescale.com
AN3645	*SEC 2/3x Descriptor Programmer's Guide*	www.freescale.com
AN2919	*Determining the I2C Frequency Divider Ratio for SCL*	www.freescale.com
Software Tools		
I2CBOOTSEQ	Boot sequencer generator tool allows configuration of any memory-mapped register before the completion of power-on reset (POR). The register data to be changed is stored in an I2C EEPROM. The P2020 requires a particular data format for register changes as outlined in the P2020RM. The boot sequencer tool (I2CBOOTSEQ) is a C-code file. When compiled and given a sample data file, it will generate the appropriate raw data format as outlined in the P2020RM. The file that is generated is an s-record file that can be used to program the EEPROM.	Contact your Freescale representative.
LBCUPMIBCG	UPM Programming tool features a GUI for a user-friendly programming interface. It allows programming of all three of the P2020's user-programmable machines. The GUI consists of a wave editor, a table editor, and a report generator. The user can edit the waveform directly or the RAM array directly. At the end of programming, the report generator will print out the UPM RAM array that can be used in a C-program.	Contact your Freescale representative.
Hardware Tools		
P2020DS	Development System including schematics, bill of materials, board errata list, User's Guide, and configuration guide[2]	Contact your Freescale representative.
P2020RDB	Reference Design Board including schematics, bill of materials, board errata list, User's Guide, and configuration guide[2]	Contact your Freescale representative.
Recommended Models		
IBIS	To ensure first-path success, Freescale strongly recommends using the IBIS models for board-level simulations, especially for SerDes and DDR characteristics.	www.freescale.com
BSDL	Use the BSDL files in board verification	www.freescale.com
Flotherm	Use for thermal simulation. Especially without forced cooling or constant airflow, a thermal simulation must not be skipped.	www.freescale.com

Table 1. P2020 Helpful Tools and References (continued)

ID	Name	Location
Training		
—	Our third-party partners are part of an extensive Design Alliance Program. The current training partners can be found on our website under Design Alliance Program at www.freescale.com/alliances. Training material from Freescale Technology Forums are also available. These trainings modules are a valuable resource in understanding the P2020. This material is also available at our website listed on the back cover of this document	—

1 This chip errata document describes the latest fixes and work arounds for the P2020. It is strongly recommended that the chip errata document be thoroughly researched prior to starting a design with the P2020.

2 Design requirements in the device hardware specification and design checklist supersede the design/implementation of the P2020DS or P2020RDB system.

1.3 Product Revisions

Table 2 lists the processor version register (PVR) and system version register (SVR) values for the various P2020 silicon derivatives.

Table 2. P2020 PowerQUICC III Product Revisions

Device Number	Device Revision	e500 v2 Core Revision	Processor Version Register Value	System Version Register Value	Note
P2020	2.0	5.0	0x8021_1050	0x80EA_0020	With Security
P2020	2.0	5.0	0x8021_1050	0x80E2_0020	Without Security
P2020	2.1	5.1	0x8021_1051	0x80EA_0021	With Security
P2020	2.1	5.1	0x8021_1051	0x80E2_0021	Without Security

2 Power Design Considerations

This section provides design considerations for the P2020 power supplies. For information about core and I/O power consummation numbers, and thermal characteristics for the P2020, see the *P2020 QorIQ Integrated Processor Hardware Specifications* (P2020EC).

2.1 PLL Power Supply Filtering

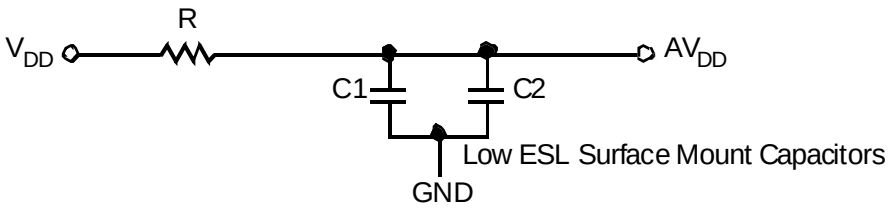
Each of the PLLs is provided with power through independent power supply pins (AVDD_PLAT, AVDD_CORE, AVDD_LBIU, AVDD_DDR, and AVDD_SRDS, respectively). The AVDD level should

always be equivalent to VDD, and these voltages must be derived directly from VDD through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 2, one for each of the AVDD pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

The PLL power supply filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range. It should be built with surface mount capacitors of size 0402 or smaller with minimum effective series inductance (ESL) of less than or equal to 0.5 nH. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AVDD pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AVDD pin, which is on the periphery of 689 WB-TePBGA the footprint, without the inductance of vias.



Notes:
1. R = 5 Ω ¬±5%.
2. C1 = 10 uF ¬± 10%, 0603, X5R with ESL <= 0.5 nH.
3. C2 = 1.0 uF ¬± 10%, 0402 X5R with ESL <= 0.5 nH.

Figure 2. Power Supply Filter Circuit

NOTE

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH).

The AVDD_SRDS signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 3. For maximum effectiveness, the filter circuit is placed as closely as possible to the AVDD_SRDSn balls to ensure it filters out as much noise as possible. The ground connection should be near the AVDD_SRDSn balls. The 0.003-µF capacitor is closest to the balls, followed by two 2.2-µF capacitors, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from

AVDD_SRDSn to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.

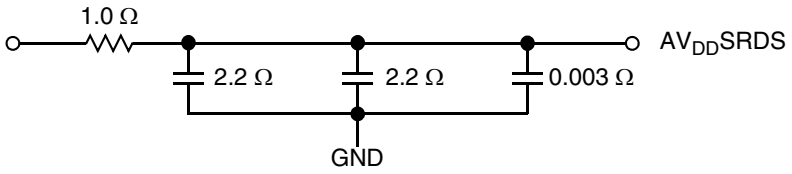


Figure 3. SerDes PLL Power Supply Filter

NOTE

- An 0805 sized capacitor is recommended.
- AVDD-SRDS should be a filtered version of SVDD.
- Signals on the SerDes interface are fed from the XVDD power plane.

CAUTION

These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk.

2.2 Power Supply Decoupling Recommendations

Due to large address and data buses as well as high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the P2020 system, and the device itself requires a clean, tightly regulated source of power.

The recommendations for ensuring a reliable power supply are as follows:

- It is recommended to provide large power planes because immediate charge requirements by the device are always serviced from the power planes first.
- It is recommended that the system designer should place at least one decoupling capacitor at each V_{DD} and B/G/L/O/CV_{DD} pin of the device. These decoupling capacitors should have a value of 0.1 µF and receive their power from separate V_{DD}, B/G/L/O/$CV_{DD,}$ and GND planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.
- These capacitors should have a value of 0.1µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.
- In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the VDD, BVDD, OVDD, CVDD, GVDD, and LVDD planes, to enable quick recharging of the smaller chip capacitors.
- These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary.
- They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

- The capacitors should be placed as close as possible to the processor. The capacitors need to be selected to work well with the power-supply so as to be able to handle the P2020's dynamic load requirements.

2.3 SerDes Block Power Supply Decoupling

If the SerDes module is used, it requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

- Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.
- Board should have at least one 0.1 µF SMT ceramic chip capacitors as close as possible for each supply ball of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- There should be a 10-µF ceramic chip capacitor on the power plane of the SVDD and/or XVDD planes, on the sides of the device where those planes are present. This should be done for all SerDes supplies.

2.4 Power Supplies Checklist

Table 3. Power Supplies Checklist for Designer

Item	Customer Comments	Completed
1. V_{DD}, AV_{DD}_n, XV_{DD}, and SV_{DD} power supplies have a voltage tolerance no greater than 3% from the nominal value. Refer to the hardware specification for more details.		
2. All other power supplies have a voltage tolerance no greater than 5% from the nominal value. Refer to the hardware specification for more details.		
3. Power supply selected is based on MAXIMUM power dissipation. Refer to the hardware specification for more details.		
4. Thermal design is based on THERMAL power dissipation. Refer to the hardware specification for more details.		
5. Power-up sequence is within 50 ms. Refer to the hardware specification for more details.		
6. Recommend using large power planes to the extent possible.		
7. Recommended PLL filter circuit is applied to AV_{DD}_PLAT, AV_{DD}_CORE0, AV_{DD}_CORE1, AV_{DD}_DDR, and AV_{DD}_LBIU.		
8. If SerDes is enabled, the recommended PLL filter circuit is applied to AV_{DD}_SRDS, respectively. Otherwise, a filter is not required.		
9. PLL filter circuits are placed as close to the respective AV_{DD} pin as possible.		
10. Decoupling capacitors of 0.1 µF are placed at each V_{DD}, B/G/L/C/OV_{DD} pin.		

3 Power-on Reset and Reset Configurations

3.1 Configuration and Timing

Various device functions are initialized by sampling certain signals during the assertion of HRESET. These power-on reset (POR) inputs are pulled either high or low during this period. While these pins are generally output pins during normal operation, they are treated as inputs while HRESET is asserted. HRESET must be asserted for a minimum on 100 µs. When HRESET de-asserts, the configuration pins are sampled and latched into registers, and the pins then take on their normal output circuit characteristics.

Most of the configuration pins have an internally gated 20 kΩ nominal pull-up resistor, enabled only during HRESET. For those configurations in which the default state is desired, no external pull-up is required. Otherwise, a 4.7 kΩ pull-down resistor is recommended to pull the configuration pin to a valid logic low level. In cases where a configuration pin has no default, 4.7 kΩ pull-up or pull-down resistors are recommended for appropriate configuration of the pin.

An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device that drives the configuration signals to the P2020 when HRESET is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the de-assertion of HRESET (PLL configuration inputs must meet a 100 µs set-up time to HRESET), hold their values for at least 2 SYSCLK cycles after the de-assertion of HRESET, and then release the pins to high impedance afterward for normal device operation. Refer to the *P2020 Integrated Processor Hardware Specifications* for details about reset initialization timing specifications.

3.2 Configuration Settings

Table 4 summarizes the customer configurable device settings. Refer to the *P2020 QorIQ Integrated Host Processor Family Reference Manual* for a more detailed description of each configuration option.

Table 4. User Configuration Options

Configuration Type	Functional Pins	Comments
CCB Clock PLL Ratio	LA[29:31]	There is no default value for this PLL ratio; these signals must be pulled to the desired value. Refer to the “System PLL Ratio” section in the P2020RM.
e500 Core0 PLL Ratio	LBCTL, LALE, LGPL2/LOE/LFRE	There is no default value for this PLL ratio; these signals must be pulled to the desired value. Refer to the “e500 Core PLL Ratio” section in the P2020RM.
e500 Core1 PLL Ratio	LWE0,UART_SOUT1, READY_P1	There is no default value for this PLL ratio; these signals must be pulled to the desired value. Refer to the “e500 Core PLL Ratio” section in the P2020RM.
DDR Controller Clock PLL Ratio	TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2,	There is no default value for this PLL ratio; these signals must be pulled to the desired value. Refer to the “DDR Controller Clock PLL Ratio” section in the P2020RM.
Boot ROM Location	TSEC1_TXD[6:4], TSEC1_TX_ER	Default: Local Bus GPCM (16-bit ROM)

Table 4. User Configuration Options (continued)

Configuration Type	Functional Pins	Comments
Host/Agent	$\overline{\text{LWE}}$1/$\overline{\text{LBS}}$1,LA[18:19]	Default: P2020 acts as the host processor/root complex for all PCI Express/Serial RapidIO interfaces.
I/O Port Selection	TSEC1_TXD[3:1], TSEC2_TX_ER	Default: PCI Express 1 (×2) (2.5 Gbps) on SerDes lanes [0:1] SGMII eTSEC2 (×1) (1.25 Gbps) on SerDes lane [2] SGMII eTSEC3 (×1) (1.25 Gbps) on SerDes lane [3]
CPU0 Boot Configuration	LA27	There is no default value for CPU boot configuration.
CPU1 Boot Configuration	LA16	There is no default value for CPU boot configuration.
Boot Sequencer	LGPL3/$\overline{\text{LFWP}}$, LGPL5	Default: Boot sequencer is disabled. No I^2C ROM is accessed.
DDR SDRAM Type	TSEC2_TXD1	Default: DDR controller is configured for DDR3.
eTSEC2 SGMII Mode	LGPL1	Default: eTSEC2 Ethernet interface operates in standard parallel interface mode and uses the TSEC2 pins
eTSEC3 SGMII Mode	TSEC_1588_ALARM_OUT2	Default: eTSEC3 Ethernet interface uses parallel interface operates in standard parallel interface mode and uses the TSEC3 muxed pins.
eTSEC1 and eTSEC2 Width	EC_MDC	Default: eTSEC1 and eTSEC2 Ethernet interfaces operate in their standard width TBI, GMII, or MII mode.
eTSEC1 Protocol	TSEC1_TXD0, TSEC1_TXD7	Default: The eTSEC1 controller operates using the TBI protocol (or RTBI if configured in reduced mode).
eTSEC2 Protocol	TSEC2_TXD0, TSEC2_TXD7	Default: The eTSEC2 controller operates using the TBI protocol (or RTBI if configured in reduced mode) if not configured to operate in SGMII mode.
eTSEC3 Protocol	$\overline{\text{UART\_RTS0}}$, UART_RTS1	Default: The eTSEC3 controller operates using the RTBI protocol if not configured to operate in SGMII mode.
SerDes Reference Clock	TSEC_1588_ALARM_OUT1	Default: SerDes expects a 100 MHz reference clock frequency.
RapidIO System Size	LGPL0	Default: Small system size (up to 256 devices)
DDR Speed	LA26	Default: DDR controller clock frequency is greater than or equal to 500 MHz data rate.
Core 0 Speed	LA24	Default: Core 0 clock frequency is greater than 1000 MHz.
Core 1 Speed	LA25	Default: Core 1 clock frequency is greater than 1000 MHz.
Platform Speed	LA23	Default: Platform clock frequency is at or above 333 MHz.
System Speed	LA28	Default: SYSCLK frequency is at or above 66 MHz.
eLBC ECC	MSRCID0	Default: eLBC ECC checking is enabled.

Table 4. User Configuration Options (continued)

Configuration Type	Functional Pins	Comments
Engineering Use POR	LA[20:22], UART_SOUT0, MSRCID1, MSRCID4, DMA1_DDONE	These POR configuration inputs may be used in the future to control functionality. It is advised that boards be built with the ability to pull down these pins.
SerDes PLL Time-out Enable	TRIG_OUT	This configuration allows for the reset sequence to avoid hanging if a SerDes PLL reference clock is not provided. By default the PLL lock-out counter is disabled.
Memory Debug	DMA2_DACK0	Default: Debug information from the DDR SDRAM controller is driven on the MSRCID and MDVAL signals.
SDHC Card Detect Polarity Select	TSEC2_TXD[5]	Default: The eSDHC card-detect polarity is not inverted. Refer to Table 1 footnote 16 in the P2020 hardware specification.
DDR Debug	DMA2_DDONE0	Default: The debug information is not driven on ECC pins. ECC pins function in their normal mode.
General Purpose POR	LAD[0:15]	There is no default value. The general-purpose POR configuration register (GPPORCR) reports the value on LAD[0:15] during POR.

3.3 I/O Supply Voltage Setting

The P2020 is capable of supporting multiple power supply levels on the BV_{DD}, CV_{DD}, and LV_{DD} I/O supplies. Table 5, Table 6, and Table 7 show the encoding used to select the voltage level for each I/O supply.

WARNING

Incorrect voltage select settings can lead to irreversible device damage.

Table 5. Default Voltage Level for LV_{DD}

LV_{DD} VSEL	I/O Voltage Level (V)
0	3.3
1	2.5

Table 6. Default Voltage Level for BV_{DD}

BV_{DD} VSEL [0:1]	I/O Voltage Level (V)
00	3.3
01	2.5
10	1.8
11	3.3

Table 7. Default Voltage Level for CV_{DD}

CV_{DD} VSEL [0:1]	I/O Voltage Level (V)
00	3.3
01	2.5
10	1.8
11	3.3

4 Debug and Test Interface Pin Recommendations

This section discusses the termination of debug and test pins on the device. Table 8 shows how the debug and test pins should be connected.

Table 8. Debug and Test Pin Recommendations

Pin Name	Pin Used	Pin Not Used
ASLEEP	Since these pins have an internal pull-up enabled only at reset, they may be left floating if unconnected. Otherwise, they may need to be driven high (that is, by a PLD) if the device to which they are connected does not release these pins to high impedance during reset.	
MDVAL		
MSRCID[2:3]		
SD_IMP_CAL_RX	This pin must be pulled down through a 200 Ω precision ±1% resistor.	
SD_IMP_CAL_TX	This pin must be pulled down through a 100 Ω precision ±1% resistor.	
SD_PLL_TPA	Do not connect.	
SD_PLL_TPD		
$\overline{\text{SCAN\_MODE}}$	This pin requires a pull up with 1 kΩ to OV_{DD}.	
$\overline{\text{TEST\_SEL}}$	This pin requires a pull up with 4.7 kΩ to OV_{DD} for normal machine operation.	
TRIG_IN	—	Tie low through a 2–10 kΩ resistor to GND.

5 Device Pins and Recommended Test Points

For easier debug, include the pins listed in Table 9 on the board.

Table 9. Recommended Pins for Easier Debug

Test Point Pin	Helps Verify:
CLK_OUT	The various internal clocks, as selected by the CLKOCR register
SYSCLK	Input clock at the device pin
MDVAL and MSRCID[0:4]	Memory debug signals
TRIG_OUT	The end of the reset sequence
ASLEEP	The end of the reset sequence
TRIG_OUT/READY0	Verify the end of the reset sequence for Core 0

Table 9. Recommended Pins for Easier Debug

Test Point Pin	Helps Verify:
READY_P1	Verify the end of the reset sequence for Core 1
CKSTP_OUT	Core checkstop indication
HRESET_REQ	Proper boot sequencer functions and reset requests

6 Clock Pin Recommendations

The clock inputs for the P2020 are:

- EC_GTX_CLK125
- USB_CLK
- RTC
- SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$
- SYSCLK
- DDRCLK (for asynchronous mode)

The EC_GTX_CLK125 input is used by the eTSEC controller as a reference clock for gigabit Ethernet modes. SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are the reference clocks for PCI-Express and SGMII operating modes. SYSCLK is the primary clock input to the device. Table 10 shows how the clock pins should be connected.

Table 10. Clock Pin Recommendations

Pin Name	Pin Used	Pin Not Used
EC_GTX_CLK125	If any of the eTSECs are used in gigabit mode, connect it to a 125 MHz clock.	Pull high or low through a 2–10 kΩ resistor to LV_{DD} or GND, respectively.
DDRCLK	DDRCLK input is only required when the DDR controller is running in asynchronous mode. When running in asynchronous mode the same input oscillator can be used for both SYSCLK and DDRCLK.	It is recommended to tie this signal off to GND when the DDR controller is configured for synchronous mode (POR setting cfg_ddr_pll[0:2] = 111).
RTC	The default source of the time base is the CCB clock divided by eight. For more details, see the *PowerPC e500 Core Complex Reference Manual*.	Pull high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
SD_REF_CLK/ SD_REF_CLK	If the SerDes is enabled at POR, connect these pins to the appropriate input clock frequency as specified by the I/O port selection POR pins.	These pins must be connected to GND.
SYSCLK	This pin must always be connected to an input clock of 66–100 MHz.	
CLK_OUT	If clock out is enabled, the CLK_OUT signal is driven according to CLKOCR[CLK_SEL]. **Note:** CLK_OUT is for monitoring purposes only, not for clocking other devices.	This pin may be left unconnected. CLK_OUT signal is tristated.

6.1 System Clocking

This device includes six PLLs:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 6.1.3, “CCB/SYSCLK PLL Ratio.”
- The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 6.1.4, “e500 Core PLL Ratio.”
- The enhanced local bus PLL generates the clock for the enhanced local bus.
- There is one PLL for the SerDes block.
- There is one PLL for the DDR for asynchronous operation.

6.1.1 Clock Ranges

Table 11 provides the clocking range for the processor cores, platform, memory, and enhanced local bus.

Table 11. Processor Clocking Range

Characteristic	Processor Core Frequency						Unit	Notes
	800 MHz		1000 MHz		1200 MHZ			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	533	800	533	1000	533	1200	MHz	1, 2
Platform/CCB clock frequency	266	400	266	500	266	600	MHz	1
Memory bus clock frequency	200	400	200	400	200	400	MHz	3
Enhanced local bus clock frequency	16.63	100	16.63	125	16.63	150	MHz	4
Security engine (SEC) clock frequency	133	200	133	250	133	300	MHz	5

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 6.1.3, “CCB/SYSCLK PLL Ratio,” and Section 6.1.4, “e500 Core PLL Ratio,” for ratio settings.
2. The minimum e500 core frequency is based on the minimum platform frequency of 266 MHz.
3. The memory bus speed is half of the DDR2/DDR3 data rate.
4. The local bus clock speed on LCLK[0:1] is determined by the platform clock divided by the local bus ratio programmed in LCRR[CLKDIV]. See the P2020RM for more information.
5. Security engine (SEC) clock frequency equal to CCB/2

6.1.2 DDR Clocking Range

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL. Table 12 provides the clocking specifications for the memory bus.

Table 12. Memory Bus Clocking Range

Characteristic	Min	Max	Unit	Notes
DDR2 memory bus clock speed	200	333	MHz	1, 2, 3, 4
DDR3 memory bus clock speed	333	400	MHz	1, 2, 3, 4

Notes:
1. Caution: The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 6.1.3, "CCB/SYSCLK PLL Ratio," Section 6.1.4, "e500 Core PLL Ratio," and Section 6.1.5, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. The memory bus clock refers to the P2020 memory controllers' MCK[0:5] and MCK[0:5] output clocks, running at clock frequencies that are half of the DDR data rate.
3. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform frequency. If the desired DDR data rate is higher than the platform frequency, asynchronous mode must be used.
4. In asynchronous mode, the memory bus clock speed is dictated by its own PLL. The memory bus clock frequency must be less than or equal to the platform clock frequency. See Section 6.1.5, "DDR/DDRCLK PLL Ratio."

6.1.3 CCB/SYSCLK PLL Ratio

The CCB clock, also called the platform clock, is the clock that drives the e500 core complex bus (CCB). The frequency of the CCB is set using the following reset signals, as shown in Table 13:

- SYSCLK input signal
- Binary value on LA[29:31] at power up

NOTE

There is no default value for this CCB/SYSCLK PLL ratio. The following signals must be pulled to the desired values for specified CCB/SYSCLK PLL ratio.

Table 13. CCB Clock Ratio

Binary Value of LA[29:31] Signals	CCB:SYSCLK Ratio
000	4:1
001	5:1
010	6:1
011	8:1
100	Reserved
101	Reserved

Table 13. CCB Clock Ratio (continued)

Binary Value of LA[29:31] Signals	CCB:SYSCLK Ratio
110	Reserved
111	Reserved

6.1.4 e500 Core PLL Ratio

Table 14 and Table 15 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock for Core 0 and Core 1. This ratio is determined by the binary value of LBCTL, LALE, and LGPL2 at power up for Core 0 and by the binary value of the $\overline{\text{LWE}}$[0], UART_SOUT[1], and READY_P1 signals for Core 1.

Table 14. e500 Core 0 to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core: CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core: CCB Clock Ratio
000	4:1	100	2:1
001	9:2(4.5:1)	101	5:2
010	1:1	110	3:1
011	3:2	111	7:2

Table 15. e500 Core 1 to CCB Clock Ratio

Binary Value of $\overline{\text{LWE}}$[0], UART_SOUT[1], READY-P1 Signals	e500 core: CCB Clock Ratio	Binary Value of $\overline{\text{LWE}}$[0], UART_SOUT[1], READY-P1 Signals	e500 core: CCB Clock Ratio
000	4:1	100	2:1
001	9:2(4.5:1)	101	5:2
010	1:1	110	3:1
011	3:2	111	7:2

6.1.5 DDR/DDRCLK PLL Ratio

The DDR memory controller complex can be synchronous with, or asynchronous to, the CCB depending on configuration.

Table 16 describes the clock ratio between the DDR memory controller complex and the DDR input clock.

When synchronous mode is selected, the memory buses are clocked at half the CCB clock rate. The default mode of operation is the synchronous mode. The DDRCLKDR configuration register in the global utilities block allows the DDR controller to be run in a divided down mode where the DDR bus clock is half the

speed of the default configuration. Changing these defaults must be completed prior to initialization of the DDR controller.

Table 16. DDR Clock Ratio

Binary Value of TSEC_1588_CLK_Out, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 Signals	DDR:DDRCLK Ratio
001	4:1
010	6:1
011	8:1
100	10:1
101	12:1
111	Synchronous mode (DDR data rate = CCB clock)

6.2 Frequency Options

This section discusses the frequency options.

6.2.1 Core to CCB Frequency Options

Table 17 shows the expected core frequency values for specific core to CCB frequency ratio options.

Table 17. Frequency Options for e500 Core Frequency

Core to CCB Ratio	Platform/CCB Frequency (MHz)					
	266	333	400	500	533	600[1]
	Core Frequency (MHz)					
1:1	—	—	—	—	533	600
1.5:1	—	—	600	750	800	900
2:1	533	666	800	1000	1067	1200
2.5:1	666	833	1000			
3:1	800	1000	1200			
3.5:1	933	1167				
4:1	1067					
4.5:1	1200					

Notes:1.The 600 MHz CCB is limited to products that support 1200 MHz core speed.

6.2.1.1 Platform to SYSCLK Frequency Options

Table 18 shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

Table 18. Frequency Options for Platform Frequency

Platform: SYSCLK Ratio	SYSCLK (MHz)			
	64	66.66	83	100
	Platform/CCB Frequency (MHz)[1]			
4:1	—	266	332	400
5:1	320	333	415	500
6:1	384	400	500	600
8:1	512	533		

6.2.1.2 DDRCLK to DDR controller operating Frequency Options

Table 19 shows the expected frequency values for the DDR controller operating frequency when using an external asynchronous clock.

Table 19. DDRCLK to DDR Controller Frequency (Data Rate)

DDRC to DDRCLK Ratio	DDRCLK (MHz)	
	66.66	100
	DDR Controller Data Rate Frequency (MHz)	
4		400
6	400	600
8	533	800
10	667	—
12	800	—

6.3 Minimum Platform Frequency Requirements for High-Speed Interfaces

The “I/O Port Selection” section of the *P2020 QorIQ Integrated Host Processor Family Reference Manual* describes various high-speed interface configuration options. Note that the CCB clock frequency must be considered for proper operation of such interfaces as described below.

For proper PCI Express operation, the CCB clock frequency must be greater than:

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

See the “Link Width” section of the *P2020 QorIQ Integrated Host Processor Family Reference Manual* for PCI Express interface width details. Note that the ‘PCI Express link width’ in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection. See the “System PLL Ratio” section of the *P2020 QorIQ Integrated Host Processor Family Reference Manual* for details of selecting this ratio.

For proper serial RapidIO operation, the platform clock frequency must be greater than or equal to:

$$\frac{2 \times (0.8512) \times (\text{Serial RapidIO interface frequency}) \times (\text{Serial RapidIO link width})}{64}$$

7 DDR Interface Pin Recommendations

This section discusses the termination of DDR pins on the device. Table 20 shows how the DDR pins should be connected.

Table 20. DDR Pin Recommendations

Pin Name	Pin Used	Pin Not Used
MA[0:15]	Auto-precharge for DDR signaled on MA10 when DDR_SDRAM_CFG[PCHB8] = 0. Auto-precharge for DDR signaled on MA8 when DDR_SDRAM_CFG[PCHB8] = 1.	These pins may be left unconnected.
MBA[0:2]	Connect to memory module or discrete memory	These pins may be left unconnected.
MCAS	Connect to memory module or discrete memory	These pins may be left unconnected.
MCK/$\overline{\text{MCK}}$[0:5]	Unused MCK pins must be disabled via DDRCLKDR register.	These pins may be left unconnected. However, all unused MCK pins should be disabled via DDRCLKDR[DDR_MCKx_DIS] register at offset 0xE_0B28.
MCKE[0:3]	These pins are actively driven during reset instead of being released to high impedance.	These pins may be left unconnected.
MCS[0:3]	—	These pins may be left unconnected.
$\overline{\text{MAPAR\_ERR}}$	—	These pins should be pulled high or low via a 2–10 kΩ resistor.
MAPAR_OUT	—	These pins may be left unconnected.
MDIC[0:1]	For DDR2, MDIC[0] is grounded through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor, and MDIC[1] is connected to GVDD through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs. The calibration resistor value for DDR3 should be 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode).	
MDM[0:8]	—	These pins may be left unconnected.
MDQ[0:63]	—	
MDQS[0:8] / MDQS[0:8]	—	
MECC[0:7]	—	These pins should be pulled high or low via 8 individual 2–10 kΩ resistors. Do not connect to a common pull up.

Table 20. DDR Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
MODT[0:3]	—	These pins may be left unconnected.
MRAS	—	
$\overline{\text{MCAS}}$	—	
MWE	—	
MVREF	DDR Reference Voltage: 0.49 × GVDD to 0.51 × GVDD. MVREF can be generated using a divider from GVDD as MVREF. Another option is to use supplies that generate GVDD, VTT, and MVREF voltage. These methods help reduce differences between GVDD and MVREF. MVREF generated from a separate regulator is not recommended as MVREF will not track GVDD as closely.	

8 DMA Interface Pin Recommendations

This section discusses the termination of DMA pins on the device. Table 21 shows how the DMA pins should be connected.

Table 21. DMA Pin Recommendations

Pin Name	Pin Used	Pin Not Used
$\overline{\text{DMA1\_DACK}}$	This pin must NOT be pulled down during power-on reset.	If this pin is not used, it may be left floating.
$\overline{\text{DMA2\_DACK}}$	This pin is a reset configuration pin that sets the device derivative. This pin requires a 4.7 kΩ pull-up or pull-down resistor.	If this pin is not used, it may be left floating.
$\overline{\text{DMA1\_DREQ}}$	—	If this pin is not used, it should be pulled up with a 4.7–10 kΩ resistor.
$\overline{\text{DMA2\_DREQ}}$	—	
$\overline{\text{DMA1\_DDONE}}$	Spare POR pin. The spare POR configuration input may be used in the future to control functionality. It is advised that boards be built with the ability to pull up or pull down	If this pin is not used, it may be left floating.
$\overline{\text{DMA2\_DDONE}}$	This pin is a reset configuration pin that sets the device derivative. This pin requires a 4.7 kΩ pull-up or pull-down resistor.	

9 DUART Interface Pin Recommendations

This section discusses the termination of DUART pins on the device. Table 22 shows how the DUART pins should be connected.

Table 22. DUART Pin Recommendations

Pin Name	Pin Used	Pin Not Used
$\overline{\text{UART0\_CTS}}$	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{UART1\_CTS}}$	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{UART0\_RTS}}$	This pin is a reset configuration pin that sets the device derivative. These pins require 4.7 kΩ pull-up or pull-down resistors.	This output pin may be left floating.
$\overline{\text{UART1\_RTS}}$		This output pin may be left floating.
UART0_SIN	—	Tie low through a 2–10 kΩ resistor to GND.
UART1_SIN	—	Tie low through a 2–10 kΩ resistor to GND.
UART0_SOUT	—	This output pin may be left floating.
UART1_SOUT	The value of this pin at reset sets the e500 core clock to the CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 6.1.4, “e500 Core PLL Ratio.”	This output pin may be left floating.

10 eSDHC Interface Pin Recommendations

This section discusses the termination of eSDHC pins on the device. Table 23 shows how the eSDHC pins should be connected.

Table 23. eSDHC Pin Recommendations

Pin Name	Pin Used	Pin Not Used
SDHC_DAT[0:2]	10–100 kΩ pull-up resistor if used	—
SDHC_DAT[03]	100-kΩ pull down needed if SDHC_DAT3 signal is used as a CD pin for SD cards. The 100-kΩ pull down is not needed for MMC cards or if SDHC_CD is used for card detection.	
$\overline{\text{SPI\_CS}}$[00]/SDHC_DAT[4]	10–100 kΩ pull-up resistor if used	—
$\overline{\text{SPI\_CS}}$[01]/SDHC_DAT[5]	10–100 kΩ pull-up resistor if used	—
$\overline{\text{SPI\_CS}}$[02]/SDHC_DAT[6]	10–100 kΩ pull-up resistor if used	—
$\overline{\text{SPI\_CS}}$[03]/SDHC_DAT[7]	10–100 kΩ pull-up resistor if used	—
GPIO[08]/$\overline{\text{SDHC\_CD}}$	When eSDHC controller is not used, $\overline{\text{SDHC\_CD}}$ and SDHC_WP are GPIO configured as outputs. Thus, no termination is needed.	
GPIO[09]/SDHC_WP		

11 eSPI Interface Pin Recommendations

This section discusses the termination of eSPI pins on the device. Table 24 shows how the eSPI pins should be connected.

Table 24. eSPI Pin Recommendations

Pin Name	Pin Used	Pin Not Used
SPI_MISO	Connect as needed.	Connect through a 2–10 kΩ to CVDD.
SPI_MOSI	Connect as needed.	Connect through a 2–10 kΩ to CVDD.
$\overline{\text{SPI\_CS}}$[0]/SDHC_DATA[04]	Connect as needed.	Connect through a 2–10 kΩ to CVDD.
$\overline{\text{SPI\_CS}}$[1]/SDHC_DATA[05]	Connect as needed.	Output pin may be left floating.
$\overline{\text{SPI\_CS}}$[02]/SDHC_DATA[06]	Connect as needed.	
$\overline{\text{SPI\_CS}}$[03]/SDHC_DATA[07]	Connect as needed.	
SPI_CLK	Connect as needed	Connect through 1 kΩ GND.

12 USB Interface Pin Recommendations

This section discusses the termination of USB pins on the device. Table 25 shows how the USB pins should be connected.

Table 25. USB Pin Recommendations

Pin Name	Pin Used	Pin Not Used
USB_NXT	Connect as needed.	Connect through 1 kΩ GND.
USB_DIR	Connect as needed.	Connect through 1 kΩ GND.
USB_STP	Connect as needed.	Output pin may be left floating. Note: This pin must not be pulled down during power-on reset.
USB_PWRFAULT	Connect as needed.	Connect through 1 kΩ GND.
USB_CLK	Connect as needed.	Connect through 1 kΩ GND.
USB_D[0:7]	Connect as needed.	Connect through 1 kΩ GND.
GPIO[10]/USB_PCTL0	Configured via PMUXCR at offset 0xE_0060; Exposes USB_PCTL0 signal used for host-mode USB port status indication. Default: the pin retains its primary function as GPIO.	When the USB controller is not used, USB_PCTL0 and USB_PCTL1 are a GPIO configured as output. Thus, no termination is needed.
GPIO[11]/USB_PCTL1	Configured via PMUXCR at offset 0xE_0060; Exposes USB_PCTL1 signal used for host-mode USB port status indication. Default: the pin retains its primary function as GPIO.	

13 Ethernet Management Interface Pin Recommendations

This section discusses the termination of the Ethernet management pins on the device. Table 26 shows how the Ethernet management pins should be connected.

Table 26. Ethernet Management Pin Recommendations

Pin Name	Pin Used	Pin Not Used
EC_MDC	This pin is a reset configuration pin. It has a weak internal pull-up that is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
EC_MDIO	—	Tie high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.

14 eTSEC Interface Pin Recommendations

This section discusses the termination of the Ethernet pins on the device. Table 27 shows how the Ethernet pins should be connected.

Table 27. Ethernet Pin Recommendations

Pin Name	Pin Used	Pin Not Used
TSEC1_COL/TSEC3_RX_CLK	—	Tie low through a 2–10 kΩ resistor to GND.
TSEC2_COL/TSEC3_TX_CLK	—	
TSEC1_CRS/TSEC3_RX_DV	—	
TSEC2_CRS/TSE3_RX_ER	—	
TSEC1_GTX_CLK	—	These output pins may be left floating.
TSEC2_GTX_CLK	—	
TSEC1_RX_CLK	—	Tie high or low through a 2–10 kΩ resistor to LV_{DD} or GND, respectively
TSEC2_RX_CLK	—	
TSEC1_RX_DV	—	Tie low through a 2–10 kΩ resistor to GND.
TSEC2_RX_DV	—	
TSEC1_RX_ER	—	
TSEC2_RX_ER	—	
TSEC1_RXD[7:0]	—	Tie high or low through a 2–10 kΩ resistor to LVDD or GND, respectively.
TSEC2_RXD[7:0]	—	Tie high or low through a 2–10 kΩ resistor to LVDD or GND, respectively.
TSEC1_TX_CLK	—	Tie high or low through a 2–10 kΩ resistor to LV_{DD} or GND, respectively
TSEC2_TX_CLK	—	

Table 27. Ethernet Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
TSEC1_TX_EN	These pins require an external 4.7 kΩ pull-down resistor to prevent the PHY from seeing a valid Transmit Enable before it is actively driven (during reset).	These output pins may be left floating.
TSEC2_TX_EN		
TSEC1_TX_ER	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
TSEC2_TX_ER		
TSEC1_TXD[07]/TSEC3_TXD[03]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
TSEC1_TXD[06]/TSEC3_TXD[02]		
TSEC1_TXD[05]/TSEC3_TXD[01]		
TSEC1_TXD[04]/TSEC3_TXD[00]		
TSEC1_TXD[03]		
TSEC1_TXD[02]		
TSEC1_TXD[01]		
TSEC1_TXD[00]		
TSEC2_TXD[07]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled only when the processor is in the reset state.	This output pin may be left floating.
TSEC2_TXD[06]	Must NOT be pulled down during power-on reset.	
TSEC2_TXD[05]/TSEC3_TX_EN	TSEC2_TXD[05] is a POR configuration pin for eSDHC card-detect (cfg_sdhc_cd_pol_sel) and also has an alternate function as TSEC3_TX_EN. When using eTSEC3 as a parallel interface, the TSEC3_TX_EN requires a pull down. However, because the pull-down resistor on TSEC2_TXD[05]/TSEC3_TX_EN signal causes the eSDHC card-detect (cfg_sdhc_cd_pol_sel) to be inverted, the inversion should be overridden from the SDHCDCR [CD_INV] debug control register.	This output pin may be left floating.
TSEC2_TXD[04]/TSEC3_GTX_CLK	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	This output pin may be left floating.
TSEC2_TXD[03]		
TSEC2_TXD[02]		
TSEC2_TXD[01]	TSEC2_TXD[01] is used as cfg_dram_type. It must be valid at power up, even before HRESET assertion.	
TSEC2_TXD[00]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled only when the processor is in the reset state.	This output pin may be left floating.

15 I^2C Interface Pin Recommendations

This section discusses the termination of I^2C pins on the device. Table 28 shows how the I^2C pins should be connected.

Table 28. I^2C Pin Recommendations

Pin Name	Pin Used	Pin Not Used
IIC1_SCL	Tie these open-drain signals high through a nominal 1 kΩ resistor to OV_{DD}. Optimum pull-up value depends on the capacitive loading of external devices and required operating speed.	Tie high through a 2–10 kΩ resistor to OV_{DD}.
IIC2_SCL		
IIC1_SDA		
IIC2_SDA		

16 JTAG Interface Pin Recommendations

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 5. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions, as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged along with these signals with logic.

The arrangement shown in Figure 5 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 4, for connection to the target system. This header is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header, so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right whereas others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 4 is common to all known emulators.

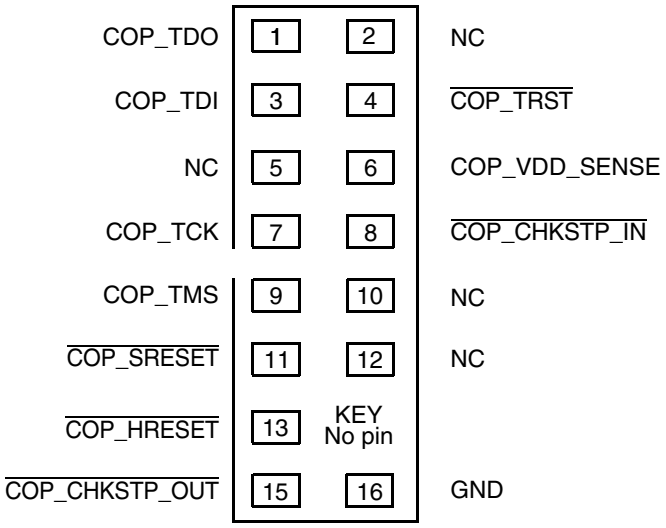
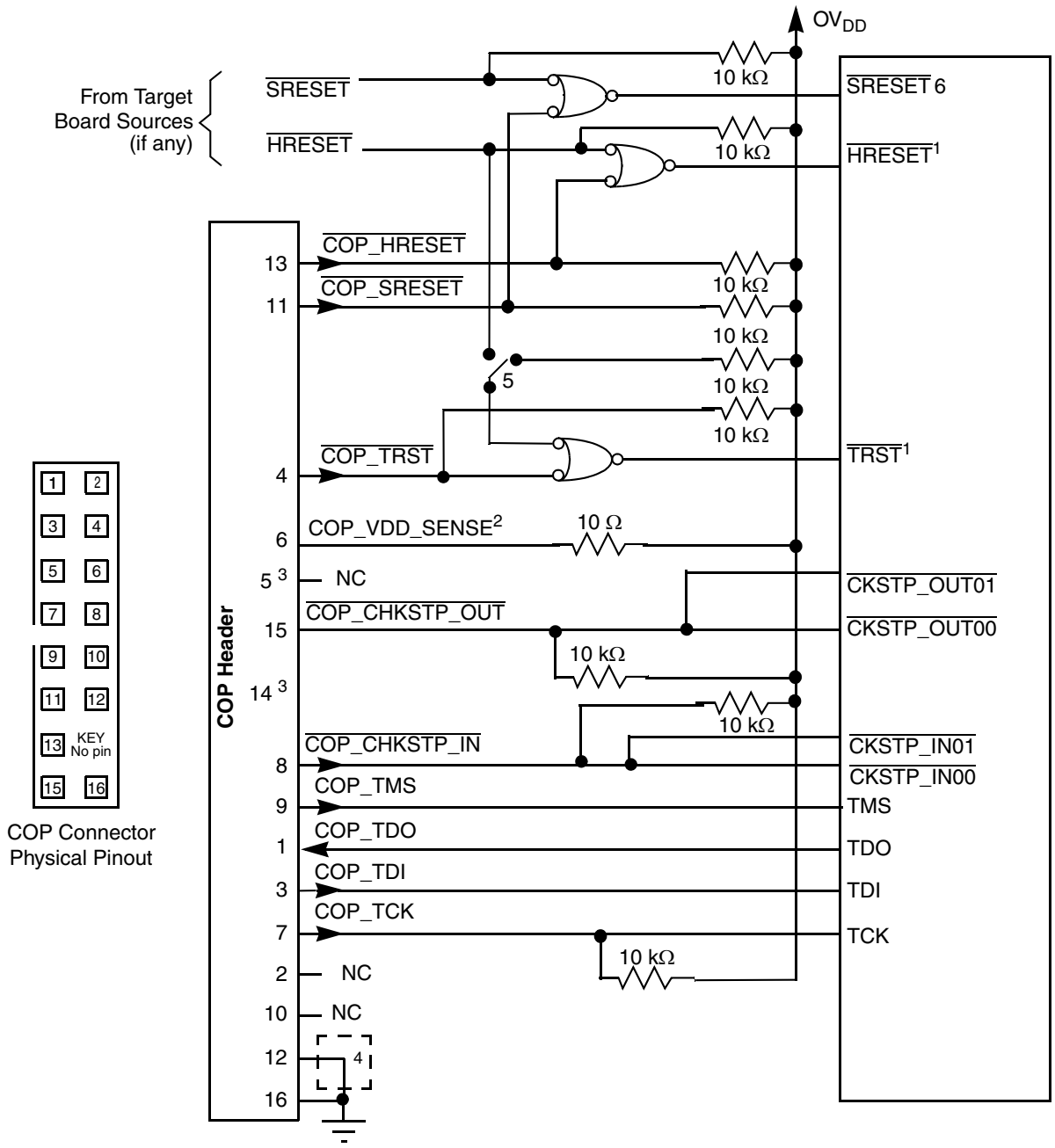


Figure 4. COP Connector Physical Pinout (Top View)



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10–Ω (1/6W rating; 0402 or larger) resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 5. JTAG Interface Connection

16.1 JTAG Pin Recommendations

If the JTAG interface and COP header are not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 5. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, or TDO.

Table 29 shows how the JTAG pins should be connected.

Table 29. JTAG Pin Recommendations

Pin Name	Pin Used	Pin Not Used
TCK	If COP is used, connect as needed and strap to OVDD via a 10 kΩ pull up.	If COP is unused, tie TCK to OVDD through a 10 kΩ resistor. This prevents TCK from changing state and reading incorrect data into the device.
TDI	This pin has a weak internal pull-up P-FET that is always enabled. Connect to Pin3 of the COP connector.	This pin may be left unconnected.
TDO	Connect to Pin1 of the COP connector.	This pin may be left unconnected.
TMS	This pin has a weak internal pull-up P-FET that is always enabled. Connect to Pin9 of the COP connector.	This pin may be left unconnected.
$\overline{\text{TRST}}$	Connect as shown in Figure 5.	$\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω resistor.

17 eLBC Interface Pin Recommendations

This section discusses the termination of local bus pins on the device. Table 30 shows how the local bus pins should be connected.

Table 30. Local Bus Pin Recommendations

Pin Name	Pin Used	Pin Not Used
LA[16]	The value of LA[27] and LA[16] during reset is used to determine CPU boot configuration. This pin requires a 4.7-kΩ pull-up or pull-down resistor.	
LA[17]	Must NOT be pulled down during power-on reset	This output pin may be left floating.
LA[18]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
LA[19]		
LA[20]	Spare POR pin. The spare POR configuration inputs may be used in the future to control functionality. It is advised that boards be built with the ability to pull up or pull down.	If the POR default is acceptable, this output pin may be left floating.
LA[21]		
LA[22]		

Table 30. Local Bus Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
LA[23]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
LA[24]		
LA[25]		
LA[26]		
LA[27]	The value of LA[27]and LA[16] during reset is used to determine CPU boot configuration. These pins require 4.7-kΩ pull-up or pull-down resistors.	
LA[28]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
LA[29:31]	The value of LA[29:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 6.1.3, "CCB/SYSCLK PLL Ratio."	
LAD[0:15]	These pins are reset configuration pins. They have a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.The value of LAD[0:15] during reset sets the upper 16 bits of the GPPORCR	Tie high or low through a 2–10 kΩ resistor to BV_{DD} or GND, respectively, if the general purpose POR configuration is not used.
LALE	This pin is a reset configuration pin that sets the e500 core clock to CCB Clock PLL ratio. These pins require 4.7 kΩ pull-up or pull-down resistors. To meet the setup and hold time of LALE and LAD, insure LALE arrives at least 500ps before LAD data.	
LBCTL	This pin is a reset configuration pin that sets the e500 core clock to CCB Clock PLL ratio. These pins require 4.7 kΩ pull-up or pull-down resistors.	
LCLK[0:1]	—	These output pins may be left floating.
$\overline{\text{LCS}}$[0:4]	If this pin is configured for local bus controller use, recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to BVDD, to ensure no random chip select assertion due to possible noise and etc.	If the DMA functions of these pins are not used, these output pins may be left floating.
$\overline{\text{LCS}}$[05]/$\overline{\text{DMA2\_DREQ}}$[01]		
$\overline{\text{LCS}}$[06]/$\overline{\text{DMA2\_DACK}}$[01]		
$\overline{\text{LCS}}$[07]/$\overline{\text{DMA2\_DDONE}}$[01]		
LGPL[00]/LFCLE	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR defaults are acceptable, these output pins may be left floating.
LGPL[01]/LFALE		
LGPL[02]/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	This pin is a reset configuration pin that sets the e500 core clock to CCB Clock PLL ratio. These pins require 4.7 kΩ pull-up or pull-down resistors.	
LGPL[03]/$\overline{\text{LFWP}}$	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
LGPL[04]/$\overline{\text{LGTA}}$/LFRB/ LUPWAIT	— This pin should be pulled up whether used or not used.	
LGPL[05]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.

Table 30. Local Bus Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
LSYNC_IN	LSYNC_IN needs to be connected via a trace to LSYNC_OUT of length equal to the longest LCK*n* signal used.	LSYNC_IN needs to be directly connected to LSYNC_OUT.
LSYNC_OUT		
$\overline{\text{LWE[00]}}$	This pin is a reset configuration pin that sets the e500 core clock to CCB Clock PLL ratio. These pins require 4.7 kΩ pull-up or pull-down resistors.	—
$\overline{\text{LWE[01]}}$	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR defaults are acceptable, these output pins may be left floating.

18 PIC Interface Pin Recommendations

This section discusses the termination of programmable interrupt controller pins on the device. Table 31 shows how the PIC pins should be connected.

Table 31. PIC Pin Recommendations

Pin Name	Pin Used	Pin Not Used
IRQ[0:6]	A weak pull-up or pull-down may be needed to the inactive state.	Tie high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively,
GPIO[00]/IRQ[07]	When using one of these shared GPIO/IRQ pins as an external IRQ, the user cannot use the associated pin as GPIO. The user must keep the default GPIO input direction and ignore the state of GPDAT for the associated pin.	
GPIO[01]/IRQ[08]		
GPIO[02]/IRQ[09]		
GPIO[03]/IRQ[10]		
GPIO[04]/IRQ[11]		
$\overline{\text{IRQ\_OUT}}$	Pull high through a 2–10 kΩ resistor to OV_{DD}.	This output pin may be left floating.
$\overline{\text{MCP0}}$[0:1]	Pull high through a 2–10 kΩ resistor to OV_{DD}.	
$\overline{\text{UDE0}}$[0:1]		

19 GPIO Interface Pin Recommendations

This section discusses the termination of general purpose input/output (GPIO) pins on the device. Table 32 shows how the GPIO pins should be connected.

Table 32. GPIO Pin Recommendations

Pin Name	Pin Used	Pin Not Used
GPIO[00]/IRQ[07]	When using one of these shared GPIO/IRQ pins as GPIO, the user must keep the associated IRQ masked in the PIC. Note that these external IRQs are masked in the PIC by default.	Pull high through a2–10 kΩ to OV_{DD} or leave floating and configured as outputs via the GPIO direction register (GPDIR).
GPIO[01]/IRQ[08]	—	
GPIO[02]/IRQ[09]	—	
GPIO[03]/IRQ[10]	—	
GPIO[04]/IRQ[11]	—	
GPIO[5:7]	—	
GPIO[08]/$\overline{\text{SDHC\_CD}}$	When the eSDHC controller is not used, $\overline{\text{SDHC\_CD}}$ and SDHC_WP are GPIOs configured as output. Thus, no termination is needed.	Pull high through a 2–10kΩ to BV_{DD} or leave floating and configured as outputs via the GPIO direction register (GPDIR).
GPIO[09]/SDHC_WP	Configured via PMUXCR at offset 0xE_0060; Exposes USB_PCTL0 signal used for host-mode USB port status indication. Default: the pin retains its primary function as GPIO.	
GPIO[10]/USB_PCTL0		
GPIO[11]/USB_PCTL1	Configured via PMUXCR at offset 0xE_0060; Exposes USB_PCTL1 signal used for host-mode USB port status indication. Default: the pin retains its primary function as GPIO.	
GPIO[12:15]	—	

20 SerDes Interface Pin Recommendations

This section discusses the termination of SerDes pins on the device. Table 33 shows how the SerDes pins should be connected. Note that the SerDes must always have power applied to its supply pins. SerDes pins are used to interface to the PCI Express, serial RapidIO, and SGMII interfaces.

Table 33. SerDes Pin Recommendations

Pin Name	Pin Used	Pin Not Used
SD_RX[0:3]	—	These pins must be connected to GND.
$\overline{\text{SD\_RX}}$[0:3]		
SD_TX[0:3]	—	These pins must be left unconnected (float).
$\overline{\text{SD\_TX}}$[0:3]		

Table 33. SerDes Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
SD_REF_CLK	—	These pins must be connected to GND.
$\overline{\text{SD\_REF\_CLK}}$		

20.1 HSSI System Design Information

This section provides electrical and thermal design recommendations for successful application of the P2020.

20.1.1 Interfacing With Other Differential Signaling Levels

Note the following prior to interfacing with other differential signaling levels:

- With on-chip termination to SGND_SRDSn (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used, but they may need to be AC-coupled due to the limited common mode input range allowed for DC-coupled connection (100–400 mV).
- LVPECL outputs can produce signals with too large of an amplitude. In addition to being AC-coupled, they may need to be DC-biased at the clock driver output first, then series terminated with a resistor to reduce the amplitude.

NOTE

Figure 6 to Figure 9 below are for conceptual reference only. Due to the fact that the internal structure, output impedance, and termination requirements are different among various clock driver manufacturers, it is possible that the clock circuit reference designs provided by clock driver chip vendor may be different from what is shown below. They may also vary from one vendor to another. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits based on the SerDes reference clock receiver requirement provided in this document.

Figure 6 shows the SerDes reference clock connection reference circuits for the HCSL-type clock driver. It assumes that the DC levels of the clock driver chip is compatible with the SerDes reference clock input's DC requirement.

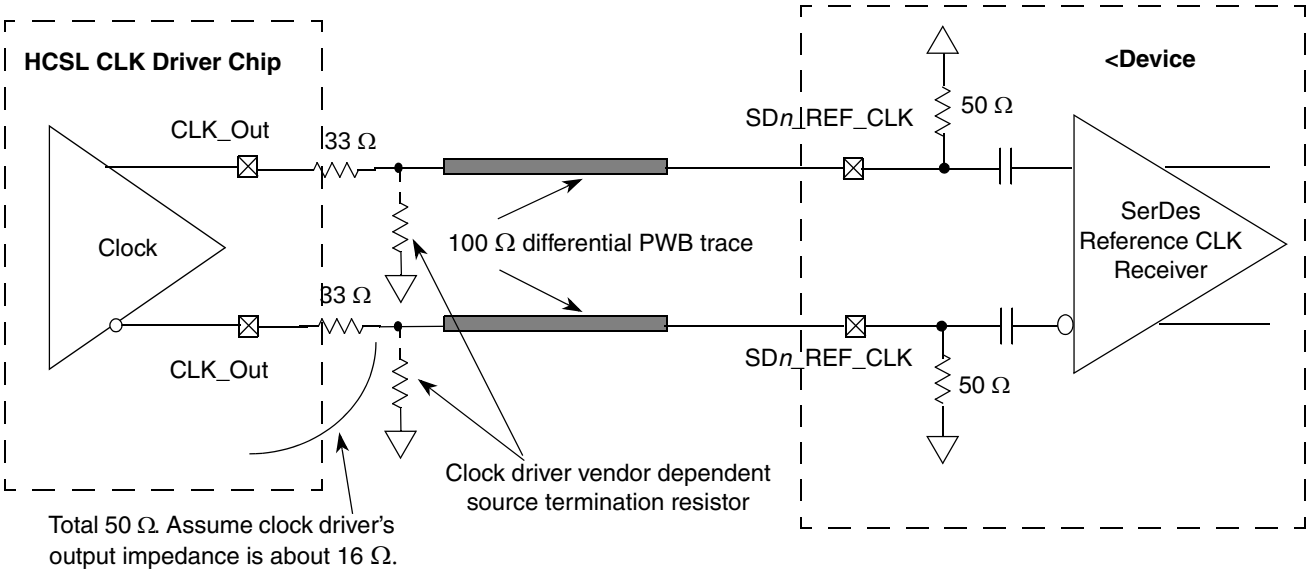


Figure 6. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 7 shows the SerDes reference clock connection reference circuits for the LVDS-type clock driver. Because the LVDS clock driver's common mode voltage is higher than the SerDes reference clock input's allowed range (100–400 mV), an AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external components.

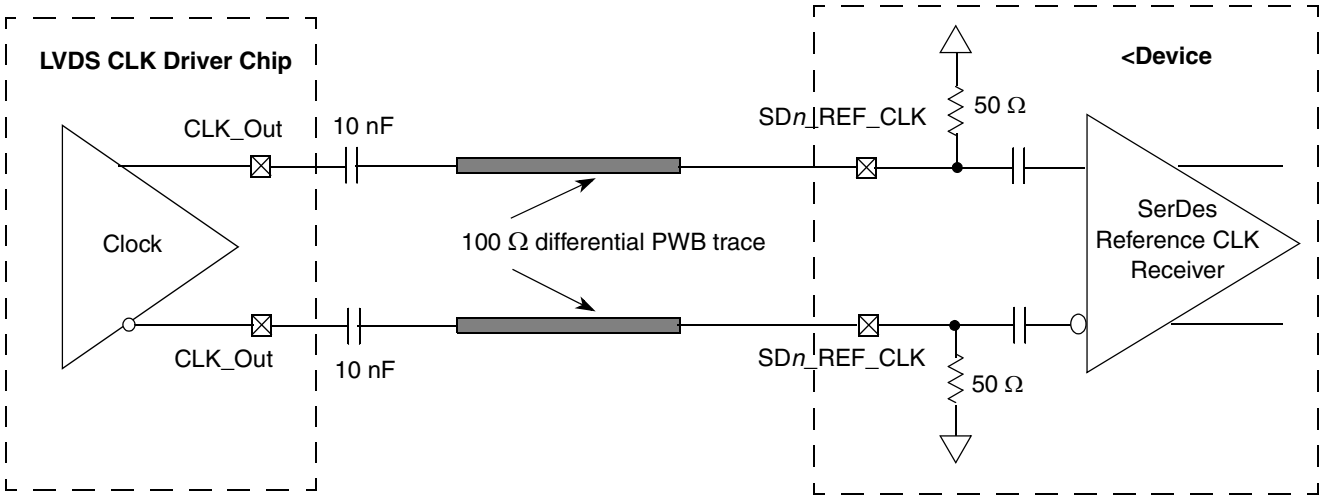


Figure 7. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 8 shows the SerDes reference clock connection reference circuits for the LVPECL-type clock driver. Since the LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the SerDes reference clock input's DC requirement, AC-coupling must be used.

Figure 8 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value can range from 140 Ω to 240 Ω, depending on the clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the SerDes reference clock's differential input amplitude requirement (between a 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Please consult the clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

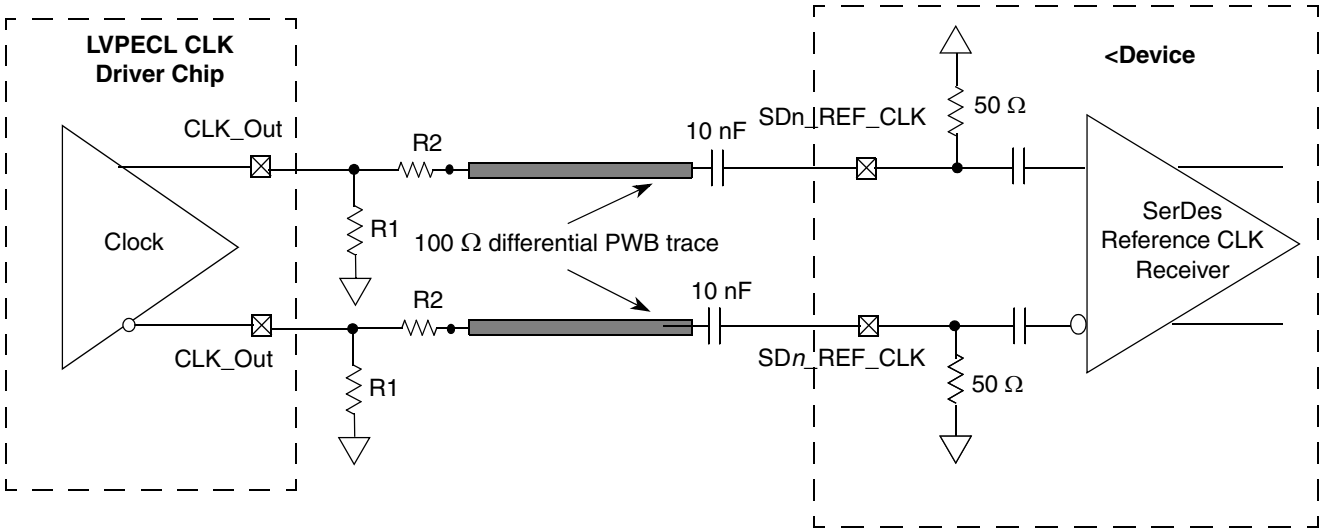


Figure 8. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 9 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the P2020 SerDes reference clock input's DC requirement.

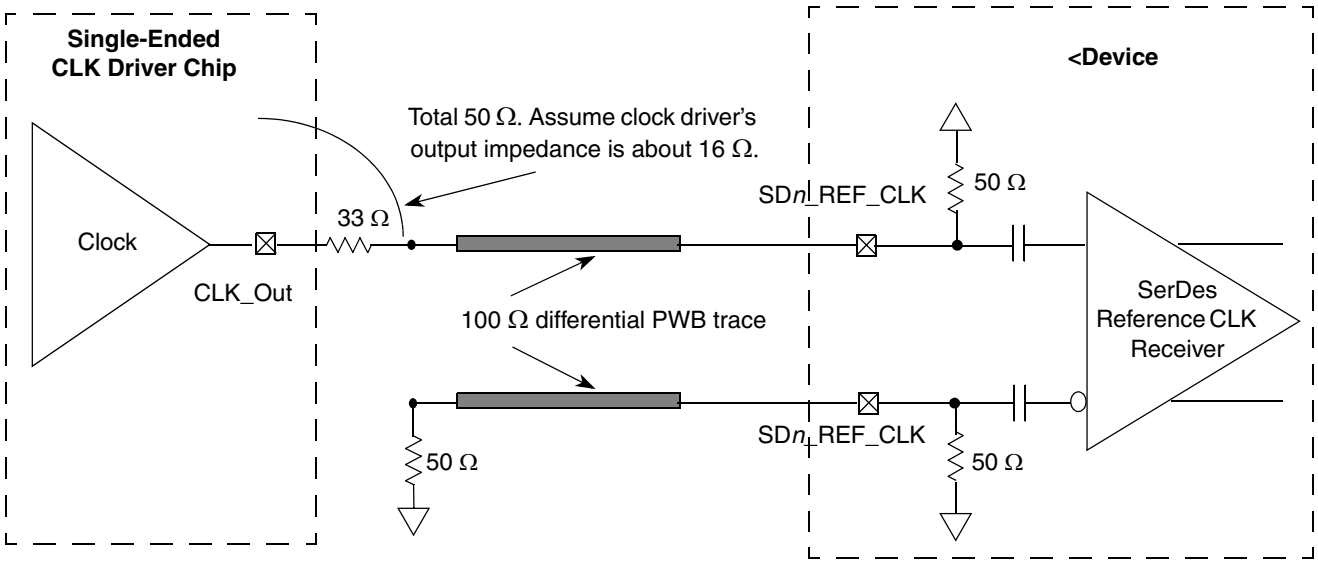


Figure 9. Single-Ended Connection (Reference Only)

20.1.2 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a reference clock with low phase noise and low cycle-to-cycle jitter. Phase noise less than 100 KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 0.1–15 MHz range. The clock source outputs should be carefully impedance-matched to the PCB transmission line to minimize reflections, which are a source of noise to the system.

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. Refer to the *P2020 QorIQ Integrated Processor Hardware Specifications* for detailed information about the PCI Express, SGMII, and serial RapidIO interfaces.

20.2 PCI Express Eye Diagrams

20.2.1 Transmitter Compliance Eye Diagrams

The Tx eye diagram in Figure 10 is specified using the passive compliance/test measurement load (see Figure 12) in place of any real PCI Express interconnect and receiver component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending on whether the diagram is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UIs in the center of the 3500 UIs used for calculating the Tx UI.

NOTE

It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI intervals with a fit algorithm using a minimization merit function (i.e., least squares and median deviation fits).

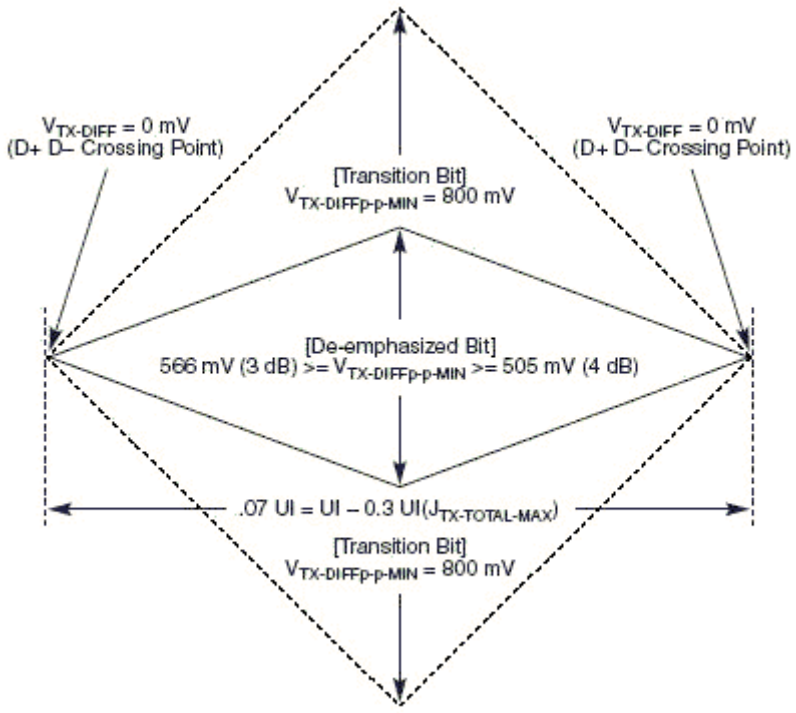


Figure 10. Minimum Transmitter Timing and Voltage Output Compliance Specifications

20.2.2 Receiver Compliance Eye Diagrams

The Rx eye diagram in Figure 11 is specified using the passive compliance/test measurement load (see Figure 12) in place of any real PCI Express Rx component.

Note that in general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 12) will be larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics that cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. The Rx component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 11) expected at the input receiver based on some adequate combination of system simulations and the Return Loss measured looking into the Rx package and silicon. The Rx eye diagram must be aligned in time, using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UIs in the center of the 3500 UIs used for calculating the Tx UI.

NOTE

The reference impedance for return loss measurements is 50 Ωto ground for both the D+ and D– line (i.e., as measured by a Vector Network Analyzer with 50-Ωprobes; see Figure 12). Note that the series capacitors, CTX, are optional for the return loss measurement.

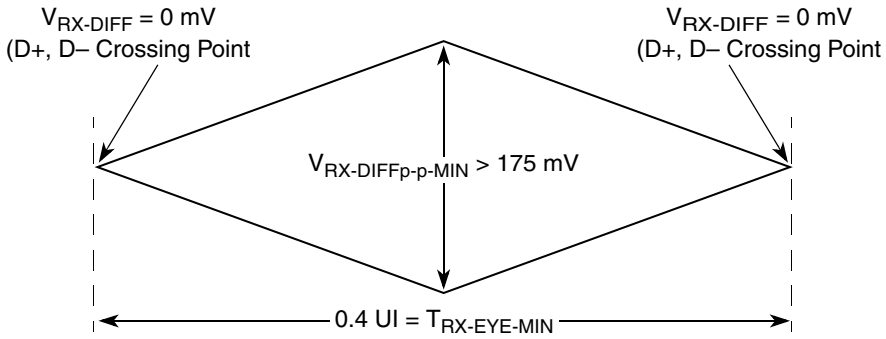


Figure 11. Minimum Receiver Eye Timing and Voltage Compliance Specification

20.2.3 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 12.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

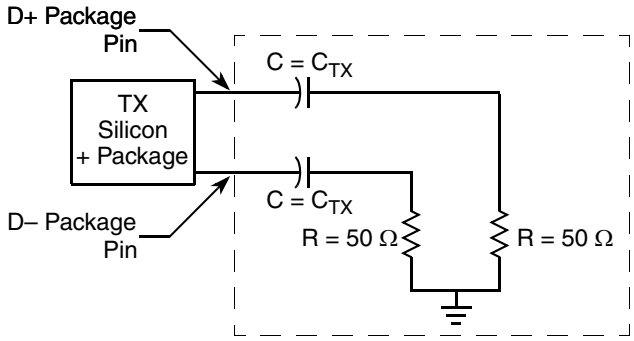


Figure 12. Compliance Test/Measurement Load

20.3 Serial RapidIO Measurement and Test Requirements

Because the LP-Serial electrical specification is guided by the XAUI electrical interface specified in clause 47 of the IEEE 802.3ae-2002 standard, the measurement and test requirements defined here are similarly guided by clause 47. In addition, the CJPAT test pattern defined in Annex 48A of the IEEE 802.3ae-2002 standard is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of the

IEEE 802.3ae-2002 standard is recommended as a reference for additional information on jitter test methods.

20.3.1 Eye Template Measurement Requirements

The eye template measurement requirements are as follows:

- For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter.
- The data pattern for template measurements is the Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of the IEEE 802.3ae standard.
- All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks.
- Four lane implementations shall use CJPAT as defined in Annex 48A.
- Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0.
- The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}.
- The eye pattern shall be measured with AC coupling and the compliance template centered at 0 volts differential.
- The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ω resistive ± 5% differential to 2.5 GHz.

20.3.2 Jitter Test Measurement Requirements

The jitter test measurement requirements are as follows:

- For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter.
- The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of the IEEE 802.3ae standard.
- All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks.
- Four lane implementations shall use CJPAT as defined in Annex 48A.
- Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0.
- Jitter shall be measured with AC coupling and at 0 volts differential.
- Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of the IEEE 802.3ae standard.

20.3.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive ± 5% differential to 2.5 GHz.

20.3.4 Measuring Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in the "AC Requirements for Serial RapidIO Transmitter and Receiver" section of the *P2020 QorIQ Integrated Processor Hardware Specifications* and then adjusting the signal amplitude until the data eye contacts the six points of the transmitter's output compliance mask of the receive template shown in Figure 13 and Table 34. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in the "AC Requirements for Serial RapidIO Transmitter and Receiver" section of the *P2020 QorIQ Integrated Processor Hardware Specifications* is then added to the signal, and the test load is replaced by the receiver being tested.

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in Figure 13 with the parameters specified in Table 34 when measured at the output pins of the device and the device is driving a 100 Ω ± 5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) only needs to comply with the transmitter output compliance mask when pre-emphasis is disabled or minimized.

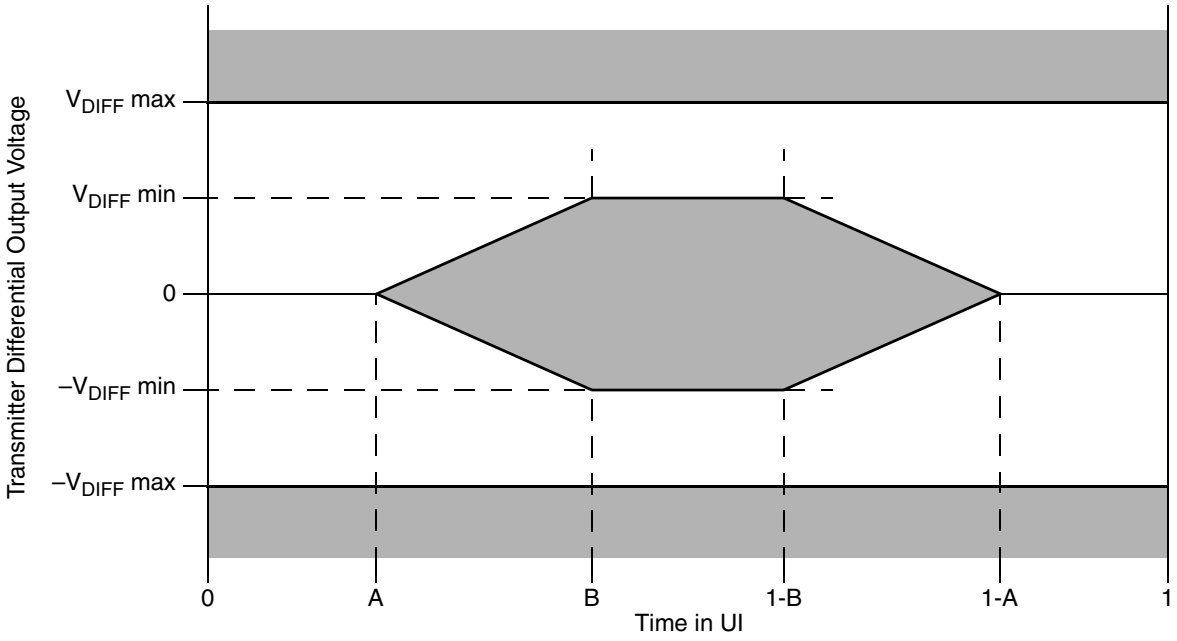


Figure 13. Transmitter Output Compliance Mask

Table 34. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

21 eTSEC IEEE 1588 Pin Recommendations

This section discusses the termination of eTSEC IEEE 1588 pins on the device. Table 35 shows how the pins should be connected.

Table 35. eTSEC IEEE 1588 Pin Recommendations

Pin Name	Pin Used	Pin Not Used
TSEC_1588_CLK_IN	External high precision timer reference clock input	Tie high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
TSEC_1588_TRIG_IN[01]	—	
TSEC_1588_TRIG_IN[02]		
TSEC_1588_ALARM_OUT[01]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
TSEC_1588_ALARM_OUT[02]		
TSEC_1588_CLK_OUT	The value of TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, and TSEC_1588_PULSE_OUT2 during reset is used to set the DDR clock PLL settings. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 6.1.5, "DDR/DDRCLK PLL Ratio."	
TSEC_1588_PULSE_OUT[01]		
TSEC_1588_PULSE_OUT[02]		

22 System Control Pin Recommendations

This section discusses the termination of system control pins on the device. Table 36 shows how the system control pins should be connected.

Table 36. System Control Pin Recommendations

Pin Name	Pin Used	Pin Not Used
$\overline{\text{CKSTP\_IN[00]}}$	Pull high through a 2–10 kΩ resistor to OV_{DD}. Connect to Pin8 of the COP connector (refer to Figure 5).	Pull high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{CKSTP\_IN[01]}}$		
$\overline{\text{CKSTP\_OUT[00]}}$	Pull this open-drain signal high through a 2–10 kΩ resistor to OV_{DD}. Connect to Pin15 of the COP connector (refer to Figure 5).	This output pin may be left floating.
$\overline{\text{CKSTP\_OUT[01]}}$		

Table 36. System Control Pin Recommendations (continued)

Pin Name	Pin Used	Pin Not Used
HRESET	Pull high through a 2–10 kΩ resistor to OV_{DD}. Connect to Pin13 of the COP connector (refer to Figure 5).	
HRESET_REQ	Pull high through a 2–10 kΩ resistor to OV_{DD}. This pin must NOT be pulled down during power-on reset.	This pin must NOT be pulled down during power-on reset.
SRESET	Pull high through a 2–10 kΩ resistor to OV_{DD}. Connect to Pin11 of the COP connector (refer to Figure 5).	Pull high through a 2–10 kΩ resistor to OV_{DD}.

23 Reserved POR Configuration Pins

Several pins on the P2020 are marked reserved configuration as shown in Table 37. The reserved pins are unused POR configuration pins. It is highly recommended that the customer provide capability for setting these pins low to support new configuration options should they arise between revisions.

Table 37. Reserved POR Configuration Pin List

Pin Name	Pin Number	Comment
LA[20]	E12	cfg_spare[0]
LA[21]	A21	cfg_spare[1]
LA[22]	D11	cfg_spare[2]
MSRCID[01]	R27	cfg_spare[5]
MSRCID[04]	N26	cfg_spare[6]
$\overline{\text{DMA1\_DDONE}}$	T26	cfg_spare[7]

24 Power and Ground Signals

The P2020 has several power supplies and ground signals. Table 38 shows how the SerDes pins should be connected.

Table 38. Power and Ground Pin Recommendations

Pin	Comment
AV_{DD}_CORE0	Power supply for the e500 Core PLL0 supply (1.05 V through a filter).
AV_{DD}_CORE1	Power supply for the e500 Core PLL1 supply (1.05 V through a filter).
AV_{DD}_LBIU	Power supply for the local bus PLL supply (1.05 V through a filter).
AV_{DD}_DDR	Power supply for the DDR PLL supply (1.05 V through a filter).
AV_{DD}_PLAT	Power supply for the core complex bus PLL (1.05 V through a filter)
AV_{DD}_SRDS	Power supply for the SerDes PLL (1.05 V through a filter).
BV_{DD}	Power supply for the local bus, GPIO supply I/O voltage (1.8 V, 2.5 V/3.3 V).
CV_{DD}	Power supply for the SPI, eSDHC, USB supply (1.8 V, 2.5 V/3.3 V).
GV_{DD}	Power supply for the DDR supply (1.5 V/1.8 V).
LV_{DD}	Power supply for the TSEC I/Os (2.5 V/3.3 V).
OV_{DD}	Power supply for the general I/O supply DUART, I^2C, GPIO , and JTAG I/O voltage (3.3 V).
SV_{DD}_SRDS	Power supply for the SerDes core logic supply (1.05 V).
XV_{DD}_SRDS	Pad Power for the SerDes transceiver supply (1.05 V)
XGND_SRDS	SerDes transceiver GND
SGND_SRDS	SerDes core logic GND

Table 38. Power and Ground Pin Recommendations (continued)

Pin	Comment
AGND_SRDS	SerDes PLL GND
V_{DD}	Power supply for the core I/Os (1.05 V).
GND	Ground

25 No-Connect Pins

Table 39. No-Connect Pins

Pin	Comment
NC[1:9]	The following pins should be left as no connects. AE10, AF10, E13, E14, W6, Y14, Y15, Y16, G6
NC[12:13]	The following pins should be left as no connects. F13, P6

26 Thermal Recommendations

This section provides information on thermal management.

26.1 Recommended Thermal Model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

26.2 Thermal Management for WB-TePBGA

This section provides thermal management information for the plastic ball grid array (WB-TePBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 14. The heat sink should be attached to the printed-circuit board with the spring force centered over the center of the package. This spring force should not exceed 10 pounds of force (45 Newton).

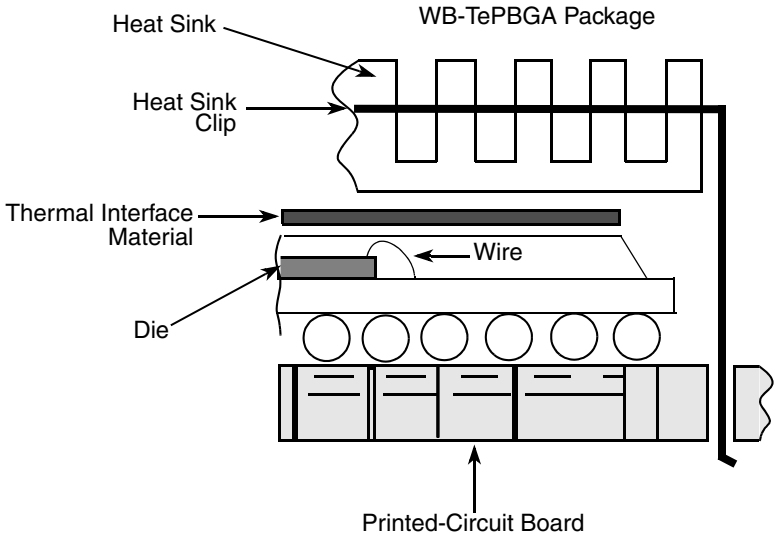


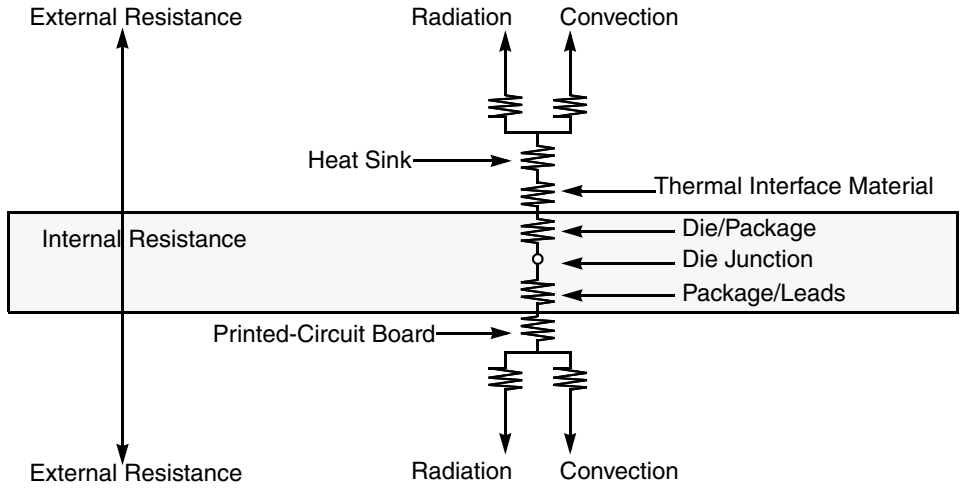
Figure 14. Package Exploded Cross-Sectional View

26.3 Internal Package Conduction Resistance

For the WB-TePBGA package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Figure 15 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 15. Package with Heat Sink Mounted to a Printed-Circuit Board

With the WB-TePBGA package, heat flow is both to the board and to the heat sink. A thermal simulation is required to determine the performance in the application. A Flotherm thermal model of the part is available.

26.4 Minimizing Thermal Contact Resistance

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board see Figure 14.

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interface materials to choose from in the industry.

27 Revision History

Table 40 provides a revision history for this application note.

Table 40. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	04/2011	Initial public release

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Japan
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+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
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China
+86 10 5879 8000
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1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

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