Freescale Semiconductor
Data Sheet: Technical DataProduct Preview

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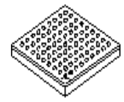
P1012

P1012 QorIQ™ Integrated Processor Hardware Specifications



WB-TePBGA–689
31 mm × 31 mm

The following list provides an overview of the P1012 feature set:

- High-performance 32-bit Book E-enhanced cores that implement the Power Architecture™ technology:
  - P1012 has one core .
  - 36-bit physical addressing
  - Double-precision floating-point support
  - 32 KB L1 instruction cache and 32 KB L1 data cache for each core
  - 400 MHz to 800 MHz clock frequency
- 256 KB L2 cache with ECC. Also configurable as SRAM and stashing memory.
- Three 10/100/1000 Mbps enhanced three-speed Ethernet controllers (eTSECs)
  - TCP/IP acceleration, quality of service, and classification capabilities
  - IEEE® 1588 support
  - Lossless flow control
  - RGMII, SGMII
- High-speed interfaces supporting various multiplexing options:
  - Four SerDes to 3.125 GHz multiplexed across controllers
  - Two PCI Express interfaces
  - Two SGMII interfaces
- High-Speed USB controller (USB 2.0)
  - Host and device support
  - Enhanced host controller interface (EHCI)
  - ULPI interface to PHY
- Enhanced secure digital host controller (SD/MMC)
- Enhanced Serial peripheral interface(eSPI)
- Integrated security engine
  - Protocol support includes SNOW, ARC4, 3DES, AES, RSA/ECC, RNG, single-pass SSL/TLS, Kasumi
  - XOR acceleration
- 32-bit DDR2/DDR3 SDRAM memory controller with ECC support
- Programmable interrupt controller (PIC) compliant with OpenPIC standard
- One four-channel DMA controller
- Two I2C controllers, DUART, timers
- Enhanced local bus controller (eLBC)
- QUICC Engine
- Operating junction temperature (T_j) range: 0–125°C and –40°C–125°C (industrial specification)
- 31 × 31 mm 689-pin WB-TePBGA II (wire bond temperature-enhanced plastic BGA)

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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Figure 2 shows the major functional units within the P1012.

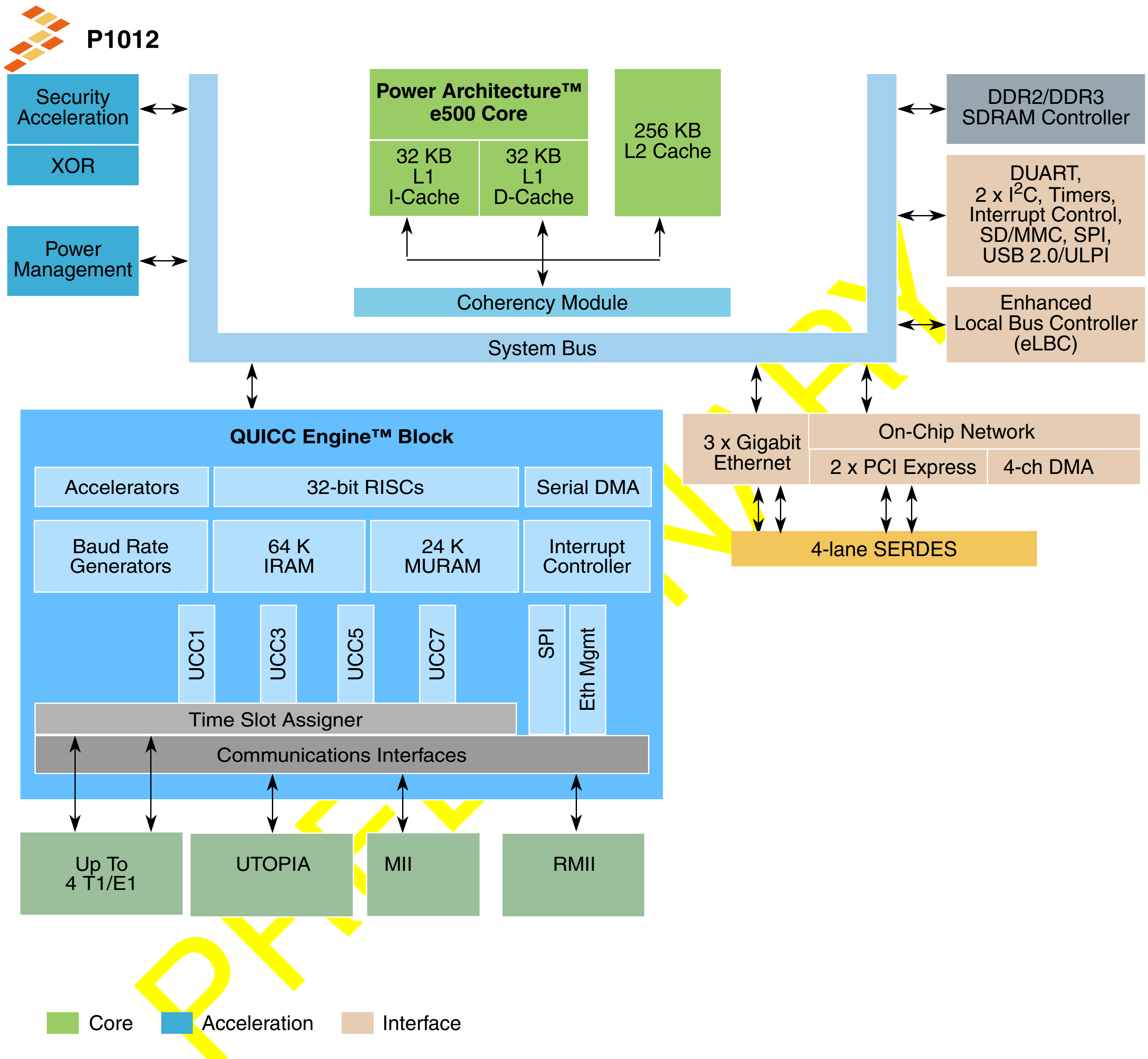


Figure 1. P1012 Block Diagram

1 Pin Assignments and Reset States

1.1 Ball Layout Diagrams

Figure 2. shows the top view of the P1012 689-pin BGA ball map diagram.

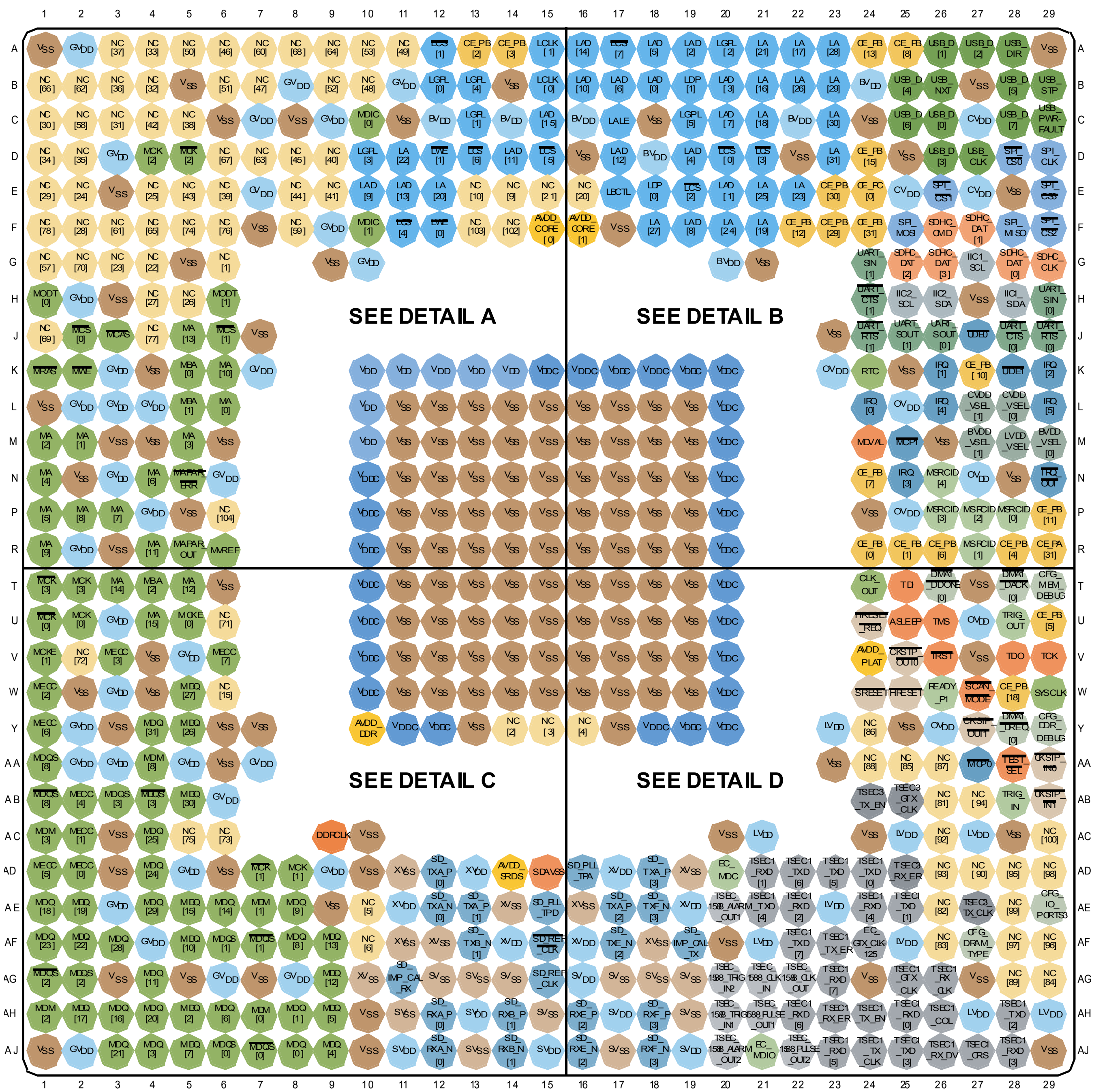


Figure 3. P1012 top view ballmap

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	V_{SS}	GV_{DD}	NC [37]	NC [33]	NC [50]	NC [46]	NC [60]	NC [68]	NC [64]	NC [53]	NC [49]	$\overline{\text{LCS}}$ [1]	CE_PB [2]	CE_PB [3]	LCLK [1]
B	NC [66]	NC [62]	NC [36]	NC [32]	V_{SS}	NC [51]	NC [47]	GV_{DD}	NC [52]	NC [48]	GV_{DD}	LGPL [0]	LGPL [4]	V_{SS}	LCLK [0]
C	NC [30]	NC [58]	NC [31]	NC [42]	NC [38]	V_{SS}	GV_{DD}	V_{SS}	GV_{DD}	MDIC [0]	V_{SS}	BV_{DD}	LGPL [1]	BV_{DD}	LAD [15]
D	NC [34]	NC [35]	GV_{DD}	MCK [2]	$\overline{\text{MCK}}$ [2]	NC [67]	NC [63]	NC [45]	NC [40]	LGPL [3]	LA [22]	$\overline{\text{LWE}}$ [1]	$\overline{\text{LCS}}$ [6]	LAD [11]	$\overline{\text{LCS}}$ [5]
E	NC [29]	NC [24]	V_{SS}	NC [25]	NC [43]	NC [39]	GV_{DD}	NC [44]	NC [41]	LAD [9]	LAD [13]	LA [20]	NC [10]	NC [9]	NC [21]
F	NC [78]	NC [28]	NC [61]	NC [65]	NC [74]	NC [76]	V_{SS}	NC [59]	GV_{DD}	MDIC [1]	$\overline{\text{LCS}}$ [4]	$\overline{\text{LWE}}$ [0]	NC [103]	NC [102]	AVDD_ CORE [0]
G	NC [57]	NC [70]	NC [23]	NC [22]	V_{SS}	NC [1]			V_{SS}	GV_{DD}					
H	MODT [0]	GV_{DD}	V_{SS}	NC [27]	NC [26]	MODT [1]									
J	NC [69]	$\overline{\text{MCS}}$ [0]	$\overline{\text{MCAS}}$	NC [77]	MA [13]	$\overline{\text{MCS}}$ [1]	V_{SS}								
K	$\overline{\text{MRAS}}$	$\overline{\text{MWE}}$	GV_{DD}	V_{SS}	MBA [0]	MA [10]	GV_{DD}			V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DDC}
L	V_{SS}	GV_{DD}	GV_{DD}	GV_{DD}	MBA [1]	MA [0]				V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
M	MA [2]	MA [1]	V_{SS}	V_{SS}	MA [3]	V_{SS}				V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
N	MA [4]	V_{SS}	GV_{DD}	MA [6]	$\overline{\text{MAPAR\_ERR}}$	GV_{DD}				V_{DDC}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
P	MA [5]	MA [8]	MA [7]	GV_{DD}	V_{SS}	NC [104]				V_{DDC}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
R	MA [9]	GV_{DD}	V_{SS}	MA [11]	MAPAR_ OUT	MVREF				V_{DDC}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}

DETAIL A

Figure 4. P1012 detail A ballmap

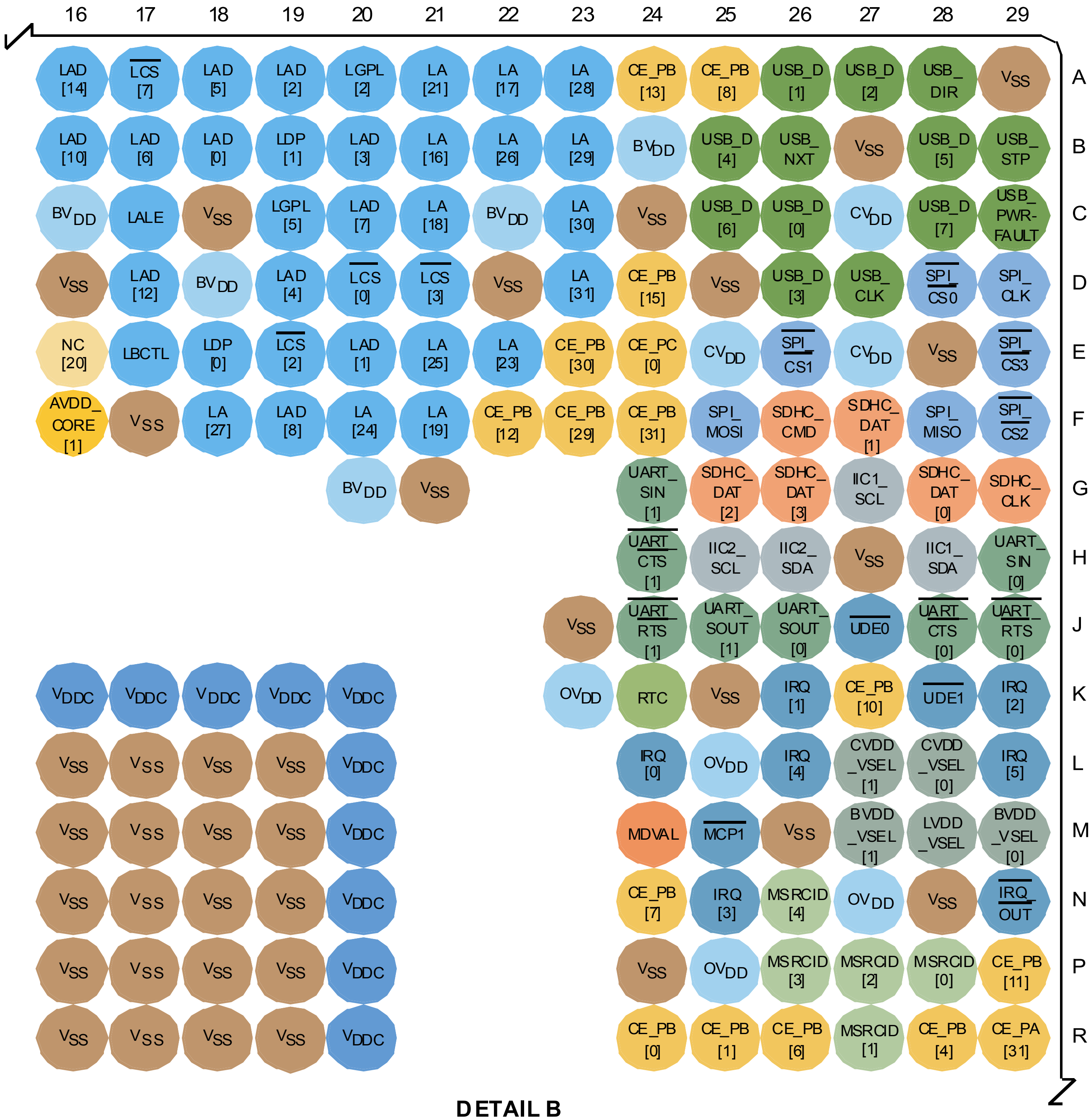


Figure 5. P1012 detail B ballmap

DETAIL C

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
T	$\overline{MCK}$ [3]	MCK [3]	MA [14]	MBA [2]	MA [12]	V_{SS}				V_{DDC}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
U	$\overline{MCK}$ [0]	MCK [0]	GV_{DD}	MA [15]	MCKE [0]	NC [71]				V_{DDC}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
V	MCKE [1]	NC [72]	MECC [3]	V_{SS}	GV_{DD}	MECC [7]				V_{DDC}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
W	MECC [2]	V_{SS}	GV_{DD}	V_{SS}	MDQ [27]	NC [15]				V_{DDC}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
Y	MECC [6]	GV_{DD}	V_{SS}	MDQ [31]	MDQ [26]	V_{SS}	V_{SS}			AVDD_ DDR	V_{DDC}	V_{DDC}	V_{SS}	NC [2]	NC [3]
AA	MDQS [8]	GV_{DD}	GV_{DD}	MDM [8]	GV_{DD}	V_{SS}	GV_{DD}								
AB	$\overline{MDQS}$ [8]	MECC [4]	MDQS [3]	$\overline{MDQS}$ [3]	MDQ [30]	GV_{DD}									
AC	MDM [3]	MECC [1]	V_{SS}	MDQ [25]	NC [75]	NC [73]			DDRCLK	V_{SS}					
AD	MECC [5]	MECC [0]	V_{SS}	MDQ [24]	GV_{DD}	V_{SS}	$\overline{MCK}$ [1]	MCK [1]	GV_{DD}	V_{SS}	XV_{SS}	SD_ TXA_P [0]	XV_{DD}	AVDD_ SRDS	SDAVSS
AE	MDQ [18]	MDQ [19]	GV_{DD}	MDQ [29]	MDQ [15]	MDQ [14]	MDM [1]	MDQ [9]	V_{SS}	NC [5]	XV_{DD}	SD_ TXA_N [0]	SD_ TXA_P [1]	XV_{SS}	SD_PLL _TPD
AF	MDQ [23]	MDQ [22]	MDQ [28]	GV_{DD}	MDQ [10]	MDQS [1]	$\overline{MDQS}$ [1]	MDQ [8]	MDQ [13]	NC [6]	XV_{SS}	XV_{SS}	SD_ TXB_N [1]	XV_{DD}	$\overline{SD\_REF\_CLK}$
AG	$\overline{MDQS}$ [2]	MDQS [2]	V_{SS}	MDQ [11]	V_{SS}	GV_{DD}	V_{SS}	GV_{DD}	MDQ [12]	XV_{SS}	SD_ IMP_CAL _RX	SV_{SS}	SV_{SS}	SV_{SS}	SD_REF _CLK
AH	MDM [2]	MDQ [17]	MDQ [16]	MDQ [20]	MDQ [2]	MDQ [6]	MDM [0]	MDQ [1]	MDQ [5]	V_{SS}	SV_{SS}	SD_ RXA_P [0]	SV_{DD}	SD_ RXB_P [1]	SV_{SS}
AJ	V_{SS}	GV_{DD}	MDQ [21]	MDQ [3]	MDQ [7]	MDQS [0]	$\overline{MDQS}$ [0]	MDQ [0]	MDQ [4]	V_{SS}	SV_{DD}	SD_ RXA_N [0]	SV_{SS}	SD_ RXB_N [1]	SV_{DD}

Figure 6. P1012 detail C ballmap

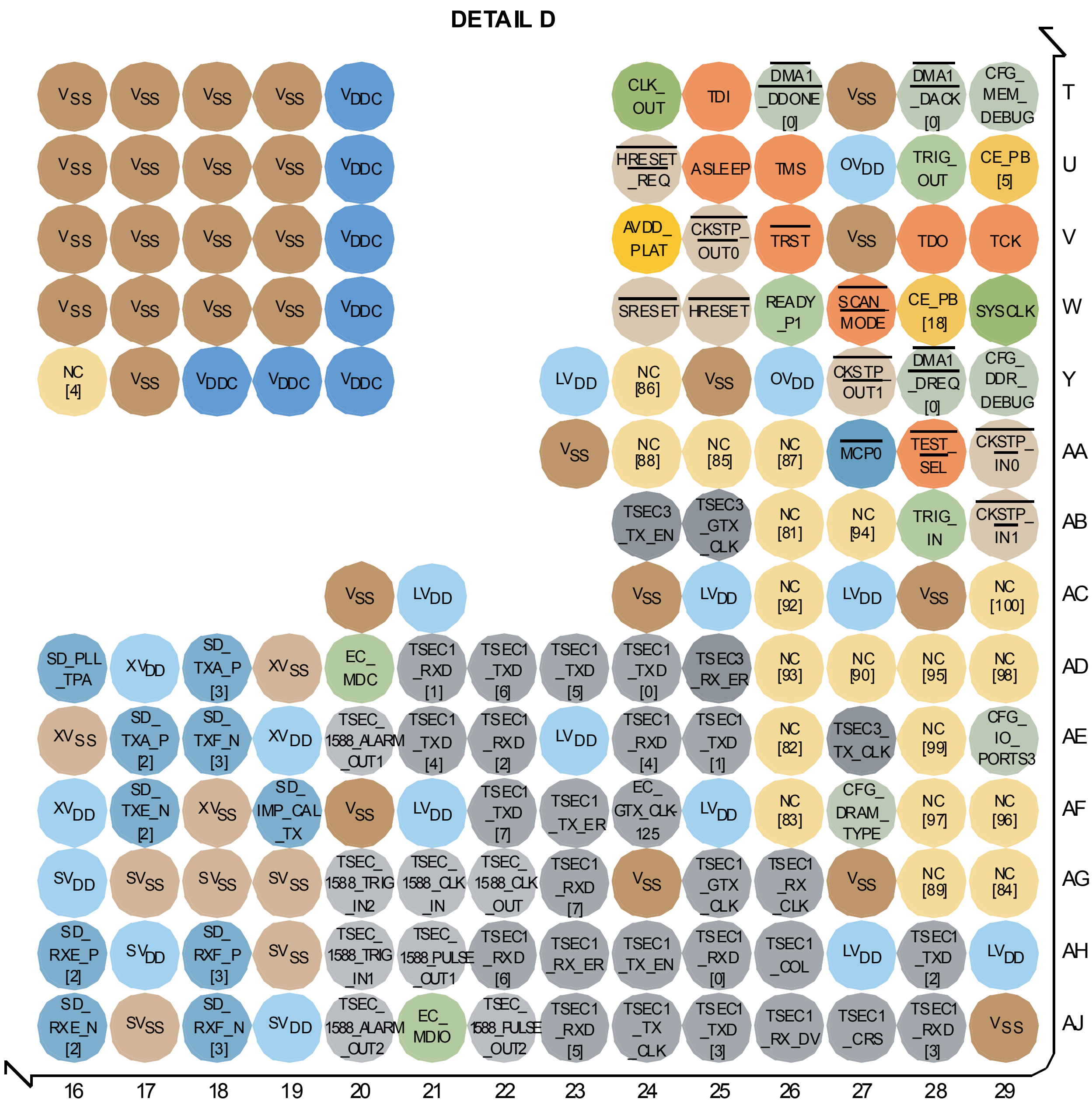


Figure 7. P1012 detail D ballmap

1.2 Pinout Assignments

Table 1 provides the pinout listing for the P1012.

Table 1. P10 12 Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface				
MDQ00	AJ8	I/O	GV_{DD}	—
MDQ01	AH8	I/O	GV_{DD}	—
MDQ02	AH5	I/O	GV_{DD}	—
MDQ03	AJ4	I/O	GV_{DD}	—
MDQ04	AJ9	I/O	GV_{DD}	—
MDQ05	AH9	I/O	GV_{DD}	—
MDQ06	AH6	I/O	GV_{DD}	—
MDQ07	AJ5	I/O	GV_{DD}	—
MDQ08	AF8	I/O	GV_{DD}	—
MDQ09	AE8	I/O	GV_{DD}	—
MDQ10	AF5	I/O	GV_{DD}	—
MDQ11	AG4	I/O	GV_{DD}	—
MDQ12	AG9	I/O	GV_{DD}	—
MDQ13	AF9	I/O	GV_{DD}	—
MDQ14	AE6	I/O	GV_{DD}	—
MDQ15	AE5	I/O	GV_{DD}	—
MDQ16	AH3	I/O	GV_{DD}	—
MDQ17	AH2	I/O	GV_{DD}	—
MDQ18	AE1	I/O	GV_{DD}	—
MDQ19	AE2	I/O	GV_{DD}	—
MDQ20	AH4	I/O	GV_{DD}	—
MDQ21	AJ3	I/O	GV_{DD}	—
MDQ22	AF2	I/O	GV_{DD}	—
MDQ23	AF1	I/O	GV_{DD}	—
MDQ24	AD4	I/O	GV_{DD}	—
MDQ25	AC4	I/O	GV_{DD}	—
MDQ26	Y5	I/O	GV_{DD}	—
MDQ27	W5	I/O	GV_{DD}	—
MDQ28	AF3	I/O	GV_{DD}	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MDQ29	AE4	I/O	GV_{DD}	—
MDQ30	AB5	I/O	GV_{DD}	—
MDQ31	Y4	I/O	GV_{DD}	—
NC22	G4	NC	—	—
NC23	G3	NC	—	—
NC24	E2	NC	—	—
NC25	E4	NC	—	—
NC26	H5	NC	—	—
NC27	H4	NC	—	—
NC28	F2	NC	—	—
NC29	E1	NC	—	—
NC30	C1	NC	—	—
NC31	C3	NC	—	—
NC32	B4	NC	—	—
NC33	A4	NC	—	—
NC34	D1	NC	—	—
NC35	D2	NC	—	—
NC36	B3	NC	—	—
NC37	A3	NC	—	—
NC38	C5	NC	—	—
NC39	E6	NC	—	—
NC40	D9	NC	—	—
NC41	E9	NC	—	—
NC42	C4	NC	—	—
NC43	E5	NC	—	—
NC44	E8	NC	—	—
NC45	D8	NC	—	—
NC46	A6	NC	—	—
NC47	B7	NC	—	—
NC48	B10	NC	—	—
NC49	A11	NC	—	—
NC50	A5	NC	—	—
NC51	B6	NC	—	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
NC52	B9	NC	—	—
NC53	A10	NC	—	—
MECC00	AD2	I/O	GV_{DD}	—
MECC01	AC2	I/O	GV_{DD}	—
MECC02	W1	I/O	GV_{DD}	—
MECC03	V3	I/O	GV_{DD}	—
MECC04	AB2	I/O	GV_{DD}	—
MECC05	AD1	I/O	GV_{DD}	—
MECC06	Y1	I/O	GV_{DD}	—
MECC07	V6	I/O	GV_{DD}	—
MAPAR_ERR_B	N5	I	GV_{DD}	—
MAPAR_OUT	R5	O	GV_{DD}	—
MDM00	AH7	O	GV_{DD}	—
MDM01	AE7	O	GV_{DD}	—
MDM02	AH1	O	GV_{DD}	—
MDM03	AC1	O	GV_{DD}	—
NC57	G1	NC	—	—
NC58	C2	NC	—	—
NC59	F8	NC	—	—
NC60	A7	NC	—	—
MDM08	AA4	O	GV_{DD}	—
MDQS00	AJ6	I/O	GV_{DD}	—
MDQS01	AF6	I/O	GV_{DD}	—
MDQS02	AG2	I/O	GV_{DD}	—
MDQS03	AB3	I/O	GV_{DD}	—
NC61	F3	NC	—	—
NC62	B2	NC	—	—
NC63	D7	NC	—	—
NC64	A9	NC	—	—
MDQS08	AA1	I/O	GV_{DD}	—
MDQS_B00	AJ7	I/O	GV_{DD}	—
MDQS_B01	AF7	I/O	GV_{DD}	—
MDQS_B02	AG1	I/O	GV_{DD}	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MDQS_B03	AB4	I/O	GV_{DD}	—
NC65	F4	NC	—	—
NC66	B1	NC	—	—
NC67	D6	NC	—	—
NC68	A8	NC	—	—
MDQS_B08	AB1	I/O	GV_{DD}	—
MBA00	K5	O	GV_{DD}	—
MBA01	L5	O	GV_{DD}	—
MBA02	T4	O	GV_{DD}	—
MA00	L6	O	GV_{DD}	—
MA01	M2	O	GV_{DD}	—
MA02	M1	O	GV_{DD}	—
MA03	M5	O	GV_{DD}	—
MA04	N1	O	GV_{DD}	—
MA05	P1	O	GV_{DD}	—
MA06	N4	O	GV_{DD}	—
MA07	P3	O	GV_{DD}	—
MA08	P2	O	GV_{DD}	—
MA09	R1	O	GV_{DD}	—
MA10	K6	O	GV_{DD}	—
MA11	R4	O	GV_{DD}	—
MA12	T5	O	GV_{DD}	—
MA13	J5	O	GV_{DD}	—
MA14	T3	O	GV_{DD}	—
MA15	U4	O	GV_{DD}	—
MWE_B	K2	O	GV_{DD}	—
MRAS_B	K1	O	GV_{DD}	—
MCAS_B	J3	O	GV_{DD}	—
MCS_B00	J2	O	GV_{DD}	—
MCS_B01	J6	O	GV_{DD}	—
NC69	J1	NC	—	—
NC70	G2	NC	—	—
MCKE00	U5	O	GV_{DD}	11

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MCKE01	V1	O	GV_{DD}	11
NC71	U6	NC	—	—
NC72	V2	NC	—	—
MCK00	U2	O	GV_{DD}	—
MCK01	AD8	O	GV_{DD}	—
MCK02	D4	O	GV_{DD}	—
MCK03	T2	O	GV_{DD}	—
NC73	AC6	NC	—	—
NC74	F5	NC	—	—
MCK_B00	U1	O	GV_{DD}	—
MCK_B01	AD7	O	GV_{DD}	—
MCK_B02	D5	O	GV_{DD}	—
MCK_B03	T1	O	GV_{DD}	—
NC75	AC5	NC	—	—
NC76	F6	NC	—	—
MODT00	H1	O	GV_{DD}	—
MODT01	H6	O	GV_{DD}	—
NC77	J4	NC	—	—
NC78	F1	NC	—	—
MDIC00	C10	I/O	GV_{DD}	23
MDIC01	F10	I/O	GV_{DD}	23
SerDes				
SD_TX_3	AD18	O	XV_{DD}_SRDS	—
SD_TX_2	AE17	O	XV_{DD}_SRDS	—
SD_TX_1	AE13	O	XV_{DD}_SRDS	—
SD_TX_0	AD12	O	XV_{DD}_SRDS	—
SD_TX_B3	AE18	O	XV_{DD}_SRDS	—
SD_TX_B2	AF17	O	XV_{DD}_SRDS	—
SD_TX_B1	AF13	O	XV_{DD}_SRDS	—
SD_TX_B0	AE12	O	XV_{DD}_SRDS	—
SD_RX_3	AH18	I	XV_{DD}_SRDS	—
SD_RX_2	AH16	I	XV_{DD}_SRDS	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_RX_1	AH14	I	XV_{DD}_SRDS	—
SD_RX_0	AH12	I	XV_{DD}_SRDS	—
SD_RX_B3	AJ18	I	XV_{DD}_SRDS	—
SD_RX_B2	AJ16	I	XV_{DD}_SRDS	—
SD_RX_B1	AJ14	I	XV_{DD}_SRDS	—
SD_RX_B0	AJ12	I	XV_{DD}_SRDS	—
SD_REF_CLK	AG15	I	XV_{DD}_SRDS	—
SD_REF_CLK_B	AF15	I	XV_{DD}_SRDS	—
SD_PLL_TPD	AE15	O	XV_{DD}_SRDS	15
SD_IMP_CAL_RX	AG11	I	XV_{DD}_SRDS	34
SD_IMP_CAL_TX	AF19	I	XV_{DD}_SRDS	34
SD_PLL_TPA	AD16	O	XV_{DD}_SRDS	15
Enhanced Local Bus Controller Interface				
LAD00	B18	I/O	BV_{DD}	5,29
LAD01	E20	I/O	BV_{DD}	5,29
LAD02	A19	I/O	BV_{DD}	5,29
LAD03	B20	I/O	BV_{DD}	5,29
LAD04	D19	I/O	BV_{DD}	5,29
LAD05	A18	I/O	BV_{DD}	5,29
LAD06	B17	I/O	BV_{DD}	5,29
LAD07	C20	I/O	BV_{DD}	5,29
LAD08 / CE_PA0	F19	I/O	BV_{DD}	5,29
LAD09	E10	I/O	BV_{DD}	5,29
LAD10	B16	I/O	BV_{DD}	5,29
LAD11	D14	I/O	BV_{DD}	5,29
LAD12	D17	I/O	BV_{DD}	5,29
LAD13	E11	I/O	BV_{DD}	5,29
LAD14	A16	I/O	BV_{DD}	5,29
LAD15	C15	I/O	BV_{DD}	5,29
LDP00 / CE_PA11	E18	I/O	BV_{DD}	10
LDP01 / CE_PA12	B19	I/O	BV_{DD}	10
LA16 / CE_PA4	B21	I/O	BV_{DD}	9,31

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LA17 / CE_PA5	A22	I/O	BV_{DD}	9,19
LA18 / CE_PA6	C21	I/O	BV_{DD}	5,9
LA19 / CE_PA7	F21	I/O	BV_{DD}	5,9
LA20 / CE_PA8	E12	I/O	BV_{DD}	5,9
LA21 / CE_PA9	A21	I/O	BV_{DD}	5,9
LA22 / CE_PA10	D11	I/O	BV_{DD}	5,9
LA23 / CE_PA17	E22	I/O	BV_{DD}	5,9
LA24 / CE_PA18	F20	I/O	BV_{DD}	5,9
LA25 / CE_PA19	E21	I/O	BV_{DD}	5,9
LA26 / CE_PA20	B22	I/O	BV_{DD}	5,9
LA27 / CE_PA21	F18	I/O	BV_{DD}	9,31
LA28 / CE_PA13	A23	I/O	BV_{DD}	9,19
LA29 / CE_PA25	B23	I/O	BV_{DD}	—
LA30 / CE_PA26	C23	I/O	BV_{DD}	—
LA31 / CE_PA30	D23	I/O	BV_{DD}	—
LCS_B00	D20	O	BV_{DD}	10
LCS_B01	A12	O	BV_{DD}	10
LCS_B02	E19	O	BV_{DD}	10
LCS_B03	D21	O	BV_{DD}	10
LCS_B04 / CE_PA22	F11	I/O	BV_{DD}	10
LCS_B05 / CE_PA23	D15	I/O	BV_{DD}	10
LCS_B06 / CE_PA24	D13	O	BV_{DD}	10
LCS_B07 / CE_PA27	A17	O	BV_{DD}	10
LWE_B00	F12	O	BV_{DD}	9
LWE_B01 / CE_PB9	D12	I/O	BV_{DD}	9
LBCTL / CE_PB20	E17	I/O	BV_{DD}	8
LALE	C17	O	BV_{DD}	8
LGPL0 / CE_PA1	B12	I/O	BV_{DD}	5
LGPL1 / CE_PA2	C13	I/O	BV_{DD}	5
LGPL2	A20	O	BV_{DD}	8
LGPL3 / CE_PA3	D10	I/O	BV_{DD}	5
LGPL4	B13	I/O	BV_{DD}	—
LGPL5	C19	I/O	BV_{DD}	5

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LCLK00 / CE_PA28	B15	I/O	BV_{DD}	—
LCLK01 / CE_PA16	A15	I/O	BV_{DD}	—
CE_PB2	A13	I/O		—
CE_PB3	A14	I/O		—
DMA				
DMA1_DREQ_B00	Y28	I	OV_{DD}	—
NC101 / CE_PB18	W28	I/O	OV_{DD}	—
DMA1_DACK_B00	T28	O	OV_{DD}	—
CFG_MEM_DEBUG / CE_PB19	T29	I/O	OV_{DD}	—
DMA1_DDONE_B00	T26	O	OV_{DD}	—
CFG_DDR_DEBUG / CE_PA29	Y29	I/O	OV_{DD}	—
Programmable Interrupt Controller				
UDE0_B	J27	I	OV_{DD}	—
NC105	K28	I	OV_{DD}	—
MCP0_B	AA27	I	OV_{DD}	—
NC106	M25	I	OV_{DD}	—
IRQ00	L24	I	OV_{DD}	—
IRQ01	K26	I	OV_{DD}	—
IRQ02	K29	I	OV_{DD}	—
IRQ03	N25	I	OV_{DD}	—
IRQ04	L26	I	OV_{DD}	—
IRQ05	L29	I	OV_{DD}	—
CE_PB10	K27	I	OV_{DD}	—
IRQ_OUT_B	N29	O	OV_{DD}	2
Voltage select				
LVDD_VSEL	M28	I	OV_{DD}	28
BVDD_VSEL0	M29	I	OV_{DD}	28
BVDD_VSEL1	M27	I	OV_{DD}	28
CVDD_VSEL0	L28	I	OV_{DD}	28
CVDD_VSEL1	L27	I	OV_{DD}	28
1588				
TSEC_1588_CLK_IN	AG21	I	LV_{DD}	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC_1588_TRIG_IN1	AH20	I	LV_{DD}	—
TSEC_1588_TRIG_IN2	AG20	I	LV_{DD}	—
TSEC_1588_ALARM_OUT1	AE20	O	LV_{DD}	5,9
TSEC_1588_ALARM_OUT2	AJ20	O	LV_{DD}	5,9
TSEC_1588_CLK_OUT	AG22	O	LV_{DD}	5,9
TSEC_1588_PULSE_OUT1	AH21	O	LV_{DD}	5,9
TSEC_1588_PULSE_OUT2	AJ22	O	LV_{DD}	5,9
Ethernet Management Interface				
EC_MDC	AD20	O	LV_{DD}	5,9
EC_MDIO	AJ21	I/O	LV_{DD}	—
Gigabit Ethernet Reference Clock				
EC_GTX_CLK125	AF24	I	LV_{DD}	26
Enhanced Three Speed Ethernet Controller 1				
TSEC1_TXD07 / TSEC3_TXD03	AF22	O	LV_{DD}	5,9
TSEC1_TXD06 / TSEC3_TXD02	AD22	O	LV_{DD}	5,9
TSEC1_TXD05 / TSEC3_TXD01	AD23	O	LV_{DD}	5,9
TSEC1_TXD04 / TSEC3_TXD00	AE21	O	LV_{DD}	5,9
TSEC1_TXD03	AJ25	O	LV_{DD}	5,9
TSEC1_TXD02	AH28	O	LV_{DD}	5,9
TSEC1_TXD01	AE25	O	LV_{DD}	5,9
TSEC1_TXD00	AD24	O	LV_{DD}	5,9
TSEC1_TX_EN	AH24	O	LV_{DD}	33
TSEC1_TX_ER	AF23	O	LV_{DD}	5,9
TSEC1_TX_CLK / TSEC1_GTX_CLK125	AJ24	I	LV_{DD}	—
TSEC1_GTX_CLK	AG25	O	LV_{DD}	—
TSEC1_CRS / TSEC3_RX_DV	AJ27	I/O	LV_{DD}	—
TSEC1_COL / TSEC3_RX_CLK	AH26	I	LV_{DD}	—
TSEC1_RXD07 / TSEC3_RXD03	AG23	I	LV_{DD}	—
TSEC1_RXD06 / TSEC3_RXD02	AH22	I	LV_{DD}	—
TSEC1_RXD05 / TSEC3_RXD01	AJ23	I	LV_{DD}	—
TSEC1_RXD04 / TSEC3_RXD00	AE24	I	LV_{DD}	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_RXD03	AJ28	I	LV_{DD}	—
TSEC1_RXD02	AE22	I	LV_{DD}	—
TSEC1_RXD01	AD21	I	LV_{DD}	—
TSEC1_RXD00	AH25	I	LV_{DD}	—
TSEC1_RX_DV	AJ26	I	LV_{DD}	—
TSEC1_RX_ER	AH23	I	LV_{DD}	—
TSEC1_RX_CLK	AG26	I	LV_{DD}	—
Three Speed Ethernet Controller 3				
NC82	AE26	NC	—	—
NC83	AF26	NC	—	—
TSEC3_TX_EN	AB24	O	LV_{DD}	33
TSEC3_GTX_CLK	AB25	O	LV_{DD}	—
NC84	AG29	NC	—	—
NC85	AA25	NC	—	—
CFG_DRAM_TYPE	AF27	O	LV_{DD}	—
NC86	Y24	NC	—	—
NC87	AA26	NC	—	—
CFG_IO_PORTS3	AE29	O	LV_{DD}	—
NC88	AA24	NC	—	—
NC89	AG28	NC	—	—
TSEC3_RX_ER	AD25	I/O	LV_{DD}	—
TSEC3_TX_CLK	AE27	I	LV_{DD}	—
NC90	AD27	NC	—	—
NC91	AB26	NC	—	—
NC92	AC26	NC	—	—
NC93	AD26	NC	—	—
NC94	AB27	NC	—	—
NC95	AD28	NC	—	—
NC96	AF29	NC	—	—
NC97	AF28	NC	—	—
NC98	AD29	NC	—	—
NC99	AE28	NC	—	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
NC100	AC29	NC	—	—
DUART				
UART_SOUT00	J26	O	OV_{DD}	27
UART_SOUT01 / CE_PB17	J25	I/O	OV_{DD}	
UART_SIN00	H29	I	OV_{DD}	—
UART_SIN01 / CE_PB16	G24	I/O	OV_{DD}	—
UART_CTS_B00	J28	I	OV_{DD}	—
UART_CTS_B01 / CE_PB14	H24	I/O	OV_{DD}	—
UART_RTS_B00	J29	O	OV_{DD}	5
UART_RTS_B01 / CE_PB15	J24	O	OV_{DD}	5
I2C				
IIC1_SDA	H28	I/O	OV_{DD}	18
IIC1_SCL	G27	I/O	OV_{DD}	18
IIC2_SDA / CE_PB21	H26	I/O	OV_{DD}	18
IIC2_SCL / CE_PB22	H25	I/O	OV_{DD}	18
eSDHC				
SDHC_DATA00	G28	I/O	CV_{DD}	—
SDHC_DATA01	F27	I/O	CV_{DD}	—
SDHC_DATA02	G25	I/O	CV_{DD}	—
SDHC_DATA03	G26	I/O	CV_{DD}	—
SDHC_CMD	F26	I/O	CV_{DD}	—
SDHC_CLK	G29	O	CV_{DD}	—
SPI				
SPI_MISO	F28	I	CV_{DD}	—
SPI_MOSI	F25	I/O	CV_{DD}	—
SPI_CS0_B / SDHC_DATA04	D28	I/O	CV_{DD}	—
SPI_CS1_B / SDHC_DATA05	E26	I/O	CV_{DD}	—
SPI_CS2_B / SDHC_DATA06	F29	I/O	CV_{DD}	—
SPI_CS3_B / SDHC_DATA07	E29	I/O	CV_{DD}	—
SPI_CLK	D29	O	CV_{DD}	—
USB				
USB_NXT	B26	I	CV_{DD}	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
USB_DIR	A28	I	CV_{DD}	—
USB_STP	B29	O	CV_{DD}	—
USB_PWRFAULT	C29	I	CV_{DD}	—
USB_CLK	D27	I	CV_{DD}	—
USB_D07	C28	I/O	CV_{DD}	—
USB_D06	C25	I/O	CV_{DD}	—
USB_D05	B28	I/O	CV_{DD}	—
USB_D04	B25	I/O	CV_{DD}	—
USB_D03	D26	I/O	CV_{DD}	—
USB_D02	A27	I/O	CV_{DD}	—
USB_D01	A26	I/O	CV_{DD}	—
USB_D00	C26	I/O	CV_{DD}	—
General-Purpose Input/Output				
CE_PB4	R28	I/O	OV_{DD}	—
CE_PB6	R26	I/O	OV_{DD}	—
CE_PB11	P29	I/O	OV_{DD}	—
CE_PB7	N24	I/O	OV_{DD}	—
CE_PB5	U29	I/O	OV_{DD}	—
CE_PB0	R24	I/O	OV_{DD}	—
CE_PA31	R29	I/O	OV_{DD}	—
CE_PB	R25	I/O	OV_{DD}	—
SDHC_CD / CE_PB12	F22	I/O	BV_{DD}	—
SDHC_WP / CE_PB13	A24	I/O	BV_{DD}	—
USB_PCTL0 / TSEC3_XTRNL_TX_STMP / CE_PB8	A25	I/O	BV_{DD}	—
USB_PCTL1 / TSEC3_XTRNL_RX_STMP / CE_PA15	D24	I/O	BV_{DD}	—
TSEC1_XTRNL_TX_STMP / CE_PB29	F23	I/O	BV_{DD}	—
TSEC1_XTRNL_RX_STMP / CE_PB30	E23	I/O	BV_{DD}	—
TSEC2_XTRNL_TX_STMP / CE_PB31	F24	I/O	BV_{DD}	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_XTRNL_RX_STMP / CE_PC0	E24	I/O	BV_{DD}	—
System Control				
HRESET_B	W25	I	OV_{DD}	—
HRESET_REQ_B	U24	O	OV_{DD}	19
SRESET_B	W24	I	OV_{DD}	—
CKSTP_IN0_B	AA29	I	OV_{DD}	—
NC107	AB29	I	OV_{DD}	—
CKSTP_OUT0_B	V25	O	OV_{DD}	2
NC108	Y27	O	OV_{DD}	2
Debug				
TRIG_IN	AB28	I	OV_{DD}	9,27
TRIG_OUT	U28	O	OV_{DD}	9
NC109	W26	O	OV_{DD}	
MSRCID00 / LB_MSRCID00 / PLL_PER_OUT00 / CE_PB23	P28	I/O	OV_{DD}	27
MSRCID01 / LB_MSRCID01 / PLL_PER_OUT01 / CE_PB24	R27	I/O	OV_{DD}	19
MSRCID02 / LB_MSRCID02 / PLL_PER_OUT02 / CE_PB25	P27	I/O	OV_{DD}	19
MSRCID03 / LB_MSRCID03 / PLL_PER_OUT03 / CE_PB26	P26	I/O	OV_{DD}	19
MSRCID04 / LB_MSRCID04 / PLL_UP_DN / CE_PB27	N26	I/O	OV_{DD}	27
MDVAL/ LB_MDVAL / PLL_PER_VALID / CE_PB28	M24	I/O	OV_{DD}	19
Clocks				
CLK_OUT	T24	O	OV_{DD}	11
RTC	K24	I	OV_{DD}	—
DDRCLK	AC9	I	OV_{DD}	25
SYSCLK	W29	I	OV_{DD}	—
DFT				
SCAN_MODE_B	W27	I	OV_{DD}	—
TEST_SEL_B	AA28	I	OV_{DD}	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
JTAG				
TCK	V29	I	OV_{DD}	—
TDI	T25	I	OV_{DD}	12
TDO	V28	O	OV_{DD}	11
TMS	U26	I	OV_{DD}	12
TRST_B	V26	I	OV_{DD}	12
Power Management				
ASLEEP	U25	O	OV_{DD}	19
NC1	G6	NC	—	—
NC2	Y14	NC	—	—
NC3	Y15	NC	—	—
NC4	Y16	NC	—	—
NC5	AE10	NC	—	—
NC6	AF10	NC	—	—
NC9	E14	NC	—	—
NC10	E13	NC	—	—
NC15	W6	NC	—	—
Power and Ground Signals				
GND	AH10	—	—	—
GND	AJ10	—	—	—
GND	AD10	—	—	—
NC20	E16	NC	—	—
NC21	E15	NC	—	—
AGND_SRDS	AD15	—	—	—
AV_{DD}_CORE0	F16	—	—	17,32
NC	F15	—	—	17,32
AV_{DD}_DDR	Y10	—	—	17
NC102	F14	NC	—	17
AV_{DD}_PLAT	V24	—	—	17
AV_{DD}_SRDS	AD14	—	—	17
BV_{DD}	B24	—	—	—
BV_{DD}	C12	—	—	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
BV_{DD}	C14	—	—	—
BV_{DD}	C16	—	—	—
BV_{DD}	C22	—	—	—
BV_{DD}	D18	—	—	—
BV_{DD}	G20	—	—	—
CV_{DD}	C27	—	—	—
CV_{DD}	E25	—	—	—
CV_{DD}	E27	—	—	—
GV_{DD}	A2	—	—	—
GV_{DD}	B8	—	—	—
GV_{DD}	B11	—	—	—
GV_{DD}	C7	—	—	—
GV_{DD}	C9	—	—	—
GV_{DD}	D3	—	—	—
GV_{DD}	E7	—	—	—
GV_{DD}	F9	—	—	—
GV_{DD}	G10	—	—	—
GV_{DD}	H2	—	—	—
GV_{DD}	K3	—	—	—
GV_{DD}	K7	—	—	—
GV_{DD}	L2	—	—	—
GV_{DD}	L3	—	—	—
GV_{DD}	L4	—	—	—
GV_{DD}	N3	—	—	—
GV_{DD}	N6	—	—	—
GV_{DD}	P4	—	—	—
GV_{DD}	R2	—	—	—
GV_{DD}	U3	—	—	—
GV_{DD}	V5	—	—	—
GV_{DD}	W3	—	—	—
GV_{DD}	Y2	—	—	—
GV_{DD}	AA2	—	—	—
GV_{DD}	AA3	—	—	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GV_{DD}	AA5	—	—	—
GV_{DD}	AA7	—	—	—
GV_{DD}	AB6	—	—	—
GV_{DD}	AD5	—	—	—
GV_{DD}	AD9	—	—	—
GV_{DD}	AE3	—	—	—
GV_{DD}	AF4	—	—	—
GV_{DD}	AG6	—	—	—
GV_{DD}	AG8	—	—	—
GV_{DD}	AJ2	—	—	—
LV_{DD}	Y23	—	—	—
LV_{DD}	AC21	—	—	—
LV_{DD}	AC25	—	—	—
LV_{DD}	AC27	—	—	—
LV_{DD}	AE23	—	—	—
LV_{DD}	AF21	—	—	—
LV_{DD}	AF25	—	—	—
LV_{DD}	AH27	—	—	—
LV_{DD}	AH29	—	—	—
SV_{DD}_SRDS	AG16	—	—	—
SV_{DD}_SRDS	AH13	—	—	—
SV_{DD}_SRDS	AH17	—	—	—
SV_{DD}_SRDS	AJ11	—	—	—
SV_{DD}_SRDS	AJ15	—	—	—
SV_{DD}_SRDS	AJ19	—	—	—
SGND_SRDS	AG12	—	—	—
SGND_SRDS	AG13	—	—	—
SGND_SRDS	AG14	—	—	—
SGND_SRDS	AG17	—	—	—
SGND_SRDS	AG18	—	—	—
SGND_SRDS	AG19	—	—	—
SGND_SRDS	AH11	—	—	—
SGND_SRDS	AH15	—	—	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SGND_SRDS	AH19	—	—	—
SGND_SRDS	AJ13	—	—	—
SGND_SRDS	AJ17	—	—	—
XV_{DD}_SRDS	AD13	—	—	—
XV_{DD}_SRDS	AD17	—	—	—
XV_{DD}_SRDS	AE11	—	—	—
XV_{DD}_SRDS	AE19	—	—	—
XV_{DD}_SRDS	AF14	—	—	—
XV_{DD}_SRDS	AF16	—	—	—
XGND_SRDS	AD11	—	—	—
XGND_SRDS	AD19	—	—	—
XGND_SRDS	AE14	—	—	—
XGND_SRDS	AE16	—	—	—
XGND_SRDS	AF11	—	—	—
XGND_SRDS	AF12	—	—	—
XGND_SRDS	AF18	—	—	—
XGND_SRDS	AG10	—	—	—
MVREF	R6	—	—	—
OV_{DD}	K23	—	—	—
OV_{DD}	L25	—	—	—
OV_{DD}	N27	—	—	—
OV_{DD}	P25	—	—	—
OV_{DD}	U27	—	—	—
OV_{DD}	Y26	—	—	—
NC103	F13	—	—	—
NC104	P6	—	—	—
NC110	K10	—	—	—
NC111	K11	—	—	—
NC112	K12	—	—	—
NC113	K13	—	—	—
NC114	K14	—	—	—
NC115	L10	—	—	—
NC116	M10	—	—	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
V_{DDC}	K15	—	—	—
V_{DDC}	K17	—	—	—
V_{DDC}	K19	—	—	—
V_{DDC}	K16	—	—	—
V_{DDC}	L20	—	—	—
V_{DDC}	K18	—	—	—
V_{DDC}	K20	—	—	—
V_{DDC}	N10	—	—	—
V_{DDC}	N20	—	—	—
V_{DDC}	M20	—	—	—
V_{DDC}	R10	—	—	—
V_{DDC}	R20	—	—	—
V_{DDC}	P10	—	—	—
V_{DDC}	P20	—	—	—
V_{DDC}	U10	—	—	—
V_{DDC}	U20	—	—	—
V_{DDC}	T10	—	—	—
V_{DDC}	T20	—	—	—
V_{DDC}	W10	—	—	—
V_{DDC}	V10	—	—	—
V_{DDC}	V20	—	—	—
V_{DDC}	W20	—	—	—
V_{DDC}	Y11	—	—	—
V_{DDC}	Y19	—	—	—
GND	A1	—	—	—
GND	A29	—	—	—
GND	B5	—	—	—
GND	B14	—	—	—
GND	B27	—	—	—
GND	C6	—	—	—
GND	C8	—	—	—
GND	C11	—	—	—
GND	C18	—	—	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	C24	—	—	—
GND	D16	—	—	—
GND	D22	—	—	—
GND	D25	—	—	—
GND	E3	—	—	—
GND	E28	—	—	—
GND	F7	—	—	—
GND	G5	—	—	—
GND	G9	—	—	—
GND	G21	—	—	—
GND	H3	—	—	—
GND	H27	—	—	—
GND	J7	—	—	—
GND	J23	—	—	—
GND	K4	—	—	—
GND	F17	—	—	—
GND	L12	—	—	—
GND	L14	—	—	—
GND	L16	—	—	—
GND	L18	—	—	—
GND	M11	—	—	—
GND	K25	—	—	—
GND	L1	—	—	—
GND	L11	—	—	—
GND	L13	—	—	—
GND	L15	—	—	—
GND	L17	—	—	—
GND	L19	—	—	—
GND	M3	—	—	—
GND	M4	—	—	—
GND	M6	—	—	—
GND	M19	—	—	—
GND	M12	—	—	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	M13	—	—	—
GND	M14	—	—	—
GND	M15	—	—	—
GND	M16	—	—	—
GND	M17	—	—	—
GND	M18	—	—	—
GND	P11	—	—	—
GND	M26	—	—	—
GND	N2	—	—	—
GND	N11	—	—	—
GND	N12	—	—	—
GND	N13	—	—	—
GND	N14	—	—	—
GND	N15	—	—	—
GND	N16	—	—	—
GND	N17	—	—	—
GND	N18	—	—	—
GND	N19	—	—	—
GND	N28	—	—	—
GND	P5	—	—	—
GND	P19	—	—	—
GND	P12	—	—	—
GND	P13	—	—	—
GND	P14	—	—	—
GND	P15	—	—	—
GND	P16	—	—	—
GND	P17	—	—	—
GND	P18	—	—	—
GND	T11	—	—	—
GND	P24	—	—	—
GND	R3	—	—	—
GND	R11	—	—	—
GND	R12	—	—	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	R13	—	—	—
GND	R14	—	—	—
GND	R15	—	—	—
GND	R16	—	—	—
GND	R17	—	—	—
GND	R18	—	—	—
GND	R19	—	—	—
GND	T6	—	—	—
GND	T19	—	—	—
GND	T12	—	—	—
GND	T13	—	—	—
GND	T14	—	—	—
GND	T15	—	—	—
GND	T16	—	—	—
GND	T17	—	—	—
GND	T18	—	—	—
GND	V11	—	—	—
GND	T27	—	—	—
GND	U11	—	—	—
GND	U12	—	—	—
GND	U13	—	—	—
GND	U14	—	—	—
GND	U15	—	—	—
GND	U16	—	—	—
GND	U17	—	—	—
GND	U18	—	—	—
GND	U19	—	—	—
GND	V4	—	—	—
GND	V19	—	—	—
GND	V12	—	—	—
GND	V13	—	—	—
GND	V14	—	—	—
GND	V15	—	—	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	V16	—	—	—
GND	V17	—	—	—
GND	V18	—	—	—
GND	W12	—	—	—
GND	V27	—	—	—
GND	W2	—	—	—
GND	W4	—	—	—
GND	W11	—	—	—
GND	W13	—	—	—
GND	W14	—	—	—
GND	W15	—	—	—
GND	W16	—	—	—
GND	W17	—	—	—
GND	W19	—	—	—
GND	Y3	—	—	—
GND	Y6	—	—	—
GND	Y7	—	—	—
GND	W18	—	—	—
V_{DDC}	Y12	—	—	—
GND	Y13	—	—	—
GND	Y17	—	—	—
V_{DDC}	Y18	—	—	—
V_{DDC}	Y20	—	—	—
GND	Y25	—	—	—
GND	AA6	—	—	—
GND	AA23	—	—	—
GND	AC3	—	—	—
GND	AC10	—	—	—
GND	AC20	—	—	—
GND	AC24	—	—	—
GND	AC28	—	—	—
GND	AD3	—	—	—
GND	AD6	—	—	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	AE9	—	—	—
GND	AF20	—	—	—
GND	AG3	—	—	—
GND	AG5	—	—	—
GND	AG7	—	—	—
GND	AG24	—	—	—
GND	AG27	—	—	—
GND	AJ1	—	—	—
GND	AJ29	—	—	—

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

Note:

1. All multiplexed signals are listed only once and do not re-occur.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to OVDD.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kO pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[29:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 4.1.3, "CCB/SYSCLK PLL Ratio."
8. The value of LALE, LGPL2, LBCTL, LWE_B00, UART_SOUT1, and READY_PL, at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 4.1.4, "e500 Core PLL Ratio."
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
10. If this pin is configured for local bus controller usage, recommend a weak pull-up resistor (2-10 KΩ) be placed on this pin to BVDD, to ensure no random chip select assertion due to possible noise and etc.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the VDD/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
15. Do not connect.
16. These are test signals for factory use only and must be pulled up (100 Ω–1 kΩ) to OVDD for normal machine operation.
17. Independent supplies derived from board VDD.
18. Recommend a pull-up resistor (~1 kΩ) be placed on this pin to OVDD.
19. The following pins must NOT be pulled down during power-on reset: LA[17],, $\overline{\text{HRESET\_REQ}}$, MSRCID[1:4], MDVAL, ASLEEP.
22. cfg_dram_type must be valid at powerup, even before HRESET assertion.
23. For DDR2 MDIC[0] is grounded through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor and Dn_MDIC[1] is connected to GVDD through an 18.2-Ω (full-strength mode) or 36.4-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs. The calibration resistor value for DDR3 should be 20-Ω(full-strength mode) or 40-Ω (half-strength mode).
24. These pins have other manufacturing or debug test functions. It's recommended to add both pull-up resistor pads to OVDD and pull-down resistor pads to GND on board to support future debug testing when needed.

Table 1. P10 12 Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

25. DDRCLK input is only required when the DDR controller is running in asynchronous mode. When the DDR controller is configured to run in synchronous mode via POR setting cfg_ddr_pll[0:2]=111, the DDRCLK input is not required. It is recommended to tie it off to GND when DDR controller is running in synchronous mode. See the *QorIQ™ Integrated Host Processor Family Reference Manual*, Table 4-3 in Section 4.2.2, “Clock Signals”, Section 4.4.3.2, “DDR PLL Ratio” and Table 4-10, “DDR Complex Clock PLL Ratio” for more detailed description regarding DDR controller operation in asynchronous and synchronous modes
26. EC_GTX_CLK125 is a 125-MHz input clock shared among all eTSEC ports in the following modes: GMII, TBI, RGMII and RTBI. If none of the eTSEC ports is operating in these modes, the EC_GTX_CLK125 input can be tied off to GND.
27. These POR configuration inputs may be used in the future to control functionality. It is adviced that boards are built with the ability to pullup or pulldown these pins .LA[20:22], UART_SOUT[0], TRIG_OUT, MSRCID[1], MSRCID[4], and DMAI_DDONE_B00 are resesrved for future reset configuration.
28. Incorrect settings can lead to irreversible device damage.
29. The value of LAD[0:15] during reset sets the upper 16 bits of the GPPORCR.
30. The value of TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, and TSEC_1588_PULSE_OUT2, during reset is used to set the DDR clock PLL settings. These pins require 4.7 kΩ pull up or pul down resistors. See Section 4.1.5, “DDR/DDRCLK PLL Ratio.”
31. The value of LA27 and LA16 during reset is used to determine CPU boot configuration. See Section 4.4.3.7, “CPU boot POR Configuration,” in the applicable device reference manual.
32. It must be the same as V_{DD}_Core.
33. When eTSEC1 and eTSEC3 are used as parallel interfaces, pins TSEC1_TX_EN and TSEC3_TX_EN requires an external 4.7-k_ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven. However, because of the pull-down resistor on TSEC3_TX_EN cause the eSDHC card-detect (cfg_sdhc_cd_pol_sel) to be inverted, the inversion should be overridden from the SDHCDCR [CD_INV] debug control register.
34. SD_IMP_CAL_RX is grounded through an 200-Ω precision 1% resistor and SD_IMP_CAL_TX is grounded through an 100-Ω precision 1% resistor.
35. This pin is a reset configure pin. if driven from external logic a bus switch should be enabled during assertion of PORESET

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the P1012. The P1012 is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 2 provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings [1]

Characteristic	Symbol	Max Value	Unit	Notes
Core 0 and Platform supply voltage	V_{DDC}	–0.3 to 1.05	V	—
PLL supply voltage	AV_{DD}_CORE0 AV_{DD}_DDR AV_{DD}_PLAT AV_{DD}_SRDS	–0.3 to 1.05	V	8
Core power supply for SerDes transceivers	SV_{DD}_SRDS	–0.3 to 1.05	V	—
Pad power supply for SerDes transceivers	XV_{DD}_SRDS	–0.3 to 1.05	V	—
DDR2/3 DRAM I/O voltage	GV_{DD}	–0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage (eTSEC)	LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	1,4
DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	—
USB, eSPI, eSDHC	CV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Enhanced local bus I/O voltage and GPIOx8 voltage	BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—

Table 2. Absolute Maximum Ratings [1] (continued)

Characteristic		Symbol	Max Value	Unit	Notes
Input voltage	DDR2/DDR3 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 7
	DDR2/DDR3 DRAM reference	MV_{REF}	–0.3 to (GV_{DD}/2 + 0.3)	V	—
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	3, 7
	Enhanced local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	5
	DUART, SYSCLK, system control and power management, I^2C, clocking, I/O voltage select, and JTAG I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6, 7
	USB, eSPI, eSDHC	CV_{IN}	–0.3 to (CV_{DD} + 0.3)	V	4
	Serdes signals	XV_{IN}	–0.3 to (XV_{DD} + 0.3)	V	—
Storage temperature range		T_{STG}	–55 to 150	°C	—

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: MVIN must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. Caution: LVIN must not exceed LVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. Caution: CVIN must not exceed CVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. Caution: BVIN must not exceed BVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. Caution: OVIN must not exceed OVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. (C,X,B,G,L,O)VIN and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 8.
8. AV_{DD} is measured at the input to the filter and not at the pin of the device.

2.1.2 Recommended Operating Conditions

Table 3 provides the recommended operating conditions for this device. Note that the values in Table 3 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

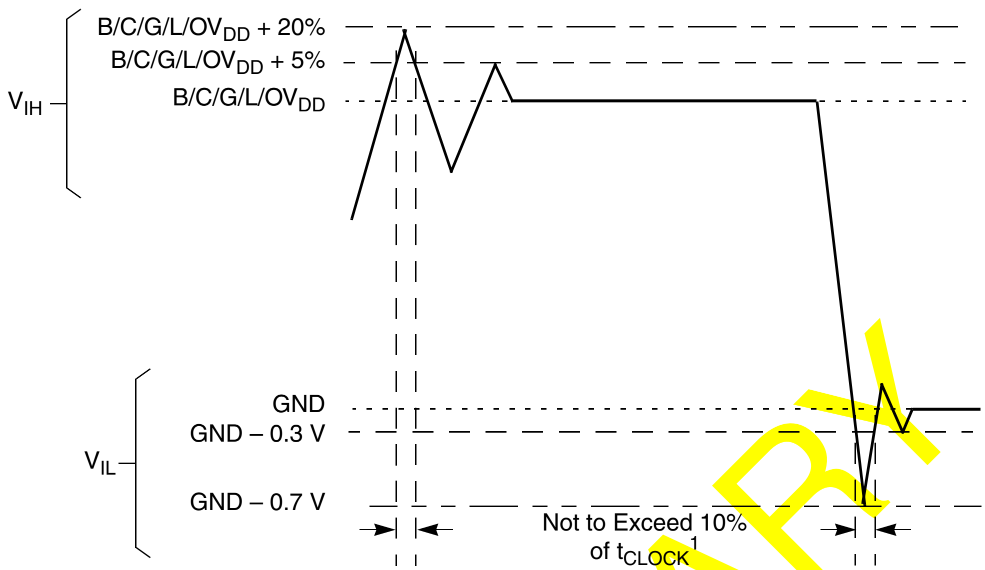
Table 3. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Core 0 and Platform supply voltage		V_{DDC}	1.0± 50 mV	V	1
PLL supply voltage		AV_{DD}_CORE0 AV_{DD}_DDR AV_{DD}_PLAT AV_{DD}_SRDS	1.0± 50 mV	V	—
Core power supply for SerDes transceivers		SV_{DD}_SRDS	1.0± 50 mV	V	—
Pad power supply for SerDes transceivers and PCI Express		XV_{DD}_SRDS	1.0± 50 mV	V	—
DDR2 DRAM I/O voltage		GV_{DD}	1.8 V ± 90 mV	V	—
DDR3 DRAM I/O voltage		GV_{DD}	1.5 V ± 75 mV	—	—
Three-speed Ethernet I/O voltage (eTSEC)		LV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
DUART, system control and power management, I^2C, QE, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
Enhanced local bus I/O and QUICC Engine (QE) voltage		BV_{DD}	3.3 V ± 165 mV	V	—
USB, eSPI, eSDHC		CV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Input voltage	DDR2/3 DRAM signals	MV_{IN}	GND to GV_{DD}	V	—
	DDR2/3 DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	—
	Three-speed Ethernet signals	LV_{IN}	GND to LV_{DD}	V	—
	Enhanced local bus signals	BV_{IN}	GND to BV_{DD}	V	—
	DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	—
	USB, eSPI, eSDHC	CV_{IN}	GND to CV_{DD}	V	—
Junction Temperature range		TA/TJ	0 to 125 Commercial –40 to 125 Industrial	°C	3

Notes:

1. **Caution:** Until V_{DD} reaches its recommended operating voltage, V_{DD} may exceed L/C/B/G/OV_{DD} by up to 0.7 V. If 0.7 V is exceeded, extra current will be drawn by the device.
2. **Caution:** Until V_{DD} reaches its recommended operating voltage, if L/C/B/G/OV_{DD} exceeds V_{DD} extra current may be drawn by the device.
3. Min temp is specified with TA; Max temp is specified with TJ

Figure 8 shows the undershoot and overshoot voltages at the interfaces of the P1012.



Note:

1. t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^{2}C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
   For eLBC, t_{CLOCK} references LCLK.

Figure 8. Overshoot/Undershoot Voltage for $BV_{DD}/CV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}$

The core voltage must always be provided at nominal 1.0 V(See Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The SDRAM interface uses a differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$). The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.3 Output Driver Characteristics

Table 4 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage	Notes
Enhanced local bus interface, GPIO[0:7]	45 45 45	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	—
DDR2/3 signal (Programmable)	16 32 (half strength mode)	GV_{DD} = 1.8 V DDR2 GV_{DD} = 1.5 V DDR3	1

Table 4. Output Drive Capability (continued)

Driver Type	Output Impedance (Ω)	Supply Voltage	Notes
TSEC signals	45	LV_{DD} = 2.5/3.3 V	—
DUART, system control, JTAG	45	OV_{DD} = 3.3 V	—
I^2C	45	OV_{DD} = 3.3 V	—
USB, SPI, eSDHC	45	CV_{DD} = 3.3 V CV_{DD} = 2.5 V CV_{DD} = 1.8 V	—

Notes:

1. The drive strength of the DDR2/3 interface in half-strength mode is at T_j = 105°C and at GV_{DD} (min)

2.2 Power Sequencing

The P1012 requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD}, V_{DDC}, AV_{DD}, BV_{DD}, LV_{DD}, $CV_{DD,}$ OV_{DD}, SV_{DD_SRDS} and, XV_{DD_SRDS}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GV_{DD} is not required.

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

2.3 Power Characteristics

The estimated typical core power dissipation for the core complex bus (CCB) versus the core frequency for this family of QorIQ devices is shown in Table 5.

Table 5. 12 Core Power Dissipation

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V_{DD} (V)	Junction Temperature (°C)	Power (W)	Notes
Typical	533	267	1.0	65	TBD	1, 2
Thermal				125	TBD	1, 3
Maximum					TBD	1, 4
Typical	667	333	1.0	65	TBD	1, 2
Thermal				125	TBD	1, 3
Maximum					TBD	1, 4

Table 5. 12 Core Power Dissipation

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V_{DD} (V)	Junction Temperature (°C)	Power (W)	Notes
Typical	800	400	1.0	65	TBD	1, 2
Thermal				125	TBD	1, 3
Maximum					TBD	1, 4

Notes:
1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}) and 65°C junction temperature (see Table 3) while running the Dhrystone 2.1 benchmark.
3. Thermal power is the average power measured at nominal core voltage (V_{DD}) and maximum operating junction temperature (see Table 3) while running the Dhrystone 2.1 benchmark.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}) and maximum operating junction temperature (see Table 3) while running a smoke test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep the execution unit maximally busy.

At allowable voltage levels, the estimated power dissipation on the 1.0-V AV_{DD} supplies for the 12PLLs is TBD.

2.4 Input Clocks

2.4.1 System Clock Timing

Table 6 provides the system clock (SYSCLK) DC specifications for the 12.

Table 6. SYSCLK DC Electrical Characteristics (OV_{DD} = 3.3 V ± 165 mV)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
High-level input voltage	V_{IH}	2.0	—	—	V	1
Low-level input voltage	V_{IL}	—	—	0.8	V	1
Input Capacitance	C_{IN}	—	7	15	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DD})	I_{IN}	—	—	±50	μA	2

Note:
1. The max V_{IH}, and min V_{IL} values can be found in Table 3
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced inTable 3

Table 7 provides the system clock (SYSCLK) AC timing specifications for the P1012.

Table 7. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	64	—	100	MHz	1
SYSCLK cycle time	t_{SYSCLK}	10	—	15	ns	—
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	2

Table 7. SYSCLK AC Timing Specifications (continued)

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK jitter phase npise at – 56dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Notes:

1. **Caution:** The CCB_clk to SYSCLK ratio and e500 core to CCB_clk ratio settings must be chosen such that the resulting SYSCLK frequency, e500 core frequency, and CCB_clk frequency do not exceed their respective maximum or minimum operating frequencies.Refer to Section 4.1.3, "CCB/SYSCLK PLL Ratio," and Section 4.1.4, "e500 Core PLL Ratio" for ratio settings. Refer to Section 4.1.3, "CCB/SYSCLK PLL Ratio," and Section 4.1.4, "e500 Core PLL Ratio" for ratio settings.
2. Measured at the rising edge and/or the falling edge at OV_{DD}/2.
3. Slew rate as measured from +/- 0.3 ΔV_{AC} at center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.4.2 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 8 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the P1012 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the P1012 is compatible with spread spectrum sources if the recommendations listed in Table 8 are observed.

Table 8. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 3.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Note:

1. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 7.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device

CAUTION

The processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.

2.4.3 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

2.4.4 eTSEC Gigabit Reference Clock Timing

Table 9 lists the eTSEC gigabit reference clock DC electrical characteristics for the P1012.

Table 9. eTSEC Gigabit Reference Clock DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	—	V	1
Low-level input voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±40	μA	2

Note:
1. The max V_{IH}, and min V_{IL} values can be found in Table 3
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3

Table 10 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the P1012.

Table 10. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK rise and fall time LV_{DD} = 2.5V LV_{DD} = 3.3V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	 47	—	 53	%	2,3

Notes:
1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5V and 2.0V for LV_{DD}=2.5V, and from 0.6 and 2.7V for LV_{DD}=3.3V at 0.6 V and 2.7 V.
2. .EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 2.9.3.2, “RGMII AC Timing Specifications” for duty cycle for 10Base-T and 100Base-T reference clock.

2.4.5 DDR Clock Timing

Table 11 provides the system clock (DDRCLK) DC specifications for the P1012

Table 11. DDRCLK DC Electrical Characteristics (OV_{DD} = 3.3 V ± 165 mV)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
High-level input voltage	V_{IH}	2.0	—	OV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	—	0.8	V	—
Input Capacitance	C_{IN}	—	7	15	pf	—
Input current (V_{IN}[1] = 0 V or V_{IN} = $V_{DD)}$	I_{IN}	—	—	±50	μA	—

Note:

1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

Table 12 provides the DDR clock (DDRCLK) AC timing specifications for the P1012

Table 12. DDRCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}	66.7	—	166.7	MHz	1, 2
DDRCLK cycle time	t_{DDRCLK}	6	—	15	ns	1, 2
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	40	—	60	%	2
DDRCLK slew rate	—	1	—	4	V/ns	3
DDRCLK peak period jitter	—	—	—	± 150	ps	—
DDRCLK jitter phase npise at – 56dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Notes:

1. **Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. Refer to Section 4.1.5, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from +/- 0.3 ΔV_{AC} at center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes and eTSEC, see the specific section of this document.

2.5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the P1012. Table 13 provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 13. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HREST}}$	25	—	µs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	µs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1, 2

Notes:
1. SYSCLK is the primary clock input for the P1012.
2.)HRESET should have a rise time of no less than one sysclk cycle.

Table 14 provides the PLL lock times.

Table 14. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—

2.6 DDR2 and DDR3 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the P1012. Note that the required GV_{DD}(typ) voltage is 1.8 V or 1.5 V when interfacing to DDR2 or DDR3 SDRAM respectively.

2.6.1 DDR SDRAM DC Electrical Characteristics

Table 15 provides the recommended operating conditions for the DDR SDRAM component(s) of the P1012 when interfacing to DDR2 SDRAM.

Table 15. DDR2 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.8 V[1]

Parameter	Symbol	Min	Max	Unit	Notes
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2, 3, 4
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	—	V	5
Input low voltage	V_{IL}	—	$MV_{REF} - 0.125$	V	5

Table 15. DDR2 SDRAM Interface DC Electrical Characteristics (continued)

At recommended operating condition with GV_{DD} = 1.8 V[1]

Parameter	Symbol	Min	Max	Unit	Notes
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	6
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	6
I/O leakage current	I_{OZ}	–50	50	μA	7

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MV_{REF} with a min value of MV_{REF} – 0.04 and a max value of MV_{REF} + 0.04. V_{TT} should track variations in the DC level of MV_{REF}
4. The voltage regulator for MV_{REF} must be able to supply up to 1500 μA.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Refer to the IBIS model for the complete output IV curve characteristics.
7. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 16 provides the DDR controller interface capacitance for DDR2 and DDR3.

Table 16. DDR2 DDR3 SDRAM Capacitance

At recommended operating conditions with GV_{DD} of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3

Parameter	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1, 2

Note:

1. This parameter is sampled. GVDD = 1.8 V ± 0.1 V (for DDR2), f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.
2. This parameter is sampled. GVDD = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.175 V.

Table 17 provides the current draw characteristics for MV_{REF}.

Table 17. Current Draw Characteristics for MV_{REF}

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Current draw for DDR2 SDRAM for MV_{REF}	MV_{REF}	—	1500	μA	—
Current draw for DDR3 SDRAM for MV_{REF}	MV_{REF}	—	1250	μA	—

2.6.2 DDR2 and DDR3 SDRAM Interface AC Timing Specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that the required GV_{DD}(typ) voltage is 1.8 V or 1.5 V when interfacing to DDR2 or DDR3 SDRAM respectively.

2.6.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

Table 18 provides the input AC timing specifications for the DDR controller when interfacing to DDR2 SDRAM.

Table 18. DDR2 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GVDD of 1.8 V ± 5%

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	≥ 667 MHz data rate	V_{ILAC}	—	MV_{REF} – 0.20	V	—
	≤ 533 MHz data rate		—	MV_{REF} – 0.25		
AC input high voltage	≥ 667 MHz data rate	V_{IHAC}	MV_{REF} + 0.20	—	V	—
	≤ 533 MHz data rate		MV_{REF} + 0.25	—		

Table 19 provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 19. DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GVDD of 1.5 V ± 5%

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{ILAC}	—	MV_{REF} – 0.175	V	—
AC input high voltage	V_{IHAC}	MV_{REF} + 0.175	—	V	—

Table 20 provides the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

Table 20. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GVDD of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1
667 MHz data rate		–390	390		1
533 MHz data rate		–450	450		1
400 MHz data rate		–515	515		1

Table 20. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications (continued)

At recommended operating conditions with GVDD of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3

Parameter	Symbol	Min	Max	Unit	Notes
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}	—	—	ps	3
667 MHz data rate		–360	360		3
533 MHz data rate		–488	488		3
400 MHz data rate		–733	733		3

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. DDR3 only
3. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

Figure 9 shows the DDR2 and DDR3 SDRAM interface input timing diagram.

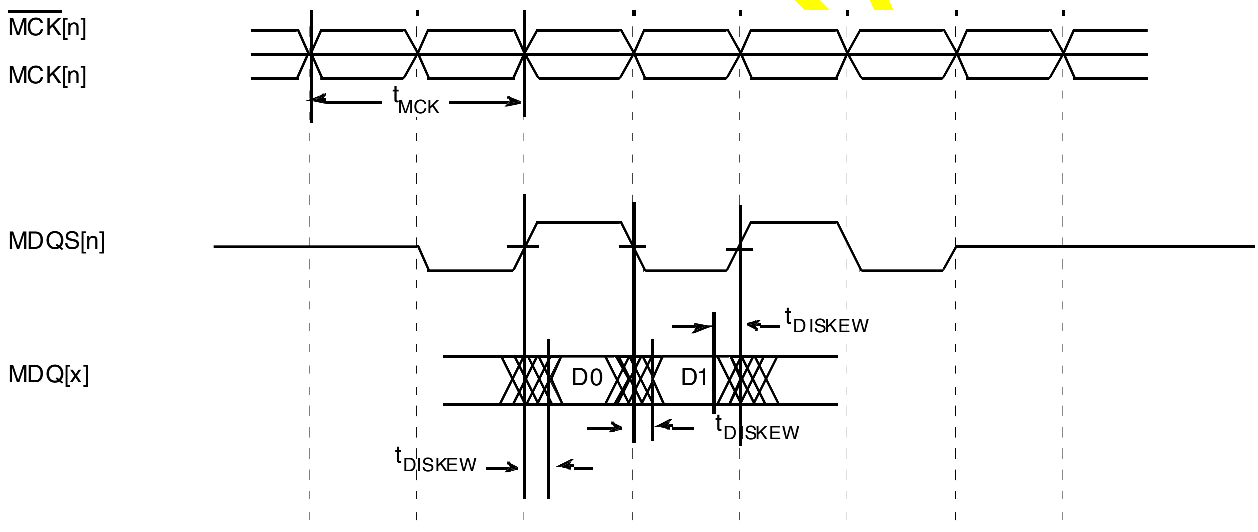


Figure 9. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

2.6.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

Table 21 contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

Table 21. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

At recommended operating conditions with GVDD of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}	—	—	ns	3
667 MHz data rate		1.10	—		3
533 MHz data rate		1.48	—		3
400 MHz data rate		1.95	—		3
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}	—	—	ns	3
667 MHz data rate		1.10	—		3
533 MHz data rate		1.48	—		3
400 MHz data rate		1.95	—		3
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}	—	—	ns	3
667 MHz data rate		1.10	—		3
533 MHz data rate		1.48	—		3
400 MHz data rate		1.95	—		3
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}	—	—	ns	3
667 MHz data rate		1.10	—		3
533 MHz data rate		1.48	—		3
400 MHz data rate		1.95	—		3
MCK to MDQS Skew	t_{DDKHMH}	—	—	ns	4
≤ 667 MHz data rate		–0.6	0.6		4

Table 21. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GVDD of 1.8 V ± 5% for DDR2 or 1.5 V ± 5% for DDR3

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}	—	—	ps	5
667 MHz data rate		300	—		5
533 MHz data rate		388	—		5
400 MHz data rate		550	—		5
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}	—	—	ps	5
667 MHz data rate		300	—		5
533 MHz data rate		388	—		5
400 MHz data rate		550	—		5
MDQS preamble	t_{DDKHMP}	$0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	—

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ and MCDQS/$\overline{\text{MCDQS}}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *P10PowerQUICC™ III Integrated Host Processor Family Reference Manual* for a description and explanation of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.

NOTE

For the ADDR/CMD setup and hold specifications in Table 21, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

Figure 10 shows the DDR2 and DDR3 SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

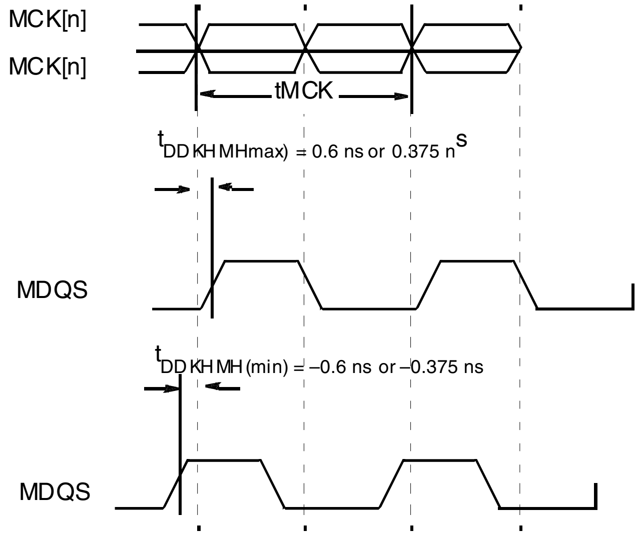


Figure 10. t_{DDKHMH} Timing Diagram

Figure 11 shows the DDR2 and DDR3 SDRAM output timing diagram.

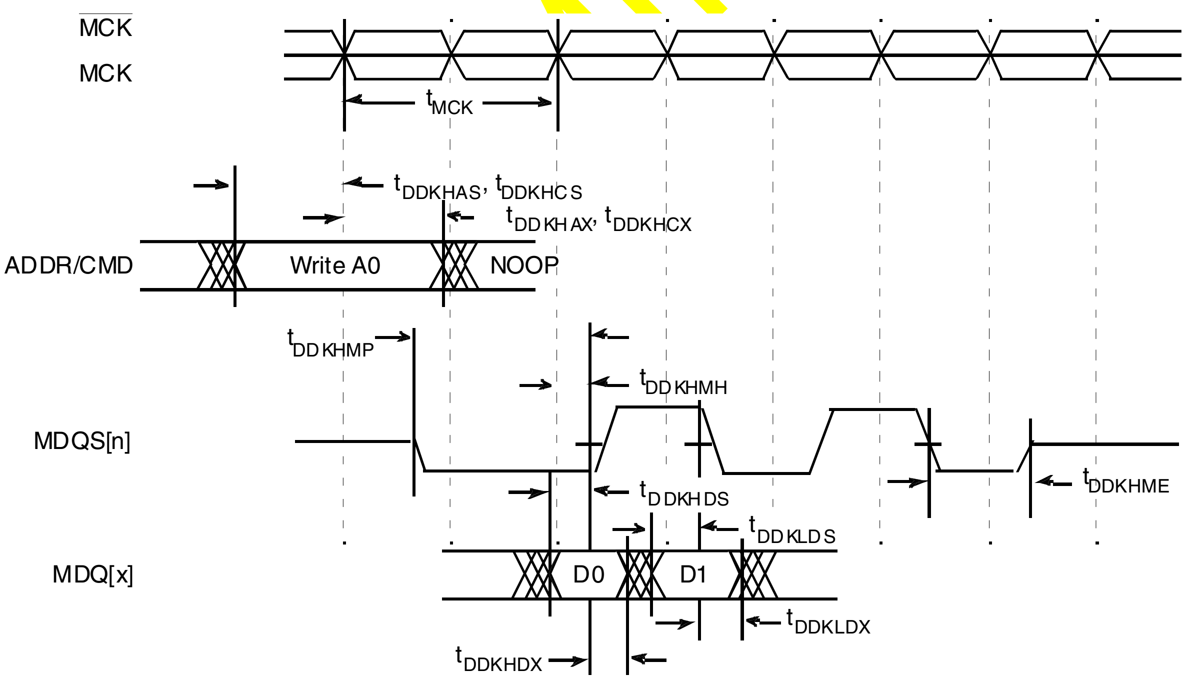


Figure 11. DDR2 and DDR3 Output Timing Diagram

Figure 12 provides the AC test load for the DDR2 and DDR3 controller bus.

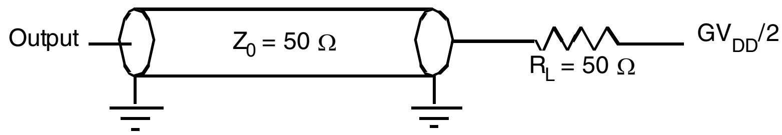


Figure 12. DDR2 and DDR3 Controller Bus AC Test Load

2.6.2.3 DDR2 and DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR2 and DDR3 SDRAM controller interface. Figure 13 shows the differential timing specification.

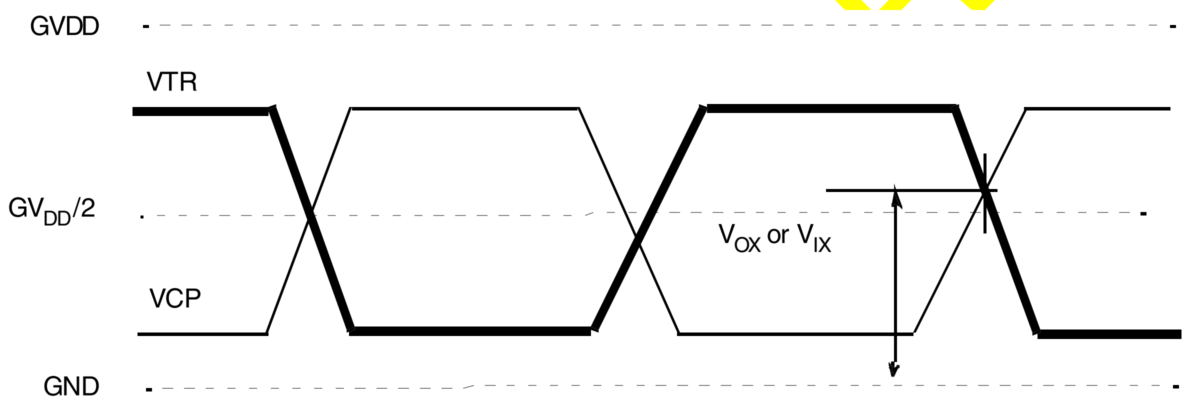


Figure 13. DDR2 and DDR3 SDRAM Differential Timing Specifications

NOTE

VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

Table 22 provides the DDR2 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 22. DDR2 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Input AC Differential Cross-Point Voltage	V_{IXAC}	0.5 × GVDD – 0.175	0.5 × GVDD + 0.175	V	—
Output AC Differential Cross-Point Voltage	V_{OXAC}	0.5 × GVDD – 0.125	0.5 × GVDD + 0.125	V	—

Table 23 provides the DDR3 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 23. DDR3 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Input AC Differential Cross-Point Voltage	V_{IXAC}	0.5 × GVDD – 0.150	0.5 × GVDD + 0.150	V	—
Output AC Differential Cross-Point Voltage	V_{OXAC}	0.5 × GVDD – 0.115	0.5 × GVDD + 0.115	V	—

2.7 eSPI

This section describes the DC and AC electrical specifications for the SPI of the P1012.

2.7.1 eSPI DC Electrical Characteristics

Table 26 provides the DC electrical characteristics for eSPI interface at CV_{DD}.=3.3V

Table 24. SPI DC Electrical Characteristics (3.3V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (0 V ≤ V_{IN} ≤ CV_{DD})	I_{IN}	—	±10	μA	2
Output high voltage (I_{OH} = –6.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (I_{OL} = 6.0mA)	V_{OL}	—	0.5	V	—
Output low voltage (IOL = 3.2mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 32.Note that the symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions".

Table 25 provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 2.5 V.

Table 25. SPI DC Electrical Characteristics (2.5 V)

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	1.7	—	V	1
Low-level input voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
High-level output voltage (CV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Low-level output voltage (CV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

Table 26 provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 1.8 V.

Table 26. SPI DC Electrical Characteristics (1.8 V)

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	1.25	—	V	1
Low-level input voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
High-level output voltage (CV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Low-level output voltage (CV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions"

2.7.2 eSPI AC Timing Specifications

Table 27 provides the SPI input and output AC timing specifications.

Table 27. SPI AC Timing Specifications [1]

For recommended operating conditions, see Table 3

Characteristic	Symbol	Min	Max	Unit	Note
SPI outputs—Master data (internal clock) hold time	t_{NIKHOX}	0.5	— —	ns	2
SPI outputs—Master data (internal clock) delay	t_{NIKHOV}	— —	6.0	ns	2
SPI_CS outputs—Master data (internal clock) hold time	$t_{NIKHOX2}$	0	—	ns	2
SPI_CS outputs—Master data (internal clock) delay	$t_{NIKHOV2}$	—	6.0	ns	2
SPI inputs—Master data (internal clock) input setup time	t_{NIIVKH}	5	—	ns	—
SPI inputs—Master data (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Figure 14 provides the AC test load for the SPI.

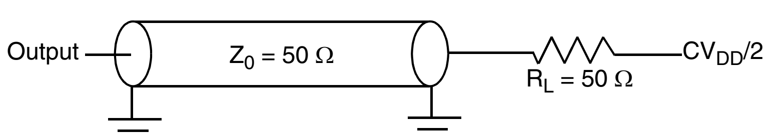


Figure 14. SPI AC Test Load

Figure 15 represents the AC timing from Table 27 in master mode (internal clock). Note that although the specifications are generally refer to the rising edge of the clock, Figure 14 also apply when the falling edge is the active edge. Also, note that the clock edge is selectable on SPI.

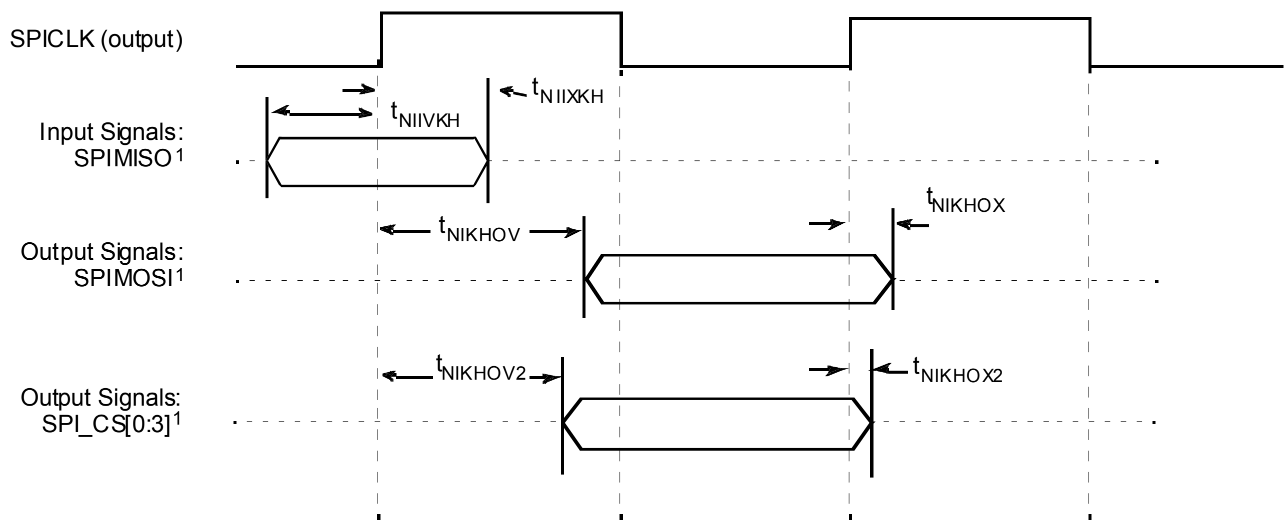


Figure 15. SPI AC Timing in Master Mode (Internal Clock) Diagram

2.8 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the P1012.

2.8.1 DUART DC Electrical Characteristics

Table 28 provides the DC electrical characteristics for the DUART interface.

Table 28. DUART DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Figure 3
2. Note that the symbol OVIN represents the input voltage of the supply. It is referenced in Figure 3

2.8.2 DUART AC Electrical Specifications

Table 29 provides the AC timing parameters for the DUART interface.

Table 29. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	CCB clock/1,048,576	baud	1
Maximum baud rate	CCB clock/16	baud	2
Oversample rate	16	—	3

Notes:

1. CCB clock refers to the platform clock.
2. Actual attainable baud rate will be limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

2.9 Ethernet: Enhanced Three-Speed Ethernet (eTSEC) (10/100/1000 Mbps)— MII/RMII/RGMII/SGMII Electrical Characteristics

The electrical characteristics specified here apply to all serial gigabit media independent interface (SGMII), media independent interface (MII), The RGMII interfaces are defined for 2.5 V, while the MII interfaces can be operated at 3.3 or 2.5 V. Whether the MII interface is operated at 3.3 or 2.5 V, the timing is compliant with IEEE 802.3®. The SGMII interfaces conforms (with exceptions) to the *Serial Gigabit Media-Independent Interface (SGMII) Specification, Version 1.8*. The RGMII interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification, Version 1.3* (12/10/2000). The electrical characteristics for MDIO and MDC are specified in Section 2.9.5, “MII Management.”

2.9.1 MII Interface Electrical Specifications

This section provides AC and DC electrical characteristics of MII interface for eTSEC.

2.9.1.1 MII and RMII DC Electrical Characteristics

All MII drivers and receivers comply with the DC parametric attributes specified in Table 37 and Table 33.

Table 30. MII DC Electrical Characteristics a tLV_{DD} = 3.3V

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage (LV_{DD} = min, I_{OH} = –4.0 mA)	V_{OH}	2.40	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 4.0 mA)	V_{OL}	—	0.40	V	—
Input high voltage (MII, RMII and TBI)	V_{IH}	2.0	—	V	—
Input high voltage (GMII)	V_{IH}	1.90	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	40	μA	1

Table 30. MII DC Electrical Characteristics (continued)a tLV$_{DD}$ = 3.3V

Parameter	Symbol	Min	Max	Unit	Notes
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	1

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

2.9.1.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

2.9.1.2.1 MII Transmit AC Timing Specifications

Table 31 provides the MII transmit AC timing specifications.

Table 31. MII Transmit AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	$t_{MTXH/}t_{MTX}$	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns

Figure 16 shows the MII transmit AC timing diagram.

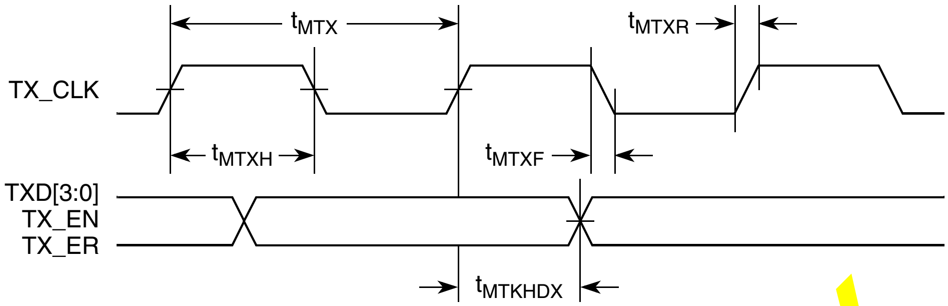


Figure 16. MII Transmit AC Timing Diagram

2.9.1.2.2 MII Receive AC Timing Specifications

Table 32 provides the MII receive AC timing specifications.

Table 32. MII Receive AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns

Figure 17 provides the AC test load for eTSEC.

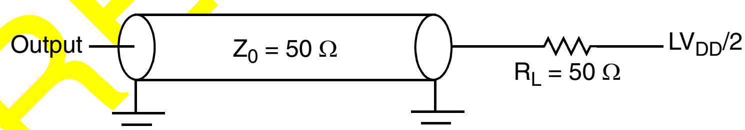


Figure 17. eTSEC AC Test Load

Figure 18 shows the MII receive AC timing diagram.

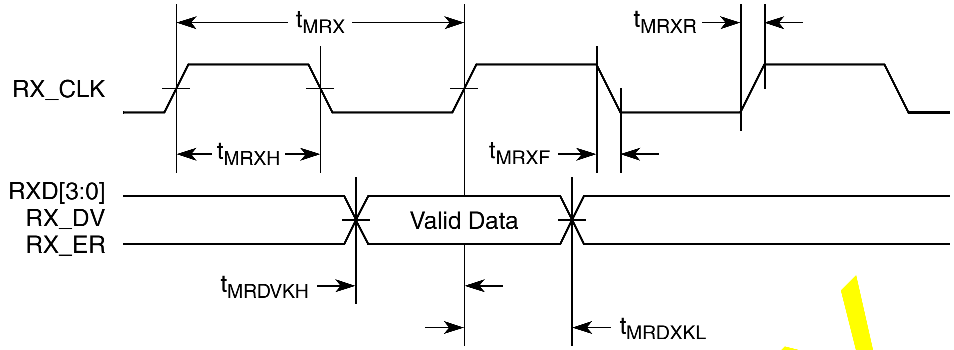


Figure 18. MII Receive AC Timing Diagram

2.9.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

Table 33 lists the RMII transmit AC timing specifications.

Table 33. RMII Transmit AC Timing Specifications

For recommended operating conditions, see Table ?

Parameter	Symbol	Min	Typ	Max	Unit
TSEC*n*_TX_CLK clock period	t_{RMT}	—	20.0	—	ns
TSEC*n*_TX_CLK duty cycle	t_{RMTH}	35	—	65	%
TSEC*n*_TX_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time TSEC*n*_TX_CLK (20%–80%)	t_{RMTR}	1.0	—	5.0	ns
Fall time TSEC*n*_TX_CLK (80%–20%)	t_{RMTF}	1.0	—	5.0	ns
TSEC*n*_TX_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Figure 19 shows the RMII transmit AC timing diagram.

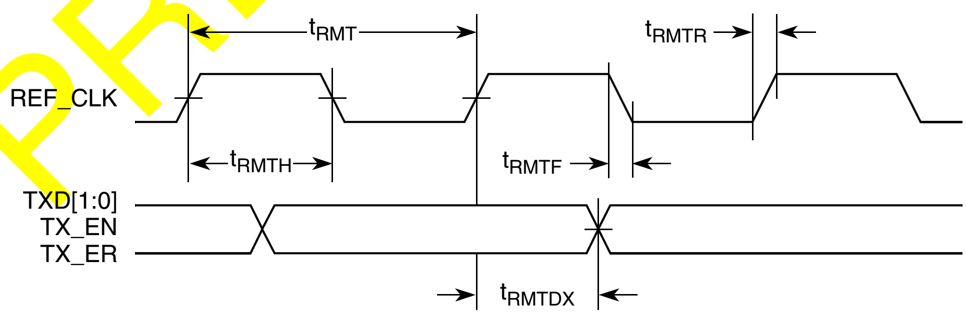


Figure 19. RMII Transmit AC Timing Diagram

Table 34 lists the RMII receive AC timing specifications.

Table 34. RMII Receive AC Timing Specifications

For recommended operating conditions, see Table ?

Parameter	Symbol	Min	Typ	Max	Unit
TSEC*n*_RX_CLK clock period	t_{RMR}	—	20.0	—	ns
TSEC*n*_RX_CLK duty cycle	t_{RMRH}	35	—	65	%
TSEC*n*_RX_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time TSEC*n*_RX_CLK (20%–80%)	t_{RMRR}	1.0	—	5.0	ns
Fall time TSEC*n*_RX_CLK (80%–20%)	t_{RMRF}	1.0	—	5.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to TSEC*n*_RX_CLK rising edge	t_{RMRDV}	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to TSEC*n*_RX_CLK rising edge	t_{RMRDX}	2.0	—	—	ns

Figure 20 provides the AC test load for eTSEC.

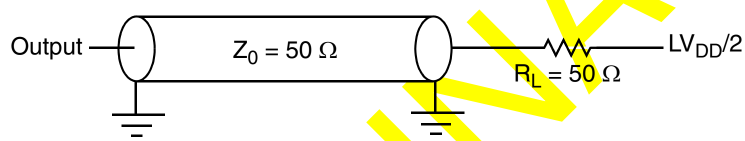


Figure 20. eTSEC AC Test Load

Figure 21 shows the RMII receive AC timing diagram.

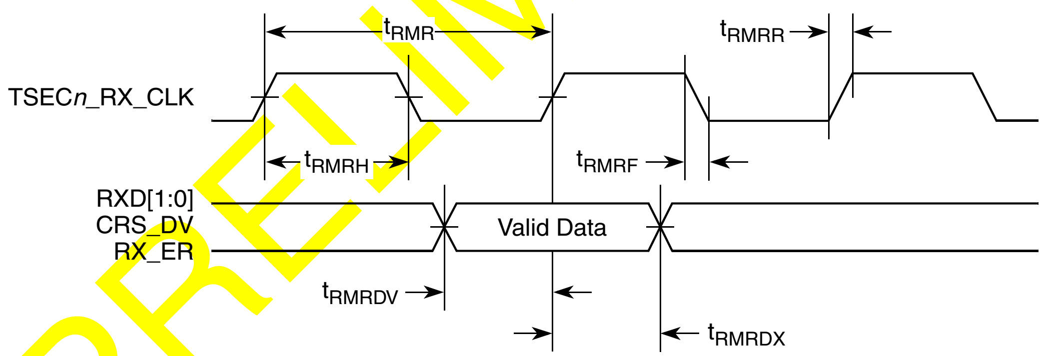


Figure 21. RMII Receive AC Timing Diagram

2.9.3 RGMII Interface Electrical Specifications

This section provides AC and DC electrical characteristics of RGMII interface for eTSEC.

2.9.3.1 RGMII DC Electrical Characteristics

Table 35 shows the RGMII DC electrical characteristics when operating from a 2.5V supply.

Table 35. RGMII DC Electrical Characteristics (2.5V)

At recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.70	V	—
Input high current ($V_{IN} = LV_{DD}$)	I_{IH}	—	10	μA	—
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	1
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 3.

2.9.3.2 RGMII AC Timing Specifications

Table 36 presents the RGMII and RTBI AC timing specifications.

Table 36. RGMII AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	—
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

Figure 22 shows the RGMII and RTBI AC timing and multiplexing diagrams.

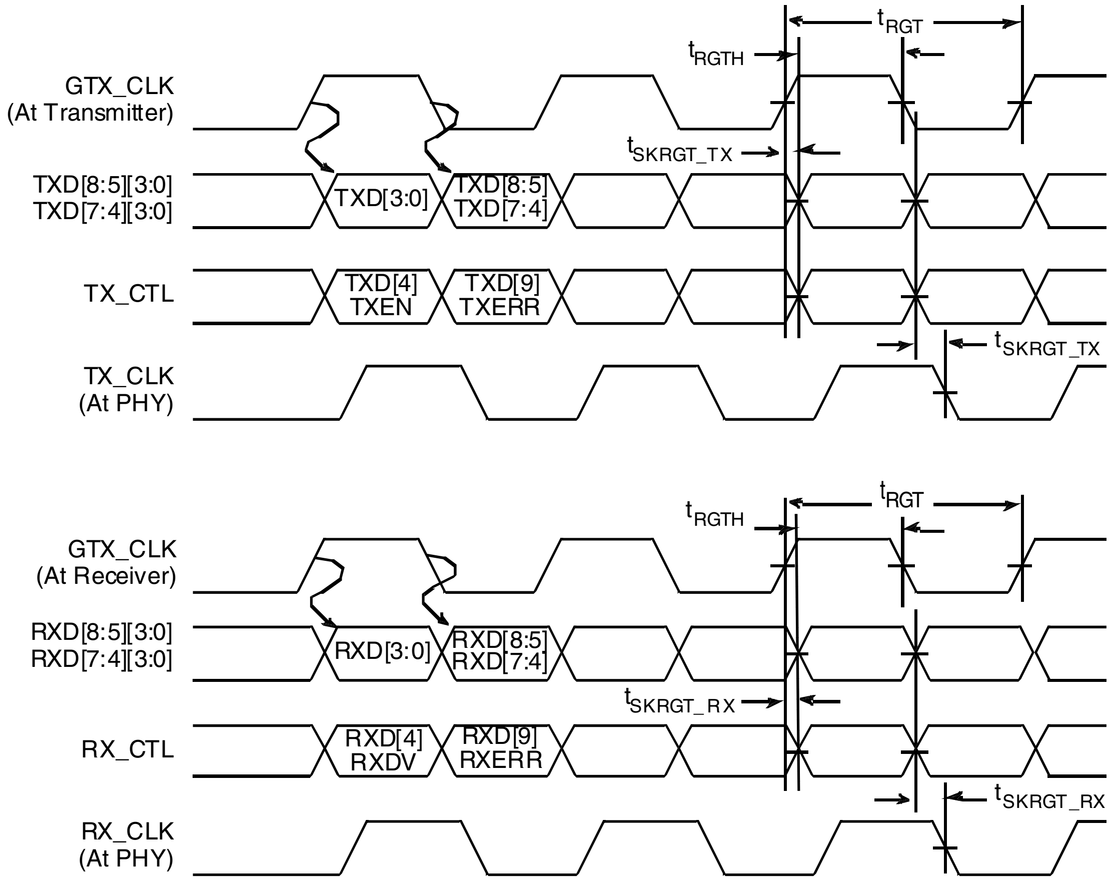


Figure 22. RGMII AC Timing and Multiplexing Diagrams

2.9.4 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the dedicated SerDes interface of P1012 as shown in Figure 24, where C_{TX} is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to SGND_SRDS. The reference circuit of the SerDes transmitter and receiver is shown in Figure 49.

2.9.4.1 SGMII DC Electrical Characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.9.4.1.1 DC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 2.16.2.2, “DC Level Requirement for SerDes Reference Clocks.”

2.9.4.1.2 SGMII Transmit DC Timing Specifications

Table 37 describe the SGMII SerDes transmitter AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs ($SDn\_TX[n]$ and $\overline{SDn\_TX}[n]$) as shown in Figure 24.

Table 37. SGMII DC Transmitter Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	$XV_{DD\_SRDS2\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-}max}/2$	mV	1
Output low voltage	V_{OL}	$XV_{DD\_SRDS2\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-}max}/2$	—	—	mV	1
Output differential voltage[2, 3, 4] ($XV_{DD\text{-}Typ}$ at 1.0V)	$\lvert V_{OD}\rvert$	304	475	689	mV	Equalization setting: 1.0x
		279	436	632		Equalization setting: 1.09x
		254	396	574		Equalization setting: 1.2x
		229	357	518		Equalization setting: 1.33x
		202	316	459		Equalization setting: 1.5x
		178	277	402		Equalization setting: 1.71x
		152	237	344		Equalization setting: 2.0x
Output impedance (single-ended)	R_O	40	50	60	Ω	—

Note:

1. This will not align to DC-coupled SGMII. $XV_{DD\_SRDS2\text{-}Typ}$=1.0V.
2. $\lvert V_{OD}\rvert = \lvert V_{SD2\_TXn} - V_{\overline{SD2\_TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the table assumes the following transmit equalization setting in the XMITEQ**AB** (for SerDes lanes A & B) or XMITEQ**EF** (for SerDes lanes E & E) bit field of P1012's SerDes 2 Control Register:
   - The MSbit (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude - power up default);
   - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$=1.0V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TX[n] and $\overline{SD\_TX}$[n].

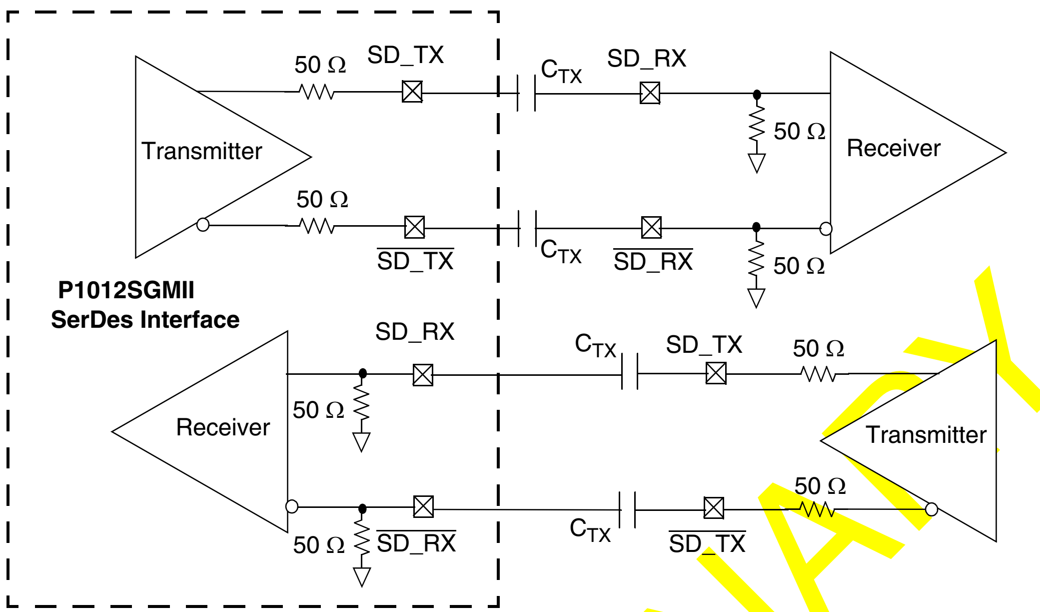


Figure 23. 4-Wire AC-Coupled SGMII Serial Link Connection Example

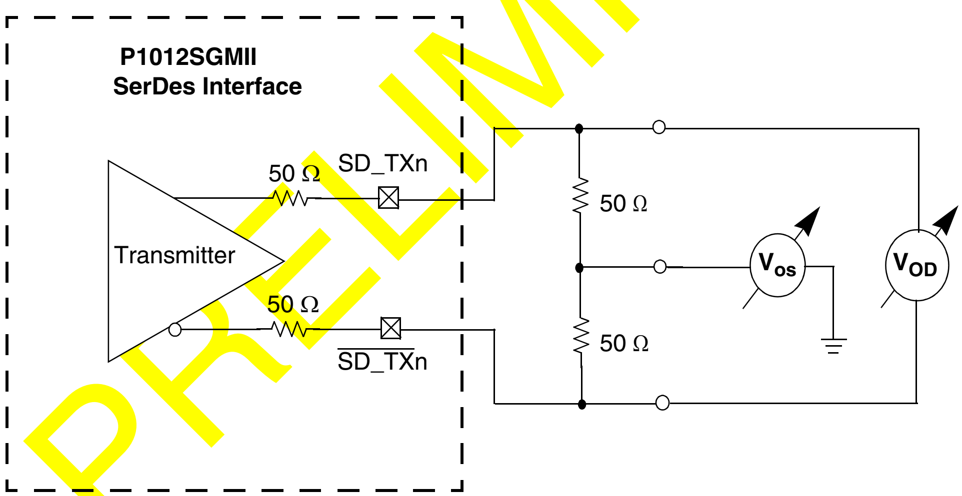


Figure 24. SGMII Transmitter DC Measurement Circuit

2.9.4.1.3 SGMII DC Receiver Timing Specification

Table 38 lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 38. SGMII DC Receiver Electrical Characteristics[5]

For recommended operating conditions, see Table 3

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC Input voltage range		—	N/A			—	1
Input differential voltage	LSTS = 0	$V_{RX\_DIFFp\text{-}p}$	100	—	1200	mV	2, 4
	LSTS = 1		175	—			
Loss of signal threshold	LSTS = 0	VLOS	30	—	100	mV	3, 4
	LSTS = 1		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	Ω	—

Note:

1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in PCI Express. Refer to PCI Express Differential Receiver (RX) Input Specifications section for further explanation.
4. The LSTS shown in the table refers to the LSTS**AB** or LSTS**EF** bit field of P1012's SerDes Control Register.
5.) The supply voltage is 1.0 V.

2.9.4.2 SGMII AC Timing Specifications

This section describes the AC timing specifications for the SGMII interface.

2.9.4.2.1 AC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

Note that the SGMII clock requirements for SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are intended to be used within the clocking guidelines specified by Section 2.16.2.3, "AC Requirements for SerDes Reference Clocks".

2.9.4.2.2 SGMII Transmit AC Timing Specifications

Table 39 provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter

Table 39. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XV_{DD_SRDS} = 1.0V ± 50mV

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	—
Unit Interval	UI	799.92	800	800.08	ps	—

Notes:

1. Each UI is 800 ps ± 100 ppm.
2.)See Figure 26 for single frequency sinusoidal jitter limits

2.9.4.2.3 SGMII AC Measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX[n] and $\overline{\text{SD\_TX}}$[n]) or at the receiver inputs (SD_RX[n] and $\overline{\text{SD\_RX}}$[n]) as depicted in Figure 25, respectively.

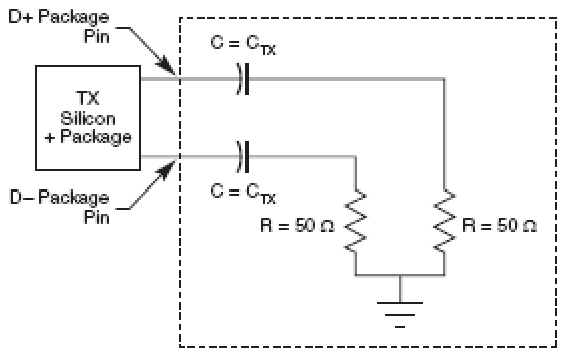


Figure 25. SGMII AC Test/Measurement Load

2.9.4.2.4 SGMII Receiver AC Timing Specifications

Table 40 provides the SGMII receive AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 40. SGMII Receive AC Timing Specifications

At recommended operating conditions with XV_{DD_SRDS2} = 1.0V ± 50mV

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1, 2
Bit Error Ratio	BER	—	—	10^{-12}		—
Unit Interval	UI	799.92	800	800.08	ps	3

Notes:

1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 26.

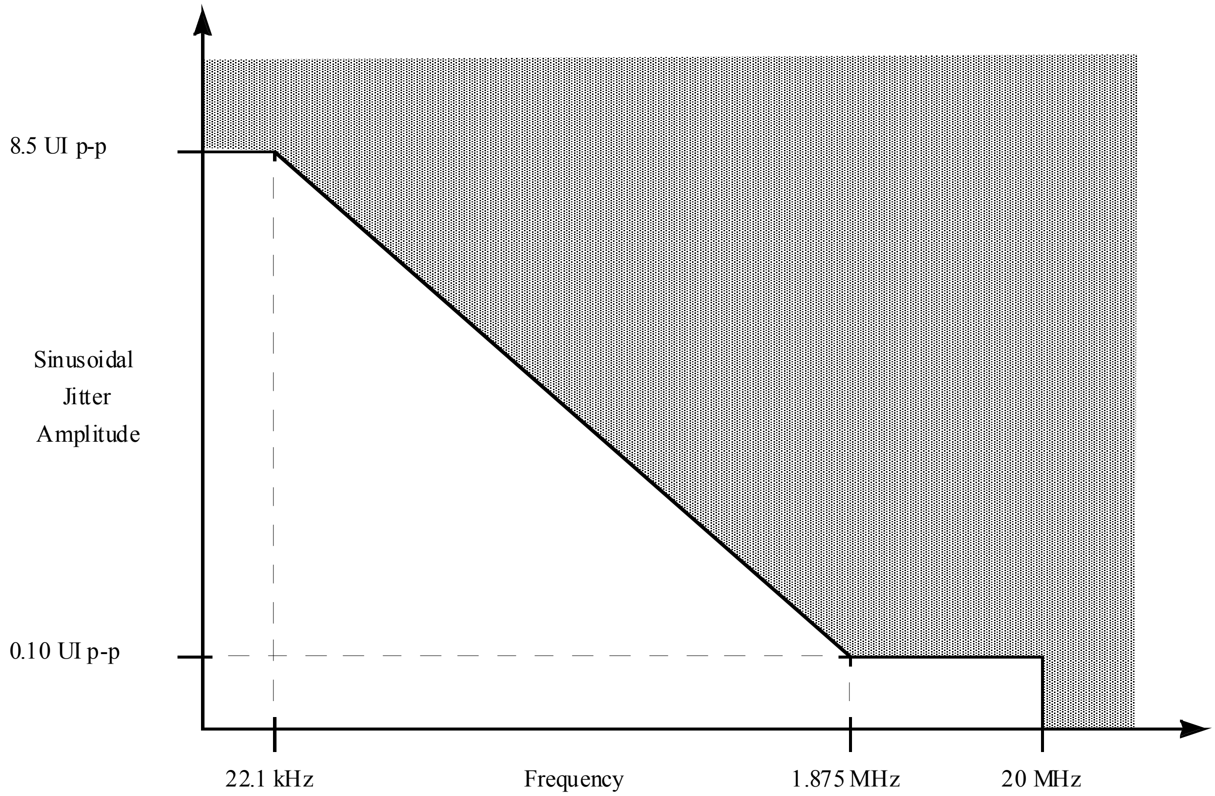


Figure 26. Single Frequency Sinusoidal Jitter Limits

2.9.5 MII Management

2.9.5.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V and 2.5V. The DC electrical characteristics for MDIO and MDC are provided in Table 41 and Table 42.

Table 41. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	LV_{DD} + 0.3	V	—

Table 41. MII Management DC Electrical Characteristics (continued)

At recommended operating conditions with LV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Notes
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.50	V	—

Note:

1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.

Table 42. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage (LV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—
Input high voltage	V_{IH}	1.70	LV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD},)	I_{IH}	—	10	μA	1, 2
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	—

Notes:

1. EC1_MDC and EC1_MDIO operate on LV_{DD}.
2. Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 3.

2.9.5.1.1 MII Management AC Electrical Specifications

Table 43 provides the MII management AC timing specifications.

Table 43. MII Management AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16*t_{plb\_clk}) - 3$	—	$(16*t_{plb\_clk}) + 3$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—

Table 43. MII Management AC Timing Specifications (continued)

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns.
4. t_{plb_clk} is the platform (CCB) clock.

Figure 27 shows the MII management interface timing diagram.

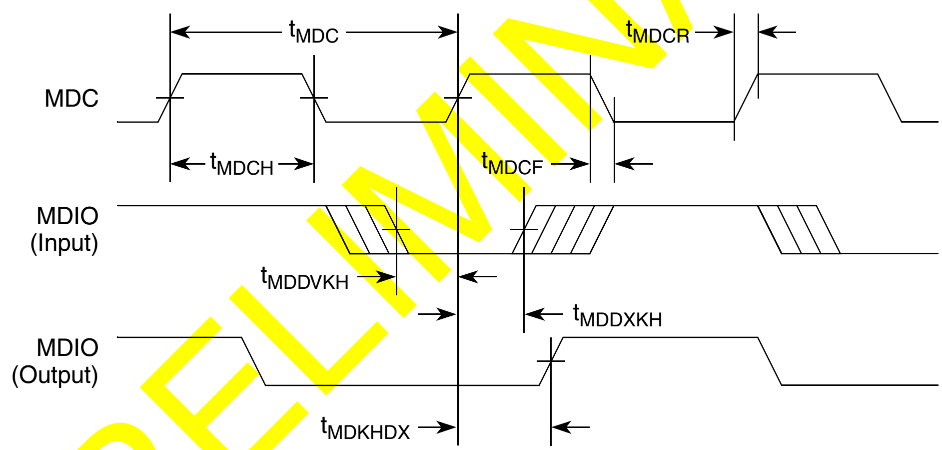


Figure 27. MII Management Interface Timing Diagram

2.9.6 eTSEC IEEE 1588 AC Specifications

Table 44 provides the IEEE 1588 AC timing specifications.

Table 44. eTSEC IEEE 1588 AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.8	—	T_{RX_CLK}*7	ns	1, 3
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$ /$t_{T1588CLK}$	40	50	60	%	—
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—

Table 44. eTSEC IEEE 1588 AC Timing Specifications

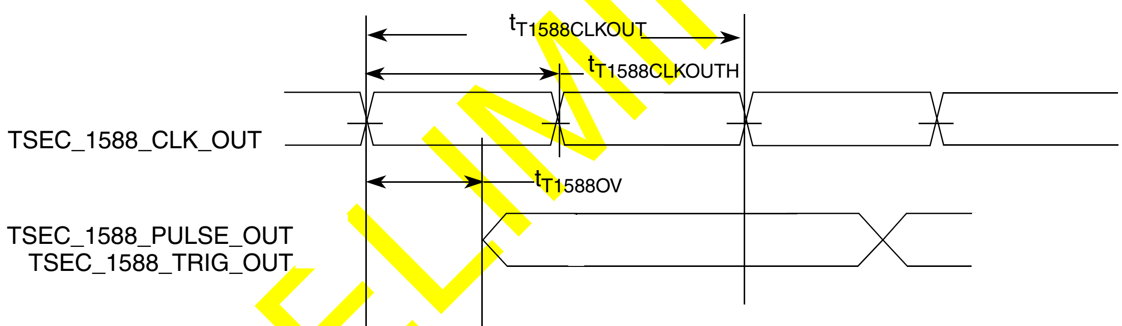
For recommended operating conditions, see Table 3

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2 x $t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	2*$t_{T1588CLK\_MAX}$	—	—	ns	2

Note:

1. T_{RX_CLK} is the max clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *P1012QorIQ Integrated Processor Reference Manual* for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *P1012QorIQ Integrated Processor Reference Manual* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns respectively.

Figure 28 shows the data and command output AC timing diagram.



[1] eTSEC IEEE 1588 Output AC timing: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 28. eTSEC IEEE 1588 Output AC Timing

Figure 29 shows the data and command input AC timing diagram.

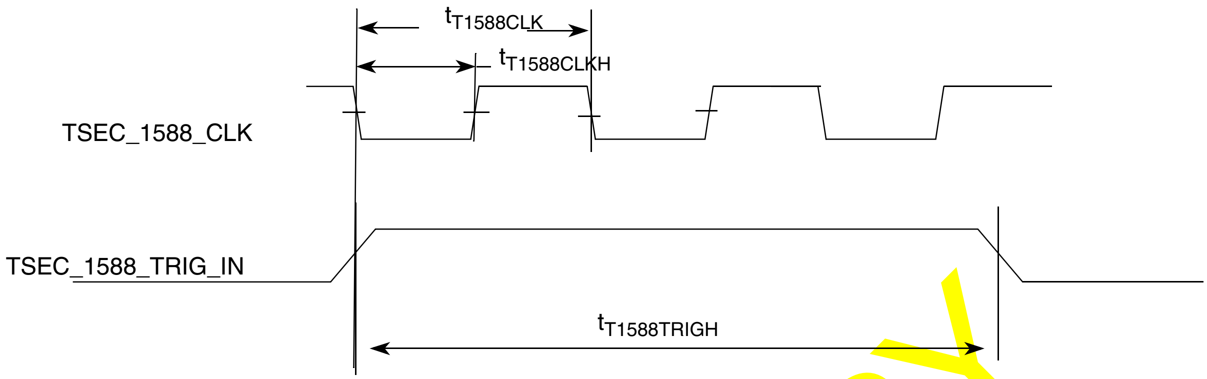


Figure 29. eTSEC IEEE 1588 Input AC Timing

2.10 USB

This section provides the AC and DC electrical specifications for the USB interface of the P1012.

2.10.1 USB DC Electrical Characteristics

Table 47,Table 46and Table 47 provides the DC electrical characteristics for the USB interface.

Table 45. USB DC Electrical Characteristics (CV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (CV_{IN} = 0V or $CV_{IN} = CV_{DD}$)	I_{IN}	—	±40	μA	2
Output High voltage (CV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—
Output Low voltage (CV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. Note that the symbol CV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

Table 46. USB DC Electrical Characteristics (CV_{DD} = 2.5 V)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage[1]	V_{IH}	1.7	—	V	1
Low-level input voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
High-level output voltage (CV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	3
Low-level output voltage (CV_{DD} = min, I_{OL} = 1mA)	V_{OL}	—	0.4	V	—

Notes:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."
3. Not applicable for open drain signals.

Table 47. USB DC Electrical Characteristics (CV_{DD} = 1.8V)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage[1]	V_{IH}	1.25	—	V	1
Low-level input voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
High-level output voltage (CV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	3
Low-level output voltage (CV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."
3. Not applicable for open drain signals.

2.10.2 USB AC Electrical Specifications

Table 48 describes the general timing parameters of the USB interface of the P1012.

Table 48. USB General Timing Parameters

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	15	—	ns	2, 3, 4, 5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2, 3, 4, 5
input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2, 3, 4, 5

Table 48. USB General Timing Parameters (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
USB clock to output valid— all outputs	t_{USKHOV}	—	7	ns	2, 3, 4, 5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2, 3, 4, 5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $CV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times CV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Figure 30 and Figure 31 provide the AC test load and signals for the USB, respectively.

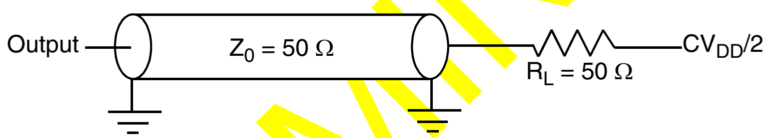


Figure 30. USB AC Test Load

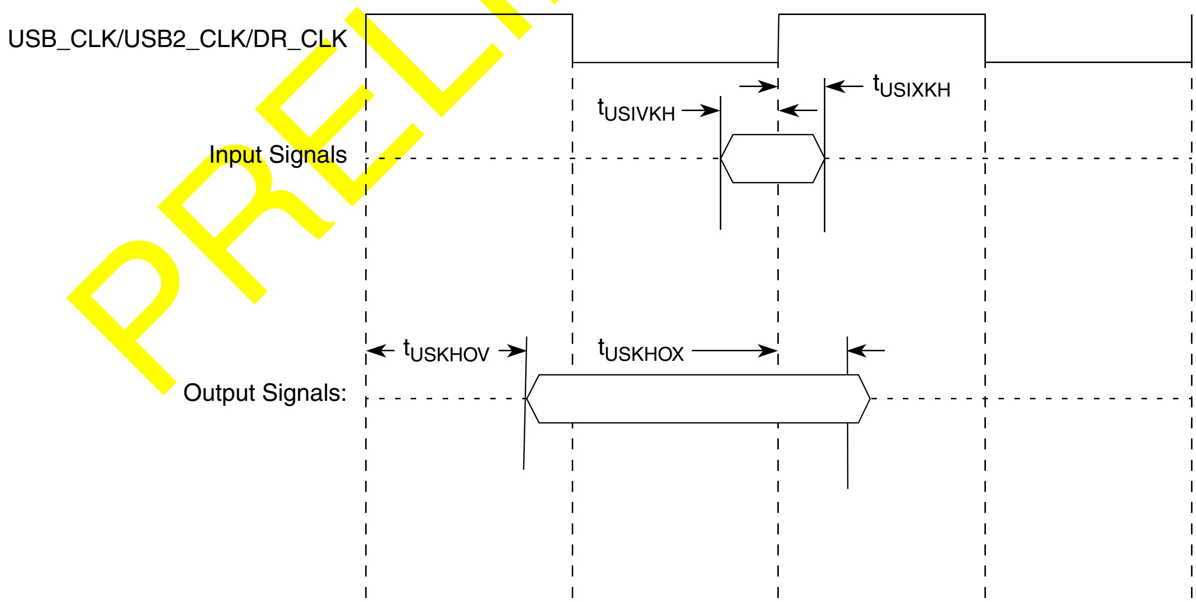


Figure 31. USB Signals

Table 49 provides the USB clock input (USB_CLK_IN) AC timing specifications.

Table 49. USB_CLK_IN AC Timing Specifications

Parameter/Condition	Conditions	Symbol	Min	Typ	Max	Unit
Frequency range	—	$f_{USB\_CLK\_IN}$	54	60	66	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	–0.05	0	0.05	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/time interval error	Peak-to-peak value measured with a second order high-pass filter of 500 kHz bandwidth	t_{CLK_PJ}	—	—	200	ps

2.11 Enhanced Local Bus

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

2.11.1 Enhanced Local Bus DC Electrical Characteristics

Table 50 provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 3.3 V DC.

Table 50. Enhanced Local Bus DC Electrical Characteristics (3.3 V DC)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2	—	V
Input low voltage	V_{IL}	—	0.8	V
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions".

Table 51 provides the DC electrical characteristics for the enhanced local bus interface when operating at BV_{DD} = 2.5 V DC.

Table 51. Enhanced Local Bus DC Electrical Characteristics (2.5 V DC)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	1.7	—	V
Input low voltage	V_{IL}	—	0.7	V

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions".

Table 51. Enhanced Local Bus DC Electrical Characteristics (2.5 V DC) (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit
Input current (V_{IN} = 0 V or V_{IN} =BV_{DD})	I_{IN}	—	±40	μA
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V
Output low voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions".

Table 52 provides the DC electrical characteristics for the enhanced local bus interface when operating at BV_{DD} = 1.8 V DC.

Table 52. Enhanced Local Bus DC Electrical Characteristics (1.8 V DC)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	1.25	—	V
Input low voltage	V_{IL}	—	0.6	V
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA
Output high voltage (BVDD = min, IOH = –0.5 mA)	V_{OH}	1.35	—	V
Output low voltage (BVDD = min, IOL = 0.5 mA)	V_{OL}	—	0.4	V

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol VIN, in this case, represents the BVIN symbol referenced in Section 2.1.2, "Recommended Operating Conditions".

2.11.2 Enhanced Local Bus AC Electrical Specifications

2.11.2.1 Test Condition

Figure 32 provides the AC test load for the enhanced local bus.

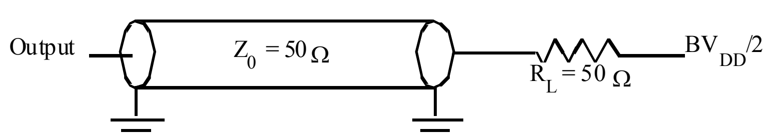


Figure 32. Enhanced Local Bus AC Test Load

2.11.2.2 Local Bus AC Timing Specifications for PLL Bypass Mode

All output signal timings are relative to the falling edge of any LCLKs for PLL bypass mode. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LGTA/LUPWAIT/LFRB are relative to the rising edge of LCLKs. LGTA/LUPWAIT/LFRB are relative to the falling edge of LCLKs.

Table 5 describes the timing specifications of the local bus interface for PLL bypass mode.

Table 53. Enhanced Local Bus Timing Specifications (BV_{DD} = 3.3 V, 2.5 V, and 1.8 V)—PLL Bypass Mode

For recommended operating conditions, see Table ?

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	**12 (Device Specific 2)**	—	ns	—
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	2
Input setup (except LGTA/LUPWAIT/LFRB)	t_{LBIVKH}	6	—	ns	—
Input hold (except LGTA/LUPWAIT/LFRB)	t_{LBIXKH}	1	—	ns	—
Input setup (for LGTA/LUPWAIT/LFRB)	t_{LBIVKL}	6	—	ns	—
Input hold (for LGTA/LUPWAIT/LFRB)	t_{LBIXKL}	1	—	ns	—
Output delay (Except LALE)	t_{LBKLOV}	—	1.5	ns	—
Output hold (Except LALE)	t_{LBKLOX}	-3.5	—	ns	5
Local bus clock to output high impedance for LAD/LDP	t_{LBKLOZ}	—	2	ns	3
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	**1/2 (LBCR[AHD]=1) (Device Specific 3) 1 (LBCR[AHD]=0) (Device Specific 5)**	—	eLBC controller clock cycle **(=n platform clock cycles) (Device Specific 4)**	4

Note:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of LCLK to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different LCLK signals at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle, which is the internal clock that runs the local bus controller, not the external LCLK. LCLK cycle = eLBC controller clock cycle × LCRR[CLKDIV]. After power on reset, LBCR[AHD] defaults to 0 and eLBC runs at maximum hold time.
5. Output hold is negative. This means that output transition happens earlier than the falling edge of LCLK.

Figure 33 shows the AC timing diagram for PLL bypass mode.

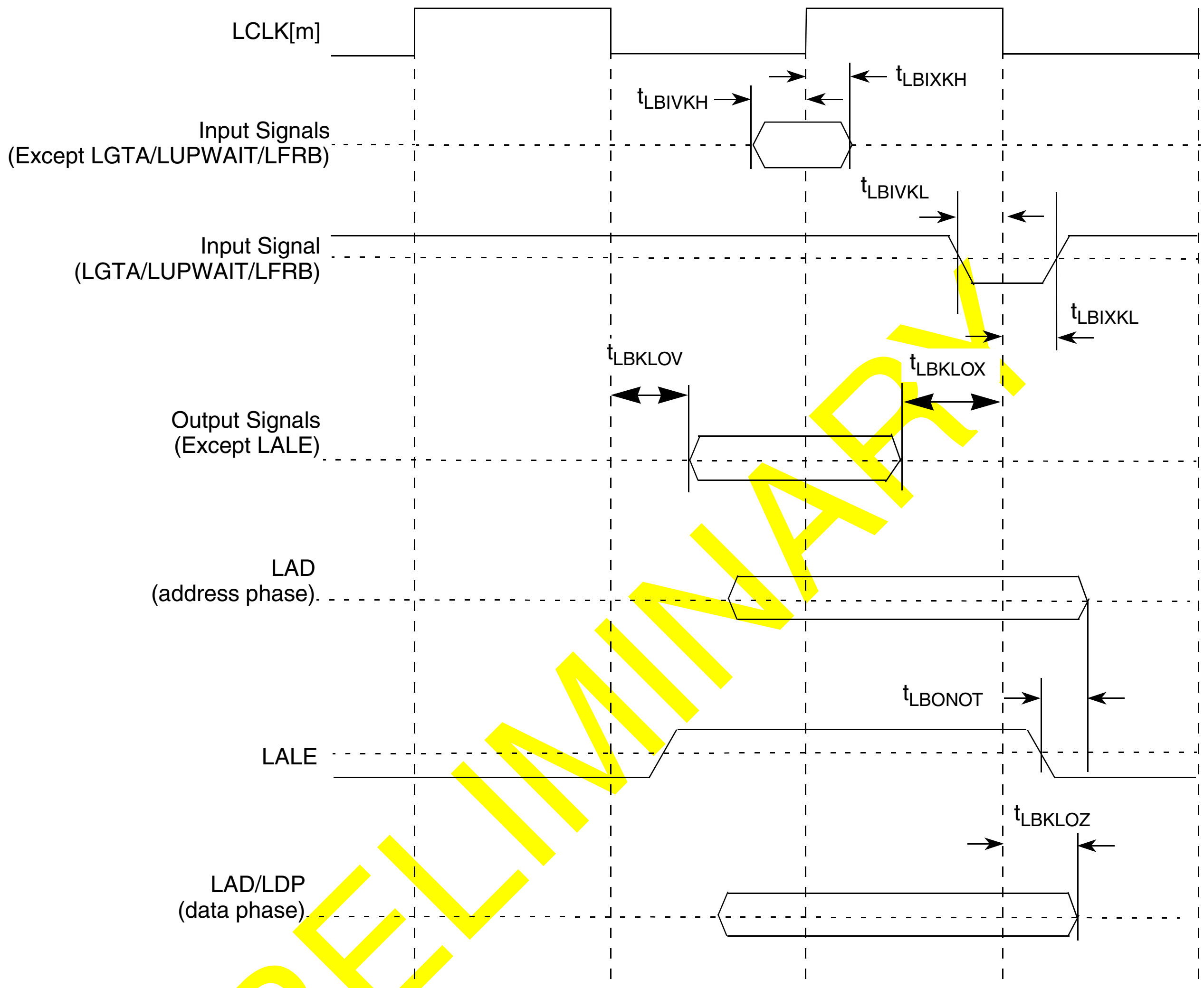


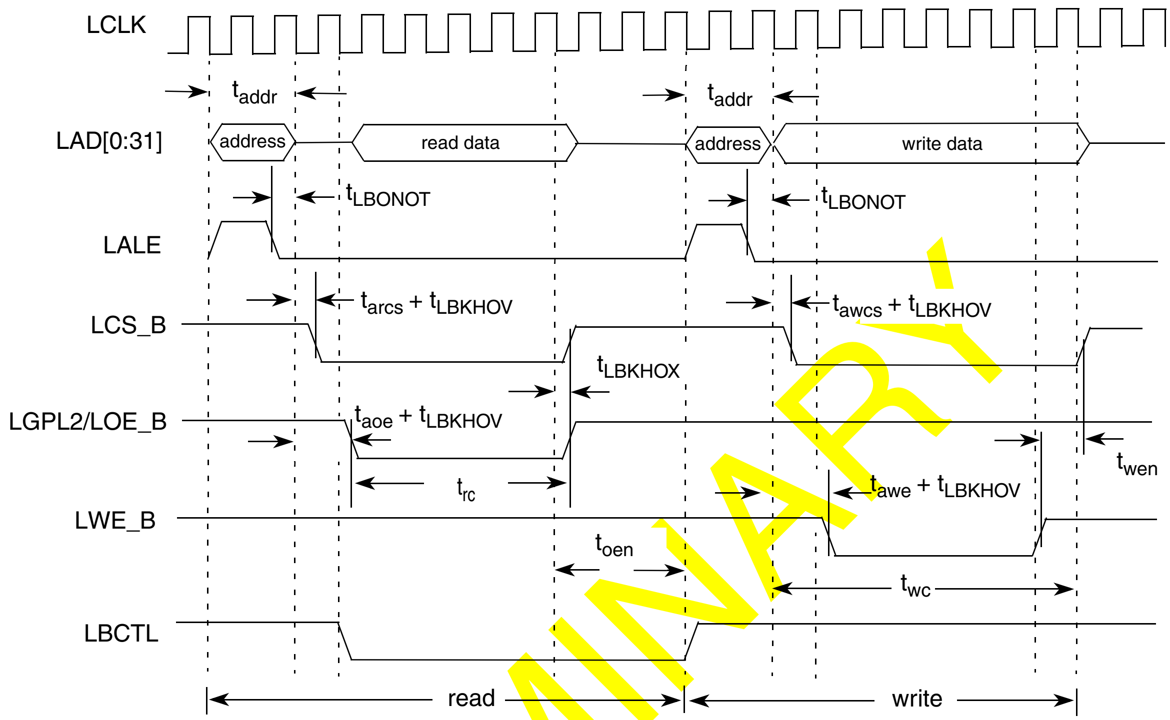
Figure 33. Enhanced Local Bus Signals (PLL Bypass Mode)

Figure 33 applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKHOV}$.

Figure 5 shows how the AC timing diagram applies to GPCM in PLL bypass mode. The same principle applies to UPM and FCM.



1 t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].
2 t_{arcs}, t_{awcs}, t_{aoe}, t_{rc}, t_{oen}, t_{awe}, t_{wc}, t_{wen} are determined by ORx. See the <Device name> reference manual.

Figure 34. GPCM Output Timing Diagram (PLL Bypass Mode)

2.12 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface of the P1012.

2.12.1 eSDHC DC Electrical Characteristics

Table 54 provides the DC electrical characteristics for the eSDHC interface of the P1012.

Table 54. eSDHC Interface DC Electrical Characteristics

At recommended operating conditions with CV_{DD} = 3.3 V

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	—	0.625 × CV_{DD}	—	V	1
Input low voltage	V_{IL}	—	—	0.25 × CV_{DD}	V	1
Output high voltage	V_{OH}	I_{OH} = –100 uA at CV_{DD}min	0.75 × CVDD	—	V	—
Output low voltage	V_{OL}	I_{OL} = 100uA at CV_{DD}min	—	0.125 × CVDD	V	—
Output high voltage	V_{OH}	I_{OH} = –100 uA	CV_{DD} - 2	—	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	V	2

Table 54. eSDHC Interface DC Electrical Characteristics (continued)

At recommended operating conditions with CV_{DD} = 3.3 V

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input/output leakage current	I_{IN}/I_{OZ}	—	–10	10	uA	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Figure 3.
2. Open drain mode for MMC cards only.

2.12.2 eSDHC AC Timing Specifications

Table 55 provides the eSDHC AC timing specifications as defined in Figure 36.

Table 55. eSDHC AC Timing Specifications

At recommended operating conditions with CV_{DD} = 3.3V

Parameter	Symbol	Min	Max	Unit	Notes
SD_CLK clock frequency: SD/SDIO Full-speed/High-speed mode MMC Full-speed/High-speed mode	f_{SFSCK}	0	25/50 20/52	MHz	2, 4
SD_CLK clock low time—Full-speed/High-speed mode	t_{SFSCKL}	10/7	—	ns	4
SD_CLK clock high time—Full-speed/High-speed mode	t_{SFSCKH}	10/7	—	ns	4
SD_CLK clock rise and fall times	$t_{SFSCKR}/$ t_{SFSCKF}	—	3	ns	4
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SFSIVKH}$	5.0	—	ns	4
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SFSIXKH}$	2.5	—	ns	3,4
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	-3	3	ns	4

Note:
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full speed mode, clock frequency value can be 0–25 MHz for a SD/SDIO card and 0–20 MHz for a MMC card. In high speed mode, clock frequency value can be 0–50 MHz for a SD/SDIO card and 0–52 MHz for a MMC card.
3. To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2ns.
4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF

Figure 35 provides the eSDHC clock input timing diagram.

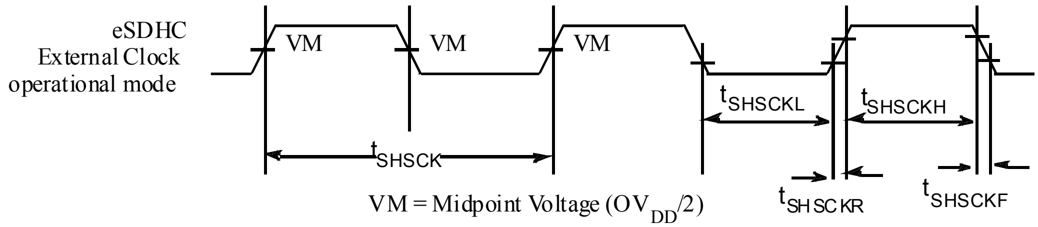


Figure 35. eSDHC Clock Input Timing Diagram

Figure 36provides the data and command input/output timing diagram.

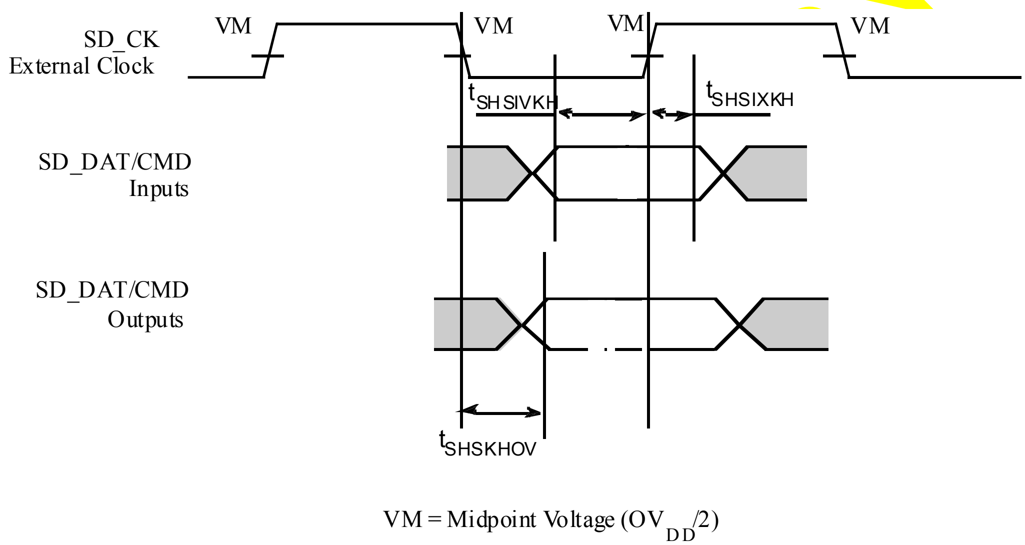


Figure 36. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.13 Programmable Interrupt Controller (PIC) Sepcifications

This section describes the DC and AC electrical specifications for PIC on the P1012.

2.13.1 PIC DC Electrical Characteristics

Table 56 provides the DC electrical characteristics for the PIC interface.

Table 56. PIC DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—

Table 56. PIC DC Electrical Characteristics (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Note that the symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.13.2 PIC AC Timing Specifications

Table 57 provides the PIC input and output AC timing specifications.

Table 57. PIC Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
PIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLK	1

Note:

1. PIC inputs and outputs are asynchronous to any visible clock. PIC outputs should be synchronized before use by any external synchronous logic. PIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge-triggered mode.

2.14 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the P1012.

2.14.1 JTAG DC Electrical Characteristics

Table 58 provides the JTAG DC electrical characteristics.

Table 58. JTAG DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3
2. Note that the symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.14.2 JTAG AC Timing Specifications

Table 59 provides the JTAG AC timing specifications as defined in Figure 37 through Figure 40.

Table 59. JTAG AC Timing Specifications

For recommended operating conditions see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—

Table 59. JTAG AC Timing Specifications (continued)

For recommended operating conditions see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	2
Input setup times	t_{JTDVKH}	4	—	ns	—
Input hold times	t_{JTDXKH}	10	—	ns	—
Output valid times	t_{JTKLDV}	4	10	ns	3
Output hold times	t_{JTKLDX}	30	—	ns	3
JTAG external clock to output high impedance	t_{JTKLDZ}	4	10	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

Figure 37 provides the AC test load for TDO and the boundary-scan outputs.

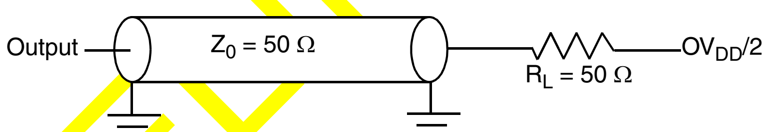
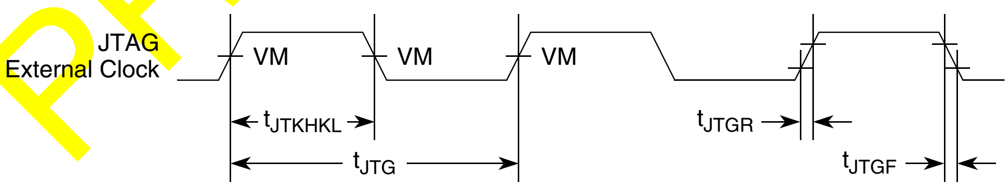


Figure 37. AC Test Load for the JTAG Interface

Figure 38 provides the JTAG clock input timing diagram.



VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 38. JTAG Clock Input Timing Diagram

Figure 39 provides the $\overline{\text{TRST}}$ timing diagram.

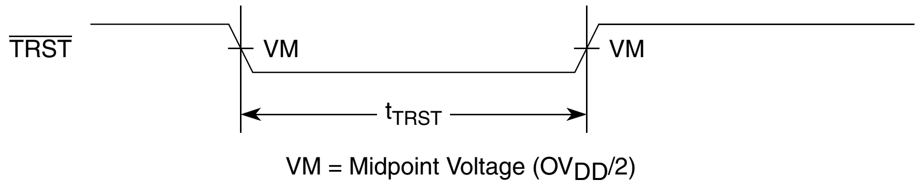


Figure 39. $\overline{\text{TRST}}$ Timing Diagram

Figure 40 provides the boundary-scan timing diagram.

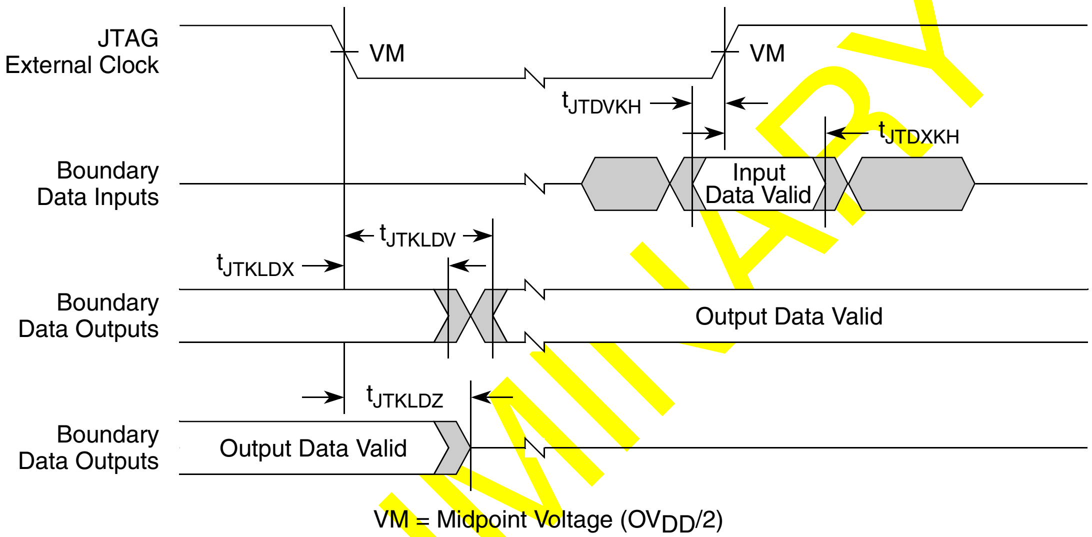


Figure 40. Boundary-Scan Timing Diagram

2.15 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the P1012.

2.15.1 I²C DC Electrical Characteristics

Table 60 provides the DC electrical characteristics for the I²C interfaces.

Table 60. I²C DC Electrical Characteristics

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output low voltage	V_{OL}	0	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	μA	4

Table 60. I²C DC Electrical Characteristics (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Notes
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. Refer to the *12QorIQ Integrated Communications Host Processor Reference Manual* for information on the digital filter used.
4. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.15.2 I²C AC Electrical Specifications

Table 61 provides the AC timing parameters for the I²C interfaces.

Table 61. I²C AC Electrical Specifications

For recommended operariong conditions see Table 3. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 60)

Parameter	Symbol	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—

Table 61. I²C AC Electrical Specifications (continued)

For recommended operariong conditions see Table 3. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 60)

Parameter	Symbol	Min	Max	Unit	Notes
Capacitive load for each bus line	Cb	—	400	pF	

Note:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. Refer to Freescale application note AN2919, "Determining the I2C Frequency Divider Ratio for SCL."
3. As a transmitter, the 12 provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the 12 acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the 12 does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the 12 as transmitter, application note AN2919 referred to in note 4 below is recommended.
4. The maximum t_{I2OVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

Figure 41 provides the AC test load for the I²C.

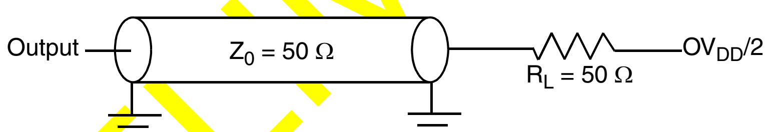


Figure 41. I²C AC Test Load

Figure 42 shows the AC timing diagram for the I²C bus.

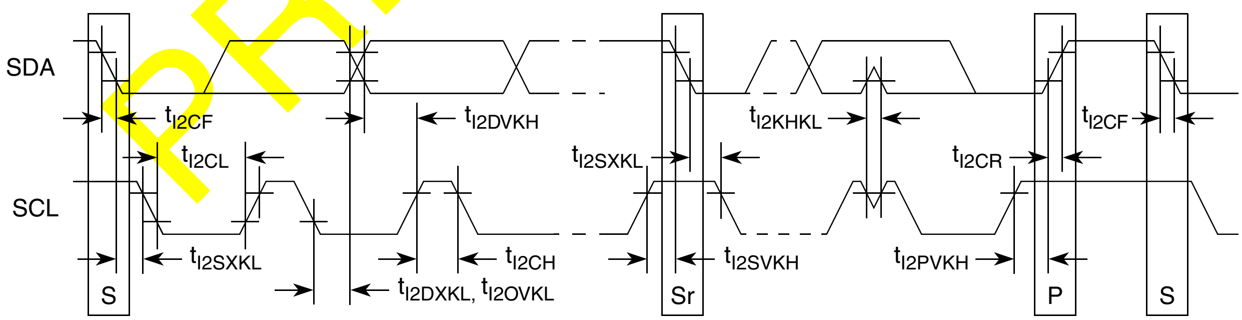


Figure 42. I²C Bus AC Timing Diagram

Figure 43.

2.16 High-Speed Serial Interfaces (HSSI)

The P1012 features one Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express data transfers and for SGMII application.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

2.16.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 44 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\mathrm{SD}n\_\mathrm{TX}}$) or a receiver input (SD*n*_RX and $\overline{\mathrm{SD}n\_\mathrm{RX}}$). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals SD*n*_TX, $\overline{\mathrm{SD}n\_\mathrm{TX}}$, SD*n*_RX and $\overline{\mathrm{SD}n\_\mathrm{RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's Single-Ended Swing.

2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

   The Differential Output Voltage (or Swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{\mathrm{SD}n\_\mathrm{TX}} - V_{\overline{\mathrm{SD}n\_\mathrm{TX}}}$. The V_{OD} value can be either positive or negative.

3. **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

   The Differential Input Voltage (or Swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{\mathrm{SD}n\_\mathrm{RX}} - V_{\overline{\mathrm{SD}n\_\mathrm{RX}}}$. The V_{ID} value can be either positive or negative.

4. **Differential Peak Voltage, V_{DIFFp}**

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp\text{-}p}$**

   Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp\text{-}p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{OD}|$.

6. **Differential Waveform**

   The differential waveform is constructed by subtracting the inverting signal (SDn_TX, for example) from the non-inverting signal (SDn_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 44 as an example for differential waveform.

7. **Common Mode Voltage, V_{cm}**

   The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, V_{cm_out} = (VSD*n*_TX + VSD*n*_TX)/2 = (A + B) / 2, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may even be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset occasionally.

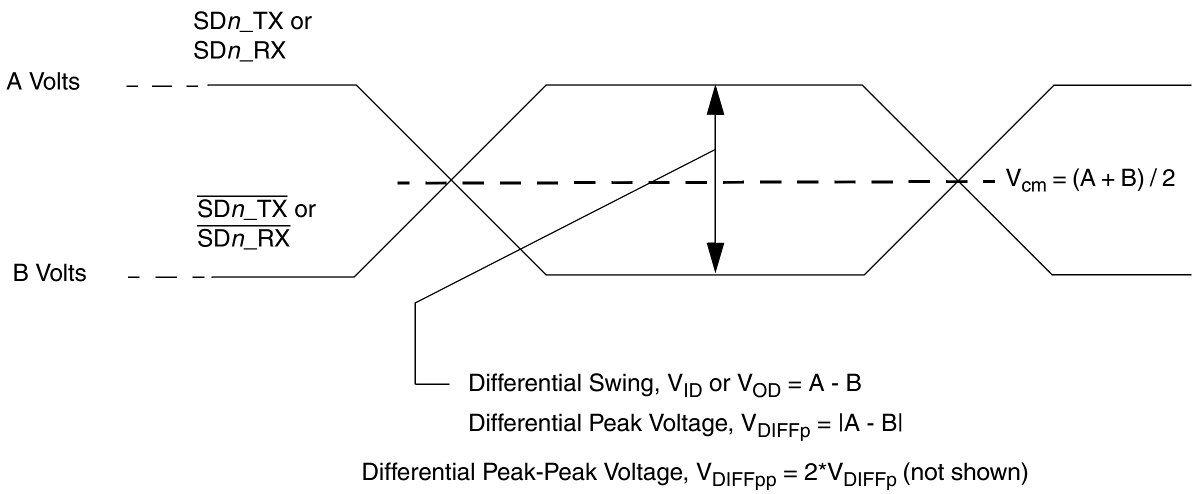


Figure 44. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock inputs are SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ for PCI Express and SGMII interface.

The following sections describe the SerDes reference clock requirements and some application information.

2.16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 45 shows a receiver reference diagram of the SerDes reference clocks.

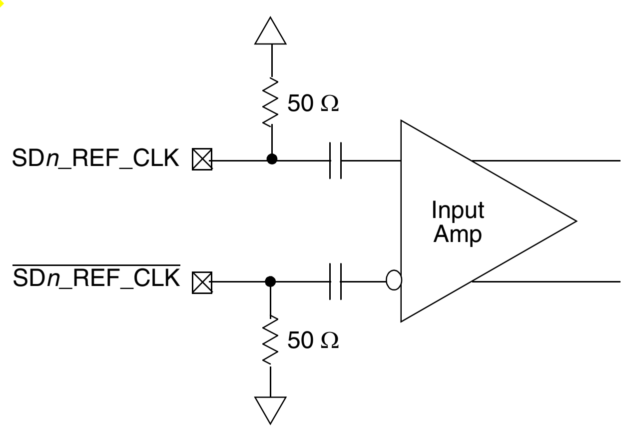


Figure 45. Receiver of SerDes Reference Clocks

The characteristics of the clock signals are as follows:

- The supply voltage requirements for XV_{DD_SRDS2} are specified in Table 2 and Table 3.
- SerDes reference clock receiver reference circuit structure
  - — The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 45. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to SGND_SRDS followed by on-chip AC-coupling.
  - — The external reference clock driver must be able to drive this termination.
  - — The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  - — This current limitation sets the maximum common mode input voltage to be less than 0.4V (0.4V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS . For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0V to 800mV with the common mode voltage at 400 mV.
  - — If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDS DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

2.16.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the P1012 P1012 SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - — The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - — For **external DC-coupled** connection, as described in Section 2.16.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 46 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - — For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDS. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDS). Figure 47 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

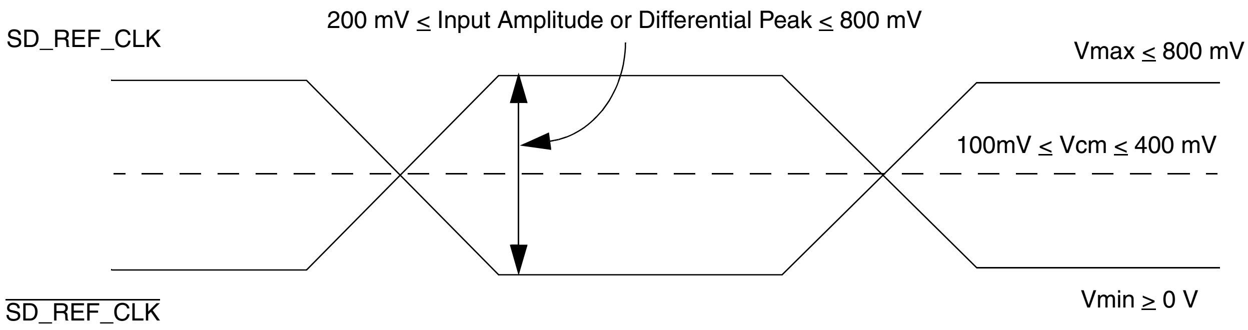


Figure 46. Differential Reference Clock Input DC Requirements (External DC-Coupled)

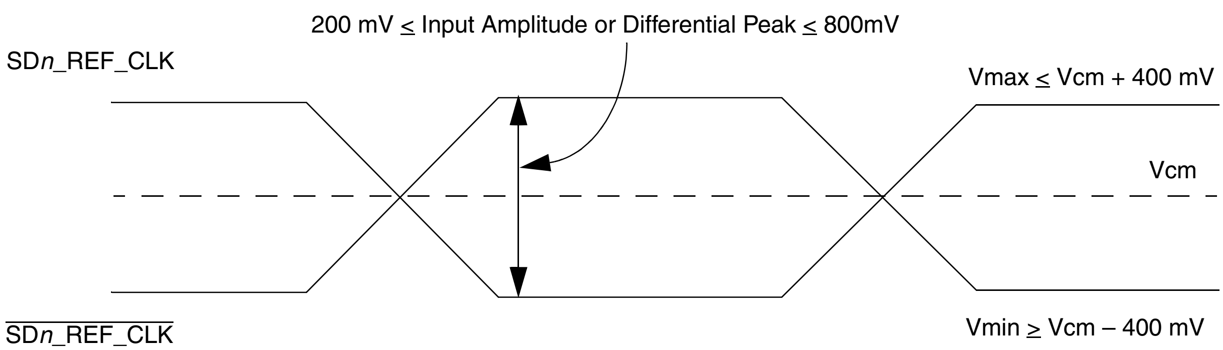


Figure 47. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- **Single-ended Mode**
  - The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  - The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 48 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

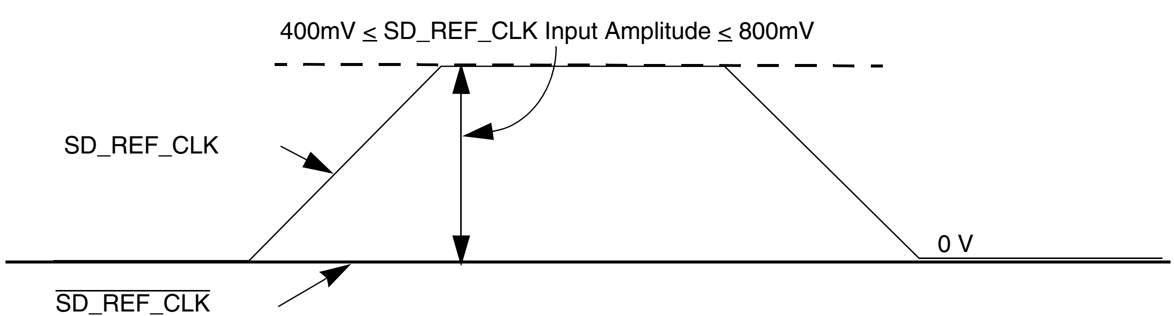


Figure 48. Single-Ended Reference Clock Input DC Requirements

2.16.2.3 AC Requirements for SerDes Reference Clocks

Table 1 lists AC requirements for the PCI Express and SGMII SerDes reference clocks to be guaranteed by the customer's application design.

Table 62. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ Input Clock Requirements

Parameter	Symbol	Min	Typical	Max	Unit	Notes
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	-350	—	+350	ppm	—
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle (Measured at 1.6V)	t_{CLK_DUTY}	40	50	60	%	—
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-peak Jitter @ 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter @ 10^{-6} BER (Peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3

Notes:
1. Only 100/125 have been tested, other in between values will not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus $\overline{\text{SDn\_REF\_CLK}}$).The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing.

2.16.2.4 SerDes Transmitter and Receiver Reference Circuits

Figure 49 shows the reference circuits for SerDes data lane's transmitter and receiver.

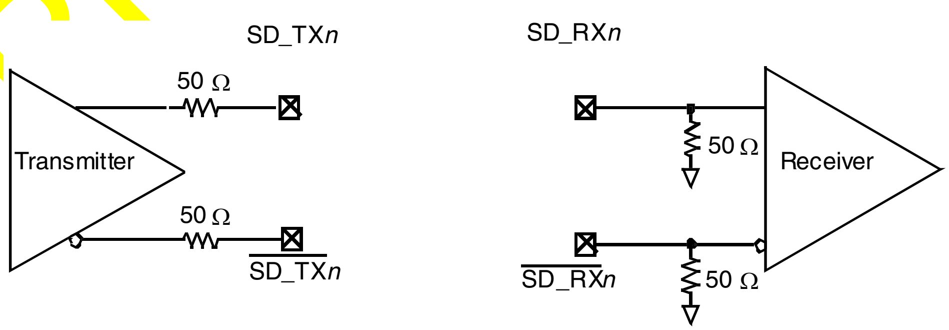


Figure 49. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO or SGMII) in this document based on the application usage:

- Section 2.9.4, "SGMII Interface Electrical Characteristics"
- Section 2.17, "PCI Express"

Note that external AC Coupling capacitor is required for the above three serial transmission protocols per the protocol's standard requirements.

2.17 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the P1012.

2.17.1 PCI Express DC Requirements for PCI Express SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

For more information, see Section 2.16.2.2, "DC Level Requirement for SerDes Reference Clocks."

2.17.2 PCI Express DC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.17.2.1 PCI Express DC Physical Layer Transmitter Specifications

This section discusses PCI Express DC physical layer transmitter specifications for 2.5 Gb/s.

Table 63 defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 63. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output DC Specifications

Symbol	Parameter	Min	Typical	Max	Units	Comments
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak-to-Peak Output Voltage	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2*\|V_{TX\text{-}D+} - V_{TX\text{-}D-}\|$ See Note 1.
$V_{TX\text{-}DE\text{-}RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 1.
$Z_{TX\text{-}DIFF\text{-}DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
$Z_{TX\text{-}DC}$	Transmitter DC Impedance	40	50	60	Ω	Required TX D+ as well as D- DC Impedance during all states

Note:
1. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 50 and measured over any 250 consecutive TX UIs.

2.17.2.2 PCI Express DC Physical Layer Receiver Specifications

This section discusses PCI Express DC physical layer receiverspecifications for 2.5 Gb/s.

Table 63 defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 64. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications

Symbol	Parameter	Min	Typical	Max	Units	Comments
$V_{RX\text{-}DIFFp\text{-}p}$	Differential Input Peak-to-Peak Voltage	175	—	1200	mV	$V_{RX\text{-}DIFFp\text{-}p} = 2*\lvert V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}\rvert$ See Note 1.
$Z_{RX\text{-}DIFF\text{-}DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 2
$Z_{RX\text{-}DC}$	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	Powered Down DC Input Impedance	50 k	—	—	Ω	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 3.
$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	Electrical Idle Detect Threshold	65	—	175	mV	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2*\lvert V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}\rvert$ Measured at the package pins of the Receiver

Notes:
1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 50 should be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
2. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
3. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

2.17.3 PCI Express AC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.17.3.1 PCI Express AC Physical Layer Transmitter Specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5Gb/s.

Table 65 defines the PCI Express (2.5Gb/s) AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 65. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output AC Specifications

Symbol	Parameter	Min	Typical	Max	Units	Comments
UI	Unit Interval	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$T_{TX\text{-}EYE}$	Minimum TX Eye Width	0.70	—	—	UI	The maximum Transmitter jitter can be derived as $T_{TX\text{-}MAX\text{-}JITTER} = 1 - T_{TX\text{-}EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
C_{TX}	AC Coupling Capacitor	75	—	200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 50 and measured over any 250 consecutive TX UIs.
3. A $T_{TX\text{-}EYE} = 0.70$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX\text{-}JITTER\text{-}MAX} = 0.30$ UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. P1012SerDes transmitter does not have CTX built-in. An external AC Coupling capacitor is required.

2.17.3.2 PCI Express AC Physical Layer Receiver Specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 Gb/s.

Table 66 defines the AC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 66. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input AC Specifications

Symbol	Parameter	Min	Typical	Max	Units	Comments
UI	Unit Interval	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$T_{RX\text{-}EYE}$	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX\text{-}MAX\text{-}JITTER}$ = 1 - $T_{RX\text{-}EYE}$= 0.6 UI. See Notes 2 and 3.
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 50 should be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX\text{-}EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.17.3.3 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 50.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

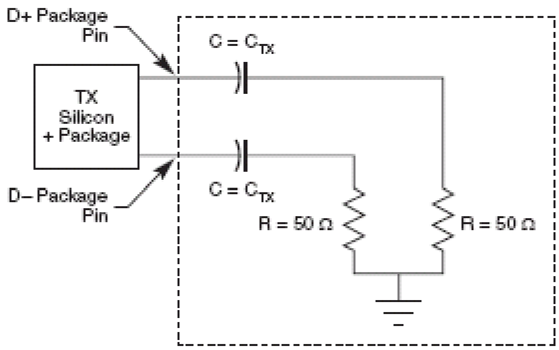


Figure 50. Compliance Test/Measurement Load

3 QUICC Engine Specifications

3.1 Ethernet Interface

This section provides the AC and DC electrical characteristics for the Ethernet interfaces inside the QUICC Engine.

3.1.1 MII and RMII DC Electrical Characteristics

Table 67 shows the MII and RMII DC electrical characteristics

Table 67. MII, and RMII DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.9	V	—
Input high current (V_{IN} = BV_{DD})	I_{IH}	—	40	μA	2
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	2
Output high voltage (BV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.1	BV_{DD} + 0.3	V	—
Output low voltage (BV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	—

Note:
1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3

3.1.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

Table 68 provides the MII transmit AC timing specifications.

Table 68. MII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	399.96	400	400.04	ns
TX_CLK clock period 100 Mbps	t_{MTX}	39.996	40	40.004	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	0	—	25	ns
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns

Figure 51 shows the MII transmit AC timing diagram.

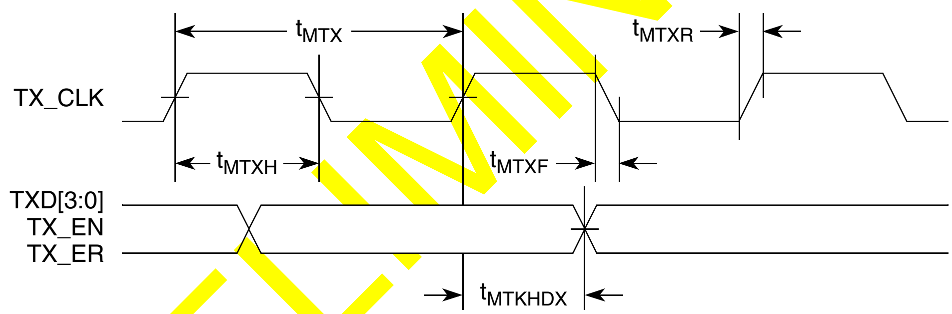


Figure 51. MII Transmit AC Timing Diagram

Table 69 provides the MII receive AC timing specifications.

Table 69. MII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	399.96	400	400.04	ns
RX_CLK clock period 100 Mbps	t_{MRX}	39.996	40	40.004	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns

Figure 52 shows the MII receive AC timing diagram.

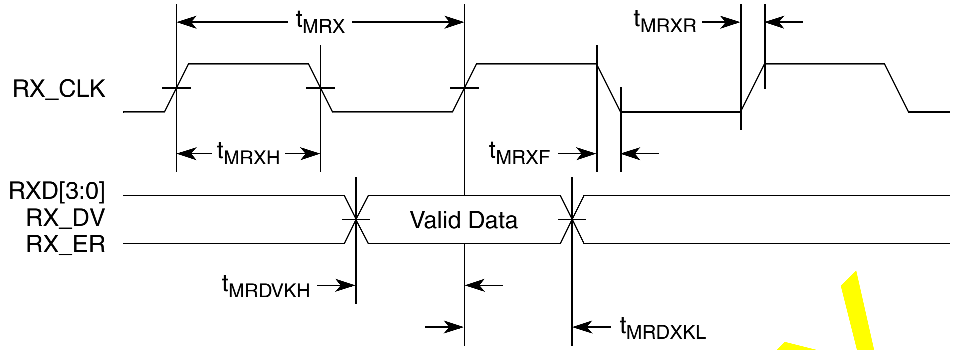


Figure 52. MII Receive AC Timing Diagram

Figure 53 provides the MII AC test load.

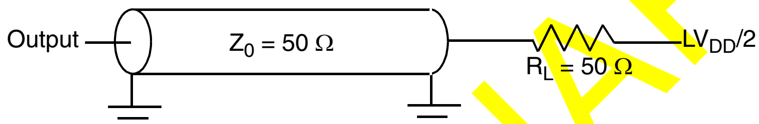


Figure 53. MII AC Test Load

3.1.3 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

The RMII transmit AC timing specifications are in Table 70.

Table 70. RMII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter/Condition	Symbol	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMT}	—	20.0	—	ns
REF_CLK duty cycle	t_{RMTH}	35	—	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	5.0	ns
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	5.0	ns
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Figure 54 shows the RMII transmit AC timing diagram.

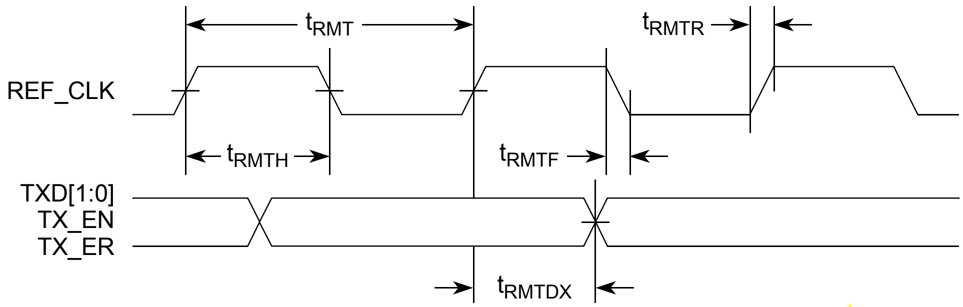


Figure 54. RMII Transmit AC Timing Diagram

Table 71 provides the MII receive AC timing specifications.

Table 71. RMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter/Condition	Symbol	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMR}	—	20.0	—	ns
REF_CLK duty cycle	t_{RMRH}	35	—	65	%
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	5.0	ns
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	—	5.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	$t_{RMRKHDX}$	2.0	—	—	ns

Figure 55 shows the RMII receive AC timing diagram.

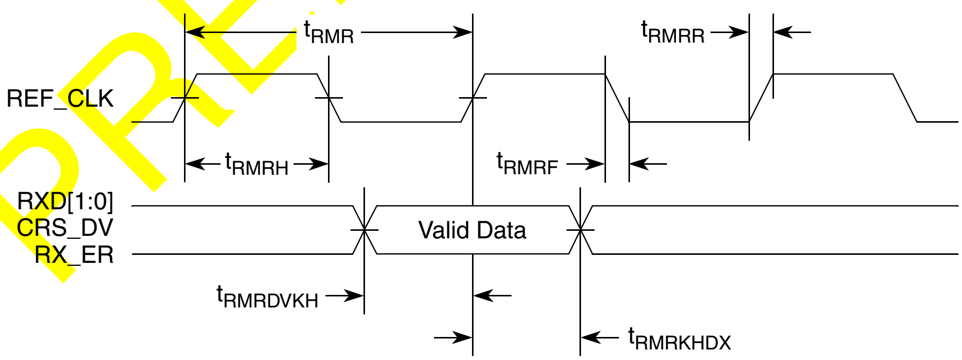


Figure 55. RMII Receive AC Timing Diagram

Figure 56 provides the AC test load.

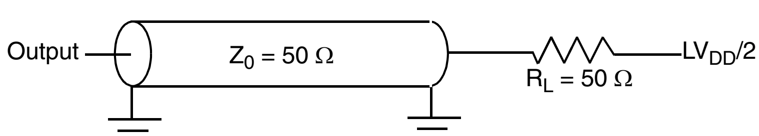


Figure 56. AC Test Load

3.2 HDLC, BISYNC, Transparent, and Synchronous UART Interfaces

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent and synchronous UART of the P101221.

3.2.1 HDLC, BISYNC, Transparent and Synchronous UART DC Electrical Characteristics

Table 72 provides the DC electrical characteristics for the P101221 HDLC, BISYNC, Transparent and Synchronous UART protocols.

Table 72. HDLC, BiSync, Transparent and Synchronous UART DC Electrical Characteristics

For recommended operating conditions, see Table 3

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (BV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

3.2.2 HDLC, BISYNC, Transparent and Synchronous UART AC Timing Specifications

Table 73 provides the input and output AC timing specifications for HDLC, BiSync, and Transparent and Synchronous UART protocols.

Table 73. HDLC, BiSync, Transparent AC Timing Specifications

For recommended operating conditions, see Table 3

Characteristic	Symbol [1]	Min	Max	Unit	Notes
Outputs—Internal clock delay	t_{HIKHOV}	0	5.5	ns	2
Outputs—External clock delay	t_{HEKHOV}	1	8	ns	2
Outputs—Internal clock High Impedance	t_{HIKHOX}	0	5.5	ns	2
Outputs—External clock High Impedance	t_{HEKHOX}	1	8	ns	2
Inputs—Internal clock input setup time	t_{HIIVKH}	6	—	ns	—
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns	—
Inputs—Internal clock input Hold time	t_{HIIXKH}	0	—	ns	—

Table 73. HDLC, BiSync, Transparent AC Timing Specifications (continued)

For recommended operating conditions, see Table 3

Characteristic	Symbol [1]	Min	Max	Unit	Notes
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Table 74 provides the input and output AC timing specifications for the synchronous UART protocols.

Table 74. Synchronous UART AC Timing Specifications

For recommended operating conditions, see Table 3

Characteristic	Symbol [1]	Min	Max	Unit	Notes
Outputs—Internal clock delay	t_{HIKHOV}	0	11	ns	2
Outputs—External clock delay	t_{HEKHOV}	1	14	ns	2
Outputs—Internal clock High Impedance	t_{HIKHOX}	0	11	ns	2
Outputs—External clock High Impedance	t_{HEKHOX}	1	14	ns	2
Inputs—Internal clock input setup time	t_{HIIVKH}	10	—	ns	—
Inputs—External clock input setup time	t_{HEIVKH}	8	—	ns	—
Inputs—Internal clock input Hold time	t_{HIIXKH}	0	—	ns	—
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns	—

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 57 provides the AC test load.

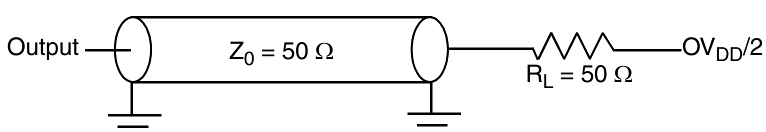


Figure 57. AC Test Load

Figure 58 and Figure 59 represent the AC timing from Table 73 and Table . Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. Figure 58 shows the timing with external clock.

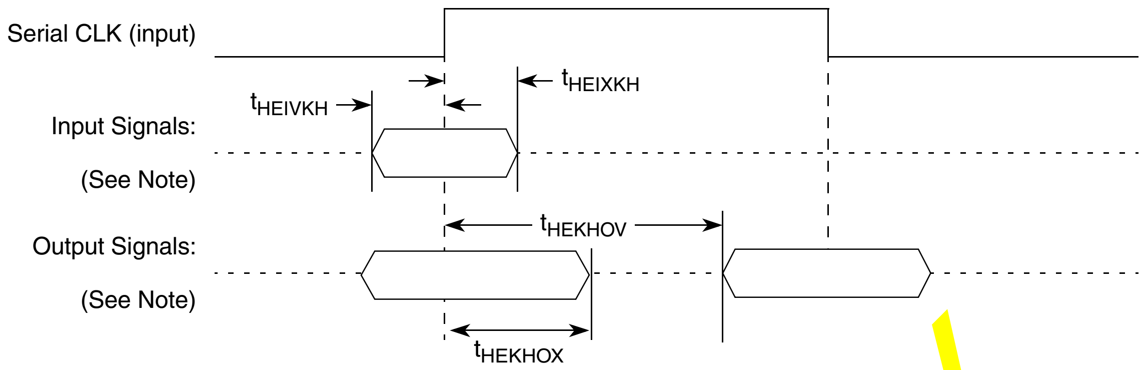


Figure 58. AC Timing (External Clock) Diagram

Figure 59 shows the timing with internal clock.

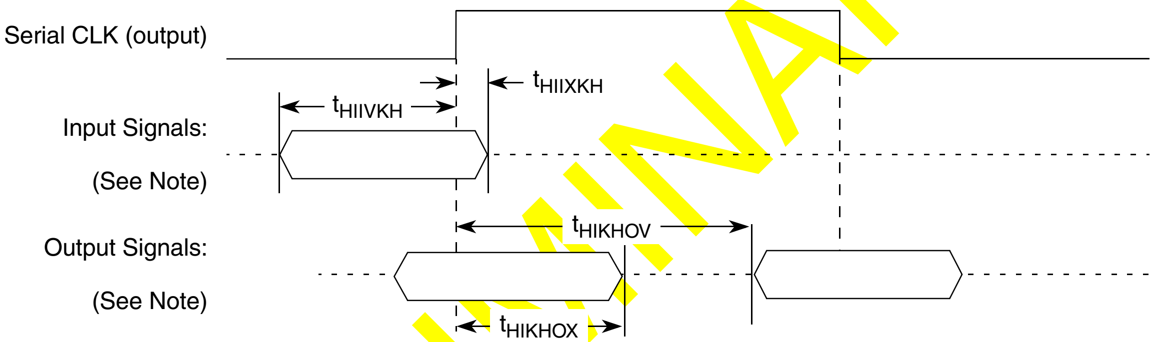


Figure 59. AC Timing (Internal Clock) Diagram

3.3 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the P1012/21.

3.3.1 TDM/SI DC Electrical Characteristics

Table 75 provides the DC electrical characteristics for the P1012/21 TDM/SI.

Table 75. TDM/SI DC Electrical Characteristics

For recommended operating conditions, see Table 3

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—

Table 75. TDM/SI DC Electrical Characteristics (continued)

For recommended operating conditions, see Table 3

Characteristic	Symbol	Min	Max	Unit	Notes
Output low voltage (BV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

3.3.2 TDM/SI AC Timing Specifications

Table 76 provides the TDM/SI input and output AC timing specifications.

Table 76. TDM/SI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	11	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 60 provides the AC test load for the TDM/SI.

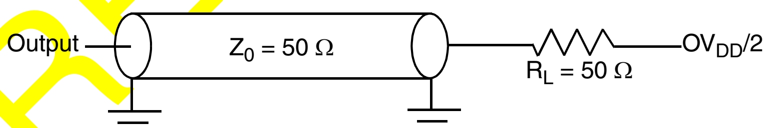
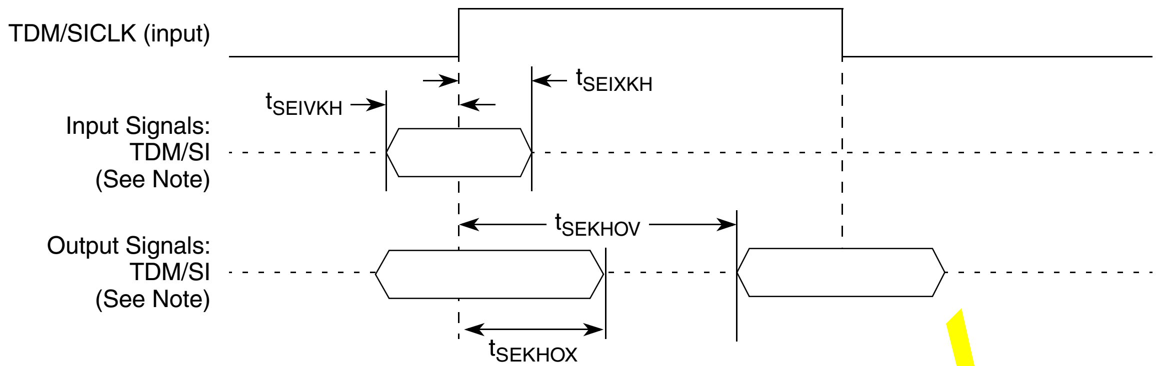


Figure 60. TDM/SI AC Test Load

Figure 61 represents the AC timing from Table 76. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. Figure 61 shows the TDM/SI timing with external clock.



Note: The clock edge is selectable on TDM/SI

Figure 61. TDM/SI AC Timing (External Clock) Diagram

3.4 UTOPIA Interface

This section describes the DC and AC electrical specifications for the UTOPIA of the P101221.

3.4.1 UTOPIA DC Electrical Characteristics

Table 77 provides the DC electrical characteristics for the P1012/21 UTOPIA.

Table 77. UTOPIA DC Electrical Characteristics

For recommended operating conditions, see Table 3

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (BV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

3.4.2 UTOPIA AC Timing Specifications

Table 78 provides the UTOPIA input and output AC timing specifications.

Table 78. UTOPIA AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
UTOPIA/POS outputs—Internal clock delay	t_{UIKHOV}	0	8	ns
UTOPIA/POS outputs—External clock delay	t_{UEKHOV}	1	10	ns
UTOPIA/POS outputs—Internal clock High Impedance	t_{UIKHOX}	0	8	ns

Table 78. UTOPIA AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
UTOPIA/POS outputs—External clock High Impedance	t_{UEKHOX}	1	10	ns
UTOPIA/POS inputs—Internal clock input setup time	t_{UIIVKH}	6	—	ns
UTOPIA/POS inputs—External clock input setup time	t_{UEIVKH}	4	—	ns
UTOPIA/POS inputs—Internal clock input Hold time	t_{UIIXKH}	0	—	ns
UTOPIA/POS inputs—External clock input hold time	t_{UEIXKH}	1	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{UIKHOX} symbolizes the UTOPIA/POS outputs internal timing (UI) for the time t_{Utopia} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 62 provides the AC test load for the UTOPIA.

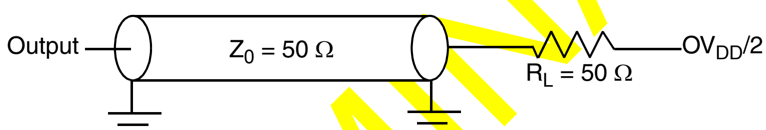


Figure 62. UTOPIA AC Test Load

Figure 63 through Figure 64 represent the AC timing from Table 78. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 63 shows the UTOPIA timing with external clock.

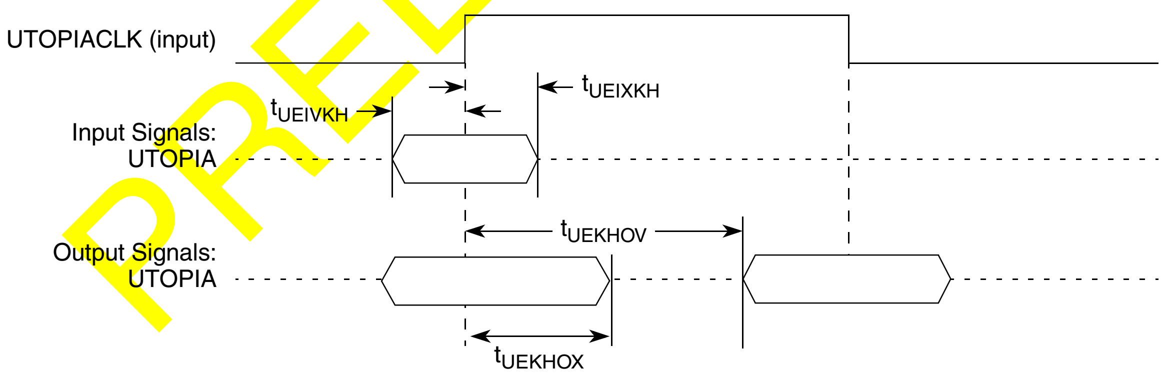


Figure 63. UTOPIA AC Timing (External Clock) Diagram

Figure 64 shows the UTOPIA timing with internal clock.

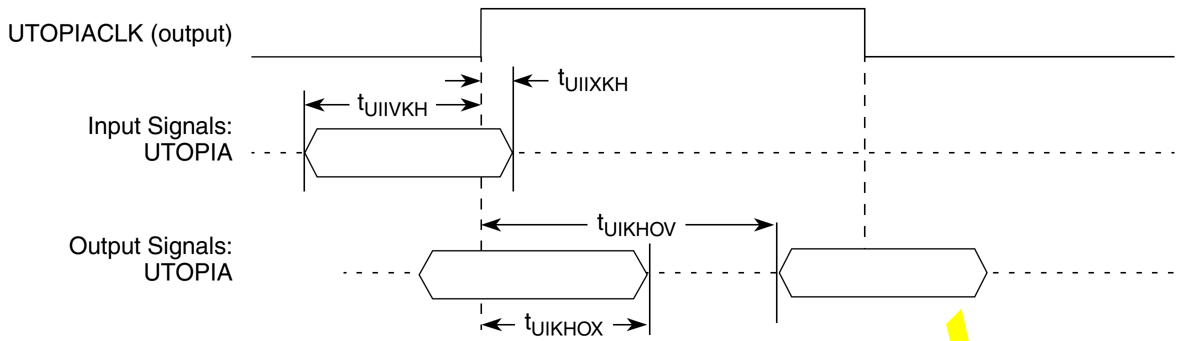


Figure 64. UTOPIA AC Timing (Internal Clock) Diagram

4 Hardware Design Considerations

This section provides electrical and thermal design recommendations for successful application of the P1012.

4.1 Clocking

This section describes the PLL configuration of the P1012. Note that the platform clock is identical to the core complex bus (CCB) clock.

4.1.1 System Clocking

This device includes six PLLs:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 4.1.3, "CCB/SYSCLK PLL Ratio."
- The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 4.1.4, "e500 Core PLL Ratio."
- The enhanced local bus PLL generates the clock for the enhanced local bus.
- There is one PLL for the SerDes block.
- There is one PLL for DDR for asynchronous operation

4.1.2 Clock Ranges

Table 79 provides the clocking specifications for the processor cores and Table 80 provides the clocking specifications for the memory bus.

Table 79. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800 MHz			
	Min	Max		
e500 core processor frequency	333	800	MHz	1, 2, 3

Notes:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 4.1.3, "CCB/SYSCLK PLL Ratio," and Section 4.1.4, "e500 Core PLL Ratio," for ratio settings.
2.The minimum e500 core frequency is based on the minimum platform frequency of 167MHz.
3. These values are preliminary and subject to change

The DDR memory controller can run in either synchronous or asynchronous mode. When running in synchronous mode, the memory bus is clocked relative to the platform clock frequency. When running in asynchronous mode, the memory bus is clocked with its own dedicated PLL. Table 80 provides the clocking specifications for the memory bus.

Table 80. Memory Bus Clocking Specifications

Characteristic	Min	Max	Unit	Notes
DDR2 Memory bus clock speed	200	333	MHz	1, 2
DDR3 Memory bus clock speed	333	333	MHz	1, 2

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 4.1.3, "CCB/SYSCLK PLL Ratio," Section 4.1.4, "e500 Core PLL Ratio," and Section 4.1.5, "DDR/DDRCLK PLL Ratio," for ratio settings.
2. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In asynchronous mode, the memory bus clock speed is dictated by its own PLL. Refer to Section 4.1.5, "DDR/DDRCLK PLL Ratio."

4.1.3 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in Table 81:

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values.

Table 81. CCB Clock Ratio

Binary Value of LA[29:31] Signals	CCB:SYSCLK Ratio
000	4:1
001	5:1
010	6:1
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Reserved

4.1.4 e500 Core PLL Ratio

Table 82 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE and LGPL2 at power up for Core0 as shown in Table 82.

Table 82. e500 Core 0 to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core: CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core: CCB Clock Ratio
000	Reserved	100	2:1
001	Reserved	101	5:2
010	1:1	110	3:1
011	3:2	111	Reserved

4.1.5 DDR/DDRCLK PLL Ratio

The DDR memory controller complex can be synchronous with, or asynchronous to, the CCB, depending on configuration.

Table 83 describes the clock ratio between the DDR memory controller complex and the DDR/DDRCLK PLL reference clock, DDRCLK, which is not the memory bus clock.

When synchronous mode is selected, the memory buses are clocked at half the CCB clock rate. The default mode of operation is for the DDR data rate for the DDR controller to be equal to the CCB clock rate in synchronous mode, or the resulting DDR PLL rate in asynchronous mode. The DDRCLKDR configuration register in the Global Utilities block allows the DDR controller to be run in a divided down mode where the DDR bus clock is half the speed of the default configuration. Changing these defaults must be completed prior to initialization of the DDR controller.

Table 83. DDR Clock Ratio

Binary Value of TSEC_1588_CLK_Out, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 Signals	DDR:DDRCLK Ratio
000	3:1
001	4:1
010	6:1
011	8:1
100	10:1
101	Reserved
110	Reserved
111	Synchronous mode

4.1.6 QUICC Engine to CCB Clock Ratio

The QUICC Engine works on the same clock as CCB.

4.1.7 Frequency Options

4.1.7.1 SYSCLK to Platform Frequency Options

Table 84 shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

Table 84. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)	
	66.66	**100**
	Platform /CCB Frequency (MHz)	
4	267	400
5	333	
6	400	

4.1.7.2 Core to CCB Frequency Options

Table 85 shows the expected frequency values for the core frequency when the e500 core clock PLL inputs that program the core PLLs and establish the ratio between the e500 core clocks and the e500 core complex bus (CCB) clock.

Table 85. Frequency Options for e500 Core Frequency

Core to CCB Ratio	Platform /CCB Frequency (MHz)		
	266	**333**	**400**
	Core Frequency (MHz)		
1:1		333	400
1.5:1	400	500	600
2:1	533	666	800
2.5:1	666		
3:1	800		

4.1.7.3 DDRCLK to DDR controller operating Frequency Options

Table 86 shows the expected frequency values for the DDR controller operating frequency when using external asynchronous clock.

Table 86. DDRCLK to DDR Controller Frequency

DDRC to DDRCLK Ratio	DDRCLK (MHz)			
	66.66	**100**	**133.33**	**166.66**
	DDR Controller Frequency (MHz			
3	200	300	400	500
4	267	400	533	667
6	400	600		
8	533			
10	667			

4.1.8 Minimum Platform Frequency Requirements for High-speed Interfaces

Section 4.4.3.8 “I/O Port Selection” of the P1012 *QorIQ Integrated Host Processor Family Reference Manual,* describes various high-speed interface configuration options. Note that the CCB/platform clock frequency must be considered for proper operation of such interfaces as described below.

For proper PCI Express operation, the CCB/platform clock frequency must be greater than:

$$\frac{500\text{ MHz} \times (\text{PCI Express link width})}{8}$$

See Section 18.1.3.2, "Link Width" of the P1012 *QorIQ Integrated Host Processor Family Reference Manual,* for PCI Express interface width details. Note that the "PCI Express link width" in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

See Section 4.4.3.1, "System PLL Ratio," of the P1012 *QorIQ Integrated Host Processor Family Reference Manual,* for details of selecting this ratio.

4.2 Supply Power Default Setting

P1012 is capable of supporting multiple power supply levels on its I/O supply. Table 87, Table 88, and Table 89 show the encoding used to select the voltage level for each I/O supply.

Table 87. Default Voltage Level for LV_{DD}

LV_{DD} VSEL	I/O Voltage Level
0	3.3 V
1	2.5 V

Table 88. Default Voltage Level for BV_{DD}

BV_{DD} VSEL [0:1]	I/O Voltage Level
00	3.3 V
01	2.5 V
10	1.8 v
11	3.3 v

Table 89. Default Voltage Level for CV_{DD}

CV_{DD} VSEL [0:1]	I/O Voltage Level
00	3.3 V
01	2.5 V
10	1.8 v
11	3.3 v

4.3 Power Supply Design and Sequencing

4.3.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CORE, AV_{DD}_DDR, and AV_{DD}_SRDS respectively). The AV_{DD} level should always be equivalent to V_{DD}, and these voltages must be derived directly from V_{DD} through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 66, one for each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr.

Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of 689 WB-TePBGA the footprint, without the inductance of vias.

Figure 66 shows the PLL power supply filter circuit.

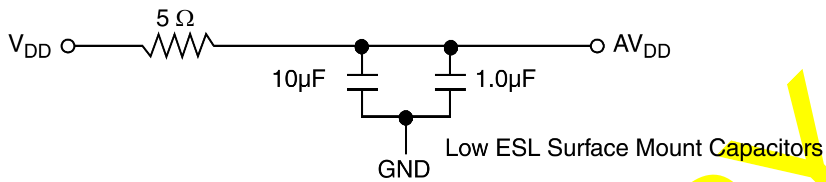


Figure 65. P1012 **PLL Power Supply Filter Circuit**

The AV_{DD}_SRDS signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 66. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS*n* balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDS*n* balls. The 0.003-µF capacitor is closest to the balls, followed by the 1-µF capacitor, and finally the 1 ohm resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.

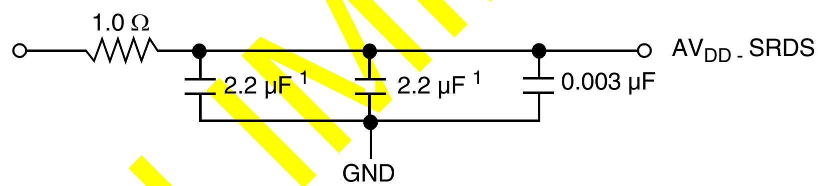


Figure 66. SerDes PLL Power Supply Filter Circuit

Note the following:

- AV_{DD} should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.
- AV_{DD}_SRDS consumes less than 300 mW; SV_{DD} + AV_{DD}_SRDS consumes less than 750 mW.

4.4 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the P1012 system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, BV_{DD}, OV_{DD}, CV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, BV_{DD}, OV_{DD}, CV_{DD}, GV_{DD}, and LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, BV_{DD}, OV_{DD}, CV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

4.5 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

4.6 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to V_{DD}, BV_{DD}, CV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external $V_{DD,}$ BV_{DD}, CV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} and GND pins of the device.

4.7 Pull-Up and Pull-Down Resistor Requirements

The P1012 requires pull-up resistors on open drain type pins including I^2C pins (1 kΩ is recommended) and MPIC interrupt pins (2–10 kΩ is recommended).

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 69. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

The following pins must NOT be pulled down during power-on reset: HRESET_REQ, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[1:4], ASLEEP. The DMA1_DACK_B00 and USB_STP pins must be set to a proper state during POR configuration. Please refer to the pinlist table. See Table 96 for more details.

Table 90. Test Mode Select

DMA1_DACK_B00	USB_STP	TEST_SEL_B	SCAN_MODE_B
1	0	0	1

4.8 Output Buffer DC Impedance

The P1012 drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 61). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

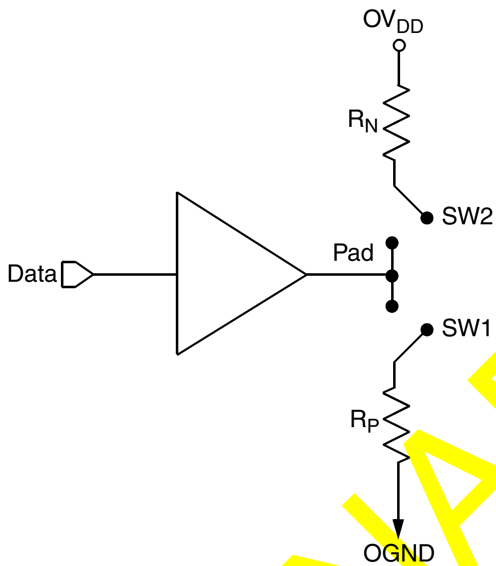


Figure 67. Driver Impedance Measurement

Table 91 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD}, nominal OV_{DD}, 90°C.

Table 91. Impedance Characteristics

Impedance	Enhanced Local Bus, Ethernet, DUART, Control, Configuration, Power Management	DDR DRAM	Symbol	Unit
R_N	43 Target	20 Target	Z_0	W
R_P	43 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See Table 2

4.9 Configuration Pin Muxing

The P1012 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

4.10 JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 69 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 69 for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

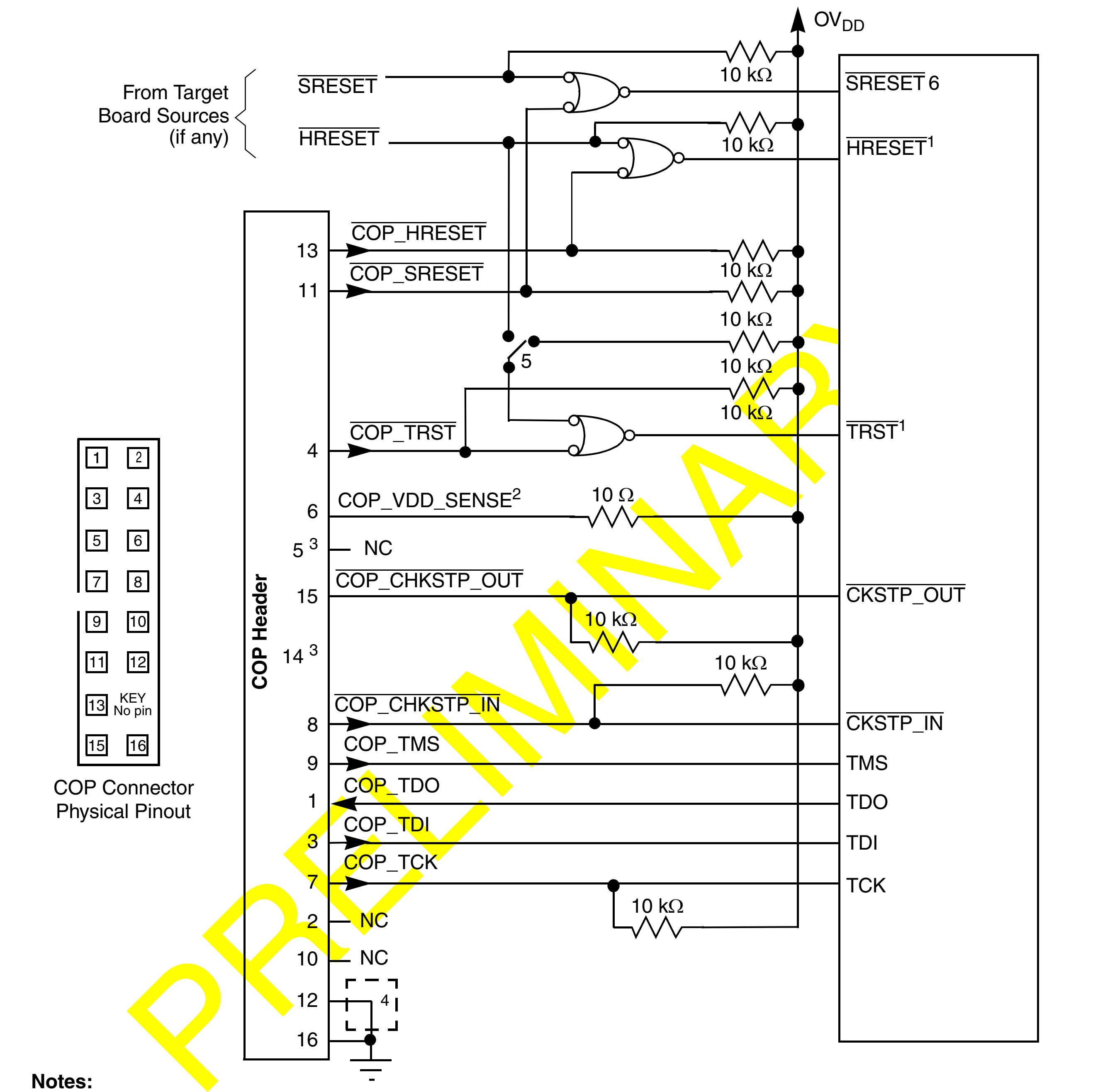
The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 69 is common to all known emulators.

4.10.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 69. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 kΩ resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.



Notes:
1. The COP port and target board should be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.

3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting SRESET causes a machine check interrupt to the e500 core.

Figure 68. JTAG Interface Connection

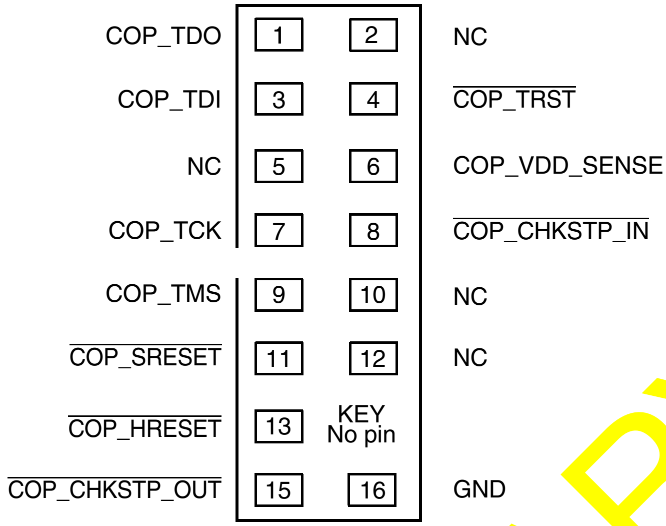


Figure 69. COP Connector Physical Pinout

4.11 Guidelines for High-Speed Interface Termination

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section. However, the SerDes must always have power applied to its supply pins.

The following pins must be left unconnected (float):

- SD_TX[3:0]
- $\overline{\text{SD\_TX}}$[3:0]

The following pins must be connected to GND:

- SD_RX[3:0]
- $\overline{\text{SD\_RX}}$[3:0]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

4.12 Thermal

This section describes the thermal specifications of the P1012.

4.12.1 Thermal Characteristics

Table 92 provides the package thermal characteristics.

Table 92. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	23	°C/W	1, 2
Junction-to-ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	17	°C/W	1, 2,
Junction-to-ambient (at 200 ft/min)	Single layer board (1s)	$R_{\theta JA}$	18	°C/W	1, 2
Junction-to-ambient (at 200 ft/min)	Four layer board (2s2p)	$R_{\theta JA}$	14	°C/W	1, 2
Junction-to-board thermal	—	$R_{\theta JB}$	9	°C/W	3

Table 92. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-case thermal	—	$R_{\theta JC}$	7	°C/W	4

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

Table 93 provides the thermal resistance with heat sink in open flow.

Table 93. Thermal Resistance with Heat Sink in Open Flow

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance (°C/W)
Wakefield 53 × 53 × 25 mm Pin Fin	Natural Convection	10.3
	0.5 m/s	9.0
	1 m/s	8.2
	2 m/s	7.7
	4 m/s	7.4
Aavid 35 x 31 x 23 mm Pin Fin	Natural Convection	12.5
	0.5 m/s	9.9
	1 m/s	9.1
	2 m/s	8.6
	4 m/s	8.2
Aavid 30 x 30 x 9.4 mm Pin Fin	Natural Convection	14.1
	0.5 m/s	12.0
	1 m/s	10.7
	2 m/s	9.6
	4 m/s	8.9
Aavid 43 x 41 x 16.5 mm Pin Fin	Natural Convection	12.4
	0.5 m/s	10.3
	1 m/s	9.1
	2 m/s	8.3
	4 m/s	7.8

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. A power value of 4.5 W was used for the heat sink simulations.The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease.

Simulation Details:

The 1/8 symmetry model included the following package parameters:
Four layer Substrate
Substrate solder mask thickness: 0.030 mm
Substrate metal thicknesses: 0.030mm, 0.064mm, 0.064mm, 0.030 mm
Substrate core thickness: 0.115mm, 0.100mm, 0.115 mm
Core via I.D: 0.118 mm, Core via plating 0.016 mm
Flag: trace style with ground balls under the die connected to the flag
Die Attach: 0.033 mm conductive die attach, k = 1.5 W/m K
Mold Compound: generic mold compound, k = 0.9 W/m K

4.12.1.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, TJ, can be obtained from the equation:

$T_J = T_A + (R_{\theta JA} \times P_D)$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W) The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity TJ - TA) are possible.

4.12.1.2 Heat Sinks and Junction-to-Case Thermal Resistance

In application environments, a heat sink is frequently required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is frequently approximated as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

For P1012in the WB-TEPBGA package, a substantial portion of the heat flow is to the board. Not all the heat flows to the heat sink. As a result, it is inappropriate to size a heat sink based on this equation. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required. To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. Table 93 provides the thermal resistance with a heat sink in an open flow

Table 94. Thermal Resistance with Heat Sink in Open Flow

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance (°C/W)
23x23x10mm Extruded cross cut pin fin, Base is 1.5mm thick AAVID374024B60023G	Natural Convection	16.9
	0.5 m/s	13.8
	1 m/s	12.1
	2 m/s	10.6
38x38x16.5 mm Extruded cross cut pin fin, Base is 5 mm thick AAVID2330B	Natural Convection	13.8
	0.5 m/s	11.5
	1 m/s	10.7
	2 m/s	9.5
53x54x25 mm Extruded cross cut pin fin Base is 3.7 mm thick Wakefield 698100AB	Natural Convection	13.0
	0.5 m/s	10.4
	1 m/s	9.3
	2 m/s	8.8

The thermal resistances with heat sinks were simulated in an open flow environment per JEDEC JESD51-6 with the part on a 2s2p board as specified in JESD51-9. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease.

4.12.2 Recommended Thermal Model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

4.12.3 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (WB-TePBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The P1012 implements several features designed to assist with thermal management, including the temperature diode. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system

The recommended attachment method to the heat sink is illustrated in Figure 70. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).

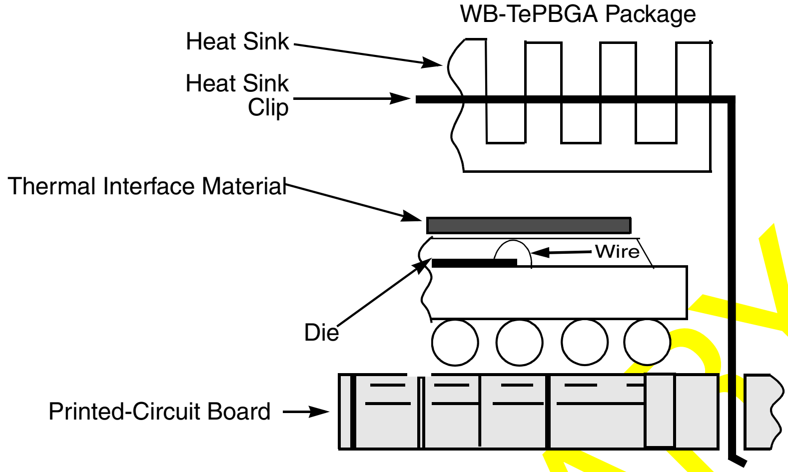


Figure 70. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the device. Ultimately, the final selection of an appropriate heat sink depends on factors such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Aavid Thermalloy

Internet: www.aavidthermalloy.com

Alpha Novatech

Internet: www.alphanovatech.com

Wakefield Engineering

Internet: www.wakefield.com

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Corporate Center P.O.Box 999 Midland, MI 48686-0997 Internet: www.dow.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

4.12.3.1 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb force (45 Newtons). If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

4.12.3.2 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted between the case of the package and the heat sink. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction to case thermal resistance.

$T_J = T_C + (R_{\theta JC} x\ P_D)$

Where

T_c is the case temperature of the package

$R_{\theta JC}$ is the junction-to-case thermal resistance

P_D is the power dissipation

5 Package Information

5.1 Package Parameters for the P1012 WB-TePBGA

The package parameters are provided in the following list. The package type is 31 mm × 31 mm, 689 plastic ball grid array (WB-TePBGA).

Package outline	31 mm × 31 mm
Interconnects	689
Pitch	1.00 mm
Module height (typical)	2.0 mm to 2.46 mm (Maximum)
Solder Balls	3.5% Ag, 96.5% Sn
Ball diameter (typical)	0.60 mm

Figure 75 shows the P1012 package.

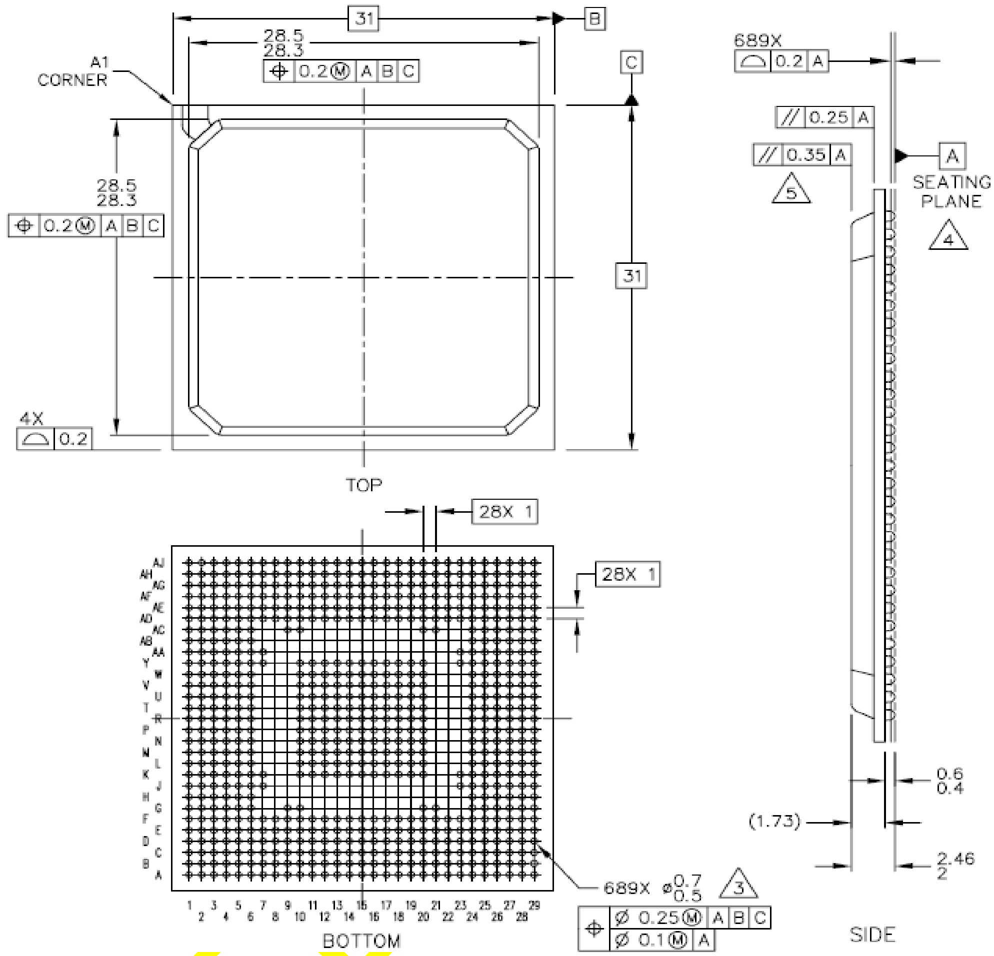


Figure 71. P1012 **Package**

NOTES for Figure 75**:**

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14. 5M-1994.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

5.2 Ordering Information

Table 95 provides the Freescale part numbering nomenclature for the P1020/21. Each part number also contains a revision code which refers to the die mask revision number.

Table 95. Part Numbering Nomenclature

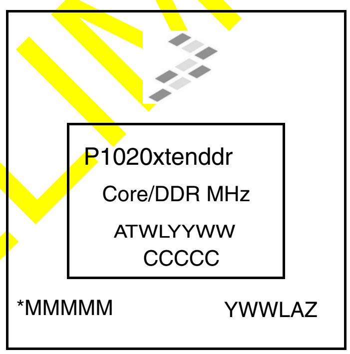
P	1	02 or 01	2	q	t	e	n	dd	r
Generation	**Platform**	**Number of Cores**	**Derivative**	**Qual Status**	**Temperature Range**	**Encryption**	**Package Type**	**CPU/CCB/DDR Frequency (MHz)**	**Die Revision**
P	1	01	2	N	S	E	2	FF	B
P= 45nm	1–5	01 = Single Core 02 = Dual Core	0–9	P = Prototype N = Qual'd to Industral Tier S = Special	S = Std Temp X = Ext. Temp	E = SEC Present N = SEC Not Present	2 = TEPBGA Pbfree	HF = 800/400/667 FF = 667/333/667 DF = 533/333/667 FD =667/333/533	A = 1.0 B = 1.1

Notes:

1. See Section 5, "Package Information," for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

3) The QUICC engine RISC clock speed is equal to the CCB/Platform speed.

Parts are marked as the example shown in Figure 72.



WB-TePBGA

Notes:

P1020xtenddr is the orderable part number
*MMMMM is the mask number
YWWLAZ is the assembly traceability code.
CCCCC is the country code
ATWLYYWW is the standard assembly, test, year and work week codes.

Figure 72. Part Marking for WB-TePBGA Device

6 Product Documentation

The following documents are required for a complete description of the device and are needed to design properly with the part:

- P1012 *QorIQ Integrated Processor Reference Manual* (document number P1012RM)
- e500 PowerPC Core Reference Manual (E500CORERM)

7 Revision History

Table 96 provides a revision history for the P1012 hardware specification.

Table 96. Document Revision History

Rev. Number	Date	Substantive Change(s)
L	10/2010	• Updated Package Numbering Nomenclature Table 95 • Updated the Thermal Characteristic Section 4.12, “Thermal • Replaced DDR3 DC Electrical Spec with DDR2 DC Electrical Spec Table 15
K	9/2010	• Swapped AV_{DD}_CORE0 and AV_{DD}_CORE1 to F16 and F15 in Table 1as this pins are swapped in silicon. • Minor edit on foot notes of Table 1 • Updated DDR Spec Table 17 and Table 19 • Updated Package Numbering Nomenclature Table 95 • Removed DDR2 DC electrical spec • Added DDR3 DC electrical spec
J	6/2010	• Added Footnotes to pins • Changed R&C values of Core PLL filter circuit • Removed DDR3 DC Electrical spec • Removed t_{NIKHOX} and t_{NIKHOV} spec from eSPI as it is not required with new feature Hold adjust • Removed eLBC PLL enabled mode AC spec
H	5/2010	• Added TEST_SEL_B and SCAN_MODE_B pins in Table 90: Test Mode Select • Updated eLBC spec to match standard C45 spec • Added DC and AC Spec for MII and RMII • Removed qq parmeter from Table 95 Part Numbering Nomenclature
G	3/2010	• Changed SYSCLK min to 64MHz from 66.7Mhz • Changed all 0.95V Spec to 1.0V • Added table for e500 core1 PLL ratio POR configuration bits • Added USB DC Electrical Specification for 2.5V and 1.8V • Added eSPI DC Electrical Specification for 2.5V and 1.8V • Changed RGMII T_{SKRGT_RX} from 2.8ns to 2.6ns • Added Part Ordering Information table
F	10/2009	• Modified Table 13 $\overline{\text{HREST}}$ Min parameter • Modified Table 74 Synchronous UART parameter t_{HIIVKH} • Modified Table 55 eSDHC parameter $t_{SFSIVKH}$ • Remove eSPI AC Spec Note 3 , As SPCOM[RxDelay] bit is removed. • Added Table 15 max PLL Lock Time • Changed the conditional texting of partnumber P1011202112 in order to generate separate document for single core products.

Table 96. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
E	5/2009	• Added Section 4.1.7.2, “Core to CCB Frequency Options” and Section 4.1.7.3, “DDRCLK to DDR controller operating Frequency Options” • Modified Table 84 to remove option of 33MHz • In Table 83, marked options 110 as reserved. • In Table 82, marked options 000, 001, & 111 as reserved. • In Table 79, marked options 100 & 101 as reserved. • Removed the row of t_{I2CR} and changed all the notes of Table 61 • Modified all the notes in Table 59 • Added Section 2.13.1, “PIC DC Electrical Characteristics”, Section 2.13.2, “PIC AC Timing Specifications”, and Section 2.14.1, “JTAG DC Electrical Characteristics” • Changed all the values in Table 55 • Removed min value of V_{IL}, max value for V_{IH} and changed value of V_{OH} & V_{OL} in Table 54, Table 60, , • Modified Figure 34 & Figure 35 and removed figure titled as “Enhanced Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (PLL Bypass Mode)” • Removed min value of V_{IL}, max value for V_{IH} and changed value of V_{OH} & V_{OL} in Table 50
		• Changed notes of Table 48 • Removed min value of V_{IL}, max value for V_{IH} and changed value of V_{OH} & V_{OL} in Table 41 • Rewrote Section 2.9, “Ethernet: Enhanced Three-Speed Ethernet (eTSEC)”, Section 2.16, “High-Speed Serial Interfaces (HSSI)”, and Section 2.17, “PCI Express” • Removed min value of V_{IL}, max value for V_{IH} and changed value of V_{OH} & V_{OL} in Table 28 • Modified Table 15 • Added two rows for $t_{NIKHOX2}$ and $t_{NIKHOV2}$ inTable 27 • Added a row each for t_{NIKHOX} & t_{NIKHOV} for different values of SPCOM[RxDelay] in Table 27 • Removed min value of VIL, max value for VIH and added two notes in Table 26 • Renamed Table 11 • Added rows on the basis of frequency for V_{ILAC} and V_{IHAC} in Table 18 • Added a row in Table 17 for DDR3
		• Added note 2 in Table 16 • Changed all the values and notes in Table 17 • Added note 4, 5, and 6 in Table 15 • Added note 2 in Table 13 • In Table 8, removed min valie of Frequency modulcation and added note 2. • Replace old notes with new notes in Table 7 • In Table 7, changed the min value for fSYSCLK from 33MHz to 66.7 MHz and hence max SYSCLK cycle time to 15ns. • Added Table 6, Table 9, Section 2.4.5, “DDR Clock Timing”, Figure 10, Section 2.6.2.3, “DDR2 and DDR3 SDRAM Differential Timing Specifications, Section 2.11.2.1, “Test Condition, • Changed the range of all 1V signal from 0.95V to 1.05V in Figure 2 • Shortenned feature list in intorductory section • Replaced SENSEVDD and SENSEVSS with NC103 and NC104 in Table 1 • Changed frequency combination from 400-600Mhz to 267-533MHz in Table 5

Table 96. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
D	4/2009	Changes done onTable 1 • Renamed all XVDD_SRDS to XV_{DD}_SRDS • Renamed all AVDD_CORE0 to AV_{DD}_CORE0, AVDD_CORE1 to AV_{DD}_CORE1, AVDD_DDR to AV_{DD}_DDR, AVDD_PLAT to AV_{DD}_PLAT, AVDD_SRDS to AV_{DD}_SRDS, SVDD_SRDS to SV_{DD}_SRDS • Replaced AV_{DD}_LBIU with NC102 as eLBC PLL has been removed • V_{DD} has been split into V_{DD} & V_{DDC} Changes in Table 2 & Table 3 • Added a row for V_{DDC} • PLL AVDD expanded to AV_{DD}_CORE0, AV_{DD}_CORE1, AV_{DD}_DDR, AV_{DD}_PLAT, and AV_{DD}_SRDS • Changed SVDD to SV_{DD}_SRDS, XVDD to XV_{DD}_SRDS
C	2/2009	• Shifted Piinout List from Section 5.2 to Section 1.2, “Pinout Assignments” • Following changes were done on Table 1 : Replaced • NC54 with MECC05, • NC55 with MECC06, • NC56 with MECC07, • DMA2_DACK_B00 with CFG_MEM_DEBUG, • and DMA2_DDONE_B00 with CFG_DDR_DEBUG Added • LB_MSRCID00 / PLL_PER_OUT00 to P28, • LB_MSRCID01 / PLL_PER_OUT01 to R27, • LB_MSRCID02 / PLL_PER_OUT02 to P27, • LB_MSRCID03 / PLL_PER_OUT03 to P26, • LB_MSRCID04 / PLL_UP_DN to N26, • and LB_MDVAL / PLL_PER_VALID to M24 Removed • DMA2_DREQ_B1, • DMA2_DACK_B1, • DMA2_DDONE_B[1],and USB_VBUSEN

Table 96. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
B	12/2008	• Removed adjective "weak" for pull up from first line of first paragraph of Section 4.7, "Pull-Up and Pull-Down Resistor Requirements" • Removed Note 3 stating "memory bus clock should be less than CCB clock rate" in Table 80 • Renamed $t_{LBKHOV4}$ to $t_{LBKLOV4}$ in Table 51 • Added a note below Table 51 • Changed the platform frequency from 400 to 333Mhz in second row of Table 5 • Removed E from • Modified eTSEC features in introductory section. • Added TSEC1_GTX_CLK125, TSEC3_RX_DV, TSEC3_RX_CLK, TSEC3_RXD[3:0], CFG_DRAM_TYPE, CFG_IO_PORTS3, SDHC_DAT[7:4], TDM_TFS, TDM_TX_CLK, TDM_RFS, TDM_RX_DATA in Table 1 • Removed TSEC2_TXD05, TSEC2_TXD04, TSEC2_TXD01, TSEC2_TX_ER, TSEC2_CRS and TSEC2_COL from Table 1. • • Added suppport for x2 and x4 port in PCIe feature list • Added Note 1 in Table 1 • Removed all the references, figures and tables for PLL Enable. Added figures and tables for PLL Bypas mode in Section 2.11, "Enhanced Local Bus" • Changed minimum time of t_{MCK} from 2.5ns to 3ns in Table 21 • Added Section 2.9.5, "MII Management" • Added simlation details in Section 4.12.1, "Thermal Characteristics" • Added data in Table 92 and Table 93.
A	10/2008	Initial release.

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