Akhilesh Kumar Jaiswal (India-Bangalore)

From: hari.r@arrowasia.com
Sent: Friday, June 17, 2011 8:27 AM
To: Akhilesh Kumar Jaiswal (India-Bangalore)
Cc: vinod.tarale@arrowasia.com
Subject: RE: Internet Tech Support - LAN8720 / Mindteck


Crystal Frequency Stability Se...


Schematic Checklist LAN8720 QF...

Hi Akhilesh

Please find below the SMSC review

we have looked over your LAN8720i design and for the most part, it was very good. I did have some minor comments; please review:

1. I checked your schematic shape for the LAN8720i pin-by-pin and found one problem there. You'll need to add a pin 25 to your shape for the EDP (Exposed Die Paddle) grounding pad underneath the LAN8720i. This pin should be connected directly to your digital ground plane.

2. I only checked the U13 section of your schematic. Please be sure to apply all these fixes as necessary to the U14 section of your schematic as well.

3. I couldn't review the magnetics you've selected for use with the LAN8720i as you did not provide a vendor or data sheet for the magnetics. I like to verify the pinouts and the operational characteristics of the magnetics for our customers when they deviate from the norm.

4. I also couldn't review your RJ45 pinout as that was not included in your schematic for this review.

5. Please verify that R53, R54, R55 & R56 in your design are all sized to at least SMD_ 0805 components. This will ensure proper power delivery in all modes of operation. For your Industrial Temp application, you may even elect to use SMD_1206 components.

6. Please be sure to take your VDDA_ENET1 analog power rail over your backplane connection to the magnetics. The two shorted center taps of the magnetics must be powered directly from the VDDA_ENET1 power rail.

7. Currently, you have the two analog power rails of U13 & U14 shorted together. You'll need to separate these two rails so each Phy has it's own
VDDA_ENET1 & VDDA_ENET5 rail.

8. C30 in your schematic should be a bulk capacitor for this analog power rail.

9. Make sure you have connected your EDP pin to digital ground.

10. Please review the latest copy of the LAN8720 schematic checklist attached below. You should find all these details within.

11. Please verify that C41 in your design is a low ESR capacitor. The low ESR requirement is to ensure the proper stability of the +1.2V internal regulator of the LAN8720i. We recommend a high quality, low ESR, ceramic type capacitor for this particular application.

12. In addition, C31 should be a 470 pF capacitor. Check the schematic checklist below (page 7) for more details.

13. Please verify that the 50.000 MHz oscillator and U11 in your design introduces no more than 200 pS of added jitter to the clock input. The low jitter requirement for the clock input is necessary in order to meet the stringent IEEE waveform jitter specification. Specifically, this is Cycle-to-Cycle jitter measured Peak-to-Peak.

14. Also on the oscillator, please be sure of it's accuracy. The LAN8720i requires a 25.000 MHz clock accuracy of better than +/- 50 PPM over the entire temperature range of your application. Please see the next paper below for more details on this subject. The paper speaks of a crystal, but the information is applicable to an oscillator as well.

15. Your RMII series terminations should probably be more on the order of 10 - 22 ohms instead of 100 ohms.

16. As for the rest of the RMII interface, that interface looks OK. Just double check all your connections; make sure inputs on the LAN8720i are being driven by outputs from the MAC in your design. Likewise, make sure outputs from the LAN8720i are driving inputs on the MAC.

17. It probably makes more sense to separate the two interrupt outputs of the Phys in your application. Right now, they are both labeled IRQ5_ENET#.

18. D1 power for R43 should be from your VDDA_ENET1 power rail. Please see page 14 of the checklist below for more details.

19. For the LAN8720i, a hardware reset (nRST assertion) is required following power-up. Please refer to the latest copy of the LAN8720i data sheet for reset timing requirements. SMSC does not recommend the use of an RC circuit for this required pin reset. A reset generator / voltage monitor is one option to provide a proper reset. Better yet, for increased design flexibility, a controllable reset (GPIO, dedicated reset output) should be considered. In this case, SMSC recommends a push-pull type output (not an open-drain type) for the monotonic reset to ensure a sharp rise time transition from low-to-high.

20. It might also make sense to allow for two separate reset lines for the Phys. With each Phy having it's own reset, this should provide enough flexibility in your design to overcome any unforeseen problems.

21. There is one other thing to be aware of when designing with the LAN8720i. Please double check the timing and states of all lines from the SOC/FPGA in your system to configuration strap pins on the LAN8720i. We have had customers get into odd operational states when, during reset, the SOC connected to the LAN8720i, drives the configuration strap pin to an unexpected level. So, in your design, just double check and make certain what the SOC/FPGA part in your system is doing during reset. If the SOC/FPGA's normal state during reset is to drive any line opposite to one of the LAN8720i's weak internal pull-ups/pull-downs, you're going to have a conflict. So, just be sure and double check all the pins on the LAN8720i where you are relying on the weak internal pull-up/pull-down to take affect during reset. Check Tables 2.1 through 2.5 in the LAN8720i data sheet for details on which pins have internal pull-ups / pull-downs.

22. Configuration strap values are typically latched on power-on reset and system reset. SMSC will guarantee that the proper high / low level will be latched in on any device pin with an internal pull-up or pull-down where the device pin is a true no-connect. However, when the configuration strap pin (typically an output pin) is connected to a load, the input leakage current associated with the input load may have an adverse affect on the high / low level ability of the internal pull-up / pull-down. In this case, it is SMSC's recommendation to include an external resistor to augment the internal pull-up / pull-down to ensure the proper high / low level for configuration strap values. Lower VDDIO voltages will further exacerbate this condition.

23. I'd like to learn more about your specific application in order that we may provide additional information to you to enhance your Ethernet design.
If your application calls for strict Ethernet waveform compliance testing, ESD compliance testing, EMC compliance testing or EMI Class "A" compliance testing, knowledge of what testing you require would help us understand your design better. If you need any of this type of compliance testing, let me know and I may have additional information and

application notes for you to consider for your Ethernet design.

24. For instance, one common thread we have been seeing with EMI testing is increased EMI levels with the use of integrated magnetics. It seems any noise riding on the PCB is much more easily coupled into the magnetics and then passed into the CAT-5 cable when an integrated solution is used. By switching to a discrete magnetic solution, you gain separation in the Ethernet front end and, as a result, we see lower EMI readings with this configuration. So, if you have the board space, want to save some money and need to pass stringent Class "A" EMI levels, you might want to consider switching to a discrete magnetic solution.

25. Otherwise, everything else looks good in your design.

Please fidn below the attached
(See attached file: Crystal Frequency Stability Selection.pdf)(See attached file: Schematic Checklist LAN8720 QFN Rev B.pdf)

With regards
Hari R
----- Forwarded by HARI R/IN/AEIL/AAP on 06/17/2011 08:23 AM -----

HARI R
06/16/2011 06:49 PM

To: "Akhilesh Kumar Jaiswal (India-Bangalore)" <akhilesh.jaiswal@mindteck.com>
cc: Madhur.Dogra@smsc.com, vinod.tarale@arrowasia.com
Subject: RE: Internet Tech Support - LAN8720 / Mindteck(Document link: HARI R)

Hi akhilesh

we will clarify on trace length . The schematics review are under progress and update .

With regards
Hari R

"Akhilesh Kumar Jaiswal (India-Bangalore)" <akhilesh.jaiswal@mindteck.com>
06/16/2011 06:22 PM

To: <hari.r@arrowasia.com>
cc: <vinod.tarale@arrowasia.com>, <Madhur.Dogra@smsc.com>
Subject: RE: Internet Tech Support - LAN8720 / Mindteck

Hi Hari,

Please send me the contact details of technical support person from SMSC.
Basically I need some clarification on the below implementation. I want to know if is there any trace length matching requirement between the two clocks/ clock and RMII signals. Also is there any recommended minimum/maximum trace length for RMII signals?

Also pleas send me the update on the schematic I submitted for review.

Regards,

Akhilesh

-----Original Message-----

From: Akhilesh Kumar Jaiswal (India-Bangalore)

Sent: Tuesday, June 07, 2011 3:36 PM

To: 'hari.r@arrowasia.com'

Cc: vinod.tarale@arrowasia.com

Subject: RE: Internet Tech Support - LAN8720 / Mindteck

Hi,

I have attached the correct schematic for the review.

Regards,

Akhilesh

-----Original Message-----

From: hari.r@arrowasia.com [mailto:hari.r@arrowasia.com]

Sent: Monday, June 06, 2011 9:34 AM

To: Akhilesh Kumar Jaiswal (India-Bangalore)

Cc: vinod.tarale@arrowasia.com

Subject: RE: Internet Tech Support - LAN8720 / Mindteck

Dear Akhilesh

I could not find the SMSC 8720 - in the attached schematics

. Please check and confirm .

With regards

Hari R

"Akhilesh Kumar Jaiswal (India-Bangalore)" <akhilesh.jaiswal@mindteck.com>

To: <Madhur.Dogra@smsc.com>

cc: <hari.r@arrowasia.com>, <vinod.tarale@arrowasia.com>

Subject: RE: Internet Tech Support - LAN8720 / Mindteck

06/03/2011 04:54 PM

Hi Madhur,

I have attached the schematic pdf for your review

Warm Regards,

Akhilesh Jaiswal

(Embedded image moved to file: pic16413.gif)Tech Lead, PES

Mindteck | 16/3, Cambridge Road, Bangalore 560 008, India.

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From: Madhur.Dogra@smsc.com [mailto:Madhur.Dogra@smsc.com]

Sent: Friday, June 03, 2011 1:45 PM

To: Akhilesh Kumar Jaiswal (India-Bangalore)

Cc: hari.r@arrowasia.com; vinod.tarale@arrowasia.com

Subject: Fw: Internet Tech Support - LAN8720 / Mindteck

Hi Akhilesh,

Please submit your schematic for review check.

Best Regards

MD

Smart Mixed-Signal Connectivity

SMSC,India

www.smsc.com

Cell:-+919880060631

"Creating Valued Connectivity Ecosystem"

----- Forwarded by Madhur Dogra/SMSC on 03-06-2011 13:47 -----

From: Eric Tang/SMSC

To: Madhur Dogra/SMSC@SMSC

Cc: HC Tan/SMSC@SMSC, YongLin Li/SMSC@SMSC

Date: 03-06-2011 12:26

Subject: Internet Tech Support - LAN8720 / Mindteck

Madhur,

Pls follow up.

Thanks,

Eric

REQUEST INFORMATION

Summary: Tech Support Request from the Internet

I am designing a hot swappable board using LAN8720Ai. I want to know

will there

be any issue while inserting my board in an active system where the

MDI lines

of LAN8720Ai are connected to the other active board before it

(LAN8720Ai) is

powered up and its reset is released?

	COMPANY/CONTACT INFORMATION	(Embedded image moved to file: pic29168.gif)	(Embedded image moved to file: pic00900.gif)
Contact Name:	Akhilesh Jaiswal	Address:	16/3 Cambridge Road
Company:	Mindteck	City:	Bangalore

Country:	India	State/Prvnce:	Karnataka
Phone #:	Unknown	Postal Code:	560008
FAX #:	(Embedded image moved to file: pic32591.gif)	E-Mail Addr:	akhilesh.jaiswal@mindteck.com

(See attached file: KSZ8721_Mindteck.pdf)