Freescale Semiconductor
Application Note

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Design Checklist for QorIQ™ P1020 and P1021 Processor

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This document provides recommendations for designs based on the P1020 and the P1021 devices from the QorIQ™ family of integrated communications processors. This document may also be useful in debugging newly designed systems by highlighting those aspects of a design that merit special attention during initial system bring-up. The P1020 and the P1021 both combines dual Power Architecture™ e500v2 processor cores with system logic required for networking, wireless infrastructure, and telecommunications applications.

Contents

1 Getting Started

This section outlines recommendations to simplify the first phase of design. Before designing a system with a P1020/21 device, it is recommended that the designer be familiar with the available documentation, software, microcodes, models, and tools.

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1.1 References

Please note that some items below may only be available under a nondisclosure agreement (NDA). For those documents, please contact your local field applications engineer or sales representative to obtain a copy.

- Collateral
  - — *QorIQ TM P1020 Integrated Processor Reference Manual* (P1020RM)
  - — *QorIQ TM P1021 Integrated Processor Reference Manual* (P1021RM)
  - — *P1020 Chip Errata* (P1020CE)
  - — *P1021 Chip Errata* (P1021CE)
  - — *QorIQ TM P1020 Integrated Processor Hardware Specifications* (P1020EC)
  - — *QorIQ TM P1021 Integrated Processor Hardware Specifications* (P1020EC)
- Available Tools
  - — Pin Mux Tool
- Models
  - — IBIS
  - — SWIFT (Verilog)
  - — BSDL, Rev 1.0 silicon

1.2 Device Errata

The device errata documents (P1020CE, P1021CE) describe the latest fixes and work arounds for the family of QorIQ^{TM} P1020/21 devices. The errata documents should be thoroughly researched prior to starting a design with the respective QorIQ^{TM} device.

1.3 Pin Mux Tool

To verify the availability of the I/O functions chosen through pin multiplexing, designers are encouraged to use the P1020 Pin Mux Tool. After selecting the signals required by your application, this utility assists in defining the pin configuration . A report can then be generated that includes all your selections and C-initialization code for the registers associated with the I/O ports.

The Pin Mux Tool can be found on the P1020/21 device website.

1.4 Available Training

Our 3rd party partners are part of an extensive Design Alliance Program. Our current training partners can be found on our external website under the Design Alliance Program.

In addition to this, training material from past Smart Network Developer's Forums is available. The training material is a valuable resource for understanding the QorIQ and is also available on the website.

2 Power

This section provides design considerations for the QorIQ P1020/21 power supplies. For information on AC and DC electrical specifications and thermal characteristics for theP1020/21, refer to the P1020EC and the P1021EC.

2.1 Power Supply

The P1020/21 has a core voltage V_{DDC} and V_{DD} which operates at a lower voltage than the I/O voltages GV_{DD}, LV_{DD}, OV_{DD}, BV_{DD} and CV_{DD}. It is recommended that the core voltages V_{DD}/V_{DDC} of P1020/21 be supplied through a variable switching supply or regulator to allow for future compatibility with possible core voltage changes on future silicon revisions. The core voltages, 1.0 V (±5%), is supplied across V_{DD} ,V_{DDC} and GND.

The DDR I/O's of P1020/21 are supplied with 1.8V (±5%) in case of DDR2 or 1.5V(±5%) in case of DDR3 memories across GV_{DD} and GND., 2.5 V (±5%) or 3.3 V (±5%) across LV_{DD} and GND, 3.3 V (±5%) across OV_{DD} and GND,and 1.5V(±5%), 2.5 V (±5%) or 3.3 V (±5%) across CV_{DD}/$BV_{DD}$and GND. Typically, these are supplied by simple linear regulators. This increases the complexity of the system because multiple voltage supplies and PCB power planes are required for the design. No external signals on P1020/21 are 5 V tolerant. All input signals need to meet the G/L/OV_{IN} DC specification of the respective I/O block.

Table 1. Power Supplies

Type	Name	Block	(V)
Core 0	V_{DDC}	Core 0 and Platform supply volatge	1.0
Core 1	V_{DD}	Core 1 supply voltage	1.0
PLL	AV_{DD}	Core 0/1PLL, Platform PLL,DDR PLL, SRDS PLL	1.0
SerDes core	SV_{DD}_SRDS	Core power supply for SerDes transceivers	1.0
SerDes Pad	XV_{DD}_SRDS	Pad power supply for SerDes transceivers	1.0
I/O	GV_{DD}	DDR2/3 DRAM I/O voltage	1.5/1.8
I/O	LV_{DD}	Three-speed Ethernet I/O, MII management voltage (eTSEC)	2.5 / 3.3
I/O	OV_{DD}	DUART, system control and power management, I^2C, and JTAG I/O voltage	3.3
I/O	CV_{DD}	USB, eSPI, eSDHC	1.5/2.5/3.3
I/O	BV_{DD}	Enhanced local bus I/O voltage and GPIOx8 voltage	1.5/2.5/3.3

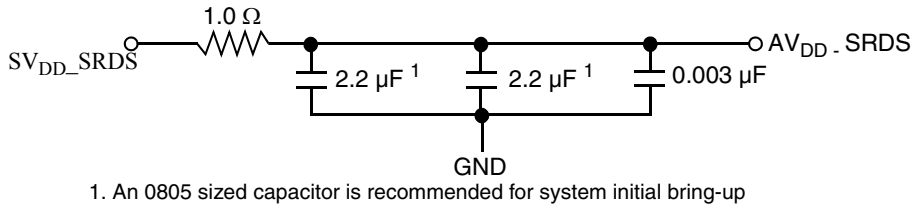
2.2 SerDes Power Supply

There are three different supplies used in SerDesBlock

- SV_{DD}_SRDS: Core power supply for SerDes transceivers
- XV_{DD}_SRDS: Pad power supply for SerDes transceivers
- AV_{DD}_SRDS: SerDesPLL supply

Signals on the SerDes interface are fed from the XV_{DD} power plan. It needs to be taken into consideration for designing XV_{DD} return path on PCB. AV_{DD}_SRDS should be a filtered version of SV_{DD}.The AV_{DD}_SRDS signal provides power for the analog portions of the SerDesPLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 1. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS ball to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDS ball. The 0.003-µF capacitor is closest to the balls,followed by the 1-µF capacitor, and finally the 1 ohm resistor to the board supply plane. The capacitors are

connected from AV_{DD}_SRDS*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequencyAll traces should be kept short, wide, and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up

Figure 1. SerDes PLL Power Supply Filter Circuit

2.3 Power Consumption

The P1020EC and the P1021EC Hardware Specification documents provide estimated power dissipation for various frequency configurations of the core complex bus (CCB) clock and the e500 core frequencies. Suitable thermal management is required to ensure the junction temperature does not exceed the maximum specified value.

Keep in mind that the numbers provided in the hardware specification include dissipation for all blocks except the PLL supplies and the I/Os. Both must be added to the typical number in order to accurately determine whether a heat sink or other form of chip cooling mechanism is required.

To estimate the I/O power consumption for the P1020/21, designers are encouraged to use the P1020/21 Power Consumption Calculator Tool. Users are required to enter valid clock frequencies and a valid V_{DD} voltage. Even though the tool recognizes individual invalid parameter values, it does not recognize combinations of invalid parameters. To ensure valid combinations, users should refer to the relevant hardware specification document. All fields are required.

2.4 Power Sequencing

One consequence of multiple power supplies is that when power is initially applied, the voltage rails will ramp up at different rates. These rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. However, with the advancement in the QorIQ ESD design, the order in which the various QorIQ power rails ramp is open without adverse effect to the QorIQ device as long as the supplies do not exceed absolute maximum ratings (as defined in the device-specific hardware specification documents). The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation.It is required before GVDD gets powered-up, supplies like VDD, AVDD, BVDD, LVDD, OVDD,CVDD, SVDD_SRDS, XVDD_SRDS (there is no ordering requirment with respect to one another) must be stable. All Supplies must be at their stable values within 50 ms.

NOTE

From a system standpoint, If any of the I/O power supplies ramp prior to VDD core supplies, the associated I/O supply may drive a logic one or zero during power-up thus causing excessive current to be drawn by the device

Below are the current maximum ratings for the power supplies. Supplies must not exceed these absolute maximum ratings. However, during normal operation, use of the recommended operating conditions given in the hardware specification is recommended. Any information in the relevant hardware specification supersedes information in Table 2.

Table 2. Maximum Voltage Ratings

Type	Name	Block	(V)	(Vmax)
Core	V_{DD},V_{DDC}	-	1	1.05
PLL	AV_{DD}AVDD_CORE0,AVDD_CORE1,AVDD_DDR,AVDD_PLAT,AVDD_SRDS	Core PLL, Platform PLL	1	1.05
SerDes	SVDD_SRDS, XVDD_SRDS	SerDes transceivers Core and Pad power supply	1	1.05
I/O	GV_{DD}	DDR	1.5/1.8	1.98
I/O	LV_{DD}	TSEC	2.5 / 3.3	2.75 / 3.63
I/O	OV_{DD}	DUART, system control and power management, I2C, and JTAG I/O voltage	3.3	3.63
I/O	CV_{DD}	USB, eSPI, eSDHC	1.8/2.5/3.3	1.98/2.75/3.63
I/O	BV_{DD}	Enhanced local bus I/O voltage and GPIOx8 voltage	1.8/2.5/3.3	1.98/2.75/3.63

2.5 Power Planes

Each V_{DD} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip.The capacitor leads and associated printed circuit traces connecting to chip V_{DD} and ground should be kept to less than half an inch per capacitor lead.

2.6 Decoupling

Due to large address and data buses, and high operating frequencies, the P1020/21 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the P1020/21 system, and the P1020/21 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DDC},V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, CV_{DD} and BV_{DD} pins of the P1020/21. These decoupling capacitors should receive their power from separateV_{DDC}, V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, CV_{DD} ,$BV_{DD}$and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DDC},V_{DD}, GV_{DD}, LV_{DD}, OV_{DD} ,CV_{DD} and BV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF.

Simulation is strongly recommended to minimize noise on the power supplies before proceeding into the PCB design and manufacturing stage of development.

2.7 SerDes Decoupling

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-µF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

2.8 PLL Power Supply Filtering

Each of the PLLs is provided with power through independent power supply pins (AVDD_PLAT, AVDD_CORE,AVDD_DDR, and AVDD_SRDS respectively). The AVDD level should always be equivalent to VDD, and these voltages must be derived directly from VDD through a low frequency filter scheme.The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 2, one for each of the AVDD pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced. This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr.Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor. Each circuit should be placed as close as possible to the specific AVDD pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AVDD pin, which is on the periphery of 689 WB-TePBGA the footprint, without the inductance of vias.

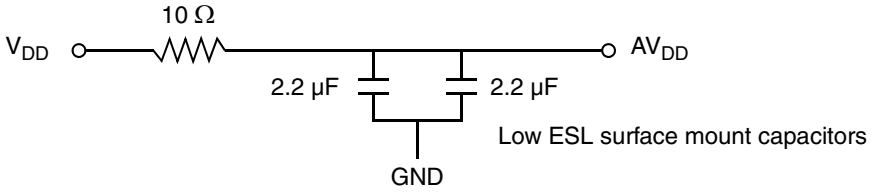


Figure 2. PLL Power Supply Filter Circuit

3 Clocking

3.1 System Clock

The P1021 takes a single input clock, SYSCLK, as its primary clock source for the e500 core and all of the devices and interfaces that operate synchronously with the core. The system clock SYSCLK input (frequency) is multiplied up using a phase lock loop (PLL) to create the core complex bus (CCB) clock (also called the platform clock). The CCB clock is used by virtually all of the synchronous system logic, including the L2 cache, and other internal blocks such as the DMA and interrupt controller. The CCB clock also feeds the PLLs in the e500 cores and the PLL that create clocks for the local bus memory controller. Note that the divide-by-two CCB clock divider and the divide-by-*n* CCB clock divider, are located in the DDR and local bus blocks, respectively. The DDR memory controller complex may use the platform clock and thus have operation of both DDR interfaces be synchronous with the platform. Alternately, an independent clock, DDRCLK, may be multiplied up using a separate PLL to create a unique DDR memory controller complex clock. In this case, the DDR complex operates asynchronous with respect to the platform clock

Table 3. Clocking Quick Reference

Functional Block	Clock Derivation
Core (including L1)	CCB * [1.5,2, 2.5, 3]
DDR	CCB / 2(Synchronous Mode) or DDRCLK
QUICC Engine	CCB
L2 cache, CPM	CCB
Local Bus	CCB / [4,8,16]
SerDes	100MHz/125Mhz External
USB_CLK	ULPI PHY clock
SDHC_CLK	CCB
SPI_CLK	CCB
I^2C	CCB / (I2CFDR ratio)
TSEC	125MHz from PHY or External (certain modes)

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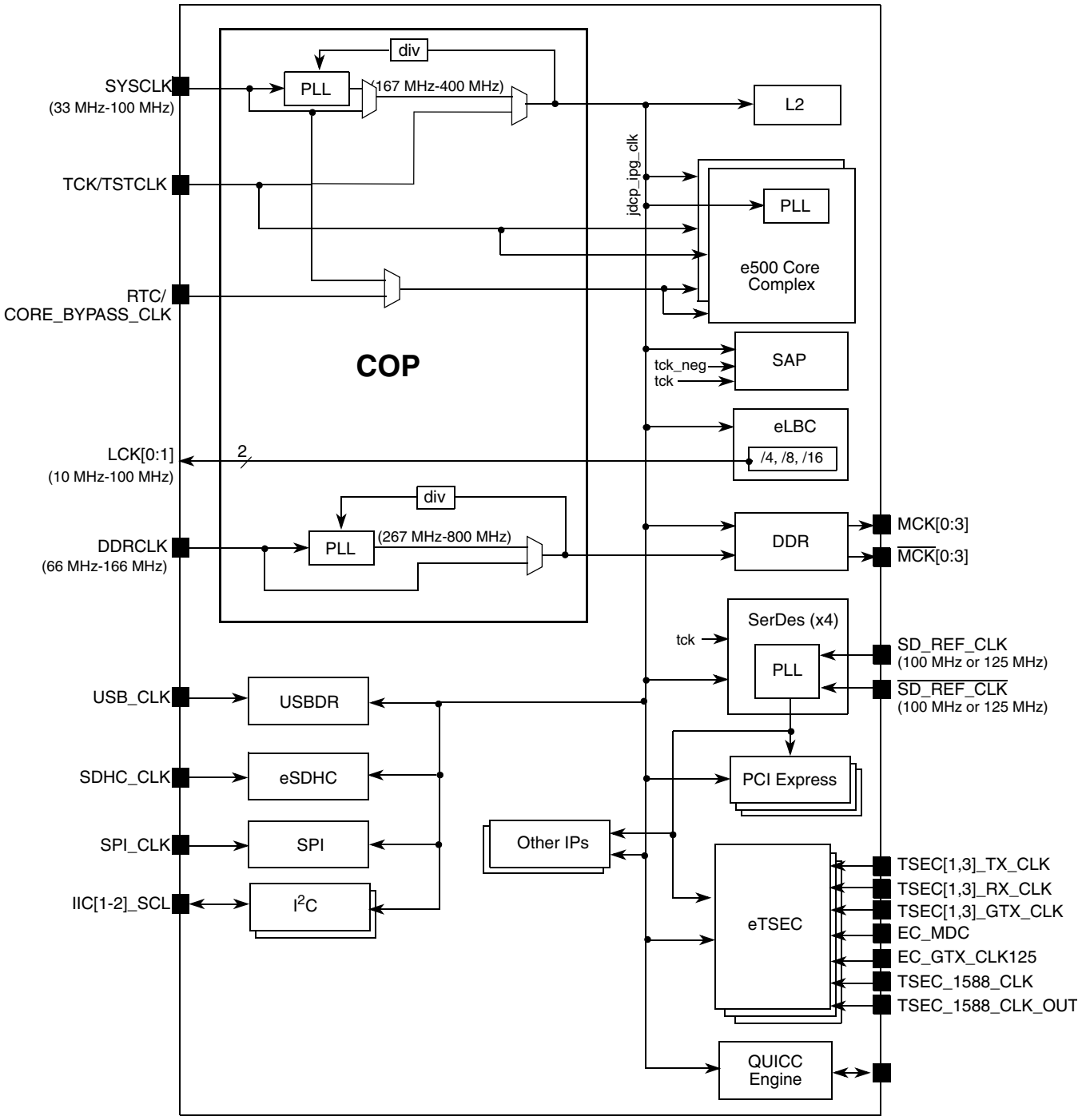

Figure 3-3. P1021 Clock Subsystem Block DiagramClocking Example

Assume that the frequencies of certain key interfaces should be maximized. Then use the following inputs:

- SYSCLK = 66 MHz
- DDRCLK = 66 MHz
- RTC= 66 MHz

- SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ = 100MHz
- EC_GTX_CLK = 125MHz
- CCB multiplier = 6 (cfg_sys_pll)
- Core0 multiplier = 2(cfg_core0_pll)
- Core1 multiplier = 2(cfg_core1_pll)
- DDR Multiplier = 10(cfg_ddr_pll)
- Local bus divider = 4 (LCRR[CLKDIV])

The resulting frequencies for the following interfaces are:

- Core0 = SYSCLK * cfg_sys_pll * cfg_core0_pll = 800 MHz
- Core1 = SYSCLK * cfg_sys_pll * cfg_core1_pll = 800 MHz
- DDR (MCK*n*) = DDRCLK * cfg_ddr_pll = 667 MHz
- PCI Express x1 = 2.5 Gbps Bit Rate
- SGMII x1= 1.25Gbaud rate
- Local Bus (LCLK*n*) = SYSCLK * cfg_sys_pll / CLKLDIV = 100 MHz

These frequencies are the maximum frequencies supported today. Please check the relevant product website for updated options.

3.2 E500 Core Clock

The frequency of the cores is determined at POR through the LBCTL, LALE and LGPL2 pins for e500 core0 and for e500 core1 LWE0, UART_SOUT1and READY_P1 pins. Below in Table 4 and Table 5are the options for configuring the core clock as a multiple of the CCB clock. This information can be found in the P1020/21RM .

Table 4. E500 Core0 Clock POR Configuration

LBCTL, LALE,LGPL2	E500 Core: CCB
000	Reserved
001	Reserved
010	1:1
011	1.5:1
100	2:1
101	2.5:1
110	3:1
111	Reserved

Table 5. E500 Core1 Clock POR Configuration

LWE0, UART_SOUT1, READY_P1	E500 Core: CCB
000	Reserved
001	Reserved
010	1:1

Table 5. E500 Core1 Clock POR Configuration

LWE0, UART_SOUT1, READY_P1	E500 Core: CCB
011	1.5:1
100	2:1
101	2.5:1
110	3:1
111	Reserved

3.3 DDR SDRAM Clock Outputs

The DDR PLL inputs, shown in Table 6, establish the clock ratio between the DDRCLK input and the DDR complex clock. This DDR complex clock domain is asynchronous to the platform clock or CCB clock domain, and is sourced from a separate PLL than the rest of the platform, unless the DDR PLL encoding for synchronous mode operation is selected. When synchronous mode is selected, the DDR complex is driven by the CCB clock, which becomes the DDR data rate. There is no default value for this PLL ratio; these signals must be pulled to the desired values.

Table 6. DDR Complex Clock POR Configuration

TSEC_1588_CLK_OUT,TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2	DDR Core Complex : DDRCLK Ratio
000	3:1
001	4:1
010	6:1
011	8:1
100	10:1
101	12:1
110	Reserved
111	Synchronous mode

3.4 SerDes Clock

The SerDes reference clock inputs are SD_REF_CLK and SD_REF_CLK_B. Each differential clock input phase has a 50 ohm termination to GND. The reference clock must be able to drive this termination. The input is AC-coupled on chip following the termination.The input amplitude of the clock must be between 400 mV and 1600mV differential peak-peak. In addition, each phase of the input clock must be less than 800 mV peak-peak.

The common mode voltage at the clock inputs must be between 0 and 400 mV. The differential reference clock (SD_REF_CLK/SD_REF_CLK) input is HCSL compatible DC coupled or LVDS compatible with AC coupling.

3.4.1 PCI Express or SGMII Clocking

The P1020/21 processor contains an integrated Lynx SerDes that can be programmed to act as either a PCI Express lane or SGMII interface. This PHY has its own PLL and requires a 125 MHz or 100 MHz differential clock reference

input. SGMII requires 125 MHz, and PCI Express requires a 100 MHz clock. The reference is 1 V and not 3.3 V. The PHY generates its own transmit and receive sampling clock. The receive clock is recreated from the receive data. The PHY supplies the transmit/receive clock between the PHY and the MAC (PCI Express controller/eTSEC controller). Synchronization between the MAC and the CCB clock domain occurs in the MAC. For proper synchronization, the CCB must be running at a higher frequency than the transmit/receive clock.

3.5 Ethernet Clock

When running in RGMII or MII modes (not using the SerDes) the reference clock is supplied by the GTX_CLK125 input on the eTSEC interface.The Ethernet blocks operate asynchronously with respect to the rest of the device. These blocks use receive and transmit clocks supplied by their respective PHY chips, plus a 125-MHz clock input for gigabit protocols. Data transfers are synchronized to the CCB clock internally.

3.6 Real Time Clock

The real time clock (RTC) input can optionally be used to clock the e500 core timer facilities. RTC can also be used (optionally) by the P1021 programmable interrupt controller (PIC) global timer facilities. The RTC is separate from the e500 core clock and is intended to support relatively low frequency timing applications. The RTC frequency range is specified in the *P1021 QorIQ™ Integrated Processor Hardware Specifications*, but the maximum value should not exceed one-quarter of the CCB frequency.

4 Debug

The following sections describes the P1020/21 reset sequence and recommendations for the system.

4.1 $\overline{\text{TRST}}$

$\overline{\text{TRST}}$ is the reset pin for the JTAG/COP interface. It must be held at a low level during the assertion of $\overline{\text{HRESET}}$ in order to completely reset all logic on the P1020/21.

For compatibility with third party tools, it is required that $\overline{\text{TRST}}$ and $\overline{\text{HRESET}}$ have the ability to independently assert. Figure 4 demonstrates one example of circuity that can be used to accomplish this:

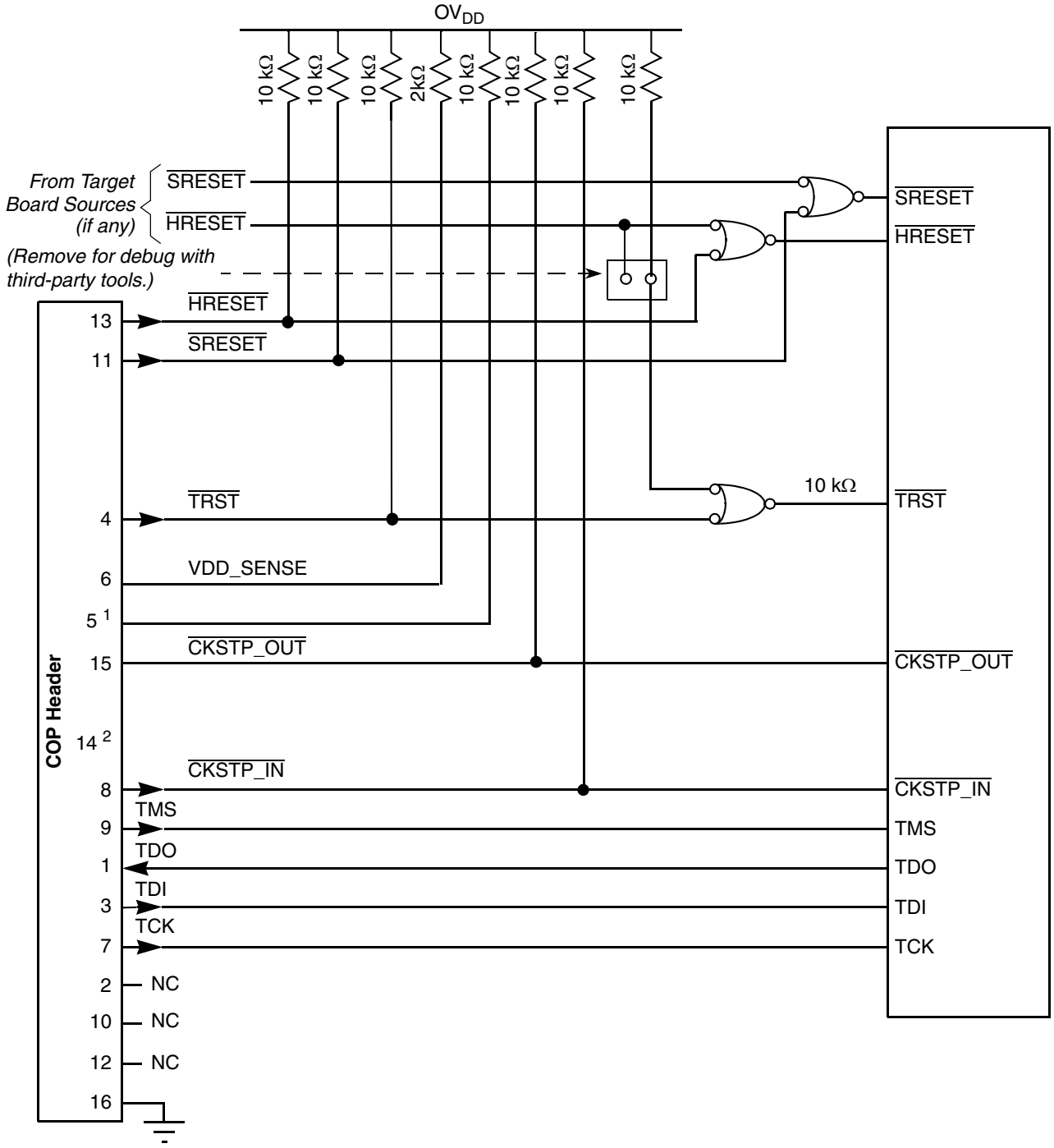

Figure 4. COP Connections to P1020/21

The COP header is fully described in Figure 5 and Table 7.

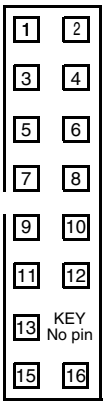

Figure 5. COP Header Pinout

Table 7. COP Header Definition

Header Position	Name	Description
1	TDO	Test Data Output
2	NC	
3	TDI	Test Data Input
4	TRST	Test Reset
5	Not implemented. Connect to OV_{DD} with a 10 KΩ resistor.	
6	VDDS	VDD Sense
7	TCK	Test Clock
8	CKI	Checkstop In
9	TMS	Test Mode Select
10	NC	
11	SRST	Soft Reset
12	NC	
13	HRST	Hard Reset
14	KEY	
15	CKO	Checkstop Out
16	GND	Ground

4.2 Recommended Test Points

For easier debug, it is recommended that the test points on the board include the following pins:

- TRIG_OUT/READY (This helps to verify the end of the reset sequence)
- TRIG_IN (Trigger in to trigger the watchpointand trace buffers. Note: this is an active-high rising-edge triggered signal)
- IRQ_OUT (Interrupt output)
- ASLEEP (This helps to verify the end of the reset sequence)
- HRESET_REQ (This helps to verify proper boot sequencer functionsand reset requests)
- MSRCID [0:4] (This helps identify the owner of the bus cycle)
- MDVAL (This helps identify when the data is valid)
- SD_PLL_TPA (SerDesAnalog PLL lock indication)
- SD_PLL_TPD (SerDesDigital PLL lock indication)
- CKSTP_OUT (e500 checkstopindication)
- CLK_OUT (This helps to verify the CCB clock)
- SYSCLK (To verify input clock at the device pin)
- DDRCLK (To verify DDR Clkwhen in asynchronies mode)
- DDR MCK[0:5] and MCK_B[0:5] -visibility of at least one data bit for each clock domain and its associated clock to check the data eye and signal integrity.
- LCLK[0:2] -local bus clock, at least make one of signals visible.
- SD_REF_CLK and SD_REF_CLK_B (Reference clocks for SGMII/PCI Express SerDes block)
- SerDesTransmission Lanes
- Berg connector would be optimum if it is a differential clock

5 Power-On Reset and Reset Configurations

5.1 Configurable Options

Various device functions are initialized by sampling certain signals during the assertion of $\overline{\text{HRESET}}$. These inputs are either pulled high or low during this period. While these pins are generally output pins during normal operation, they are treated as inputs while $\overline{\text{HRESET}}$ is asserted. $\overline{\text{HRESET}}$ must be asserted for a minimum on 25µs. When $\overline{\text{HRESET}}$ de-asserts, the configuration pins are sampled and latched into registers and the pins then take on their normal output circuit characteristic from an input circuit during $\overline{\text{HRESET}}$.

Most of the configuration pins have an internally gated 20 KΩ pull-up resistor, enabled only during $\overline{\text{HRESET}}$. For those configurations in which the default state is desired, no external pull-up is required. Otherwise, a 4.7 KΩ pull-down resistor is recommended to pull the configuration pin to a valid logic low level. In the case where a configuration pin has no default, 4.7 KΩ pull-up or pull-down resistors are recommended for appropriate configuration of the pin. Table 8 summarizes all the power-on reset configurations possible on the device.

Table 8. Power-On Reset Configurations

Type of Configuration	Configuration Pins	Default State
CCB Clock PLL Ratio	LA[29:31]	**No default state;** pins must be configured at $\overline{\text{HRESET}}$
e500 Core0 PLL Ratio	LBCTL,LALE, LGPL2	**No default state;** pins must be configured at $\overline{\text{HRESET}}$
e500 Core1 PLL Ratio	$\overline{\text{LWE0}}$, UART_SOUT1, READY_P1	**No default state;** pins must be configured at $\overline{\text{HRESET}}$
Boot ROM Location	TSEC1_TXD[6:4], TSEC1_TX_ER	Local Bus GPCM, 16-bit ROM
Host/Agent	$\overline{\text{LWE1}}$,LA[18:19]	P1020/21 acts as the host processor/root complex for all PCI Express interfaces
I/O Port Selection	TSEC1_TXD[3:1], CFG_IO_PORTS	PCI Express 1 (x2) (2.5 Gbps) . SerDes lanes 0-1 SGMII eTSEC2 (x1) (1.25Gbps) . SerDes lane 2 SGMII eTSEC3 (x1) (1.25Gbps) . SerDes lane 3
CPU Boot	LA27,LA16	The e500 core is allowed to boot without waiting for configuration from any external master
Boot Sequencer	LGPL3, LGPL5	Boot sequencer is disabled.No I^2C ROM is accessed.
DDR SDRAM Type	CFG_DRAM_TYPE	DDR3,1.5 V, CKE low at reset
SerDes Reference Clock Configuration	TSEC_1588_ALARM_OUT1	SerDes expects a 100 MHz reference clock frequency
TSEC Width	EC_MDC	Ethernet interfaces operate in standard SGMII or RGMII modes
TSEC1 Protocol	TSEC1_TXD0,TSEC1_TXD7	TSEC1 operates using the RGMII protocol
TSEC2 Protocol	TSEC1_TXD7,TSEC1_TXD7	TSEC2 operates using the SGMII protocol
TSEC3 Protocol	UART_RTS0,UART_RTS1,TSEC_1588_ALARM_OUT2	TSEC3 operates using the RGMII protocol
Memory Debug Configuration	CFG_MEM_DEBUG	Debug information from the DDR SDRAM controller is driven on the MSRCID and MDVAL signals.
DDR Debug Configuration	CFG_DDR_DEBUG	Debug information is not driven on ECC pins. ECC pins function in their normal mode
General-Purpose POR Configuration	LAD[0:15]	**No default state;** General-purpose POR configuration vector to be placed in GPPORCR
eLBC ECC Enable Configuration	MSRCID0	eLBC ECC checking is enabled
System Speed	LA28	SYSCLK frequency is at or above 66 MHz
Platform Speed	LA23	Platform clock frequency is at or above 300 MHz
e500 Core 0 Speed	LA24	Core 0 clock frequency is greater than 450 MHz
e500 Core 1Speed	LA25	Core 1 clock frequency is greater than 450 MHz

Table 8. Power-On Reset Configurations (continued)

Type of Configuration	Configuration Pins	Default State
DDR Speed	LA26	DDR clock frequency is greater than or equal to 450 MHz
LVDD Voltage Configuration	LVDD_VSEL	**No default state;** pins must be configured.
BVDD Voltage Configuration	BVDD_VSEL[0:1]	**No default state;** pins must be configured.
CVDD Voltage Configuration	CVDD_VSEL[0:1]	**No default state;** pins must be configured.

An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device which drives the configuration signals when $\overline{\text{HRESET}}$ is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the de-assertion of $\overline{\text{HRESET}}$ (PLL configuration inputs must meet a 100 ms set-up time to $\overline{\text{HRESET}}$), hold their values for at least 2 SYSCLK cycles after the de-assertion of $\overline{\text{HRESET}}$, and tri-state the pins afterward for normal device operation.

For a more detailed description on the power-on reset configurations and their definitions, refer to the P1020RM or the P1021RM.

The POR configuration settings can be read in the POR PLL status register (PORPLLSR), the POR boot mode status register (PORBMSR), the POR device status register (PORDEVSR), the POR debug mode status register (PODBGMSR), the POR device status register 2 (PORDEVSR2) and the general-purpose POR configuration register (GPPORCR). See the P1020RM or the P1021RM for details of these registers. (Note that all of these registers are read-only registers.)

The general purpose POR configuration register (GPPORCR) can be used to pass any information on the local bus address/data pins LAD[0:31] to software. For instance, we can pass information about a circuit board's revision number to software by driving the pins in any order. The information is automatically sampled from LAD[0:31] during POR. Then software can at any time read this register and process the data accordingly. There is no default settings for this register. If it is not used, it is not necessary to drive the pins high or low.

5.2 Internal Manufacturing Test Modes

A few pins on the P1020/21 device have a secondary function of enabling internal manufacturing test modes on the device. These modes are enabled during the HRESET sequence by driving the respective pin to a logic zero state.

NOTE

If any of these modes are enabled during normal operation of the device, the device will not come out of reset, and the system will hang.

To avoid accidentally enabling these internal test modes, care should be taken to make sure that these pins are either floating (as they implement an internal weak pull-up resistor), or are pulled high during the reset sequence in the event that they are connected to a device which pulls these pins low.

There are some additional test pins which must be pulled up by a resistor connected to OV_{DD} during all normal operation of the device. If any of these pins are pulled low, the system may hang. (Please refer to the P1020EC or the P1021EC).

Table 9. Internal Test Mode and Debug Pins

Pin	Pin Type	Comment
ASLEEP	Internal test mode	Pull up or leave floating during reset only
HRESET_REQ	Internal debug	Pull up to OV_{DD}
MSRCID[2:4]	Internal debug	Pull up to OV_{DD}
TRIG_OUT/READY/QUIESCE	Internal debug	Pull up to OV_{DD}
DMA1_DACK_B[0]	Internal testmode	Pull up to OV_{DD}
USB1_STP	Internal test mode	Pull up to OV_{DD}

5.3 Boot Sequencer

The boot sequencer allows configuration of any memory mapped register prior to running the boot-up code. When enabled, it will load code from an EEPROM located on the I^2C bus. For example, this code can be used to configure the port interface registers if the device is booting from PCI-E, ,eSPI or eSDHC.

The boot sequencer is enabled during power-on reset by the [LGPL3, LGPL5] pins. These two signals can also enable extended boot sequencer mode.

Please refer to the P1020RM or the P1021RM for the complete data format for programming the I^2C EEPROM.

The CRC algorithm used is:

$$1 + x^1 + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$$

The start value is 0xFFFF_FFFF. The final XOR value is 0x0000_0000.

The boot sequencer contains a basic level of error detection. If a preamble or CRC fail is detected, the external HRESET_REQ will assert. The I^2C pins will continue to be pulled low during a fail until a hard reset occurs.

5.4 Boot Hold-off Mode

The P1020/21 can be put into slave mode in a system by configuring with pin cfg_cpu0_boot = 0b0 for Core0 and cfg_cpu1_boot = 0b0 Core1. In this situation, an external master on the PCI-E, will need to configure the device. Boot hold-off mode, when enabled during power-on reset, allows any external master on these buses to configure the device. To enable this mode during power-on reset, use the LA27 and LA16 pin. During this mode, the core is suspended from fetching boot code. To exit this mode, the EEBPCR[CPU0_EN] for Core0 and EEBPCR[CPU1_EN] for Core1 is set by external masters.

6 Functional Blocks

The following sections discuss the recommendations and guidelines for designing with the various functional blocks on P1020/21.

6.1 Global Utilities

The P1020/21 provides a global utilities block which controls power management, I/O device enabling, power-on reset configuration monitoring, and other debug functions. Refer to Section 5.1, “Configurable Options”. Below is information about the device disable register (DEVDISR) and low-power modes of which the designer should be aware.

6.1.1 Device Disable Register (DEVDISR)

After the P1020/21 comes out of reset, all functional blocks are enabled. However, there are situations where all interfaces of the P1020/21 may not be used. In this case, it would be more power efficient to disable these interfaces.The DEVDISR contains disable bits for the PCI-E0/1, SEC,USB,eSDHC,eLBC,DMA,TSEC1/2/3, DDR, e500 Core 0/1, QE,Time Base,SPI,DUART and the I^2C interface. If desired, these blocks may be disabled by setting these bits to a logic 1 by the core or an external master.

When a block is disabled with this register, all clocks are disabled to the block, thereby saving power. However, a result of not having clocks to an interface is that the interface will not respond to any interrupts or accesses. A programming error will occur when trying to access configuration or status registers of a block while disabled.

These interfaces may not be re-enabled without asserting $\overline{\text{HRESET}}$. Without asserting $\overline{\text{HRESET}}$, the results will be undefined.

Disabling the e500 core through this register is equivalent to nap mode. This is not recommended since any interface disabled through DEVDISR requires an $\overline{\text{HRESET}}$ to re-enable it. Use the low-power nap mode instead.

6.1.2 Low-Power Modes

In addition to the DEVDISR, the P1020/21 allows you to further reduce the power consumption through the low-power modes. There are three low-power modes: doze, nap, and sleep. Detailed information about these modes can be found in the relevant user’s manual.

Putting the device into nap mode is equivalent to disabling the e500 core through the DEVDISR register. However, since waking up the device is not possible when using the DEVDISR except through an $\overline{\text{HRESET}}$, it is recommended that nap mode be used instead.

6.2 DDR SDRAM

Please refer to *AN2910 Hardware and Layout Design Considerations for DDR2SDRAM Memory Interfaces* for detailed information on signal integrity and layout considerations.

Configuration of the DDR bus should not be done while running from it, but rather by executing code from another interface (that is, the local bus). DDRCLK input is only required when the P1020/21 DDR controller is running in asynchronous mode. When the DDR controller is configured to run in synchronous mode via POR setting cfg_ddr_pll[0:2]=111, the DDRCLK input is not required. It is recommended to tie it off to GND when DDR controller is running in synchronous mode.

6.2.1 Termination of DDR Signals During Normal Operation

Parallel termination is optional for DDR signals and should be simulated to verify necessity. Differential termination is included on DIMM. It is only required for discrete memory applications. MDIC[0:1] are used for automatic calibration of the DDR IOs. MDIC[00] is grounded through an 18.2-K (full-strength mode) or 36.4-K (half strength mode) precision 1% resistor. MDIC[01] is connected to GVDD through an 18.2-K (full-strength mode) or 36.4 (half-strength mode) precision 1% resistor.

Refer to the application note AN2910 for more detail on termination schemes.

It is strongly recommended that with any termination scheme, signal integrity analysis be performed using the respective device IBIS model.

6.2.2 Termination of Unused DDR Signals

Termination is not needed on output signals.

For I/Os, tie signals high or low through a resistor. Recommended resistor values are 2–10 KΩ.

For inputs, tie signals to their inactive state through a resistor; clock inputs may be tied high or low. Recommended resistor values are 2–10 KΩ.

6.3 Enhanced Three-Speed Ethernet Controllers (eTSEC)

The enhanced three-speed Ethernet controller (eTSEC) supports 10, 100, and 1000 Mbps Ethernet/802.3 networks. The complete eTSEC is designed for single MAC applications with several standard MAC-PHY interfaces to connect to an external Ethernet transceiver:

- IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802ab compliant
- 10/100 Mbps RGMII
- 1000 Mbps full-duplex RGMII
- 10/100 Mbps SGMII
- 1000 Mbps full-duplex SGMII

Three eTSECs can be independently configured to support any one of these interfaces. The POR configuration controls the hardware configuration of theseTSEC MAC-PHY interfaces.

Table 10 shows the pin usage and software configuration for each particular MAC-PHY mode.

Table 10. eTSEC MAC-PHY Modes

	MII	RGMII
EC_GTX_CLK125	—	125 MHz clock
TSEC*n*_COL	COL	—
TSEC*n*_CRS	CRS	—
TSEC*n*_GTX_CLK	—	GTX_CLK
TSEC*n*_RX_CLK	RX_CLK	RX_CLK
TSEC*n*_RX_DV	RX_DV	RX_CTL
TSEC*n*_RX_ER	RX_ER	—
TSEC*n*_RXD[3:0]	RxD[3:0]	RxD[3:0]
TSEC*n*_TX_CLK	TX_CLK	—
TSEC*n*_TXD[3:0]	TxD[3:0]	TxD[3:0]
TSEC*n*_TX_EN	TX_EN	TX_CTL
TSEC*n*_TX_ER	TX_ER	—

The eTSEC has one management interface that controls all external PHYs. The management interface of eTSEC1 controls the PHY from eTSEC1 as well as all external PHYs.

Table 11. Enhanced Three-Speed Ethernet Controller Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
TSEC_MDC	O	As needed	Open	
TSEC_MDIO	I/O	As needed + 2 k–10 kΩ to LV_{DD1}	2 k–10 kΩ to LV_{DD1}	Open drain signal
TSEC_GTX_CLK125	I	125 MHz clock	1 kΩ to GND	A 125 MHz reference clock should be supplied if either eTSEC is being used in RGMII or RTBI modes.
TSECn_COL	I/O	As needed	1 kΩ to GND	
TSECn_CRS	I/O	As needed	1 kΩ to GND	
TSECn_GTX_CLK	O	As needed	Open	Actively driven during $\overline{\text{RESET}}$
TSECn_RX_CLK	I	As needed	1 kΩ to GND	
TSECn_RX_DV	I	As needed	1 kΩ to GND	
TSECn_RX_ER	I	As needed	1 kΩ to GND	
TSECn_RXD[3:0]	I	As needed	1 kΩ to GND	

Table 11. Enhanced Three-Speed Ethernet Controller Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
TSECn_TX_CLK	I	As needed	1 kΩ to GND	
TSECn_TXD[3:0]	O	As needed	Open	
TSECn_TX_EN	O	As needed	Open	
TSECn_TX_ER	O	As needed	Open	

6.4 SerDes PHY (PCI Express/SGMII Interface)

The SerDes PHY block operates in the following modes (see Figure 6):

- Four SerDes lanes running at 2.5 GHz (multiplexed across controllers)
- Two lanes running 1x SGMII at 1.25 Gbps
- Two lanes running 1x PCI Express at 2.5 Gbps.

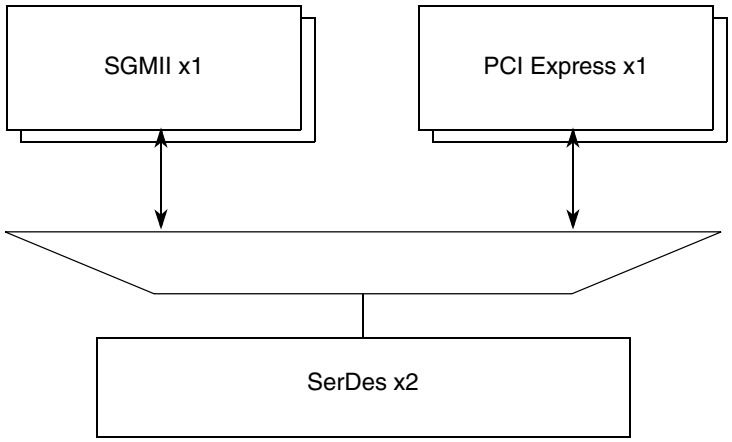

Figure 6. SerDes PHY Operating Modes

The SerDes interface is supported in both P1020 and P1021 devices, and Table 12 lists the pins and the implementation notes.

Table 12. SerDes Pin List

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
TXA	O	—	Open	Differential signal, serial transmitter, lane A, positive data
$\overline{\text{TXA}}$	O	—	Open	Differential signal, serial transmitter, lane A, negative data

Table 12. SerDes Pin List (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
RXA	I	—	Connect to GND	Differential signal, serial receiver, lane A, positive data
$\overline{\text{RXA}}$	I	—	Connect to GND	Differential signal, serial receiver, lane A, negative data
TXB	O	As needed	Open	Differential signal, serial transmitter, lane E, positive data
$\overline{\text{TXB}}$	O	As needed	Open	Differential signal, serial transmitter, lane A, negative data
RXB	I	As needed	Connect to GND	Differential signal, serial receiver, lane E, positive data
$\overline{\text{RXB}}$	I	As needed	Connect to GND	Differential signal, serial receiver, lane E, negative data
SD_REF_CLK	I	As needed	Connect to GND	SGMII: Single-ended 125 MHz clock/differential 125 MHz clock must be connected and the reference is 1 V. PCI Express: 100 MHz differential clock must be connected.
$\overline{\text{SD\_REF\_CLK}}$	I	As needed	Connect to GND	Differential clock input. When Single ended clock is used, leave this pin unconnected. **Note:** PCI express requires Differential clock only
SD_IMP_CAL_TX	I	As needed: Connect it to 1V	Connect to 1V	High: Fixed Impedance Low: Impedance can be calibrated
SD_IMP_CAL_RX	I	As needed: Connect it to 1V	Connect to 1V	High: Fixed Impedance Low: Impedance can be calibrated
SD_PLL_TPD	O	Open	Open	Test point
SD_PLL_TPA_ANA	O	Open	Open	

Figure 7 shows the connection diagram for the impedance calibration pins.

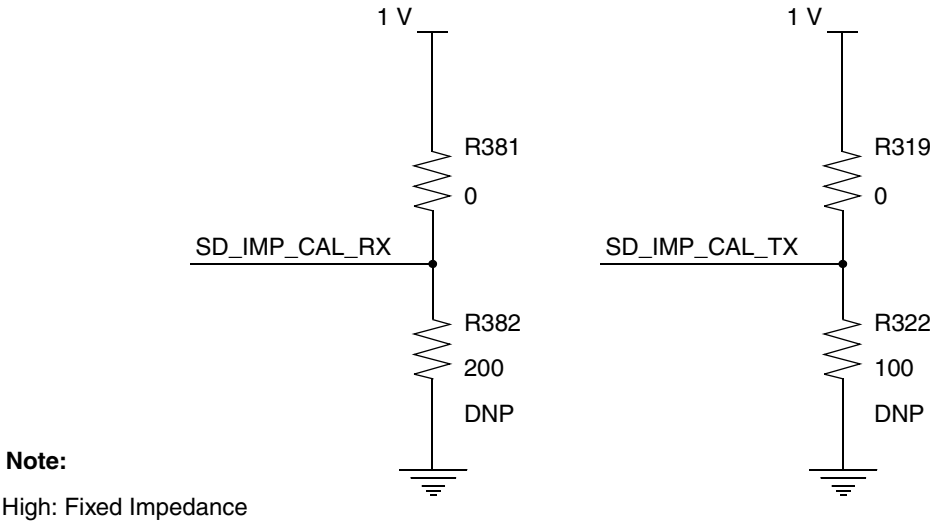

Figure 7. Connection Diagram for Impedance Calibration Pins

6.4.1 PCI Express Layout Guidelines

The PCI Express layout guidelines are described as follows:

- Recommended microstrip trace routing guidelines
  - Single ended: 50 Ohms +/– 15%
  - Differential: 100 Ohms +/– 15%
- Recommended stripline trace routing guidelines
  - Single ended: 50 Ohms +/– 15%
  - Differential: 100 Ohms +/– 15%
- Recommended length matching intra-pair: Maximum 5 mil delta, matching maintained segment to segment, and matching at point of discontinuity. However, avoid tight bends.
- Recommended length matching inter-pair: Recommended to keep differences within 3 inches to minimize latency.
- Recommended for all differential signal pairs: Maintain ≥ 20 mil trace edge to plane edge gap.
- Gnd referenced signals is recommended.
- Use Gnd stitching vias by signal layer vias for layer changes.
- Do not route over plane splits or voids. Allow no more than a half trace width routed over via antipad.
- Via usage: Limit via usage to 4 vias per TX trace and 2 vias per RX trace (6 vias total, entire path).
- Bends: Match left/right turn bends whenever possible. No 90-degree bends or tight bend structures.
- The reference clock signal pair should maintain the same reference plane for the entire routed length and should not cross any plane splits (breaks in the reference plane).
- A minimum separation from the reference clock and other traces should be maintained. Assuming a trace width of 'w', no other trace or signal should be allowed within '3w'.
- The reference clock signal pair routing length should be minimized.

- The reference clock signal pair via count should be minimized. As a rule of thumb, via count should not exceed four.
- Reference clock terminating components should be placed as close as possible to their respective devices, ideally within 100 mils of the clock/receiver component pin.
- Match all segment lengths between differential pairs along the entire length of the pair.
- Maintain constant line impedance along the routing path by keeping the same line width and line separation.
- Avoid routing differential pairs adjacent to noisy signal lines or high speed switching devices, such as clock chips.
- Keep clock lines adequately separated from I/O lines.
- Recommended PCI Express reference clock to PCI express reference clock length matching to within 25 mils.
- Unused PCI Express clock outputs (unpopulated down devices or unpopulated add-in card connectors) should be disabled to limit EMI radiations and possible signal reflections.
- Decoupling capacitors: Several PCB-mounted 0.1 to 1.0 μF capacitors should be placed near the PCI Express silicon on the sides of the package to which the PCI Express I/O buffers connect.
- AC coupling capacitors:
  - Do not use capacitor-packs (C-packs) for PCI Express AC coupling capacitor purpose.
  - The same package size and value of capacitor should be used for each signal in a differential pair.
  - Locate capacitors for coupled traces in a differential pair at the same location along the differential traces. Place them as close to each other as possible, as allowed by DFM rules.
  - The breakout into and out of the capacitor mounting pads should be symmetrical for both signal lines in a differential pair.
- Test points and probing structures should not introduce stubs on the differential pairs.

6.5 Time-Division Multiplexing (TDM) (Only in P1020)

Four to six signals are required for TDM full-duplex operation, depending on the selected operating mode (shared or independent). The function of the I/O pins for the TDM is determined by a number of control bits, and the direction of clocks and frame syncs can also be configured. Each signal pin can be configured as an input or output. The frame syncs and the clocks can be shared with the other TDM modules on-chip. Table 13 lists the TDM pins.

Table 13. Programmable Interrupt Controller Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
TDM_RCK/ IRQ06	I/O	As needed	2k–10k to OVDD	Pin functionality is determined by the PMUXCR[TDM_EN] bit settings. In shared mode, this pin can be ignored or used as GPIO.
TDM_RFS/ /GPIO3/IRQ10	I/O	As needed	2k–10k to OVDD	Pin functionality is determined by the PMUXCR[TDM_EN] bit settings. In shared mode, this pin can be ignored or used as GPIO.
TDM_RD/ GPIO4/IRQ11	I/O	As needed	2k–10k to OVDD	Pin functionality is determined by the PMUXCR[TDM_EN] bit settings.

Table 13. Programmable Interrupt Controller Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
TDM_TCK/ GPIO2/IRQ9	I/O	As needed	2k–10k to OVDD	Pin functionality is determined by the PMUXCR[TDM_EN] bit settings. In shared mode, this clock is used by both transmitter and receiver.
TDM_TFS/ /GPIO1/IRQ8	I/O	As needed	2k–10k to OVDD	Pin functionality is determined by the PMUXCR[TDM_EN] bit settings. In shared mode, this pin is used as a sync by both the transmitter and receiver.
TDM_TD/ GPIO0/IRQ7	I/O	As needed	2k–10k to OVDD	Pin functionality is determined by the PMUXCR[TDM_EN] bit settings.

6.6 DUART

The P1020/21 DUART module provides two standard UART interfaces, and any UCC from the QUICC Engine block can be programmed to function as UART. Refer to Section 6.9.4, "QUICC Engine UART." The DUART pins are multiplexed with the QUICC Engine and POR configuration pins . The registers in each UART interface are used for configuration, control, and status. The divisor latch access bit, ULCR[DLAB], is used to access the divisor latch least- and most-significant bit registers and the alternate function register. If only UARTn_SOUT and UARTn_SIN are used, $\overline{\text{UARTn\_CTS}}$ must be pulled down.

Table 14. Dual UART Pin Listing

Critical	Signal	Pin Type	Connection		Notes
			If Used	If Not Used	
	UART0_SOUT	O	As needed	Open	Pin functionality determined by SICRL[URT_CTPR] bit setting.
	UART0_SIN/ CE_PB16	I/O	As needed	2 k–10 kΩ to GND or program pin to function as a debug pin	Pin functionality determined by SICRL[URT_CTPR] bit setting.
	$\overline{\text{UART0\_CTS}}$/	I/O	As needed	2 k–10 kΩ to GND or program pin to function as a debug pin	Pin functionality determined by SICRL[URT_CTPR] bit setting If DUART1 is used, but $\overline{\text{CTS}}$ is not used, pull it down.
	$\overline{\text{UART0\_RTS}}$/	O	As needed	Open	Pin functionality determined by SICRL[URT_CTPR] bit setting. If DUART1 is used but RTS is not used, leave open.
	UART1_SOUT/ CE_PB17/cfg_core1_pll1	O	As needed	Open	Pin functionality determined by SICRL[URT_CTPR] bit setting.

Table 14. Dual UART Pin Listing (continued)

Critical	Signal	Pin Type	Connection		Notes
			If Used	If Not Used	
	UART1_SIN/CE_PB16	I/O	As needed	2 k–10 kΩ to GND or program pin to function as a debug pin	Pin functionality determined by SICRL[URT_CTPR] bit setting.
	$\overline{\text{UART1\_CTS}}$/CE_PB14	I	As needed	2 k–10 kΩ to GND or program pin to function as a debug pin	If DUART2 is used, but $\overline{\text{CTS}}$ is not used, pull it down.
	$\overline{\text{UART1\_RTS}}$/CE_PB15 /cfg_tsec3_prtcl1	O	As needed	Open	If DUART2 is used but RTS is not used, leave open.

6.7 I²C Unit

Table 15 lists the I²C pins.

Table 15. I²C Pin Listing

Signal	Pin Type	Termination		Notes
		If used	If not used	
IIC1_SCL/ $\overline{\text{CKSTOP\_IN}}$	I/O	**$\overline{\text{CKSTOP\_IN}}$:** As needed + 10 kΩ to OV_{DD} IIC1_SCL**:** As needed + 2 k-10 kΩ to OV_{DD}	**$\overline{\text{CKSTOP\_IN}}$:** 4.7 kΩ to OV_{DD} IIC1_SCL**:** 2 k–10 kΩ to OV_{DD}	Pin functionality determined by SICRL[LDP_LCS_A] bit settings.
IIC1_SDA/ $\overline{\text{CKSTOP\_OUT}}$	I/O	**$\overline{\text{CKSTOP\_OUT}}$:** As needed + 10 kΩ to OV_{DD} **Others:** As needed + 2k-10 kΩ to OV_{DD}	**$\overline{\text{CKSTOP\_OUT}}$:** Open **Others:** 2 k–10 kΩ to OV_{DD}	Pin functionality determined by SICRL[LDP_LCS_A] bit settings.

6.8 Local Bus Interface Unit

The local bus supports four chip selects: $\overline{\text{LCS}}$[0:3]. LGPL4 must be pulled high to OV_{DD} with a 1K-Ω resistor. In the normal case, when P1020/21 boots from the flash memory on the local bus, the local bus uses the GPCM machine. Under GPCM, the LGPL4 functions as $\overline{\text{LGTA}}$, which is an input. Therefore, it must be pulled high. If it is floating and drifts to low, it terminates GPCM access prematurely. The pullup also avoids the issue described in the local bus signal description table in the reference manual.

The local bus frequency can be adjusted through the LCRR[CLKDIV] register field. Therefore, the user must adjust the value of the LCRR[CLKDIV] in order to meet the local bus supported frequencies. Software should not reconfigure the local bus clock while code is executing from the local bus, but rather while code is executing from another interface, such as the DDR controller.

6.8.1 Local Bus Address

To save signals on the local bus, address and data are multiplexed onto the same 16-bit bus. An external latch is needed to demultiplex the 16-bit MSB address and, together with LA[16:25], to reconstruct the original address. No external intelligence is needed, because LALE provides the correct timing to control a standard logic latch. The LAD signals can be directly connected to the data signals of the memory/peripheral. Transactions on the local bus start with an address phase, where the LBC drives the transaction address on the LAD signals and asserts the LALE signal. This can be used to latch the address and then the LBC can continue with the data phase. Figure 8 and Figure 9 illustrate the connection of the local bus in both multiplexed and non-multiplexed address modes defined by the state of the CFG_LBIU_MUX_EN signal. For details on the operation of the local bus controller, refer to the reference manual.

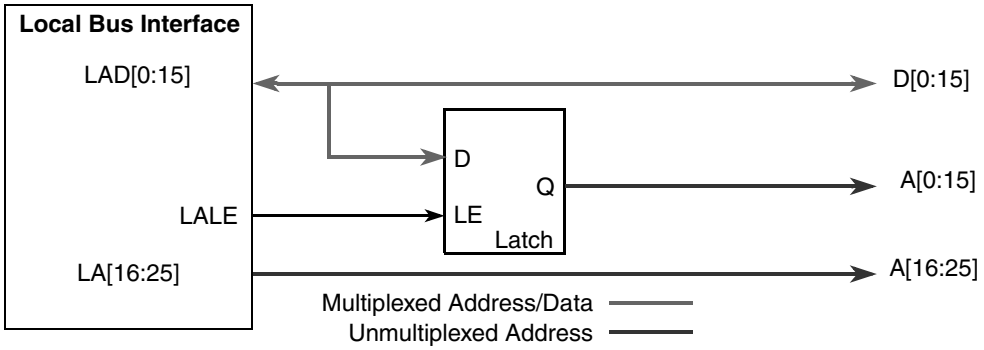

Figure 8. Local Bus Address Connection Example (Multiplexed Mode)

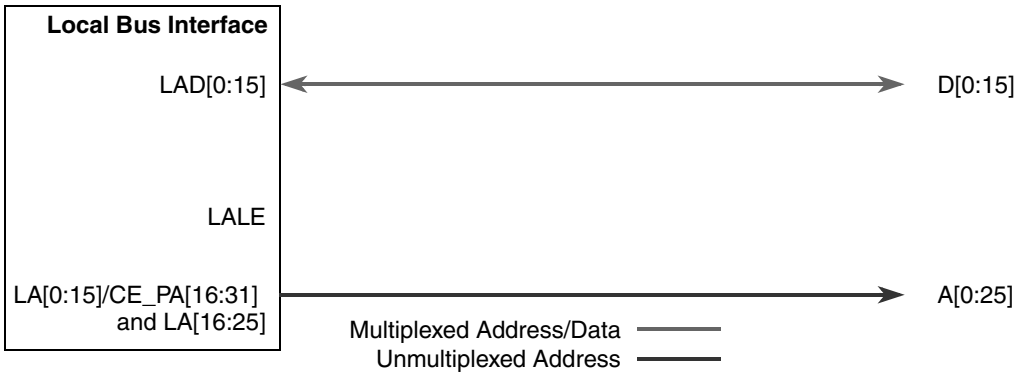

Figure 9. Unmultiplexed Address and Data Bus Connection Example

6.8.2 Connecting Devices to the Local Bus

The P1020/21 local bus features a multiplexed address and data bus, LAD[0:15]. An external latch is required to de-multiplex these signals to the connecting device. Figure 10 shows the timing of LALE. When LALE is high, it indicates LAD[0:15] is in the address phase.

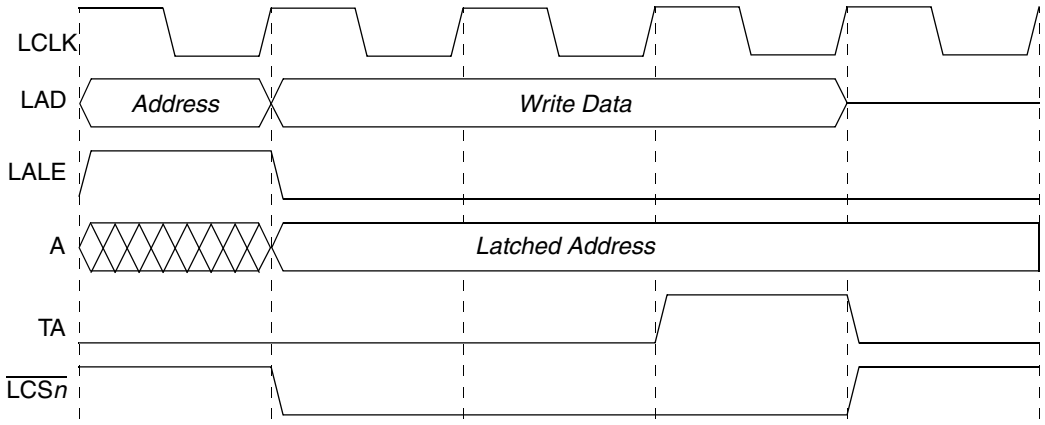

Figure 10. LALE Timing

For every assertion of $\overline{\text{LCS}}$n, LALE is asserted first. While LALE is asserted, all other control signals are negated. The duration of LALE can be programmed to 1–4 cycles in LCRR[EADC]. The default is 4 cycles. The timing of LALE negation is important to ensure the correct latch. If the change of LAD and negation of LALE are too close and the margin for the latch is not sufficient, RCWHR[LALE] can be set. LALE is negated ½ a local bus clock earlier, which should ensure enough margin. Table 16 shows the termination recommendations for the local bus pins.

Table 16. Local Bus Pin Listing

Critical	Signal	Pin Type	Connection		Notes
			If Used	If Not Used	
Local Bus Interface					
	LAD[0:15]	I/O	As needed	2 k–10 kΩ to OV_{DD}	
	LA[0:25]	O	As needed	Open	
	$\overline{\text{LCS}}$[0:3]	O	As needed	Open	
	$\overline{\text{LWE}}$[0:1]/$\overline{\text{LBS}}$[0:1]	O	As needed	Open	
	LBCTL	O	As needed	Open	
	LALE	O	As needed	Open	
X	LGPL0	I/O	As needed	Open	
X	LGPL1	I/O	As needed	Open	
	LGPL2/$\overline{\text{LOE}}$	O	As needed	Open	
X	LGPL3	I/O	As needed	Open	
	LGPL4/$\overline{\text{LGTA}}$/LUPWAIT	I/O	As needed + 1 k–10 kΩ to OV_{DD}	Open	
X	LGPL5	O	As needed	Open	
	LCLK[0:1]	O	As needed	Open	

6.9 QUICC Engine Communication Interfaces (Only in P1021)

The QUICC Engine communication interfaces include the Ethernet controller, TDM/SI,UTOPIA/POS, HDLC, BISYNC, universal asynchronous receiver/transmitter (UART), and serial peripheral interface (SPI).

6.9.1 Ethernet Controller

The interfaces of the QUICC Engine are as follows:

- Media-independent interface (MII)
- Reduced media-independent interface (RMII)

6.9.1.1 Media-Independent Interface (MII)

The P1021 supports MII Ethernet interface on UCC1 can be programmed to be an Ethernet controller. We denote UCC*n* Ethernet as Ethernet *n*. All UCC Ethernet interfaces have dedicated NMSI pins that support MII interfaces, excluding the clocking signals. The NMSI signals include:

- Enet-TXD[0:3]
- Enet-TX_EN
- Enet-TX_ER
- Enet-RXD[0:3]
- Enet-COL
- Enet-CRS
- Enet-RX_DV
- Enet-RX_ER

The P1021 MII interface clocking pins (RX_CLK and TX_CLK) are inputs. They are driven by the PHY device. The RX_CLK and TX_CLK are routed through CLKx pins that are multiplexed with other Parallel I/O Ports pin signals. See the P1021RM reference manual. For each Ethernet *n*, the RX_CLK and TX_CLK multiplexing is controlled by CMXUCRx.

Because the Ethernet pins are multiplexed with other I/O port pins, all three Ethernet interfaces can render other interfaces unusable due to pin multiplexing limitations. Therefore, you should carefully review the port tables in P1021RM reference manual before starting a new design.

6.9.1.2 RMII Interface Connection

The UCC1 and UCC5 support the RMII interface, which uses only a subset of the MII signals. The RMII signals should be connected as shown in Table 17. For RMII, the TX and RX share one clock called REF_CLK. The REF_CLK from the PHY must be connected to TX_CLK of the P1021. RX_CLK is not used.

Table 17. RMII Connection

P1021 Signals	PHY Signals
Enet-TXD[0:1]	TXD[0:1]
Enet-TX_EN	TX_EN
Enet-RXD[0:1]	RXD[0:1]
Enet-RX_ER	RX_ER
Enet-RX_DV	CRS_DV
TX_CLK	REF_CLK

6.9.2 Utopia

The P1021 supports one Utopia L2 interface. If you are familiar with the Utopia interface of the CPM in MPC82xx and MPC85xx, note that the external signal naming convention of the QUICC Engine block follows the Utopia standard. Therefore, there is different naming in master and slave modes. The naming conventions in the CPM retain the master mode signal naming for slave mode. For example, the QUICC Engine block transmit TXSOC in slave mode is named RXSOC, but the CPM transmit SOC in slave mode is named TXSOC. In the QUICC Engine block, you should connect signals between master and slave by name. In the example here, we connect the external master TXSOC with the QUICC Engine TXSOC.

6.9.3 QUICC Time-Division-Multiplexed/Serial Interface (TDM/SI)

The P1021 supports four TDMs on UCC1,UCC3,UCC5 and UCC7.The TDM can only work with an external sync and external clock; other options are not supported. The external clock and external sync need to meet the timing specifications as provided in the *P1021EC QorIQ™ Integrated Processor Hardware Specifications*.

The P1021 supports TDM in a high-speed mode. To run in this mode, the QUICC Engine platform to TDM interface frequency ratio should be 8:1, where a ratio of 400 MHz:50 MHz is recommended. The TDM maximum frequency is 50 MHz.

For the ISDN protocol, the maximum frequency supported is 25 MHz, with the condition that the QUICC Engine platform to ISDN interface frequency ratio is 16:1. For example, if the QUICC Engine platformfrequency is 400 MHz, then the ISDN interface maximum frequency is 25 MHz.

6.9.4 QUICC Engine UART

The UCC7 in the P1021 QUICC Engine block can be programmed to function as a UART controller. The QUICC Engine UART programming model is compatible with that of the CPM SCC UART. Therefore, the user may prefer to use the QUICC Engine UART to reuse existing CPM SCC UART software drivers. However, using the QUICC Engine UART consumes I/O port pins and also acts as a load for the RISC controller inside the QUICC Engine block. If you face either pin multiplexing limitation issues or QUICC Engine performance issues, you may instead decide to use the DUART interface.

6.9.4.1 UART Configuration

The pins of the QUICC Engine UART are on each UCC NMSI interface, and they are programmed through the following registers:

- CPODRx: Determines the open-drain configuration, one bit per pin.
- CPDIR1x, CPDIR2x: Determines the in/out characteristics of the pins, two bits per pin.
- CPPAR1x, CPPAR2x: Determines the functionality of each pin, two bits per pin

Refer to the parallel I/O port table of the P1021RM reference manual for details on the pin multiplexing of each UART pin. In general, the mapping for the QUICC Engine UART pins is as described in Table 18.

NOTE

The P1021, must load a RAM microcode package to use the QUICC Engine UART protocol.

Table 18. QUICC Engine UART Pin Listing

UCC No.	Signal	QE Port	Termination
UCCn (where n = 1,2,3,4, or 5)	UARTn_SOUT	SERn_TXD[0]	If QE UARTn is not used, all the pins can be programmed for other functions.
	UARTn_SIN	SERn_RXD[0]	
	UARTn_CTS	$\overline{\text{SERn\_CTS}}$	If $\overline{\text{CTS}}$ is programmed for UART function but is not connected, it must be pulled low.
	UARTn_RTS	$\overline{\text{SERn\_RTS}}$	Programming $\overline{\text{CTS}}$ for non-UART use automatically terminates the pin to low. No pulldown resistor is needed.

7 Documentation History

Table 19 provides a revision history for this application note.

Table 19. Documentation History

Revision	Release Date	Changes
A	10/02/2010	Initial release

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