XPort1002

Multi-Protocol Four Port Serial PMC Module Based on the MPC8280 PowerQUICC II™ Series

User's Manual

Revision 050621

X-ES

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Revision History

Revision	Principal Changes	Date	Board Rev.
050621	Preliminary Release	June 2005	SA

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1. Overview

The XPort1002 is a serial communications module providing up to four serial ports on a PMC module. The serial interfaces can be built to support either RS-232 or RS-485/RS-422 modes.

The serial and PCI interfaces are provided by the Motorola PowerQUICC II MPC8270 Integrated Communications Processor. The MPC8270 contains a PowerPC G2 that can be disabled featuring a built in floating point unit and MMU, with integrated 16K byte instruction and data caches.

The MPC8270 System Interface Unit (SIU) provides memory controllers supporting 4 to 16MB of external Flash and 8 to 256MB of 66Mhz SDRAM. The MPC8270 also features a built in PCI interface.

The MPC8270 Communications Processing Module (CPM) provides four Serial Communications Controllers (SCCs) and two Serial Management Controllers (SMCs), supporting a variety of synchronous and asynchronous serial communications modes. It also contains the baud rate generators, an integrated 10/100 Mbps ethernet controller and counter timers.

Board Support Packages (BSP) are available for Wind River Systems' VxWorks real-time operating system and provides the ability to support HDLC, Transparent, BI-SYNC, and UART protocols.

1.1 XPort1002 Series Features

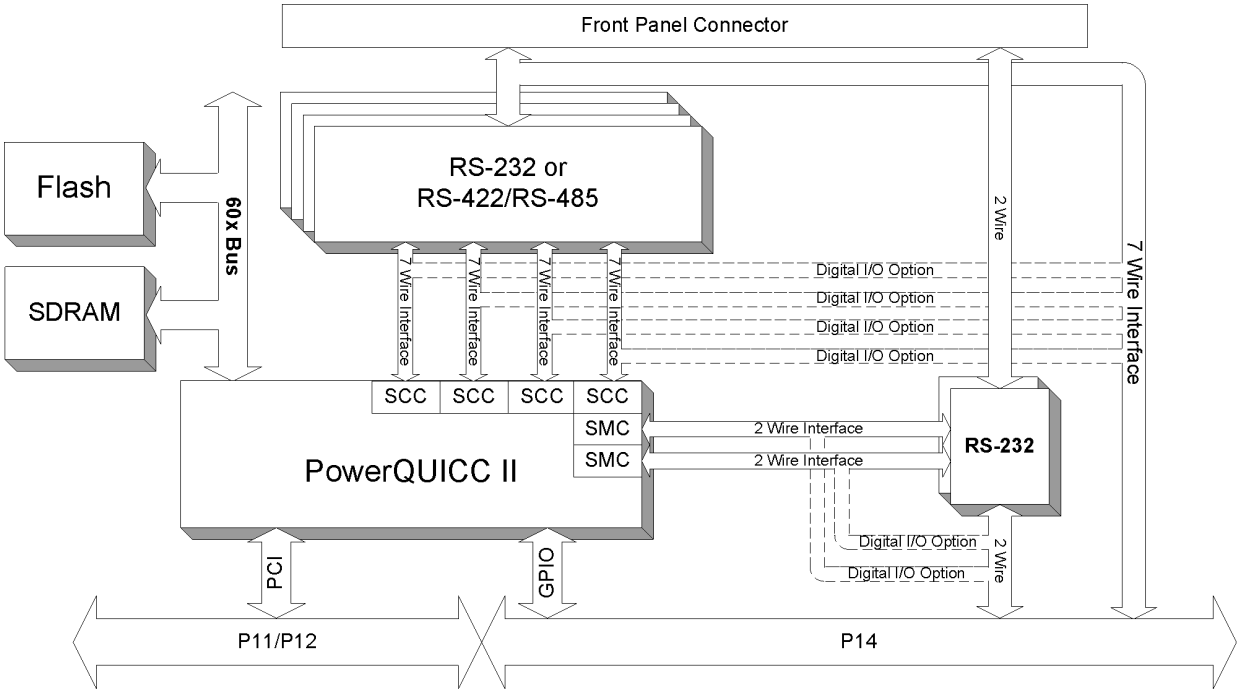
The list below is a brief description of the features the XPort1002 module provides. Refer to the specific section in the manual for additional information.

Table 1.1.1: XPort1002 Features

	XPort1002 Features
PCI Slave	The PCI slave interface provides access to MPC8270 registers, SDRAM, and flash.
PCI Master	The PCI master interface allows the MPC8270 to transfer serial data directly to and from PCI memory. Four DMA units are available allowing for data transfers in excess of 100MB/s.
Serial Communication Controller (SCC)	Four SCCs implementing independent interfaces. Each SCC independently supports UART, HDLC, BISYNC, and TRANPARENT protocols, each port implementing either a RS-232 or RS-485/RS-422 DTE seven wire serial interface. Each seven wire interface consists of data (TXD, RXD), clocks (TXC, RXC), and control signals (RTS, CTS, DCD). For added flexibility, the XPort1002 allows the Transmit Clock (TXC) to be set up as an input or to be configured as an output.
Processor	The XPort1002 can optionally be configured in core enabled mode. In this mode, the MPC8270 PowerPC G2 Core may be used operating internally at 166 to 450MHz with 16KB internal instruction and data caches. The 60x bus is a 64 bit architecture operating externally at 66MHz.
SEEPROM	16 Kb of SEEPROM is supported for storing manufacturing and application data.
RAM	The XPort supports 8, 32, 64, 128 or 256MB of SDRAM. With the Core disabled one of the SDRAMs can be used for buffer storage.
ROM	The XPort supports 4, 8, or 16MB of flash memory in addition to the 512KB of socketed flash.
Development Port	The XPort allows for the optional placement of external ethernet and serial ports for development.
RTOS and Protocols	Board Support packages for Wind River Systems VxWorks operating system. Driver level initialization, configuration and protocol support for MP8270 SCCs, SMCs, I2C and FCC.

1.2 Block Diagram

Figure 1.2.1: XPort1002 Block Diagram



1.3 Terminology / Conventions

Table 1.3.1: Terminology

Term	Definition
BD	Buffer Descriptor
byte	8 bits
CPM	Communications Processor Module
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
double long word	64 bits
DRAM	Dynamic Random Access Memory
FCC	Fast Communication Controller
HDLC	High-level Data Link Control
JTAG	Joint Test Action Group
long word	32 bits
MII	Media-independent Interface
PCI	Peripheral Component Interconnect
Rx	Receive
SCC	Serial Communications Controller
SDRAM	Synchronous Dynamic Random Access Memory
SDLC	Synchronous Data Link Control
SMC	Serial Management Controller
SRAM	Synchronous Random Access Memory
Tx	Transmit
UART	Universal Asynchronous Receiver Transmitter
word	16 bits

Table 1.3.2: Conventions

Term	Definition
0x0	This notation denotes a hexadecimal number.
0b0	This notation denotes a binary number.
Active Low Signals	Active Low Signals are listed with a # postfix. IE: RESET#

1.4 Technical Information

The technical information in this manual is intended to describe the unique features of the XPort1002. It is assumed that the reader has familiarity with the devices and interface standards incorporated into the XPort1002. This information can be found in the following manuals and specifications.

Table 1.4.1: XPort1002 Manuals/Standards Reference List

MPC8270	MPC8280 PowerQUICC II User's Manual	Motorola	MPC8280UM/D, 3/2004, Rev 0
	MPC603e RISC Microprocessor User's Manual	Motorola	MPC603EUM/AD, Q2/02, REV 3
	MPC8280 Hardware Specifications	Motorola	MPC8280EC/D; Rev. 1.0 2/2004
PCI	PCI Local Bus Specification Revision 2.2	PCI-SIG	
SP486	Quad RS-422/RS-485 Line Driver	Sipex	SP486/487 2000
SP488	Quad RS-422/RS-485 Line Receiver	Sipex	SP488/489 2000
SN75188	Quad RS-232 Line Driver	TI	SLLS094C - September 1983 - Revised May 2004
SN75189	Quad RS-232 Line Receiver	TI	SLLS095D - September 1973 - Revised October 1998
LXT971A	3.3V Dual-Speed Fast Ethernet Transceiver LXT971A, 1/1/2001 Intel	Intel	249414, Rev: 002, August 7, 2002
RS-232	Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange	ANSI/TIA/EIA	ANSI/TIA/EIA-232-F-1997
RS-422	Electrical Characteristics of Balanced Voltage Digital Interface Circuits	ANSI/TIA/EIA	ANSI/TIA/EIA-422-B-1994, Telecommunications Industry Association, 1994
RS-485	Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems	ANSI/TIA/EIA	ANSI/TIA/EIA-485-A-1998, Telecommunications Industry Association, 1998

1.5 Ordering Information

The XPort1002 offers a wide range of configuration options. Before ordering, please review the following options and specify how the XPort1002 can be configured for your application.

Table 1.5.1: XPort1002 Configuration Options

Item	Option
SDRAM	32 - 256MB
Soldered Flash	0, 4 - 16MB
I/O	Front Panel or Rear Panel, Serial I/O or Digital I/O
SCC Port 1	RS-232 or RS-485/RS-422
SCC Port 2	RS-232 or RS-485/RS-422
SCC Port 3	RS-232 or RS-485/RS-422
SCC Port 4	RS-232 or RS-485/RS-422
Custom Oscillator 1	Frequency
Custom Oscillator 2	Frequency

1.6 XPort1002 Software/Accessories

X-ES offers several software solutions for the XPort1002, listed below. Other operating systems can be supported by request, please contact X-ES sales!

Table 1.6.1: Available Software

Operating System	Description
VxWorks	VxWorks BSP
	SCC/SMC Driver
Linux	Linux LSP
	Linux Flash Kernel
	SCC/SMC Driver
Windows	SCC/SMC Driver
Other / N/A	XPort1002 xMon Monitor

The following accessories are available for the XPort1002 board. For more information on any of these items please contact X-ES.

Table 1.6.2: Available Accessories

Part Number	Description
90000030	XPort, 6’ Molded Cable, DTE
90000001-1	XPort, 6' Ribbon Cable Assembly
90000001-5	XPort, 6' Ribbon Cable Assembly, DTE
90000001-6	XPort, 6' Ribbon Cable Assembly, DTE, ETH/SMC
90000005	XPort, DTE Ribbon Cable Adaptor Module
90070050-1	XPort1002 Development/Debug module and Cable (JTAG, COP)

The following additional documentation is available for the XPort1002 board. For more information on any of these items please contact X-ES.

Table 1.6.3: Additional Documentation

Manual	Description
XPortCableds.pdf	XPort 6’ Ribbon Cable Assembly Datasheet
XPortMoldedCableds.pdf	XPort 6’ Molded DTE Cable Assembly Datasheet
xMonXPort1002tm.pdf	XPort1002 xMon Monitor Manual
sccDrv.pdf	SCC Driver Software Manual (VxWorks)
sccDrv.pdf	SCC Driver Software Manual (Linux)
sccDrv.pdf	SCC Driver Software Manual (Windows)

2. Printed Circuit Board

This chapter describes details associated with the printed circuit board. These include component maps, installation, ESD handling concerns, environmental and power requirements.

2.1 Electrostatic Discharge

When handling this product, please remember that electrostatic discharge (ESD) can easily damage the components on this module and result in board failure. Unless you ground yourself properly, static can build in your body and cause ESD damage when you touch the board. To ground yourself, wear a grounding wrist strap. Simply placing this module on a static-shielding bag offers no protection -- place it on a grounded ESD-safe mat. Do not place this board on metal or other conductive surfaces. When this board is not in use or in an enclosure, store it in either a static-shielding bag or clamshell provided.

CAUTION: Use proper ESD procedures and handle this board only when absolutely necessary. Always wear a wrist strap while handling this board. Hold this board by the edges. Do not touch any components or circuits. Store in ESD safe bag when not in use.

2.2 Physical Dimensions

Table 2.2.1: XPort1002 PCB Dimensions

Parameter	Value
Form Factor	PMC
Length	149mm
Width	74mm
Stacking Height	10mm

2.3 Front Panel

The standard XPort1002 front panel is a standard PMC front panel which brings out the 120 pin connector. Build options exist for the XPort1002 to route serial I/O to the P14 connector, negating the need for front panel connector placement.

The front panel diagram is included below.

Figure 2.3.1: Front Panel Diagram

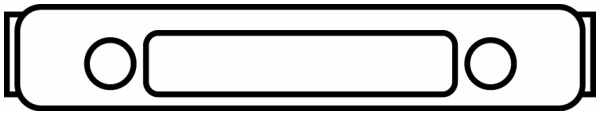
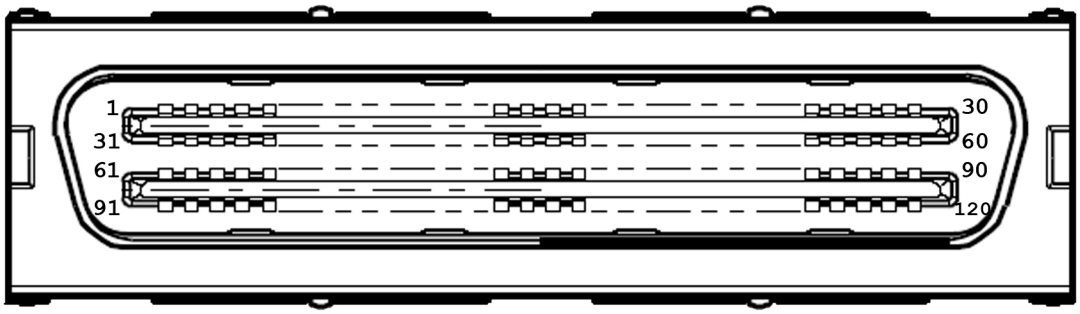


Figure 2.3.2: Front Panel Connector Detail



2.4 Component Maps

Figure 2.4.1: Component Map Front

Figure 2.4.2: Component Map Back

2.5 Connectors

The XPort1002 board has the following connectors:

Reference Designator	Description
P11	PMC connector. See Table 4.5, “Pin Assignments,” on page 4-5 for pinout.
P12	PMC connector. See Table 4.5, “Pin Assignments,” on page 4-5 for pinout.
P14	PMC connector. See Table 4.5, “Pin Assignments,” on page 4-5 for pinout.
P1000	Front Panel Serial connector. See “Serial Cables” on page 6-7 for pinout.
J350	Optional Debug module connector. See Table 5.6.1, “Development/ Debug Header Pinout,” on page 5-4 for pinout.

2.6 Jumpers

The XPort1002 has eight configuration jumpers. Each jumper is described in the table below.

Reference Designator	Description
J1000	Port 1 TXC+ Routing Select jumper. Pins 1,2: TXC+ input Pins 2,3: TXC+ output
J1001	Port 1 TXC- Routing Select jumper. Pins 1,2: TXC- input Pins 2,3: TXC- output
J1002	Port 2 TXC+ Routing Select jumper. Pins 1,2: TXC+ input Pins 2,3: TXC+ output
J1003	Port 2 TXC- Routing Select jumper. Pins 1,2: TXC- input Pins 2,3: TXC- output
J1004	Port 3 TXC+ Routing Select jumper. Pins 1,2: TXC+ input Pins 2,3: TXC+ output
J1005	Port 3 TXC- Routing Select jumper. Pins 1,2: TXC- input Pins 2,3: TXC- output
J1006	Port 4 TXC+ Routing Select jumper. Pins 1,2: TXC+ input Pins 2,3: TXC+ output
J1007	Port 4 TXC- Routing Select jumper. Pins 1,2: TXC- input Pins 2,3: TXC- output

The following diagrams illustrate how the jumpers are set to route TXC as either an input or an output

Figure 2.6.1: TXC Input Jumper Settings

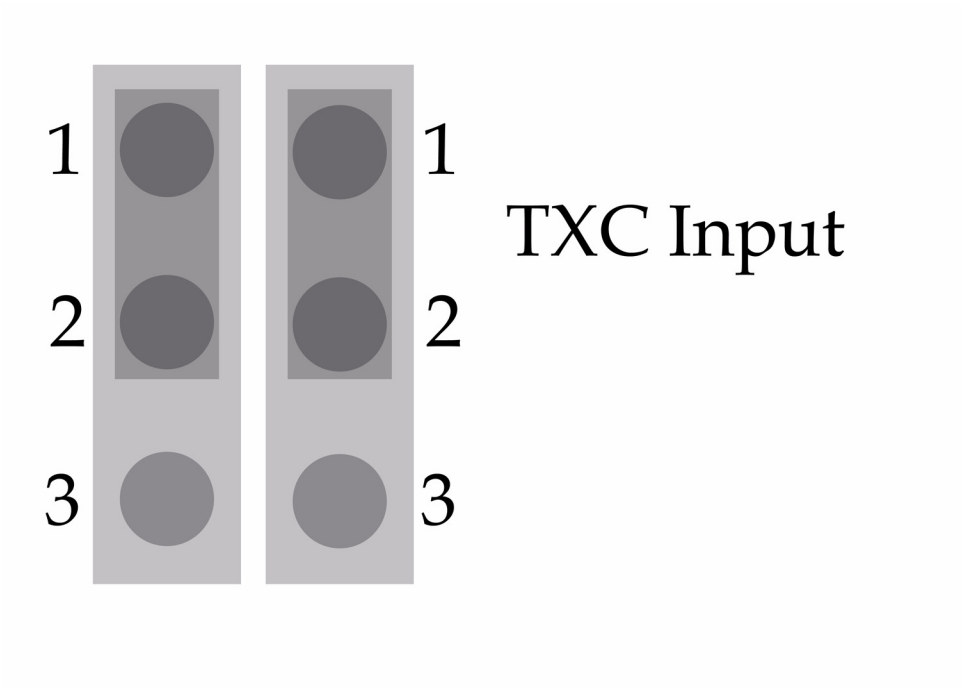
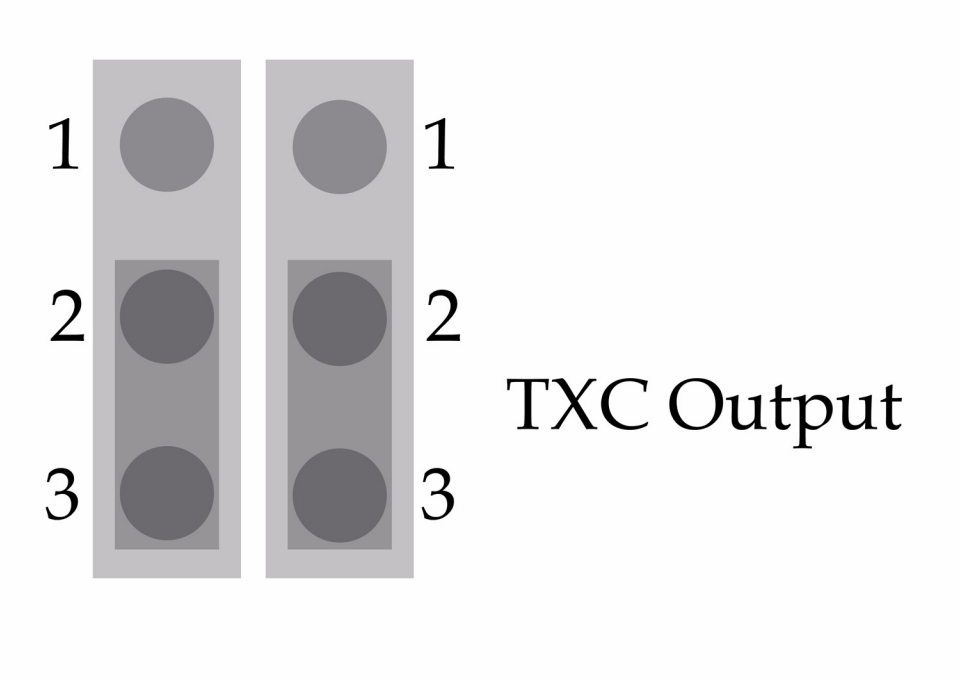


Figure 2.6.2: TXC Output Jumper Settings



2.7 LED Indicators

The XPort1002 has four green LED's on the rear of the board. They are described in the table below.

Reference Designator	Description
D700	General Purpose LED controlled by MPC8270 GPIO pin.
D701	General Purpose LED controlled by MPC8270 GPIO pin.
D702	General Purpose LED controlled by MPC8270 GPIO pin.
D703	General Purpose LED controlled by MPC8270 GPIO pin.

2.8 Typical Power Requirements

Voltage	Current (A)	Power (W)
+3.3 V	TBD	TBD
+5.0 V	TBD	TBD
+12.0 V	TBD	TBD
-12.0 V	TBD	TBD

2.9 Environmental Requirements

The XPort1002 is available in both a commercial and extended temperature variant. The following table describes the temperature and humidity requirements of each variant.

Name	Variant	Requirement	Relative Humidity
Operating Temperature	Commercial	0 to +55 Celsius, ambient	0 - 85% (non-condensing)
Operating Temperature	Extended	-40 to +85 Celsius, ambient	0 - 85% (non-condensing)
Storage Temperature	Commercial	-40 to +70 Celsius	0 - 95% (non-condensing)
Storage Temperature	Extended	-40 to +85 Celsius	0 - 95% (non-condensing)

3. Setup & Troubleshooting

This chapter describes the setup process and how to check for proper operation once the board has been installed. The chapter also includes troubleshooting, service, and warranty information.

3.1 Electrostatic Discharge

When handling this product, please remember that electrostatic discharge (ESD) can easily damage the components on this module and result in board failure. Unless you ground yourself properly, static can build in your body and cause ESD damage when you touch the board. To ground yourself, wear a grounding wrist strap. Simply placing this module on a static-shielding bag offers no protection -- place it on a grounded ESD-safe mat. Do not place this board on metal or other conductive surfaces. When this board is not in use or in an enclosure, store it in either a static-shielding bag or clamshell provided.

CAUTION: Use proper ESD procedures and handle this board only when absolutely necessary. Always wear a wrist strap while handling this board. Hold this board by the edges. Do not touch any components or circuits. Store in ESD safe bag when not in use.

3.2 Setup

You need the following items to set up and check the operation of the XPort1002. Items in bold are supplied by or optionally available from X-ES.

Table 3.2.1: Setup Requirements

	Pre-Startup Checklist
❑	**XPort1002 module**
❑	Compatible baseboard host
❑	Chassis and/or Power supply
❑	**XPort Series Serial Cable (optional)**
❑	**SCC Driver software (optional)**
❑	Terminal

3.3 Check Power Supply

Verify that your power supply or host module is sufficient for the board. See “Typical Power Requirements” on page 2-7 for the XPort1002 module’s power requirements.

3.4 Installation / Removal

XPort1002 is a PMC module. It can be inserted into and removed from a CompactPCI carrier card. The process for installing and removing XPort1002 is indicated in the following diagram.

CAUTION: To avoid damaging the module and/or baseboard, do not force the module onto the baseboard.

Figure 3.4.1: Installation for PMC Module

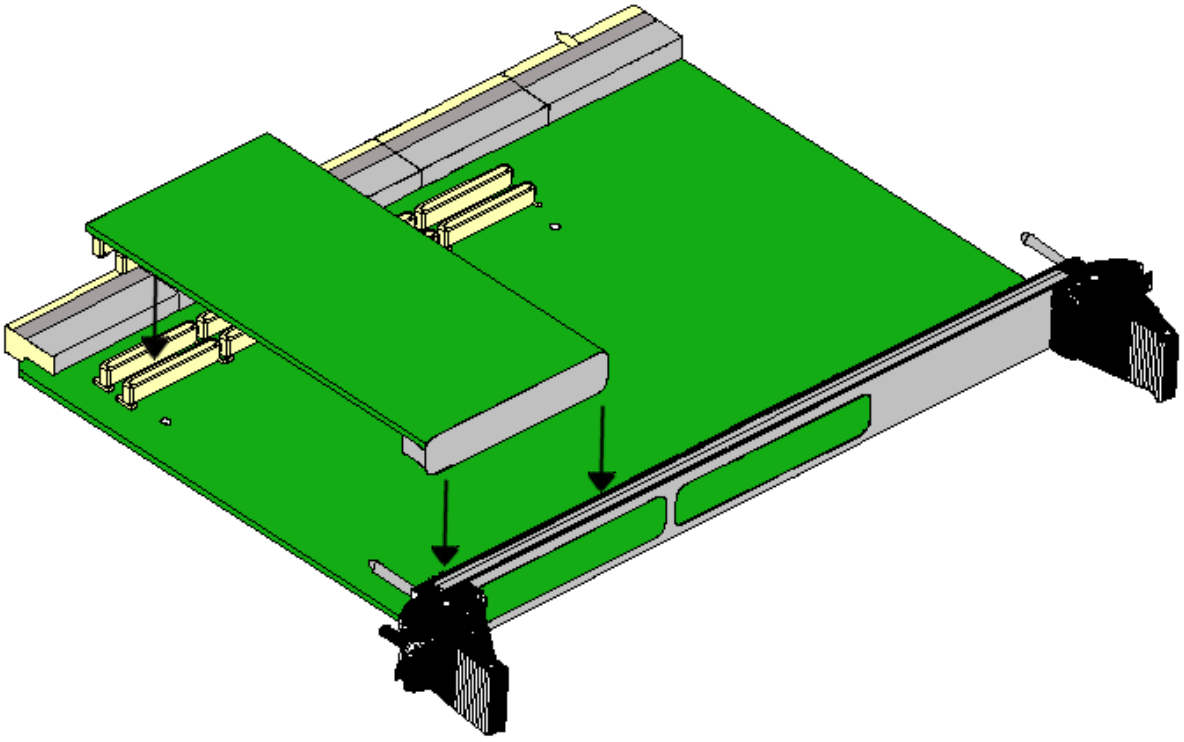


Table 3.4.2: Installation Procedure

Step	Procedure
1	Operator gently inserts XPort1002 front panel into CompactPCI carrier card front panel PMC slot.
2	Operator fully seats XPort1002 PMC connectors into CompactPCI carrier card PMC site
3	Operator may now install and power up the CompactPCI carrier card with XPort1002 module installed, following any installation instructions of the carrier card manufacturer.

Table 3.4.3: Removal Procedure

Step	Procedure
1	Remove CompactPCI carrier card with XPort1002 module from chassis, following manufacturer removal instructions.
2	Operator gently unseats XPort1002 PMC connectors from CompactPCI carrier card PMC site.
3	Operator removes XPort1002 front panel from CompactPCI carrier card's front panel. XPort1002 module is now removed from system.

3.5 Troubleshooting

In case of difficulty, use this checklist:

Table 3.5.1: Troubleshooting Checklist

	Troubleshooting Checklist
❑	Be sure the XPort1002 is fully seated into the baseboard.
❑	Be sure the system is not overheating
❑	Check the cables and connectors to be certain they are secure.
❑	If you are using the XPort1002 xMon, check that your terminal is connected to SMC1 and verify that the baud rate is set to 9600.
❑	If you are using the XPort1002 xMon, check the results of the power on self-test (POST). Check the SMC1 serial output. See XPort1002 xMon manual for more details.
❑	Check your power supply for proper DC voltages. If possible, use an oscilloscope to look for excessive power supply ripple or noise. On the back of the XPort1002 PCB are labeled test points for each of the card voltages.

3.6 Technical Support

If you have verified the above items, send an email to support@xes-inc.com (or call 1-608-833-1155) and ask for technical support from our support system. Please have the following information handy:

- XPort1002 board serial number
- Baseboard model number
- Operating System and version
- SCC Driver Software version (if applicable)
- xMon monitor version (if applicable)
- Any custom modifications to your board

To determine the serial number of your board, look for the white sticker attached to the PCB.

3.7 Service Information

If you plan to return the board to X-ES for service, send an email to support@xes-inc.com (or call 1-608-833-1155) and ask for a Return Merchandise Authorization (RMA) number. We will ask which items you are returning, the board serial numbers, reason for return, plus your purchase order number. If you are returning hardware that is out of warranty, we will require billing information as well. Contact us at support@xes-inc.com for any warranty questions. When returning any product, be sure to enclose it in an anti-static bag or clamshell, such as the original shipping material. Send it pre-paid to:

Extreme Engineering Solutions, Inc.
3225 Deming Way, Suite 120
Middleton, WI 53562

RMA#_____

Our service department cannot accept material returned without an RMA number.

4. PCI Interface

XPort1002 is a PrPMC module that conforms to the PMC interface specification, which is based on the PCI bus interface standard.

The PCI Standard defines the electrical characteristics of the interface. The XPort module provides a PCI compliant slave interface, allowing for direct memory accesses from the host board to the XPort module. The XPort module also provides a PCI compliant master interface that allows the XPort module to transfer data to/from host memory. Four PCI DMA units provide for efficient PCI memory access for buffer transfers.

The PCI 2.2 compliant interface is implemented using the MPC8270's integrated PCI interface controller, which acts a bridge to the MPC8270's internal registers and to the MPC8270's 60x bus.

4.1 PCI Signals

The following signals are available on the PMC connector. For details, refer to the PCI specification.

Signal	Signal Description
AD[31:0]	PCI ADDRESS/DATA BUS. The PCI address/data bus consists of 32 signals that are used as inputs and outputs for address and data handling.
C/BE[3:0]#	COMMAND/BYTE ENABLE. During the address phase, the command/byte enable signals define bus commands and signify which byte lanes are carrying meaningful data.
CLK	CLOCK. The clock signal is an input which provides timing for all PCI transactions.
DEVSEL#	DEVICE SELECT. Device select indicates that a device on the bus has decoded the current address and has been selected as the target of the access.
FRAME#	FRAME. The frame signal indicates the initiation and final data phase of a bus transaction.
GNT#	GRANT. Grant indicates that an agent has been granted control of the PCI bus.
IDSEL	INITIALIZATION DEVICE SELECT. An input signal acting as a chip select during configuration read and write transactions.
IRDY#	INITIATOR READY. The initiator ready signal indicates that this PCI controller, acting as a PCI master, can complete the current data phase of a PCI transaction.
LOCK#	LOCK. This signal indicates that an atomic operation to a bridge may require multiple transactions to complete.

Signal	Signal Description
M66EN	ENABLE 66 MHZ. This enable signal indicates to other devices that the bus is either running at 66 or 33 MHz.
PAR	PARITY. The PCI parity signal indicates odd parity across AD[31:0] and C/BE[3:0] when asserted during address and data phases.
PERR#	PARITY ERROR. The PCI parity error signal is asserted when a parity error is detected on the bus.
PRESENT#	PRESENT. Indicates to the host, when grounded, that the module is installed.
REQ#	REQUEST. Request indicates that an agent is requesting control of the PCI bus to perform a transaction.
SERR#	SYSTEM ERROR. The system error signal indicates that an address parity error, a target-abort, or some other system error has occurred.
STOP#	STOP. The stop signal requests that the initiator stop the current transaction.
TRDY#	TARGET READY. Indicates that the target can complete the current data phase of a PCI transaction.

4.2 Configuration space

The PCI interface's configuration space defines a standard programming model for configuring PCI devices. The configuration space registers are implemented by the MPC8270's PCI controller and conform to PCI version 2.2. The following table illustrates the configuration space as defined by the PCI bus specification.

Table 4.2.1: PCI Configuration Registers

Index	31 21	23 16	15 8	7 0
0	Device ID (0x18C0)		Vendor ID (0x1057)	
4	Status		Command	
8	Class Code (0x0E)	Subclass Code (0x00)	Standard Programming (0x01)	Revision ID
C	BIST Control	Header Type	Latency Timer	Cache Line Size
10	PIMMR Base Address Register			
14				
1C	SDRAM Base Address Register			
20	Reserved			
24	Reserved			
28	Reserved			
2C	Subsystem ID (0x1002)		Subsystem Vendor ID (0x0000)	
30	Reserved			
34	Reserved			
38	Reserved			
3C	MAX LAT	MIN GNT	Interrupt Pin	Interrupt Line
40	Reserved			
44	PCI Arbiter Control		PCI Function	
48		Host Swap CSR		Hot Swap Cap. ID

The PMC interface's IDSEL pin is used for the host to assign a specific address line to the module's interface. Refer to the host board's manual for the configuration register locations.

There are three base address registers used by the XPort module. The base address at offset 0x10 defines a window to the MPC8270's internal registers and dual port memory. The base address at offset 0x14 defines a window to the local devices and XPort1002 control registers. The base address register at offset 0x18 defines a window into the MPC8270's SDRAM memory. The size of the window is dependent on the size of the SDRAM.

4.3 Interrupts

XPort1002 is capable of receiving interrupts on pins INTA#, INTB#, INTC# and INTD# and is capable of generating interrupts on INTA#. The interrupt registers are used to select which interrupt pin the XPort uses.

4.4 Memory Map

XPort1002 maps memory and registers to PCI memory space via two independent base address registers. Note, these address ranges are configurable and the location of each BAR is likely to be remapped by the host system's PCI enumeration software.

Table 4.4.1: BAR 2 Memory Map

Address Range	Device
0x0000,0000 - 0x0080,0000 (8MB) 0x0000,0000 - 0x0200,0000 (32MB) 0x0000,0000 - 0x0400,0000 (64MB) 0x0000,0000 - 0x0800,0000 (128MB) 0x0000,0000 - 0x1000,0000 (256MB)	SDRAM

4.5 Pin Assignments

Table 4.5.1: PMC Connector Pin Assignments

Pin	P11	P12	Pin	P11	P12
1	-	+12V	2	-12V	GROUND
3	GROUND	-	4	INTA*	-
5	INTB*	-	6	INTC*	GROUND
7	PRESENT*	GROUND	8	+5V	-
9	INTD*	-	10	-	-
11	GROUND	PUP	12	-	+3.3V
13	CLK	RST*	14	GROUND	PDN
15	GROUND	+3.3V	16	GNT*	PDN
17	REQ*	-	18	+5V	GROUND
19	-	AD30	20	AD31	AD29
21	AD28	GROUND	22	AD27	AD26
23	AD25	AD24	24	GROUND	+3.3V
25	GROUND	IDSEL	26	C/BE3*	AD23
27	AD22	+3.3V	28	AD21	AD20
29	AD19	AD18	30	+5V	GROUND
31	-	AD16	32	AD17	C/BE2*
33	FRAME*	GROUND	34	GROUND	-
35	GROUND	TRDY*	36	IRDY*	+3.3V
37	DEVSEL*	GROUND	38	+5V	STOP*
39	GROUND	PERR*	40	LOCK*	GROUND
41	-	+3.3V	42	-	SERR*
43	PAR	C/BE1*	44	GROUND	GROUND
45	-	AD14	46	AD15	AD13
47	AD12	M66EN	48	AD11	AD10
49	AD9	AD8	50	+5V	+3.3V
51	GROUND	AD7	52	C/BE0*	-
53	AD6	+3.3V	54	AD5	-
55	AD4	-	56	GROUND	GROUND
57	-	-	58	AD3	EREADY
59	AD02	GROUND	60	AD1	RESETOUT*
61	AD0	ACK64*	62	+5V	+3.3V
63	GROUND	GROUND	64	REQ64*	MONARCH*

Table 4.5.2: PMC P14 Connector Pin Assignment

Pin	P14	Pin	P14
1	TXD_RXD1-	2	TXD_RXD1+
3	TXC_RXC1+	4	RXD_TXD1+
5	RXD_TXD1-	6	RTS_CTS1+
7	RXC_AC1+	8	CTS_RTS1+
9	TXC_RXC1-	10	DCD_DCD1-
11	RTS_CTS1-	12	GND
13	RXC_AC1-	14	DCD_DCD1+
15	CTS_RTS1-	16	TXD_RXD2-
17	TXD_RXD2+	18	TXC_RXC2+
19	RXD_TXD2+	20	RXD_TXD2-
21	RTS_CTS2+	22	RXC_AC2+
23	CTS_RTS2+	24	TXC_RXC2-
25	DCD_DCD2-	26	RTS_CTS2-
27	SMC_TXD1 / GND	28	RXC_AC2-
29	DCD_DCD2+	30	CTS_RTS2-
31	TXD_RXD3-	32	TXD_RXD3+
33	TXC_RXC3+	34	RXD_TXD3+
35	RXD_TXD3-	36	RTS_CTS3+
37	RXC_AC3+	38	CTS_RTS3+
39	TXC_RXC3-	40	DCD_DCD3-
41	RTS_CTS3-	42	GND
43	RXC_AC3-	44	DCD_DCD3+
45	CTS_RTS3-	46	TXD_RXD4-
47	TXD_RXD4+	48	TXC_RXC4+
49	RXD_TXD4+	50	RXD_TXD4-
51	RTS_CTS4+	52	RXC_AC4+
53	CTS_RTS4+	54	TXC_RXC4-
55	DCD_DCD4-	56	RTS_CTS4-
57	SMC_RXD4 / GND	58	RXC_AC4-
59	DCD_DCD4+	60	CTS_RTS4-
61	ETH_TX_POS / SMC_TXD1	62	ETH_RX_POS / SMC_RXD1
63	ETH_TX_NEG / SMC_TXD2	64	ETH_RX_NEG / SMC_RXD2

5. MPC8270 Processor

This chapter describes details the MPC8270's embedded G2 PowerPC microprocessor core. This includes flash and SDRAM memories, exception processing, interrupts and local service registers used to support the MPC8270.

The integrated G2 microprocessor operates at up to 450MHz. At 450MHz, the G2 Core delivers 855 Dhrystones MIPS.

The MPC8270 implements bus timers, counter timers, memory controllers, parallel buses and serial controllers, none of which are described in this chapter. For details on these features, refer to the MPC8270 User's Manual.

5.1 Configuration Options

By default, the XPort1002 is built with the on board processor core disabled. The XPort1002 may also be ordered configured in core enabled mode. Please contact X-ES for more information.

5.2 Memory Map

The XPort1002 memory map is dependent on the state of the MPC8270. The table below defines the memory map as seen from the MPC8270 while in core enabled operation.

Table 5.2.1: Memory Map (Core Enabled Mode)

Start Address	End Address	Device
0xF800,0000	0xFFFF,FFFF	Boot Flash
0xF000,0000	0xF7FF,FFFF	Storage Flash
0xEFF0,0000	0xEFFF,FFFF	MPC82xx Internal Registers
0xE000,0000	0xE7FF,FFFF	PCI I/O Space
0x4000,0000	0xDFFF,FFFF	PCI Memory Space
0x0000,0000	0x07FF,FFFF	SDRAM

5.3 Flash Memory

XPort1002 supports up to 16MB of surface mount flash memory and 512KB of socketed flash memory. The following table gives the peripherals assigned to the chip selects provided by the MPC8270.

Table 5.3.1: Device Chip Select Assignment

Chip Select	Width	Peripheral Device
Device 0	8 bit	Socketed Flash (Read Only)
Device 1	8 bit	Surface Mount Flash

Table 5.3.2: Flash Memory Map

Address	Device
0xFFF8,0000 - 0xFFFF,FFFF	Socketed Flash
0xFE00,0000 - 0xFEFF,FFFF	Surface Mount Flash

5.3.3: Boot Flash

The socketed boot flash device on chip select 0 is used by the XPort1002 as the boot device. The MPC8270 processor uses this flash to load its hardware configuration word in both core enabled and core disabled modes. In core disabled mode, this flash is also used to store the PCI hardware configuration information for the CP Auto Load.

Because of its importance to the correct operation of the XPort1002, this flash is by default factory configured to be read-only. Build options exist to make this flash writable, please contact X-ES for more information.

The following table describes how the boot flash is configured.

Table 5.3.3.1: Boot Flash Memory Map

Address	Function
TBD	TBD

5.4 SDRAM Memory

The XPort supports up to 256MB of SDRAM. The SDRAM spans range appropriate for the memory installed starting at the base of the CPU memory map (0000,0000H). The memory size can be determined by reading the Mod Conf Register. The SDRAM is organized as one bank of 4Mx64 bits to 32Mx64 bits. The SDRAM memory range for each memory size is illustrated in the table below.

Table 5.4.1: XPort1002 SDRAM Memory Map

Memory Size	Memory Address Range
0MB	-
8MB	0000,0000H to 0080,0000H
32MB	0000,0000H to 0200,0000H
64MB	0000,0000H to 0400,0000H
128MB	0000,0000H to 0800,0000H
256MB	0000,0000H to 1000,0000H

5.5 Exception Handling

The MPC8270's exception table is located in the first 8KB of SDRAM. The details of the exception table can be found in the MPC8270 User's Manual.

5.6 Development Module Header

The following table gives the pinout of the 30 pin development/debug module header on the XPort1002 module. This header gives access to an RS232 debug port, an ethernet port, COP development header, and the PLD JTAG port.

This header is optional and may not be present on all XPort1002 modules. For information about the XPort1002 Development/Debug module, contact X-ES at sales@xes-inc.com or 608-833-1155 for the XPort1002 Development/Debug Module Datasheet.

Table 5.6.1: Development/Debug Header Pinout

Pin	Signal Name	Pin	Signal Name
1	TBD	16	TBD
2		17	
3		18	
4		19	
5		20	
6		21	
7		22	
8		23	
9		24	
10		25	
11		26	
12		27	
13		28	
14		29	
15		30	

5.7 Software Configuration

5.7.1: Hardware Configuration Word

During a hardware reset, the MPC8270 reads the Hardware Configuration Word from the on card boot flash.

Table 5.7.1.1: Hardware Configuration Word

Core Enabled	Core Disabled
0x04840600	0x24840620

5.7.2: Core Disabled Configuration

When the core is disabled, the follow configuration information is read from the boot flash.

Table 5.7.2.1: Core disabled configuration

Register	Address	Value	Description
SYPCR	0xF0010004	0xF3FFFFFF	Clear software watchdog timer
PITAR0	0xF00108E8	0x000E8000	Write PITAR0
PICMR0	0xF00108F8	0x000FFFFF	Write PICMR0
PITAR1	0xF00108D0	0x000F0000	Write PITAR1
PICMR1	0xF00108E0	0x000FFF00	Write PICMR1
Config Address	0xF0010900	0x80000044	Write the address for a config cycle
Config Data	0xF0010904	0x80000001	Write config cycle data

5.7.3: Hardware Interface programming

The following table describes the programming of chip selects and other hardware interface registers.

Table 5.7.3.1: Hardware Interface Registers

Register	Offset	Value	Description
BR0	0x10100	0xF8000901	Boot Flash Base Register
OR0	0x10104	0xF80008A6	Boot Flash Option Register
BR1	0x10108	0x00000041	SDRAM Base Register
OR1	0x1010C	0xF0002EC0	SDRAM Option Register
BR2	0x10110	0xF0000901	Storage Flash Base Register
OR2	0x10114	0xF80008A6	Storage Flash Option Register
PSDMR	0x10190	0x8149C072	60x SDRAM Mode Register
MPTPR	0x10184	0x4000	Memory Refresh Timer Prescalar Register
PSRT	0x1019C	0x0010	60x-Bus Assigned SDRAM Refresh Timer
SYPCR	0x10004	0xFFFFFFC0	System Protection Control Register
TESCR1	0x10044	0x00004000	60x Bus Transfer Error Status and Control Register 1
L_TESCR1	0x10048	0x00004000	Local Bus Transfer Error Status and Control Register

6. Serial Interface

This chapter describes details of the SCC and SMC serial interfaces, which are routed between the MPC8270 and the front panel connector. Each SCC Port can be independently configured in either RS-232 or RS-485/RS-422 serial modes. Each SCC is capable of supporting synchronous and asynchronous protocols such as UART, HDLC, BISYNC and transparent modes. Eight on board baud rate generators are available to provide eight unique baud rates that can be changed during operation for each SCC transmitter and receiver.

Build options exist to support operating the baud rate generators from an external oscillator for precision frequencies.

6.1 SCC Interfaces

The XPort1002 provides four SCC interfaces each capable of acting as a DTE supporting RS-232 or RS-485/RS-422 modes. The performance of the SCC ports is dependent upon the interface mode selected, the protocol of the SCC, and the cable.

6.1.1: Seven Wire Interface

Each XPort1002 SCC interface is routed as a seven wire interface consisting essential data, control signals, and clocks. The following table describes the seven wire signal set:

Table 6.1.1.1: Seven Wire Interface Description

Signal	Description
TXD	Transmit Data
RXD	Receive Data
RTS	Request To Send
CTS	Clear To Send
DCD	Data Carrier Detect
TXC	Transmit Clock
RXC	Receive Clock

6.1.2: Physical Interface Support

The XPort1002 supports several serial physical interface modes. Each of the four SCC interfaces can be independently configured as either an RS-232 or RS-485/RS-422 DTE port. In addition, the XPort1002 may be configured to bypass the physical interface and route each of the SCC interfaces digital I/O to either the P14 or front panel connector.

The XPort1002 is available in several standard build configurations, or with a custom configuration to fit your application. When ordering the XPort1002, please specify what physical interface your application requires for each port.

See (Ordering Instructions) for more details.

6.1.3: Serial Protocol Support

Each of the four SCC ports can be independently configured to support UART, HDLC, BISYNC, or Transparent protocol modes.

6.1.4: MPC8270 Parallel Port Pin Usage

The MPC8270 provides serial port support through four parallel ports, which must be programmed according to how each port is to be used. The following table illustrates where each SCC port is connected to the MPC8270 and the direction of the signal.

Table 6.1.4.1: MPC8270 SCC DTE Port Connections

Serial Function	SCC1 Port Usage	SCC2 Port Usage	SCC3 Port Usage	SCC4 Port Usage	Direction
TXD	PD30/ SCC1:TXD	PD27/ SCC2:TXD	PD24/ SCC3TXD	PD21/ SCC4:TXD	OUTPUT
RXD	PD31/ SCC1:RXD	PD28/ SCC2:RXD	PD25/ SCC3:RXD	PD22/ SCC4:RXD	INPUT
RTS	PD29/ SCC1:RTS	PD26/ SCC2:RTS	PD23/ SCC3:RTS	PD20/ SCC4:RTS	OUTPUT
CTS	PC15/ SCC1:CTS	PC13/ SCC2:CTS	PC11/ SCC3:CTS	PC9/ SCC4:CTS	INPUT
DCD	PC14/ SCC1:CD	PC12/ SCC2:CD	PC10/ SCC3:CD	PC8/ SCC4:CD	INPUT
TXC	PC21/CLK11	PC29/CLK3	PC27/CLK5	PC25/CLK7	INPUT
	PC31/BRG1	PC29/BRG2	PC27/BRG3	PC25/BRG4	OUTPUT
RXC	PC20/CLK12	PC28/CLK4	PC26/CLK6	PC24/CLK8	INPUT

Table 6.1.4.2: DTE Serial Signal Description

Mnemonic	Circuit Name	Description	DTE Direction
TXD	Transmit Data	Data sent by DTE	OUT
RXD	Receive Data	Data received by DTE	IN
RTS	Request to Send	DTE Ready to Transmit	OUT
CTS	Clear to Send	DCE Ready to Receive	IN
DCD	Data Carrier Detect	DCE received a basic carrier signal	IN
TXC	Transmit Clock Reference	DTE transmission timing signal	IN (OUT)
RXC	Receive Clock Reference	DTE receive timing signal	IN

6.1.5: Clock Routing

The XPort1002 module has multiple clocking options for maximum flexibility. Clock generation is done internally using the PowerQUICC II's internal BRG's and is based on the XPort's carrier's PCI clock (which might not be exactly 33.333MHz). Due to this, one or two oscillators can be placed on XPort1002. Baud rate generation is still done internally, but due to MPC8270 pin multiplexing clock routing must be done by the PLD. These external oscillators are only necessary when a precise clock is needed, when a system may have different PCI clock rates, or when a specific baudrate is required.

As a standard DTE mode device, the XPort1002 accepts both a transmit clock and a receive clock from the serial interface. For maximum flexibility, the XPort1002 provides options for both transmit clock and receive clock routing. The transmit clock may be configured as an output, driven from an on board BRG. In addition, the receive clock may be echoed back as the transmit clock and used as the transmit clock.

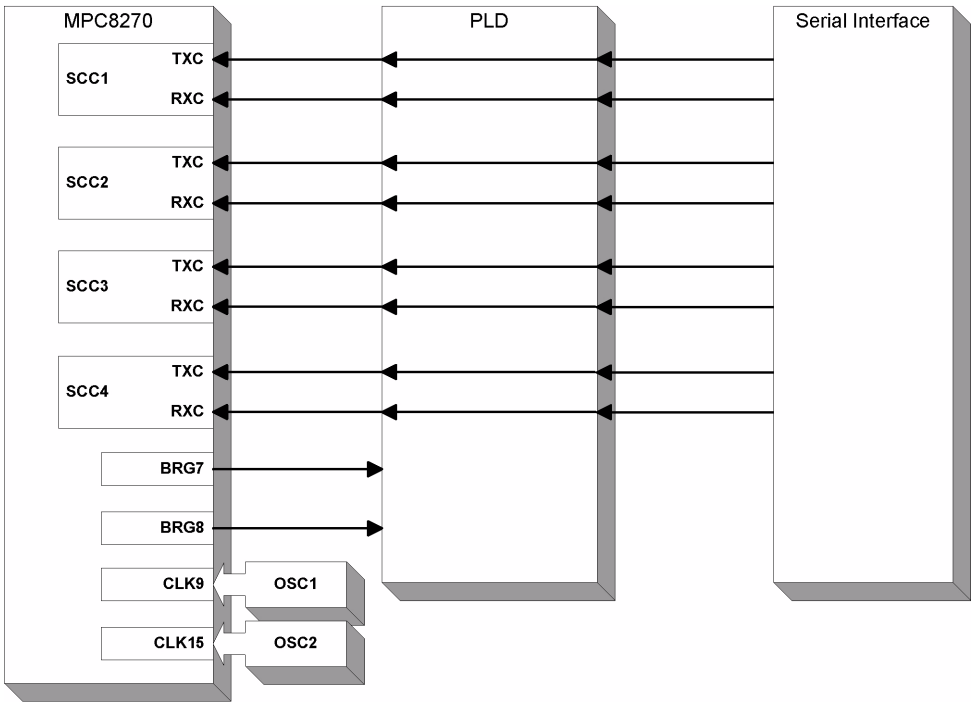
Clock routing is configured using the on board PLD drive by MPC8270 general purpose I/O pins. The table below describes the MPC8270 general purpose I/O pins used by the clock routing logic and how each pin functions.

Table 6.1.5.1: PLD General Purpose I/O Usage

MPC8270 Pin	PLD Pin	Function
TBD	TBD	TBD

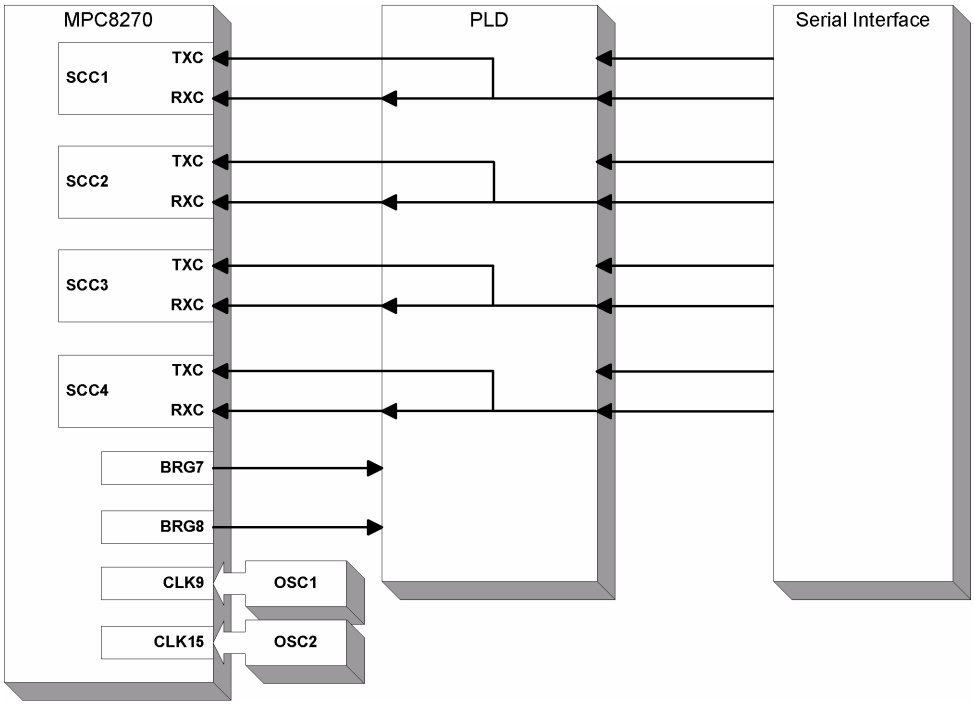
The following figures describe each of the available clock routing options.

Figure 6.1.5.2: Transmit Clock Input



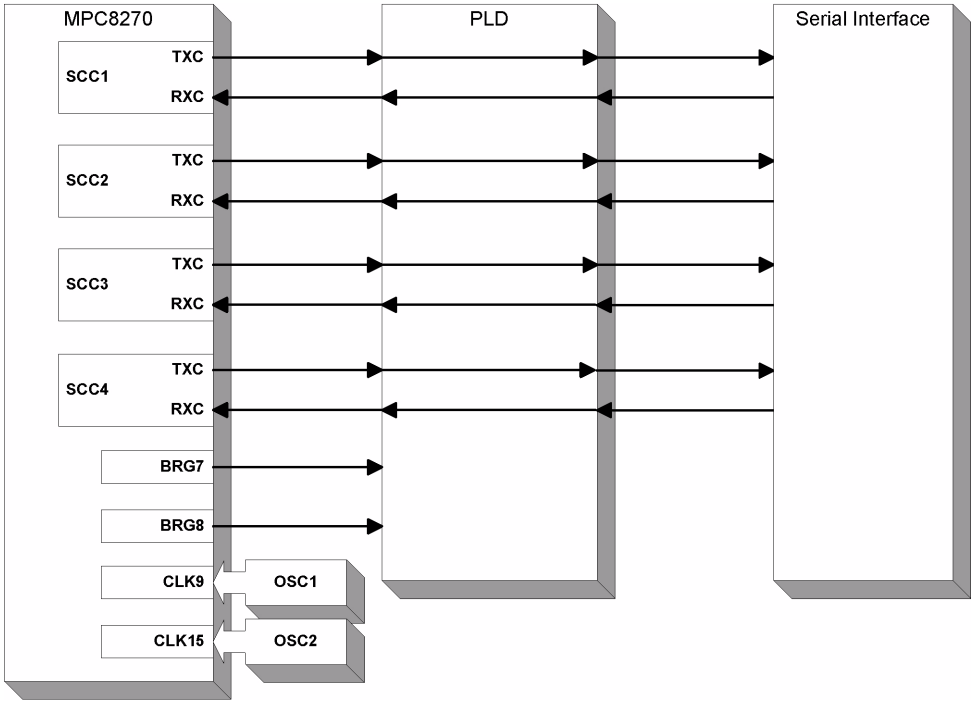
The default configuration, both the Receive Clock (RXC) and Transmit Clock (TXC) are input to the serial interface.

Figure 6.1.5.3: Transmit Clock Input (Receive Clock)



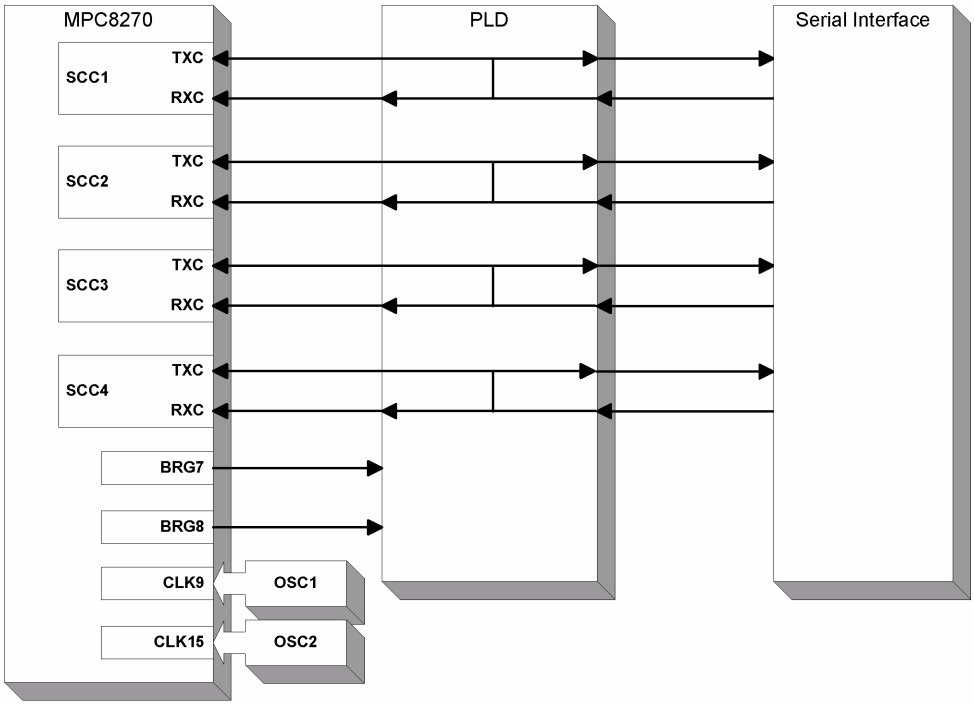
The Receive Clock (RXC) may optionally be used as both the receive and transmit clock inputs.

Figure 6.1.5.4: Transmit Clock Output



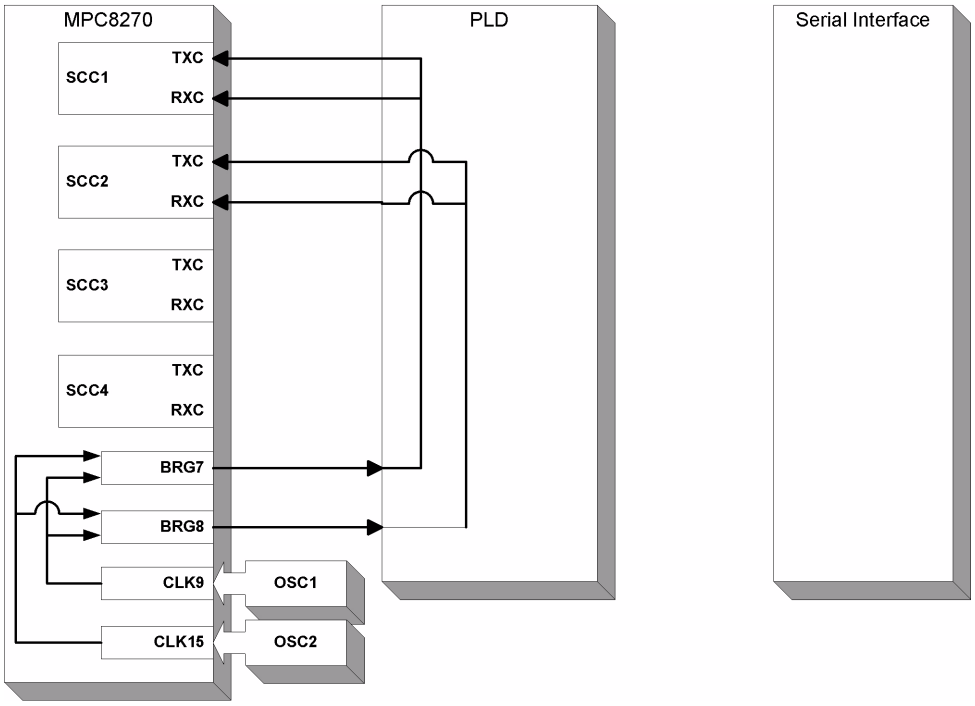
The Transmit Clock (TXC) may optionally be configured as an output from serial interface.

Figure 6.1.5.5: Transmit Clock Output (Receive Clock)



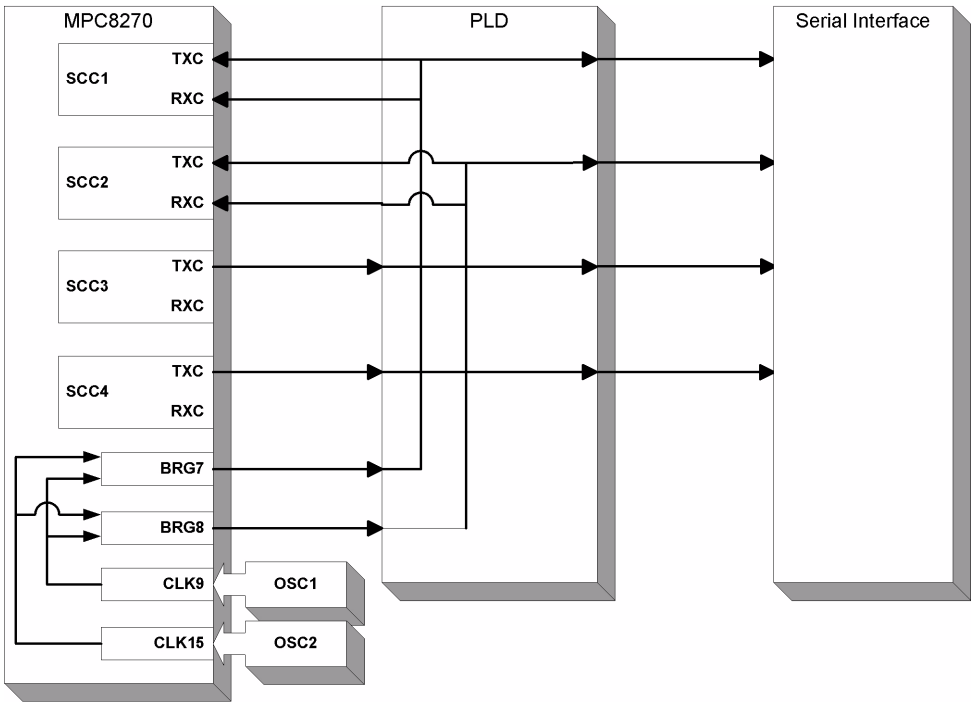
The Receive Clock (RXC) may also be used to source the Transmit Clock (TXC) and simultaneously echoed back onto the serial interface.

Figure 6.1.5.6: Transmit Clock Input (External Oscillator)



Custom oscillators may be placed on the board and be connected to the SCC interfaces. SCC Ports 3 and 4 can be connected internally to these frequencies, while Ports 1 and 2 must use the PLD to route the BRG output due to MPC8270 pin multiplexing.

Figure 6.1.5.7: Transmit Clock Output (External Oscillator)



Similarly, the custom oscillator frequencies may be used to drive Transmit Clock (TXC) as and output from the serial interface.

6.1.6: Serial Cables

X-ES offers a cable to route the front panel connections to DB-25 connectors. This cable consists of two parts, the serial cable and four modular adaptor ends. The serial cable comes in a number of lengths and can be made to fit your needs. The adaptor ends are interchangeable, each adaptor routing a single DTE DB-25 serial port. In addition, two SMC ports and one 10/100 Ethernet port can be routed from the front panel to a DTE or DCE adaptor end and terminated with an RJ-45 connector. The arrangement and pinouts for these connectors are described below. For additional information about the XPort1002 Series Cable and Adaptor Modules see the XPort1002 Series Cable Datasheet.

Figure 6.1.6.1: XPort1002 Front Panel Connector Detail

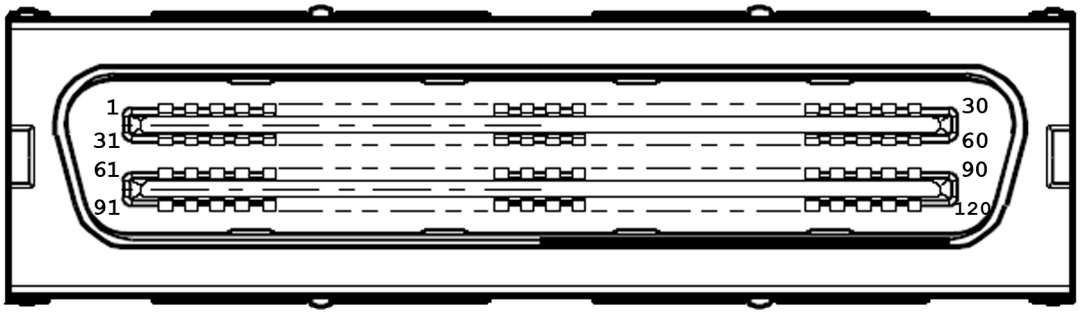


Table 6.1.6.2: Serial Cable and Adaptor Options

Front Panel Pins	Primary Port Options			Optional Secondary Port	
	Device Type	Connector	SCC Port	Connector	Option Port
1-30	DTE	DB-25	SCC Port 1	RJ-45	SMC Port 1
31-60	DTE	DB-25	SCC Port 2	RJ-45	Ethernet Port
61-90	DTE	DB-25	SCC Port 3	RJ-45	SMC Port 2
91-120	DTE	DB-25	SCC Port 4	-	-

Table 6.1.6.3: SCC Port 1 Pin Assignments

Pin Number			RS-232		RS-485/RS-422	
DB25	Front Panel	Back Panel	Mnemonic	Direction	Mnemonic	Direction
1	1		Shield		Shield	
14	2	1			TXD-	OUT
2	3	2	TXD	OUT	TXD+	OUT
15	4	3	TXC	IN	TXC+	IN
3	5	4	RXD	IN	RXD+	IN
16	6	5			RXD-	IN
4	7	6	RTS	OUT	RTS+	OUT
17	8	7	RXC	IN	RXC+	IN
5	9	8	CTS	IN	CTS+	IN
18	10					
6	11					
19	12	11			RTS-	OUT
7	13	12	GROUND		GROUND	
20	14					
8	15	14	DCD	IN	DCD+	IN
21	16					
9	17	13			RXC-	IN
22	18					
10	19	10			DCD-	IN
23	20					
24	21					
11	22					
12	23	9			TXC-	IN
25	24					
13	25	15			CTS-	IN
7 / NC	26					
	27					
	28					
	29	27 (61)	SMC_TXD1+	OUT	SMC Port 1 TX Data	
	30	57 (62)	SMC_RXD1+	IN	SMC Port 1 RX Data	

Table 6.1.6.4: SCC Port 2 Pin Assignments

Pin Number			RS-232		RS-485/RS-422	
DB25	Front Panel	Back Panel	Mnemonic	Direction	Mnemonic	Direction
1	31		Shield		Shield	
14	32	16			TXD-	OUT
2	33	17	TXD	OUT	TXD+	OUT
15	34	18	TXC	IN	TXC+	IN
3	35	19	RXD	IN	RXD+	IN
16	36	20			RXD-	IN
4	37	21	RTS	OUT	RTS+	OUT
17	38	22	RXC	IN	RXC+	IN
5	39	23	CTS	IN	CTS+	IN
18	40					
6	41					
19	42	26			RTS-	OUT
7	43	27	GROUND		GROUND	
20	44					
8	45	29	DCD	IN	DCD+	IN
21	46					
9	47	28			RXC-	IN
22	48					
10	49	25			DCD-	IN
23	50					
24	51					
11	52					
12	53	24			TXC-	IN
25	54					
13	55	30			CTS-	IN
7 / NC	56					
	57	61	E_TX_POS	OUT	10/100 Eth TX+	
	58	62	E_TX_NEG	OUT	10/100 Eth TX-	
	59	63	E_RX_POS	IN	10/100 Eth RX+	
	60	64	E_RX_NEG	IN	10/100 Eth RX-	

Table 6.1.6.5: SCC Port 3 Pin Assignments

Pin Number			RS-232		RS-485/RS-422	
DB25	Front Panel	Back Panel	Mnemonic	Direction	Mnemonic	Direction
1	61		Shield		Shield	
14	62	31			TXD-	OUT
2	63	32	TXD	OUT	TXD+	OUT
15	64	33	TXC	IN	TXC+	IN
3	65	34	RXD	IN	RXD+	IN
16	66	35			RXD-	IN
4	67	36	RTS	OUT	RTS+	OUT
17	68	37	RXC	IN	RXC+	IN
5	69	38	CTS	IN	CTS+	IN
18	70					
6	71					
19	72	41			RTS-	OUT
7	73	42	GROUND		GROUND	
20	74					
8	75	44	DCD	IN	DCD+	IN
21	76					
9	77	43			RXC-	IN
22	78					
10	79	40			DCD-	IN
23	80					
24	81					
11	82					
12	83	39			TXC-	IN
25	84					
13	85	45			CTS-	IN
7 / NC	86					
	87					
	88					
	89	(62)	SMC_TXD2+	OUT	SMC Port 2 TX Data	
	90	(63)	SMC_RXD2+	IN	SMC Port 2 RX Data	

Table 6.1.6.6: SCC Port 4 Pin Assignments

Pin Number			RS-232		RS-485/RS-422	
DB25	Front Panel	Back Panel	Mnemonic	Direction	Mnemonic	Direction
1	91		Shield		Shield	
14	92	46			TXD-	OUT
2	93	47	TXD	OUT	TXD+	OUT
15	94	48	TXC	IN	TXC+	IN
3	95	49	RXD	IN	RXD+	IN
16	96	50			RXD-	IN
4	97	51	RTS	OUT	RTS+	OUT
17	98	52	RXC	IN	RXC+	IN
5	99	53	CTS	IN	CTS+	IN
18	100					
6	101					
19	102	54			RTS-	OUT
7	103	55	GROUND		GROUND	
20	104					
8	105	56	DCD	IN	DCD+	IN
21	106					
9	107	57			RXC-	IN
22	108					
10	109	58			DCD-	IN
23	110					
24	111					
11	112					
12	113	59			TXC-	IN
25	114					
13	115	60			CTS-	IN
7 / NC	116					
	117					
	118					
	119					
	120					

6.2 SMC Interface

The XPort1002 provides two RS-232 SMC development/debug ports. Both ports are optionally routed to either the front panel and the development/debug header. Build options exist to route the SMC interfaces to the P14 connector as well.

6.2.1: Physical Interface Support

Each of the XPort1002 SMC interfaces provides an RS-232 serial interface consisting of Transmit Data (TXD) and Receive Data (RXD).

6.2.2: Serial Protocol Support

Each of the XPort1002 SMC interfaces operates as a simple UART protocol serial interface.

6.2.3: MPC8270 Parallel Port Pin Usage

The MPC8270 provides SMC port support through four parallel ports, which must be programmed according to how each port is to be used. The following table illustrates where each SMC port is connected to the MPC8270 and the direction of the signal.

Table 6.2.3.1: MPC8270 SMC Port Connections

Serial Function	SMC1 Port Usage	SMC2 Port Usage	Direction
TXD	PD9 SMC1:TXD	PA9 SMC2:TXD	OUTPUT
RXD	PD8 SMC1:RXD	PA8 SMC2:RXD	INPUT

Table 6.2.3.2: SMC Serial Signal Description

Mnemonic	Circuit Name	Description	DTE Direction
TXD	Transmit Data	Data sent by SMC	OUT
RXD	Receive Data	Data received by SMC	IN

6.2.4: Baud Rate Generator Assignment

The XPort1002 SMC ports can each be connected to either of two possible on board baud rate generators. The MPC8270 has a limited number of SCC and SMC clocking options, therefore care must be taken to ensure that BRG resources are available for any specific configuration.

Table 6.2.4.1: SMC BRG Usage Options

SMC Port	BRG Option 1	BRG Option 2
SMC1	BRG1	BRG7
SMC2	BRG2	BRG8

6.2.5: SMC Pin Assignments

The tables below show the pinout for each SMC interface on the front panel, back panel, and debug header (if applicable). Each SMC can be routed to either the front panel or the back panel. The XPort1002 series cabling, available from X-ES, routes each SMC interface to an RJ-45 connector. In addition, a 6 port cabling option exists to route the SMC interface to a DB-25 or DB-9 as required. The pinout of both the standard cabling and the XPort1002 front panel is described below.

Table 6.2.5.1: SMC Port 1 Pin Assignments

Pin Number		RS-232	
Cable RJ-45	Front Panel	Name	Direction
6	29	TXD	OUT
5	30	RXD	IN
4	13	GND	

Table 6.2.5.2: SMC Port 2 Pin Assignments

Pin Number		RS-232	
Cable RJ-45	Front Panel	Name	Direction
6	89	TXD	OUT
5	90	RXD	IN
4	73	GND	

6.3 I²C Controllers

The MPC8270 provides an I²C controller. The following table gives the I²C assignments on XPort1002.

Table 6.3.1: I²C Port Assignment

Serial Controller	Usage
I²C Port 0	16Kb SEEPROM

The device map for Port 0 is illustrated below. Each device address is 7 bit assuming the lsb bit is a don't care. The format is zzzz zzzx where z is the device address bits and x is the don't care bit.

Table 6.3.2: I²C Port 0 Device Map

I²C Device	Device Address
16Kb SEEPROM	0xA0

The following table defines the I2C pin assignments on XPort1002.

Table 6.3.3: I2C Interface Pin Assignments

Signal	MPC8270
SCL	PD14/I2CSCL
SDA	PD15/I2CSDA

7. Ethernet Interface

This chapter describes details of the 10/100Mbps ethernet interfaces, The XPort1002 uses the Intel LXT971A Fast Ethernet PHY Transceiver that directly supports both 100BASE-TX and 10BASE-T applications. It provides a Media Independent Interface (MII) that directly attaches to the MPC8270's Fast Communications Controller (FCC).

7.1 Ethernet Connections

The 10/100Mbps ethernet interface is connected to the front panel connector and the development/debug module. The following table defines the connections from the PHY to the each connector and the pinout of the optional secondary port on the serial cable adaptor.

Table 7.1.1: Ethernet Port Pin Assignments

Name	Serial Adaptor RJ-45	Front Panel	Direction
TPFOP	1	57	OUT
TPFON	2	58	OUT
TPFIP	3	59	IN
TPFIN	6	60	IN

7.2 MII Management Interface

The MII Management Interface is used to control the state of the PHY. The XPort1002's PHY is located at address 00000b. The following table lists the functional signal names as defined by the MII interface, and defines the MPC8270 Parallel Port I/O pins used.

Table 7.2.1: MII Interface Pin Assignments

Signal	MPC8270
MDIO	PA11/GPP:BI
MDC	PA10/GPP:OUT
MDINT	IRQ4

7.3 MII Data Interface

The MII Data Interface is used to pass data from the PHY to the MPC8270's FCC controller. The following table defines the functional signal names as defined by the FCC.

Table 7.3.1: FCC2 Pin Assignments

Signal	MPC8270
TXD0	PB22/FCC2:TXD0
TXD1	PB23/FCC2:TXD1
TXD2	PB24/FCC2:TXD2
TXD3	PB25/FCC2:TXD3
RXD0	PB21/FCC:RXD0
RXD1	PB20/FCC:RXD1
RXD2	PB19/FCC2:RXD2
RXD3	PB18/FCC2:RXD3
TXC	PC18/CLK14
RXC	PC16/CLK16
TxEn	PB29/FCC2:TX_EN
RxEn	PB28/FCC2:RX_EN
TxEr	PB31/FCC2:TX_ER
RxEr	PB30/FCC2:RX_ER
CRS*	PB26/FCC2:CRS
COL*	PB27/FCC2:COL