P1 Series

P1012 and P1021 single- and dual-core communications processors

Freescale QorIQ™ communications platforms are the next-generation evolution of our leading PowerQUICC® communications processors. Built using high-performance Power Architecture® cores, QorIQ platforms enable a new era of networking innovation where the reliability, security and quality of service for every connection matters.

QorIQ P1012 and P1021 Communications Processors

The QorIQ P1 platform series, which includes the P1012 and P1021 communications processors, offers the value of extensive integration and extreme power intelligence for a wide variety of applications in the networking, telecom, defense and industrial markets. Based on 45 nm technology for low-power implementation, the P1012 and P1021 processors provide single- and dual-core solutions for the 533 MHz to 800 MHz performance range, along with advanced security and a rich set of interfaces.

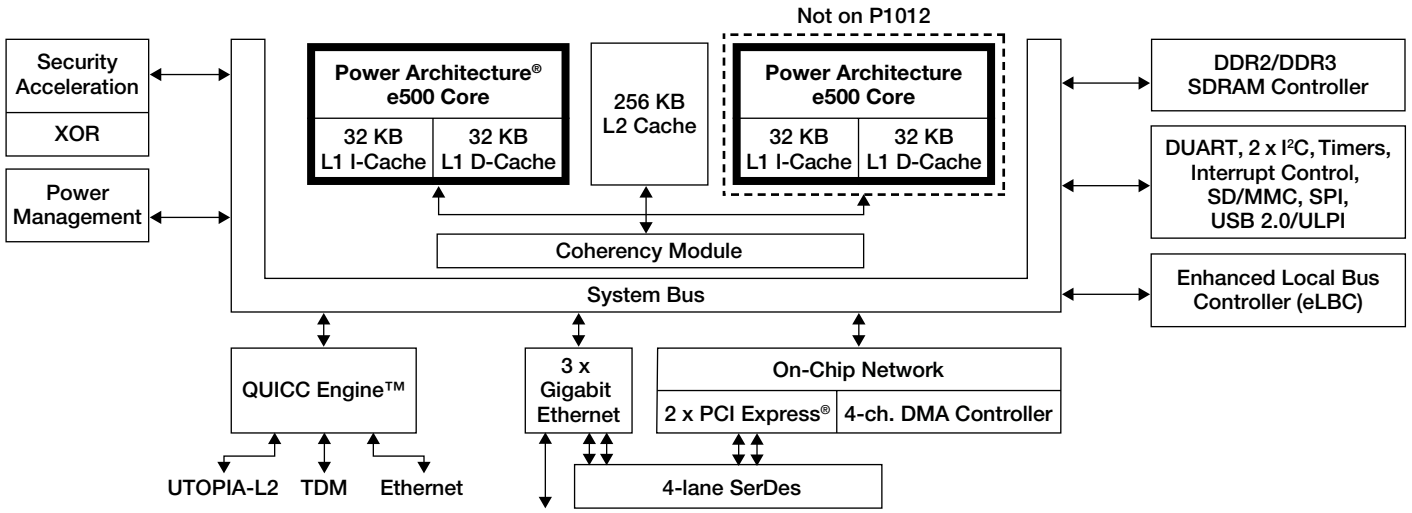
The P1012 and P1021 processors are perfectly suited for multi-service gateways, Ethernet switch controllers, wireless LAN access points and high-performance general-purpose control processor applications with tight thermal constraints.

The QorIQ P1012 and P1021 processors are pin-compatible with the QorIQ P1011, P1020 and P2 platform products, offering a six-chip range of cost-effective solutions. Scaling from a single core at 533 MHz (P1012) to a dual core at 1.2 GHz per core (P2020), the two QorIQ platforms deliver an impressive 4.5x aggregate frequency range.

The devices in these two platforms are software compatible, sharing the e500 Power Architecture core and peripherals, as well as being fully software compatible with the existing PowerQUICC processors. This enables you to create a product with multiple performance points from a single board design. The QorIQ P1021 dual-core processor supports symmetric and asymmetric processing, enabling you to further integrate your design with the same applications running on each core or serialize your application using the cores for different processing tasks.

The P1012 and P1021 processors have an advanced set of features for ease of use. The 256 KB L2 cache offers incremental configuration to partition the cache between the two cores or to configure it as SRAM or stashing memory. The integrated security engine supports the cryptographic algorithms commonly used in IPsec, SSL, 3GPP and other networking and wireless security protocols. The memory controller offers future proofing against memory technology migration with support for both DDR2 and DDR3. It also supports error correction codes, a baseline requirement for any high-reliability system.

QorIQ™ P1012 and P1021 Block Diagram



Cores

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The QorIQ P1012 and P1021 processors integrate a rich set of interfaces, including SerDes, Gigabit Ethernet, QUICC Engine™ module, PCI Express® and USB. The three 10/100/1000 Ethernet ports support advanced packet parsing, flow control and quality of service features, as well as IEEE® 1588 time-stamping—all ideal for managing the datapath traffic between the LAN and WAN interface. The QUICC Engine module provides UTOPIA-L2, TDM and 10/100 Ethernet interfaces as well as a programmable RISC engine to offload protocol termination from the main CPU cores. Four SerDes lanes can be portioned across two PCI Express ports and two SGMII ports. The PCI Express ports can provide connectivity to IEEE 802.11n radio cards for wireless support. USB or SD/MMC interfaces can be used to support local storage. Multiple memory connection ports are available, including the 16-bit local bus, a USB 2.0 controller, enhanced secure digital host controller (eSDHC) and serial peripheral interface (SPI).

Target Applications

The P1012 and P1021 processors serve a wide variety of applications. The devices are well-suited for various combinations of data plane and control plane workloads in networking and telecom applications. With an available junction temperature range of -40°C to +125°C, the devices can be used in power-sensitive defense and industrial applications, and outdoor environments less protected from the environment. The devices primarily target applications such as networking and telecom linecards.

A multi-service router or business gateway requires a combination of high performance and a rich set of peripherals to support the datapath throughputs and required system functionality. The P1012 and P1021 devices offer a scalable platform to develop a range of products that can support the same feature set. The QUICC Engine module, as well as integrated 10/100/1000 Ethernet controllers with classification and QoS capabilities, are ideal for managing the datapath traffic between the LAN and WAN interface. PCI Express ports can provide connectivity to IEEE 802.11n radio cards for wireless support, TDM for legacy phone interfaces to support voice and the USB or SD/MMC interfaces can be used to support local storage. The integrated security engine can provide encrypted secure communications for remote users with VPN support.

Technical Specifications

- Single (P1012) and dual (P1021) high-performance Power Architecture e500 cores
  - 36-bit physical addressing
  - Double-precision floating-point support
  - 32 KB L1 instruction cache and 32 KB L1 data cache for each core
  - 533 MHz to 800 MHz core clock frequency
- 256 KB L2 cache with ECC, also configurable as SRAM and stashing memory
- Three 10/100/1000 Mbps enhanced three-speed Ethernet controllers (eTSECs)
  - TCP/IP acceleration and classification capabilities
  - IEEE 1588 support
  - Lossless flow control
  - RGMII, SGMII
- High-speed interfaces (not all available simultaneously)
  - Four SerDes to 3.125 GHz multiplexed across controllers
  - Two PCI Express controllers
  - Two SGMII interfaces
- QUICC Engine module
  - UTOPIA-L2
  - Up to two 10/100 Ethernet interfaces
  - Up to four T1/E1/J1/E3 or DS-3 serial interfaces
  - Up to four HDLC interfaces with 128 channels of HDLC
  - Up to four BISYNC interfaces
  - Up to four UART interfaces
  - SPI interfaces
  - GPIO
- High-Speed USB controllers (USB 2.0)
  - Host and device support
  - Enhanced host controller interface (EHCI)
  - ULPI interface to PHY
- Enhanced secure digital host controller
- Serial peripheral interface
- Integrated security engine (SEC 3.3)
  - Crypto algorithm support includes 3DES, AES, RSA/ECC, MD5/SHA, ARC4, Snow 3G and FIPS deterministic RNG
  - Single pass encryption/message authentication for common security protocols (IPsec, SSL, SRTP, WiMAX)
  - XOR acceleration
- 32-bit DDR2/DDR3 SDRAM memory controller with ECC support
- Programmable interrupt controller (PIC) compliant with OpenPIC standard
- Four-channel DMA controller
- Two I^2C controllers, DUART, timers
- Enhanced local bus controller (eLBC)
- 16 general-purpose I/O signals
- Package: 689-pin wirebond power-BGA (TEPBGA2)

QorIQ™ Platform	Device	Cores	Top Core Frequency	L2 Size	DDR 2/3 Support	GE Ports	QUICC Engine™	SerDes	PCI Express®	Serial RapidIO®	TDM
P1	P1011	1	800 MHz	256 KB	32-bit with ECC	3	N/A	4	2	N/A	Yes
P1	P1020	2	800 MHz	256 KB	32-bit with ECC	3	N/A	4	2	N/A	Yes
P1	P1012	1	800 MHz	256 KB	32-bit with ECC	3	Yes	4	2	N/A	In QUICC Engine
P1	P1021	2	800 MHz	256 KB	32-bit with ECC	3	Yes	4	2	N/A	In QUICC Engine
P2	P2010	1	1200 MHz	512 KB	64-bit with ECC	3	N/A	4	3	2	N/A
P2	P2020	2	1200 MHz	512 KB	64-bit with ECC	3	N/A	4	3	2	N/A

Learn More: For current information about Freescale products and documentation, please visit **www.freescale.com/QorIQ**.

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