Data Sheet

BCM5338M

Integrated 10/100BASE-T/TX 9-Port Switch

GENERAL DESCRIPTION

The BCM5338M is a sixth-generation switch design based on the field proven industry leaders BCM5328 and BCM5328M. This device combines all the functions of a high-speed switch system, including packet buffers, PHY transceivers, media access controllers (MACs), address management, and a non-blocking switch fabric into a single 0.18µ CMOS device. It complies with the IEEE 802.3, 802.3u, and 802.3x specifications, including the MAC control PAUSE frame and auto-negotiation subsections, providing compatibility with all industry-standard Ethernet and Fast Ethernet devices.

The BCM5338M contains eight full-duplex 10BASE-T/100BASE-TX Fast Ethernet transceivers, each of which performs all of the physical layer interface functions for 10BASE-T Ethernet on Category 3, 4, or 5 Unshielded Twisted Pair (UTP) cable and 100BASE-TX Fast Ethernet on Category 5 UTP cable. In addition to the robust 10/100 Ethernet Digi-PHY™, MIB Autocast®, and management functions, the BCM5338M's nine-port switch has a rich feature set suitable for Voice Over IP, video, and data traffic for multimedia applications. The four-level priority queues map to 802.1p, DiffServ, TOS and COS, 4K entries 802.1Q VLAN, 802.1x EAPOL protocol filtering, and MAC based trunking with link failover. Per port bandwidth/rate control, MAC address locking, and IGMP snooping at Layer 3 allow system vendors to build advanced L2+ switch systems for the multitenant/multidweller unit (MDU/MTU) markets.

The proprietary MIB Autocast function encapsulates the on-chip MIB statistics and sends them out automatically on a predefined port (or ports) at programmed intervals. The BCM5338M periodically transmits a legal Ethernet frame on a designated port. The frames can be intercepted by an external management probe or a dedicated network management application, resident on any node within the network. This function requires only a small, low-cost microcontroller to initialize and configure the device. The BCM5338M provides an on-chip MIB statistics register to collect, receive, and transmit statistics for each port.

FEATURES

- Sixth-generation L2+ Fast Ethernet switch on a chip
- The BCM5338M integrates:
  - Eight transceivers (802.3u compliant)
  - Nine MACs (802.3x compliant)
  - 256 KB memory for packet buffer and control
  - Non-blocking switch fabric supports up to 24 ports
- Cascades to 36 ports through 3.2 Gbps expansion port
- Stack to 48 ports with 200 Mbps turbo MII port
- 802.1p QoS packet classification with four priority queues
- Port-based VLAN
- 802.1Q based VLAN with up to 4K entries
- Supports 802.1x EAPOL higher layer protocol
- MAC-based trunking with automatic link fail-over
- Programmable per port storm control
- Per port ingress/egress rate control with 64K/128K/256K (up to 100 Mbps) resolution
- 4K MAC addresses with automatic learning and aging
- Per port programmable MAC address locking
- Programmable per port flow control and backpressure
- Buffer repeater mode
- MII or reversed MII
- MDC/MDIO and SPI interfaces
- Port mirroring and IGMP Layer 3 snooping
- MIB Autocast function
- Hardware support SNMP and RMON, and STP
- Internal oscillator simplifies design and reduces cost
- JTAG
- 3.3V and 1.8V, typical power consumption: <2W
- 208-pin MQFP package

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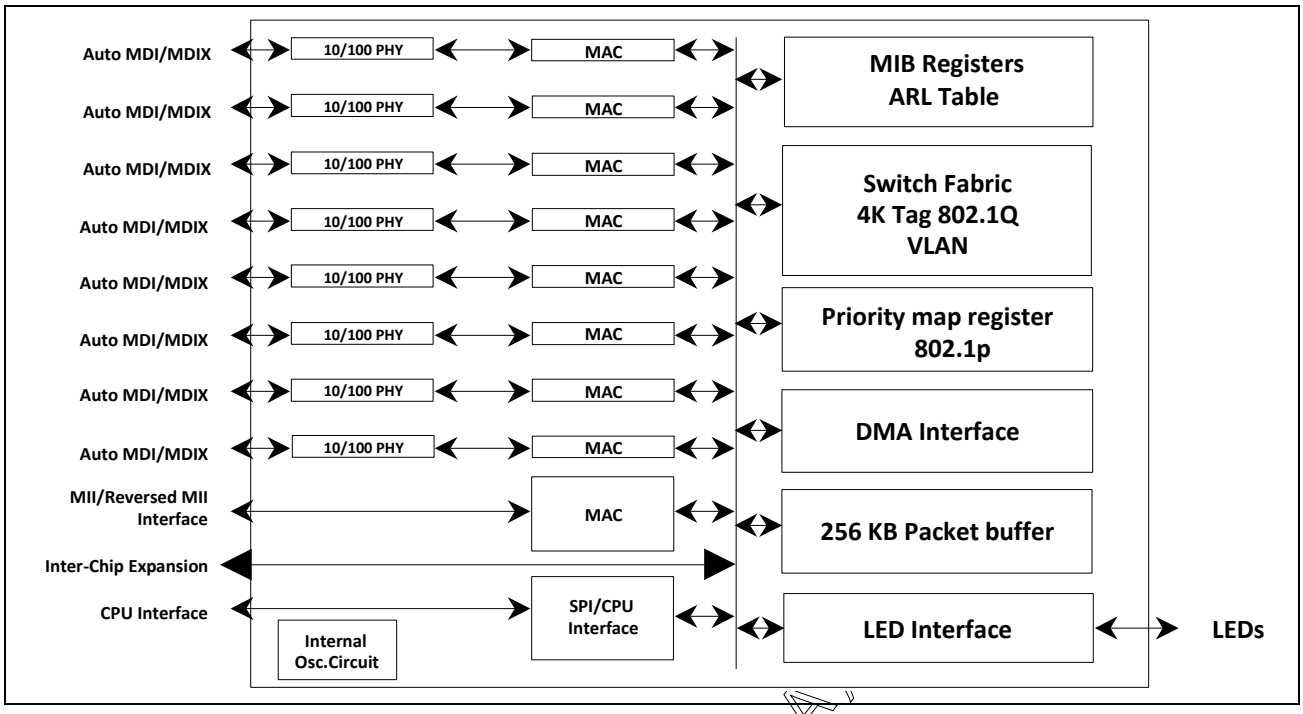

Figure 1: Functional Block Diagram

Revision History

Revision	*Date*	*Change Description*
5338M-DS202-R	07/20/10	**Updated:** • Figure 11: “MAC-to-MAC MII Connection,” on page 60. • Table 20: “Global Page Register Map,” on page 105. • Table 141: “Page 32h MAC-Based Trunking Registers,” on page 181. • Table 158: “Suppression Control Register (Page 35h, Address 00–08d, 00–08h),” on page 191. **Added:** • “Page Register” on page 210.
5338M-DS201-R	10/03/05	**Updated:** • Table 9: “Indirectly Supported MIB Counters,” on page 32. • Table 204: “Electrical Characteristics,” on page 201. **Added:** • Lead-free part number information to Section 9: “Ordering Information” on page 204.
5338M-DS200-R	04/14/05	Initial release.

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Section 1: Functional Description

Overview

The BCM5338M is a single-chip, nine-port 10/100BASE-TX switch device. This device integrates the following functions:

- Eight 10/100BASE-TX transceivers
- One general use (10/100BASE-TX/FX) MII
- Nine full-duplex capable media access controllers (MACs)
- Serial management port (SMP)
- High-performance integrated packet buffer memory
- Address resolution engine
- Non-blocking switch controller
- Set of management information base (MIB) statistics registers

The SMP allows the device to be custom-configured and the bridge management to be implemented.

The integrated 10/100BASE-TX transceivers perform all the physical layer interface functions for 100BASE-TX full-duplex or half-duplex Ethernet on CAT 5 twisted pair cable and 10BASE-T full- or half-duplex Ethernet on CAT 3, 4, or 5 cable.

The transceiver performs:

- 4B5B, MLT3, NRZI, and Manchester encoding and decoding
- Clock and data recovery
- Stream cipher scrambling/descrambling
- Digital adaptive equalization
- Line transmission
- Carrier sense and link integrity monitor
- Auto-negotiation
- MII management functions

Each of the integrated transceiver ports of the BCM5338M connects directly to the network media through isolation transformers. The integrated transceiver is fully compliant with the IEEE 802.3 and 802.3u standards. The device provides nine internal MACs.

Each MAC is dual-speed and both half-duplex and full-duplex capable. Flow control is provided in the half-duplex mode with backpressure. In full-duplex mode, 802.3x frame-based flow control is provided. The MAC is 802.3 compliant and supports a maximum frame size of 1536 bytes.

An integrated address management engine provides address learning and recognition functions at maximum frame rates. The address table provides capacity for up to 4K unicast and multicast addresses. Addresses are added to the table after receiving an error-free packet. Broadcast and multicast frames are forwarded to all ports within the VLAN domain except the port where it was received.

The MIB statistics registers collect, receive, and transmit statistics for each port, and provide direct hardware support for the EtherLike MIB, Bridge MIB, MIB II (interfaces), and the first four groups of the RMON MIB. All nine groups of RMON can be supported by using additional capabilities, such as port mirroring/snooping, together with an external microcontroller to process some MIB attributes. The MIB registers can be accessed through the SMP by an external microcontroller.

Global Functions

Clocks

The device requires a single 25 MHz clock signal at the XTALI/CK25 input pin. The other clock option is using a 25 MHz crystal at XTALI/CK25 and XTALO pins. An internal PLL derives all the clock frequencies needed by the device from the single clock input.

The device generates all internal clocks to the packet buffer memory and expansion interface. The default clock frequency is set to 83 MHz for support of system configuration up to 24 ports.

When using the MII port, an additional 25 MHz receive and transmit clock must be supplied by the external transceiver.

Reset

A power-on or hard reset is initiated by an active low reset pulse on the $\overline{\text{RST}}$ signal pin. Broadcom recommends a 50 ms low pulse to guarantee that a sufficiently long reset is applied to all internal circuits including integrated PHYs. The initialization process loads all pin configurable modes, resets all internal processes and returns them to an idle state, and initializes the memory structure. At the completion of the reset sequence, all ports are enabled for frame reception and transmission. During initialization, the XTALI/CK25 input signal must be active and the power supply to the device is stable.

Physical Layer Transceivers

Encoder/Decoder

In 100BASE-TX mode, the transceiver transmits and receives a continuous data stream on twisted pair. During transmission, nibble wide (4-bit) data from the MAC is encoded into 5-bit code groups and inserted into the transmit data stream. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start of stream delimiter (J/K codes) and appending an end of stream delimiter (T/R codes) to the end of the packet. When the MII transmit error input is asserted during a packet, the transmit error code group (H) is sent in place of the corresponding data code group. The transmitter repeatedly sends the idle code group in between packets.

In 100BASE-TX mode, the encoded data stream is scrambled by a stream cipher block and then serialized and encoded into MLT3 signal levels. A multimode transmit DAC is used to drive the MLT3 data onto the twisted pair cable.

Following baseline wander correction, adaptive equalization and clock recovery in 100BASE-TX mode, the receive data stream is converted from MLT3 to serial NRZ data. The NRZ data is descrambled by the stream cipher block and then deserialized and aligned into 5-bit code groups.

The 5-bit code groups are decoded into 4-bit data nibbles and provided as the input data stream to the MAC. The start of stream delimiter is replaced with preamble nibbles, and the end of stream delimiter and idle codes are replaced with all zeros. When an invalid code group is detected in the data stream, the transceiver asserts a receiver error indication to the MAC.

In 10BASE-T mode, Manchester encoding and decoding is performed on the data stream. The multimode transmit DAC performs preequalization for 100m of CAT 3 cable.

Link Monitor

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal or certain invalid signals are detected on the receive pair, the link monitor enters and remains in the Link Fail state where only idle codes are transmitted. When a valid signal is detected on the receive pair for a minimum period of time, the link monitor enters the Link Pass state and the transmit and receive functions are enabled.

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the RD± pins for the presence of valid link pulses.

Collision Detection

In half-duplex mode, collisions are detected whenever the transceiver is simultaneously transmitting and receiving activity.

Auto-Negotiation

Each internal transceiver contains the ability to negotiate its mode of operation over the twisted pair link using the auto-negotiation mechanism defined in the IEEE 802.3u specification. During auto-negotiation, each port automatically chooses its mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM5338M is configured to advertise 802.3x flow-control capability and can also advertise that it is Next Page capable. The transceiver negotiates with its link partner and chooses the highest level of operation available for its own link. In FDX mode, flow control is also negotiated. In HDX mode, flow control is enabled/disabled based on pin strappings. The auto-negotiation algorithm supports the Parallel Detection function for legacy 10BASE-T devices and 100BASE-TX-only devices that do not support auto-negotiation. Auto-negotiation in the BCM5338M device also allows the optional Next Page capability to be advertised, and permits Next Page exchange with a similarly capable link partner. Next Page exchange sequences and their contents are controlled via software control of the on-chip registers.

Digital Adaptive Equalizer

The digital adaptive equalizer removes intersymbol interference created by the transmission channel media. The equalizer accepts sampled unequalized data from the ADC on each channel and produces equalized data. The BCM5338M achieves an optimum signal-to-noise ratio by using a combination of feed-forward equalization and decision-feedback equalization. This powerful technique achieves a 100BASE-TX BER of less than 1×10^{-12} for transmission up to 100m on CAT 5 twisted-pair cable, even in harsh noise environments. The digital adaptive equalizers in the BCM5338M achieve performance close to theoretical limits. The all-digital nature of the design makes the performance very tolerant to on-chip noise. The filter coefficients are self-adapting to any quality of cable or cable length. Due to transmit preequalization in 10BASE-T mode and complete lack of ISI in 100BASE-FX mode, the adaptive equalizer is bypassed in these two modes.

Analog-to-Digital Converter

The receive channel has a 6-bit, 125 MHz analog-to-digital converter (ADC). The ADC samples the incoming data on the receive channel and produces a 6-bit output. The output of the ADC is fed to the digital adaptive equalizer. Advanced analog circuit techniques achieve low-offset, high-power supply noise rejection, fast settling time, and low bit error rate.

Digital Clock Recovery/Generator

The all-digital clock recovery and generator block creates all internal transmit and receive clocks. The transmit clock is locked to the 25 MHz clock input while the receive clock is locked to the incoming data stream. Clock recovery circuits optimized to MLT3, NRZI, and Manchester encoding schemes are included for use with each of the three different operating modes. The input data stream is sampled by the recovered clock and fed synchronously to the digital adaptive equalizer.

Baseline Wander Correction

A 100BASE-TX data stream is not always DC-balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can wander. This effect, known as baseline wander, can greatly reduce the noise immunity of the receiver. The transceiver automatically compensates for baseline wander by removing the DC offset from the input signal, and thereby significantly reduces the chance of a receive symbol error.

Digital-to-Analog Converter

The multimode transmit digital-to-analog converter (DAC) transmits MLT3-coded symbols in 100BASE-TX mode and Manchester-coded symbols in 10BASE-T mode. It performs programmable edge-rate control in TX mode, which decreases unwanted high frequency signal components, thus reducing EMI. High-frequency pre-emphasis is performed in 10BASE-T mode. The transmit DAC utilizes a current drive output that is well-balanced and produces very low noise transmit signals.

Stream Cipher

In 100BASE-TX mode, the transmit data stream is scrambled to reduce radiated emissions on the twisted-pair cable. The data is scrambled by exclusive ORing the NRZ signal with the output of an 11-bit-wide Linear Feedback Shift Register (LFSR), which produces a 2047-bit, non-repeating sequence. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle codes. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle code groups. The receiver does not attempt to decode the data stream unless the descrambler is locked. When locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization. The receive data stream is expected to contain interpacket idle periods. If the descrambler does not detect enough idle codes within 724 µs, it becomes unlocked, and the receive decoder is disabled. The descrambler is always forced into the unlocked state when a link failure condition is detected.

Stream cipher scrambling/descrambling is not used in 10BASE-T modes.

MII Management

Each transceiver within the BCM5338M contains a complete set of MII management registers (see “Port MII Registers” on page 148). The 5-bit transceiver address is assigned by concatenation of the 2-bit chip ID and the internal 3-bit port ID. All MII Management registers can be accessed through the shared MII management port using the MDC and MDIO signals, or through the SMP.

100BASE-FX Fiber Mode

The 10/100 port can be configured to operate in 100BASE-FX compatible mode. The following sequence is required for configuring the preferred PHY ports to 100BASE-FX-compatible operation using register write from the CPU. Each port's register can be programmed through page 10h-18h, respectively. A global write to page 19h enables writing to the registers of all 8 ports:

1. Write 2100h to "MII Control Register" on page 151. This forces the port to 100M full-duplex without auto-negotiation. Most FX applications require configuration for full-duplex.
2. Set bit 9 of "100BASE-X Auxiliary Control Register" on page 161. This bypasses the scrambler and descrambler blocks (i.e., these scrambling functions are not required for 100BASE-FX operation). Other bits within this register may be set, so it is best to perform a read-modified write to ensure proper setting of this register.
3. Set bit 5 of hidden register address 2Eh–2Fh (pages 10h–18h). This changes the three-level MLT-3 code transmitted by the PHY to two-level binary, suitable for driving standard fiber transceivers. Additionally, the PHY receiver is configured to recognize binary signaling. This register access must also be in the form of a read-modified write.

For the FX termination requirement, refer to the *531X-AN1XX 100BASE-FX Compatibility Application Note*.

Media Access Controllers

The BCM5338M contains nine internal dual-speed MACs. The MACs automatically select 10 Mbit or 100 Mbit mode, CSMA/CD or full-duplex, based on the result of auto-negotiation. In FDX mode, 802.3x PAUSE-frame-based flow control is also determined through auto-negotiation. The MACs are compliant with IEEE 802.3, 802.3u, and 802.3x specifications.

Receive Function

The MAC initiates frame reception following the assertion of receive data valid indication from the physical layer. The MAC monitors the frame for the following error conditions:

- Receive error indication from the PHY
- Run frame error if frame is fewer than 64 bytes
- CRC error
- Long frame error if frame is greater than 1536 bytes

If no errors are detected, the frame is processed by the switch controller. Frames with errors are discarded.

Transmit Function

Frame transmission begins with the switch controller queuing a frame to the MAC transmitter. The frame data is transmitted as received from the switch controller. The transmit controller is responsible for preamble insertion, carrier deferral, collision backoff, and interpacket gap enforcement.

In half-duplex mode, when a frame is queued for transmission, the transmit controller behaves as specified by the 802.3 requirements for frame deferral. Following deferral, the transmitter adds 8 bytes of preamble and SFD to the frame data received from the switch controller. If, during frame transmission, a collision is observed and the collision window timer has not expired, the transmit controller asserts jam and then executes the backoff algorithm. The frame is retransmitted when appropriate. On the sixteenth consecutive collision the backoff algorithm starts over at the initial state, the collision counter is reset and attempts to transmit the current frame continuously. Following a late collision, the frame is aborted and the switch controller is allowed to queue the next frame for transmission.

While in full-duplex mode, the transmit controller ignores carrier activity and collision indication. Transmission begins after the switch controller queues the frame and the 96 bit times of IPG have been observed.

Ingress/Egress Rate Control

Rate control is used to meter and limit the rate of data stream input or output to a port. The BCM5338M can either flow control or drop the frame if the ingress rate exceeds its limit. The BCM5338M supports ingress/egress rate control and storm control on all local ports and MII ports. The SMP and expansion ports do not support rate/storm control.

For an ingress port, the algorithm used is a dual-bucket mechanism. By checking/unchecking the mask table of each bucket, one can select the preferred packet types together for metering. For detail programming information, see Table 176 on page 201 and Table 178 on page 202.

Each bucket maintains a packet type mask table. If the item in the table is checked, the BCM5338M checks the incoming packet's type and updates the bucket.

A packet drop enable setting causes any incoming packet to be dropped if the bucket runs out. If it is not set, a pause/jam frame is sent out when bucket runs out. If the Full-duplex and Half-duplex flow control capability of the port is not enabled, the only mechanism is drop, even if the packet drop enable bit is not set. In the packet drop disable case, when the bucket runs out, a pause/jam frame is sent out. If there are more packets coming in before the bucket reaches a reasonable budget, the packet is dropped.

By setting bit rate style and refresh count in the Bit Rate Table, the BCM5338M can change the definable bit rate of each port.

A similar algorithm is used for egress rate control. For detail programming information, see Table 181 on page 203. If the egress rate exceeds the limit, the BCM5338M does not drop the frame. It just stops sending frames to the egress port.

The BCM5338M also has separate per port Storm control logic to control Multicast, Broadcast, and un_learned unicast (DLF). See the Table 158 on page 191. Any combination of Mcast, Bcast, and DLF can be selected to be controlled. The allowable rates are 3.3%, 5%, 10%, and 20% of the traffic of that port.

Flow Control

The BCM5338M implements an intelligent flow control algorithm to minimize the system impact resulting from flow control measures. Buffer memory allocation is adaptive to the status of each port's speed and duplex mode, providing an optimal balance between flow management and per port memory depth. The BCM5338M initiates flow control in response to buffer memory conditions on a per port basis.

The MACs are capable of flow control in both full-and half-duplex modes. In half-duplex mode, the MAC backpressures a receiving port by transmitting a 96-bit time-jam packet to the port. A single jam packet is asserted for each received packet for the duration of the time the port is in the flow control state.

Flow control in full-duplex mode functions as specified by the IEEE 802.3x requirements. In the receiver, MAC flow control frames are recognized and, when properly received, set the flow control pause time for the transmit controller. The pause time is assigned from the 2-byte pause time field following the pause opcode. MAC control PAUSE frames are not forwarded from the receiver to the switch controller.

When the switch controller requests flow control from a port, the transmit controller transmits a MAC control PAUSE frame with the pause time set to the PAUSE_QUANTA register value (always set to maximum). When the condition that caused the flow control state is no longer present, a MAC control PAUSE frame is sent with the pause time field set to 0.

The flow control capabilities of the BCM5338M are enabled based on the results of auto-negotiation and the state of the ENFDXFLOW and ENHDXFLOW control signals loaded during reset. Flow control in half-duplex mode is independent of the state of the link partner's flow control capability. Table 1 provides more detailed information.

Table 1: Flow Control Modes

sw_flow_con_on	*sw_flow_con*	*LPFCCAP*	*ENFDXFLOW*	*ENHDXFLOW*	*Flow Control*	
					Full-Duplex	*Half-Duplex*
0	X	X	X	0	X	Disable
0	X	X	X	1	X	Enable
0	X	0	0	X	Disable	X
0	X	0	1	X	Disable	X
0	X	1	0	X	Disable	X
0	X	1	1	X	Enable	X
1	0	X	X	X	Disable	Disable
1	1	X	X	X	Enable	Enable

Note:

- sw_flow_con_on and sw_flow_con are located in register page 00h, offset 24h.
- LPFCCAP obtained from result of AN.
- ENFDXFLOW and ENHDXFLOW are strap pins.

Serial Management Port

The SMP provides a serial interface for a general purpose microcontroller. It allows network management functions to be implemented in software in a BCM5338M-based system. The SMP is configured to be compatible with the Motorola Serial Peripheral Interface (SPI) protocol.

The internal address space of the BCM5338M device is broken into a number of pages. Each page groups a logical set of registers associated with a specific function. For examples, see:

- Table 21 on page 107
- Table 34 on page 114
- Table 74 on page 132
- Table 124 on page 170

Each page provides a logical address space of 256 bytes, although, in general, only a small portion of the address space in each page is utilized.

All pages have reserved registers from addresses F0h–FFh, and all pages behave identically over this space, as shown in "Register Definitions" on page 105. Address FFh is the page register. The page register in any page can be written with a new page number, allowing access between pages. Address FEh is the "SPI Status Register" on page 209, and addresses F0h–F7h are the "SPI Data I/O n Registers" on page 209.

SPI Mode

The BCM5338M can be controlled over a serial interface that is compatible with a subset of the Motorola Synchronous Serial Peripheral Interconnect (SPI) bus. A simplified explanation of the operation of this bus is given in this section. The microcontroller interface consists of four signals:

- Serial clock (SCK)
- Slave select ($\overline{SS}$)
- Master-in/slave-out (MISO)
- Master-out/slave-in (MOSI)

The BCM5338M always operates as an SPI slave device, in that it never initiates a transfer on the SPI, only responds to the read and write requests issued from a master device. The SCK clock can run up to 2 MHz. $\overline{SS}$ is asynchronous. If $\overline{SS}$ is asserted during SCK high, then the MOSI inputs are sampled on the rising edge of SCK. The MISO outputs are generated internally on the falling edge of SCK and have adequate setup and hold time to be sampled externally on the rising edge of SCK. Otherwise, BCM5338M samples data on the falling edge and outputs data on the rising edge of SCK.

A layer of protocol is added to the basic SPI definition to facilitate transfers from the BCM5338M. This protocol establishes the definition of the first 2 bytes issued by the master to the BCM5338M slave during a SPI transfer. The first byte issued from the SPI master in any transaction is defined as a command byte, which is always followed by a register address byte, and any additional bytes are data bytes.

The SPI mode supports two different access mechanisms, normal SPI and fast SPI, determined by the content of the command byte. Figure 2 shows the normal SPI command byte, and Figure 3 shows the Fast SPI command byte. These two mechanisms should not be mixed in an implementation, and the CPU should always initiate transfers consistently with only one of the mechanisms.

0	1	1	MODE = 0	0	0	0	Read/Write (0/1)

Figure 2: Normal SPI Command Byte

Byte Offset (MSB)	Byte Offset	Byte Offset (LSB)	MODE = 1	0	0	0	Read/Write (0/1)

Figure 3: Fast SPI Command Byte

The MODE bit (bit 4) of the command byte determines the meaning of bits 7:5. If bit 4 is 0, it is a normal SPI command byte, and bits 7:5 should be defined as 011b. If bit 4 is 1, bits 7:5 indicate a fast SPI command byte, and bits 7:5 indicate the byte offset into the register that the BCM5338M starts to read from (byte offsets are not supported for write operations).

In both command bytes, bits 3:1 indicate the CHIP ID to be accessed.The value 111b is reserved as a broadcast write address, allowing all BCM5338M devices to be written to simultaneously. No corresponding broadcast read operation is supported.

Note: The $\overline{SS}$ signal must also be active for any BCM5338M device to recognize that it is being accessed.

Bit 0 of the command byte is the R/W signal (0 = Read, 1 = Write) that determines the data direction for the transmission.

The byte following the command byte is an 8-bit register address. Initially, this sets the page address, followed by another command byte that contains the register base address in that page, which is used as the location to store the next byte of data received in the case of a write operation, or the next address from which to retrieve data in the case of a read operation. This base address increments as each byte of data is transmitted/ received, allowing a contiguous block data from a register to be stored/read in a single transmission.

Note: The actual start location of a read operation can be modified by the offset contained in bits 7:5 of the command byte, when the fast SPI command byte is used.

Reading/writing data from/to separate registers, even if those registers are contiguous in the current page, must be performed by supplying a new command byte and register address for each register, with the address as defined in the appropriate page register map.

Non-contiguous blocks are also stored/read through the use of multiple transmissions, which allow a new command byte and register base address to be specified. The SS signal must remain low for the entire read or write transaction, as shown in Figure 4 and Figure 5, with the transaction terminated by the deassertion of the SS line by the master.

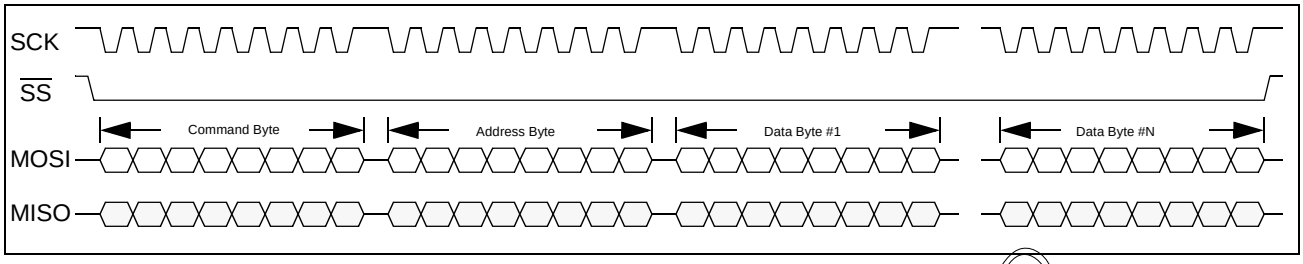

Figure 4: SPI Serial Management Port Interface Write Operation

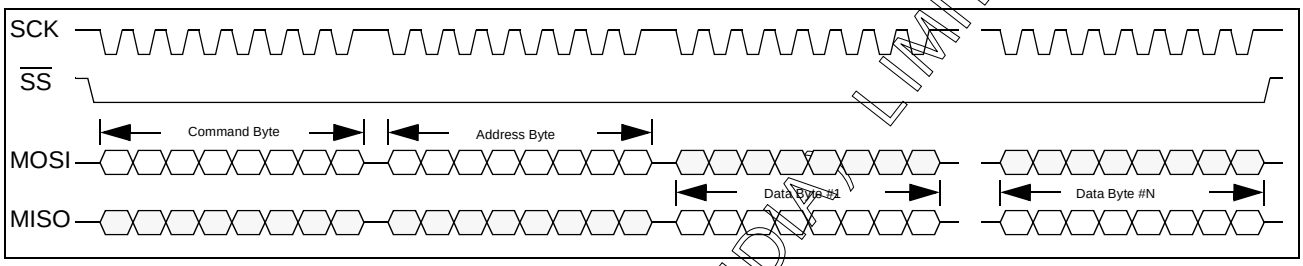

Figure 5: SPI Serial Management Port Interface Read Operation

The SMP supports operation up to 2 MHz in SPI mode. A maximum of three devices can be cascaded/addressed.

Normal SPI Mode

Normal SPI mode allows single-byte read and multibyte string write operations, with the CPU polling to monitor progress. Read operations are performed using the "SPI Status Register" on page 209 (SPI_STS register) and "SPI Data I/O n Registers" on page 209 (SPI_DIO[0:7] registers). All read operations take the form:

```
<CMD, 000, R><REG ADDR>
```

...where the first byte is the command byte with the appropriate Read bits set, and the second byte is the register address. All write operations are of the form:

```
<CMD, 000, W><REG ADDR><DATA0>...<DATAn>
```

...where the first byte is the command byte with the Write bits set, the second byte is the register address, and the exact number of data bytes appropriate for the selected register follow. Failure to provide the correct number of data bytes means the register write operation does not occur.

A simple flow chart for the read process is shown in Figure 6 on page 36. To read a register, first the page register is written (<CMD, 000, W><REG ADDR=FFh><DATA=NEW PAGE>). It is only necessary to write the page register when moving to a new page. Once in the correct page, a read operation is performed on the appropriate register (<CMD, 000, R><REG ADDR>). Once the SPI_STS register indicates that the data is available (RACK = 1), the data can be read. Data is read from the SPI_DIO[0:7] registers, located at F0h–F7h on every page (so no page swap is necessary to read the data on any page). A read operation can access any or all of the bytes

on a specific register, including the ability to start at any offset. For instance, reading from SPI_DIO[0], reads the least significant byte of the register, and successive reads to SPI_DIO[0] read the remaining bytes. However, reading the first byte from SPI_DIO[2] would read the third byte of the register, and successive reads to SPI_DIO[2] would read the remaining bytes of the register up to the most significant byte of the register. It is not necessary to read all bytes of a registers, only the bytes of interest. The SPI master can then move on to perform another read or write operation.

A flow chart for the write process is shown in Figure 7 on page 37. To write a register, the page register is written if necessary (<CMD, 000, W><REG ADDR=FFh><DATA=NEW PAGE>), then data is written to the selected register (<CMD, 000, W><REG ADDR><DATA0>...<DATAn>), where DATA0 is the least significant byte of the register, and DATAn is the most significant byte of the register, and the exact number of bytes is present as defined by the register width. No byte offset is provided for write operations, and all bytes must be present to activate the write process internal to the BCM5338M.

The following simple rules apply to the normal SPI mode:

- A write to the page register at any time causes the SPI state machine to reset.
- A read operation can access any number of bytes at any offset using the SPI_DIO[0:7] registers.
- A write operation must write the exact number of bytes to the register being accessed.
- The RXRDY/TXRDY flags must be checked after each 8-byte string has been read/written, to ensure the next string is ready/can be accepted (since the largest internal register is 8 bytes, this restriction only applies to reading and writing frames via the SPI).

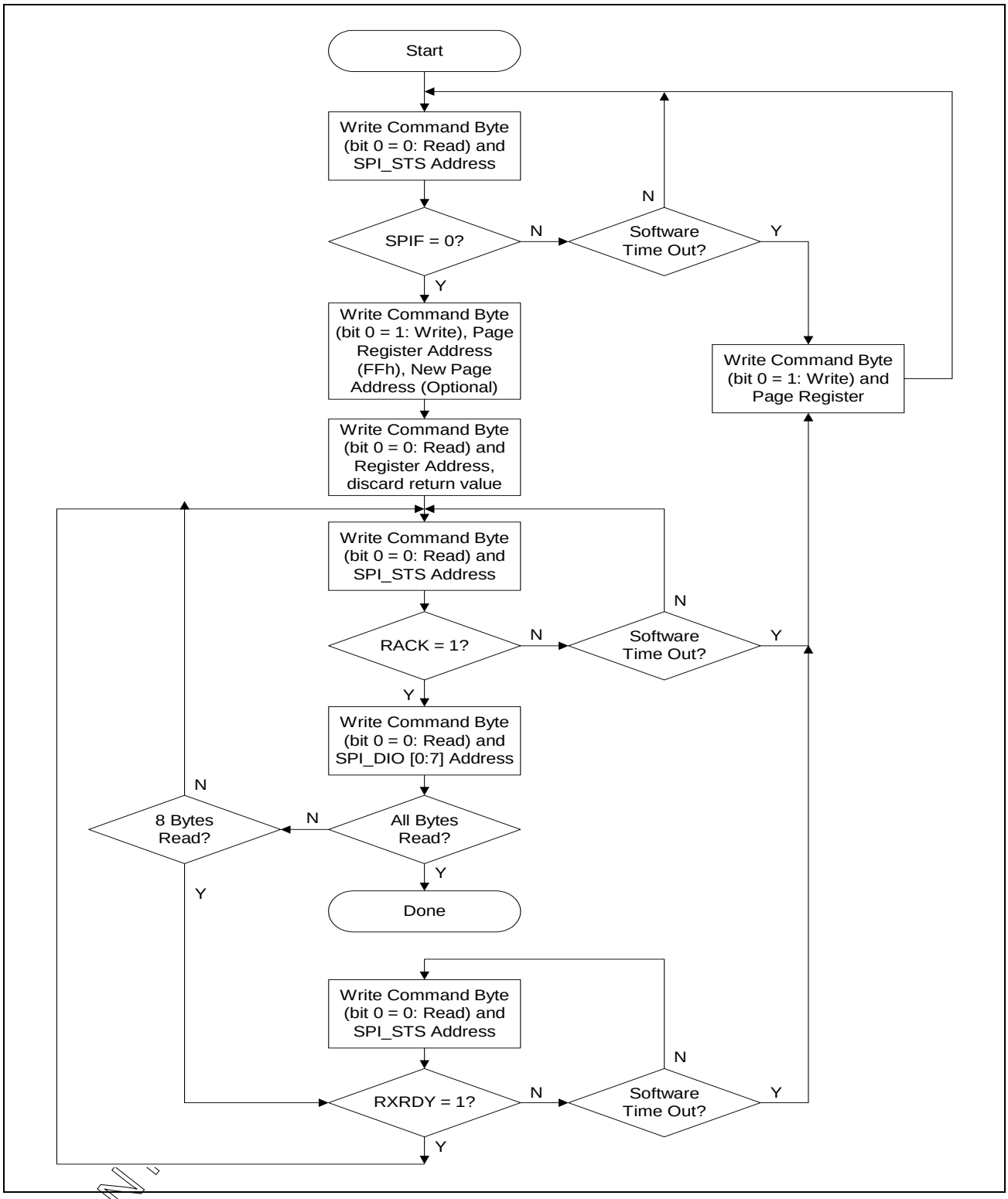

Figure 6: Normal SPI Mode Read Flow Chart

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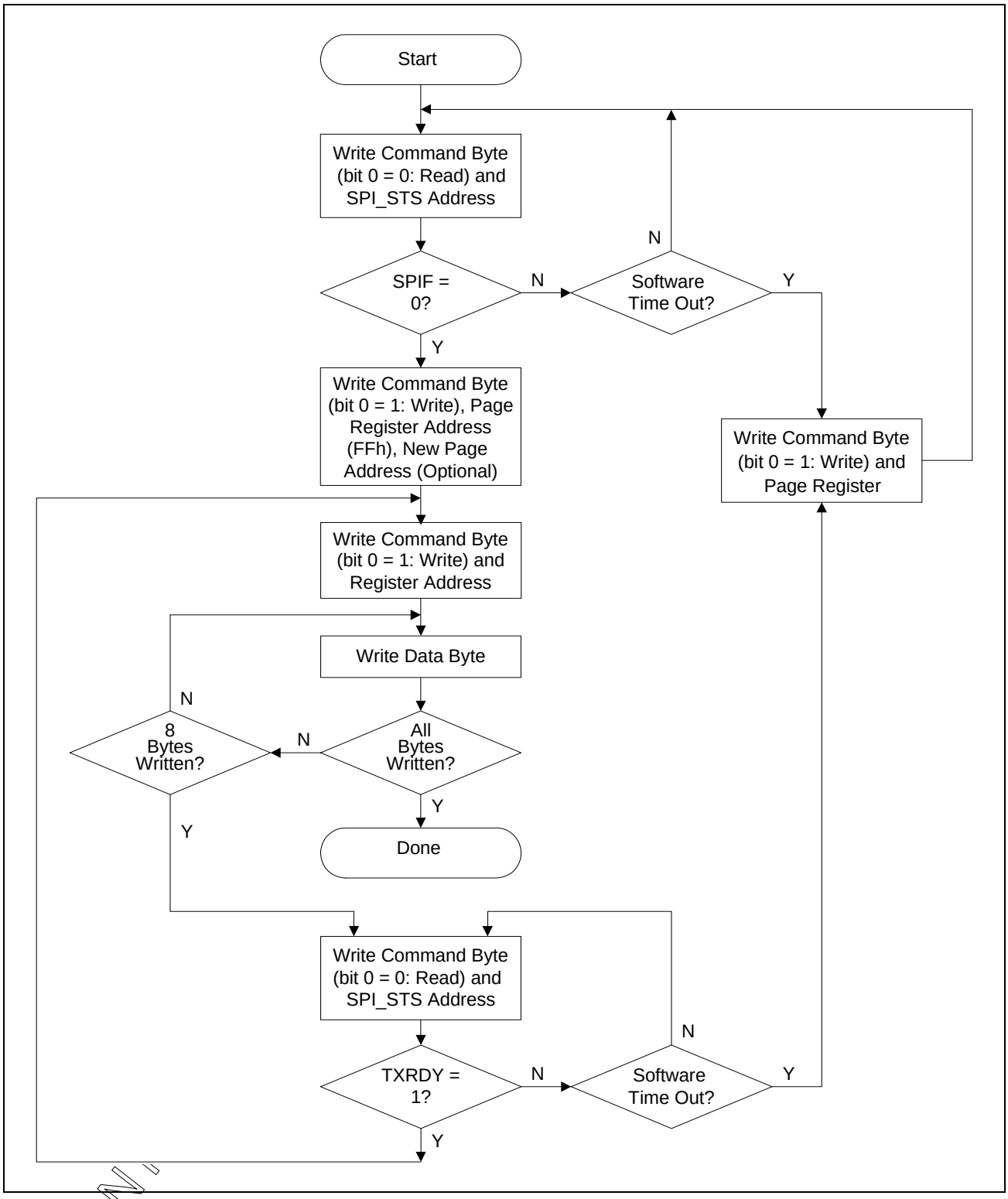


Figure 7: Normal SPI Mode Write Flow Chart

Fast SPI Mode

Fast SPI mode makes use of the fact that the SPI port is inherently full-duplex and provides an explicit acknowledge on read cycles to eliminate the polling of the SPI_STS register for RACK polling. Fast SPI mode requires the MODE bit in the command byte to be set as indicated in Figure 3 on page 33. Like normal SPI mode, fast SPI mode also supports byte offsets for read operations, and broadcast (multichip) write operations.

Read operations do not access the SPI_DIO[0:7] registers. Instead, status and data are output on the MISO line by the BCM5338M. Once the page register and the register within that page have been set, the master reads the MISO line state, The BCM5338M immediately puts out a byte string, which indicates the state of the RACK bit in bit 0 of each byte. Once bit 0 is sampled high in a byte, the next byte is the least significant byte of the read data, and successive bytes follow. Byte offset into the register is provided by using bits 7:5 of the command byte, to index from byte 0 (000 b) to byte 7 (111) as the first byte to be presented on MISO.

Example: If command byte [7:0] = 011_1_000_0 indicates a read offset of 3 (4th byte) in the register to be accessed (register 6 in this example). The hardware RACK signal is provided by the MISO line when the read data is ready to be read by the master. The following shows a timing example.

$\overline{SS}$ ----------_____----------

MOSI XXXXXXXX_01110010_00000110_XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX

MISO XXXXXXXX_XXXXXXXX_00000000_00000001_b7.....b0_b7.....b0_XXXXXXXX

Write operations are identical in fast and normal SPI mode.

EEPROM Port

The EEPROM port enables the chip to download register programming instruction from an external low cost serial EEPROM, (such as 93C46). For each programming instruction fetched from the EEPROM, the instruction is executed immediately for the particular register. A predefined magic code is expected as the first data entity (header) of the EEPROM. The EEPROM should be configured to x16 word format. The header contains a key and length information as in Table 2. The actual data stored in EEPROM is byte-swapped as shown in Table 3.

- Upper 9 bits are magic code 1AAh, which indicates that valid data follows.
- Bit 6 is for speed indication. A 0 indicates normal speed. A 1 indicates speed up. Default is 0.
- Lower 6 bits indicate the total length of all entries.

Example: In a 93C46 only up to 64 words are allowed.

Table 2: EEPROM Header Format

15:8	*7*	*6*	*5:0*
Magic code, AAh	Magic code, 1	Speed	Total Entry Number

Table 3: EEPROM Contents

7	*6*	*5:0*	*15:8*
Magic code, 1	Speed	Total Entry Number	Magic code, AAh

After chip initialization, the header is read from the EEPROM and used to compare to the predefined magic code. When the fetched data does not match the predefined magic code, the EEPROM instruction fetch process is stopped. If the magic code is matched, fetching instructions continue until the instruction length is defined in the HEADER.

The EEPROM Port shares pins with the SMP port. Either the SPI port or the EEPROM can be selected by using the strap pin, CPU_EEPROM_SEL. The register space for the EEPROM port is the same as for the SMP port.

For more details on EEPROM data format, ask your local Broadcom FAE for the *EEPROM Programming Guide*.

Address Management

The BCM5338M Address Resolution Logic contains the following features:

- The two-bin per bucket address table configuration
- Hashing of the MAC address and VID (if 802.1Q is enabled) to generate the address table pointer
- Generation of a learn massage to the expansion port for address coherency across multiple BCM5338M devices

The address management unit of the BCM5338M provides packet rate learning and recognition functions. The address table supports 4K unicast and multicast addresses in the 256 KB on-chip memory. Although the address table shares the packet buffer memory, adequate memory bandwidth is provided for both functions to operate at maximum packet rate.

Address Table Organization

The address table is in the bottom of the internal SRAM, occupying the address range from 7000 to 7FFF. Each bucket contains two entries (or bins). The address table is organized into 2K buckets with two entries in each bucket. This allows up to two MAC addresses with the same index bits to be mapped into the address table.

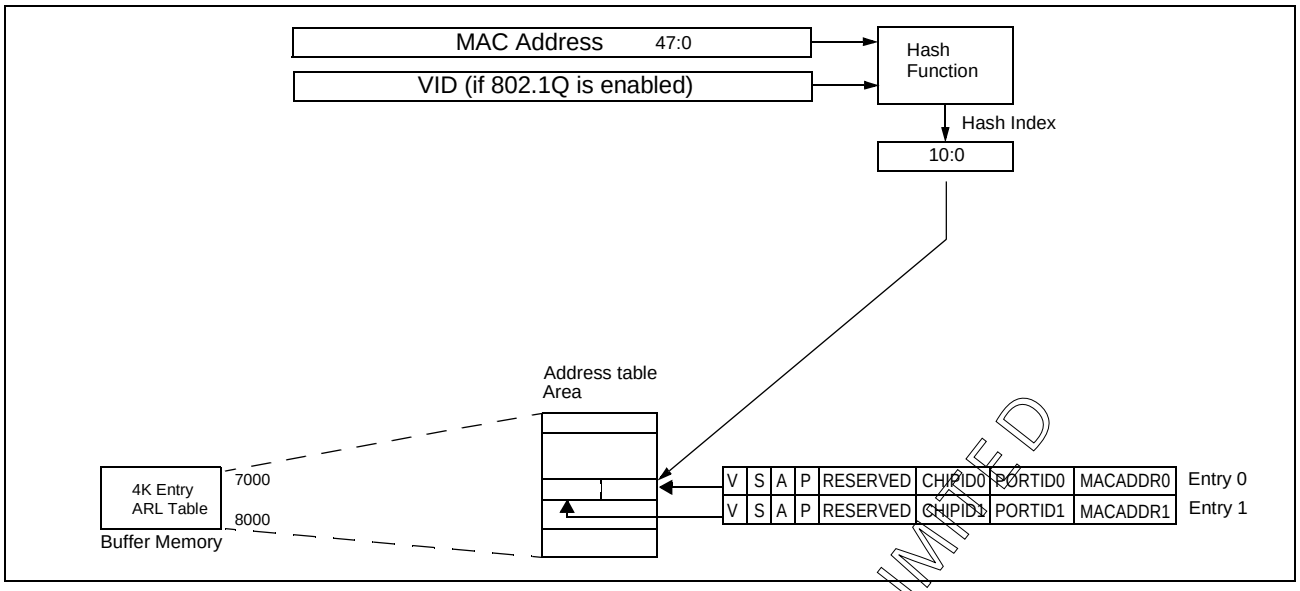


Figure 8: Mode Address Table Organization

The index into the address table is computed from the MAC address and VID (if 802.1Q is enabled) using a hash algorithm. The hash algorithm uses the CRC-CCITT polynomial. The 48-bit MAC address and VID (if 802.1Q is enabled) is reduced to a 16-bit CRC hash value. Bits 10:0 of the CRC hash value are used to index the 4K address table.

The CRC-CCITT polynomial is:
$x^{16}+x^{12}+x^{5}+1$

Hashing can be disabled by setting HASH_DISABLE = 1 in the ARL Configuration register, in which case the BCM5338M device reverts to the direct addressing method.

Address Table Entry

See the definition of the Table 74 on page 132 for details of how to read/write the ARL table entries. Table 4 indicates the fields contained in each address table entry.

Table 4: Address Table Entry

Bits	*Field*	*Description*
Unicast		
74:64	VLAN_ID[11:1]	–
63	Valid	1 = Indicates entry is valid. 0 = Indicates entry is empty.
62	Static	1 = Indicates entry is static and is administrated by software. 0 = Indicates entry is dynamic learned, aged, updated, and deleted.

Table 4: Address Table Entry (Cont.)

Bits	Field	Description
61	Age	1 = Indicates entry has been accessed or learned since last aging process. 0 = Indicates entry has not been accessed since last aging process.
60:59	Priority	11 = Priority 3. 10 = Priority 2. 01 = Priority 1. 00 = Priority 0.
58	VLAN_ID[0]	–
57	Disable_Learning_PKT R/W	Set to indicate that the device should not send out an ARL packet across the expansion bus. Must be set if the STATIC bit is set.
56:54	Reserved	000. ***Note:*** In Version A2 silicon, bits 56:54 can be programmed with any proprietary bits the customer wishes to store with the Unicast MAC Address.
53:52	CHIP ID	Device ID.
51:48	Port ID	Port Identifier. Stores the port association of the MAC address.
47:0	MAC Address	48-bit MAC address.
Multicast: New Control register (page 00h, offset 21h), bit 1 must be set to 1		
74:64	VLAN_ID[11:1]	–
63	Valid	1 = Indicates entry is valid. 0 = Indicates entry is empty.
62	Static	1 = Indicates entry is static and is administrated by software. 0 = Indicates entry is dynamic learned, aged, updated, and deleted.
61	CPU	1 = CPU is part of multicast group.
60:59	Priority	11 = Priority 3. 10 = Priority 2. 01 = Priority 1. 00 = Priority 0.
58:48	Multicast map	Exp, MII, P7, P6, P5, P4, P3, P2, P1, P0.
47:0	MAC Address	48-bit MAC address.

Address table entries are accessed by one of two mechanisms. The first is the ARL Read Write Control, which allows both bins in an address bucket location to be read, modified and/or written, based on the value of a known MAC address. The ARL Read Write Control mechanism is used to interrogate the ARL when a MAC address is known, such as writing a Static MAC address entries into the table. The MAC address is written to the "MAC Address Index Register" on page 133, the "ARL Read/Write Control Register" on page 133 is set up to perform either a read or write operation, and the Start bit is set, which is cleared when the operation has been performed. The known MAC address is used to calculate the index into the address table, based on whether hashing is enabled or not, and reads/writes both of the bins in the address bucket. The "ARL Entry 0

Register" on page 134 and "ARL Entry 1 Register" on page 136 are used to store the contents of the entry after a read or before a write. These contain the full 75-bit ARL bin entry as defined in Table 4 on page 40. It is important that in general, except after power-up before any addresses have been learnt, that a read of the address table is performed prior to a write. Since both bins in the bucket are read/write, writing to a bucket with only one bin valid still overwrites the other bin location with whatever data is residual in the ARL Entry 0/1 register. In the case of an operating switch, this may lead to a valid entry being deleted from the table.

The second mechanism to access the ARL is the ARL Search Control. The ARL Search Control is used to search the entire ARL in order to determine which MAC addresses have been learned, which port they reside on, and what their state is. The "ARL Search Control Register" on page 138 is used to (re)start the search from the top of the ARL, using the Start bit, which is cleared when the entire ARL has been searched. The ARL_SR_VALID bit indicates a search result is valid, and the "ARL Search Result Register" on page 139 contains the next 75-bit entry that was found to be in use and was retrieved from the address table. When the host reads the contents of the ARL Search Result register, the search process automatically continues to seek the next used entry in the address table. Address entries in the table that are not in use are skipped, providing the host with a very simple and effective way of searching the entire address table.

The ARL Search and ARL Read/Write operations can execute in parallel with other accesses to the BCM5338M registers. This allows the host processor to start a read, write, or search process, and then read/write other registers on the part, returning periodically to see if the operation has completed, using the relevant control register. A new ARL access or search should not be started until the current cycle is complete, although it is permissible to restart the search from the top of the ARL space at any point the ARL_SR_VALID bit is set.

Reserved Addresses

The BCM5338M treats certain 802.1 administered reserved multicast destination addresses in specific ways, dependent on the mode of operation. Table 5 defines the response to these reserved multicast addresses.

Table 5: Behavior for Reserved Multicast Addresses

MAC Address	*Function*	*802.1 Specified Action*	*Unmanaged Mode Action (Note 1)*	*Managed Mode Action*
01-80-C2-00-00-00	Bridge group address	Drop frame	Forward frame	Forward frame to frame management port only (Note 2).
01-80-C2-00-00-01	IEEE Std 802.3x MAC control frame	Drop frame	Receive MAC determines if valid PAUSE frame and acts accordingly	Receive MAC determines if valid PAUSE frame and acts accordingly.
01-80-C2-00-00-02	Reserved	Drop frame	Drop frame	Forward frame to management port only.
01-80-C2-00-00-03	Reserved	Drop frame	Drop frame	Forward frame to management port only.
01-80-C2-00-00-04	Reserved	Drop frame	Drop frame	Forward frame to management port only.
01-80-C2-00-00-05	Reserved	Drop frame	Drop frame	Forward frame to management port only.
01-80-C2-00-00-06	Reserved	Drop frame	Drop frame	Forward frame to management port only.
01-80-C2-00-00-07	Reserved	Drop frame	Drop frame	Forward frame to management port only.
01-80-C2-00-00-08	Reserved	Drop frame	Drop frame	Forward frame to management port only.
01-80-C2-00-00-09	Reserved	Drop frame	Drop frame	Forward frame to management port only.
01-80-C2-00-00-0A	Reserved	Drop frame	Drop frame	Forward frame to management port only.
01-80-C2-00-00-0B	Reserved	Drop frame	Drop frame	Forward frame to management port only.
01-80-C2-00-00-0C	Reserved	Drop frame	Drop frame	Forward frame to management port only.
01-80-C2-00-00-0D	Reserved	Drop frame	Drop frame	Forward frame to management port only.
01-80-C2-00-00-0E	Reserved	Drop frame	Drop frame	Forward frame to management port only.
01-80-C2-00-00-0F	Reserved	Drop frame	Drop frame	Forward frame to management port only.
01-80-C2-00-00-10	All LANs bridge management group address	Forward frame	Forward frame	Forward frame to all ports including frame management port.
01-80-C2-00-00-20	GMRP address	Forward frame	Forward frame	Forward frame to all ports except frame management port (Note 3).
01-80-C2-00-00-21	GVRP address	Forward frame	Forward frame	Forward frame to all ports except frame management port (Note 3).
01-80-C2-00-00-22	Reserved	Forward frame	Forward frame	Forward frame to all ports except frame management port.

Table 5: Behavior for Reserved Multicast Addresses (Cont.)

MAC Address	Function	802.1 Specified Action	Unmanaged Mode Action (Note 1)	Managed Mode Action
01-80-C2-00-00-23	Reserved	Forward frame	Forward frame	Forward frame to all ports except frame management port.
01-80-C2-00-00-24	Reserved	Forward frame	Forward frame	Forward frame to all ports except frame management port.
01-80-C2-00-00-25	Reserved	Forward frame	Forward frame	Forward frame to all ports except frame management port.
01-80-C2-00-00-26	Reserved	Forward frame	Forward frame	Forward frame to all ports except frame management port.
01-80-C2-00-00-27	Reserved	Forward frame	Forward frame	Forward frame to all ports except frame management port.
01-80-C2-00-00-28	Reserved	Forward frame	Forward frame	Forward frame to all ports except frame management port.
01-80-C2-00-00-29	Reserved	Forward frame	Forward frame	Forward frame to all ports except frame management port.
01-80-C2-00-00-2A	Reserved	Forward frame	Forward frame	Forward frame to all ports except frame management port.
01-80-C2-00-00-2B	Reserved	Forward frame	Forward frame	Forward frame to all ports except frame management port.
01-80-C2-00-00-2C	Reserved	Forward frame	Forward frame	Forward frame to all ports except frame management port.
01-80-C2-00-00-2D	Reserved	Forward frame	Forward frame	Forward frame to all ports except frame management port.
01-80-C2-00-00-2E	Reserved	Forward frame	Forward frame	Forward frame to all ports except frame management port.
01-80-C2-00-00-2F	Reserved	Forward frame	Forward frame	Forward frame to all ports except frame management port.

Notes:

1 Unmanaged mode disables the frame management port option. Neither the SMP nor the IMP receives frame data when in this mode. The MII port is treated as a normal network port and has frames forwarded to it in accordance with the entries in the address table.

2 Frames with the reserved multicast address corresponding to the Bridge Group Address (01-80-C2-00-00-00) are forwarded to the programmed frame management port based on the contents of the BPDU Multicast Address register (in the ARL Control register page). Changing this register from the default value causes frames with the new address to be forwarded to the frame management port, and BPDUs are flooded to all ports except the frame management port.

3 Frames with the reserved multicast address corresponding to the GMRP or GVRP Addresses (01-80-C2-00-00-20 or 01-80-C2-00-00-21) are forwarded to all ports except the source and frame management ports. If the switch product implements either of these protocols, the BCM5338M should be programmed to use the managed mode, and the frames are forwarded to the management port.

Learning

During the receive process, the source address (SA) of the packet is saved until completion of the packet. The address is stored in the address table memory if the following conditions are met:

- The packet is not from the Management port.
- The packet has been received without error.
- The packet is of legal length.
- The packet has a unicast address.
- There is a free space available in one of the two entries (STATIC=0 and VALID=0) in the bucket that the hashed address indexes to. If there is no free space available in the bucket, the address is not learned.

When learning, the MAC address, VID, and the source port ID are stored into the address table. The VALID bit is set, the AGE bit is set, and the STATIC bit is reset in the entry.

The BCM5338M incorporates signaling between devices, using the expansion port, which assists coherency between the ARL tables in separate chips. When a new address is learned, a 4-word x 32-bit message is constructed, which contains the newly learned 48-bit MAC address, prepended by a 16-bit header field which includes the source port ID where the new address was learned. This message is passed on the expansion port to each device before being deleted.

Static Address

The BCM5338M supports static filtering entries that are created and updated by software through the SMP. Bridge management software can create these entries by directly writing the entry location of the buffer memory and setting the STATIC bit of the entry. Static entries do not have new MAC addresses or port associations learned automatically and are not aged out by the automatic internal aging process. For details of how ARL entries are read, stored, and written, see “ARL Read/Write Control Register” on page 133.

For instance, addresses associated with a switch’s network ports and the management port should be instantiated as Static entries in the address table by the management processor, with the source port ID and as the physical management port (in the “Global Management Configuration Register” on page 119).

Resolution

The destination address (DA) of the received packet is used by the address resolution function to search the address table and assign a destination port for the packet. The destination port is assigned by locating a matching address in the address table and selecting the source port identifier field as the destination port. The search for a matching address occurs only for unicast packets. The address resolution function for unicast packets proceeds as follows:

- The hash of the MAC address (and VID if 802.1Q is enabled) is used as a pointer into the address table memory and both entries in the bucket are retrieved. The address resolution logic processes the two entries in parallel.
- If the valid indicator is set and the address stored at one of the locations matches the DA of the packet received, the port identifier is assigned to be the destination port of the packet.
- If the destination port matches the source port, the packet is not forwarded.
- If the valid indicator is not set or the address stored does not match the DA address of the packet, the packet is forwarded as a broadcast packet and transmitted to all other ports.

If SW_FWDG_MODE is Unmanaged, packets with the group address bit set in the DA are handled as follows:

- If the DA matches the globally assigned multicast address of the 802.3x MAC Control PAUSE frame of 01-80-C2-00-00-01, the packet is not forwarded.
- If the DA matches the Bridge Group Address, the packet is forwarded to all ports except the source port.
- If the DA matches one of the other globally assigned reserved address (between 01-80-C2-00-00-02 and 01-80-C2-00-00-0F), the packet is not forwarded.
- All other multicast and broadcast packets are forwarded to all ports except the source port and the management port.

If SW_FWDG_MODE is Managed, packets with the group address bit set in the DA are handled as follows:

- If the DA matches the globally assigned multicast address of the 802.3x MAC control PAUSE frame of 01-80-C2-00-00-01, the packet is not forwarded.
- If the DA matches one of the globally assigned reserved address (between 01-80-C2-00-00-00 and 01-80-C2-00-00-0F excluding 802.3x MAC Control PAUSE frame address), the packet is forwarded to the Management port.
- If the DA matches the GARP addresses of 01-80-C2-00-00-20 to 01-80-C2-00-00-2F, the packet is forwarded to the management port.
- All other multicast and broadcast packets are forwarded to all ports except the source port. The management port can selectively have broadcast packets and/or multicast packets individually disabled based on the RX_MCST_DISABLE and RX_BCST_DISABLE bits in the "MII/IMP Port Control Register [8]" on page 108 for the SMP or IMP (MII). If 802.1Q is enabled, flooding is limited to the particular VLAN domain.

Aging

For both ARL modes, the Aging process periodically removes dynamically learned addresses. The AGE_TIME is a programmable timer with a default value of 300s. Aging can be disabled by setting the AGE_TIME = 0, in which case no entries are aged from the table. For each entry in the Address Table, the Aging process performs the following if the VALID bit is:

- Not set—do nothing.
- Set and the STATIC is set—do nothing.
- Set, the STATIC bit is not set, and the AGE bit is set—reset the AGE bit. This keeps the entry in the table.
- Set, the STATIC bit is not set, and the AGE bit is reset—reset the VALID bit. This effectively deletes the entry from the Address table.

Aging can be enabled on a per port or per Spanning Tree basis using Table 189 on page 207.

Static or Fast Aging can be enabled per Table 184 on page 205 through Table 188 on page 207.

Hash Function

The address resolution logic incorporates a hash function to randomize storage location for the MAC address. The hash function can be disabled using the HASH_DISABLE bit in the "Switch Mode Register" on page 110.

ARL Miss Options

When ARL miss occurs, the BCM5338M allows the user to program two registers to decide what to do with this ARL missed packet:

- MLF_FWD_MAP[10:0] (page:00h,addr:2Ah-2Bh) is for Multicast packet.
- ULF_FWD_MAP[10:0] (page:00h,addr: 28H-29h) is for unicast packet.

When a unicast ARL miss occurs, the BCM5338M forwards it according to the ULF_FWD_MAP value (bit = 1 means forward, bit = 0 means drop) based on the value of bit 6 of the Table 28 on page 112. When a Multicast ARL miss occurs, the BCM5338M forwards it according to the MLF_FWD_MAP value (bit = 1 means forward, bit = 0 means drop) based on the value of bit 7 in Table 28 on page 112.

Bridge Management

To support bridge management, the BCM5338M provides the following services:

- Bridge Management state register access through the CPU interface
- Bridge Protocol Data Unit (BPDU) frame forwarding through the CPU interface or the MII interface

Spanning Tree Port State

The BCM5338M device supports the Spanning Tree Protocol (STP) by providing the spanning tree state in the Port Control register for each of the nine network ports.

Each Port Control Register (PCR) contains 3 bits dedicated to STP state (STP_STATE[2:0]) as well as additional bits to control the operation of the MAC port.

In the unmanaged compatible mode of operation (SW_FWDG_MODE = Unmanaged), the default state of the STP_STATE[2:0] bits are all 0s, and no spanning tree state is maintained. Write operations to the spanning tree state bits are ignored. Frames are forwarded based only on their DA. Known unicast address frames are forwarded to their single defined destination port, and unknown unicast, as well as all multicast/broadcast addressed frames, are flooded to all ports, with the exception of the management port, providing SW_FWDG_EN = 1. BPDU frames, are one of the 802.1 reserved multicast addresses that the unmanaged mode floods. For a complete list of the forwarding behavior of the unmanaged address resolution logic, see Table 5 on page 43.

In the BCM5338M mode of operation (SW_FWDG_MODE = Managed), all ports are considered network ports and can have STP port state associated with them, these being the following:

- Eight integral 10/100BASE-T ports
- The MII port

The SMP has no STP state associated with it. The MII port, when configured as the in-band management port (IMP), also has no STP state associated with it. The expansion port never has any STP state associated with it. The BCM5338M reacts to the STP state bits as written by the management CPU, as follows (providing SW_FWDG_EN = 1):

Disable

In this state, all frames received by the port are discarded. The port also does not forward any transmit frames, queued by either BCM5338M receive network ports, or frames cast by the management entity via the SMP or IMP. Addresses are not learned by ports in the Disabled state. This is the default state that the BCM5338M powers up in when SW_FWDG_MODE = Managed.

Blocking

In this state, the MAC port forwards received BPDUs to the designated Management port (SMP or IMP). All other frames received by the port are discarded and the addresses are not learned. The port also does not forward any transmit frames, queued by other BCM5338M receive network ports.

Listening

In this state, the MAC port forwards received BPDUs to the designated Management port (SMP or IMP). All other frames received by the port are discarded and the addresses are not learned. The port also does not forward any transmit frames, queued by other BCM5338M receive network ports, but transmits frames cast by the management entity via the MSP or IMP, as expected (such as BPDUs). The Learning and Listening states of all BCM5338M ports are identical. The external management processor running the STP algorithm must distinguish these two states using the STP algorithm, and is able to store the learning and listening state information into the BCM5338M for consistency.

Learning

In this state, the MAC port forwards received BPDUs to the Management port, transmits BPDUs sent into the Management port, and does not learn incoming frames' MAC addresses. All other frames received by the port are discarded.

Forwarding

In this state, the MAC port forwards received BPDUs to the Management port, transmits BPDUs sent into the Management port, forwards all other frames, and learns all in coming frames' MAC addresses.

Table 6: Multiple Spanning Tree State

Spanning Tree State	*Receive BPDU*	*Transmit BPDU*	*Normal Frame*	*Address Learning*	*STP_State*
No Spanning Tree or Spanning Tree Disable	Treated as Multicast	Flood to all ports	Forward	Learn	11 + Global flag
Disable State	Disabled	Disabled	Don't Forward	Don't Learn	00
Blocking State	Forward to Management	Disabled	Don't Forward	Don't Learn	01
Listening State	Forward to Management	Enabled	Don't Forward	Don't Learn	10
Learning State	Forward to Management	Enabled	Don't Forward	Don't Learn	10
Forwarding State	Forward to Management	Enabled	Forward	Learn	11

The Multiple Spanning Tree Protocol (MSTP) enables VLANs to be grouped into a spanning-tree instance, provides for multiple forwarding paths for data traffic, and enables load balancing. It improves the fault tolerance of the network because a failure in one instance (forwarding path) does not affect other instances (forwarding paths). The most common initial deployment of MSTP and RSTP is in the backbone and distribution layers of a Layer 2 switched network; this deployment provides the highly-available network required in a service-provider environment. Both RSTP and MSTP improve the operation of the spanning tree while maintaining backward compatibility with equipment that is based on the (original) 802.1D spanning tree. The BCM5338M can support up to 32 Spanning Trees.

To support the multiple spanning tree protocol, each spanning tree needs a different status (i.e., Disable, Block, Listen/learn, and forward) for each switch port.

The BCM5338M supports up to 32 spanning trees, so it has 32 Spanning Tree Status registers. The BCM5338M also supports 4K VLANs. Each VLAN entry in the VLAN table has a spanning_tree_ID field to indicate the spanning tree status.

To enable multiple spanning trees, complete the following steps:

1. Enable 802_1s by setting Table 183 on page 204 bit[2] = 1.
2. Set up the VLAN table. Each VID in the VLAN table needs a spanning tree ID field assigned to a preferred spanning tree (defined in one of the MST Table registers, Page 43h).
3. Enable Global MST aging by setting the MST control register bit[1]=1.
4. Fill out per spanning tree port status.

There are 32 items in the Table 189 on page 207:

- bits[17:0] of each register are for {mii, port[7:0]}.
- The BCM5338M supports four spanning tree states internally (disable, block, listen/learn, and forward), so two bits are encoded for each spanning tree state.
- bit[18] = 1 enables per spanning tree aging on this spanning tree, so each spanning tree's aging can be turned on or off individually.

Note: When multiple spanning tree is disabled, the BCM5338M uses the old spanning tree status from Table 22 on page 108 and the Table 23 on page 108.

Management Frames

Management frames received by the BCM5338M are forwarded to the Bridge Management entity (an external CPU or microcontroller) either through the SMP or optionally through the MII Port. When the MII is used as the interface to the external management subsystem, the port is referred to as the in-band management port (IMP).

Note: When operating in the unmanaged mode, management frames are treated differently, as defined in Table 5 on page 43.

The following frames are forwarded to the Bridge Management entity in the BCM5338M mode:

- BPDU Frames—BPDUs are identified by the bridge group address (01-80-C2-00-00-00) in the destination address field of a frame. The STP_STATE bits in the "MII/IMP Port Control Register [8]" on page 108 must be configured to permit BPDU reception on a particular port. A BPDU received on such a port is forwarded with the Port ID of the receiving port to the port configured in the Management Port ID register.
- Reserved Multicast Addressed Frames—Frames with 802.1 administered reserved multicast addresses (between 01-80-C2-00-00-02 and 01-80-C2-00-00-0F in their DA field are forwarded only to the management port, with a header which includes the Port ID of the port from which the frame was received. Frames with the All LANs bridge management group address (01-80-C2-00-00-10) as the DA are forwarded to all ports, with the management port again receiving the header information to identify the

Port ID from which the frame was received.

- Directed Management Agent Frames—Packets with the DA equal to one of the MAC addresses associated with the management port. These addresses are generally entered as Static addresses by the management entity itself.
- Mirrored Frames—Ingress or egress port frames that have been assigned to be mirrored to the management port.

To transmit a frame from the management port, the management agent is responsible to encapsulate the actual management frame which is transmitted in its entirety, within an additional header and FCS field. The definition of this frame format is defined in Figure 14 on page 63. The resolution rules for transmitted management frames are as follows if the header OPCODE (see Table 11 on page 64) indicates that the frame is:

- A Normal unicast or multicast address, then the frame is forwarded according to the address table resolution. Frames with broadcast addresses or multicast addresses not found in the address table are flooded to all ports.
- An Egress Directed frame, then the frame is forwarded to the Port ID identified in the header.

Switch Controller

The core of the BCM5338M device is a cost-effective and high-performance switch controller. The controller manages packet forwarding between the MAC receive and transmit ports through the frame buffer memory with a store and forward architecture. The switch controller encompasses the functions of buffer management, memory arbitration, and transmit descriptor queueing.

Buffer Management

The frame buffer memory is divided into 256 bytes per page. Each packet received may allocated more than one page, of which, six pages are required for storing maximum 1536B frame data. Frame data is stored to the memory block as the packet is received. After reception, the frame is queued to the egress port(s) transmit queue. For unicast frames, following transmission of a packet from the frame buffer memory, the block of memory for the frame is released to the free buffer pool. If the frame is destined to multiple ports, the memory block is not released until all ports complete transmission of the frame.

Memory Arbitration

Processes requesting access to the internal memory include the receive and transmit frame data handlers, address resolution, learning and aging functions, and output port queue managers. These processes are arbitrated to provide fair access to the memory and minimize latency of critical processes to provide a completely non-blocking solution.

Transmit Output Port Queues

When the Quality of Service (QoS) function is turned off, the switch controller maintains an output port queue for each port. The queues are located in the internal memory, and the maximum depth of the queue is 512 (512 transmit descriptors). The queue depth becomes smaller for each output port when the QoS function is on. Transmit descriptors are updated after the packet has been received and the destination port resolved. One or two transmit descriptors are assigned to each destination port queue linking the destination with the frame data. Packets that have frame sizes larger than 512 bytes require two transmit descriptors. In the case of multicast and broadcast packets, a transmit descriptor for the packet is assigned to the transmit descriptor queues of multiple ports.

For each port, frames are initiated for transmission with minimum IPG until the transmit descriptor queue of the port is empty.

When the QoS is turned on, the single queue is split into four different-sized priority queues. These four queues are maintained by the switch controller for each transmit port. The weighted fair scheduling is applied to the queues to select frames from all queues and prevent starvation.

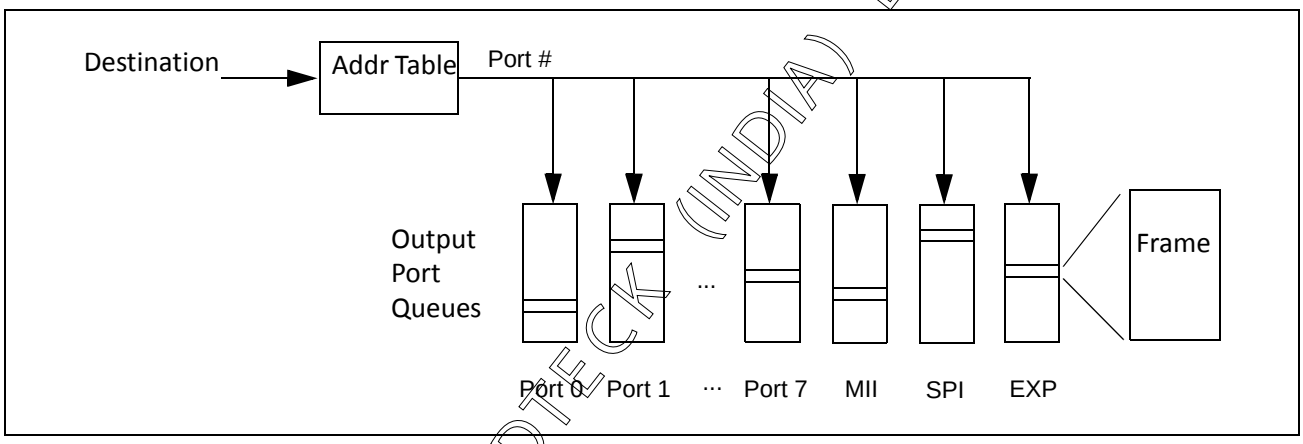


Figure 9: Transmit Output Queues

Integrated High-Performance Memory

The BCM5338M includes 256 KB of integrated, high-performance RAM, which stores all packet buffer and address table information and eliminates the need for external memory. This allows for the implementation of extremely low-cost systems.

The internal RAM controller efficiently executes memory transfers and achieves non-blocking performance for up to 24 port applications.

The internal memory is configured to 64-bit data words. All accesses to the memory are 64-bit aligned. The BCM5338M performs a memory test at power-on.

Clocking

The BCM5338M provides simple clock selection. From a single 25 MHz clock input, the device's internal clocks operate at 83 MHz/91 MHz/100 MHz depending on EXPFREQ[1:0]; this affects the operation of the system logic, internal RAM, and expansion port. This option allows for the best trade-offs with respect to performance, cost, and power.

MIB Engine

The MIB Engine is responsible for processing status words received from each port. Based on whether it is a receive status or transmit status, appropriate MIB counters are updated. The BCM5338M implements 35 MIB counters on a per port basis. MIB counters can be categorized into three groups:

- Receive Only Counters
- Transmit Only Counters
- Receive or Transmit Counters

This latter group can as a group be selectively steered to the receive or transmit process on a per port basis. The section below describes each individual counter.

MIB Counters Per Port

Table 7: MIB Counters

Counters	*Description of Counter*
Receive Only Counters (16)	
RxDropPkts (32-bit)	The number of good packets (received by a port) that were dropped due to lack of resources (lack of input buffers) or due to lack of resources before a determination of the validity of the packet was made (e.g., receive FIFO overflow). The counter is only incremented if the receive error was not counted by either the RxExcessSizeDisc, the RxAlignmentErrors, or the RxFCSErrors counters.
RxOctets (64-bit)	The number of bytes of data received by a port (excluding preamble but including FCS), including bad packets.
RxBroadcastPkts (32-bit)	The number of good packets (received by a port) that are directed to the broadcast address. This counter does not include errored broadcast packets or valid multicast packets.
RxMulticastPkts (32-bit)	The number of good packets received by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.
RxSAChanges (32-bit)	The number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater based network.
RxUndersizePkts (32-bit)	The number of good packets received by a port that are less than 64 bytes long (excluding framing bits but including the FCS).

Table 7: MIB Counters (Cont.)

Counters	*Description of Counter*
RxOversizePkts (32-bit)	The number of good packets received by a port that are greater than 1522 bytes inclusive (excluding framing bits but including the FCS). ***Note:*** This counter alone is incremented for packets in the range 1523-1536 bytes inclusive, whereas both this counter and the RxExcessSizeDisc counter are incremented for packets of 1537 bytes and higher.
RxFragments (32-bit)	The number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error.
RxJabbers (32-bit)	The number of packets received by a port that are longer than 1522 bytes and have either an FCS error or an alignment error.
RxUnicastPkts (32-bit)	The number of good packets received by a port that are addressed to a unicast address.
RxAlignmentErrors (32-bit)	The number of packets received by a port that have a length (excluding framing bits but including FCS) between 64 and 1522 bytes, inclusive, and have a bad FCS with a non-integral number of bytes.
RxFCSErrors (32-bit)	The number of packets received by a port that have a length (excluding framing bits but including FCS) between 64 and 1522 bytes inclusive, and have a bad FCS with an integral number of bytes.
RxGoodOctets (64-bit)	The total number of bytes in all good packets received by a port (excluding framing bits but including FCS).
RxExcessSizeDisc (32-bit)	The number of good packets received by a port that are greater than 1536 bytes (excluding framing bits but including the FCS) and were discarded due to excessive length. ***Note:*** The RxOversizePkts counter alone is incremented for packets in the range 1523-1536 bytes inclusive, whereas both this counter and the RxOversizePkts counter are incremented for packets of 1537 bytes and higher.
RxPausePkts (32-bit)	The number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC Control Frame EtherType field (88-08h), have a destination MAC address of either the MAC Control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE Opcode (00-01), be a minimum of 64 bytes in length (excluding preamble but including FCS), and have a valid CRC. Although an 802.3 compliant MAC is only permitted to transmit PAUSE frames when in Full-duplex mode, with flow control enabled, and with the transfer of PAUSE frames determined by the result of auto-negotiation, an 802.3 MAC receiver is required to count all received PAUSE frames, regardless of its half/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a non-compliant transmitting device on the network.
RxSymbolErrors (32-bit)	The total number of times a valid length packet was received at a port and at least one invalid data symbol was detected. Counter only increment once per carrier event and does not increment on detection of collision during the carrier event.
RxQoSQPkt (32-bit)	The total number of good packets received in any priority, which is specified in MIB Queue Select register when QoS is enabled.
RxQoSQOctet (64-bit)	The total number of good bytes received in any priority, which is specified in MIB Queue Select register when QoS is enabled.
Transmit Counters Only (13)	

Table 7: MIB Counters (Cont.)

Counters	*Description of Counter*
TxDropPkts (32-bit)	This counter is incremented every time a transmit packet is dropped due to lack of resources (e.g., transmit FIFO underflow), or an internal MAC sublayer transmit error not counted by.in either the TxLateCollision or the TxExcessiveCollision counters.
TxOctets (64-bit)	The total number of good bytes of data transmitted by a port (excluding preamble but including FCS).
TxBroadcastPkts (32-bit)	The number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include errored broadcast packets or valid multicast packets.
TxMulticastPkts (32-bit)	The number of good packets transmitted by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.
TxCollisions (32-bit)	The number of collisions experienced by a port during packet transmissions.
TxUnicastPkts (32-bit)	The number of good packets transmitted by a port that are addressed to a unicast address.
TxSingleCollision (32-bit)	The number of packets successfully transmitted by a port that experienced exactly one collision.
TxMultipleCollision (32-bit)	The number of packets successfully transmitted by a port that experienced more than one collision.
TxDeferredTransmit (32-bit)	The number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy.
TxLateCollision (32-bit)	The number of times that a collision is detected later than 512 bit-times into the transmission of a packet.
TxExcessiveCollision (32-bit)	The number of packets that are not transmitted from a port because the packet experienced 16 transmission attempts.
TxPausePkts (32-bit)	The number of PAUSE frames transmitted by a port. The MAC resolve to Full-duplex mode, with 802.3x flow control PAUSE frame exchange enabled at the completion of auto-negotiation.
TxFrameInDisc (32-bit)	The number of valid packets received which are discarded by the forwarding process due to lack of space on an output queue (i.e., not maintained or reported in the MIB counters). Located in the Congestion Management registers (Page 0Ah). This attribute only increments if a network device is not acting in compliance with a flow control request, or the BCM5338M internal flow control/buffering scheme has been misconfigured.
TxQoSQPkt (32-bit)	The total number of good packets transmitted on any queue, which is specified in MIB Queue Select register when QoS is enabled.
TxQoSQOctet (64-bit)	The total number of good bytes transmitted on any queue, which is specified in MIB Queue Select register when QoS is enabled.
Transmit or Receive Counters (6)	
Pkts64Octets (32-bit)	The number of packets (including error packets) that are 64 bytes long.
Pkts65to127Octets (32-bit)	The number of packets (including error packets) that are between 65 and 127 bytes long.
Pkts128to255Octets (32-bit)	The number of packets (including error packets) that are between 128 and 255 bytes long.

Table 7: MIB Counters (Cont.)

Counters	*Description of Counter*
Pkts256to511Octets (32-bit)	The number of packets (including error packets) that are between 256 and 511 bytes long.
Pkts512to1023Octets (32-bit)	The number of packets (including error packets) that are between 512 and 1023 bytes long.
Pkts1024to1522Octets (32-bit)	The number of packets (including error packets) that are between 1024 and 1522 bytes long.
Total Number of Counters Per Port: 35	

Table 8 identifies the mapping of the BCM5338M MIB counters and their generic mnemonics to the specific counters and mnemonics for each of the key IETF MIBs which are supported.

Note: This is defined where there is a direct mapping, but there are several additional statistics counters that are indirectly supported and make up the full complement of the counters required to fully support each MIB (shown in Table 9 on page 57).

Table 10 on page 57 identifies the additional counters supported by the BCM5338M and references the specific standard or reason for the inclusion of the counter.

Table 8: Directly Supported MIB Counters

MIB	*Ethernet-Like MIB RFC 1643*	*Bridge MIB RFC 1493*	*MIB II Interface RFC 1213/1573*	*RMON MIB RFC 1757*
RxDropPkts	dot3StatsInternalMACReceiveErrors	dot1dTpPortInDiscards	ifInDiscards	–
RxOctets	–	–	ifInOctets	etherStatsOctets
RxBroadcastPkts	–	–	ifInBroadcastPkts	etherStatsBroadcastPkts
RxMulticastPkts	–	–	ifInMulticastPkts	etherStatsMulticast Pkts
RxSAChanges	Note 2	Note 2	Note 2	Note 2
RxUndersizePkts	–	–	–	etherStatsUndersizePkts
RxOversizePkts	dot3StatsFrameTooLongs	–	–	etherStatsOverrsizePkts
RxFragments	–	–	–	eytherStatsFragments
RxJabbers	–	–	–	etherStatsJabbers
RxUnicastPkts	–	–	ifInUcastPkts	–
RxAlignmentErrors	dot3StatsAlignmentErrors	–	–	–
RxFCSErrors	dot3StatsFCSErrors	–	–	–
RxGoodOctets	–	–	–	–
RxExcessSizeDisc	Note 2	Note 2	Note 2	Note 2
RxPausePkts	Note 2	Note 2	Note 2	Note 2
RxSymbolErrors	Note 2	Note 2	Note 2	Note 2
Note 1	–	–	ifInErrors	–
Note 1	–	–	ifInUnknownProtos	–
Note 1	–	dot1dTpPortInFrames	–	–

Table 8: Directly Supported MIB Counters (Cont.)

MIB	Ethernet-Like MIB RFC 1643	Bridge MIB RFC 1493	MIB II Interface RFC 1213/1573	RMON MIB RFC 1757
TxDropPkts	dot3StatsInternalMACTransmit Errors	–	ifOutDiscards	–
TxOctets	–	–	ifOutOctets Note 3	–
Note 1	–	dot1dTpPortOutFrames	–	–
TxBroadcastPkts	–	–	ifOutBroadcastPkts	–
TxMulticastPkts	–	–	ifOutMulticastPkts	–
TxCollisions	–	–	–	etherStatsCollisions
TxUnicastPkts	–	–	ifOutUcastPkts	–
TxSingleCollision	dot3StatsSingle CollisionFrames	–	–	–
TxMultipleCollision	dot3StatsMultiple CollisionFrames	–	–	–
TxDeferredTransmit	dot3StatsDeferred Transmissions	–	–	–
TxLateCollision	dot3StatsLate Collision	–	–	–
TxExcessiveCollision	dot3StatsExcessive Collision	–	–	–
TxFrameInDisc	Note 2	Note 2	Note 2	Note 2
TxPausePkts	Note 2	Note 2	Note 2	Note 2
Note 4	dot3StatsCarrier SenseErrors	–	–	–
Note 1	–	–	ifOutErrors	–
Pkts64Octets	–	–	–	etherStatsPkt64 Octets
Pkts65to127Octets	–	–	–	etherStatsPkt65to127Octets
Pkts128to255Octets	–	–	–	etherStatsPkt128to255Octets
Pkts256to511Octets	–	–	–	etherStatsPkt256to511Octets
Pkts512to1023Octets	–	–	–	etherStatsPkt512to1023Octets
Pkts1024to1522Octets	–	–	–	etherStatsPkt1024to1522Octets
Note 1	–	–	–	etherStatsDrop Events
Note 1	–	–	–	etherStatsPkts
Note 1	–	–	–	etherStatsCRCAlignErrors
Note 4	dot3StatsSQETest Errors	–	–	–

Note 1: Derived by summing two or more of the supported counters. For specific details, see Table 9 on page 57.
Note 2: Extensions required by recent Standards developments or BCM5338M operation specifics.
Note 3: The MIB II Interfaces specification for ifOutOctets includes preamble/SFD and errored bytes. Because 802.3 compliant MACs have no requirement to keep track of the number of transmit bytes in an errored frame, this count is impossible to maintain. The TxOctets maintained by the BCM5338M are consistent with good bytes transmitted, excluding preamble but including FCS. The count can be adjusted to match more closely the ifOutOctets definition by adding the preamble for TxGoodPkts, and possibly an estimate of the octets involved in TxCollisions and TxLateCollision.
Note 4: The attributes TxCarrierSenseErrors and TxSQETestErrors are not supported in the BCM5338M. These attributes were originally defined to support coax-based AUI transceivers. The BCM5338M's integrated transceiver design means these error conditions are eliminated. MIBs intending to support such counters should return a value of zero or are not supported.

Table 9: Indirectly Supported MIB Counters

MIB	*Ethernet-Like MIB RFC 1643*	*Bridge MIB RFC 1493*	*MIB II Interface RFC 1213/1573*	*RMON MIB RFC 1757*
RxErrorPkts = RxAlignmentErrors + RxFCSErrors + RxFragments + RxOversizePkts + RxJabbers	–	–	ifInErrors	–
RxGoodPkts = RxUnicastPkts + RxMulticastPkts + RxBroadcastPkts	–	dot1dTpPortIn Frames	–	–
DropEvents = RxDropPkts + TxDropPkts	–	–	–	etherStatsDrop Events
RxTotalPkts = RxGoodPkts + RxErrorPkts	–	–	–	etherStatsPkts
RxCRCAlignErrors = RxCRCErrors + RxAlignmentErrors	–	–	–	etherStatsCRCAlignErrors
NA - 5318 cannot suffer this error - return as zero	dot3StatsSQETest Errors	–	–	–
RxFramesTooLong = RxOversizePkts + RxJabber	dot3StatsFrameTooLongs	–	–	–
TxGoodPkts = TxUnicastPkts + TxMulticastPkts + TxBroadcastPkts	–	dot1dTpPortOut Frames	–	–
TxErrorPkts = TxExcessiveCollision + TxLateCollision Note 1	–	–	ifOutErrors	–

Note 1: The number of packets transmitted from a port which experienced late collision, or excessive collision. While for some media types in half-duplex operation, frames that experience carrier sense errors are also summed in this counter, the BCM5338M's integrated design means this error condition is eliminated.

Table 10: Supported MIB Extensions

MIB	*Appropriate Standards Reference*
RxSAChanges	IEEE 802.3u Clause 30 - Repeater Port Managed Object Class — aSourceAddressChanges.
RxExcessSizeDisc	5318 Specific - The BCM5338M cannot store packets in excess of 1536 bytes (excluding preamble/SFD, but including FCS). This counter indicates packets that were discarded by the BCM5338M due to excessive length.
RxPausePkts	IEEE 802.3x Clause 30 - PAUSE Entity Managed Object Class — aPAUSEMACCtrlFramesReceived.

Table 10: Supported MIB Extensions (Cont.)

MIB	*Appropriate Standards Reference*
RxSymbolErrors	IEEE 802.3u Clause 30 - Repeater Port Managed Object Class —aSymbolErrorDuringPacket.
TxFrameInDisc	Internal diagnostic use for optimization of flow control and buffer allocation algorithm.
TxPausePkts	IEEE 802.3x Clause 30 - PAUSE Entity Managed Object Class —aPAUSEMACCtrlFramesTransmitted.

MIB Autocast

The BCM5338M supports a unique MIB autocast feature that allows a low-cost manageable switch to be constructed either without any additional CPU requirement, or with a very minimal microcontroller. When this feature is configured, the BCM5338M routinely packs the MIB statistics counters from each port into a legal Ethernet frame, and autocasts these frames to a configurable number of ports on the device. Using this feature, an external entity can capture these frames and use them in any way to monitor the performance of the switch and/or network.

Using MIB Autocast, management information is conveyed with no impact on the system cost of the switch, using the existing in-band network. The MIB Autocast frames can be captured and processed, stored, or analyzed as a background activity in any of the existing network nodes.

The format of the MIB Autocast transmit frame is shown in Figure 10. The BCM5338M allows complete flexibility of the frame header, including the DA and SA fields, the Type field, and any additional protocol header fields that are required to ensure delivery of the frame to the preferred end station (i.e., routing information). See the definitions in the Management Mode registers and the MIB Autocast registers for an explanation of the default and programmable parameters for MIB Autocast.

Destination Address (from MIB Autocast DA register)	Source Address (from MIB Autocast SA register	Type 8874h (from MIB Autocast Typeregister)	OPCODE (Tx MIB Autocast)	Port Number	Port State	MIB Statistic 1	MIB Statistic 2	MIB Statistic 3	MIB Statistic 35	FCS

Figure 10: Transmit MIB Autocast Frame Format

The MIB Autocast mechanism can be configured to forward to any port or port group. This includes the ability to cast frames only at the local CPU, attached via the management port of choice. This can be used to offload routine processor reads on the MIB registers.

Note: For details in MIB Autocast setup, refer to the *BCM5308M/BCM531X/BCM532X 10/100BASE-T/TX Managed Switches Technical Information* document (5308M_531X_532XTI1XX-R).

Access of the MIB counters via the SPI interface does not work correctly when MIB Autocast is enabled.

MII Port

The BCM5338M provides a fully 802.3u compatible MII interface as an additional network port. The port can be configured to operate differently dependent on the programming of the internal registers.

MII MAC Port

In its default mode after power-up, the MII operates as a normal MAC-based MII port, capable of interfacing directly to an external TX or FX transceiver. The port incorporates a ninth internal MAC and functions identically to the integrated 10/100 ports. Frames are forwarded to the port under control of the forwarding model defined in Table 5 on page 43, dependent on the state of the SW_FWDG_MODE bit in the "Switch Mode Register" on page 110, and dependent on the state of the frame management port in the "Global Management Configuration Register" on page 119.

Predecessors of the BCM5338M device allowed the MII management signals (MDC/MDIO) to interrogate the internal MII registers associated with the integrated 10/100 Mbps PHYs. The BCM5338M can still support this mode, in which case configuration of the integrated PHYs requires the 2.5 MHz clock to be supplied to the BCM5338M MDC pin and any external MII-connected transceiver, and the external management device controls MDIO to select and configure all the PHYs appropriately. To operate in this mode, the external transceiver needs to support some signals in addition to the standard MII signals, so that the state of the external transceiver can be monitored by the BCM5338M. Individual active-low Link, Speed (100 Mbps), Duplex, and link partner Flow Control mode signals from the transceiver should be provided. An MII-based single 10/100 Mbps PHY, such as the BCM5202, provides these additional signals. With these additional signals, the BCM5338M generates port LEDs for the external MII-based PHY, equivalent to the LEDs of the internal transceivers.

The more typical use of the MII in a BCM5338M implementation is that the device is managed via the SMP. In this case, on sensing activity of the SMP, the BCM5338M takes control of the MII management pins and sources the 2.5 MHz clock signal for MDC. The external PHY can be accessed by the management entity, since its MII registers are aliased to the Port 8 MII registers (Page 18h). Access to MII registers in this page in the register map automatically generates an MDIO/MDC request to the external MII-based transceiver, allowing configuration control and status monitoring of the off-chip PHY port. The MII port uses the unique PHY address of A#A#_000, where A#A# is the bit inversion of the CHIP ID[1:0] bits. So the MII PHY address for CHIP ID[1:0] = 01 would be 10_000. The external PHY must be programmed/strapped to respond to the CHIP ID dependent PHY address. See Table 16 on page 86 in the MII Management section for additional detail on internal and external PHY address values.

When an external transceiver is connected to the BCM5338M MII port and managed by the MDC/MDIO lines, the state of the link, speed, full/half-duplex and link partner flow control capabilities (among many others) can all be accessed via software and need not be provided as hardware pins. In order to preserve LED display capabilities for the MII port, an additional alias register is provided in the "Control Registers" on page 107 (Page 0h), defined as the "MII Port State Override Register" on page 111 (Address 0Eh). This allows the state of the aforementioned status bits to be read from the external PHY and then written to this register, so that consistent LED status information for all nine 10/100 ports can be preserved.

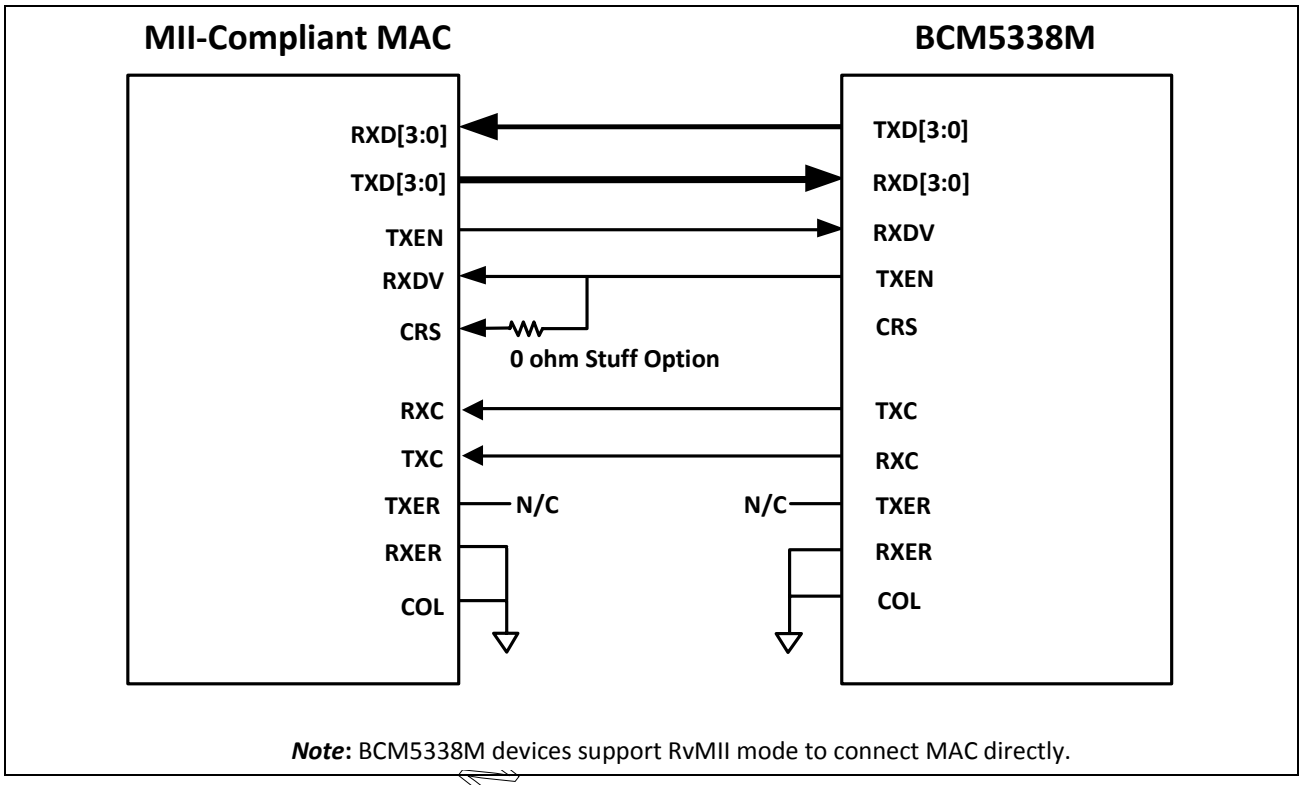
If no MII-based external transceiver is present, page 18h of the register space is not present and returns indeterminate data when read.

Reverse MII Port

BCM5338M device includes an enhanced MII mode that supports direct MAC-to-MAC connectivity. The BCM5338M device supports a software-selectable Reverse MII mode, which makes the BCM5338M MII interface appear as a 100 Mbps full-duplex PHY MII, as seen by the external MAC.

To support this RvMII mode, the clock-to-data timing has been modified. The TXC/RXC input clocks become 25 MHz clock outputs (identical to those of a PHY MII) that only support a 100 Mbps MII interface.

RvMII mode is enabled by setting RvMII_EN, bit 4 of Table 26 on page 111.



***Note*:** BCM5338M devices support RvMII mode to connect MAC directly.

Figure 11: MAC-to-MAC MII Connection

Turbo MII

The MII port can be run at speeds up to 50 MHz to create a 48-port design (blocking). The MII port acts as a stacking port that can transfer up to 200 Mb/s. The basic block diagram can be seen in Figure 12. Flow control between the two rings across the Turbo MII bus is not supported.

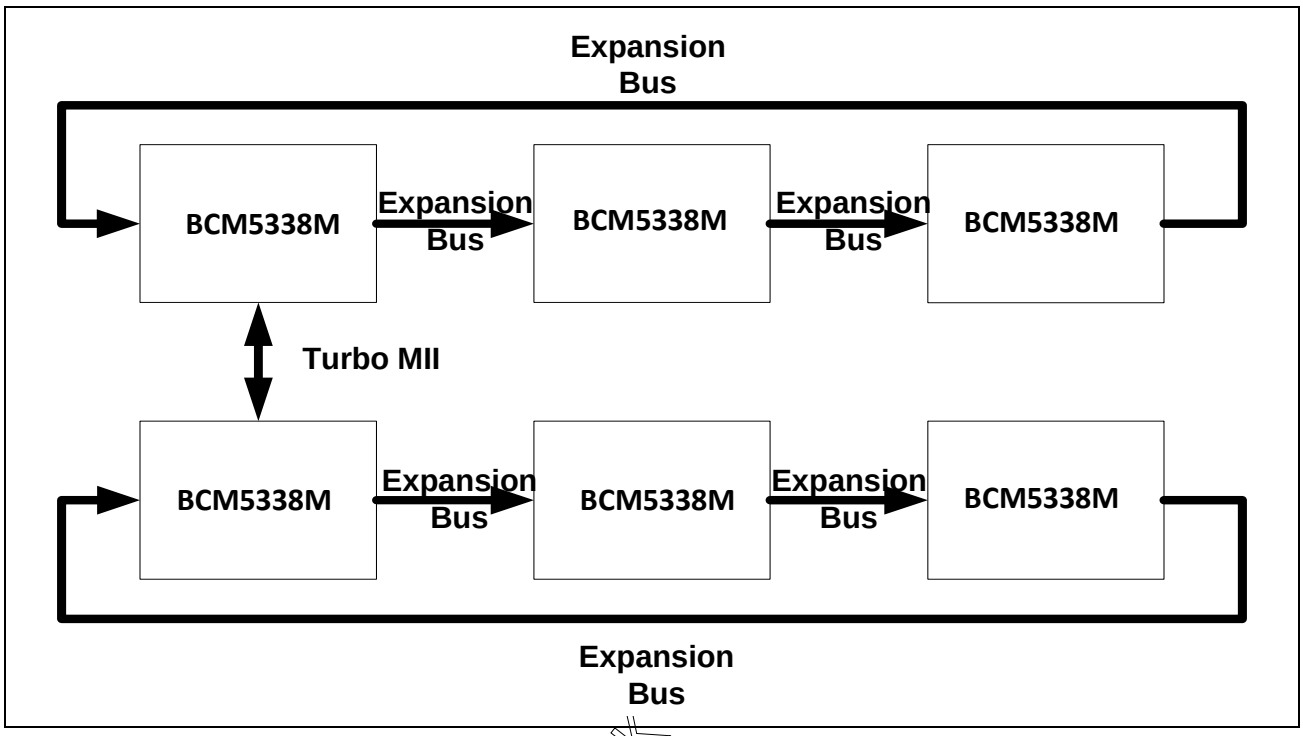


Figure 12: Turbo MII Block Diagram

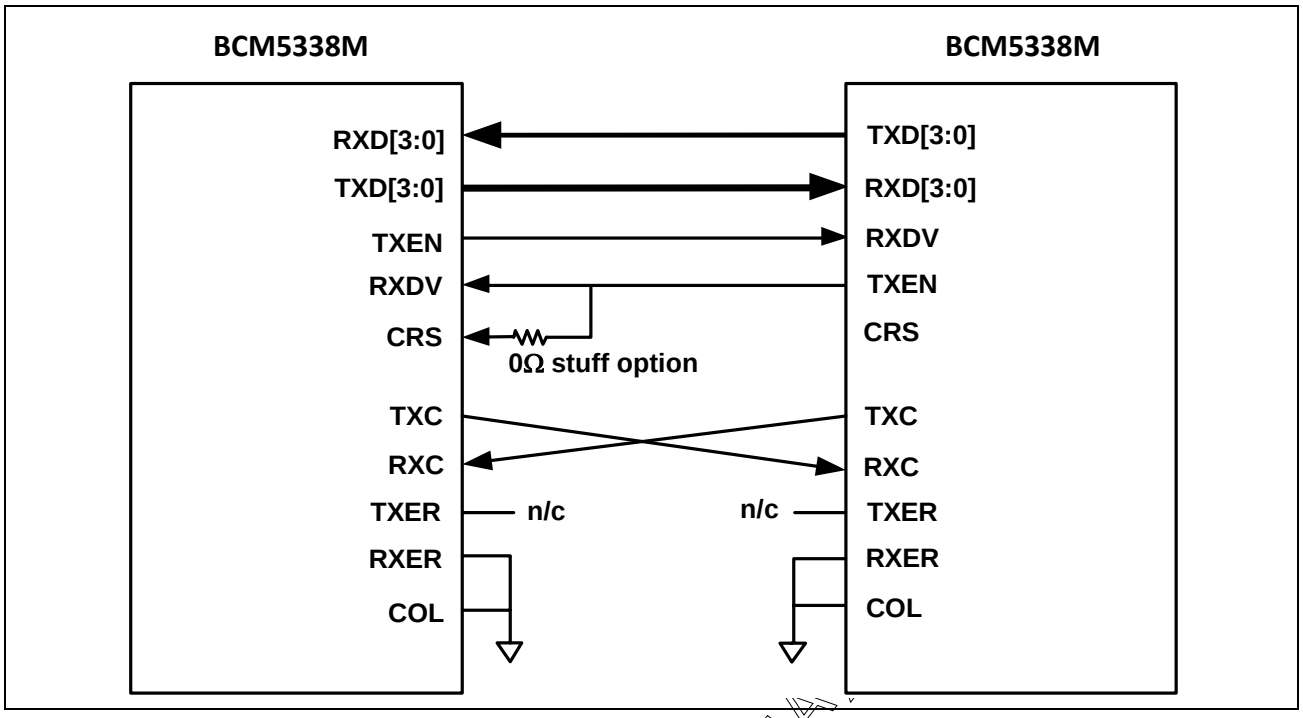


Figure 13: Turbo MII Connections Between BCM5338M

Management Port

The BCM5338M provides the capability to operate as a 11-port device. This allows the nine internal MAC ports and the SMP to operate simultaneously.

The dedicated MII port can be used as a high speed connection to transfer management packets to the external management agent. The MII port can be connected to a transceiver (such as a BCM5202) or directly to a MAC device with an MII, as illustrated in Figure 11 on page 60.

The SMP can also be designated as the management port, although its limited bandwidth means additional care must be taken when configuring advanced management features, such as port mirroring. Additional filtering can be configured so that a smaller number of the received frames are forwarded to the SMP or MII ports to allow for this. The SMP is always required for register configuration and status read/write of the internal registers. However, the MII or the SMP can be selected as the management port, using the frame management port bits in the Global Management Configuration register, and the Management Port ID register. When the MII port is defined as the Frame Management Port, it is referred to as the in-band management port (IMP).

The IMP can be used as a full-duplex 100 Mbps port, allowing substantially higher bandwidth than the SMP, which can be used to forward management information to the external management agent, such as BPDUs, mirrored frames, or frames addressed to other Static address entries that have been identified as of special interest to the management system.

Regardless of whether the SMP or IMP is defined as the frame management port, normal frame data is forwarded to the port based on the state of the RX_UCST_EN, RX_MCST_EN and RX_BCST_EN bits in the associated Port Control register. If these bits are cleared, no frame data is forwarded to the frame management port, with the exception of frames meeting the mirror ingress/egress rules criteria, which are always forwarded to the designated frame management port.

The BCM5338M device intrusively tags frames destined to the management entity to allow the identity of the originating ingress port of a frame to be retained. Additional header information is inserted into the original frame, between the original SA field and Type/Length fields. The tag includes the BRCM Type (8874h) field and the BRCM Tag field. A recalculated FCS is appended to the resultant frame, before the frame is transmitted on the TXD lines. The Management frame format is defined in Figure 14.

Destination Address	Source Address	BRCM Type (8874h)	BRCM Tag (32 bits)	Original Type/Length	Frame Data	Original FCS	Recalculated FCS

Figure 14: Transmit/Receive Frame Format Over Management Port

Similarly, the host system must insert the BRCM Type/Length and Tag fields into frames it wishes to send into the management port, to be routed to specific egress ports. The OPCODE within the Tag field determines how the frame is handled, and allows frames to be forwarded using the normal address lookup or via a Port ID designation within the Tag.

Note: The FCS (outer) is ignored by the BCM5338M device. However the management entity is still supposed to provide 4 bytes of any data as a place holder. Only the final outgoing FCS (inner) is required.

Both the inner and outer FCS can be ignored by setting register Page 34h, offset 05h, bits 1 and 0 to a value of 1. Remember that a placeholder for the inner and outer CRCs must still be sent in with the management packet.

The BRCM Tag and BRCM Type/Length fields are transmitted with the convention of highest significant octet first, followed by next lowest significant octet, and so on, and with the least significant bit of each octet transmitted out from the MAC first. So for the BRCM Type/Length field in Table 15 on page 63, the most significant octet would be transmitted first (bits 24:31), with bit 24 being the first bit transmitted.

Figure 15 shows the format of the BRCM Tag field. The OPCODE field slightly modifies the use and validity of some fields in the Tag. Table 11 on page 64 defines the supported OPCODEs and Table 12 on page 64 identifies each of the other fields in the BRCM Tag in detail.

31 29	28	27	26 16	15 12	11 10	9 8	7 6	5 4	3 2 1 0
Opcode=Unicast	MIR	MO	Frame Octet Count	Reserved	Reserved	Dest DevId	Reserved	Src DevId	Src PortId
Opcode=Multicast	MIR	MO	Frame Octet Count	Reserved	Reserved	Reserved	Reserved	Src DevId	Src PortId
Opcode=Egress Directed	MIR	MO	Frame Octet Count	Reserved	Reserved	Dest DevId	Reserved	Src DevId	Dest PortId
Opcode=Ingress Directed	MIR	MO	Frame Octet Count	Reserved	Reserved		Reserved	Src DevId	Src PortId

Figure 15: BRCM Tag Format

Table 11: OPCODE Field in BRCM Tag for Management Port Frame

OpCodes	Name	Description
0 0 0	Unicast/Multicast	Normal unicast and multicast frames are forwarded using the address table lookup of the DA contained in the frame. If the address is unknown, the frame is flooded. The Source Device ID and Source Port ID fields in the BRCM Tag are required for the learning process. The management port may transmit or receive frames with this format.
0 0 1	Reserved	Reserved.
0 1 0	Egress Directed	An Egress Directed frame is sent by the host management system into the SMP or the IMP port, and is fowarded to the Egress Port specified in the Destination Device ID and Destination Port ID fields in the BRCM Tag.
0 1 1	Ingress Directed	Frame received at an ingress port which had a destination address corresponding either to the Bridge Group Address or the All LAN Bridge Management Group Address. The Source Device ID and Source Port ID identify the ingress port the frame was initially received on.
1 x x	Reserved	Reserved.

Table 12: Fields in BRCM Tag for Management Port Frame

Field	Name	Description
MIR	Mirror Bit	The Mirror Bit tag is applied at the mirrored port. Ingress data received at an Ingress Mirror Port be classified as standard frame type (i.e., Unicast, Multicast, Ingress Frame-BPDU, and so on). Egress data transmitted at an Egress Mirror Port is classified there—mirrored egress frames are classified as standard frame types at the ingress port.
MO	Mirror Only	Indicates to ARL that the frame should only be forwarded to Mirroring port.
	Frame Octet Count	This 11-bit field incorporates the Octet Count of the entire Ethernet frame octet count starting at the DA field and inclusive of CRC, but not including the BRCM Type, BRCM Tag, and recalculated FCS.
Dest DevId	Destination Device ID	A 2-bit Chip ID field which indicates the destination Chip ID for Egress Directed frames.
Dest Portid	Destination Port ID	Indicates the destination Port ID for Egress Directed frames.
Reserved	Reserved	00.
Src Portid	Source Port ID	Indicates the source Port ID for ingress directed frames.

Expansion Interface

The BCM5338M provides an independent expansion port and MII port on separate pins, allowing all nine MAC ports, as well as the expansion port, to operate simultaneously.

Packets are forwarded to the expansion port following address resolution and frame buffering to memory. All eleven ports 8 x 10/100BASE-T, 1 x MII, expansion port and SMP maintain a transmit descriptor queue in the same manner.

The port uses a Full-duplex interface with 16-bit in and out data buses running at 83 MHz to provide up to 2.66 Gbps of bandwidth. The signals provided support a direct connection to a second BCM5338M device as shown in Figure 16 on page 66. For further expansion, the port may be configured as a daisy chain with additional BCM5338Ms as shown in Figure 17 on page 67. This enables the development of a glueless 24-port switch systems with non-blocking performance.

Frames are forwarded to the expansion port in the order queued. All bytes of each frame are transmitted before initiating the transfer of a second frame. Frames may be fragmented into 32-byte bursts across the expansion interface depending on the status of the ready signal (ERDYO). When ERDYO is deasserted, frame forwarding stops at the end of the current 32-byte burst.

Note: The ERDYO/ERDYI signalling runs in the opposite direction to the rest of the expansion bus signalling.

Frames received via the expansion interface are processed as follows:

1. The first 32 bits of the transfer are the header of the frame and contain the source ID and the frame length. The source CHIPID is saved for address learning.
2. Address resolution determines the destination port of the frame by using the destination address within the frame. Concurrently, the frame is buffered to memory
3. After the frame has been buffered to memory, the transmit descriptor queue(s) of the destination port(s) are updated.
4. The SA is learned by the receiving BCM5338M and saved to the local address table according to the learning rules. The transmit port ID field of the address table entry is assigned to be the source CHIP ID saved from the 16-bit header. Subsequent packets received at a local port with a matching DA are forwarded to the expansion port.

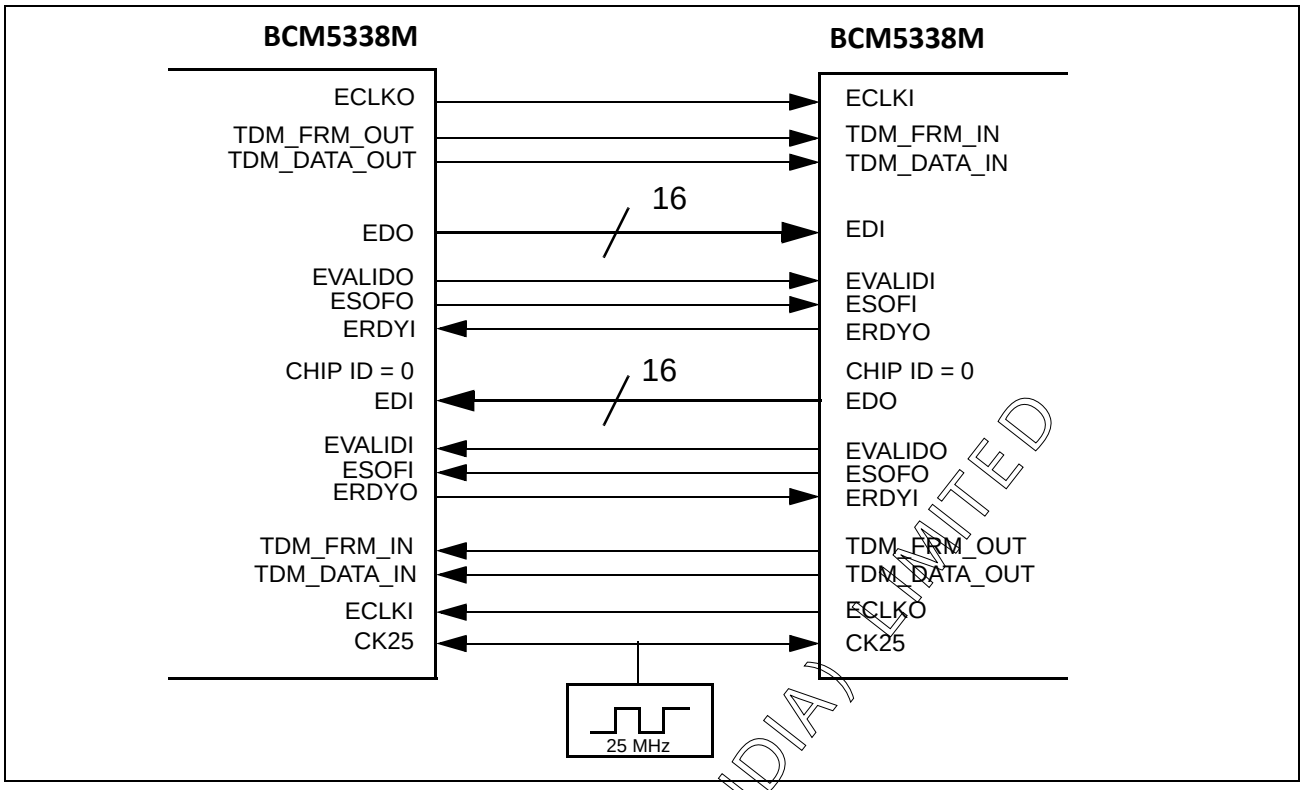


Figure 16: Expansion Port Interface with Two BCM5338M

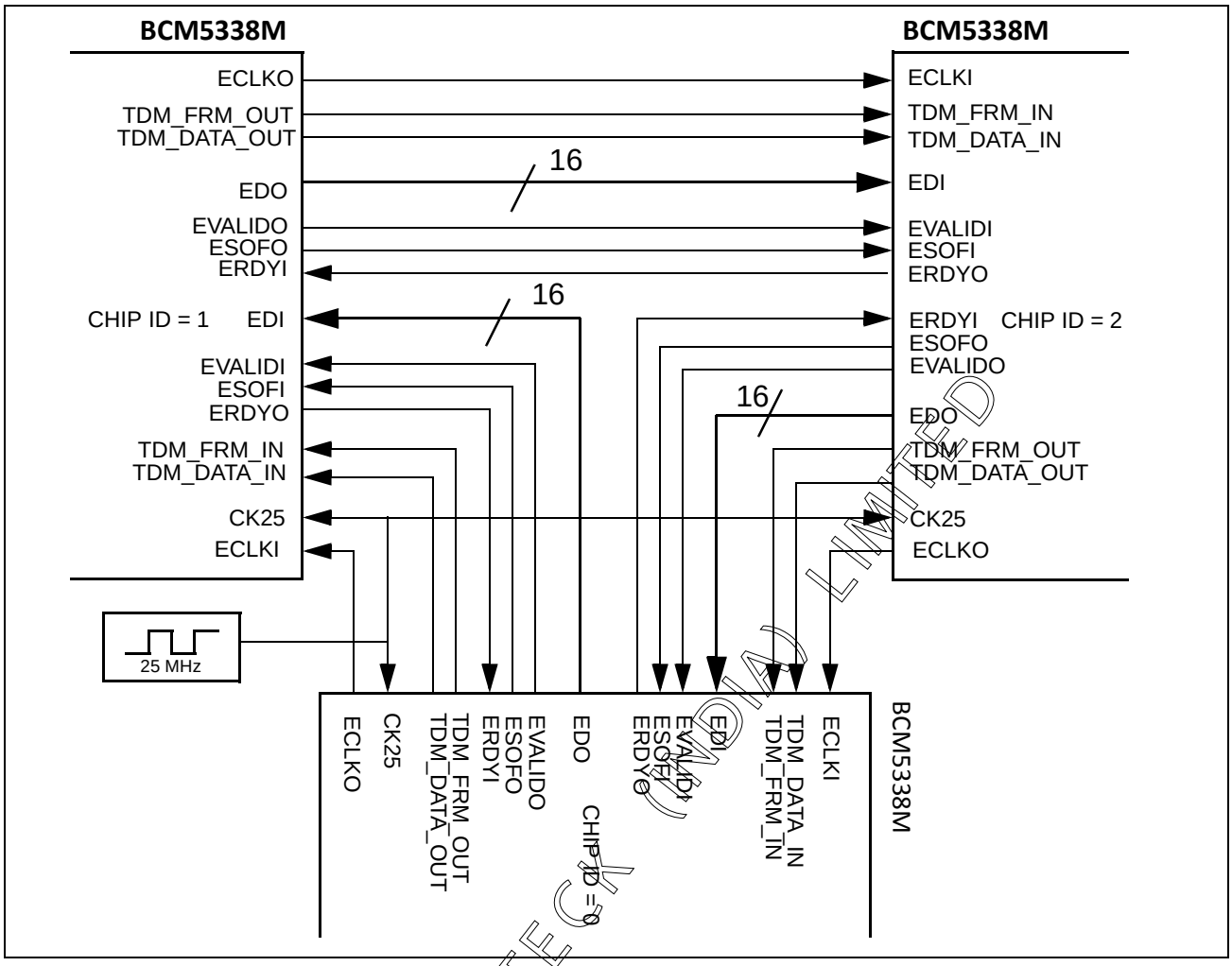


Figure 17: Expansion Port Interface with Daisy-Chained BCM5338Ms

Port Mirroring

The BCM5338M supports port mirroring, allowing any port's ingress and/or egress traffic to be mirrored to a predefined mirror capture port. In a BCM5338M-based system, a single port must be assigned as the mirror capture port. This can be any of the following ports:

- 10/100
- MII/IMP
- SMP

The BCM5338M can be configured to mirror or capture ingress traffic, egress traffic, or both, for any port(s). Mirroring multiple ports is possible but can create congestion at the mirror capture port.

Note: Trunking ports cannot be selected as the mirror capture port.

Note: If the SMP is the mirror capture port, or multiple ports are being mirrored to the IMP, then filtering should be used to reduce traffic congestion and possible loss of mirrored data.

Configuring Port Mirroring

Port mirroring is configured using a set of registers located in the Table 44 on page 118.

Port Mirroring is enabled by setting the MIRROR_ENABLE bit in the "Mirror Capture Control" on page 121 for all BCM5338M devices within the system. This allows intermediate BCM5338Ms between the mirroring port and the mirror capture port to forward mirrored traffic to the mirror capture port. It is necessary to configure the mirror capture port in all BCM5338M devices, but only one chip has the MIRROR_CAPTURE_PORT[10:0] mask set to a network port or the frame management port. These devices then forward mirrored traffic to the expansion port, and the traffic is passed on until it is removed and sent to the mirror capture port by the BCM5338M device that physically owns the mirror capture port.

There is no restriction on the physical location of the mirror capture port, other than there can only be one in any BCM5338M-based system. This allows the internal frame management port to be used as the mirror capture port, in which case additional software resides in the host to process and/or analyze the mirrored data. An external 10/100BASE-T/TX network port or an MII port can also be used, in which case an external probe would likely be attached to capture the mirrored traffic.

Ingress Mirror Rules

Ingress mirror rules are the collective set of port snooping, MAC address, and filter operations that are applied to traffic received at a switch port. The Ingress Mirror Rules are programed using three registers, the "Ingress Mirror Control" on page 122, the "Ingress Mirror Divider" on page 122, and the "Ingress Mirror MAC Address" on page 123.

The Ingress Mirror Control register is used to set the type of filtering to be applied to the receive traffic and to which port(s) this applies. The IN_MIRROR_FILTER bits select among the following:

- Mirror all received frames
- Mirror transmitted frames with DA=x
- Mirror received frames with SA=y

where *y* is the 48-bit MAC address programmed into the Ingress Mirror MAC register.

The IN_MIRROR_MASK[10:0] bits in the Ingress Mirror Control register define the receive ports in an individual BCM5338M device to be monitored.

Note: Any number of receive ports can be programmed to be mirrored, but bandwidth restrictions on the mirror capture port require that this capability be used with appropriate caution, so as not to cause congestion or packet loss

The IN_DIV_EN bit in the Ingress Mirror Control register allows further statistical sampling to be performed. When IN_DIV_EN = 0, the IN_MIRROR_FILTER and the IN_MIRROR_MASK rules are applied to the receive port traffic as described above. When IN_DIV_EN = 1, the receive frames that pass the initial filter are divided by the value IN_MIRROR_DIV, which is a 10-bit value stored in the Ingress Mirror Divider register. This allows the following additional capabilities:

- Mirror every n^{th} received frame
- Mirror every n^{th} transmitted frame with DA=x
- Mirror every n^{th} received frame with SA=y

where n = IN_MIRROR_DIV value.

When multiple receive ports on a single chip (including the Expansion port) have been enabled in the IN_MIRROR_MASK, the cumulative total packet count received from all ports is divided by the value of IN_MIRROR_DIV to deliver the n^{th} receive frame to the mirror capture port.

Egress Mirror Rules

Egress mirror rules are the collective set of port snooping, MAC address and filter operations that are applied to traffic transmitted from a switch port. The Egress Mirror Rules are programed using three registers, the "Egress Mirror Control" on page 123, the "Egress Mirror Divider" on page 124, and the "Egress Mirror MAC Address" on page 124.

The Egress Mirror Control register is used to set the type of filtering to be applied to the transmit traffic and to which port(s) this applies. The OUT_MIRROR_FILTER bits select among the following:

- Mirror all transmitted frames
- Mirror transmitted frames with DA=x
- Mirror transmitted frames with SA=y

Where x and y are the 48-bit MAC address programmed into the Egress Mirror MAC register.

The OUT_MIRROR_MASK[10:0] bits in the Egress Mirror Control register define the transmit ports in an individual BCM5338M device to be monitored.

Note: Any number of transmit ports can be programmed to be mirrored, but bandwidth restrictions on the mirror capture port require that this capability is used with appropriate caution, in order not to cause congestion or packet loss.

The OUT_DIV_OUT bit in the Egress Mirror Control register allows further statistical sampling to be performed. When OUT_DIV_EN =0, the OUT_MIRROR_FILTER and the OUT_MIRROR_MASK rules are applied to the transmit port traffic as described above. When OUT_DIV_EN = 1, the transmit frames that pass the initial filter are divided by the value OUT_MIRROR_DIV, which is a 10-bit value stored in the Egress Mirror Divider register. This allows the following additional capabilities:

- Mirror every n^{th} transmitted frame
- Mirror every n^{th} transmitted frame with DA=x
- Mirror every n^{th} transmitted frame with SA=y

...where n = OUT_MIRROR_DIV value.

When multiple ports on a single chip (including the Expansion port) have been enabled in the OUT_MIRROR_MASK, the cumulative total packet count transmitted from all mirrored ports are divided by the value of OUT_MIRROR_DIV to deliver the n^{th} transmit frame to the mirror capture port.

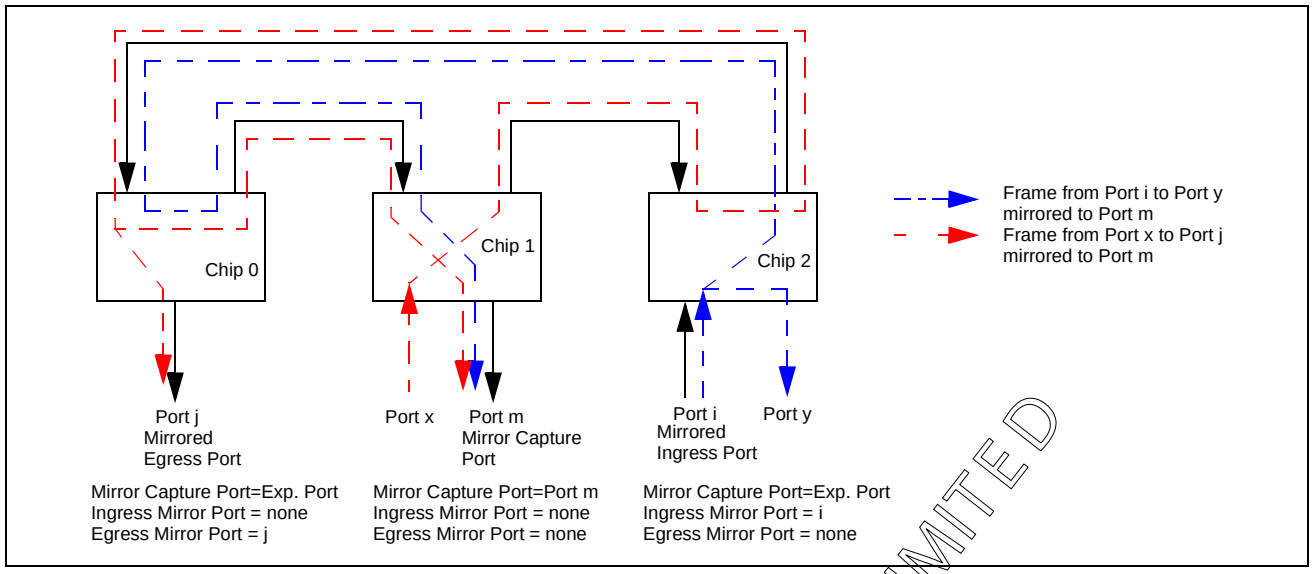


Figure 18: Simple Port Mirroring Example

Chip 1 is configured to have the mirror capture port as port m. Chip 2 is configured to have receive traffic mirrored from port i, and the mirror capture port as the expansion port. Chip 0 is configured to have transmit traffic mirrored from port j, and the mirror capture port as the expansion port. Traffic received at port i on chip 2 is mirrored to the mirror capture port on chip 1 via the expansion port, even though it is still transmitted at its normal destination. Traffic transmitted at port j of chip 0, is mirrored to the mirror capture port on chip 1 via the expansion port, even though it was received on a different chip. Special cases:

If the frame needs to go out to the expansion port, there are 2 bits in the expansion port header field that identify how the frame should be treated:

- The mirror (MIR) bit indicates the frame was classified as a mirrored frame at the ingress port.
- The mirror only (MO) bit Indicates to the ARL that the frame should only be forwarded to mirror capture port.

These bits are used to determine:

- A forwarded frame—if a forwarded frame is received from the expansion port, apply the normal filtering rules for forwarding frame, or
- A mirrored frame—if a mirrored frame is received from the expansion port, forward this frame directly to the mirroring port, or
- A mirrored frame that is also a forwarded frame—forward this frame to both the mirror capture port and the destination port. If the forwarding and mirroring decision is the same egress port, then only one frame is forwarded to the egress port.

If the SMP is the frame management port but not the mirror capture port, the SMP Control register bits RX_BCST_EN, RX_MCST_EN and RX_UCST_EN, turns on/off the forwarding of broadcast, multicast and unicast frames respectively, MP. If the SMP is also configured as the mirror capture port for the system and the Ingress/ Egress Mirror Rules match a frame, it is forwarded to the SMP regardless of the state of the RX_BCST_EN, RX_MCST_EN and RX_UCST_EN bits.

A port that receives frames that would normally result in a decision not to forward the frame (i.e., both the DA and SA are attached to the same port) causes a frame to be forwarded to the mirror capture port if the Ingress mirror rules have been configured to mirror that port, DA, or SA.

Note: For Traffic Mirroring in multiple chip configurations, there may be some limitations based upon the traffic flow between the chips.

IGMP Snooping

IGMP is a commonly used protocol to transmit video and multimedia streams over IP. When enable IGMP IP layer snooping is set in the Global Configuration register (page 0x02, register 0x00), the BCM5338M looks in the protocol field of the IP header for each packet to trap IGMP control packets and forwards them to the management port. The management CPU can then determine from the IGMP control packets which port should participate in the multigroup session by programming the multicast address in the ARL table or the Multiport Address 1/2 registers and the Multiport Vector 1/2 registers.

Protected Ports

Traffic between protected port group members is blocked. Traffic can only be sent from protected ports to unprotected ports. An unprotected port can send traffic to any other port. Several applications can benefit from protected ports:

- Aggregator

  Example: If ports[4:2] are grouped as protected ports, then all port[4:2] traffic can be aggregated to port 1. Mcast, Bcast, and DLF traffic on ports[4:2] is not flooded, it only forwards to port1.

- To avoid certain user (ports) seeing important information on a server port, make that server port and those unsecured port protected ports. This way, those unsecured ports can never see traffic on the server port.

The BCM5338M has the Table 30 on page 113 which can be used to select a group of ports as protected.

WAN Port

See Table 29 on page 112. If a port is selected as a WAN port, then all that port's traffic is forwarded to the CPU port only. All non-WAN port traffic from local ports do not flood to the WAN port.

To avoid CPU Mcast, Bcact, and DLF packets flooding to the WAN port, the BCM5338M can limit CPU traffic to the WAN port by setting the WAN Port Select Reg[9] = 1 so only egress directed frames (from the CPU) can go to the WAN port. A non-egress-direct frame from the CPU (including DLF, Mcast, and Bcast) does not go to WAN port, so the WAN port is not flooded with unrelated frames. If the CPU needs to send a frame to the WAN port, it should use egress-direct frames.

Note: If WAN Port Select Reg[9] = 0, then the WAN port is flooded with DLF, Mcast, and Bcast from the CPU port if the CPU uses non-egress-direct frames to access a non-WAN port.

Only the ports on CHIPID = 0 can be configured as the WAN port.

802.1x Port-Based Security

802.1X is a port-based authentication protocol. By receiving and extracting special frames, the CPU can control whether the ingress and egress ports should forward packets or not. If a user port (supplicant) wants to get service from another port (authenticator), it must get approved by the authenticator. EAPOL is the protocol used by the authentication process. The BCM5338M detects EAPOL frames and passes them to the CPU port. If the BCM5338M is configured for 802.1x after reset, all traffic is blocked except EAPOL traffic (but can optionally allow for other special frames to pass). After the authentication process is finished, some limitations are added to each port based on the result of authentication.

The BCM5338M also supports static and dynamic per port secured MAC functions.

- **In the static secure MAC mode**, the BCM5338M has a separate secure MAC memory. An incoming frame is dropped if its SA is in or not in that MAC memory, depending on the chosen mode.
- **In the dynamic secure MAC mode**, the BCM5338M can drop the frame if:
  - Per port MAC addresses exceed a programmed number.
  - The incoming frame's SA is not in the ARL.

The BCM5338M also supports per port aging. To enable per port aging, perform the following steps:

1. Enable global per port aging by setting Table 184 on page 205 bit[0] = 1.
2. Set Table 185 on page 206 through Table 188 on page 207 to the appropriate value to enable each port's aging function.

The BCM5338M has two registers to control per port security:

- See Table 166 on page 196.
- See Table 167 on page 197.

Within these two registers, there are eight control fields, MAC_SEC_CON_p0 to MAC_SEC_CON_p7. Each field has three bits and can be used to control the per port MAC security function.

Since 802.1x and Secure MAC are per port based, each port can be programmed to a different mode.

Example:

- Port_0: Normal mode.
- Port_1: Standard 802.1x mode.
- Port_2: Extended 802.1x with static secure MAC mode.

The BCM5338M can support four different types of applications:

- **Standard 802.1x application** (MAC_sec_con_px[2:0]= 000): until authentication passes, the BCM5338M blocks ingress traffic, or it blocks ingress and egress traffic (802.1x_special_frames are not blocked).
- **Extended 802.1x mode application with SA number-based dynamic secure MAC mode** (MAC_sec_con_p[2: 0] = 110): the BCM5338M uses ARL to store all user MAC addresses so each port can support up to 4K MAC users. The BCM5338M counts the per port number of SA in ARL. If the ingress port's SA number exceeds the programmed limit, then the BCM5338M drops that frame, except those 802.1x_special_frames. Optionally, the BCM5338M can be programmed not to drop any frames.
- **Extended 802.1x mode application with ARL-based dynamic secure MAC mode** (MAC_sec_con_p[2:0] = 111): the BCM5338M uses ARL to store all user MAC addresses so each port can support up to 4K MAC users. For each ingress frame, the BCM5338M checks if the SA is in the ARL. If the SA is not in the ARL, then the BCM5338M drops that frame, except those 802.1x_special_frames. Optionally, the BCM5338M can be programmed not to drop any frames.
- **Extended 802.1x mode application with static MAC pass mode** (MAC_sec_con_p[2:0]=100): each Ingress port can support up to 16 users in a BCM5338M special static secure MAC table. If a frame's MAC_SA is:
  - In the static secure MAC table, the BCM5338M forwards it.
  - Not in the static MAC table, then it is dropped if it is not a 802.1x_special_frame.

  Optionally, the BCM5338M can be programmed not to drop any frames. In the BCM5338M device's static secure mode, byte counters for up to 16 source MAC addresses per port can be used to measure usage.

Note: This mode supports port security, but not 802.1x.

Figure 19 on page 75 shows the Static MAC table, and Figure 20 on page 76 shows the format and addressing.

Note: Programming the Static MAC addresses is done via the 802.1Q VLAN and Secure MAC Access register (Page 34h, offset 08h, see "802.1Q VLAN and Secure MAC Table Access Register" on page 187) and the Secure MAC Write register (Page 34h, offset 30h, see "802.1Q VLAN and Secure MAC Write Register" on page 187).

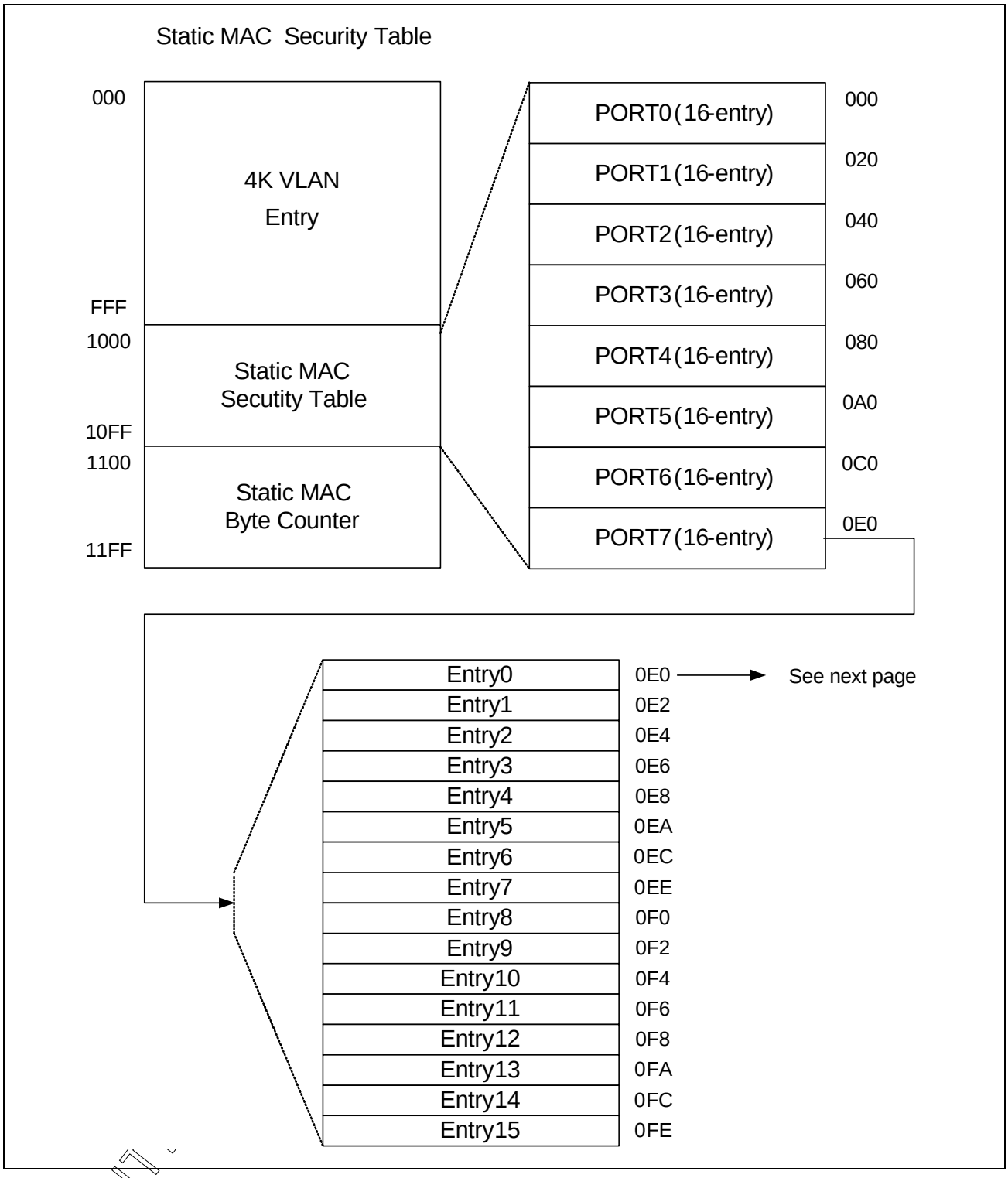


Figure 19: Static MAC Security Table (Rev. B)

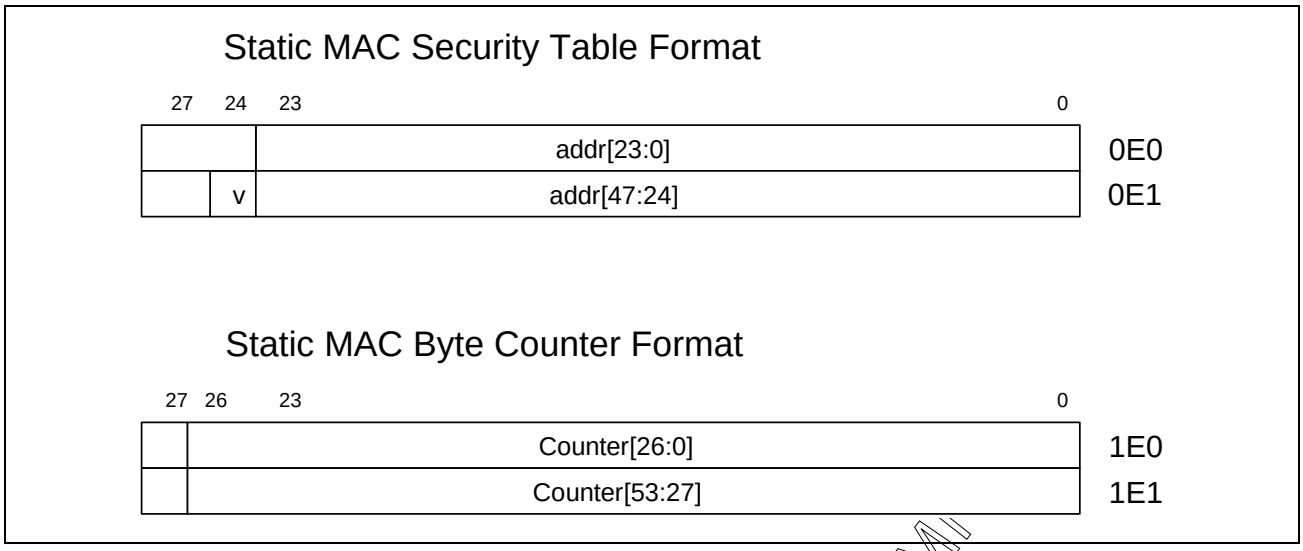


Figure 20: Format and Addressing of the Static MAC Table

MAC-Based Trunking

The BCM5338M allows ports to be trunked together. This helps increase the effective bandwidth through a link and provide redundancy. The MAC-based algorithm has some added features over port-based trunking. By performing a dynamic hashing algorithm on the MAC address or addresses, each packet can choose which port within a trunk group to transmit a packet across. This method has several key advantages. By dynamically performing this function, the traffic patterns can be more balanced across each port within a trunk. In addition, the MAC-based algorithm also provides enhanced feature, dynamic failover. If a port within a trunking group fails, dynamic failover allows the other good ports to take over all the traffic. Thus it allows for a seamless, automatic way for redundancy to occur over a trunk. The BCM5338M allows up to four trunking groups with a maximum of eight ports per trunk.

Note: Within a system, MAC-based trunking is limited to one BCM5338M device with CHIPID = 00 in the system having ports in a trunk.

Port-Based VLAN

The VLAN, virtual LAN, feature provides a solution to partition the switching ports into different private domains. Data switching between different private domains is not allowed, so that data security can be maintained. The BCM5338M provides flexible VLAN configuration and allows virtually unlimited number of VLAN group combinations. Any switch port can be grouped into the same VLAN group by programming the register file without any constraints.

The VLAN mechanism basically is a filter function. The BCM5338M builds the function as per ingress port associated. For each receiving packet, the ARL resolves the Destination Address (DA) and gets a forwarding vector. Then the ARL applies the VLAN filter to the forwarding vector to mask out the non-private domained ports. Without forwarding information records in the forwarding vector, the non-private domained egress ports never get chance to inqueue the packet.

The VLAN registers are located on Page 31h and contain an array of registers which correspond to the various ingress ports. The VLAN port register is a bit per port vector and one for each ingress port. For BCM5338M, 10 VLAN port registers have been designed to support eight 10/100, MII and SMP ports.

802.1Q VLAN

The BCM5338M supports IEEE 802.1Q VLAN. The BCM5338M supports up to 4K VLAN table entries. The VLAN table resides in the internal embedded memory. Each VID consists of a Valid Bit, Untag Map, and Fwd Map.

Untag Map and Fwd Map

- Untag Map controls whether the egress packet is tagged or untagged.
- Fwd Map defines the membership within a VLAN domain.

Untag Map and Fwd Map include bit-wise representation of all the ports. Once the VLAN table is programmed and maintained by the CPU, the BCM5338M autonomously handles all operations of the protocol. These actions include the stripping or adding of the 802.1Q tag depending on the requirements of the individual transmitting port. It also performs all the necessary VLAN lookups in addition to MAC L2 lookups. These are necessary to determine the correct packet routing. In addition to being supported for a single chip, 802.1Q is also supported across multiple chips.

Quality of Service

The Quality of Service (QoS) feature provides four internal queues to support four different classifications of traffic. High priority packet streams experience less delay inside the switch, which supports lower latency for certain delay-sensitive traffic. The BCM5338M can classify the packet as one of the four priorities according to Port ID, MAC address, 802.1p priority tag, DiffServ and/or IP TOS. The QoS mechanism operates at full wire speed.

The BCM5338M supports up to four priority queues. The Table 126 on page 172 is used to select the number of queues. The BCM5338M uses a Weighted Round Robin (WRR) algorithm to schedule each tx_queue. The BCM5338M also supports Preemp + WRR. When enabled, the highest priority queue in Table 98 on page 145 is emptied first, then the lower priority queues use WRR to schedule their queues. In this scheme, the highest priority queue always gets serviced as long as there is any data in that queue.

Note: If four queues are programmed, the lowest priority queue is queue_0, the highest priority queue is queue_3.

Port-Based Priority

The QoS feature can be activated by either asserting the configuration strap pin QOS_EN or programming the QoS Control register. Strap options allow for a particular subset of ports to be classified as high priority ports (that is, by default all incoming traffic on that port is considered high priority). This option requires no additional register programming. Alternatively, the Table 126 on page 172 allows for complete CPU control of all ports' priority defaults.

Additionally, two other mechanisms determine whether an individual incoming packet is classified as one of the four priorities.

MAC-Based Priority

Static addresses in the ARL can be designated by the CPU as high priority. If an incoming packet's Destination Address (DA) matches one of these designated high priority addresses, the packet is routed as a high priority packet. Because the CPU must assign the priority to the matching DA ahead of time, the ARL entry should be made static.

802.1p Priority

When QoS is enabled, the packet is examined for the presence of a valid 802.1p priority tag. If present, the packet is routed at a priority that is determined by the mapping defined by the value in the Table 131 on page 175.

For handling different priority packets, each egress port has been designed to provide up to four queues. Once the feature has been enabled, the QoS classification mechanism routes each received packet to the appropriate egress queue on the fly. At each egress port, the QoS scheduler uses a weighed fair algorithm to select a packet from the different queues, one at a time, and deliver it. By using programmable parameters for the weights, the relative weighting of the algorithm can be adjusted. The QoS scheduler first selects and delivers up to HQ_weight blocks of data, and then switches to pick up low priority blocks (up to LQ_weight). As long as each queue is given some weighting, the algorithm can prevent queue starvation.

IP TOS Priority

The BCM5338M can classify traffic based on the TOS field in the IP Header. If TOS priority is enabled, the BCM5338M classifies traffic based on 8 different precedence values. These values get mapped to the different priority queues based upon the following TOS Priority registers:

- Monetary Cost Priority
- Reliability Priority
- Throughput Priority
- Delay Priority

TOS priority is controlled by the Table 132 on page 175. To enable TOS priority mapping, set this register to a value of 0x81.

DiffServ DSCP Priority

The BCM5338M can classify traffic based on the DSCP field in the IP Header. If DSCP priority is enabled, the BCM5338M classifies traffic based on the DSCP value. The Table 137 on page 177 and Table 138 on page 177 are used to assign priority to different Differentiated Services.

The BCM5338M uses the following conditions to make a final decision on any priority conflicts for each port:

```
if (port_based priority enable)
   Follow port based priority rule
else if (TOS/Diff been enable)
   Follow TOS/Diff priority rule
else if (802.1p been enabled)
   Follow 802.1p priority rule
else if (MAC based priority been set)
   Follow MAC priority rule
else
   Set frame to lowest priority.
```

LED Interfaces

The BCM5338M provides visibility per port of link status, port speed, duplex mode, combined transmit and receive activity, and collision. Both a parallel and serial interfaces are supplied to drive the status to the LEDs. The parallel interface provides the lowest cost solution for implementing LEDs. However, as the port density of the system increases, the number of signals required for the parallel implementation may become prohibitively large. In these cases, the serial mode is more appropriate. The serial interface provides up to five status indications per port; whereas, the parallel interface indicates only up to three. Combinations of serial and parallel status can also be effective in lowering the system cost.

During power-on and reset, the parallel LED signals are driven low and the serial interface shifts a continuous low value for 1.34s.

Parallel LED Interface

Three pins per port, including the MII port, are provided for directly driving LED status:

- $\overline{\text{LEDA}}$
- $\overline{\text{LEDB}}$
- $\overline{\text{LEDC}}$

The LED mode configuration signals control the LED status type driven by each pin. Table 13 on page 81 describes the selectable status types, and Table 14 on page 82 gives a complete LED mode matrix for parallel interface.

Serial LED Interface

A two pin serial interface, LEDDATA and LEDCLK, provides data and clock to enable external shift registers to capture the LED status indications from the BCM5338M for each internal port. The LED status of the MII port is excluded since its PHY is external. The status encapsulated within the shift sequence is configured by the LED mode configuration signals. The configuration signals select both the number of status bits per port and the status type of each bit. The serial interface also provides an 8-bit value indicating the percentage of total bandwidth used by the switch.

Note: In a multichip system, the percentage of total system bandwidth is indicated by the 8-bit value of the last device in the chain.

Example: In a 3-chip system, the LOAD status of the system is available from device with CHIP ID 10.

The LEDCLK is generated by dividing the 25-MHz input clock by 16, providing a 640 ns clock period. The LEDDATA outputs are generated on the falling edge of the LEDCLK and have adequate setup and hold time to be clocked externally on the rising edge of LEDCLK.

The first two bits in the sequence are RESVD and $\overline{\text{LEDERR}}$. The following shift sequence is a consecutive stream of 8-bit status words. The first word of the sequence is the LOAD status, followed by optional port status words. Each 8-bit port status word contains one bit for each port of the designated LED status type. The words are shifted MSB first. For a port status word, the MSB corresponds to port 7. The shift sequence is repeated every 42 ms.

See Figure 21 on page 81 for an illustration of the serial LED shift sequence, Table 13 on page 81 for LED status type, and Table 14 on page 82 for a LED mode matrix.

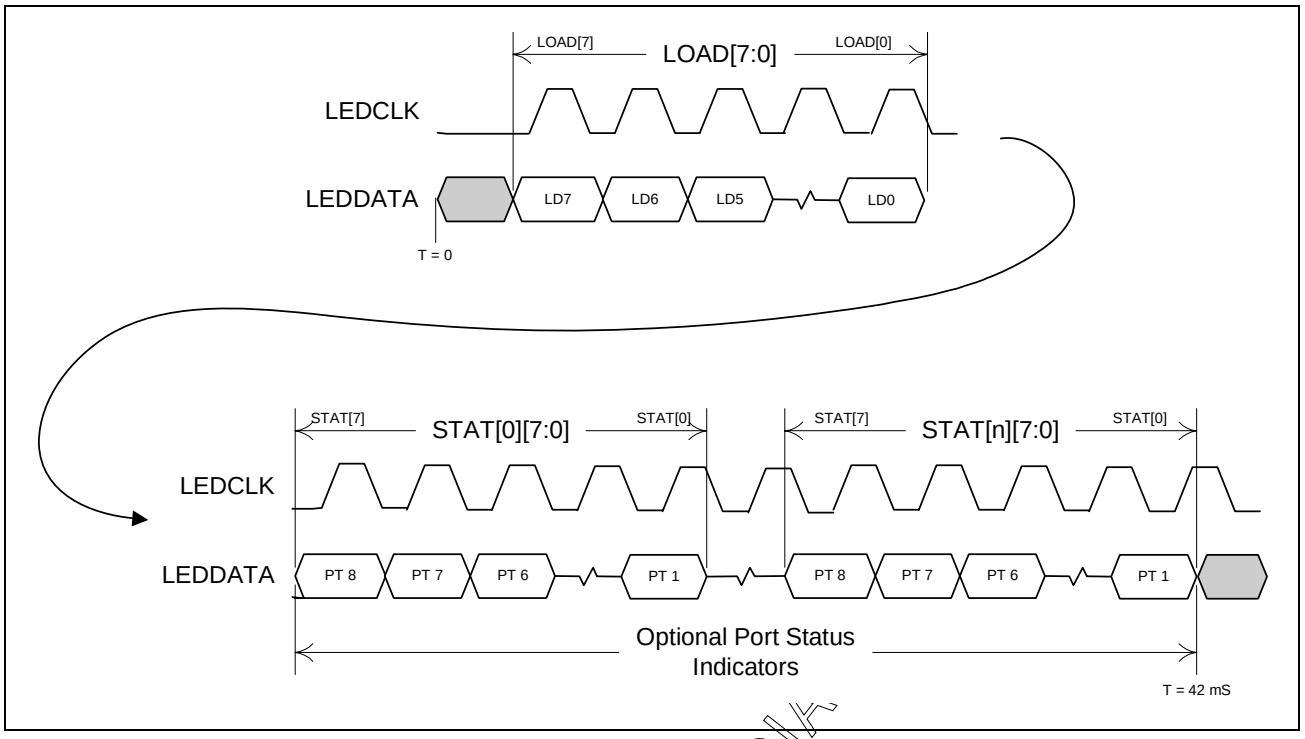


Figure 21: Serial LED Shift Sequence

Table 13: LED Status Types

Name	*Description*
LOAD	Bandwidth utilization meter. 8-bit value indicating the percentage of total bandwidth of the switch utilized over a 42 ms interval for packet data. In multichip system, the 8-bit value from the last device in the chain contains the system bandwidth utilization meter.
LNK/ACT	Link and Activity status indicator. Low when link is established. Blinking at 12 Hz when link is up and port is transmitting and receiving.
LNK/ACT/SPD	Link, Activity and Speed indicator. Active when link is up. Blinking at 3 Hz when port is transmitting or receiving in 10 MB mode. Blinking at 12 Hz when port is transmitting or receiving in 100 MB mode.
LNK	Link status indicator. Low when link is established. High when link is off.
DUPLEX	Duplex mode indicator. High for half-duplex or no link, and low for full-duplex and link.
SPEED	Speed indicator. High for 10 Mbps or no link, and low for 100 Mbps and link.
ACT	Activity. Low for 42 ms when transmit or receive activity is detected during previous 42-ms interval. High during no activity or no link.
COLSN	Collision. Low for 42 ms when collision is detected during the previous 42 ms interval. High in the absence of collisions or no link.
$\overline{\text{LEDERR}}$	Error indication. Internal memory fails self-test during power-on reset. Low if failure occurs.

Table 14: LED Mode Matrix

LED Mode [2]	*LED Mode [1]*	*LED Mode [0]*	*$\overline{\text{LEDA}}$*	*$\overline{\text{LEDB}}$*	*$\overline{\text{LEDC}}$*	*Shift Sequence*
0	0	0	LNK/ACT	DUPLEX	SPEED	$\overline{\text{RESVD}}$ (1 bit) $\overline{\text{LEDERR}}$ (1 bit) $\overline{\text{LOAD}}$ (8 bits) LNK/ACT (8 bits) DUPLEX (8 bits) SPEED (8 bits)
0	0	1	LNK/ACT/SPD	DUPLEX	-	$\overline{\text{RESVD}}$ (1 bit) $\overline{\text{LEDERR}}$ (1 bit) $\overline{\text{LOAD}}$ (8 bits) LNK/ACT/SPD (8 bits) DUPLEX (8 bits)
0	1	0	LNK	ACT	SPEED	$\overline{\text{RESVD}}$ (1 bit) $\overline{\text{LEDERR}}$ (1 bit) $\overline{\text{LOAD}}$ (8 bits) LINK (8 bits) ACTIVITY (8 bits) SPEED (8 bits) DUPLEX (8 bits)
1	0	0	LNK/ACT	DUPLEX	SPEED	$\overline{\text{RESVD}}$ (1 bit) $\overline{\text{LEDERR}}$ (1 bit) $\overline{\text{LOAD}}$ (8 bits) LNK/ACT (8 bits) DUPLEX (8 bits) SPEED (8 bits) COLSN (8 bits)
1	0	1	LNK/ACT/SPD	DUPLEX	COLSN	$\overline{\text{RESVD}}$ (1 bit) $\overline{\text{LEDERR}}$ (1 bit) $\overline{\text{LOAD}}$ (8 bits) LNK/ACT/SPD (8 bits) DUPLEX (8 bits) COLSN (8 bits)
1	1	0	LNK	ACT	SPEED	$\overline{\text{RESVD}}$ (1 bit) $\overline{\text{LEDERR}}$ (1 bit) $\overline{\text{LOAD}}$ (8 bits) DUPLEX (8 bits) COLLISION (8 bits)

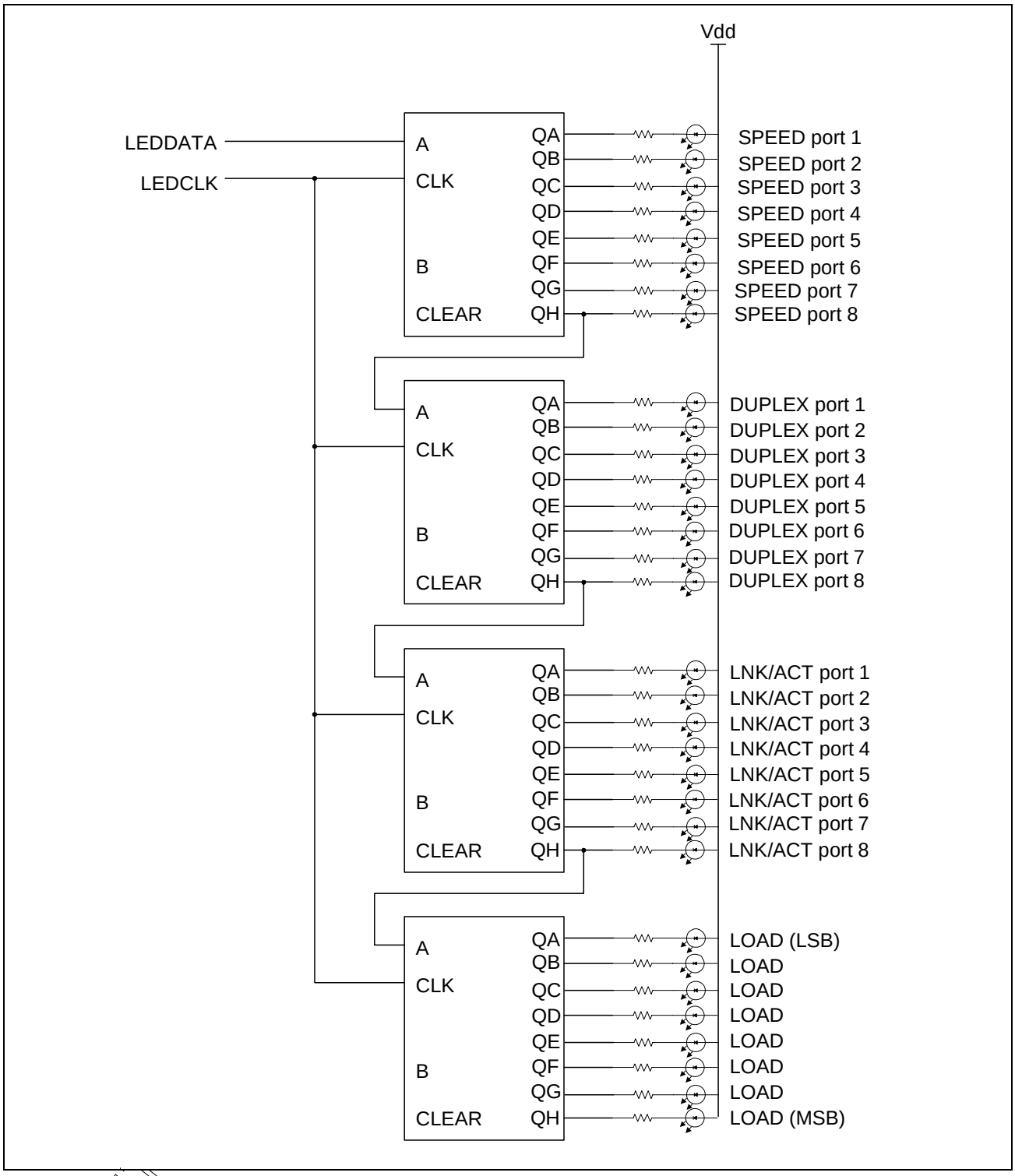


Figure 22: Partial Example External Circuit for Serial LED Mode

Load Meter LED

The load meter LEDs provide a bar-graph indication of the percentage of total available bandwidth of the switch utilized by packet data over a periodic interval of 42 ms. The bar-graph scale is shown in Table 15. The load meter is valid in both single and expanded systems.

In the expanded systems, the bandwidth information is accumulated across multiple BCM5338M devices. The accumulation is initiated by the device with CHIPID = 00. Each device in the system accumulates the bandwidth value of the previous device with its own and passes the accumulated value to the next device in the chain through the expansion interface. The last device in the chain displays the accurate load value for the entire system through the serial LED interface.

Table 15: Load Meter LED Decode

Load Value $\overline{Load}$[7:0]	***Number of LEDs On***	***Bandwidth (%)***
11111111	0	Less than 0.4 (all LEDs off)
11111110	1	Less than 0.8
11111100	2	Less than 1.6
11111000	3	Less than 3.2
11110000	4	Less than 6.4
11100000	5	Less than 12.8
11000000	6	Less than 25
10000000	7	Less than 50
00000000	8	Greater than 50 (all LEDs on)

Configuration

Configuration of the BCM5338M takes place during reset by loading internal control values from pins on the device. All of the pins used for initialization are also used as functional pins during normal operation. These pins are configured to default settings with internal pullup or pulldown resistors and must be configured with external pullup or pulldown resistors to change the default value. The value at the pin is loaded when the reset sequence completes and the pin transitions to normal operation.

An optional configuration solution is using the external serial EEPROM. After default value been captured from the strap pins, the EEPROM download sequence can also be activated by deasserting the CPU_EEPROM_SEL strap pin. The EEPROM configuration mechanism fetches instructions from the EEPROM; the first word fetched is the header and then programming commands follow. The header is used to indicate if the EEPROM exists or not. Also, total command length encapsulates in the head. The EEPROM configuration mechanism deactivates if the header fetched has been identified as invalid. The address and data paired command store in the EEPROM describe which register is to be updated to which contents. Because the command can affect entire register scope, it can be used to configure the chip for more advanced features. Because the interface for using the EEPROM is sharing with the SPI interface, only one interface can be activated. The CPU_EEPROM_SEL strap pin controls the activated interface.

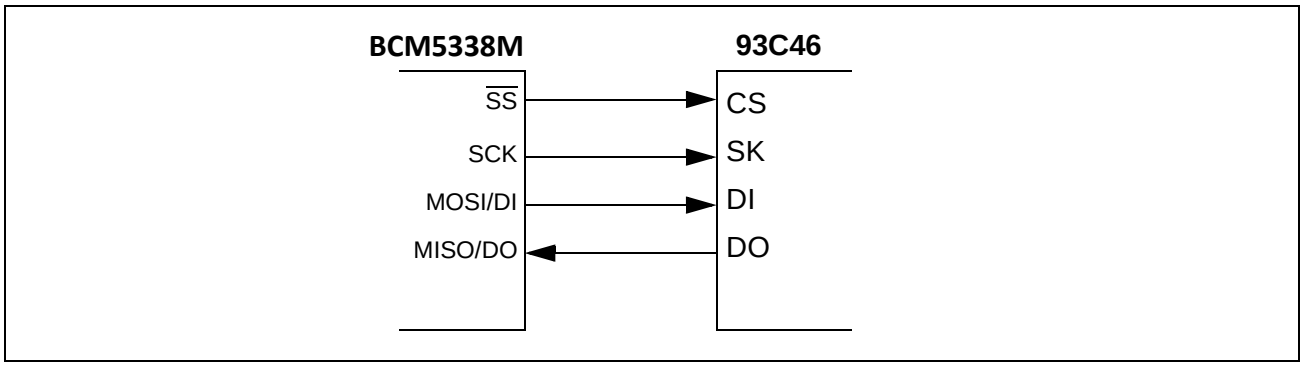


Figure 23: Serial EEPROM Connection

MII Management

PHY Address

The MDC/MDIO pins of the BCM5338M allow no enhanced features over-and-above those of the original BCM5308 device. This means that when the SMP is active, the MDC/MDIO pins have no access to the new BCM5338M status and configuration registers, and nor do they allow the additional MII port to be configured or monitored. These functions must be provided via the SMP.

Each transceiver in the BCM5338M has a unique PHY address for MII management. The addresses are set through the PHY address pins. The pins are latched at the trailing end of reset. Transceiver 1 have the address AA000, where AA=CHIPID[1:0]. Transceivers 2-8 have addresses AA001 through AA111, respectively.

Every time an MII write or read operation is executed, the transceiver compares the PHY address with its own PHY address definition. The operation is executed only when the addresses match.

Register Programming

Using MDC/MDIO for this mode only applies when the SMP is disabled. The BCM5338M fully complies with the IEEE 802.3u Media Independent Interface (MII) specification. The MII management interface registers of each port are serially written to and read from using a common set of MDIO and MDC pins. A single clock waveform must be provided to the BCM5338M at a rate of 0–12.5 MHz through the MDC pin. The serial data is communicated on the MDIO pin. Every MDIO bit must have the same period as the MDC clock. The MDIO bits are latched on the rising edge of the MDC clock. MDC may be stopped between frames provided that no timing requirements are violated. MDC must be active during each valid bit of every frame, including all preamble, instruction, address, data, and at least one idle bit. Every MII read or write instruction frame contains the fields in the following table.

Table 16: MII Management Frame Format

Operation	*PRE*	*ST*	*OP*	*PHYAD*	*REGAD*	*TA*	*Data*	*Idle*	*Direction*
Read	1 ... 1	01	10	AAAAA	RRRRR	ZZ Z0	Z ... Z D ... D	Z Z	Driven to BCM5338M Driven by BCM5338M
Write	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Z	Driven to BCM5338M

Preamble (PRE)

Thirty-two consecutive 1 bits must be sent through the MDIO pin to the BCM5338M to signal the beginning of an MII instruction. Fewer than thirty-two 1 bits cause the remainder of the instruction to be ignored. In preamble suppression mode, only two preamble bits are required between frames.

Start of Frame (ST)

A 01 pattern indicates that the start of the instruction follows.

Operation Code (OP)

A read instruction is indicated by 10, while a WRITE instruction is indicated by 01.

PHY Address (PHYAD)

A 5-bit PHY address follows next, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips.

The BCM5338M supports the full 32-PHY address space with the upper two bits of the address configured from input pins and PHYAD[2:0] internally decoded to select one of the eight transceivers.

Register Address (REGAD)

A 5-bit register Address follows, with the MSB transmitted first. The register map of the BCM5338M, containing register addresses and bit definitions, are provided on the following pages.

Turnaround (TA)

The next 2 bit times are used to avoid contention on the MDIO pin when a read operation is performed. For a Write operation, 10 must be sent to the BCM5338M chip during these two bit times. For a read operation, the MDIO pin must be placed into high-impedance during these two bit times. The chip drives the MDIO pin to 0 during the second bit time.

Data

The last 16 bits of the frame are the actual data bits. For a write operation, these bits are sent to the BCM5338M, whereas, for a read operation, these bits are driven by the BCM5338M. In either case, the MSB is transmitted first. When writing to the BCM5338M, the data field bits must be stable during the rising edge of MDC. When reading from the BCM5338M, the data field bits are valid after the rising edge of MDC until the next rising edge of MDC.

Idle

A high impedance state of the MDIO line. All tristate drivers are disabled and an external pullup resistor pulls the MDIO line to logic 1. At least one or more clocked idle states are required between frames.

Following are two examples of MII write and read instructions:

- To put a transceiver with PHY address 00001 into Loopback mode, the following MII write instruction must be issued:
  `1111 1111 1111 1111 1111 1111 1111 1111  0101 00001 00000 10 0100 0000 0000 0000`
- To determine if a PHY is in the link pass state, the following MII read instruction must be issued:
  `1111 1111 1111 1111 1111 1111 1111 1111  0110 00001 00001 ZZ ZZZZ ZZZZ ZZZZ ZZZZ`

For the MII read operation, the BCM5338M drives the MDIO line during the second half of the TA field and the Data field (the last 17 bit times).

Accessing All Registers Using The MDC/MDIO Pins

The MDC/MDIO pins can be used to access all the registers described in the Register section using the MDC/MDIO pins instead on the SPI interface. The figures below show the register setup flow chart for accessing the registers via the MDC/MDIO interface.

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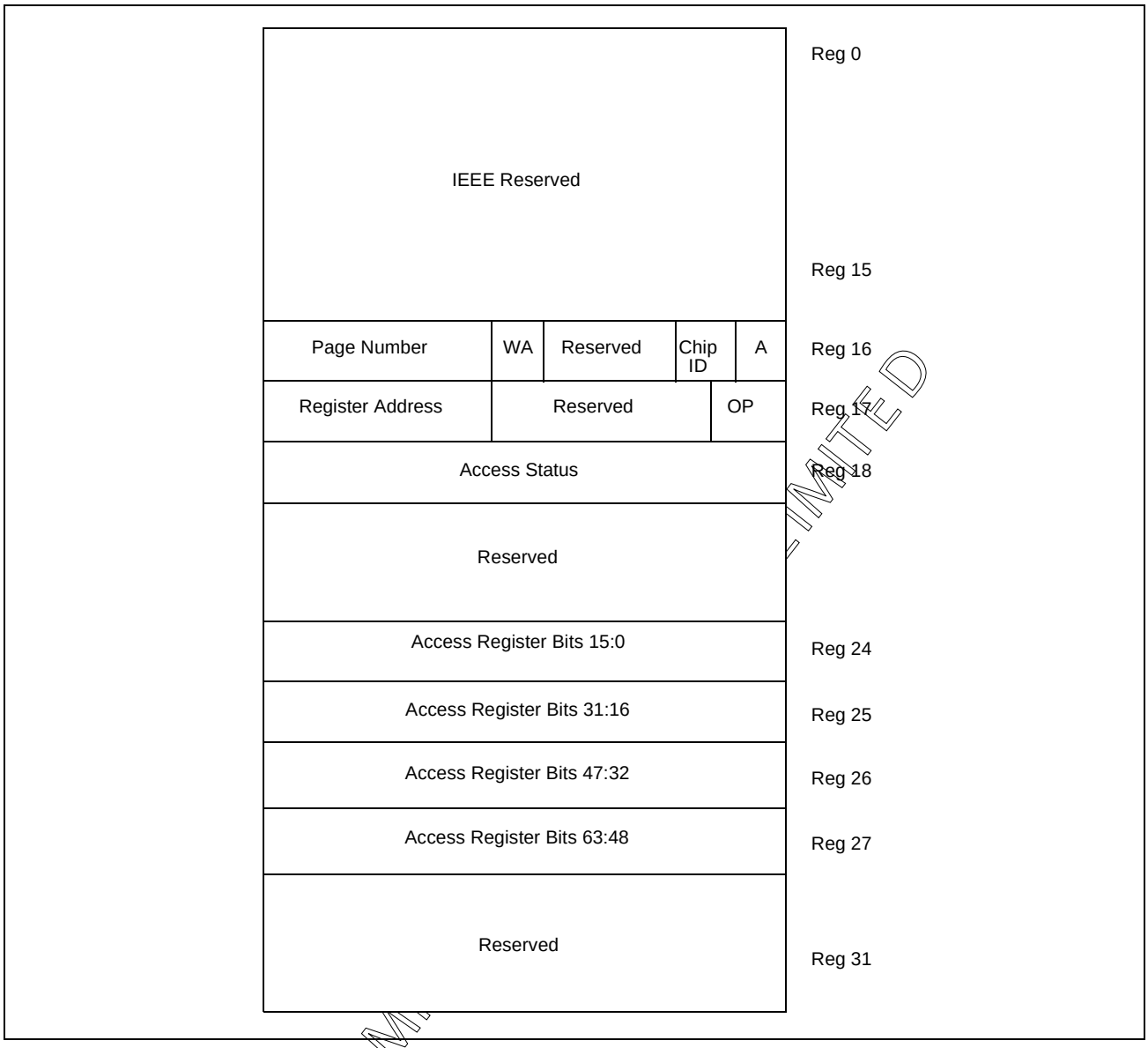

Figure 24: Pseudo-PHY MII Register Definitions

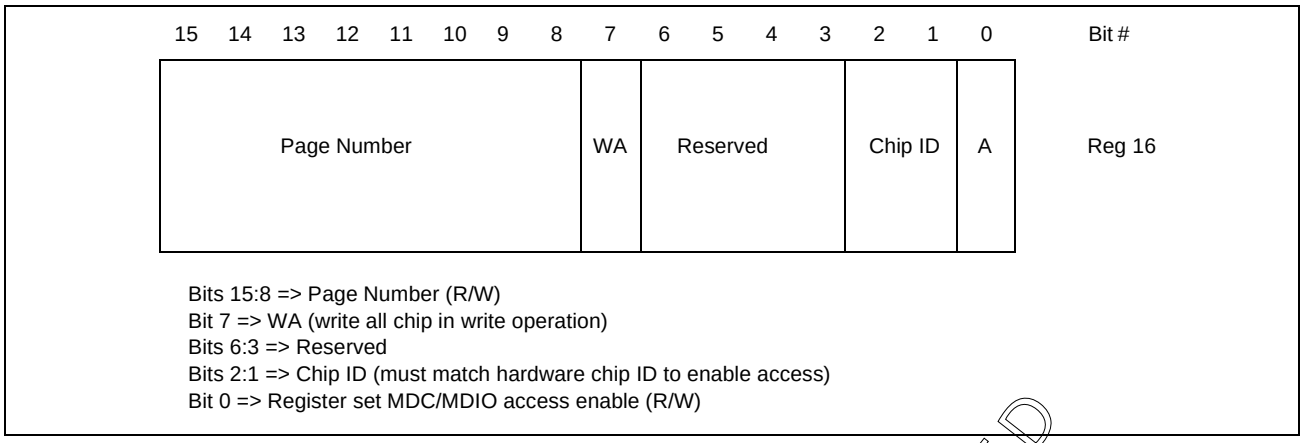

Figure 25: Pseudo-PHY MII Register 16: Register Set Access Control Bit Definition

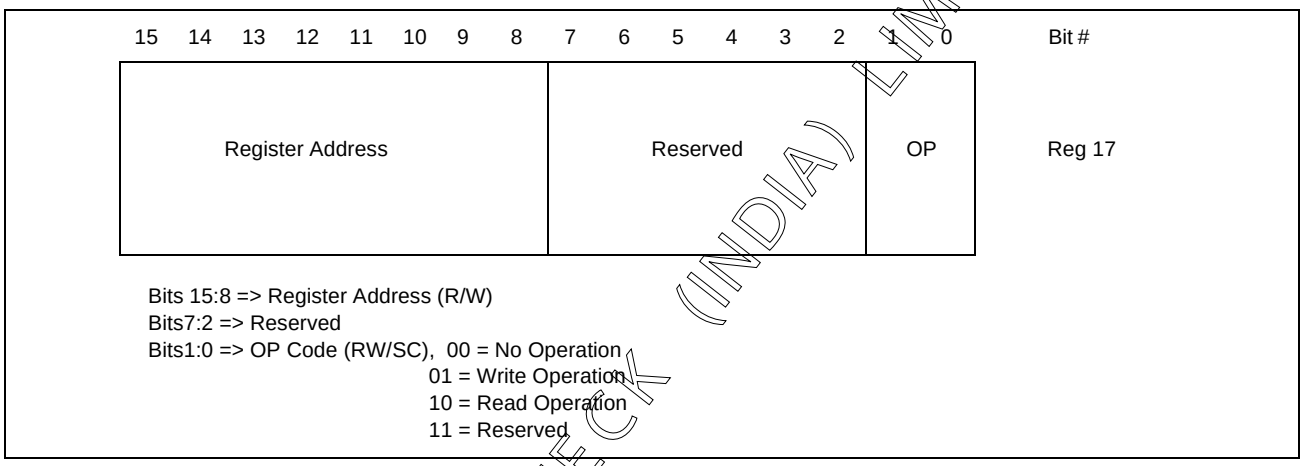

Figure 26: Pseudo-PHY MII Register 17: Register Set Read/Write Control Bit Definition

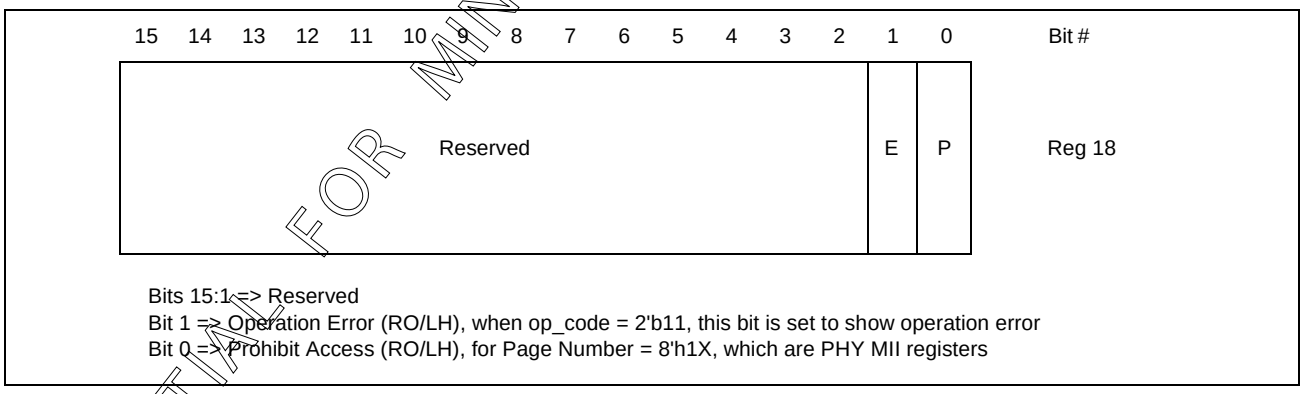

Figure 27: Pseudo-PHY MII Register 18: Register Access Status Bit Definition

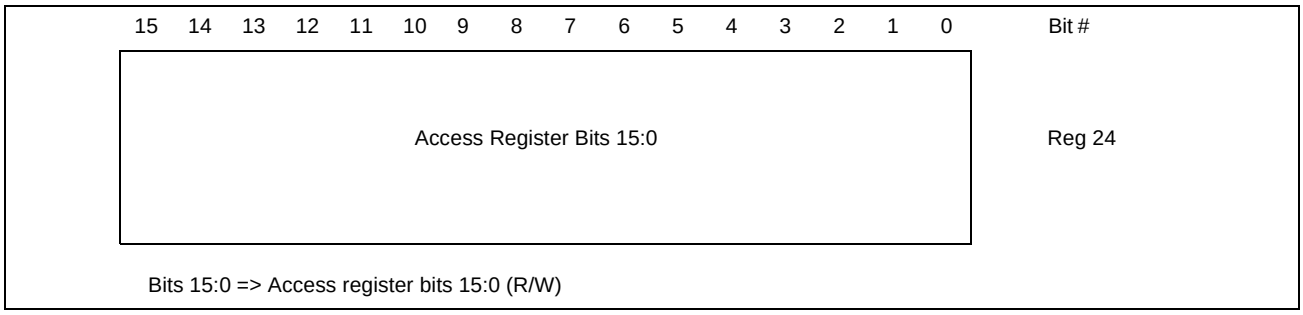

Figure 28: Pseudo-PHY MII Register 24: Access Register Bit Definition

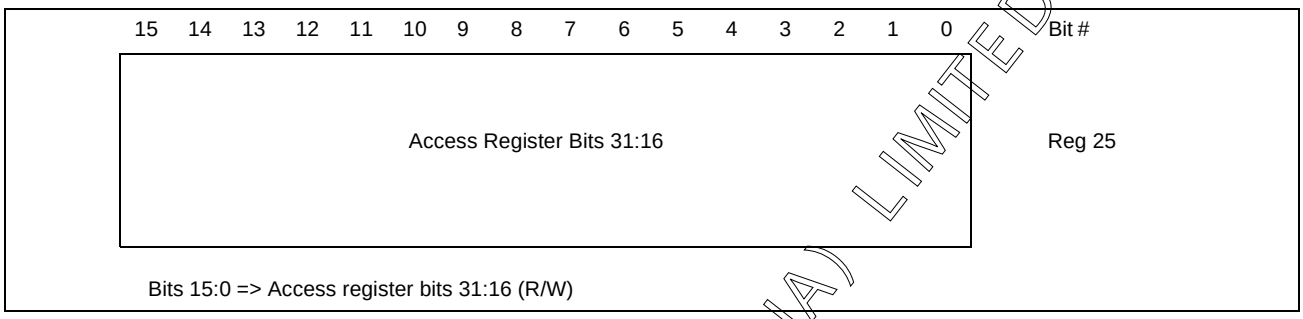

Figure 29: Pseudo-PHY MII Register 25: Access Register Bit Definition

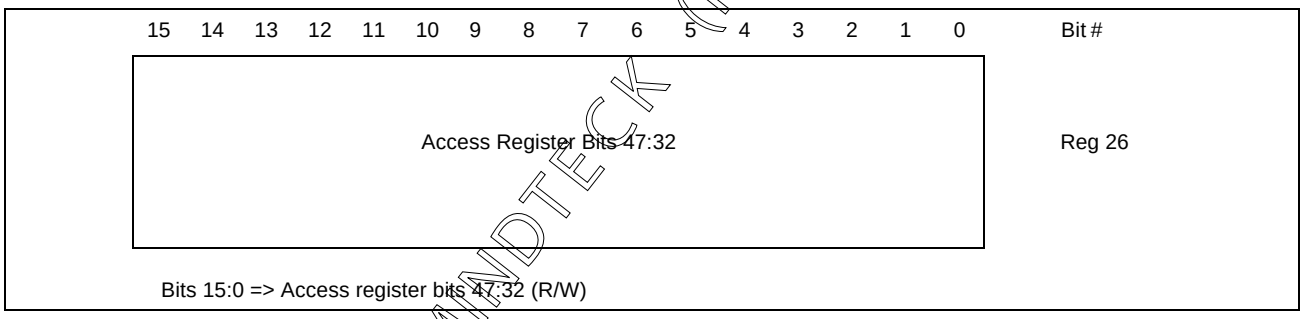

Figure 30: Pseudo-PHY MII Register 26: Access Register Bit Definition

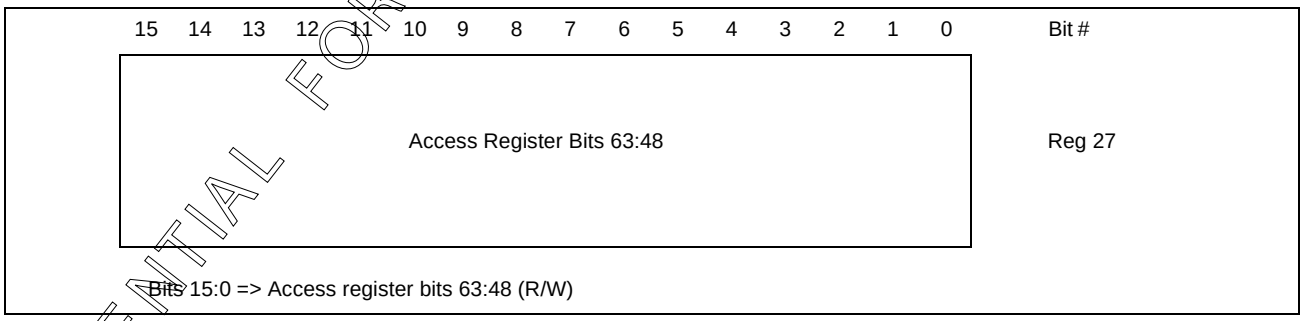

Figure 31: Pseudo-PHY MII Register 27: Access Register Bit Definition

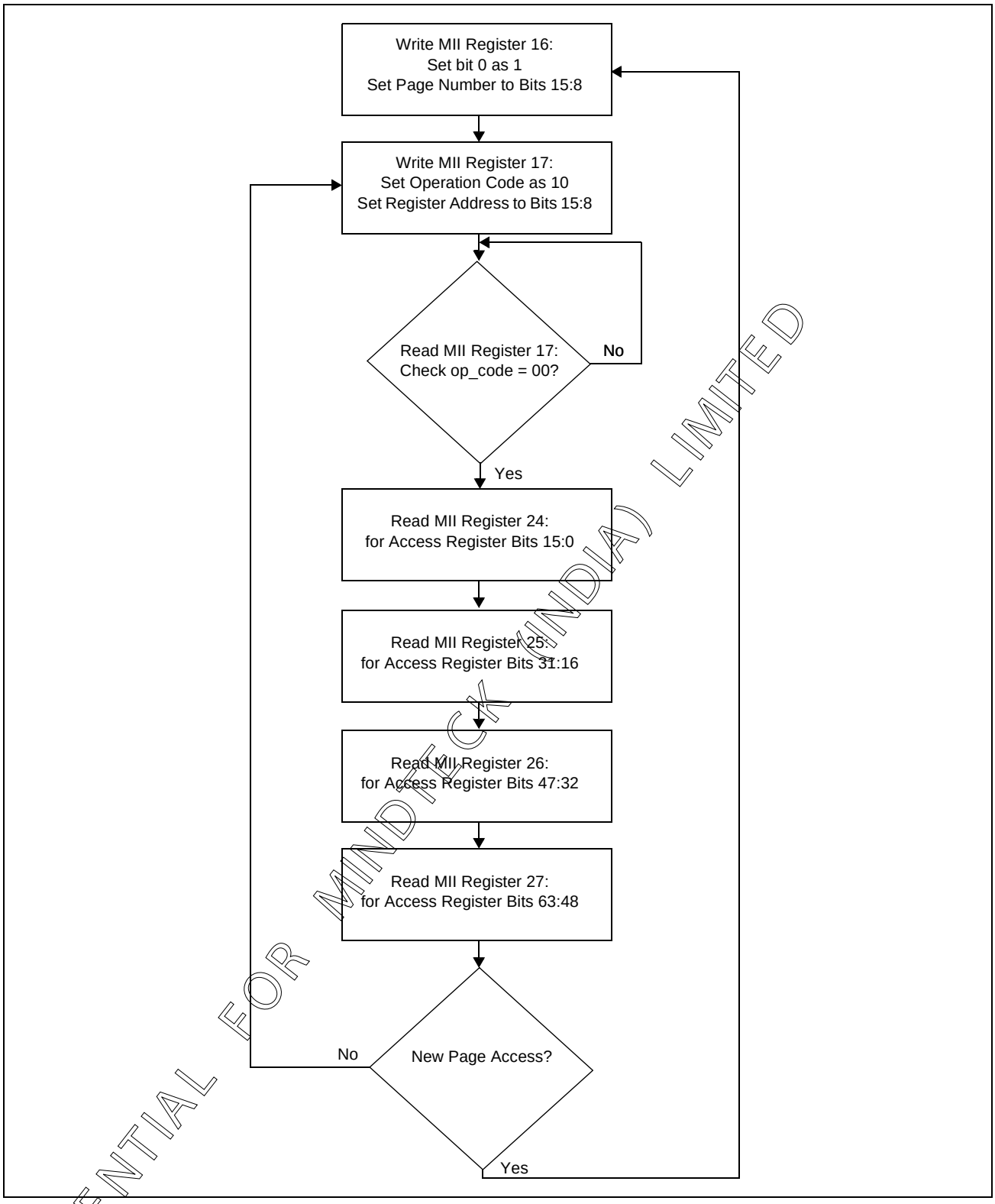

Figure 32: Read Access to the Register Set Via the Pseudo-PHY (Phyad = 11110) MDC/MDIO Path

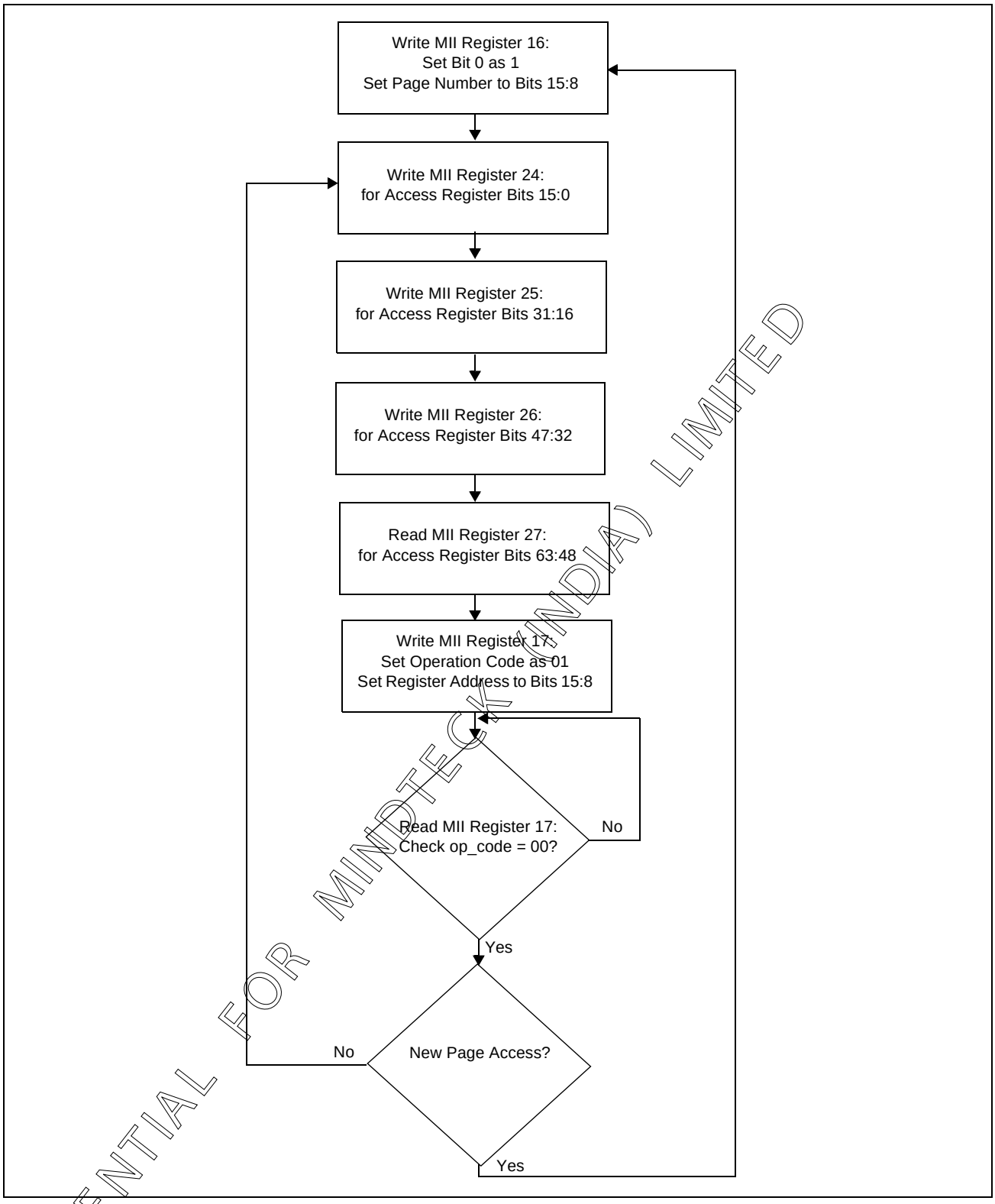

Figure 33: Write Access to the Register Set Via the Pseudo-PHY (Phyad = 11110) MDC/MDIO Path

Section 2: Hardware Signal Definitions

- $\overline{\text{Overline}}$ = Active-low signal
- I = Input
- O = Output
- I/O = Bidirectional
- I_{PU} = Input with internal pullup
- I_{PD} = Input with internal pulldown
- I_S = Input with Schmidtt Trigger
- O_{OD} = Open-drain output
- O_{3S} = Three-state output
- B = Bias
- PWR = Power supply
- GND = Ground

Table 17: Signal Descriptions

Signal Name	*Type*	*Drive (mA)*	*Description*
Media Connections			
RD[1:8]±	I		**Receive Pair.** Differential data from the media is received on the **RD**± signal pair.
TD[1:8]±	O		**Transmit Pair.** Differential data is transmitted to the media on the **TD**± signal pair.
Clock/Reset			
$\overline{\text{RST}}$	I_S		**Reset.** Active Low. Resets the BCM5338M.
XTALI/CK25	I		**25 MHz Crystal/Clock Input.**
XTALO	O		For a single-ended clock signal input, connect a 25.000 MHz (±50 ppm) reference clock to the CK25 pin. This pin must be driven with a continuous clock. Leave XTALO unconnected for this mode of operation. Alternatively, a 25.000 MHz parallel-resonant crystal can be connected between the XTALI/XTALO pins, with a 27 pF capacitor from each pin to GND. ***Note:*** This mode should only be used in a non-expanded system, as all clocks in a multichip system require the same source clock.
MII			
CRS	I_{PD}		**Carrier Sense.** Active high. Indicates traffic on link.
COL	I_{PD}		**Collision Detect.** In half-duplex mode, active high input indicates that a collision has occurred. In full-duplex mode, COL remains low. COL is an asynchronous input signal.
$\overline{\text{LINK}}$	I_{PU}		**Link Status Indicator.** Active low indication of the link status of the transceiver connected at the MII port. When low, the link pass condition is indicated.

Table 17: Signal Descriptions (Cont.)

Signal Name	Type	Drive (mA)	Description
MDIO	I/O_{PD}	8	**Management Data I/O.** This serial input/output bit is used to read from and write to the MII registers of the internal transceivers. The input data value on the MDIO pin is valid and latched on the rising edge of MDC.
MDC	I/O_{PD}	8	**Management Data Clock.** MDC must be provided to the BCM5338M as an input to allow MII management functions. Clock frequencies up to 12.5 MHz are supported. If the BCM5338M detects SCK activity on the SMP, the BCM5338M sources a 2.5 MHz clock to the external PHY device.
RXC	I/O_{PD}	10	**Receive Clock.** 25 MHz input in 100BASE-X mode and 2.5 MHz input in 10BASE-T mode. RXC is expected to be continuously running. RXC may have an irregular period when RXDV= 0 at the beginning of a packet.
RXD[3] RXD[2] RXD[1] RXD[0]	I_{PD} I_{PD} I_{PD} I_{PD}		**Receive Data Inputs.** Nibble-wide receive data. RXD[3] is the most significant bit.
RXDV	I_{PD}		**Receive Data Valid.** Active high. Indicates that a receive frame is in progress, and that the data stream present on the RXD input pins is valid.
RXER	I_{PD}		**Receive Error Detected.** Active high. Indicates that there has been an error during a receive frame.
TXC	I/O_{PD}	10	**Transmit Clock.** For MII mode, 25 MHz input in 100BASE-X mode and 2.5 MHz in 10BASE-T mode. This clock must be a continuously driven input, generated from the PHY.
TXD[3:0]	I/O_{PU}	10	**Transmit Data Output.** Nibble-wide transmit data is output on these pins synchronously to TXC. TXD[3] is the most significant bit. TXD[2] is shared with $\overline{\text{TURBOMII}}$. Although this pin is internally pulled up, but an external pullup, 4.7K is recommended.
TXEN	I/O_{PD}	10	**Transmit Enable.** Indicates that the data nibble is valid on TXD[3:0].
TXER	I/O_{PD}	10	**Transmit Error.** Asserted while TXEN is active to force a bad code into the transmit data stream.
Expansion Port			
ECLKI	I_{PD}		**Expansion Clock In.** Clock input synchronous with EDI. Generated by the adjacent BCM5338M which is driving data on its EDO pins, and used to sample data on the EDI pins of the next BCM5338M in the expansion port chain.
ECLKO	O	16	**Expansion Clock Out.** Synchronous clock sourced from one BCM5338M to the next in the expansion port chain, from EDO to EDI.
EDI[15:0]	I		**Expansion Data Input.** Data is sampled on the rising edge of the internal system clock when EVALIDI is also asserted.

Table 17: Signal Descriptions (Cont.)

Signal Name	Type	Drive (mA)	Description
EDO[15:0]	O	10	**Expansion Data Out.** Contains valid frame data when EVALIDO is also asserted. Data is generated from the rising edge of the internal system clock. Shared with various Configuration interface signals.
ERDYI	I_{PU}		**Expansion Ready In.** The BCM5338M begins data transfers across the expansion interface when asserted and the BCM5338M is ready to transmit at least 32 bytes of data or the remaining bytes of a frame.
ERDYO	O	8	**Expansion Ready Out.** Controls the flow of data into the expansion interface. Indicates the BCM5338M device is ready to accept data on the EDI input bus. Shared with LEDMODE2.
ESOFI	I_{PD}		**Expansion Start of Frame Input.** Indicates the start of a new frame on the EDI bus.
ESOFO	O	10	**Expansion Start of Frame Output.** Delineates start of frames within the data stream provided on EDO. Shared with MII_FDX.
EVALIDI	I_{PD}		**Expansion Valid Input.** Enables the reception of expansion data.
EVALIDO	O	10	**Expansion Data Valid.** When asserted, valid data is present on the EDO bus. Shared with MII_SPD100.
TDM_DATA_IN	I_{PD}		**Data Input**. Port status information is continuously read from the device specific slot within the period marked by the TDM_FRM_IN, allowing each BCM5338M device to monitor the port state of other devices communicating on the expansion port.
TDM_DATA_OUT	O	10	**Data Output.** Port status information is continuously output during a specific slot within the period marked by the TDM_FRM_OUT. Each chip outputs its port state information within one of the four available 48 clock cycle slots, dependent on its CHIP ID. Shared with MDIX_DIS.
TDM_FRM_IN	I_{PD}		**Frame Input.** Monitored by CHIP ID = 0. If no frame pulse is detected, the BCM5338M device sets an internal error flag.
TDM_FRM_OUT	O	10	**Frame Output.** The BCM5338M device with a CHIP ID = 0 takes control of this output and drive a single pulse of one expansion port clock cycle out every 192 clock pulses. This delineates the total time available for all other chips to drive their port state information, at their appropriate slot within this period.
Bias			
RDAC	B		**DAC Bias Resistor.** Adjusts the drive level of the transmit DAC. A 1% precision resistor must be connected between the RDAC pin and GND. See Table 204 on page 220 for the required value.

Table 17: Signal Descriptions (Cont.)

Signal Name	Type	Drive (mA)	Description
LEDs			
LED[1:9]A LED[1:9]B LED[1:9]C	O	8	**Per Port LED Indicators.** For a functional description of these signals, see Table 13 on page 81 and Table 14 on page 82.
LEDCLK	O	8	**LED Shift Clock**. Periodically active to enable the shift of LEDDATA into external registers. Shared with LEDMODE0.
LEDDATA	O	8	**LED Data Output.** Serial LED data is shifted out when LEDCLK is active. For a functional description of these signals, see Table 13 on page 81 and Table 14 on page 82. Shared with LEDMODE1.
Serial Management Port			
MISO	O_{3S}	8	**Master-in/Slave-out.** Output signal from the BCM5338M driven with serial data during a SMP Read operation. Shared with TDO and DO.
MOSI	I_{PU}		**Master-out/Slave-in.** Input signal which receives control and address information for the SMP as well as serial data during Write operations. Shared with TDI and DI.
SCK	I_{PD}		**Serial Clock.** Clock input to the SMP supplied by the SPI master. Supports up to 2 MHz. Shared with TCK.
$\overline{SS}$	I_{PU}		**Slave Select.** Active low signal which enables a SMP Read or Write operation. Shared with TMS.
EEPROM			
CS	O_{PU}	8	**Chip Select.** Active high signal which enables an EEPROM read operation. Shared with TMS and $\overline{SS}$.
DI	O_{PU}	8	**Data In.** Serial data input to the external EEPROM. Shared with TDI and MOSI.
DO	I_{PU}		**Data Out.** Serial data output from the external EEPROM. Shared with TDO and MISO.
SCK	O_{PD}	8	**Serial Data Clock.** Clock output to the EEPROM supplied by the BCM5338M. Shared with TCK and SPI's SCK.
Test Interface			
TCK	I_{PD}		**JTAG Test Clock Input.** Clock input used to synchronize JTAG control and data transfers. If unused, may be left unconnected. Shared with SCK.

Table 17: Signal Descriptions (Cont.)

Signal Name	Type	Drive (mA)	Description
TDI	I_{PU}		**JTAG Test Data Input.** Serial data input to the JTAG TAP Controller. Sampled on the rising edge of TCK. If unused, may be left unconnected. Shared with MOSI.
TDO	O_{3S}	8	**JTAG Test Data Output.** Serial data output from the JTAG TAP Controller. Updated on the falling edge of TCK. Actively driven both high and low when enabled; high impedance otherwise. Shared with MISO.
TEST[1:0]	I_{PD}		**Device Test.** Active high signals enable JTAG functionality. Do not set for normal operation.
TMS	I_{PU}		**JTAG Mode Select Input.** Single control input to the JTAG TAP Controller used to traverse the test-logic state machine. Sampled on the rising edge of TCK. If unused, may be left unconnected. Shared with $\overline{SS}$.
$\overline{TRST}$	I_{PU}		**JTAG Test Reset.** Asynchronous active-low reset input to the JTAG TAP Controller. This reset controls the JTAG state machine when TEST[1:0] is asserted (driven high). The $\overline{TRST}$ input must be driven low to insure the TAP controller initializes to the proper state. Shared with $\overline{RST}$.
Configuration			
BIST_CLRMEM_SEL	I_{PD}		**Selects BIST or Memory Clear.** 0 = Select the memory clear function 1 = Select the BIST function Shares pin with TXD1
CHAIN	I_{PU}		**Transmit Frames to Same Port.** CHAIN = 0: 1 chip, or 2 chips in point-to-point configuration. CHAIN = 1: 3 chips in daisy-chain configuration. Shared with EDO13.
CHIPCNT	I_{PU}		**[EXPMODE, CHAIN, CHIPCNT]** 00x = 1 chip 10x = 2 chips 111 = 3 chips 110 = 4 chips Shares pin with EDO12
CHIPID[1:0]	I_{PD}		**Chip Identifier.** CHIPID[1:0] = Upper two bits of 5-bit address field used by the MII management interface. Chip ID used by the expansion port and SMP in a multiple BCM5338M environment. In a multichip application, the chip ID values must be sequential (i.e., 00,01,10). Shared with EDO[15:14].

Table 17: Signal Descriptions (Cont.)

Signal Name	Type	Drive (mA)	Description
CPU_EPROM_SEL	I_{PU}		**CPU or EPROM Interface Selection.** CPU_EPROM_SEL = 0: Disables SPI interface, and allows for connection to EPROM. CPU_EPROM_SEL = 1: Configures SPI interface to connect to CPU. Shared with TXD3.
EE_93C46	I_{PU}		**Selects EPROM Type.** 0 = 93C56/66 1 = 93C46 Shares pin with TXD0
ENFDXFLOW	I_{PU}		**Enable Automatic Full-duplex Flow Control.** In combination with the results of auto-negotiation, sets the flow control mode. For more information, see Table 1 on page 31. Shared with EDO7.
ENHDXFLOW	I_{PU}		**Enable Automatic Backpressure.** ENHDXFLOW = 0: Half-duplex flow control is disabled. ENHDXFLOW = 1: Half-duplex flow control is enabled. For more information, see Table 1 on page 31. Shared with EDO08.
EXPFREQ[0] EXPFREQ[1]	I_{PD}		**Expansion Port and SYSCLK Clock Frequency Select.** Selects expansion port as well as internal operational clock speed. EXPFREQ[0] shared with EDO00. EXPFREQ[1] shared with EDO01. EXPFREQ[1:0] = 00: 83 MHz (default for 8, 16, and 24 port configurations) EXPFREQ[1:0] = 01: 91 MHz EXPFREQ[1:0] = 10: 100 MHz EXPFREQ[1:0] = 11: 66 MHz
EXPMODE	I_{PU}		**Expansion Port Mode.** EXPMODE = 0: Disables the expansion port. EXPMODE = 1: Activates the expansion port, a high speed full-duplex channel, to interconnect additional BCM5338M devices. Shared with EDO11.
HW_FWDG_EN	I_{PU}		**Forwarding Enable.** HW_FWDG_EN = 0: Frame forwarding is disabled at power-up. Typically implemented to support compliant 802.1 Spanning Tree Protocol in a managed application. HW_FWDG_EN = 1: Frame forwarding is enabled (typical for unmanaged applications). Shared with EDO10.

Table 17: Signal Descriptions (Cont.)

Signal Name	Type	Drive (mA)	Description
LEDMODE[2] LEDMODE[1] LEDMODE[0]	I_{PU} I_{PD} I_{PD}		**LED Mode.** LEDMODE0 shared with LEDCLK. LEDMODE1 shared with LEDDATA. LEDMODE2 shared with ERDYO. For details, see Table 15 on page 84.
MDIX_DIS	I_{PD}		**HP Auto-MDIX Disable.** MDIX_DIS = 0: Automatic TX cable swap detection enabled. MDIX_DIS = 1: Automatic TX cable swap detection disabled. Shared with TDM_DATA_OUT.
$\overline{\text{MII\_FDX}}$	I_{PD}		**MII Default Duplex Operation.** Sets the default duplex setting of the MII port. Can be overridden by software through the MII Port State Override register. $\overline{\text{MII\_FDX}}$ = 1: MII port defaults to half-duplex operation. $\overline{\text{MII\_FDX}}$ = 0: MII port defaults to full-duplex operation. Shared with ESOFO.
$\overline{\text{MII\_SPD100}}$	I_{PD}		**MII Default Speed Operation.** Sets the default speed setting of the MII port. Can be overridden by software through the MII Port State Override register. $\overline{\text{MII\_SPD100}}$ = 0: MII port defaults to 100 Mb/s operation. MII_SPD100 = 1: MII port defaults to 10 Mb/s operation. Shared with EVALIDO.
QOS_EN	I_{PD}		**QoS Enable.** QOS_EN = 0: Disables QoS functionality. QOS_EN = 1: Enables QoS functionality. Shared with EDO[2].
QOS_FC_DIS	I/O_{PU}	10	**QoS Flow Control Disable.** QOS_FC_DIS = 0: 802.3x flow control is enabled when QoS is active. QOS_FC_DIS = 1: 802.3x flow control is disabled when QoS is active (default). Shared with EDO[3].
QOS_PORT_SEL[0] QOS_PORT_SEL[1] QOS_PORT_SEL[2]	I_{PU} I_{PU} I_{PD}		**10/100 Port QOS Priority Setting.** QOS_PORT_SEL[2:0] = 000: All local ports are set to priority 1. QOS_PORT_SEL[2:0] = 001: MII and port 1are set to priority 1. QOS_PORT_SEL[2:0] = 010: MII and ports 1,2 are set to priority 1. QOS_PORT_SEL[2:0] = 011: MII and ports 1,2,3 are set to priority 1. QOS_PORT_SEL[2:0] = 100: MII and ports 1,2,3,4 are set to priority 1. QOS_PORT_SEL[2:0] = 101: MII and ports 1,2,3,4,5 are set to priority 1. QOS_PORT_SEL[2:0] = 110: MII and ports 1,2,3,4,5,6 are set to priority 1. QOS_PORT_SEL[2:0] = 111: MII and ports 1,2,3,4,5,6,7 are set to priority 1. Shared with EDO04, EDO05, EDO06.

Table 17: Signal Descriptions (Cont.)

Signal Name	*Type*	*Drive (mA)*	*Description*
SKIP_SRAMBIST	I_{PD}		**Turn off BIST/Memory Clear Function.** Shares pin with TDM_FRM_OUT.
TURBOMII	I_{PU}		**MII or TURBO MII Interface Selection.** TURBOMII = 0: Configures MII pins to support Turbo MII (txclk is output, rxclk is input, 50 MHz). TURBOMII = 1: Configures MII pins to support connection to an external MII device. Shared with TXD[2]. Although this pin is internally pulled up, but an external pullup, 4.7K is recommended.
Power			
GNDA	GND		**Analog GND.**
GNDBIAS	GND		**Bias Circuit GND.**
GNDC	GND		**Digital Core GND.**
GNDP	GND		**Digital periphery (Output Buffer) GND.**
GNDPLL	GND		**PLL circuit GND.**
GNDXTAL	GND		XTAL circuit GND.
VDDA	PWR		**1.8V analog VDD.**
VDDBIAS	PWR		**3.3V bias circuit VDD.**
VDDC	PWR		**1.8V digital core VDD.**
VDDP	PWR		**3.3V digital periphery (output buffer) VDD.**
VDDPLL	PWR		**1.8V PLL circuit VDD.**
VDDXTAL	PWR		3.3V XTAL VDD.

Section 3: Pin Assignments

Table 18: Pin Assignment by Pin Number

Pin #	Signal Name
1	GNDA
2	NC
3	NC
4	VDDA
5	GNDA
6	RD1-
7	RD1+
8	GNDA
9	TD1-
10	TD1+
11	GNDA
12	TD2+
13	TD2-
14	GNDA
15	RD2+
16	RD2-
17	GNDA
18	VDDA
19	GNDA
20	VDDA
21	GNDA
22	RD3-
23	RD3+
24	GNDA
25	TD3-
26	TD3+
27	GNDA
28	TD4+
29	TD4-
30	GNDA
31	RD4+
32	RD4-
33	GNDA
34	VDDA
35	GNDA
36	VDDC
37	GNDC
38	VDDC
39	GNDC
40	$\overline{\text{LED1A}}$
41	$\overline{\text{LED1B}}$
42	$\overline{\text{LED1C}}$
43	$\overline{\text{LED2A}}$
44	$\overline{\text{LED2B}}$
45	$\overline{\text{LED2C}}$
46	VDDP
47	GNDP
48	$\overline{\text{LED3A}}$
49	$\overline{\text{LED3B}}$
50	$\overline{\text{LED3C}}$
51	$\overline{\text{LED4A}}$
52	$\overline{\text{LED4B}}$
53	$\overline{\text{LED4C}}$
54	VDDBIAS
55	RDAC
56	GNDBIAS
57	VDDPLL
58	VDDXTAL
59	XTALI/CK25
60	XTALO
61	GNDXTAL
62	GNDPLL
63	VDDA
64	GNDA
65	RD5-
66	RD5+
67	GNDA
68	TD5-
69	TD5+
70	GNDA
71	TD6+
72	TD6-
73	GNDA
74	RD6+
75	RD6-
76	GNDA
77	VDDA
78	GNDA
79	GNDA
80	VDDA
81	GNDA
82	RD7-
83	RD7+
84	GNDA
85	TD7-
86	TD7+
87	GNDA
88	TD8+
89	TD8-
90	GNDA
91	RD8+
92	RD8-
93	GNDA
94	VDDA
95	GNDA
96	TEST1
97	TEST0
98	MDIO
99	MDC
100	MISO/TDO/DO
101	MOSI/TDI/DI
102	SCK/TCK/SCK
103	$\overline{\text{SS}}$/TMS/CS
104	$\overline{\text{LED5A}}$
105	$\overline{\text{LED5B}}$
106	$\overline{\text{LED5C}}$
107	$\overline{\text{LED6A}}$
108	$\overline{\text{LED6B}}$
109	$\overline{\text{LED6C}}$
110	VDDP
111	GNDP
112	$\overline{\text{LED7A}}$
113	$\overline{\text{LED7B}}$
114	$\overline{\text{LED7C}}$
115	VDDP
116	GNDP
117	$\overline{\text{LED8A}}$
118	$\overline{\text{LED8B}}$
119	$\overline{\text{LED8C}}$
120	$\overline{\text{LED9A}}$
121	$\overline{\text{LED9B}}$
122	$\overline{\text{LED9C}}$
123	GNDC
124	VDDC
125	VDDC
126	GNDC
127	$\overline{\text{RST}}$/$\overline{\text{TRST}}$
128	LEDCLK/LEDMODE0
129	LEDDATA/LEDMODE1
130	EVALIDO/$\overline{\text{MII\_SPD100}}$
131	ESOFO/$\overline{\text{MII\_FDX}}$
132	ERDYI
133	ECLKO
134	TDM_FRM_OUTSKIP_SRAMBIST
135	TDM_DATA_OUT/MDIX_DIS
136	VDDP
137	GNDP
138	EDO00/EXPFREQ0
139	EDO01/EXPFREQ1
140	EDO02/QOS_EN
141	EDO03/QOS_FC_DIS
142	EDO04/QOS_PORT_SEL[0]
143	EDO05/QOS_PORT_SEL[1]
144	EDO06/QOS_PORT_SEL[2]
145	EDO07/ENFDXFLOW
146	VDDP
147	GNDP
148	EDO08/ENHDXFLOW

Pin #	Signal Name
149	EDO09
150	EDO10/HW_FWDG_EN
151	EDO11/EXPMODE
152	EDO12/CHIPCNT
153	EDO13/CHAIN
154	EDO14/CHIPID0
155	EDO15/CHIPID1
156	$\overline{\text{LINK}}$
157	CRS
158	COL
159	TXD3/CPU_EPROM_SEL
160	TXD2/$\overline{\text{TURBOMII}}$
161	TXD1/ BIST_CLRMEM_SEL
162	VDDP
163	VDDC
164	GNDC
165	GNDP
166	TXD0/EE_93C46
167	TXEN
168	TXC
169	TXER
170	VDDP
171	GNDP
172	RXER
173	RXC
174	RXDV
175	RXD0
176	RXD1
177	RXD2
178	RXD3
179	VDDC
180	GNDC
181	GNDP
182	VDDP
183	EDI15
184	EDI14
185	EDI13
186	EDI12
187	EDI11
188	EDI10
189	VDDC
190	GNDC

Pin #	Signal Name
191	EDI09
192	EDI08
193	EDI07
194	EDI06
195	EDI05
196	EDI04
197	EDI03
198	EDI02
199	VDDP
200	GNDP
201	EDI01
202	EDI00
203	TDM_DATA_IN
204	TDM_FRM_IN
205	ECKLI
206	ERDYO/LEDMODE2
207	ESOFI
208	EVALIDI

Table 19: Pin Assignment by Signal Name

Pin #	Signal Name
158	COL
157	CRS
205	ECKLI
133	ECLKO
202	EDI00
201	EDI01
198	EDI02
197	EDI03
196	EDI04
195	EDI05
194	EDI06
193	EDI07
192	EDI08
191	EDI09
188	EDI10
187	EDI11
186	EDI12
185	EDI13
184	EDI14
183	EDI15
138	EDO00/EXPFREQ0
139	EDO01/EXPFREQ1
140	EDO02/QOS_EN
141	EDO03/QOS_FC_DIS
142	EDO04/ QOS_PORT_SEL[0]
143	EDO05/ QOS_PORT_SEL[1]
144	EDO06/ QOS_PORT_SEL[2]
145	EDO07/ENFDXFLOW
148	EDO08/ENHDXFLOW
149	EDO09
150	EDO10/HW_FWDG_EN
151	EDO11/EXPMODE
152	EDO12/CHIPCNT
153	EDO13/CHAIN
154	EDO14/CHIPID0
155	EDO15/CHIPID1
132	ERDYI
206	ERDYO/LEDMODE2
207	ESOFI
131	ESOFO/MII_FDX

Pin #	Signal Name
208	EVALIDI
130	EVALIDO/MII_SPD100
1	GNDA
5	GNDA
8	GNDA
11	GNDA
14	GNDA
17	GNDA
19	GNDA
21	GNDA
24	GNDA
27	GNDA
30	GNDA
33	GNDA
35	GNDA
64	GNDA
67	GNDA
70	GNDA
73	GNDA
76	GNDA
78	GNDA
79	GNDA
81	GNDA
84	GNDA
87	GNDA
90	GNDA
93	GNDA
95	GNDA
56	GNDBIAS
37	GNDC
39	GNDC
123	GNDC
126	GNDC
164	GNDC
180	GNDC
190	GNDC
47	GNDP
111	GNDP
116	GNDP
137	GNDP
147	GNDP
165	GNDP

Pin #	Signal Name
171	GNDP
181	GNDP
200	GNDP
62	GNDPLL
61	GNDXTAL
40	LED1A
41	LED1B
42	LED1C
43	LED2A
44	LED2B
45	LED2C
48	LED3A
49	LED3B
50	LED3C
51	LED4A
52	LED4B
53	LED4C
104	LED5A
105	LED5B
106	LED5C
107	LED6A
108	LED6B
109	LED6C
112	LED7A
113	LED7B
114	LED7C
117	LED8A
118	LED8B
119	LED8C
120	LED9A
121	LED9B
122	LED9C
128	LEDCLK/LEDMODE0
129	LEDDATA/LEDMODE1
156	LINK
99	MDC
98	MDIO
100	MISO/TDO/DO
101	MOSI/TDI/DI
2	NC
3	NC
6	RD1-

Pin #	Signal Name
7	RD1+
16	RD2-
15	RD2+
22	RD3-
23	RD3+
32	RD4-
31	RD4+
65	RD5-
66	RD5+
75	RD6-
74	RD6+
82	RD7-
83	RD7+
92	RD8-
91	RD8+
55	RDAC
127	RST/TRST
173	RXC
175	RXD0
176	RXD1
177	RXD2
178	RXD3
174	RXDV
172	RXER
102	SCK/TCK/SCK
103	SS/TMS/CS
9	TD1-
10	TD1+
13	TD2-
12	TD2+
25	TD3-
26	TD3+
29	TD4-
28	TD4+
68	TD5-
69	TD5+
72	TD6-
71	TD6+
85	TD7-
86	TD7+
89	TD8-
88	TD8+

Pin #	Signal Name
203	TDM_DATA_IN
135	TDM_DATA_OUT/ MDIX_DIS
204	TDM_FRM_IN
134	TDM_FRM_OUT/ SKIP_SRAMBIST
97	TEST0
96	TEST1
168	TXC
166	TXD0/EE_93C46
161	TXD1/ BIST_CLRMEM_SEL
160	TXD2/$\overline{\text{TURBOMII}}$
159	TXD3/CPU_EPROM_SEL
167	TXEN
169	TXER
4	VDDA
18	VDDA
20	VDDA
34	VDDA
63	VDDA
77	VDDA
80	VDDA
94	VDDA
54	VDDBIAS
36	VDDC
38	VDDC
124	VDDC
125	VDDC
163	VDDC
179	VDDC
189	VDDC
46	VDDP
110	VDDP
115	VDDP
136	VDDP
146	VDDP
162	VDDP
170	VDDP
182	VDDP
199	VDDP
57	VDDPLL
58	VDDXTAL
59	XTALI/CK25
60	XTALO

Section 4: Register Definitions

Register Definitions

The BCM5338M register set can be accessed through the SMP. The register space is organized into pages, each contains a certain set of registers. The following table lists the pages defined in the BCM5338M.

To access a page, the page register (0xFF) is written with the page value. The registers contained in the page can then be accessed by their address.

Table 20: Global Page Register Map

Page	*Description*
00h	"Control Registers" on page 107.
01h	"Status Registers" on page 114.
02h	"Management Mode Registers" on page 118.
03h	"MIB Autocast Registers" on page 125.
04h	"ARL Control Registers" on page 128.
05h	"ARL Access Registers" on page 132.
06h	"Management Frame Access Registers" on page 141.
07h	Reserved.
08h	"Generic Memory Access Registers" on page 143.
09h	Reserved.
0Ah	"Priority Queue Control Registers" on page 144.
0Bh–0Fh	Reserved.
10h	Port 0 MII registers (10/100 Port 0).
11h	Port 1 MII registers (10/100 Port 1).
12h	Port 2 MII registers (10/100 Port 2).
13h	Port 3 MII registers (10/100 Port 3).
14h	Port 4 MII registers (10/100 Port 4).
15h	Port 5 MII registers (10/100 Port 5).
16h	Port 6 MII registers (10/100 Port 6).
17h	Port 7 MII registers (10/100 Port 7).
18h	Port 8 MII registers (MII/IMP Port).
19h–1Fh	Reserved.
20h	Port 0 MIB registers (10/100 Port 0).
21h	Port 1 MIB registers (10/100 Port 1).
22h	Port 2 MIB registers (10/100Port 2).
23h	Port 3 MIB registers (10/100 Port 3).

Table 20: Global Page Register Map (Cont.)

Page	*Description*
24h	Port 4 MIB registers (10/100 Port 4).
25h	Port 5 MIB registers (10/100 Port 5).
26h	Port 6 MIB registers (10/100 Port 6).
27h	Port 7 MIB registers (10/100 Port 7).
28h	Port 8 MIB registers (MII/IMP Port).
29h–2Fh	Reserved.
30h	"QoS Registers" on page 172.
31h	"Port-Based VLAN Registers" on page 178.
32h	"MAC-Based Trunking Registers" on page 181.
33h	Reserved.
34h	"802.1Q VLAN Registers" on page 182.
35h	"Broadcast/Multicast Suppression Registers" on page 191.
36h–3Fh	Reserved.
40h	"802.1x Registers" on page 192.
41h	"MAC Address Security Registers" on page 195.
42h	"Ingress/Egress Rate Control Registers" on page 200.
43h	"802.1s Multiple Spanning Tree Registers" on page 204.
44h–EFh	Reserved.
F0h-F7h	SPI Data I/O 0-7—Table 190: "SPI Registers (Maps Globally to All Pages)," on page 209
F8h–FDh	Reserved.
FEh	"SPI Status Register" on page 209.
FFh	"Page Register" on page 210.

Control Registers

Table 21: Control Registers (Page 00h)

Addr	*Bits*	*Register Name*
00h	8	10/100 Port Control register 0
01h	8	10/100 Port Control register 1
02h	8	10/100 Port Control register 2
03h	8	10/100 Port Control register 3
04h	8	10/100 Port Control register 4
05h	8	10/100 Port Control register 5
06h	8	10/100 Port Control register 6
07h	8	10/100 Port Control register 7
08h	8	MII/IMP Port Control register 8
09h	Reserved	
0Ah	8	SMP Control register
0Bh	8	Switch Mode register
0Ch–0Dh	Reserved	
0Eh	8	MII Port State Override register
0Fh	8	Power-Down mode
10h–20h	Reserved	
21h	8	New Control register
22h–23h	16	WAN Port Select register
24h–25h	16	Protected Port Select register
26h–27h	16	Software Flow Control register
28h–29h	16	Unicast Lookup Fail Drop MAP register
2Ah–2Bh	16	Multicast Lookup Fail Drop MAP register
2Ch–FEh	Reserved	
FFh	8	Page register

10/100 Port Control Register [0:7]

Table 22: 10/100 Port Control Register (Page 00h: Address 00d–07d, 00h–07h)

Bit	Name	R/W	Description	Default
7:5	STP_STATE[2:0]	R/W	The CPU writes the current computed states of its spanning tree algorithm for this port: 000 = No spanning tree (unmanaged mode). 001 = Disabled state (default for managed mode). 010 = Blocking state. 011 = Listening state. 100 = Learning state. 101 = Forwarding state. 110–111 = Reserved.	Controlled by the HW_FWDG_EN Strap option
1	TX_DISABLE	R/W	Disables the transmit function of the port at the MAC level.	0
0	RX_DISABLE	R/W	Disables the receive function of the port at the MAC level.	0

MII/IMP Port Control Register [8]

Table 23: MII/IMP Port Control Register (Page 00h: Address 08d, 08h)

Bit	Name	R/W	Description	Default
7:5	STP_STATE[2:0]	R/W	**Spanning Tree Protocol State.** CPU writes the current computed states of its spanning tree algorithm for this port. 000 = No spanning tree (unmanaged mode). 001 = Disabled state. 010 = Blocking state. 011 = Listening state. 100 = Learning state. 101 = Forwarding state. 110–111 = Reserved. Ignored when SW_FWDG_MODE = Unmanaged.	001 (controlled by HW_FWDG_EN strap option)
4	RX_UCST_EN	R/W	**Receive Unicast Enable.** Enables the receipt of unicast frames on the IMP, when the IMP is configured as the frame management port, and the frame was flodded due to no matching address table entry. When cleared, unicast frames that meet the mirror ingress/egress rules are still forwarded to the frame management port. Ignored if the IMP is not selected as the frame management port.	0

Table 23: MII/IMP Port Control Register (Page 00h: Address 08d, 08h) (Cont.)

Bit	Name	R/W	Description	Default
3	RX_MCST_EN	R/W	**Receive Multicast Enable.** Enables the receipt of multicast frames on the IMP, when the IMP is configured as the frame management port, and the frame was flooded due to no matching address table entry. When cleared, multicast frames that meet the Mirror Ingress/Egress Rules are still forwarded to the frame management port. Ignored if the IMP is not selected as the frame management port.	0
2	RX_BCST_EN	R/W	**Receive Broadcast Enable.** Enables the receipt of broadcast frames on the IMP, when the IMP is configured as the frame management port. When cleared, multicast frames that meet the Mirror Ingress/Egress Rules are still forwarded to the frame management port. Ignored if the IMP is not selected as the frame management port.	0
1	TX_DISABLE	R/W	Disables the transmit function of the port at the MAC level.	0
0	RX_DISABLE	R/W	Disables the receive function of the port at the MAC level.	0

SMP Control Register

Table 24: SMP Control Register (Page 00h: Address 10d, 0Ah)

Bit	Name	R/W	Description	Default
7–5	RESERVED	RO		0
4	RX_UCST_EN	R/W	**Receive Unicast Enable.** Enables the receipt of unicast frames on the SMP, when the SMP is configured as the frame management port, and the frame was flooded due to no matching address table entry. When cleared, unicast frames that meet the mirror ingress/egress rules are still forwarded to the frame management port. Ignored if the SMP is not selected as the frame management port.	0
3	RX_MCST_EN	R/W	**Receive Multicast Enable.** Enables the receipt of multicast frames on the SMP, when the SMP is configured as the frame management port, and the frame was flooded due to no matching address table entry. When cleared, multicast frames that meet the mirror ingress/egress rules are still forwarded to the frame management port. Ignored if the SMP is not selected as the frame management port.	0

Table 24: SMP Control Register (Page 00h: Address 10d, 0Ah) (Cont.)

Bit	Name	R/W	Description	Default
2	RX_BCST_EN	R/W	**Receive Broadcast Enable.** Enables the receipt of broadcast frames on the SMP, when the SMP is configured as the frame management port. When cleared, multicast frames that meet the mirror ingress/ egress rules are still forwarded to the frame management port. Ignored if the SMP is not selected as the frame management port.	0
1:0	RESERVED	RO	–	0

Switch Mode Register

Table 25: Switch Mode Register (Page 00h: Address 11d, 0Bh)

Bit	Name	R/W	Description	Default
7:6	RESERVED	RO	–	11
5:4	IPG	R/W	**Programmable Interpacket Gap.** 00 = Reserved. 01 = Reserved. 10 = 92-bit time. 11 = 96-bit time.	11
3	NOBLKCD	R/W	**Do Not Block Carrier Detected Signal .** 1 = Do not block, txport always defers to crs. 0 = Block CD (compatible with BCM5328).	0
2	RESERVED	RO	–	01
1	SW_FWDG_EN	R/W	**Software Forwarding Enable.** SW_FWDG_EN=1 = Frame forwarding is enabled. SW_FWDG_EN=0 = Frame forwarding is disabled. Read from HW_FWDG_EN pin on power-on. Can be overwritten subsequently. For managed switch implementations, the switch should be configured to disable forwarding on power-on, to allow the processor to configure the internal address table and other parameters, before frame forwarding is enabled.	HW_FWDG_EN pin
0	SW_FWDG_MODE	R/W	**Software Forwarding Mode.** Programmed from the inverse of the HW_FWDG_EN pin at power-on. Can be overwritten subsequently. 0 = Unmanaged mode. 1 = Managed mode. The ARL treats Reserved Multicast addresses differently dependent on this selection. See Table 5 on page 43 for a precise definition.	Inverse of HW_FWDG_EN pin

MII Port State Override Register

Table 26: MII Port State Override Register (Page 00h: Address 14d, 0Eh)

Bit	Name	R/W	Description	Default
7	MII_SW_OR	R/W	**MII Software Override.** 0 = Use MII hardware pin status 1 = Use contents of this register	0
6	EN_IMP_RX_PAUSE _NOTAG	R/W	This bit is used when MII port configured as management. 0 = RXMAC detect PAUSE frame with BRCM_TAG. 1 = RXMAC detect standard PAUSE frame.	0
5	RESERVED	RO	–	0
4	RvMII_EN	R/W	**Reverse MII Enable.** 0 = Normal MII mode 1 = Enable RvMII mode	0
3	LP_FLOW_CNTRL	R/W	**Link Partner Flow Control Capability.** 0 = Not PAUSE capable 1 = PAUSE capable	0
2	SPEED100	R/W	**Speed.** 0 = 10 Mbps 1 = 100 Mbps	0
1	FDX	R/W	**Full-duplex.** 0 = Half-duplex 1 = Full-duplex	0
0	LINK	R/W	**Link Status.** 0 = Link fail 1 = Link pass	0

Power-Down Mode Register

Table 27: Power-Down Mode Register (Page 00h: Address 15d, 0Fh)

Bit	Name	R/W	Description	Default
7:1	PORTx_POWER_DOWN	R/W	**Individual Port Power-Down Register.** Disables all clocking to an individual PHY port. 0 = PHY is enabled. 1 = PHY is disabled.	0
0	PORT0_POWER_DOWN	R/W	Never write this bit as anything but 0.	0

New Control Register

Table 28: New Control Register (Page 00h: Address 33d, 21h)

Bit	Name	R/W	Description	Default
7	MLF_FM_EN	R/W	**Multicast Lookup Fail Forward Map Enable.** When set to: 1, any incoming packets with multicast DA not in the ARL table follow the Multicast Lookup Fail Forward Map register (page 00h; offset 2ah). 0, any incoming packets with multicast DA not in the ARL table flood.	0
6	ULF_FM_EN	R/W	**Unicast Lookup Fail Forward Map Enable.** When set to: 1, any incoming packets with unicast DA not in the ARL table follow Unicast Lookup Fail Forward Map Register (page 00h; offset 28h). 0, any incoming packets with unicast DA not in the ARL table flood.	0
5	BUF_RPT	R/W	**Buffer Repeat Mode.** When set to 1, any incoming packets bypasses DA checking and flooding to other ports.	0
4	LED_SW	R/W	**LED Software Override Control Mode.** 1 = Software could override LED mode (the following bit 3:1). 0 = Using strap pins to decide LED mode.	0
3:1	LED_mode	R/W	LED mode.	LEDMODE[2:0]
0	IP_MULTICAST	R/W	Must be set to 1 to support Multicast addresses in the ARL table.	0

WAN Port Select Register

Table 29: WAN Port Select Register (Page 00h: Address 34–35d, 22–23h)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	–	0
9	EN_MAN2WAN	R/W	0 = Management port only uses egress direct frame to WAN port 1 = Management port can send non-egress direct frames to WAN port	0
8:0	Wan_select	R/W	Set the assigned WAN port to 1. ***Example:*** If port 0 is assigned as WAN port, set to 0_0000_0001. ***Note:*** Only ports located on chip 0 can be configured as the WAN port. In multiple chip designs, this port map must be the same in all chips although it only is used by chip 0. The management port cannot be configured as a WAN port.	0

Protected Port Select Register

Table 30: Protected Port Select Register (Page 00h: Address 36–37d, 24–25h)

Bit	Name	R/W	Description	Default
8:0	PROT_select	R/W	Set the assigned Protected port to 1: ***Example:*** If port 0 is assigned as Protected port, set to 0_0000_0001. ***Note:*** The management port cannot be configured as a protected port.	0

Software Flow Control Register

Table 31: Software Flow Control Register (Page 00h: Address 38–39d, 26–27h)

Bit	Name	R/W	Description	Default
9	SW_FLOW_CON_EN	R/W	Enable software override flow control result.	0
8:0	SW_FLOW_CON	R/W	Software to disable full/half duplex flow control for per port: 1 = Enable 0 = Disable	1FF

Unicast Lookup Fail Forward Map Register

Table 32: Unicast Lookup Fail Forward Map Register (Page 00h: Address 40–41d, 28–29h)

Bit	Name	R/W	Description	Default
15:11	RSEV	R/RO	Reserved	0
10:0	ULF_FORWARD_MAP[10:0]	R/W	**Unicast Lookup Fail Forward Map.** Bit 7–0 = Local 10/100 port. Bit 8 = MII port. Bit 9 = Reserved. Bit 10 = SPI port. Set bit[6], ULF_FM_EN of New Control register (Page 00, Address 21h) to enable this feature.	0

Multicast Lookup Fail Forward Map Register

Table 33: Multicast Lookup Fail Forward Map Register (Page 00h: Address 42–43d, 2a–2bh)

Bit	Name	R/W	Description	Default
15:11	RSEV	R/RO	Reserved	0

Table 33: Multicast Lookup Fail Forward Map Register (Page 00h: Address 42–43d, 2a–2bh) (Cont.)

BIt	Name	R/W	Description	Default
10:0	MLF_FORWARD_MAP[10:0]	R/W	**Multicast Lookup Fail Forward Map.** Bit 7–0 = Local 10/100 port. Bit 8 = MII port Bit 9 = Reserved Bit 10 = SPI port Set bit[7], MLF_FM_EN of New Control register (Page 00, Address 21h) to enable this feature.	0

Status Registers

Table 34: Status Registers (Page 01h)

Addr	Bits	Register Name
00h–01h	16	Link Status Summary
02h–03h	16	Link Status Change
04h–05h	16	Port Speed Summary
06h–07h	16	Duplex Status Summary
08h–09h	16	PAUSE Status Summary
0Ah–0Bh	Reserved	
0Ch–0Dh	16	Source Address Change
0Eh–0Fh	Reserved	
10h–15h	48	Last Source Address Port 0
16h–1Bh	48	Last Source Address Port 1
1Ch–21h	48	Last Source Address Port 2
22h–27h	48	Last Source Address Port 3
28h–2Dh	48	Last Source Address Port 4
2Eh–33h	48	Last Source Address Port 5
34h–39h	48	Last Source Address Port 6
3Ah–3Fh	48	Last Source Address Port 7
40h–45h	48	Last Source Address MII Port
46h	8	BIST Status register
47h–FEh	Reserved	
FFh	8	Page register

Link Status Summary

Table 35: Link Status Summary Register (Page 01h: Address 00dQQ–01d, 00h–01h)

BIt	Name	R/W	Description	Default
15:9	RESERVED	RO	–	0
8:0	LINK_STATUS[8:0]	RO	**Link Status.** The 9-bit field indicating the Link Status for each 10/100BASE-T port and the MII port (bits 0–7 = 10/100BASE-T ports, bit 8 = MII port). 0 = Link fail. 1 = Link pass. ***Note:*** The link status for the MII port can only be reported for an external transceiver by: (a) Using the LINK pin to pass the transceiver's state to the BCM5338M. (b) Using the CPU to read the link status via the MDC/MDIO interface and write this back to the MII Port Status Override register (Page 0h, Address 14h).	0

Link Status Change

Table 36: Link Status Change Register (Page 01h: Address 02d–03d, 02h–03h)

BIt	Name	R/W	Description	Default
15:9	RESERVED	RO	–	0
8:0	LINK_STATUS_CHANGE[8:0]	RC	**Link Status Change.** The 9-bit field indicating that the Link Status for an individual 10/100BASE-T port or MII port had changed since the last read operation (bits 0–7 = 10/100BASE-T ports, bit 8 = MII port). Upon change of link status, a bit remains set until cleared by a read operation. 0 = Link status constant. 1 = Link status change. ***Note:*** The link status change for the MII port can only be reported for an external transceiver by: (a) Using the LINK pin to pass the transceiver's state to the BCM5338M. (b) Using the CPU to read the link status via the MDC/MDIO interface and write this back to the MII Port Status Override register (Page 0h, Address 14h).	0

Port Speed Summary

Table 37: Port Speed Summary Register (Page 01h: Address 04d–05d, 04h–05h)

Bit	Name	R/W	Description	Default
15:9	RESERVED	RO	–	0
8:0	PORT_SPEED[8:0]	RO	**Port Speed.** The 9-bit field indicating the operating speed for each 10/100BASE-T port and the MII port (bits 0–7 = 10/100BASE-T ports, bit 8 = MII port). 0 = 10 Mbps 1 = 100 Mbps ***Note:*** The port speed for the MII port can only be reported for an external transceiver by: (a) Using the SPD100 strap to pass the transceiver's default state to the BCM5338M. (b) Using the CPU to read the port speed via the MDC/MDIO interface and write this back to the MII Port Status Override register (Page 0h, Address 14h).	0

Duplex Status Summary

Table 38: Duplex Status Summary Register (Page 01h: Address 06d–07d, 06h–07h)

Bit	Name	R/W	Description	Default
15:9	RESERVED	RO	–	0
8:0	DUPLEX_STATE[8:0]	RC	**Duplex State.** The 9-bit field indicating the half-duplex/full duplex state for each 10/100BASE-T port and the MII port (bits 0–7 = 10/100BASE-T ports, bit 8 = MII port). 0 = Half-duplex. 1 = Full-duplex.	0

Pause Status Summary

Table 39: Pause Status Summary Register (Page 01h: Address 08d–09d, 08h–09h)

Bit	Name	R/W	Description	Default
15:9	RESERVED	RO	–	0
8:0	PAUSE_STATE[8:0]	RC	**PAUSE State.** The 9-bit field indicating the PAUSE state for each 10/100BASE-T port and the MII port (bits 0–7 = 10/100BASE-T ports, bit 8 = MII port). 0 = Not pause enabled. 1 = Pause enabled. ***Note:*** The PAUSE state for the MII port can only be reported for an external transceiver by using the CPU to read the negotiated PAUSE state via the MDC/MDIO interface and write this back to the MII Port Status Override register (Page 0h, Address 14h).	0

Source Address Change

Table 40: Source Address Change Register (Page 01h: Address 12d–13d, 0Ch–0Dh)

Bit	Name	R/W	Description	Default
15:9	RESERVED	RO	–	0
8:0	SRC_ADDR_CHANGE[8:0]	RC	**Source Address Change.** 9bit field indicating that the value loaded into the Last Source Address register was not the same 48-bit value as the previous value. A 1 value indicates a dedicated link segment, a value greater than 1 generally indicates a mixing (repeater) segment. Upon change of SA, a bit remains set until cleared by a read operation. 0 = Source address constant 1 = Source address changed	0

Last Source Address Port N

Table 41: Last Source Address Port Registers (Page 01h)

Addr	Bits	Register Name
10h–15h	48	Last Source Address Port 0
16h–1Bh	48	Last Source Address Port 1
1Ch–21h	48	Last Source Address Port 2
22h–27h	48	Last Source Address Port 3
28h–2Dh	48	Last Source Address Port 4
2Eh–33h	48	Last Source Address Port 5
34h–39h	48	Last Source Address Port 6
3Ah–3Fh	48	Last Source Address Port 7
40h–45h	48	Last Source Address MII Port

Table 42: Last Source Address Port n (Page 01h: Address 16d–69d, 10h–45h)

Bit	Name	R/W	Description	Default
47:0	LSA_PORT_n	RO	Last Source Address Port n, where: n = 0–7 for 10/100BASE-T ports n = 8 for MII port	00 00 00 00 00 00

Note: The LSA_PORT_n is stored in canonical format, not wire format (it is bit-reversed within each byte).

Example: Wire address 10-00-80-0F-00-E0 would be stored as 08-00-01-F0-00-07.

BIST Status

Table 43: BIST Status Register (Page 01h: Address 70d, 46h)

BIt	*Name*	*R/W*	*Description*	*Default*
7:5	RESERVED	RO	–	0
4	VLAN_RAM_ERR	RC	**VLAN Table RAM Error.** Set to indicate the VLAN RAM failed the internal self-test during initialization/power-up.	0
3	VID_RAM_ERR	RC	**VID RAM Error.** Set to indicate the VID RAM failed the internal self-test during initialization/ power-up.	0
2	MIB_RAM_ERR	RC	**MIB RAM Error.** Set to indicate the MIB RAM failed the internal self-test during initialization/ power-up.	0
1	MEM_ERR	RC	**Internal packet buffer memory Error.** Set to indicate the packet buffer memory failed the internal self-test during initialization/power-up.	0
0	BUFF_CON_ERR	RC	**Buffer Control RAM Error.** Set to indicate the Buffer Control RAM failed the internal self-test during initialization/power-up.	0

Management Mode Registers

Table 44: Management Mode Registers (Page 02h)

Addr	*Bits*	*Register Name*
00h	8	Global Management Configuration
01h	8	Reserved
02h	8	Management Port ID
03h	Reserved	
04h–05h	16	RMON MIB Steering register
06h–09h	32	Aging Time Control
0Ah–0Fh	8	Reserved
10h–11h	16	Mirror Capture Control
12h–13h	16	Ingress Mirror Control
14h–15h	16	Ingress Mirror Divider
16h–1Bh	48	Ingress Mirror MAC Address
1Ch–1Dh	16	Egress Mirror Control
1Eh–1Fh	16	Egress Mirror Divider
20h–25h	48	Egress Mirror MAC Address
26h–2Ch	Reserved	

Table 44: Management Mode Registers (Page 02h) (Cont.)

Addr	Bits	Register Name
2Dh–FEh	Reserved	
30h	8	Chip Revision lD register
FFh	8	Page register

Global Management Configuration Register

Table 45: Global Management Configuration Register (Page 02h: Address 00d, 00h)

Bit	Name	R/W	Description	Default
7:6	FRM_MNGT_PORT	R/W	**Frame Management Port.** Defines the physical port used to report management frames directed to the switch. 00 = No management port. 01 = SMP. 10 = MII port (in-band management port [IMP]). 11 = Reserved. These bits are ignored when SW_FWD_MODE = Unmanaged in the Switch Mode register, and the device behaves as if there is no defined management port.	00
5	MIB_AC_EN	R/W	**MIB Autocast Enable.** Controls automatic generation of management (MIB) information 0 = Disable MIB autocast. 1 = Enable MIB autocast.	0
4	MIB_AC_HDR_CNTRL	R/W	**MIB Autocast Header Control.** Enables additional header information to be prepended to the MIB statistics contained in the MIB Autocast frame. The MIB autocast header pointer is used as the pointer to the area of memory where the header information is stored. ***Note:*** The length of the additional header is defined in the MIB Autocast Header Length register. 0 = No additional bytes prepended to MIB autocast frame 1 = MIB autocast header pointer used to locate start of header information	0
3	Enable IGMP snooping	R/W	When asserted, IGMP snooping is enabled. When the incoming frame has a multicast DA address, value 2 in the IP header's protocol field (and not IGMP query) is forwarded to the CPU port.	0
2	Reserved	R/W	–	0

Table 45: Global Management Configuration Register (Page 02h: Address 00d, 00h) (Cont.)

Bit	Name	R/W	Description	Default
1	RX_BPDU_EN	R/W	Receive BPDU Enable. Enables all ports to receive BPDUs and forward to the defined physical management port. Management CPU must set this bit to globally allow BPDUs to be received.	0
0	RST_MIB_CNTRS	R/W	Reset MIB Counters. Resets all MIB counters for all ports to zero (pages 20h–28h). The host must set the bit and then clear the bit in successive write cycles to activate the reset operation.	0

Management Port ID

Table 46: Management Port ID Register (Page 02h: Address 02d, 02h)

Bit	Name	R/W	Description	Default
7:4	RESERVED	RO	–	0
5:4	CHIP ID	R/W	Chip ID where management port is located.	0
3:0	PORT ID	R/W	Port ID where management port is located. This must be programmed consistent with the frame management port in the Global Management Configuration register. Only IMP (Port 8, 1000b) or SMP (Port 10, 1010b) are legal values.	0

RMON MIB Steering Register

Table 47: RMON MIB Steering Register (Page 02h: Address 04d–05d, 04h–05h)

Bit	Name	R/W	Description	Default
15:9	RESERVED	RO	–	0
8:0	OR_RMON_RCV[8:0]	R/W	**Override RMON Receive.** Forces the RMON packet size bucket counters from the normal default of snooping on the receive side of the MAC, to the transmit side. This allows the RMON bucket counters to snoop either transmit or receive, allowing full duplex MAC support. 0–7 = 10/100BASE-T ports. 8 = MII port.	0

Aging Time Control

Table 48: Aging Time Control Register (Page 02h: Address 06d–09d, 06h–09h)

Bit	Name	R/W	Description	Default
31:20	RESERVED	RO	–	0

Table 48: Aging Time Control Register (Page 02h: Address 06d–09d, 06h–09h) (Cont.)

Bit	Name	R/W	Description	Default
19:0	AGE_TIME	R/W	Specifies the aging time in seconds for dynamically learned address. Maximum age time is 1,048,575s. ***Note:*** While 802.1D specifies a range of values of 10–1,000,000 s, this register does not enforce this range. Setting the AGE_TIME to zero disables the aging process. The aging process requires two scans of the entire ARL table. An entry with no activity during that time is aged out between 300 ~ 600 s with the default AGE_TIME.	300 (decimal)

Mirror Capture Control

Table 49: Mirror Capture Control Register (Page 02h: Address 16d–17d, 10h–11h)

Bit	Name	R/W	Description	Default
15	MIRROR_ENABLE	R/W	Global enable/disable for all mirroring on this chip. When reset, mirroring is disabled. When set, mirroring is enabled according to the ingress and egress control rules to the port designated by the MIRROR_CAPTURE_PORT.	0
14	BLK_NOT_MIR	R/W	When enabled, all traffic to MIRROR_CAPTURE_PORT is blocked except mirror traffic.	0
13:11	RESERVED	RO	–	0
10:0	MIRROR_CAPTURE_PORT	R/W	**Mirror Capture Port.** Bit mask which identifies the single unique port which is designated as the port to which all ingress and/or egress traffic is mirrored on this chip/system. Bits 0–7 = 10/100BASE-T ports. Bit 8 = MII/IMP. Bit 9 = Expansion port. Bit 10 = SMP. ***Note:*** Implementations with multiple BCM5338M devices connected via their expansion ports, only one BCM5338M device in the entire system can have the MIRROR_CAPTURE_PORT set for the physical port where mirrored traffic is destined. Other BCM5338M devices that are not connected to the physical mirror port must define their MIRROR_CAPTURE_PORT to be the expansion port. Unpredictable behavior results if more than 1 bit is set in the MIRROR_CAPTURE_PORT or mirrored traffic is not forwarded via the expansion port to the single BCM5338M connected to the single physical mirror port. See “Port Mirroring” on page 68.	0

Ingress Mirror Control

Table 50: Ingress Mirror Control Register (Page 02h: Address 16d–19d, 12h–13h)

Bit	Name	R/W	Description	Default
15:14	IN_MIRROR_FILTER	R/W	**Ingress Mirror Filter.** Defines the conditions under which frames received on a port that have been selected in the IN_MRROR_MASK[10:0] are compared to determine if they should be forwarded to the MIRROR_CAPTURE_PORT. 00 = Mirror all ingress frames. 01 = Mirror all received frames with DA = IN_MIRROR_MAC. 10 = Mirror all received frames with SA = IN_MIRROR_MAC. 11 = Reserved.	0
13	IN_DIV_EN	R/W	**Ingress Divider Enable.** Mirror every n^{th} received frame (n=IN_MIRROR_DIV) that has passed through the IN_MIRROR_FILTER.	0
12:11	RESERVED	RO	–	0
10:0	IN_MIRROR_MASK[10:0]	R/W	**Ingress Mirror Port Mask.** 11 bit mask, which selectively allows any port with its corresponding bit set, to be mirrored to the port identified by the MIRROR_CAPTURE_PORT value. ***Note:*** While multiple bits in a device may be set, severe congestion and/or frame loss may occur if excessive bandwidth from the mirrored port(s) is directed to the MIRROR_CAPTURE_PORT. Bits 0–7 = 10/100BASE-T Ports Bit 8 = MII Bit 9 = Reserved Bit 10 = SPI	0

Ingress Mirror Divider

Table 51: Ingress Mirror Divider Register (Page 02h: Address 20d–21d, 14h–15h)

Bit	Name	R/W	Description	Default
15:10	RESERVED	RO	–	0
9:0	IN_MIRROR_DIV	R/W	**Ingress Mirror Divider.** Receive frames that have passed the IN_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the IN_DIV_EN bit in the Ingress Mirror Control register is set, frames that pass the IN_MIRROR_FILTER rule are further divided by the value loaded into this register, so that only one in n frames (where n = IN_MIRROR_DIV) are mirrored.	0

Ingress Mirror MAC Address

Table 52: Ingress Mirror MAC Address Register (Page 02h: Address 22d–27d, 16h–1Bh)

Bit	Name	R/W	Description	Default
47:0	IN_MIRROR_MAC	R/W	**Ingress Mirror MAC Address.** MAC address that is compared against ingress frames in accordance with the IN_MIRROR_FILTER rules. When IGMP_EN is set and IN_MIRROR_MAC is programmed to 01 00 5E 00 00 00 then BCM5338M compares the first 25 bits of DA MAC from frames received at ingress port with the Ingress Mirror MAC register bits [47:24] and [16] to determine if they should be forwarded to management port.	0

Note: The IN_MIRROR_MAC Address is stored in canonical format.

Egress Mirror Control

Table 53: Egress Mirror Control Register (Page 02h: Address 28d–29d, 1Ch–1Dh)

Bit	Name	R/W	Description	Default
15:14	OUT_MIRROR_FILTER	R/W	**Egress Mirror Filter.** Defines the conditions under which frames transmitted on a port that have been selected in the OUT_MRROR_MASK[10:0] are compared to determine if they should be forwarded to the MIRROR_CAPTURE_PORT. 00 = Mirror all egress frames 01 = Mirror all transmitted frames with DA = IN_MIROR_MAC 10 = Mirror all transmitted frames with SA = IN_MIRROR_MAC 11 = Reserved	0
13	OUT_DIV_EN	R/W	**Egress Divider Enable.** Mirror every nth transmitted frame (n=OUT_MIRROR_DIV) that has passed through the OUT_MIRROR_FILTER.	0
12:11	RESERVED	RO	–	0

Table 53: Egress Mirror Control Register (Page 02h: Address 28d–29d, 1Ch–1Dh) (Cont.)

Bit	Name	R/W	Description	Default
10:0	OUT_MIRROR_MASK[10:0]	R/W	**Egress Mirror Port Mask.** 11 bit mask which selectively allows any port with its corresponding bit set, to be mirrored to the port identified by the MIRROR_CAPTURE_PORT value. ***Note:*** While multiple bits in a device may be set, severe congestion and/or frame loss may occur if excessive bandwidth from the mirrored port(s) is directed to the MIRROR_CAPTURE_PORT. Bits 0–7 = 10/100BASE-T Ports Bit 8= MII Bit 9 = Reserved Bit 10 = SPI	0

Egress Mirror Divider

Table 54: Egress Mirror Divider Register (Page 02h: Address 30d–31d, 1Eh–1Fh)

Bit	Name	R/W	Description	Default
15:10	RESERVED	RO	–	0
9:0	OUT_MIRROR_DIV	R/W	**Egress Mirror Divider.** Transmit frames that have passed the OUT_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the OUT_DIV_EN bit in the Egress Mirror Control register is set, frames that pass the OUT_MIRROR_FILTER rule are further divided by the value loaded into this register, so that only one in n frames (where n = OUT_MIRROR_DIV) are mirrored.	0

Egress Mirror MAC Address

Table 55: Egress Mirror MAC Address Register (Page 02h: Address 32d–37d, 20h–25h)

Bit	Name	R/W	Description	Default
47:0	OUT_MIRROR_MAC	R/W	**Egress Mirror MAC Address.** MAC address that is compared against egress frames in accordance with the OUT_MIRROR_FILTER rules.	0

Note: The OUT_MIRROR_MAC Address is stored in canonical format.

Chip Revision ID Register

Table 56: Chip Revision ID Register (Page 02h: Address 48d, 30h)

Bit	Name	R/W	Description	Default
7:0	CHIP_REV_ID	RO	Chip Revision ID	38/37

MIB Autocast Registers

Table 57: MIB Autocast Register (Page 03h)

Addr	Bits	Register Name
00h–01h	16	MIB Autocast Port
02h–03hh	16	MIB Autocast Header Pointer
04h–05hh	16	MIB Autocast Header Length
06h–0Bh	48	MIB Autocast DA
0Ch–11h	48	MIB Autocast SA
12h–13h	16	MIB Autocast Type
14h	8	MIB Autocast Rate
15h–FEh	Reserved	
FFh	8	Page register

MIB Autocast Port

Table 58: MIB Autocast Port Register (Page 03h: Address 00dQ–01d, 00h–01h)

Bit	Name	R/W	Description	Default
15:11	Reserved	RO	–	0
10:0	MIB_AC_PORTS	R/W	Bit map of ports able to transmit MIB Autocast frames. Any port with 1 has MIB autocast frames queued at the appropriate interval. Bits 0–7 = 10/100BASE-T ports Bit 8 = MII Bit 9 = Expansion port Bit 10 = SMP	3FFh

MIB Autocast Header Pointer

Table 59: MIB Autocast Header Pointer Register (Page 03h: Address 02d–03d, 02h–03h)

Bit	Name	R/W	Description	Default
15	MIB_AC_HDR_VALID	R/W	**MIB Autocast Header Valid.** Indicates that the MIB_AC_HDR_PTR field is valid. Set by the BCM5338M in response to the host setting the MIB Autocast Header Control bit in the Global Management Control register. When set, indicates to the host that a buffer has been allocated, and that the MIB_AC_HDR_PTR[9:0] field contains the address of the buffer.	0
14:10	RESERVED	RO	–	0
9:0	MIB_AC_HDR_PTR[9:0]	R/W	**MIB Autocast Header Pointer.** When MIB_AC_HDR_VALID is set, contains the most significant 10-bits of the address of the first byte of header to be prepended to MIB Autocast frames.The MIB Autocast header must be written to this memory location, which is an internal buffer. Prepended bytes are inserted between the contents of the MIB Autocast Type register and the assembled MIB statistics.	0

MIB Autocast Header Length Register

Table 60: MIB Autocast Header Length Register (Page 03h: Address 04d–05d, 04h–05h)

Bit	Name	R/W	Description	Default
15:8	RESERVED	RO	–	0
7:0	MIB_AC_HDR_LEN[7:0]	R/W	Defines length of additional header (in bytes) to be prepended to MIB Autocast frame, starting at location defined by the MIB Autocast Header Pointer register.	0

MIB Autocast DA

Table 61: MIB Autocast Header Pointer Register (Page 03h: Address 06d–11d, 06h–0Bh)

Bit	Name	R/W	Description	Default
47:0	MIB_AC_DA	R/W	Contains the MAC address inserted into the DA field of all MIB Autocast frames generated by this device.	01-10-18-00-00-00h

Note: The MIB_AC_DA is stored in canonical format.

MIB Autocast SA

Table 62: MIB Autocast Header Pointer Register (Page 03h: Address 12d–17d, 0Ch–11h)

Bit	Name	R/W	Description	Default
47:0	MIB_AC_SA	R/W	Contains the MAC address inserted into the SA field of all MIB Autocast frames generated by this device. Also used to compare incoming frames to determine if this frame is a configuration message directed at this device.	01-10-18-00-00-00h

Note: The MIB_AC_SA is stored in canonical format.

MIB Autocast Type

Table 63: MIB Autocast Type Register (Page 03h: Address 18d–19d, 12h–13h)

Bit	Name	R/W	Description	Default
15:0	MIB_AC_TYPE	R/W	Contains EtherType field used in transmission of MIB Autocast frames, and used to compare for configuration messages directed to this device. Defaults to Broadcom EtherType value 8874, a reserved code.	8874h

MIB Autocast Rate

Table 64: MIB Autocast Rate Register (Page 03h: Address 20dQ–21d, 14h–15h)

Bit	Name	R/W	Description	Default
7:0	MIB_AC_RATE	R/W	Sets the rate for generation of MIB Autocast frames. Based on a 0.1s clock rate, maximum interval is 25.6s.	40h

ARL Control Registers

Table 65: ARL Control Registers (Page 04h)

Addr	Bits	Register Name
00h	8	Global ARL Configuration
01h–03h	Reserved	
04h–09h	64	BPDU Multicast Address register
0Ah–0Fh	Reserved	
10h–15h	48	Multiport Address 1
16h–17h	16	Multiport Vector 1
18h–1Fh	Reserved	
20h–25h	48	Multiport Address 2
26h–27h	16	Multiport Vector 2
28h–2Fh	Reserved	
30h–31h	16	Secure Source Port Mask
32h–33h	16	Secure Destination Port Mask
34h–FEh	Reserved	
FFh	8	Page register

Global ARL Configuration Register

Table 66: Global ARL Configuration Register (Page 04h: Address 00d, 00h)

Bit	Name	R/W	Description	Default
7:5	RESERVED	RO	–	0
4	MPORT_ADDR_EN	R/W	**Multiport Address Enable.** When set by the host, enables the Multiport Address 1 and 2 registers, and their associated Multiport Vector 1 and 2 registers. This enables these registers in the ARL search. ***Note:*** If only one multiport address is required, the host should write both Multiport Address/Vector entries to the same value.	0
3:1	RESERVED	RO	–	0
0	RESERVED	RO	Must be set to 0.	0

BPDU Multicast Address Register

Table 67: BPDU Multicast Address Register (Page 04h: Address 04d–09d, 04h–09h)

Bit	Name	R/W	Description	Default
47:0	BPDU_MC_ADDR	R/\W	**BPDU Multicast Address.** Defaults to the 802.1 defined reserved multicast address for the Bridge Group Address. Programming to an alternate value allows support of proprietary protocols in place of the normal Spanning Tree Protocol. Frames with a matching DA to this address are forwarded only to the designated management port (IMP or SMP).	01-80-C2-00-00-00h

Note: The BPDU_MC_ ADDR is stored in canonical format.

Multiport Address 1 Register

Table 68: Multiport Address 1 Register (Page 04h: Address 16d–21d, 10h–15h)

Bit	Name	R/W	Description	Default
47:0	MPORT_ADDR_1	R/W	**Multiport Address 1.** Allows a frames with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 1 register. Must be enabled using the MPORT_ADDR_EN bit in the Global ARL Configuration register.	00-00-00-00-00-00h

Note: The MPORT_ADDR_1 is stored in canonical format.

Multiport Vector 1 Register

Table 69: Multiport Vector 1 Register (Page 04h: Address 22d–23d, 16h–17h)

Bit	Name	R/W	Description	Default
15:11	RESERVED	RO	–	0
10:0	MPORT_VCTR_1 [10:0]	R/W	**Multiport Vector 1.** A bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the Multiport Address 1 register is forwarded to each port with a bit set in the Multiport Vector 1 bit map. Bits 0–7 = 10/100BASE-T ports Bit 8 = MII Ports Bit 9 = Expansion port Bit 10 = SMP	0

Multiport Address 2 Register

Table 70: Multiport Address 2 Register (Page 04h: Address 32d–37d, 20h–25h)

Bit	Name	R/W	Description	Default
47:0	MPORT_ADDR_2	R/W	**Multiport Address 2.** Allows a frames with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 2 register. Must be enabled using the MPORT_ADDR_EN bit in the Global ARL Configuration register.	00-00-00-00-00-00h

Note: The MPORT_ ADDR_2 is stored in canonical format.

Multiport Vector 2 Register

Table 71: Multiport Vector 2 Register (Page 04h: Address 38d–39d, 26h–27h)

Bit	Name	R/W	Description	Default
15:11	RESERVED	RO	–	0

Table 71: Multiport Vector 2 Register (Page 04h: Address 38d–39d, 26h–27h) (Cont.)

Bit	Name	R/W	Description	Default
10:0	MPORT_VCTR_2 [10:0]	R/W	**Multiport Vector 2.** A bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the Multiport Address 2 register is forwarded to each port with a bit set in the Multiport Vector 2 bit map. Bits 0–7 = 10/100BASE-T ports Bit 8 = MII port Bit 9 = Expansion port Bit 10 = SMP	0

Secure Source Port Mask Register

Table 72: Secure Source Port Mask Register (Page 04h: Addresses 48d–49d, 30h–31h)

Bit	Name	R/W	Description	Default
15:11	RESERVED	RO	–	0
10:0	SECSRC_PORTMASK	R/W	**Secure Source Port Mask.** A bit mask corresponding to the physical ports on the chip. A frame with a destination address that corresponds to a port with a bit set in the Secure Source Port Mask register mask drops if the frame's source port does not have its corresponding bit set in the Secure Destination Port Mask. Bits 0–7 = 10/100BASE-T physical port numbers 1 to 8 Bit 8 = MII port Bit 9 = Reserved Bit 10 = SMP port	0

Example: Usage of Secure Source and Destination Port Mask registers:

- A five-port switch case: P4, P3, P2, P1, P0
- Set SECSRC_PORTMASK = [11000]
- Set SECDEST_PORTMASK = [10101]

If a broadcast packet comes in from:

- P0, the destination port map is [11110]. Since some bits are set in SECSRC_PORTMASK, the ARL logic checks to see if bit 0 in SECDEST_PORTMASK is set or not. The answer is YES, so the ARL does not change the destination port map.
- P1, the destination port map is [11101]. Since some bits are set in SECSRC_PORTMASK, the ARL logic checks to see if bit 1 in SECDEST_PORTMASK is set or not. The answer is NO, so the ARL logic changes the destination port map as[11101] and ~[11000] = [00101]. The result is that this broadcast packet only floods to ports P2 and P0.

Secure Destination Port Mask Register

Table 73: Secure Destination Port Mask Register (Page 04h: Addresses 50d–51d, 32h–33h)

BIt	Name	R/W	Description	Default
15:11	RESERVED	RO	–	0
10:0	SECDEST_PORTMASK	R/W	**Secure Destination Port Mask.** A bit mask corresponding to the physical ports on the chip. A frame with a destination address that corresponds to a port with a bit *not* set in this mask drops if the frame's source port does not have its corresponding bit set in the Secure Destination Port Mask. Bits 0–7 = 10/100BASE-T physical port numbers 1 to 8 Bit 8 = MII port Bit 9 = Reserved Bit 10 = SMP port	0

ARL Access Registers

Table 74: ARL Access Registers (Page 05h)

Addr	Bits	Register Name
00h	8	ARL Read/Write Control
01h–0Fh	Reserved	
02h–07h	48	MAC Address Index
08h–09h	16	VID Table Index register
0Ah–0Fh	Reserved	
10h–17h	64	ARL Entry 0
18h–1Fh	64	ARL Entry 1
20h	8	ARL Search Control
21h	Reserved	
22h–23h	16	ARL Search Address
24h–2Bh	64	ARL Search Result
2Ch–2Dh	16	RL Search Result VID register
2Eh–2Fh	Reserved	
30h–31h	16	VID Entry 0 register
32h–33h	16	VID Entry 1 register
34h–FEh	Reserved	
FFh	8	Page register

ARL Read/Write Control Register

Table 75: ARL Read/Write Control Register (Page 05h: Address 0d, 0h)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	**Start/Done Command.** Write as 1 to initiate a read or write command, after first loading the MAC_ADDR_INDX register with the MAC address for which the ARL entry is to be read or written. The BCM5338M resets the bit to indicate a write operation completed, or a read operation has completed and data from the bin entry is available in ARL Entry 0/1. ***Note:*** Both ARL Entry 0 and 1 are both always read/written by the BCM5338M when accessing the address table locations in memory.	0
6:1	RESERVED	RO	–	0
0	ARL_R/W	R/W	**ARL Read/Write.** 1 = Read 0 = Write	0

MAC Address Index Register

Table 76: MAC Address Index Register (Page 05h: Address 02d–07d, 02h–07h)

Bit	Name	R/W	Description	Default
47:0	MAC_ADDR_INDX	R/W	**MAC Address Index.** The MAC address for which status is to be read or written. By writing the 48 bit SA or DA address, and initiating a read command, the complete ARL bin location (2 entries deep) is returned in the ARL Entry 0/1 locations. Both entries are 64 bits wide. Initiating a write command writes the contents of ARL Entry 0/1 to the specified bin location (2 entries deep) and overwrites the current contents of the bin, regardless of the status of the Valid bit(s) in each entry.	00-00-00-00-00-00h

Note: The MAC_ADDR_INDX is stored in canonical format.

VID Table Index Register

Table 77: VID Table Index Register (Page 05h: Address 08d–09d, 08h–09h)

Bit	Name	R/W	Description	Default
11:0	VID_TBL_INDX	R/W	**VID Table Index.** When VID_MAC is Hash Enable asserted (Page 34h, Addr 0h), VID_TBL_INDX and MAC_ADDR_INDX are used for the hashing ARL table entry when the CPU uses ARL Read/ Write Control (Page 05h, Addr 0h) to access ARL table.	0

ARL Entry 0 Register

ARL Entry 0 Register (if Not Multicast Address)

Table 78: ARL Entry 0 Register (Page 05h: Address 16d–23d, 10h–17h)

Bit	Name	R/W	Description	Default
63	VALID0	R/W	**Valid.** Set to indicate that a valid MAC address is stored in the MACADDR0 field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning takes place if an address location is not valid and has not been marked as static.	0
62	STATIC0	R/W	**Static.** Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry does not take place. When cleared, the internal learning and aging process controls the validity of the entry.	0
61	AGE0	R/W	**Age.** Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for the period set by the AGE_TIME, and the entry has not been marked as Static, the entry has the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.	0
60:59	PRIORITY	R/W	Priority bits.	0
58	RESERVED	RO	–	0
57	Disable_Learning_PKT	R/W	Set to indicate that the device should not send out an ARL packet across the expansion bus. Must be set if STATIC0 bit is set.	0
56:54	RESERVED	RO	–	

Table 78: ARL Entry 0 Register (Page 05h: Address 16d–23d, 10h–17h) (Cont.)

Bit	Name	R/W	Description	Default
53:52	CHIPID0	R/W	**Chip Identification.** The chip number which identifies where the station with unique MACADDR0 is connected.	0
51:48	PORTID0	R/W	**Port Identification.** The port number which identifies where the station with unique MACADDR0 is connected.	0
47:0	MACADDR0	R/W	MAC address.	0

Note: The MACADDR0 is stored in canonical format.

Note: In Version A2 silicon, bits 56:54 can be programmed with any proprietary bits the customer wishes to store with the Unicast MAC Address.

ARL Entry 0 Register (if Multicast Address)

Table 79: ARL Entry 0 Register (Page 05h: Address 16d–23d, 10h–17h)

Bit	Name	R/W	Description	Default
63	VALID0	R/W	**Valid.** Set to indicate that a valid MAC address is stored in the MACADDR0 field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process or the external management processor has invalidated the entry. Automatic learning takes place if an address location is not valid and has not been marked as static.	0
62	STATIC0	R/W	**Static.** Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry does not take place. When cleared, the internal learning and aging process controls the validity of the entry.	0
61	CPU0	R/W	Set to indicate that the multicast map includes the CPU port.	0
60:59	PRIORITY	R/W	Priority bits.	0
58	RESERVED	RO	–	0
57:48	Multicast_map0	R/W	Set to indicate if Expansion bus, MII, P7, P6, P5, P4, P3, P2, P1, and P0 are included in the multicast map.	0
47:0	MACADDR0	R/W	MAC address.	0

Note: The MACADDR0 is stored in canonical format.

ARL Entry 1 Register

ARL Entry 1 Register (if Not Multicast Address)

Table 80: ARL Entry 1 Register (Page 05h: Address 24d–31d, 18h–1Fh)

Bit	Name	R/W	Description	Default
63	VALID1	R/W	**Valid.** Set to indicate that a valid MAC address is stored in the MACADDR1 field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning takes place if an address location is not valid and has not been marked as static.	0
62	STATIC1	R/W	**Static.** Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry does not take place. When cleared, the internal learning and aging process controls the validity of the entry.	0
61	AGE1	R/W	**Age.** Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for the period set by the AGE_TIME, and the entry has not been marked as Static, the entry has the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.	0
60:59	PRIORITY	R/W	Priority bits.	0
58	RESERVED	RO	–	0
57	Disable_Learning_PKT	R/W	Set to indicate that the device should not send out an ARL packet across the expansion bus. Must be set if STATIC1 bit is set.	0
56:54	RESERVED	RO	–	
53:52	CHIPID1	R/W	**Chip Identification.** The chip number which identifies where the station with unique MACADDR1 is connected.	0
51:48	PORTID1	R/W	**Port Identification.** The port number which identifies where the station with unique MACADDR1 is connected.	0
47:0	MACADDR1	R/W	MAC address.	0

Note: The MACADDR1 is stored in canonical format.

Note: In Version A2 silicon, bits 56:54 can be programmed with any proprietary bits the customer wishes to store with the Unicast MAC Address.

ARL Entry 1 Register (if Multicast Address)

Table 81: ARL Entry 1 Register (Page 05h: Address 24d–31d, 18h–1Fh)

BIt	*Name*	*R/W*	*Description*	*Default*
63	VALID1	R/W	**Valid.** Set to indicate that a valid MAC address is stored in the MACADDR1 field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process or the external management processor has invalidated the entry. Automatic learning takes place if an address location is not valid and has not been marked as static.	0
62	STATIC1	R/W	**Static.** Set to indicate that the entry is controlled by the external management processor and automatic learning and aging of the entry does not take place. When cleared, the internal learning and aging process controls the validity of the entry.	0
61	CPU1	R/W	Set to indicate that the multicast map includes the CPU port.	0
60:59	PRIORITY	R/W	Priority bits.	0
58	RESERVED	RO	–	0
57:48	Multicast_map1	R/W	Set to indicate if Expansion bus, MII, P7, P6, P5, P4, P3, P2, P1, and P0 are included in the multicast map.	0
47:0	MACADDR1	R/W	MAC address.	0

Note: The MACADDR1 is stored in canonical format.

ARL Search Control Register

Table 82: ARL Search Control Register (Page 05h: Address 32d, 20h)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	**Start/Done.** Write as 1 to initiate a sequential search of the ARL entries, returning each entry that is currently occupied (Valid = 1 and AGE = 0) in the ARL Search Result register. Reading the ARL Search Result register causes the ARL search to continue. The BCM5338M clears this bit to indicate that the entire ARL entry database has been searched.	0
6:1	RESERVED	RO	–	0
0	ARL_SR_VALID	RO	**ARL Search Result Valid.** Set by the BCM5338M to indicate that an ARL entry is available in the ARL Search Result register. Reset by a host read to the ARL Search Result register, which causes the ARL search process to continue through the ARL entries until the next entry is found with a valid bit is set.	0

ARL Search Address Register

Table 83: ARL Search Address Register (Page 05h: Address 34d–35d, 22h–23h)

Bit	Name	R/W	Description	Default
15	ARL_ADDR_VALID	R/W (SC)	**ARL Address Valid.** Indicates the lower 15 bits of this register contain a valid internal representation of the ARL entry currently being accessed. Intended for factory test/diagnostic use only.	0
14:0	ARL_ADDR		**ARL Address.** 14 bit internal representation of the address of the ARL entry currently being accessed by the ARL search routine. This is not a direct address of the ARL location and is intended for factory test/diagnostic use only.	0

ARL Search Result Register

Table 84: ARL Search Result Register (Page 05h: Address 16d–23d, 24h–2Bh)

Bit	Name	R/W	Description	Default
63	VALID	RO	**Valid.** Indicates a valid MAC address is stored in the MACADDR field, and that the entry has not aged out or been freed by the management processor. All entries returned by the ARL search process has the VALID bit set.	0
62	STATIC	RO	**Static.** Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry does not take place. All entries with the STATIC bit set are returned by the ARL search process. When cleared, the internal learning and aging process controls the validity of this entry.	0
61	AGE	RO	**Age.** Set to indicate that this address entry has been learned or accessed. Reset by the internal aging algorithm. The ARL search process returns an entry if it is Valid and/or Static, the AGE bit is irrelevant.	0
60:59	PRIORITY	R/W	**Priority.** Set to 1 for an address entry that is always to be routed to the high-priority queue. ***Note:*** This bit can only be set by the user, typically for a static entry.	0
58:54	RESERVED	RO	–	0
53:52	CHIPID	RO	**Chip Identification.** The chip number which identifies where the station with unique MACADDR is connected.	0
51:48	PORTID	RO	**Port Identification.** The port number which identifies where the station with unique MACADDR is connected.	0
47:0	MACADDR	RO	**MAC Address.** The unique MAC address of the station occupying this ARL entry.	0

Note: The MACADDR Search Result is stored in canonical format.

ARL Search Result VID Register

Table 85: ARL Search Result VID Register (Page 05h: Address 42d–43d, 2Ch–2Dh)

Bit	Name	R/W	Description	Default
11:0	VID	RO	VID area for search result.	

Note: If 1Q is enabled, it is recommended to read the VID register first, then read the MAC register later.

VID Entry 0 Register

Table 86: VID Entry 0 Register (Page 05h: Address 48d–49d, 30h–31h)

Bit	Name	R/W	Description	Default
11:0	ARL_VID_Entry_0	R/W	When VID_MAC Hash Enable asserted (Page 34h, Addr 0h) and the CPU uses ARL Read/Write Control (Page 05h, Addr 0h) to access the ARL table, ARL_VID_Entry_0 is written to bin 0 of ARL table entry.	

VID Entry 1 Register

Table 87: VID Entry 1 Register (Page 05h: Address 50d–51d, 32h–33h)

Bit	Name	R/W	Description	Default
11:0	ARL_VID_Entry_1	R/W	When VID_MAC Hash Enable asserted (Page 34h, Addr 0h) and the CPU uses ARL Read/Write Control (Page 05h, Addr 0h) to access the ARL table, ARL_VID_Entry_1 is written to bin 1 of ARL table entry.	

Management Frame Access Registers

These registers are for the CPU to send/receive frames via the SMP port.

Table 88: Management Frame Access Registers (Page 06h)

Addr	*Bits*	*Register Name*
00h	8	Management Frame Read Data
01h	8	Management Frame Write Data
02h-03h	16	Management Frame Write Control
04h-05h	16	Management Frame Read Status
06h-FEh	Reserved	
FFh	8	Page register

Management Frame Read Data Register

Table 89: Management Frame Read Data Register (Page 06h: Address 00d, 00h)

Bit	*Name*	*R/W*	*Description*	*Default*
7:0	RD_FRM_DATA[7:0]	RO	Read Frame Data.	0

Management Frame Write Data Register

Table 90: Management Frame Write Data Register (Page 06h: Address 01d, 01h)

Bit	*Name*	*R/W*	*Description*	*Default*
7:0	WR_FRM_DATA[7:0]	WO	Write Frame Data	0

Management Frame Write Control Register

Table 91: Management Frame Write Control Register (Page 06h: Address 02–03d, 02–03h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:3	RESERVED	WO	–	0
2	TX_RDY	R/W	**Transmit Ready.** Indicates that the data is valid in the SMP Write Frame Data register.	1
1	EOF	WO	**End of Frame.** Written by the management host to indicate that the completed header and frame information for a transmit frame has been written to the SMP Write Frame Data register.	0

Table 91: Management Frame Write Control Register (Page 06h: Address 02–03d, 02–03h)

Bit	Name	R/W	Description	Default
0	SOF	WO	**Start of Frame.** Written by the management host to indicate that the next write access to the SMP Write Frame Data register is the header field for a new frame. The header field is always prepended to the data field for the frame.	0

Management Frame Read Status Register

Table 92: Management Frame Read Status Register (Page 06h: Address 04d–05d, 04h–05h)

Bit	Name	R/W	Description	Default
15:5	SMP_FRM_BCNT	RO	**Frame Byte Count.** An 11 bit field indicating frame length, including header field.	0
4:3	RESERVED	RO	–	0
2	RX_RDY	RO	**Receive Ready.** Indicates the Read Frame Data register is valid.	
1	FIP	RO	**Frame In Progress.** If NF is set, FIP is set after the first access to the SMP Read Frame Data register, to indicate that more receive frame data remains in the SMP Receive Frame Queue. Always zero when the New Frame bit is set. Cleared when all data for the current frame has been read.	0
0	NF	RO	**New Frame.** Set when a new frame is at the head of the SMP Receive Frame Queue, and can be read by accessing the SMP Read Frame Data register. Cleared on the first access of the SMP Read Frame Data register. Always zero when the Frame In Progress bit is set. If another packet is in the SMP Receive Frame Queue, NF is set immediately following the last read operation for the preceding frame from the SMP Read Frame Data register. Otherwise, NR is set the next time a frame is placed on the SMP Receive Frame Queue.	0

Generic Memory Access Registers

Table 93: Generic Memory Access Registers (Page 08h)

Address	Bits	Register Name
00h-03h	32	Memory Read/Write Control
04h-0Fh	64	Memory Read/Write Data register
10h	8	Memory Read/Write VID_Data register
11h-FEh	Reserved	
FFh	8	Page register

Memory Read/Write Control Register

Table 94: Memory Read/Write Control Register (Page 08h: Address 00–03d, 00–03h)

Bit	Name	R/W	Description	Default
19	START/DONE	R/W	**Start/Done Command.** Write as 1 to initiate a read or write memory location after first loading the MEM_ADDR with the address which is to be read or written. The BCM5338M resets the bit to indicate a write operation completed, or a read operation has completed and data from the memory location is available in Memory Entry register. ***Note:*** The entire 64-bit memory entry is always read/written by the BCM5338M when accessing the RAM.	0
18	MEM_R/W	R/W	**Memory Read/Write.** 1 = Read 0 = Write	0
17:15	RESERVED	RO	–	0
14:0	MEM_ADDR	R/W	The 15-bit memory address that points to a unique 64-bit memory entry in the internal RAM. The address location has its contents read into the Memory Entry register, or the contents of the Memory Entry register are written to the internal RAM location specified. ***Note:*** The addressing format is incremented by one for every 64-bit entry.	

Memory Read/Write Data Register

Table 95: Memory Read/Write Data Register (Page 08h: Address 04d–011d, 04–0Bh)

Bit	Name	R/W	Description	Default
63:0	RAM_DATA[63:0]	R/W	64-bits of data to be written to memory, or data that has been read from memory, as configured in the Memory Read/Write Control register, prior to setting the Start bit.	0

Note: The Memory Read/Write Data is stored in wire format.

Memory Read/Write VID_Data Register

Table 96: Memory Read/Write VID_Data Register (Page 08h: Address 16d, 10h)

Bit	Name	R/W	Description	Default
10:0	VIDRAM_DATA[10:0]	R/W	11 bits of data to be written to VID memory, or data that has been read from VID memory, as configured in the Memory Read/Write Control register prior to setting the Start bit.	0

Priority Queue Control Registers

Table 97: Priority Queue Control Registers (Page 0Ah)

Addr	Bits	Description
00h–2Fh	Reserved	
30h–31h	16	Global Flow Control register
32h–35h	Reserved	
36h	8	B0 silicon new control bits
37h–63h	Reserved	
64h–65h	16	Queue 0 TxDsc Control 3 register
66h–71h	Reserved	
72h–73h	16	Queue 1 TxDsc Control 3 register
74h–7Fh	Reserved	
80h–81h	16	Queue 2 TxDsc Control 3 register
82h–8Dh	Reserved	
8Eh–8Fh	16	Queue 3 TxDsc Control 3 register
90h–FEh	Reserved	

Table 97: Priority Queue Control Registers (Page 0Ah) (Cont.)

Addr	Bits	Description
FFh	8	Page register

Global Flow Control Register

Table 98: Global Flow Control Register (Page 0Ah: Address 30–31h)

Bit	Name	R/W	Description	Default
15:10	Reserved	–	–	–
9	Mode_HQ_preempt	R/W	When enabled, the highest queue is transmitted first if any packets are in the highest queue. The remaining queues are served by WRR.	0
8:0	Reserved	–	–	15 (if QoS is disabled) 1D (if QoS is enabled)

B0 Silicon New Feature Control Bits Register

Table 99: B0 Silicon New Feature Control Bits Register (Page 0Ah: Address 36h–37h)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	Write as 0, ignore when read.	0h
9	Reserved	RO	Write as 1, ignore on read.	1
8	Enhance_4	R/W	When set, allow learning SA if both 802.1Q and MSTP are enabled and the port is configured in the 10 Mbps mode.	0
7	Reserved	RO	Write as 0, ignore on read.	0
6	Enhance_3	R/W	When set, block dropping known IPMC frames if storm suppression and IGMP snooping are enabled.	0
5	Enhance_2	R/W	When set, do not drop the first broadcast packet that follows an untagged reserved multicast frame or an ingress_VID violation frame.	0
4	Enhance_1	R/W	When set, enhance throughput over the expansion port.	0
3	PASS_BPDU	R/W	When set, and when spanning tree is in blocking state, pass BPDU and reserved mcast DA frames.	1’b0
2	Reserved	RO	Write as 0, ignore when read.	1’b0
1	DROP_VIOLATIONS	R/W	When set, and when ingress_VID_check is set to 2’b01, an incoming frame with bcast DA and VID violation will be dropped.	1’b0
0	DROP_MCAST_SA	R/W	When set, a frame with mcast/bcast SA will be dropped.	1’b0

Queue 0 TxDsc Control 3 Register

Note: Broadcom recommends the user not change this register unless guided by Broadcom.

Table 100: Queue 0 TxDsc Control 3 Register (Page 0Ah: Address 64–65h)

Bit	Name	R/W	Description	Default
15:8	Reserved	R/W	–	1Q = 7Dh 2Q = 5Eh 3Q = 3Fh 4Q = 20h
7:5	Reserved	RO	–	0h
4:0	Q0_quota_size	R/W	The round robin weight for priority queue 0. ***Note:*** The user must make sure bits 15:8 are not mistakenly changed when changing Q0_quota_size.	1Q = 01h 2Q = 01h 3Q = 01h 4Q = 01h

Queue 1 TxDsc Control 3 Register

Note: Broadcom recommends the user not change this register unless guided by Broadcom.

Table 101: Queue 1 TxDsc Control 3 Register (Page 0Ah: Address 72–73h)

Bit	Name	R/W	Description	Default
15:8	Reserved	R/W	–	1Q = 0h 2Q = 20h 3Q = 20h 4Q = 20h
7:5	Reserved	RO	–	0h
4:0	Q1_quota_size	R/W	The round robin weight for priority queue 1. ***Note:*** The user must make sure bits 15:8 are not mistakenly changed when changing Q1_quota_size.	1Q = 00h 2Q = 02h 3Q = 02h 4Q = 02h

Queue 2 TxDsc Control 3 Register

Note: Broadcom recommends the user not change this register unless guided by Broadcom.

Table 102: Queue 2 TxDsc Control 3 Register (Page 0Ah: Address 80–81h)

Bit	Name	R/W	Description	Default
15:8	Reserved	R/W	–	1Q = 0h 2Q = 0h 3Q = 20h 4Q = 20h
7:5	Reserved	RO	–	0h
4:0	Q2_quota_size	R/W	The round robin weight for priority queue 2. ***Note:*** The user must make sure bits 15:8 are not mistakenly changed when changing Q2_quota_size.	1Q = 00h 2Q = 00h 3Q = 04h 4Q = 04h

Queue 3 TxDsc Control 3 Register

Note: Broadcom recommends the user not change this register unless guided by Broadcom.

Table 103: Queue 3 TxDsc Control 3 Register (Page 0Ah: Address 8E–8Fh)

Bit	Name	R/W	Description	Default
15:8	Reserved	R/W	–	1Q = 0h 2Q = 0h 3Q = 0h 4Q = 20h
7:5	Reserved	RO	–	0h
4:0	Q3_quota_size	R/W	The round robin weight for priority queue 3. The user must make sure bits 15:8 are not mistakenly changed when changing Q3_quota_size.	1Q = 00h 2Q = 00h 3Q = 00h 4Q = 08h

Port MII Registers

Note: Page 18h is external PHY dependent. For details in registers, check data sheet of external PHY connected.

Table 104: Port MII Registers (Pages 10h–18h)

Addr	*Bits*	*Description*
00h–01h	16	MII control
02h–03h	16	MII status
04h–05h	16	PHY identification high
06h–07h	16	PHY identification low
08h–09h	16	Auto-negotiation advertisement
0Ah–0Bh	16	Auto-negotiation link partner ability
0Ch–0Dh	16	Auto-negotiation expansion
0E–0F	16	Auto-negotiation next page
10h–11h	16	Link partner next page
12h–1Fh	Reserved	
20h–21h	16	100BASE-X auxiliary control
22h–23h	16	100BASE-X auxiliary Status
24h–25h	16	100BASE-X receive error counter
26h–27h	16	100BASE-X false carrier sense counter
28h–2Fh	Reserved	
30h–31h	16	Auxiliary control/status
32h–33h	16	Auxiliary status summary
34h–35h	16	Connection status
36h–37h	16	Auxiliary mode 2
38h–39h	16	Auxiliary error and general status
3Ah–3Bh	Reserved	
3Ch–3Dh	16	Auxiliary Multiple PHY register
3Eh–3Fh	16	Broadcom Test register
40h–FEh	Reserved	
FFh	8	Page register

Table 105: MII Register Map Summary

Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	INIT
00h–01h	Control	Soft Reset	Lpbk	Force 100	AutoNeg Enable	Power Down	Isolate	Restart AutoNeg	Full-duplex	Collision Test	Reserved							3000h
02h–03h	Status	T4 Capable	TX FDX Capable	TX Capable	10BT FDX Capable	10BT Capable	Reserved				Preambl Suppress	AutoNeg Cmpt	Remote Fault	AutoNeg Capable	Link Status	Jabber Detect	Extd Reg Capable	7809h
04h–05h	Phyid High	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0040h
06h–07h	Phyid Low	0	1	1	0	0	0	Model # 1	1	1	0	0	0	Revision # N				63XNh
08h–09h	Autoneg Advertise	Next Page 0	Reserved	Remote Fault	Reserved Technologies		Pause	Adv T4	Adv TX FDX	Adv TX	Adv BT FDX	Adv BT	Advertised Selector Field [4:0] 0	0	0	0	1	05E1h
0Ah–0Bh	Link Partner Ability	LP Next Page	LP Ack	LP Rmt Fault	Reserved Technologies		LP Pause	LP T4	LP TX FDX	LP TX	LP BT FDX	LP BT	Link Partner Selector Field [4:0]					0000h
0Ch–0Dh	Autoneg Expansion	Reserved											ParDet Fault	LP Next Pg Able	Next Pg Able	Page Rcvd	LP Auto Neg Able	0000h
0Eh–0Fh	Next Page	Next Page	Reserved	Message page	Acknowledge2	Toggle	Message/Unformatted Code Field											2001h
10h–11h	LP Next Page	Next Page	Reserved	Message page	Acknowledge2	Toggle	Message/Unformatted Code Field											0000h
20h–21h	100BASE-X Aux Control	Reserved		Transmit Disable	Reserved		Bypass 4B5B Enc/ Dec	Bypass Scr/ Descr	Bypass NRZI Enc/ Dec	Bypass Rcv Sym Align	Bypass BLW Correct	FEF Enable	Reserved					0000h
22h–23h	100BASE-X Aux Status	Reserved					FX Mode	Locked	Current 100 Link Status	Current Remote Fault	Rsvd	False Carrier Det	Bad ESD Det	Rcv Error Det	Xmt Error Det	Lock Error Det	MLT3 Error Det	
24h–25h	100BASE-X RCV Error Counter									Receive Error Counter								0000h

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Table 105: MII Register Map Summary (Cont.)

Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	INIT
26h–27h	100BASE-X False Carrier Counter	Reserved								False Carrier Sense Counter								0000h
28h–29h	100BASE-X Disconnect Counter	Reserved								Disconnect Counter								0000h
30h–31h	Auxiliary Control/ Status	Jabber Disable	Force Link	Reserved						HSQ	LSQ	Edge Rate [1:0]		AutoNeg Enable Indicator	Force 100 Indicator	SP100 Indicator	FDX Indicator	003xh
32h–33h	Auxiliary Status Summary	AutoNeg Cmpt	AutoNeg Cmpt Ack	AutoNeg Ack Det	AutoNeg Ability Det	AutoNeg Pause	AutoNeg HCD			AutoNeg ParDet Fault	LP Remote Fault	LP Page Rcvd	LP AutoNeg Able	SP100 Indicator	Link Status	Internal AutoNeg Enabled	Jabber Detect	0000h
34h–35h	Connection Status	Reserved												FDX Change	SPD Change	Link Change	RESV	0F00xh
36h–37h	Auxiliary Mode 2	Reserved																
38h–39h	10BASE-T AUX. ERROR & GENERAL STATUS	Reserved					Mnchstr Code Error	EOF Error (10M)	Polarity Error (10M)	0	0	1	Reserved	AutoNeg Enable Indicator	Force 100 Indicator	SP100 Indicator	FDX Indicator	002xh
3Ah–3Bh	Reserved	Reserved																0000h
3Ch–3Dh	AUXILIARY MULTI-PHY	HCD TX FDX	HCD T4	HCD TX	HCD 10BT FDX	HCD 10BT	Reserved		Restart AutoNeg	AutoNeg Cmpt	Cmpt Ack	ACK Detect	Ability Detect	Super Isolate	Rsvd	Reserved	Rsvd	0000h
3Eh–3Fh	BROADCOM Test	Reserved																

MII Control Register

Table 106: MII Control Register (Pages 10h–18h Address 00d–01d, 00h–01h)

Bit	Name	R/W	Description	Default
15	Reset	R/W (SC)	1 = PHY reset 0 = Normal operation	0
14	Loopback	R/W	1 = Loopback mode 0 = Normal operation	0
13	Forced Speed Selection	R/W	1 = 100 Mbps 0 = 10 Mbps	1
12	Auto-negotiation Enable	R/W	1 = Auto-negotiation enable 0 = Auto-negotiation disable	1
11	Power-Down	RO	0 = Normal operation	0
10	Isolate	R/W	1 = Electrically isolate PHY from MII 0 = Normal operation	0
9	Restart Auto-Negotiation	R/W (SC)	1 = Restart auto-negotiation process 0 = Normal operation	0
8	Duplex Mode	R/W	1 = Full-duplex 0 = Half duplex	0
7:0	Reserved	RO	Ignore when read	0

Note: R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.

Reset

To reset an individual part PHY, the BCM5338M by software control, 1 must be written to bit 15 of the Control register using an MII write operation. The bit clears itself after the reset process is complete and need not be cleared using a second MII write. Writes to other Control register bits have no effect until the reset process is completed, which requires approximately 1 µs. Writing 0 to this bit has no effect. Because this bit is self-clearing, after a few cycles from a write operation, it returns 0 when read.

Loopback

An individual part of the BCM5338M can be placed into loopback mode by writing 1 to bit 14 of the Control register. The loopback mode can be cleared by writing 0 to bit 14 of the control register, or by resetting the chip. When this bit is read, it returns 1 when the chip is in software-controlled loopback modes; otherwise, it returns 0.

Forced Speed Selection

If auto-negotiation is enabled, this bit has no effect on the speed selection. However, if auto-negotiation is disabled by software control, the operating speed of the BCM5338M port can be forced by writing the appropriate value to bit 13 of the Control register. Writing 1 to this bit forces 100BASE-X operation, while writing 0 forces 10BASE-T operation. When this bit is read, it returns the value of the software-controlled forced speed selection only. To read the overall state of forced speed selection, including both hardware and software control, use bit 8 of the Auxiliary Control register.

Auto-Negotiation Enable

Auto-negotiation is enabled by default. If bit 12 of the Control register is written with a value of 0, auto-negotiation is disabled by software control. Writing 1 to the same bit of the Control register or resetting the chip re-enables auto-negotiation. When read, this bit returns the value most recently written to this location, or 1 if it has not been written since the last chip reset.

Power-Down

The BCM5338M does not implement a low-power mode.

Isolate

Each individual PHY can be isolated from its Media Independent Interface by writing 1 to bit 10 of the Control register. All MII outputs are tristated and all MII inputs are ignored. Because the MII management interface is still active, the isolate mode can be cleared by writing 0 to bit 10 of the control register or by resetting the chip. When this bit is read, it returns 1 when the chip is in isolate mode; otherwise, it returns 0.

Restart Auto-Negotiation

Bit 9 of the Control register is a self-clearing bit that allows the auto-negotiation process to be restarted, regardless of the current status of the auto-negotiation state machine. For this bit to have an effect, auto-negotiation must be enabled. Writing 1 to this bit restarts the auto-negotiation, while writing 0 to this bit has no effect. Because the bit is self-clearing after only a few cycles, it always returns 0 when read. The operation of this bit is identical to bit 9 of the Auxiliary Multiple PHY register.

Duplex Mode

By default, at reset this bit indicates BCM5338M half-duplex mode. If the auto-negotiation is enabled, this bit has no effect on the duplex selection. The chip can be forced into full-duplex mode by writing 1 to bit 8 of the Control register while auto-negotiation is disabled. Half-duplex mode can be resumed by writing 0 to bit 8 of the control register or by resetting the chip.

Reserved Bits

All reserved MII register bits must be written as 0 at all times. Ignore the BCM5338M output when these bits are read.

MII Status Register

Table 107: MII Status Register (Pages 10h–18h, Address 02d–03d, 02–03h)

Bit	Name	R/W	Description	Default
15	100BASE-T4 Capability	RO	0 = Not 100BASE-T4 capable.	0
14	100BASE-TX FDX Capability	RO	1 = 100BASE-TX full duplex capable.	1
13	100BASE-TX Capability	RO	1 = 100BASE-TX half duplex capable.	1
12	10BASE-T FDX Capability	RO	1 = 10BASE-T full duplex capable.	1
11	10BASE-T Capability	RO	1 = 10BASE-T half duplex capable.	1
10:7	Reserved	RO	Ignore when read.	0
6	MF Preamble Suppression	R/W	1 = Preamble may be suppressed. 0 = Preamble always required.	0
5	Auto-negotiation Complete	RO	1 = Auto-negotiation process completed. 0 = Auto-negotiation process not completed.	0
4	Remote Fault	RO LH	1 = Remote/far-end fault condition detected. 0 = No remote/far-end fault condition detected.	0
3	Auto-negotiation Capability	RO	1 = Auto-negotiation capable. 0 = Not auto-negotiation capable.	1
2	Link Status	RO LL	1 = Link is up (Link Pass state). 0 = Link is down (Link Fail state).	0
1	Jabber Detect	RO LH	1 = Jabber condition detected. 0 = No jabber condition detected.	0
0	Extended Capability	RO	1 = Extended register capable.	1

Note: R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.

100BASE-T4 Capability

The BCM5338M is not capable of 100BASE-T4 operation and returns 0 when bit 15 of the status register is read.

100BASE-X Full-Duplex Capability

The BCM5338M is capable of 100BASE-X full-duplex operation and returns 1 when bit 14 of the Status register is read.

100BASE-X Half-Duplex Capability

The BCM5338M is capable of 100BASE-X half-duplex operation and returns 1 when bit 13 of the Status register is read.

10BASE-T Full-Duplex Capability

The BCM5338M is capable of 10BASE-T full-duplex operation and returns 1 when bit 12 of the Status register is read.

10BASE-T Half-Duplex Capability

The BCM5338M is capable of 10BASE-T half-duplex operation and returns 1 when bit 11 of the Status register is read.

Reserved Bit

Ignore the BCM5338M output when these bits are read.

MF Preamble Suppression

This bit is the only writable bit in the Status register. Setting this bit to 1 allows subsequent MII management frames to be accepted with or without the standard preamble pattern. When Preamble Suppression is enabled, only two preamble bits are required between successive Management Commands, instead of the normal 32.

Auto-Negotiation Complete

Bit 5 of the Status register returns 1 if the auto-negotiation process has been completed and the contents of registers 4, 5, and 6 are valid.

Remote Fault

When set at the completion of auto-negotiation, it indicates that a remote fault condition has been signaled by the link partner. When set in 100BASE-FX mode, it indicates that a far-end fault condition has been detected. This bit is latched high, and self-clears when read. Is immediately set once again in FX mode after clearing if the far-end fault condition remains true.

Auto-Negotiation Capability

The BCM5338M can perform IEEE auto-negotiation and returns 1 when bit 4 of the Status register is read, regardless of whether the auto-negotiation function has been disabled.

Link Status

The BCM5338M returns 1 on bit 2 of the Status register when the link state machine is in Link Pass, indicating that a valid link has been established. Otherwise, it returns 0. When a link failure occurs after the Link Pass state has been entered, the Link Status bit is latched at 0 and remains so until the bit is read. After the bit is read, it becomes 1 if the Link Pass state has been entered again.

Jabber Detect

10BASE-T operation only. The BCM5338M returns 1 on bit 1 of the Status register if a jabber condition has been detected. After the bit is read, or if the chip is reset, it reverts to 0.

Extended Capability

The BCM5338M supports extended capability registers and returns 1 when bit 0 of the Status register is read. Several extended registers have been implemented in the BCM5338M, and their bit functions are defined later in this section.

PHY Identifier Registers

Table 108: PHY Identifier Registers (Pages 10h–18h, Addresses 04h–05h and 06h–07h)

Bit	Name	R/W	Description	Default
15:0	MII Address 00010	RO	PHYID HIGH	0040h
15:0	MII Address 00011	RO	PHYID LOW	62BNh

Broadcom Corporation has been issued an Organizationally Unique Identifier (OUI) by the IEEE. It is a 24-bit number, 00-10-18, expressed as hex values. That number, along with the Broadcom Model Number for the BCM5338M part, 2Bh, and Broadcom Revision number, Nh (N=0 for the revision A0 of the BCM5338M, N=1 for the revision A1 of the BCM5338M, N=2 for the revision A2 of the BCM5338M, and N=3 for the revision B0 of the BCM5338M), is placed into two MII registers. The translation from OUI, Model Number and Revision Number to PHY Identifier register occurs as follows:

- PHYID HIGH [15:0] = OUI[21:6]
- PHYID LOW [15:0] = OUI[5:0] + MODEL[5:0] + REV[3:0]

Note: The two most significant bits of the OUI are not represented (OUI[23:22]).

The previous table shows the result of concatenating these values in order to form the MII Identifier registers PHYID HIGH and PHYID LOW.

Auto-Negotiation Advertisement Register

Table 109: Auto-Negotiation Advertisement Register (Pages 10h–18h, Address 08d–09d, 08h–09h)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Next-page operation supported. 0 = Next-page operation disabled.	0
14	Reserved	RO	Ignore when read.	0
13	Remote Fault	R/W	1 = Transmit remote fault.	0
12:11	Reserved Technologies	RO	Ignore when read.	00
10	Advertise Pause Capability	R/W	1 = Pause Operation for full-duplex.	1
9	Advertise 100BASE-T4	R/W	0 = Do Not Advertise T4 Capability.	0
8	Advertise 100BASE-X FDX	R/W	1 = Advertise 100BASE-X full-duplex. 0 = Do not advertise 100BASE-X full-duplex.	1

Table 109: Auto-Negotiation Advertisement Register (Pages 10h–18h, Address 08d–09d, 08h–09h) (Cont.)

Bit	Name	R/W	Description	Default
7	Advertise 100BASE-X	R/W	1 = Advertise 100BASE-X.	1
6	Advertise 10BASE-T FDX	R/W	1 = Advertise 10BASE-T full-duplex. 0 = Do not advertise 10BASE-T full-duplex.	1
5	Advertise 10BASE-T	R/W	1 = Advertise 10BASE-T.	1
4:0	Advertise Selector Field	R/W	Fixed value = indicates 802.3.	00001

Next Page

The BCM5338M supports the Next Page function. To enable this operation, write 1 to this bit.

Remote Fault

Writing 1 to bit 13 of the Advertisement register sends a Remote Fault indicator to the Link Partner during auto-negotiation. Writing 0 to this bit or resetting the chip clears the Remote Fault transmission bit. This bit returns the value last written to it, or else 0 if no write has been completed since the last chip reset.

Reserved Bits

Ignore output when read.

Pause Operation for Full-Duplex Links

The use of this bit is independent of the negotiated data rate, medium, or link technology. The setting of this bit indicates the availability of additional DTE capability when full-duplex operation is in use. This bit is used by one MAC to communicate Pause Capability to its Link Partner and has no effect on PHY operation.

Advertisement Bits

Use bits 9:5 of the Advertisement register to customize the ability information transmitted to the Link Partner. The default value for each bit reflects the abilities of the BCM5338M. By writing 1 to any of the bits, the corresponding ability is transmitted to the Link Partner. Writing 0 to any bit causes the corresponding ability to be suppressed from transmission. Resetting the chip restores the default bit values. Reading the register returns the values last written to the corresponding bits, or else the default values if no write has been completed since the last chip reset.

Selector Field

Bits 4:0 of the Advertisement register contain the value 00001, indicating that the chip belongs to the 802.3 class of PHY transceivers.

Auto-Negotiation Link Partner Ability Register

Table 110: Auto-Negotiation Link Partner Ability Register (Pages 10h–18h, Address 10d–11d, 0Ah–0Bh)

Bit	Name	R/W	Description	Default
15	LP Next Page	RO	Link partner next page bit.	0
14	LP Acknowledge	RO	Link partner acknowledge bit.	0
13	LP Remote Fault	RO	Link partner remote fault indicator.	0
12:11	Reserved Technologies	RO	Ignore when read.	000
10	LP Advertise Pause	RO	Link partner has pause capability.	0
9	LP Advertise 100BASE-T4	RO	Link partner has 100BASE-T4 capability.	0
8	LP Advertise 100BASE-X FDX	RO	Link partner has 100BASE-X FDX capability.	0
7	LP Advertise 100BASE-X	RO	Link partner has 100BASE-X capability.	0
6	LP Advertise 10BASE-T FDX	RO	Link partner has 10BASE-T FDX capability.	0
5	LP Advertise 10BASE-T	RO	Link partner has 10BASE-T capability.	0
4:0	Link Partner Selector Field	RO	Link partner selector field.	00000

Note: The values contained in the auto-negotiation Link Partner (LP) Ability register are only guaranteed to be valid after auto-negotiation has successfully completed, as indicated by bit 5 of the MII Status register.

Next Page

Bit 15 of the Link Partner Ability register returns a value of 1 when the Link Partner implements the Next Page function and has Next Page information to transmit.

Acknowledge

Bit 14 of the Link Partner Ability register is used by auto-negotiation to indicate that a device has successfully received its Link Partner's Link Code Word.

Remote Fault

Bit 13 of the Link Partner Ability register returns a value of 1 when the Link Partner signals that a remote fault has occurred. The BCM5338M simply copies the value to this register and does not act upon it.

Reserved Bits

Ignore when read.

Pause

Indicates that the link partner pause bit is set.

Advertisement Bits

Bits 9:5 of the Link Partner Ability register reflect the abilities of the Link Partner. A 1 on any of these bits indicates that the Link Partner is capable of performing the corresponding mode of operation. Bits 9:5 are cleared any time auto-negotiation is restarted or the BCM5338M is reset.

Selector Field

Bits 4:0 of the Link Partner Ability register reflect the value of the Link Partner's selector field. These bits are cleared any time auto-negotiation is restarted or the chip is reset.

Auto-Negotiation Expansion Register

Table 111: Auto-Negotiation Expansion Register (Pages 10h–18h, Address 12d–13d, 0Ch–0Dh)

Bit	*Name*	*R/W*	*Description*	*Default*
15:5	Reserved	RO	Ignore when read.	0
4	Parallel Detection Fault	RO LH	1 = Parallel detection fault. 0 = No parallel detection fault.	0
3	Link Partner Next Page Able	RO	1 = Link partner has next-page capability. 0 = Link Partner does not have next-page capability.	0
2	Next Page Able	RO	1 = Next page is enabled. 0 = Next page capability.	1
1	Page Received	RO	1 = New page has been received. 0 = New page has not been received.	0
0	Link Partner Auto-negotiation Able	RO LH	1 = Link partner has auto-negotiation capability. 0 = Link partner does not have auto-negotiation capability.	0

Note: R/W = Read/Write, RO = Read only, SC = Self-Clear, LL = Latched Low, LH = Latched High, LL and LH clear after read operation.

Parallel Detection Fault

Bit 4 of the auto-negotiation Expansion register is a read-only bit that gets latched high when a parallel detection fault occurs in the auto-negotiation state machine. For further details, consult the IEEE standard. The bit is reset to 0 after the register is read, or when the chip is reset.

Link Partner Next Page Able

Bit 3 of the auto-negotiation Expansion register returns 1 when the Link Partner has Next Page capabilities. It has the same value as bit 15 of the Link Partner Ability register.

Page Received

Bit 1 of the auto-negotiation Expansion register is latched high when a new Link Code Word is received from the Link Partner, checked, and acknowledged. It remains high until the register is read, or until the chip is reset.

Link Partner Auto-Negotiation Able

Bit 0 of the auto-negotiation Expansion register returns 1 when the Link Partner is known to have auto-negotiation capability. Before any auto-negotiation information is exchanged, or if the Link Partner does not comply with IEEE auto-negotiation, the bit returns a value of 0.

Auto-Negotiation Next Page Register

Table 112: Next Page Transmit Register (Pages 10h–18h, Address 14d–15d, 0Eh–0Fh)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Additional next page(s) follows. 0 = Last page.	0
14	Reserved	R/W	Ignore when read.	0
13	Message Page	R/W	1= Message page. 0 = Unformatted page.	1
12	Acknowledge 2	R/W	1 = Complying with message. 0 = Cannot comply with message.	0
11	Toggle	RO	1 = Previous value of the transmitted link code word equalled logic zero. 0 = Previous value of the transmitted link code word equalled logic one.	0
10:0	Message/Unformatted Code Field	R/W	–	1

Next Page

Indicates whether this is the last Next Page to be transmitted.

Message Page

Differentiates a Message Page from an Unformatted Page.

Acknowledge 2

Indicates that a device has the ability to comply with the message.

Toggle

Used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange.

Message Code Field

An 11-bit-wide field, encoding 2048 possible messages.

Unformatted Code Field

An 11-bit-wide field, which may contain an arbitrary value.

Link Partner Next Page Register

Table 113: Link Partner Next Page Register (Pages 10h–18h, Address 16d–17d, 10h–11h)

Bit	Name	R/W	Description	Default
15	Next Page	RO	1 = Additional next page(s) follows. 0 = Last page.	0
14	Reserved	RO	Ignore when read.	0
13	Message Page	RO	1= Message page. 0 = Unformatted page.	0
12	Acknowledge 2	RO	1 = Complies with message. 0 = Cannot comply with message.	0
11	Toggle	RO	1 = Previous value of the transmitted link code word equalled logic zero. 0 = Previous value of the transmitted link code word equalled logic one.	0
10:0	Message/Unformatted Code Field	RO	–	0

Next Page

indicates whether this is the last Next Page.

Message Page

Differentiates a Message Page from an Unformatted Page.

Acknowledge 2

Indicates that Link Partner has the ability to comply with the message.

Toggle

Used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange.

Message Code Field

An 11-bit-wide field, encoding 2048 possible messages.

Unformatted Code Field

An 11-bit-wide field, which may contain an arbitrary value.

100BASE-X Auxiliary Control Register

Table 114: 100BASE-X Auxiliary Control Register (Pages 10h–18h, Address 32d–33d, 20h–21h)

Bit	Name	R/W	Description	Default
15:14	Reserved	RO	Write as 10b, Ignore when read.	10b
13	Transmit Disable	R/W	1 = Transmitter is disabled in PHY. 0 = Normal operation.	0
12:11	Reserved	RO	Ignore when read.	0
10	Reserved	R/W	Write as 0, ignore when read.	0
9	Bypass Scrambler/Descrambler	R/W	1 = Scrambler and descrambler are disabled. 0 = Scrambler and descrambler are enabled.	0
8	Bypass NRZI Encoder/Decoder	R/W	1 = NRZI encoder and decoder are disabled. 0 = NRZI encoder and decoder are enabled.	0
7	Reserved	RO	Ignore when read.	0
6	Baseline Wander Correction Disable	R/W	1 = BASEline wander correction is disabled. 0 = BASEline wander correction is enabled.	0
5	FEF Enable	R/W	1 = Far-end fault is enabled. 0 = Far-end fault is disabled.	0
4:0	Reserved	R/W	Write as 0, ignore when read.	0

Transmit Disable

The transmitter can be disabled by writing 1 to bit 13 of MII register 10h. In TX mode, the output is forced to the MLT-3 zero state. In FX mode, the output is forced to the –1, or off state.

Bypass Scrambler/Descrambler

The stream cipher function may be disabled by writing 1 to bit 9 of MII register 10h. The stream cipher function can be re-enabled by writing 0 to this bit.

Bypass MLT3 Encoder/Decoder

The MLT3 encoder and decoder can be bypassed by writing 1 to bit 8 of MII register 10h. NRZ data is transmitted and received on the cable. The MLT3 encoder can be re-enabled by writing 0 to this bit.

Baseline Wander Correction Disable

The baseline wander correction circuit can be disabled by writing 1 to bit 6 of MII register 10h. The BCM5338M is correct for baseline wander on the receive data signal when this bit is cleared.

Reserved Bits

The Reserved bits of the 100BASE-X Auxiliary Control register must be written as 0 at all times. Ignore the BCM5338M outputs when these bits are read.

100BASE-X Auxiliary Status Register

Table 115: 100BASE-X Auxiliary Status Register (Pages 10h–18h, Address 34d–35d, 22h–23h)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	Ignore when read.	0
9	Locked	RO	1 = Descrambler locked. 0 = Descrambler unlocked.	0
8	Current 100BASE-X Link Status	RO	1 = Link pass. 0 = Link fail.	0
7	Far-end Fault	RO	1 = Far-end fault detected. 0 = No far-end fault detected.	0
6	Reserved	RO	Ignore when read.	0
5	False Carrier Detected	RO LH	1 = False carrier detected since last read. 0 = No false carrier since last read.	0
4	Bad ESD Detected	RO LH	1 = ESD error detected since last read. 0 = No ESD error since last read.	0
3	Receive Error Detected	RO LH	1 = Receive error detected since last read. 0 = No receive error since last read.	0
2	Transmit Error Detected	RO LH	1 = Transmit error code received since last read. 0 = No transmit error code received since last read.	0
1	Lock Error Detected	RO LH	1 = Lock error detected since last read. 0 = No lock error since last read.	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 code error detected since last read. 0 = No MLT3 code error since last read.	0

Note: R/W = Read/Write, RO = Read Only, SC = Self-Clear, LL = Latched Low, LH = Latched High. LL and LH clear after read operation.

Locked

The PHY returns 1 in bit 9 when the descrambler is locked to the incoming data stream. Otherwise, it returns 0.

Current 100BASE-X Link Status

The PHY returns 1 in bit 8 when the 100BASE-X link status is good. Otherwise, it returns 0.

Far-End Fault

The PHY returns 1 while its link partner is signalling 100BASE-X far-end fault condition. Otherwise, it returns 0.

False Carrier Detected

The PHY returns 1 in bit 5 of the extended status register if a false carrier has been detected since the last time this register was read. Otherwise, it returns 0.

Bad ESD Detected

The PHY returns 1 in bit 4 if an end of stream delimiter error has been detected since the last time this register was read. Otherwise, it returns 0.

Receive Error Detected

The PHY returns 1 in bit 3 if a packet was received with an invalid code since the last time this register was read. Otherwise, it returns 0.

Transmit Error Detected

The PHY returns 1 in bit 2 if a packet was received with a transmit error code since the last time this register was read. Otherwise, it returns 0.

Lock Error Detected

The PHY returns 1 in bit 1 if the descrambler has lost lock since the last time this register was read. Otherwise, it returns 0.

MLT3 Code Error Detected

The PHY returns 1 in bit 0 if an MLT3 coding error has been detected in the receive data stream since the last time this register was read. Otherwise, it returns 0.

100BASE-X Receive Error Counter

Table 116: 100BASE-X Receive Error Counter (Pages 10h–18h, Address 36d–37d, 24h–25h)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Write as 0, Ignore when read.	0
7:0	Receive Error Counter	R/W	Number of non-collision packets with receive errors since last read.	0

This counter increments each time the BCM5338M receives a non-collision packet containing at least one receive error. The counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting receive errors until cleared.

100BASE-X False Carrier Sense Counter

Table 117: 100BASE-X False Carrier Sense Counter (Pages 10h–18h, Address 38d–39d, 26h–27h)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Write as 0, Ignore when read.	0
7:0	False Carrier Sense Counter	R/W	Number of false carrier sense events since last read.	0

This counter increments each time the BCM5338M detects a false carrier on the receive input. The counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting false carrier sense errors until cleared.

Auxiliary Control/Status Register

Table 118: Auxiliary Control/Status Register (Pages 10h–18h, Address 48d–49d, 30h–31h)

Bit	Name	R/W	Description	Default
15	Jabber Disable	R/W	1= Jabber function disabled in PHY. 0 = Jabber function enabled in PHY.	0
14	Link Disable	R/W	1= Link integrity test disabled in PHY. 0 = Link integrity test enabled in PHY.	0
13:8	Reserved	RO	Ignore when read.	000000
7:6	HSQ : LSQ	R/W	These two bits define the squelch mode of the 10BASE-T carrier sense mechanism: 00 = Normal squelch. 01 = Low squelch. 10 = High squelch. 11 = Not allowed.	00
5:2	Reserved	RO	Ignore when read.	1111b

Table 118: Auxiliary Control/Status Register (Pages 10h–18h, Address 48d–49d, 30h–31h) (Cont.)

Bit	Name	R/W	Description	Default
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	0
0	Full-Duplex Indication	RO	1 = Full-duplex active. 0 = Full-duplex not active.	0

Jabber Disable

10BASE-T operation only. Bit 15 of the Auxiliary Control register allows the user to disable the Jabber Detect function, defined in the IEEE standard. This function shuts off the transmitter when a transmission request has exceeded a maximum time limit. By writing 1 to bit 15 of the Auxiliary Control register, the Jabber Detect function is disabled. Writing 0 to this bit or resetting the chip restores normal operation. Reading this bit returns the value of Jabber Detect Disable.

Link Disable

Write 1 to bit 14 of the Auxiliary Control register to disable the Link Integrity state machines and place the port into forced Link Pass status. Writing 0 to this bit or resetting the chip restores the Link Integrity functions. Reading this bit returns the value of Link Integrity Disable.

Test Mode

Active-high test mode control bit. Must be written with 0 for normal operation.

HSQ and LSQ

Extend or decrease the squelch levels for detection of incoming 10BASE-T data packets. The default squelch levels implemented are those defined in the IEEE standard. The high- and low-squelch levels are useful for situations where the IEEE-prescribed levels are inadequate. The squelch levels are used by the CRS/LINK block to filter out noise and recognize only valid packet preambles and link integrity pulses. Extending the squelch levels allows the BCM5338M to operate properly over longer cable lengths. Decreasing the squelch levels may be useful in situations where there is a high level of noise present on the cables. Reading these two bits returns the value of the squelch levels.

Speed Indication

Bit 1 of the Auxiliary Control register is a read-only bit that shows the true current operation speed of this port of the BCM5338M. A 1 bit indicates 100BASE-X operation, while 0 indicates 10BASE-T.

Note: While the auto-negotiation exchange is performed, the BCM5338M is always operating at 10BASE-T speed.

Full-Duplex Indication

Bit 0 of the Auxiliary Control register is a read-only bit that returns 1 when the BCM5338M is in full duplex mode. In all other modes, it returns 0.

Auxiliary Status Summary Register

Table 119: Auxiliary Status Summary Register (Pages 10h–18h, Address 50d–51d, 32h–33h)

Bit	Name	R/W	Description	Default
15	Auto-Negotiation Complete	RO	1 = Auto-negotiation process completed.	0
14	Auto-Negotiation Complete Acknowledge	RO LH	1 = Auto-negotiation completed acknowledge state.	0
13	Auto-Negotiation Acknowledge Detected	RO LH	1 = Auto-negotiation acknowledge detected.	0
12	Auto-Negotiation Ability Detect	RO LH	1 = Auto-negotiation for link partner ability.	0
11	Auto-Negotiation Pause	RO	BCM5338M & link partner Pause Operation bit set.	0
10:8	Auto-Negotiation HCD	RO	000 = No highest common denominator. 001 = 10BASE-T. 010 = 10BASE-T Full-duplex. 011 = 100BASE-TX. 100 = 100BASE-T4. 101 = 100BASE-TX full-duplex. 11x = Undefined.	000
7	Auto-Negotiation Parallel Detection Fault	RO LH	1 = Parallel detection fault.	0
6	Link Partner Remote Fault	RO	1 = Link partner remote fault.	0
5	Link Partner Page Received	RO LH	1 = New page has been received.	0
4	Link Partner Auto-negotiation Able	RO	1 = Link Partner is auto-negotiation capable.	0
3	Speed Indicator	RO	1 = 100 Mbps. 0 = 10 Mbps.	0
2	Link Status	RO LL	1 = Link is up (link pass state).	0
1	Auto-Negotiation Enabled	RO	1 = Auto-negotiation enabled.	1
0	Jabber Detect	RO LH	1 = Jabber condition detected.	0

Note: R/W = Read/Write, RO = Read Only, SC = Self-Clear, LL = Latched Low, LH = Latched High. LL and LH clear after read operation.

The Auxiliary Status Summary register contains copies of redundant status bits found elsewhere within the MII register space. Descriptions for each of these individual bits can be found associated with their primary register descriptions.

Auxiliary Mode 2 Register

Table 120: Auxiliary Mode 2 (Pages 10h–18h, Address 54d–55d, 36h–37h)

Bit	Name	R/W	Description	Default
15:0	Reserved Bits	RO	These are Broadcom reserved bits. Do not write.	-

10BASE-T Auxiliary Error and General Status Register

Table 121: 10BASE-T Auxiliary Error & General Status Register (Pages 10h–18h, Address 56d–57d, 38h–39h)

Bit	Name	R/W	Description	Default
15:14	Reserved	RO	Ignore when read.	0
13	MDIX Status	RO	0 = MDI is in use. 1 = MDIX is in use.	0
12	MDIX Manual Swap	R/W	0 = MDI or MDIX if MDIX is not disabled. 1 = Force MDIX.	0
11	HP Auto-MDIX disable	R/W	0 = HP Auto-MDIX enabled. 1 = HP Auto-MDIX disabled.	MDIX_DIS strap pin
10	Manchester Code Error	RO	1 = Manchester code error (10BASE-T).	0
9	EOF Error	RO	1 = EOF detection error (10BASE-T).	0
8	Polarity Inversion	RO	1 = Channel polarity inverted. 0 = Channel polarity correct.	0
7:5	Revision	RO	Revision number.	xxx
4:2	Reserved	RO	Ignore when read.	011b
1	Speed Indication	RO	1 = 100BASE-X. 0 = 10BASE-T.	0
0	Full-duplex Indication	RO	1 = Full-duplex active. 0 = Full-duplex not active.	0

All error bits in the Auxiliary Error Status register are read-only and are latched high. When certain types of errors occur in the BCM5338M, 1 or more corresponding error bits become 1. They remain so until the register is read, or until a chip reset occurs. All such errors necessarily result in data errors and are indicated by a high value on the RXER output pin at the time the error occurs.

Manchester Code Error

Indicates that a Manchester code violation was received. This bit is only valid during 10BASE-T operation.

EOF Error

Indicates that the EOF (end of frame) sequence was improperly received or not received at all. This error bit is only valid during 10BASE-T operation.

Polarity

Reflects the Polarity status of the receive channel pair. The BCM5338M is capable of automatically inverting the polarity of the receive channel. No data errors are reported to indicate that the automatic polarity inversion is occurring. Instead, this bit returns 1 whenever the polarity of the receive channel is inverted.

Revision

Read-only bits that return the chip revision number. For the A1 revision, these bits read 001.

Speed Indication

A read-only bit that shows the true current operation speed of the BCM5338M. A 1 bit indicates 100BASE-X operation, while 0 indicates 10BASE-T.

Note: While the auto-negotiation exchange is performed, the BCM5338M is always operating at 10BASE-T speed.

Full-Duplex Indication

A read-only bit that returns 1 when the BCM5338M is in full-duplex mode. In all other modes, it returns 0.

Auxiliary Multiple PHY Register

Table 122: Auxiliary Multiple PHY Register (Pages 10h–18h, Address 60d–61d, 3Ch–3Dh)

Bit	*Name*	*R/W*	*Description*	*Default*
15	HCD_TX_FDX	RO	1 = Auto-negotiation result is 100BASE-TX full-duplex.	0
14	HCD_T4	RO	1 = Auto-negotiation result is 100BASE-T4.	0
13	HCD_TX	RO	1 = Auto-negotiation result is 100BASE-TX.	0
12	HCD_10BASE-T_FDX	RO	1 = Auto-negotiation result is 10BASE-T full-duplex.	0
11	HCD_10BASE-T	RO	1 = Auto-negotiation result is 10BASE-T.	0
10:9	Reserved	RO	Ignore when read.	0
8	Restart Auto-negotiation	R/W (SC)	1 = Restart auto-negotiation process. 0 = (No effect).	0
7	Auto-negotiation Complete	RO	1 = Auto-negotiation process complete. 0 = Auto-negotiation process not complete.	0

Table 122: Auxiliary Multiple PHY Register (Pages 10h–18h, Address 60d–61d, 3Ch–3Dh) (Cont.)

Bit	Name	R/W	Description	Default
6	Acknowledge Complete	RO	1 = Auto-negotiation acknowledge complete.	0
5	Acknowledge Detected	RO	1 = Auto-negotiation acknowledge detected.	0
4	Ability Detect	RO	1 = Auto-negotiation waiting for LP ability.	0
3	Super Isolate	R/W	1 = Super isolate mode. 0 = Normal operation.	0
3:0	Reserved	RO	Ignore when read.	0

HCD Bits

Bits 15:11 of the Auxiliary Multiple PHY register are 5 read-only bits that report the Highest Common Denominator (HCD) result of the auto-negotiation process. Immediately upon entering the Link Pass state after each reset or Restart auto-negotiation, only 1 of these 5 bits is 1. The Link Pass state is identified by 1 in bit 6 or 7 of this register. The HCD bits are reset to 0 every time auto-negotiation is restarted or the BCM5338M is reset.

Note: For their intended application, these bits uniquely identify the HCD only after the first Link Pass after reset or restart of auto-negotiation. On later Link Fault and subsequent renegotiations, if the ability of the Link Partner is different, more than 1 of the above bits may be active.

Restart Auto-Negotiation

A self-clearing bit that allows the auto-negotiation process to be restarted, regardless of the current status of the state machine. For this bit to work, auto-negotiation must be enabled. Writing 1 to this bit restarts auto-negotiation. Because the bit is self-clearing, it always returns 0 when read. The operation of this bit is identical to bit 9 of the Control register.

Auto-Negotiation Complete

This read-only bit returns 1 after the auto-negotiation process has been completed. It remains 1 until the auto-negotiation process is restarted, a Link Fault occurs, or the chip is reset. If auto-negotiation is disabled or the process is still in progress, the bit returns 0.

Acknowledge Complete

This read-only bit returns 1 after the Acknowledgment exchange portion of the auto-negotiation process has been completed and the Arbitrator state machine has exited the Complete Acknowledge state. It remains this value until the auto-negotiation process is restarted, a Link Fault occurs, auto-negotiation is disabled, or the BCM5338M is reset.

Acknowledge Detected

This read-only bit is set to 1 when the Arbitrator state machine exits the acknowledged-detect state. It remains high until the auto-negotiation process is restarted, or the BCM5338M is reset.

Ability Detect

This read-only bit returns 1 when the auto-negotiation state machine is in the Ability Detect state. It enters this state a specified time period after the auto-negotiation process begins and exits after the first FLP burst or link pulses are detected from the Link Partner. This bit returns 0 any time the auto-negotiation state machine is not in the ability-detect state.

Broadcom Test Register

Table 123: Broadcom Test (Pages 10h–18h, Address 62d–63d, 3E–3Fh)

Bit	Name	R/W	Description	Default
15:0	Reserved Bits	RO	The Broadcom test register bits are reserved and should never be written.	–

Port MIB Registers

Table 124: Port MIB Registers (Pages 20h–28h)

Address	Bits	Description
00h–07h	64	TxOctets
08h–0Bh	32	TxDropPkts
0Ch–0Fh	32	TxQoSPkts
10h–13h	32	TxBroadcastPkts
14h–17h	32	TxMulticastPkts
18h–1Bh	32	TxUnicastPkts
1Ch–1Fh	32	TxCollisions
20h–23h	32	TxSingleCollision
24h–27h	32	TxMultiple Collision
28h–2Bh	32	TxDeferredTransmit
2Ch–2Fh	32	TxLateCollision
30h–33h	32	TxExcessiveCollision
34h–37h	32	TxFrameInDisc?
38h–3Bh	32	TxPausePkts
3Ch–43h	64	TxQoSOctets
44h–4Bh	64	RxOctets

Table 124: Port MIB Registers (Pages 20h–28h) (Cont.)

Address	*Bits*	*Description*
4Ch–4Fh	32	RxUndersizePkts
50h–53h	32	RxPausePkts
54h–57h	32	Pkts64Octets
58h–5Bh	32	Pkts65to127Octets
5Ch–5Fh	32	Pkts128to255Octets
60h–63h	32	Pkts256to511Octets
64h–67h	32	Pkts512to1023Octets
68h–6Bh	32	Pkts1024to1522Octets
6Ch–6Fh	32	RxOversizePkts
70h–73h	32	RxJabbers
74h–77h	32	RxAlignmentErrors
78h–7Bh	32	RxFCSErrors
7Ch–83h	64	RxGoodOctets
84h–87h	32	RxDropPkts
88h–8Bh	32	RxUnicastPkts
8Ch–8Fh	32	RxMulticastPkts
90h–93h	32	RxBroadcastPkts
94h–97h	32	RxSAChanges
98h–9Bh	32	RxFragments
9Ch–9Fh	32	RxExcessSizeDisc
A0h–A3h	32	RXSymbolError
A4h-A7h	32	RxQoSPkts
A8h-AFh	64	RxQoSOctets
B0h–FEh	Reserved	
FFh	32	Page register

QoS Registers

Table 125: Page 30h QoS Registers

Address	Bits	Description
00h–01h	16	QoS Control register
02h	8	QoS Queue Monitor Control register
03h	Reserved	
04h-05h	16	QoS 802.1p Enable register
06h-07h	16	QoS TOS/DiffServ Enable register
08h-12h	Reserved	
13h-14h	16	QoS Pause Enable register
15h-16h	16	Priority Threshold register
17-18h	Reserved	
19h	8	TOS/DiffServ Control register
1Ah-1Bh	16	D-type TOS threshold
1Ch-1Dh	16	T-type TOS threshold
1Eh-1Fh	16	R-type TOS threshold
20h-21h	16	M-type TOS threshold
22h-2Fh	Reserved	
30h-37h	64	DiffServ DSCP Priority register 1
38h-3Fh	64	DiffServ DSCP Priority register 2
40h-FEh	8	Reserved
FFh	8	Page register

QoS Control Register

Table 126: QoS Control Register (Page 30h: Address 00d–01d, 00h–01h)

Bit	Name	R/W	Description	Default
15	CPU Control Enable	R/W	1 = Register values control the port-based priority settings. This includes: • QOS_EN strap is overridden by QOS_Enable setting (bit 10 of this register). • High-priority ports are selected by this register (bits 8-0), not by the default strap settings. • Flow control enable/disable is controlled on a per- port basis in the QoS Pause Enable register (offset 13h-14h). 0 = Strap options control the port-based priority settings	0

Table 126: QoS Control Register (Page 30h: Address 00d–01d, 00h–01h) (Cont.)

Bit	Name	R/W	Description	Default
14:12	Reserved	RO	–	0
11:10	QOS_Enable	R/W	Selects the number of priority queues: 11 = When CPU Control Enable (bit 15) is asserted, this bit enables four queues QoS functionality. 10 = When CPU Control Enable (bit 15) is asserted, this bit enables three queues QoS functionality. 01 = When CPU Control Enable (bit 15) is asserted, this bit enables two queues QoS functionality 0 0= When CPU Control Enable (bit 15) is asserted, 00 disables QoS functionality.	00
9:0	Priority Port Mask	RO	If any of these bits are set to 1, then the corresponding port becomes the highest priority port which is decided by the value of QOS_enable bits[11:10]. This bit overwrites other settings and forces this port to highest queue. Bits 0–7 = 10/100BASE-T ports Bit 8 = MII port Bit 9 = SPI port	0

QoS Queue Monitor Control Register

Table 127: QoS Queue Monitor Control Register (Page 30h: Address 02d, 02h)

Bit	Name	R/W	Description	Default
7:2	Reserved	RO	–	0
1:0	MIB priority queue select	R/W	To select which priority queue is monitored by MIB counters. 00 = Lowest queue. 01 = Second lowest queue. 10 = Second highest queue. 11 = Highest queue.	00

QoS 802.1P Enable Register

Table 128: QoS 802.1P Enable Register (Page 30h: Address 04d–05d, 04h–05h)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	Reserved	0
9:0	QOS_1P_EN	R/W	802.1p QoS enable bit for per port. Bits 0–7 = 10/100BASE-T ports Bit 8 = MII port Bit 9 = SPI port	3FF

QoS TOS/DiffServ Enable Register

Table 129: QoS TOS/DiffServ Enable Register (Page 30h: Address 06d–07d, 06h–07h)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	Reserved	0
9:0	QOS_TOS_DIFF_EN	R/W	TOS/DiffServ QoS enable bit for per port. Bits 0–7 = 10/100BASE-T ports Bit 8 = MII port Bit 9 = SPI port	000

QoS Pause Enable Register

Table 130: QoS Pause Enable Register (Page 30h: Address 19d–20d, 13h–14h)

Bit	Name	R/W	Description	Default
8	MII Port	R/W	When software control of QoS is enabled by asserting the QOS_EN bit (bit 10) of the QoS Control register: 0 = Half-duplex back pressure and full-duplex flow control are disabled. Only dropping of frames is supported on the given port. 1 = Individual port supports half-duplex back pressure and full-duplex flow control when QOS_EN bit of the QoS Control register is enabled.	0
7	Port 7 QoS Pause Enable	R/W	–	0
6	Port 6 QoS Pause Enable	R/W	_	0
5	Port 5 QoS Pause Enable	R/W	_	0
4	Port 4 QoS Pause Enable	R/W	_	0
3	Port 3 QoS Pause Enable	R/W	_	0
2	Port 2 QoS Pause Enable	R/W	_	0

Table 130: QoS Pause Enable Register (Page 30h: Address 19d–20d, 13h–14h) (Cont.)

Bit	Name	R/W	Description	Default
1	Port 1 QoS Pause Enable	R/W	_	0
0	Port 0 QoS Pause Enable	R/W	_	0

Note: Broadcom recommends that flow control be disabled when QoS functionality is enabled.

Priority Threshold Register

Table 131: Priority Threshold Register (Page 30h: Address 21d–22d, 15h–16h)

Bit	Name	R/W	Tag Priority Queue Assignment	Default
15:14	802.1p Priority Tag 111	R/W	111	11
13:12	802.1p Priority Tag 110	R/W	110	11
11:10	802.1p Priority Tag 101	R/W	101	10
9:8	802.1p Priority Tag 100	R/W	100	10
7:6	802.1p Priority Tag 011	R/W	011	01
5:4	802.1p Priority Tag 010	R/W	010	01
3:2	802.1p Priority Tag 001	R/W	001	00
1:0	802.1p Priority Tag 000	R/W	000	00

TOS/DiffServ Control Register

Table 132: TOS/DiffServ Control Register (Page 30h: Address 25d, 19h)

Bit	Name	R/W	Description	Default
7:1	RESERVED	RO	–	0
0	TOS/DiffServ Select	R/W	1 = TOS 0 = DiffServ/traffic class	0

D-Type TOS Priority Register

Table 133: D-Type TOS Priority Register (Page 30h: Address 26d–27d, 1Ah–1Bh)

Bit	Name	R/W	Description	Default
15:14	D-Type TOS precedence 111	R/W	To assign priority queue of precedence 111	0
13:12	D-Type TOS precedence 110	R/W	To assign priority queue of precedence 110	0
11:10	D-Type TOS precedence 101	R/W	To assign priority queue of precedence 101	0
9:8	D-Type TOS precedence 100	R/W	To assign priority queue of precedence 100	0
7:6	D-Type TOS precedence 011	R/W	To assign priority queue of precedence 011	0
5:4	D-Type TOS precedence 010	R/W	To assign priority queue of precedence 010	0

Table 133: D-Type TOS Priority Register (Page 30h: Address 26d–27d, 1Ah–1Bh) (Cont.)

Bit	Name	R/W	Description	Default
3:2	D-Type TOS precedence 001	R/W	To assign priority queue of precedence 001	0
1:0	D-Type TOS precedence 000	R/W	To assign priority queue of precedence 000	0

T-Type TOS Priority Register

Table 134: T-Type TOS Priority Register (Page 30h: Address 28d–29d, 1Ch–1Dh)

Bit	Name	R/W	Description	Default
15:14	T-Type TOS precedence 111	R/W	To assign priority queue of precedence 111	0
13:12	T-Type TOS precedence 110	R/W	To assign priority queue of precedence 110	0
11:10	T-Type TOS precedence 101	R/W	To assign priority queue of precedence 101	0
9:8	T-Type TOS precedence 100	R/W	To assign priority queue of precedence 100	0
7:6	T-Type TOS precedence 011	R/W	To assign priority queue of precedence 011	0
5:4	T-Type TOS precedence 010	R/W	To assign priority queue of precedence 010	0
3:2	T-Type TOS precedence 001	R/W	To assign priority queue of precedence 001	0
1:0	T-Type TOS precedence 000	R/W	To assign priority queue of precedence 000	0

R-Type TOS Priority Register

Table 135: R-Type TOS Priority Register (Page 30h: Address 30d–31d, 1Eh–1Fh)

Bit	Name	R/W	Description	Default
15:14	R-Type TOS precedence 111	R/W	To assign priority queue of precedence 111	0
13:12	R-Type TOS precedence 110	R/W	To assign priority queue of precedence 110	0
11:10	R-Type TOS precedence 101	R/W	To assign priority queue of precedence 101	0
9:8	R-Type TOS precedence 100	R/W	To assign priority queue of precedence 100	0
7:6	R-Type TOS precedence 011	R/W	To assign priority queue of precedence 011	0
5:4	R-Type TOS precedence 010	R/W	To assign priority queue of precedence 010	0
3:2	R-Type TOS precedence 001	R/W	To assign priority queue of precedence 001	0
1:0	R-Type TOS precedence 000	R/W	To assign priority queue of precedence 000	0

M-Type TOS Priority Register

Table 136: M-Type TOS Priority Register (Page 30h: Address 32d–33d, 20h–21h)

Bit	Name	R/W	Description	Default
15:14	M-Type TOS precedence 111	R/W	To assign priority queue of precedence 111	0
13:12	M-Type TOS precedence 110	R/W	To assign priority queue of precedence 110	0

Table 136: M-Type TOS Priority Register (Page 30h: Address 32d–33d, 20h–21h) (Cont.)

Bit	Name	R/W	Description	Default
11:10	M-Type TOS precedence 101	R/W	To assign priority queue of precedence 101	0
9:8	M-Type TOS precedence 100	R/W	To assign priority queue of precedence 100	0
7:6	M-Type TOS precedence 011	R/W	To assign priority queue of precedence 011	0
5:4	M-Type TOS precedence 010	R/W	To assign priority queue of precedence 010	0
3:2	M-Type TOS precedence 001	R/W	To assign priority queue of precedence 001	0
1:0	M-Type TOS precedence 000	R/W	To assign priority queue of precedence 000	0

DiffServ DSCP Priority Register

Reg 30h to reg 3Fh are used to assign priority to different Differentiated Service. To provide four priority queues and 64 different traffic classes, a 64x2 table is needed. Each entry represents one traffic class, and two bits in that entry represent the priority of that traffic.

Table 137 and Table 138 define four entries. The rest 60 traffic classes are the same format as this one, so they will not be repeated here.

Table 137: DiffServ DSCP Priority Register (Page 30h: Address 48d–55d, 30h–37h)

Bit	Name	R/W	Description	Default
63:62	Priority of DSCP=011111	R/W	See detailed description above	0
…..	…….	R/W	–	
7:6	Priority of DSCP=000011	R/W	See detailed description above	0
5:4	Priority of DSCP=000010	R/W	See detailed description above	0
3:2	Priority of DSCP=000001	R/W	See detailed description above	0
1:0	Priority of DSCP=000000	R/W	See detailed description above	0

Table 138: DiffServ DSCP Priority Register (Page 30h: Address 56d–63d, 38h–3Fh)

Bit	Name	R/W	Description	Default
63:62	Priority of DSCP=111111	R/W	See detailed description above	0
7:6	Priority of DSCP=100011	R/W	See detailed description above	0
5:4	Priority of DSCP=100010	R/W	See detailed description above	0
3:2	Priority of DSCP=100001	R/W	See detailed description above	0
1:0	Priority of DSCP=100000	R/W	See detailed description above	0

Port-Based VLAN Registers

Table 139: Page 31h Port-Based VLAN Registers

Address	Bits	Description
00h–01h	10	Chip 0 Port 0 VLAN register
02h–03h	10	Chip 0 Port 1 VLAN register
04h–05h	10	Chip 0 Port 2 VLAN register
06h–07h	10	Chip 0 Port 3 VLAN register
08h–09h	10	Chip 0 Port 4 VLAN register
0Ah–0Bh	10	Chip 0 Port 5 VLAN register
0Ch–0Dh	10	Chip 0 Port 6 VLAN register
0Eh–0Fh	10	Chip 0 Port 7 VLAN register
10h–11h	10	Chip 0 Port 8 VLAN register
12h–13h	10	Chip 0 Port 9 VLAN register
14–1F	Reserved	
20h–21h	10	Chip 1 Port 0 VLAN register
22h–23h	10	Chip 1 Port 1 VLAN register
24h–25h	10	Chip 1 Port 2 VLAN register
26h–27h	10	Chip 1 Port 3 VLAN Register
28h–29h	10	Chip 1 Port 4 VLAN register
2Ah–2Bh	10	Chip 1 Port 5 VLAN register
2Ch–2Dh	10	Chip 1 Port 6 VLAN register
2Eh–2Fh	10	Chip 1 Port 7 VLAN register
30h–31h	10	Chip 1 Port 8 VLAN register
32h–33h	10	Chip 1 Port 9 VLAN register
34–3F	Reserved	
40h–41h	10	Chip 2 Port 0 VLAN register
42h–43h	10	Chip 2 Port 1 VLAN register
44h–45h	10	Chip 2 Port 2 VLAN register
46h–47h	10	Chip 2 Port 3 VLAN register
48h–49h	10	Chip 2 Port 4 VLAN register
4Ah–4Bh	10	Chip 2 Port 5 VLAN register
4Ch–4Dh	10	Chip 2 Port 6 VLAN register
4Eh–4Fh	10	Chip 2 Port 7 VLAN register
50h–51h	10	Chip 2 Port 8 VLAN register
52h–53h	10	Chip 2 Port 9 VLAN register
54–5F	Reserved	
60h–61h	10	Chip 3 Port 0 VLAN register

Table 139: Page 31h Port-Based VLAN Registers (Cont.)

Address	Bits	Description
62h–63h	10	Chip 3 Port 1 VLAN register
64h–65h	10	Chip 3 Port 2 VLAN register
66h–67h	10	Chip 3 Port 3 VLAN register
68h–69h	10	Chip 3 Port 4 VLAN register
6Ah–6Bh	10	Chip 3 Port 5 VLAN register
6Ch–6Dh	10	Chip 3 Port 6 VLAN register
6Eh–6Fh	10	Chip 3 Port 7 VLAN register
70h–71h	10	Chip 3 Port 8 VLAN register
72h–73h	10	Chip 3 Port 9 VLAN register
74–FE	Reserved	
FF	8	Page register

Chip x Port y VLAN Registers

Table 140 represents the range of chips using the wildcard x (0–3) and ports using the wildcard y (0–9) shown in Table 139 on page 178. Port 8 corresponds to the MII port and port 9 corresponds to the serial port.

Table 140: Chip x Port y VLAN Registers (Page 31h, Address 00h–73h)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	–	0
9	Serial Port Egress Enable	R/W	1 = Enables packets entering the switch at Chip x Port y to egress on the Serial Port of the local device. 0 = Blocks packets entering the switch at Chip x Port y from egressing on the Serial Port of the local device.	1
8	MII Port Egress Enable	R/W	1 = Enables packets entering the switch at Chip x Port y to egress on the MII Port of the local device. 0 = Blocks packets entering the switch at Chip x Port y from egressing on the MII Port of the local device.	1
7	Port 7 Egress Enable	R/W	1 = Enables packets entering the switch at Chip x Port y to egress on Port 7 of the local device. 0 = Blocks packets entering the switch at Chip x Port y from egressing on Port 7 of the local device.	1
6	Port 6 Egress Enable	R/W	1 = Enables packets entering the switch at Chip x Port y to egress on Port 6 of the local device. 0 = Blocks packets entering the switch at Chip x Port y from egressing on Port 6 of the local device.	1

Table 140: Chip x Port y VLAN Registers (Page 31h, Address 00h–73h) (Cont.)

Bit	Name	R/W	Description	Default
5	Port 5 Egress Enable	R/W	1 = Enables packets entering the switch at Chip x Port y to egress on Port 5 of the local device. 0 = Blocks packets entering the switch at Chip x Port y from egressing on Port 5 of the local device.	1
4	Port 4 Egress Enable	R/W	1 = Enables packets entering the switch at Chip x Port y to egress on Port 4 of the local device. 0 = Blocks packets entering the switch at Chip x Port y from egressing on Port 4 of the local device.	1
3	Port 3 Egress Enable	R/W	1 = Enables packets entering the switch at Chip x Port y to egress on Port 3 of the local device. 0 = Blocks packets entering the switch at Chip x Port y from egressing on Port 3 of the local device.	1
2	Port 2 Egress Enable	R/W	1 = Enables packets entering the switch at Chip x Port y to egress on Port 2 of the local device. 0 = Blocks packets entering the switch at Chip x Port y from egressing on Port 2 of the local device.	1
1	Port 1 Egress Enable	R/W	1 = Enables packets entering the switch at Chip x Port y to egress on Port 1 of the local device. 0 = Blocks packets entering the switch at Chip x Port y from egressing on Port 1 of the local device.	1
0	Port 0 Egress Enable	R/W	1 = Enables packets entering the switch at Chip x Port y to egress on Port 0 of the local device. 0 = Blocks packets entering the switch at Chip x Port y from egressing on Port 0 of the local device.	1

MAC-Based Trunking Registers

Table 141: Page 32h MAC-Based Trunking Registers

Addr	Bits	Description
00h	8	Reserved
01h	8	MAC-Based Trunk Control register
02h–8Fh	8	Reserved
90h–91h	16	Trunk Group 0 register
92h–93h	16	Trunk Group 1 register
94h–95h	16	Trunk Group 2 register
96h–97h	16	Trunk Group 3 register
FFh	8	Page register

MAC-Based Trunk Control Register

Table 142: MAC-Based Trunk Control Register (Page 32h, Address 01d, 01h)

Bit	Name	R/W	Description	Default
7:6	RESV	RO	Reserved	0
5:4	TRKG_CHIP_SEL	R/W	Specifies in what chip the trunk resides: 00 = Chip 0 01 = Chip 1 10 = Chip 2 11 = Chip 3	00
3	EN_FE_TRKG	R/W	1 = Enable local 10/100 port (Port0–Port7) trunking. The BCM5338M supports four different trunking groups. Each trunking group can support up to 8 ports (Port[7:0]). 0 = Disable.	0
2:0	RSEV	RO	Reserved	0

Trunk Group Register

Table 143: Trunk Group Register (Page 32h, Address 144–151d, 90–97h)

Bit	Name	R/W	Description	Default
15:8	RESV	RO	Reserved	0

Table 143: Trunk Group Register (Page 32h, Address 144–151d, 90–97h) (Cont.)

Bit	Name	R/W	Description	Default
7:0	TRNK_GRP	R/W	Per bit per trunk group vector: A bit mask corresponding to the physical ports on the chip. For physical ports which belong to the same trunk, the corresponding bit should be set to 1.	0

802.1Q VLAN Registers

Table 144: Page 34h 802.1Q VLAN Registers

Addr	Bits	Description
00h	8	802.1Q VLAN Control 0 register
01h	8	802.1Q VLAN Control 1 register
02h	8	802.1Q VLAN Control 2 register
03h	8	802.1Q VLAN Control 3 register
04h	8	802.1Q VLAN Control 4 register
05h	8	802.1Q VLAN Control 5 register
08h–09h	16	802.1Q VLAN and Secure MAC Table Access register
0Ah–0Bh	Reserved	
0Ch–0Dh	Reserved	
10h–11h	16	Default port 0's 802.1Q tag
12h–13h	16	Default port 1's 802.1Q tag
14h–15h	16	Default port 2's 802.1Q tag
16h–17h	16	Default port 3's 802.1Q tag
18h–19h	16	Default port 4's 802.1Q tag
1Ah–1Bh	16	Default port 5's 802.1Q tag
1Ch–1Dh	16	Default port 6's 802.1Q tag
1Eh–1Fh	16	Default port 7's 802.1Q tag
20h–21h	16	Default MII port's 802.1Q tag
22h–23h	16	Default SPI port's 802.1Q tag
30h–33h	32	802.1Q VLAN and Secure MAC Write register
34h–37h	32	802.1Q VLAN and Secure MAC Read register
38h–3Bh	32	Priority Remap register
3Ch–FEh	Reserved	
FFh	8	Page register

802.1Q VLAN Control 0 Register

Table 145: 802.1Q VLAN 0 Control Register (Page 34h, Address 0h)

Bit	Name	R/W	Description	Default
7	802.1Q VLAN Enable	R/W	1 = Enable 802.1q VLAN function.	0
6:5	VLAN Learning Mode	R/W	00 = SVL (Shared VLAN Learning Mode) (MAC used to hash ARL table) 11 = IVL (Individual VLAN Learning Mode) (MAC and VID used to hash ARL table) 10 = Illegal 01 = Illegal	11
4	Reserved	R/W	–	0
3:2	802.1Q Frame Control	R/W	00 = No Change 01 = Change Priority (3 bits) 10 = Change VID (12 bits) 11 = Change priority and VID (16 bits)	00
1:0	Reserved	RO	–	10

802.1Q VLAN Control 1 Register

Table 146: 802.1Q VLAN Control 1 Register (Page 34h, Address 1h)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Must be set to 0.	0
6	Enable IPMC Bypass Untag Map	R/W	When asserted, does not check the IPMC frame with Untag Map (see “Untag Map and Fwd Map” on page 77).	0
5	Enable IPMC Bypass Fwd Map	R/W	When asserted, does not check IPMC frame with Fwd Map (see “Untag Map and Fwd Map” on page 77).	0
4	Reserved	RO	Write as 0, ignore when read.	0
3	Enable RSV Mcast Untag Map	R/W	When asserted, reserved multicast frames are checked by Untag Map.	0
2	Enable RSV Mcast Fwd Map	R/W	When asserted, reserved multicast frames are checked by Fwd Map.	0
1	Enable RSV Mcast V Tagging	R/W	When asserted, reserved multicast frames are tagged according to VLAN rules.	0
0	Enable Special Entry VLAN Check	R/W	When a multiport MAC address (page 04h, offset 10–15h and 20–25h) is detected, the BCM5338M always bypasses ARL checking. The register provides the forwarding map. 1 = The two special entries (group0 and group1) address frames follow two VLAN rules (tagging, Untag Map). 0 = Bypass all VLAN checking (tagging, Fwd Map, Untag Map).	0

802.1Q VLAN Control 2 Register

Table 147: 802.1Q VLAN Control 2 Register (Page 34h, Address 2h)

Bit	Name	R/W	Description	Default
7	Enable Remap Priority Field	R/W	When asserted, the pri_field (3 bits) in ingress frame (802.1Q frame or priority tagged frame) is remapped to a new value based on re_map_reg[23:0]. The CFI bit is preserved as original frame. ***Note:*** SPI port and managed MII port do not support V_tagging. So they cannot support pri remap.	0
6:4	Reserved	RO	Write as 0, ignore when read.	0
3	en_MII_manage_bypass _Untag Map	R/W	When set to 1, frames received by MII_manage port bypass Untag Map.	0
2	en_MII_manage_bypass _Fwd Map	R/W	When set to 1, frames received by MII_manage port bypass Fwd Map checking. ***Note:*** Untagged frame received by MII_manage port are never tagged.	0
1	en_SPI_bypass_Untag Map	R/W	When set to 1, frames received by SPI port bypass Untag Map.	0
0	en_SPI_bypass_Fwd Map	R/W	When set to 1, frames received by SPI port bypass Fwd Map checking. ***Note:*** Untagged frame received by SPI port are never tagged.	0

802.1Q VLAN Control 3 Register

Table 148: 802.1Q VLAN Control 3 Register (Page 34h, Address 3h)

Bit	Name	R/W	Description	Default
7:0	Enable Drop Non 1Q Frame	R/W	Ports 8–1, respectively. When enabled, any non-1Q frame is dropped by this port.	0

802.1Q VLAN Control 4 Register

Table 149: 802.1Q VLAN Control 4 Register (Page 34h, Address 4h)

Bit	Name	R/W	Description	Default
7:6	ingress_VID_check	R/W	00 = Forward ingress VID violation frame (VID is not in Fwd Map) but do not learn in ARL table. 01 = Drop frame if frame has VID violation. 10 = Do not check ingress VID violation. ***Note:*** This rule does not apply to the SPI and MII_management port	10
5	en_ manage_receive_GVRP	R/W	When set to 1, the management port (the port with CPU) is the destination port of GVRP frame.	0
4	en_ manage_receive_GMRP	R/W	When set to 1, the management port (the port with CPU) is the destination port of GMRP frame.	0
3	Reserved	RO	Write as 0, ignore when read.	0
2:1	Reserved	RO	–	0
0	Enable Drop Non 1Q Frame	R/W	For the MII_port. ***Note:*** Only applies to MII as non-management port (no CPU on MII).	0

802.1Q VLAN Control 5 Register

Table 150: 802.1Q VLAN Control 5 Register (Page 34h, Address 5h)

Bit	Name	R/W	Description	Default
7	Reserved	RO	–	0
6	Presv_non_1q	R/W	When set to 1, non-1q incoming frames are not changed.	0
5	Dis_egress_dir_bypass_trunk	R/W	When set to 1, egress directed frames from management port do not bypass trunk checking logic (follow trunking results).	0
4	Reserved	RO	Write as 0, ignore when read.	0
3	drop_Vtable_miss	R/W	When set to 1, a frame with V_table miss is dropped When set to 0, a frame with V_table miss is flooded	0
2	Reserved	RO	Must be set to 0.	0
1	en_manage_rx_bypass_c rcchk	R/W	When set to 1, the management port (MII or SPI) with CPU on it ignores any CRC (BRCM tag frame or Ethernet frame). When set to 0 = The management port checks both CRCs (works as the BCM5318/BCM5328). ***Note:*** In previous BCM5318/BCM5328 designs, the management port needs to calculate CRC for both the Ethernet and BRCM tagged frames. Those two CRC calculations take a lot of CPU power and are not needed. With this option, the CPU does not need to calculate CRC for BRCM frame. If global_1Q_control5_g[2]=1, then the CPU does not need to generate Ethernet CRC either, and the Ethernet CRC is generated by the SPI port.	0
0	Enable tx port CRC generation	R/W	When en_1QVLAN =0 (default=0) 1 = Txport regenerates CRC even when en_1QVLAN = 0 0 = TXport does not re_generate CRC when en_1QVALN =0	0

Note: By setting bits 1:0 to 1, the CPU needs to only generate place holders for the inner and outer CRCs for any management packet.

802.1Q VLAN and Secure MAC Table Access Register

Table 151: 802.1Q VLAN and Secure MAC Table Access Register (Page 34h, Address 8h–9h)

Bit	Name	R/W	Description	Default
15	STMACSEC	R/W	1 = When asserted, Static MAC security table content can be changed or read. See MAC security page (Page 41h) for detail information 0 = When asserted, VLAN table content can be changed or read.	0
14	RESV	R/W	Reserved	0
13	Enable read/write operation	R/W SC	1 = When asserted, VLAN or Static Mac security table content can be changed or read. 0 = Disable read/write operation. This is self-clear bit. Internal circuit clears this bit after the command is executed.	0
12	Read/Write State (rd_wt_st)	R/W	1 = Write State. Write VLAN or Static Mac security content to assigned VID (vlan_ad) or address (for Static MAC security). 0 = Read State. Read VLAN or Static Mac security content from assigned VID (vlan_ad) or address (for Static MAC security).	0
11:0	VLAN ID	R/W	VID: ***Note:*** If STMACSEC is set to 1'b1, the lower 9 bits [8:0] are used to access static MAC security table.	FFF

802.1Q VLAN and Secure MAC Write Register

See "802.1Q VLAN and Secure MAC Table Access Register" on page 187.

Table 152: 802.1Q VLAN and Secure MAC Write Register (Page 34h, Address 30h–33h)

Bit	Name	R/W	Description	Default
When STMACSEC (802.1Q VLAN and Secure MAC Access register, bit 15) is set to a value of 0				
31:28	Reserved	RO	–	00
27	Valid	R/W	1 = Valid 0 = Invalid	0
26:22	SPT_ID	R/W	Spanning tree ID number.	00
21	SMP port untag enable	R/W	1 = Untag transmit packet via SMP port. 0 = Keep outgoing packet intact.	0
20	Reserved	RO	Write as 0, ignore on read.	0
19	MII port untag enable	R/W	1 = Untag transmit packet via MII port. 0 = Keep outgoing packet intact.	0
18:11	Port 7 ~ Port 0 untag enable	R/W	1 = Untag transmit packet via port 7 ~ port 0. 0 = Keep outgoing packet intact.	00

Table 152: 802.1Q VLAN and Secure MAC Write Register (Page 34h, Address 30h–33h) (Cont.)

Bit	Name	R/W	Description	Default
10	SMP port VLAN Group	R/W	1 = SMP is one of the assigned VID group. 0 = SMP is not one of the assigned VID group.	0
9	EXP port VLAN Group	R/W	1 = EXP is one of the assigned VID group. 0 = EXP is not one of the assigned VID group.	0
8	MII port VLAN Group	R/W	1 = MII is one of the assigned VID group. 0 = MII is not one of the assigned VID group.	0
7:0	Port 7 ~ Port 0 VLAN Group	R/W	1 = Port 7 ~ port 0 is one of the assigned VID group. 0 = Port 7 ~ port 0 is not one of the assigned VID group.	00
Note: When the MII port is programmed as the management port (IMP), it receives the frame with 1Q Tag information even if the MII is specified as untagged. The management port can strip off the BRCM tag and 1Q tag information at the same time.				
When STMACSEC (802.1Q VLAN and Secure MAC Access register, bit 15) is set to a value of 1				
31:25	Reserved	RO	–	00
24	Valid	R/W	1 = Valid 0 = Invalid ***Note:*** The valid bit is only for odd addresses specified in the 802.1Q VLAN and Secure MAC Access register (Page 34h, offset 8h). For even addresses, this bit is reserved.	
23:0	SA		**Source Address:** For even addresses specified in the 802.1Q VLAN and Secure MAC Access register, this is the low three bytes of the source address. For odd addresses 802.1Q VLAN and Secure MAC Access register, this is the three high bytes of the source address.	

802.1Q VLAN and Secure MAC Read Register

See "802.1Q VLAN and Secure MAC Table Access Register" on page 187.

Table 153: 802.1Q VLAN and Secure MAC Read Control Register (Page 34h, Address 34h–37h)

Bit	Name	R/W	Description	Default
When STMACSEC (802.1Q VLAN and Secure MAC Access register, bit 15) is set to a value of 0				
31:28	Reserved	RO	–	00
27	Valid	RO	Valid bit.	0
26:22	SPT_ID	RO	Spanning tree ID.	00
21:11	Untagged Port s	RO	The content of the VLAN entry of the corresponding assigned VID. Shown the untagged port of the specific VID.	000
10:0	VLAN Ports	RO	The content of the VLAN entry of the corresponding assigned VID. Shown which port belongs to the specific VID.	000

Table 153: 802.1Q VLAN and Secure MAC Read Control Register (Page 34h, Address 34h–37h) (Cont.)

Bit	Name	R/W	Description	Default
When STMACSEC (802.1Q VLAN and Secure MAC Access register, bit 15) is set to a value of 1				
31:25	Reserved	RO	–	00
24	Valid	RO	1 = Valid 0 = Invalid ***Note:*** The valid bit is only for odd addresses specified in the 802.1Q VLAN and Secure MAC Access register (Page 34h, offset 8h). For even addresses this bit is reserved.	
23:0	SA		**Source Address.** For even addresses specified in the 802.1Q VLAN and Secure MAC Access register, this is the low three bytes of the Source Address. For odd addresses 802.1Q VLAN and Secure MAC Access register, this is the three high bytes of the Source Address.	

802.1Q Default Port Tag Register

Table 154: Default Port 802.1Q Tag Registers

Addr	Bits	Description
10h–11h	16	Default port 0's 802.1Q tag
12h–13h	16	Default port 1's 802.1Q tag
14h–15h	16	Default Port 2's 802.1Q tag
16h–17h	16	Default port 3's 802.1Q tag
18h–19h	16	Default port 4's 802.1Q tag
1Ah–1Bh	16	Default port 5's 802.1Q tag
1Ch–1Dh	16	Default port 6's 802.1Q tag
1Eh–1Fh	16	Default port 7's 802.1Q tag
20h–21h	16	Default MII port's 802.1Q tag
22h–23h	16	Default SPI port's 802.1Q tag

Table 155: 802.1Q Default Port N's Tag Register (Page 34h, Address 10h–23h)

Bit	Name	R/W	Description	Default
15:0	Default Port 0's Tag	R/W	Default 802.1Q tag assigned to port 0. Default PVID should be 1, which is defined in 802.1q table 9-2.	{10'b0, chip_id[1:0], 4'b1111}
15:0	Default Port 1's Tag	R/W	Default 802.1Q tag assigned to port 1.	1{10'b0, chip_id[1:0], 4'b0001}

Table 155: 802.1Q Default Port N's Tag Register (Page 34h, Address 10h–23h) (Cont.)

Bit	Name	R/W	Description	Default
15:0	Default Port 2's Tag	R/W	Default 802.1Q tag assigned to port 2.	1{10'b0, chip_id[1:0], 4'b0010}
15:0	Default Port 3's Tag	R/W	Default 802.1Q tag assigned to port 3.	1{10'b0, chip_id[1:0], 4'b0011}
15:0	Default Port 4's Tag	R/W	Default 802.1Q tag assigned to port 4.	1{10'b0, chip_id[1:0], 4'b0100}
15:0	Default Port 5's Tag	R/W	Default 802.1Q tag assigned to port 5.	1{10'b0, chip_id[1:0], 4'b0101}
15:0	Default Port 6's Tag	R/W	Default 802.1Q tag assigned to port 6.	1{10'b0, chip_id[1:0], 4'b0110}
15:0	Default Port 7's Tag	R/W	Default 802.1Q tag assigned to port 7.	1{10'b0, chip_id[1:0], 4'b0111}
15:0	Default MII Port's Tag	R/W	Default 802.1Q tag assigned to MII port.	1{10'b0, chip_id[1:0], 4'b1000}
15:0	Default SPI Port's Tag	R/W	Default 802.1Q tag assigned to SPI port.	1{10'b0, chip_id[1:0], 4'b1010}

Priority Remap Register

Table 156: 802.1Q VLAN Read Control Register (Page 34h, Address 38h–3Bh)

Bit	Name	R/W	Description	Default
23:0	re_map_reg	R/W	When 1) control2[7]=1 and 2) control0[0]=1 and 3) control0[2]=1 The original frames's pri is then remapped to the one in re_map_reg[23:0]. The mapping rules are: **OLD PRI NEW PRI** 000 re_map_reg[2:0] 001 re_map_reg[5:3] 010 re_map_reg[8:6] 011 re_map_reg[11:9] 100 re_map_reg[14:12] 101 re_map_reg[17:15] 110 re_map_reg[20:18] 111 re_map_reg[23:21] ** If the incoming frame is a pri_tagged or tagged frame, it is re_mapped. If the re_maping feature is enabled, it is the PRI field. ** If the incoming frame is an un_tagged frame, then it is used in default_tag as the new PRI.	0

Broadcast/Multicast Suppression Registers

Table 157: Page 35h Broadcast/Multicast Suppression Registers

Addr	Bits	Description
00h	8	Port 0 Suppression Control register
01h	8	Port 1 Suppression Control register
02h	8	Port 2 Suppression Control register
03h	8	Port 3 Suppression Control register
04h	8	Port 4 Suppression Control register
05h	8	Port 5 Suppression Control register
06h	8	Port 6 Suppression Control register
07h	8	Port 7 Suppression Control register
08h	8	MII Port Suppression Control register
09h–FEh	Reserved	
FFh	8	Page register

Suppression Control Register

Table 158: Suppression Control Register (Page 35h, Address 00–08d, 00–08h)

Bit	Name	R/W	Description	Default
7	mratecnt_drop_frame	RO/RC	When bcast/mcast/dlf frames were dropped, this bit is set. It is clear after this address is accessed.	0
6	Enable mcast	R/W	Enable multicast packets to be dropped when they are over the selected rate in bit[1:0]. 1: Enable 0: Disable	0
5	Enable bcast	R/W	Enable broadcast packets to be dropped when they are over the selected rate in bit[1:0]. 1: Enable 0: Disable	0
4	Enable DLF	R/W	Enable DLF (destination MAC address lookup failure) packets to be dropped when they are over the selected rate in bit[1:0]. 1: Enable 0: Disable	0
3:2	mcast_burst_length_sel	R/W	00 = burst_length = 2*1024 byte 01 = burst_length = 4*1024 byte 10 = burst_length = 6*1024 byte 11 = burst_length = 8*1024 byte	00

Table 158: Suppression Control Register (Page 35h, Address 00–08d, 00–08h) (Cont.)

Bit	Name	R/W	Description	Default
1:0	mcast_rate_sel		00 = 3.3% mcast/bcast/dlf 01 = 5% mcast/bcast/dlf 10 = 10% mcast/bcast/dlf 11 = 20% mcast/bcast/dlf	00

802.1x Registers

Table 159: Page 40h 802.1x Registers

Addr	Bits	Description
00h–03h	32	EAP Global Configuration register
04h–0Fh	Reserved	
10h–17h	64	EAP Destination IP register 0
18h–17h	64	EAP Destination IP register 1
20h–27h	64	Port 0 EAP Configuration register
28h–2Fh	64	Port 1 EAP Configuration register
30h–37h	64	Port 2 EAP Configuration register
38h–3Fh	64	Port 3 EAP Configuration register
40h–47h	64	Port 4 EAP Configuration register
48h–4Fh	64	Port 5 EAP Configuration register
50h–57h	64	Port 6 EAP Configuration register
58h–5Fh	64	Port 7 EAP Configuration register
60h–67h	64	Port MII EAP Configuration register
68h–FEh	Reserved	
FFh	8	Page register

EAP Global Configuration Register

Table 160: EAP Global Configuration Register (Page 40h, Address 00–03d, 00–03h)

Bit	Name	R/W	Description	Default
32:23	RESV	R/W	Reserved.	0
22	EN_2_DIP	R/W	Enable Destination IP Address when EAP_BLK_MODE is set. When set, IPv4 packet with destination IP address matched with EAP Destination IP register 0/1 passes.	0
21	EN_ARP	R/W	Enable ARP frame when EAP_BLK_MODE is set. When set, ARP frame (DA = FF-FF-FF-FF-FF-FF & LT = 08-06) passes.	0

Table 160: EAP Global Configuration Register (Page 40h, Address 00–03d, 00–03h) (Cont.)

Bit	Name	R/W	Description	Default
20	EN_MAC_2F	R/W	Enable (DA = 01-80-c2-00-00-2F) frame passed when EAP_BLK_MODE is set.	0
19	EN_MAC_2E	R/W	Enable (DA = 01-80-c2-00-00-2E) frame passed when EAP_BLK_MODE is set.	0
18	EN_MAC_2D	R/W	Enable (DA = 01-80-c2-00-00-2D) frame passed when EAP_BLK_MODE is set.	0
17	EN_MAC_2C	R/W	Enable (DA = 01-80-c2-00-00-2C) frame passed when EAP_BLK_MODE is set.	0
16	EN_MAC_2B	R/W	Enable (DA = 01-80-c2-00-00-2B) frame passed when EAP_BLK_MODE is set.	0
15	EN_MAC_2A	R/W	Enable (DA = 01-80-c2-00-00-2A) frame passed when EAP_BLK_MODE is set.	0
14	EN_MAC_29	R/W	Enable (DA = 01-80-c2-00-00-29) frame passed when EAP_BLK_MODE is set.	0
13	EN_MAC_28	R/W	Enable (DA = 01-80-c2-00-00-28) frame passed when EAP_BLK_MODE is set.	0
12	EN_MAC_27	R/W	Enable (DA = 01-80-c2-00-00-27) frame passed when EAP_BLK_MODE is set.	0
11	EN_MAC_26	R/W	Enable (DA = 01-80-c2-00-00-26) frame passed when EAP_BLK_MODE is set.	0
10	EN_MAC_25	R/W	Enable (DA = 01-80-c2-00-00-25) frame passed when EAP_BLK_MODE is set.	0
9	EN_MAC_24	R/W	Enable (DA = 01-80-c2-00-00-24) frame passed when EAP_BLK_MODE is set.	0
8	EN_MAC_23	R/W	Enable (DA = 01-80-c2-00-00-23) frame passed when EAP_BLK_MODE is set.	0
7	EN_MAC_22	R/W	Enable (DA = 01-80-c2-00-00-22) frame passed when EAP_BLK_MODE is set.	0
6	EN_MAC_21	R/W	Enable (DA = 01-80-c2-00-00-21) frame passed when EAP_BLK_MODE is set.	0
5	EN_MAC_20	R/W	Enable (DA = 01-80-c2-00-00-20) frame passed when EAP_BLK_MODE is set.	0
4	EN_MAC_10	R/W	Enable (DA = 01-80-c2-00-00-10) frame passed when EAP_BLK_MODE is set.	0
3	EN_MAC_02_04_0F	R/W	Enable (DA = 01-80-c2-00-00-02) or (DA = 01-80-c2-00-00-04 ~ 0F) frame passed when EAP_BLK_MODE is set.	0
2	EN_MAC_BPDU	R/W	Enable BPDU frame passed when EAP_BLK_MODE is set.	0
1	DIS_OLD_MAN03	R/W	Disable old management mode for DA = 01-80-c2-00-00-03. In management mode, the BCM5325/BCM5328 always forwards 01-80-c2-00-00-03 frame to management port. For the BCM5338M, when in management mode and this bit is set, this forwarding path is disabled such that the BCM5338M can qualify EAPOL with DA, EtherType, and PacketType.	0
0	EN_EAP_PT_CHK	R/W	Enable EAP frame packet type check.	0

EAP Destination IP Register 0

Table 161: EAP Destination IP Register 0 (Page 40h, Address 16–23d, 10–17h)

Bit	Name	R/W	Description	Default
63:32	DIP_SUB_REG_0	R/W	EAP Destination IP Subnet register 0	0
31:0	DIP_MASK_REG_0	R/W	EAP Destination IP Mask register 0	0

EAP Destination IP Register 1

Table 162: EAP Destination IP Register 1 (Page 40h, Address 24–31d, 18–1Fh)

Bit	Name	R/W	Description	Default
63:32	DIP_SUB_REG_1	R/W	EAP Destination IP Subnet register 1	0
31:0	DIP_MASK_REG_1	R/W	EAP Destination IP Mask register 1	0

Port EAP Configuration Register

Table 163: Port EAP Configuration Registers

Addr	Bits	Description
20h–27h	64	Port 0 EAP Configuration register
28h–2Fh	64	Port 1 EAP Configuration register
30h–37h	64	Port 2 EAP Configuration register
38h–3Fh	64	Port 3 EAP Configuration register
40h–47h	64	Port 4 EAP Configuration register
48h–4Fh	64	Port 5 EAP Configuration register
50h–57h	64	Port 6 EAP Configuration register
58h–5Fh	64	Port 7 EAP Configuration register
60h–67h	64	Port MII EAP Configuration register

Table 164: Port 0 EAP Configuration Register (Page 40h, Address 32–103d, 20–67h)

Bit	Name	R/W	Description	Default
63:51	RSEV	R/W	Reserved.	0
50	EAP_EN	R/W	Enable EAP (802.1x) function.	0
49	EAP_BLK_MODE	R/W	When set, only frames defined in EAP_GCFG[22:1] are received, and other frames are dropped.	0
48	EAP_EN_UNI_DA	R/W	Enable EAP frame with Unicast DA.	0
47:0	EAP_UNI_DA	R/W	EAP frame Unicast DA register.	0

MAC Address Security Registers

Table 165: Page 41h MAC Address Security Registers

Addr	*Bits*	*Description*
00h–01h	16	MAC Address Security Control register 0
02h–03h	16	MAC Address Security Control register 1
04h–05h	16	MAC Address Security Control register 2
06h	8	MAC Address Security Control register 3
07h–0Fh	Reserved	
10h–11h	16	Port 0 Current SA Count for Dynamic mode
12h–13h	16	Port 1 Current SA Count for Dynamic mode
14h–15h	16	Port 2 Current SA Count for Dynamic mode
16h–17h	16	Port 3 Current SA Count for Dynamic mode
18h–19h	16	Port 4 Current SA Count for Dynamic mode
1Ah–1Bh	16	Port 5 Current SA Count for Dynamic mode
1Ch–1Dh	16	Port 6 Current SA Count for Dynamic mode
1Eh–1Fh	16	Port 7 Current SA Count for Dynamic mode
20h–21h	16	Port 0 Dynamic Learning Threshold register
22h–23h	16	Port 1 Dynamic Learning Threshold register
24h–25h	16	Port 2 Dynamic Learning Threshold register
26h–27h	16	Port 3 Dynamic Learning Threshold register
28h–29h	16	Port 4 Dynamic Learning Threshold register
2Ah–2Bh	16	Port 5 Dynamic Learning Threshold register
2Ch–2Dh	16	Port 6 Dynamic Learning Threshold register
2Eh–2Fh	16	Port 7 Dynamic Learning Threshold register
30h–FEh	Reserved	
FFh	8	Page register

MAC Address Security Control Register 0

Table 166: MAC Address Security Control Register 0 (Page 41h, Address 00–01d, 00–01h)

Bit	Name	R/W	Description	Default
15:13	RESV	R/W	Reserved.	0
12	SEC_MAC_1X_PASS	R/W	When SA field of incoming frame violate the MAC Address Control rule, this frame is dropped. However, set this bit to 1'b1 to enable EAP frame always passed. 1 = EAP frame passed 0 = EAP frame rejected	1
11:9	MAC_SEC_CON_P3	R/W	**Security Control for Port 3.** 0xx = No security function 100 = Static mode with accept function 101 = Static mode with reject function 110 = Dynamic mode (only check SA number) 111 = Dynamic mode (check SA matched in ARL)	0
8:6	MAC_SEC_CON_P2	R/W	**Security Control for Port 2.** 0xx = No security function 100 = Static mode with accept function 101 = Static mode with reject function 110 = Dynamic mode (only check SA number) 111 = Dynamic mode (check SA matched in ARL)	0
5:3	MAC_SEC_CON_P1	R/W	**Security Control for Port 1.** 0xx = No security function 100 = Static mode with accept function 101 = Static mode with reject function 110 = Dynamic mode (only check SA number) 111 = Dynamic mode (check SA matched in ARL)	0
2:0	MAC_SEC_CON_P0	R/W	**Security Control for Port 0.** 0xx = No security function 100 = Static mode with accept function 101 = Static mode with reject function 110 = Dynamic mode (only check SA number) 111 = Dynamic mode (check SA matched in ARL)	0

MAC Address Security Control Register 1

Table 167: MAC Address Security Control Register 1 (Page 41h, Address 02–03d, 02–03h)

Bit	Name	R/W	Description	Default
15:12	RESV	R/W	Reserved	0
11:9	MAC_SEC_CON_P7	R/W	**Security Control for Port 7.** 0xx = No security function 100 = Static mode with accept function 101 = Static mode with reject function 110 = Dynamic mode (only check SA number) 111 = Dynamic mode (check SA matched in ARL)	0
8:6	MAC_SEC_CON_P6	R/W	**Security Control for Port 6.** 0xx = No security function 100 = Static mode with accept function 101 = Static mode with reject function 110 = Dynamic mode (only check SA number) 111 = Dynamic mode (check SA matched in ARL)	0
5:3	MAC_SEC_CON_P5	R/W	**Security Control for Port 5.** 0xx = No security function 100 = Static mode with accept function 101 = Static mode with reject function 110 = Dynamic mode (only check SA number) 111 = Dynamic mode (check SA matched in ARL)	0
2:0	MAC_SEC_CON_P4	R/W	**Security Control for Port 4.** 0xx = No security function 100 = Static mode with accept function 101 = Static mode with reject function 110 = Dynamic mode (only check SA number) 111 = Dynamic mode (check SA matched in ARL)	0

MAC Address Security Control Register 2

Table 168: MAC Address Security Control Register 2 (Page 41h, Address 04–05d, 04–05h)

Bit	Name	R/W	Description	Default
15:13	STATIC_MAC_NO	R/W	**Static Mode MAC Address Number.** Indicates how many static MAC address entries supported in the system per port. 111 = 16 Static MAC address entries 110 = 14 Static MAC address entries 101 = 12 Static MAC address entries 100 = 10 Static MAC address entries 011 = Eight Static MAC address entries 010 = Six Static MAC address entries 001 = Four Static MAC address entries 000 = Two Static MAC address entries	111
12:0	Reserved	RO		FFF

Note: Programming the Static MAC addresses is done via the 802.1Q VLAN and Secure MAC Access register (Page 34h, offset 08h (see Table 151 on page 187) and the Secure MAC Write register (page 34h, offset 30h) (see Table 152 on page 187).

MAC Address Security Control Register 3

Table 169: MAC Address Security Control Register 3 (Page 41h, Address 06d, 06h)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Write as 0, ignore when read.	0
7:0	SEC_MAC_BLK_MODE[7:0]	R/W	When SA field of incoming frame violate the MAC Address Control rule, this frame is dropped. However, set this bit to 1'b1 to enable special frame always passed. (One bit for each port.) 1 = Special frame passed. 0 = Special frame rejected.	0

MAC Address Security Control Register 4

Table 170: MAC Address Security Control Register 4 (Page 41h, Address 08d, 08h)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Write as 0, ignore when read.	0
7:0	DYN_SA_Cnt_Rst	R/W	**Port Current SA Count Reset Bit Per Port.** Bits 0–7 = 10/100BASE-T ports.	0

Port Current SA Count for Dynamic Mode

Table 171: Port Current SA Count for Dynamic Mode Registers

Addr	Bits	Description
10h–11h	16	Port 0 current SA count for dynamic mode
12h–13h	16	Port 1 current SA count for dynamic mode
14h–15h	16	Port 2 current SA count for dynamic mode
16h–17h	16	Port 3 current SA count for dynamic mode
18h–19h	16	Port 4 current SA count for dynamic mode
1Ah–1Bh	16	Port 5 current SA count for dynamic mode
1Ch–1Dh	16	Port 6 current SA count for dynamic mode
1Eh–1Fh	16	Port 7 current SA count for dynamic mode

Table 172: Port Current SA Count for Dynamic Mode (Page 41h, Address 16–31d, 10–1Fh)

Bit	Name	R/W	Description	Default
15:12	RESV	RO	Reserved	0
11:0	CUR_SA_CNT_Px	RO	Port Current SA count for dynamic mode	0

Port X Dynamic Learning Threshold Register

Table 173: Port Dynamic Learning Threshold Register

Addr	Bits	Description
20h–21h	16	Port 0 Dynamic Learning Threshold register
22h–23h	16	Port 1 Dynamic Learning Threshold register
24h–25h	16	Port 2 Dynamic Learning Threshold register
26h–27h	16	Port 3 Dynamic Learning Threshold register
28h–29h	16	Port 4 Dynamic Learning Threshold register
2Ah–2Bh	16	Port 5 Dynamic Learning Threshold register
2Ch–2Dh	16	Port 6 Dynamic Learning Threshold register
2Eh–2Fh	16	Port 7 Dynamic Learning Threshold register

Note: These registers set the maximum number of Source Addresses that can be in the ARL table for a specific port.

Table 174: Port x Dynamic Learning Threshold Register (Page 41h, Address 32–47d, 20–2Fh)

Bit	Name	R/W	Description	Default
15:12	RESV	RO	Reserved.	0
11:0	DYN_MAX_MAC_NO_Px	R/W	Dynamic Mode Maximum MAC Address Number for each port. {DYN_MAX_MAC_NO[11:0]} indicates the maximum number of MAC addresses that can be learned for this port.	FFF

Ingress/Egress Rate Control Registers

Table 175: Page 42h Ingress/Egress Rate Control Registers

Addr	Bits	Description
00h–03h	32	Common Ingress Rate Control Configuration register
04h–0Fh	Reserved	
10h–13h	32	Port 0 Ingress Rate Control Configuration register
14h–17h	32	Port 1 Ingress Rate Control Configuration register
18h–1Bh	32	Port 2 Ingress Rate Control Configuration register
1Ch–1Fh	32	Port 3 Ingress Rate Control Configuration register
20h–23h	32	Port 4 Ingress Rate Control Configuration register
24h–27h	32	Port 5 Ingress Rate Control Configuration register
28h–2Bh	32	Port 6 Ingress Rate Control Configuration register
2Ch–2Fh	32	Port 7 Ingress Rate Control Configuration register
30h–33h	32	Port MII Ingress Rate Control Configuration register
34h–3Fh	Reserved	
40h–41h	16	Port 0 Egress Rate Control Configuration register
42h–43h	16	Port 1 Egress Rate Control Configuration register
44h–45h	16	Port 2 Egress Rate Control Configuration register
46h–47h	16	Port 3 Egress Rate Control Configuration register
48h–49h	16	Port 4 Egress Rate Control Configuration register
4Ah–4Bh	16	Port 5 Egress Rate Control Configuration register
4Ch–4Dh	16	Port 6 Egress Rate Control Configuration register
4Eh–4Fh	16	Port 7 Egress Rate Control Configuration register
50h–51h	16	Port MII Egress Rate Control Configuration register
52h–EFh	Reserved	
FFh	8	Page register

Common Ingress Rate Control Configuration Register

Table 176: Common Ingress Rate Control Configuration Register (Page 42h, Address 00–03d, 00–03h)

Bit	Name	R/W	Description	Default
31:17	RSEV	RO	Reserved	0
16	XLENEN	R/W	**Extra Length Calculate Enable.** 1 = IPG+Premble is Calculated 0 = Original mode.	0
15	RATE_TYPE1	R/W	**Rate Type for Bucket 1.** 0 = Fixed bit rate style 1 = Ratio style	0
14	DROP_EN1	R/W	Drop Enable for Bucket 1	0
13:8	PKT_MSK1	R/W	**Packet Mask for Bucket 1.** Bit 13 = Destination Lookup Fail (DLF) Bit 12 = MAC Control Frame (MCF) Bit 11 = Broadcast with LT >= 16'h0600 Bit 10 = Broadcast with LT < 16'h0600 Bit 9 = Other Multicast Frame Bit 8 = Unicast Frame	0
7	RATE_TYPE0	R/W	**Rate Type for Bucket 0.** 0 = Fixed bit rate style 1 = Ratio style	0
6	DROP_EN0	R/W	Drop Enable for Bucket 0	0
5:0	PKT_MSK0	R/W	**Packet Mask for Bucket 0.** Bit 5 = Destination Lookup Fail (DLF) Bit 4 = MAC Control Frame (MCF) Bit 3 = Broadcast with LT >= 16'h0600 Bit 2 = Broadcast with LT < 16'h0600 Bit 1 = Other Multicast Frame Bit 0 = Unicast Frame	0

Port Ingress Rate Control Configuration Register

Table 177: Ingress Rate Control Configuration Registers

Addr	Bits	Description
10h–13h	32	Port 0 Ingress Rate Control Configuration register
14h–17h	32	Port 1 Ingress Rate Control Configuration register
18h–1Bh	32	Port 2 Ingress Rate Control Configuration register
1Ch–1Fh	32	Port 3 Ingress Rate Control Configuration register
20h–23h	32	Port 4 Ingress Rate Control Configuration register
24h–27h	32	Port 5 Ingress Rate Control Configuration register
28h–2Bh	32	Port 6 Ingress Rate Control Configuration register
2Ch–2Fh	32	Port 7 Ingress Rate Control Configuration register
30h–33h	32	Port MII Ingress Rate Control Configuration register

Table 178: Port Ingress Rate Control Configuration Register (Page 42h, Address 16–51d, 10–33h)

Bit	Name	R/W	Description	Default
31:23	RESV	RO	Reserved	0
22	ING_RC_EN	R/W	Ingress rate control enable	0
21:19	BUCKET_SIZE1	R/W	Bucket Size for Bucket 1: 000 = 6 KB 001 = 10 KB 010 = 18 KB 011 = 34 KB 100 = 66 KB 101 = 126 KB 110–111 = Reserved	0
18	RESV	RO	Reserved	0
17:11	REF_CNT1	R/W	Refresh Count for Bucket 1	0
10:8	BUCKET_SIZE0	R/W	Bucket Size for Bucket 0: 000 = 6 KB 001 = 10 KB 010 = 18 KB 011 = 34 KB 100 = 66 KB 101 = 126 KB 110–111 = Reserved	0
7	RESV	RO	Reserved	0
6:0	REF_CNT0	R/W	Refresh Count for Bucket 0	0

By setting bit rate style in the "Common Ingress Rate Control Configuration Register" on page 201 and the refresh count, the BCM5338M can change the bit rate of each port.

- If the bit rate style is 0, the refresh count is used to define the bit rate directly. The refresh count affects the resolution of bit rate and refreshes the rate of bucket (see Table 179). When the refresh count is between:
  - 1 and 28, the formula Nx8x1024/125 is used to calculate the bit rate.
  - 29 and 127, the formula (N-27)x1024 is used to get the bit rate where N is refresh count.

  This table is precise when DROP_EN is set to 1 (page 42h; offset 00h; bit 14/6).

Table 179: Port Bit Rate (Bit Rate Style = 0)

Refresh Count	*Formula*	*Bit Rate*	*Resolution*	*Refresh Rate*
1–28	= Nx8x1024/125	64 KB, 128 KB, 192 KB, ... , 1.792 MB	64 KB	125 µs
29–127	= (N-27)x1024	2 MB, 3 MB, 4 MB, … , 100 MB	1 MB	8 µs

- If the bit rate style is 1, the refresh count is used to define the ratio of the bit rate for different link speed. From Table 180, the ratio of the bit rate is always N/1.25 under any link speed.

  This table is precise when DROP_EN set to 1 (page 42h; offset 00h; bit 14/6).

Table 180: Port Bit Rate (Bit Rate Style = 1)

Speed	*Refresh Count*	*Formula*	*Bit Rate*	*Resolution*	*Refresh Rate*
10 Mb	1–125	= Nx8x1024/100	0.08 MB, 0.16 MB, 0.24 MB, … , 10 MB	0.08 MB	100 µs
100 Mb	1–125	= Nx8x1024/10	0.8 MB, 1.6 MB, 2.4 MB, … , 100 MB	0.8 MB	10 µs

Port Egress Rate Control Configuration Register

Table 181: Egress Rate Control Configuration Registers

Addr	*Bits*	*Description*
40h–41h	16	Port 0 Egress Rate Control Configuration register
42h–43h	16	Port 1 Egress Rate Control Configuration register
44h–45h	16	Port 2 Egress Rate Control Configuration register
46h–47h	16	Port 3 Egress Rate Control Configuration register
48h–49h	16	Port 4 Egress Rate Control Configuration register
4Ah–4Bh	16	Port 5 Egress Rate Control Configuration register
4Ch–4Dh	16	Port 6 Egress Rate Control Configuration register
4Eh–4Fh	16	Port 7 Egress Rate Control Configuration register
50h–51h	16	Port MII Egress Rate Control Configuration register

Table 182: Port Egress Rate Control Configuration Register (Page 42h, Address 64–81d, 40–51h)

Bit	Name	R/W	Description	Default
15:12	RESV	RO	Reserved	0
11	ENG_RC_EN	R/W	Egress rate control enable	0
10:8	BUCKET_SIZE	R/W	Bucket size: 000 = 6 KB 001 = 10 KB 010 = 18 KB 011 = 34 KB 100 = 66 KB 101 = 126 KB 110–111 = Reserved	0
7	RESV	RO	Reserved	0
6:0	REF_CNT	R/W	Refresh count for bucket	0

802.1s Multiple Spanning Tree Registers

Table 183: Page 43h 802.1s Multiple Spanning Tree Registers

Address	Bits	Description
00h	8	MST (Multiple Spanning Tress) Control registers
01h–07h	Reserved	
08h–09h	16	Chip 0 Port-Based Aging Control register
0Ah–0Bh	16	Chip 1 Port-Based Aging Control register
0Ch–0Dh	16	Chip 2 Port-Based Aging Control register
0Eh–0Fh	16	Chip 3 Port-Based Aging Control register
10h–13h	32	MST 0 Table register
14h–17h	32	MST 1 Table register
18h–1Bh	32	MST 2 Table register
1Ch–1Fh	32	MST 3 Table register
20h–23h	32	MST 4 Table register
24h–27h	32	MST 5 Table register
28h–2Bh	32	MST 6 Table register
2Ch–2Fh	32	MST 7 Table register
30h–33h	32	MST 8 Table register
34h–37h	32	MST 9 Table register
38h–3Bh	32	MST 10 Table register
3Ch–3Fh	32	MST 11 Table register

Table 183: Page 43h 802.1s Multiple Spanning Tree Registers (Cont.)

Address	Bits	Description
40h–43h	32	MST 12 Table register
44h–47h	32	MST 13 Table register
48h–4Bh	32	MST 14 Table register
4Ch–4Fh	32	MST 15 Table register
50h–53h	32	MST 16 Table register
54h–57h	32	MST 17 Table register
58h–5Bh	32	MST 18 Table register
5Ch–5Fh	32	MST 19 Table register
60h–63h	32	MST 20 Table register
64h–67h	32	MST 21 Table register
68h–6Bh	32	MST 22 Table register
6Ch–6Fh	32	MST 23 Table register
70h–73h	32	MST 24 Table register
74h–77h	32	MST 25 Table register
78h–7Bh	32	MST 26 Table register
7Ch–7Fh	32	MST 27 Table register
80h–83h	32	MST 28 Table register
84h–87h	32	MST 29 Table register
88h–8Bh	32	MST 30 Table register
8Ch–8Fh	32	MST 31 Table register
90h–FEh	Reserved	
FFh	8	Page register

Multiple Spanning Tree Control Register

Table 184: Multiple Spanning Tree Control Register (Page 43h, Address 00d, 00h)

Bit	Name	R/W	Description	Default
7:4	RSEV	RO	Reserved.	0
3	ARL_FAST_AGING_CYCLE_EN	R/W	This bit is set by the host to initiate the fast-aging cycle. If the ARL entry is valid, the fast-aging cycle clears the AGE bit provided the FAST_AGE_EN bit of the corresponding chip is set. The cycle terminates after the AGE bit of the last valid entry is reset. This bit is self-clear at the end of the cycle.	0
2	En_802_1s	R/W	1 = Support 802.1s (multiple spanning tree); spanning tree status is fetched from MST_table. 0 = Only one spanning tree supported (original mode).	0

Table 184: Multiple Spanning Tree Control Register (Page 43h, Address 00d, 00h) (Cont.)

Bit	Name	R/W	Description	Default
1	AGE_MODE_SPT	R/W	Aging mode control, per-spanning tree, following MST setting.	0
0	AGE_MODE_PORT	R/W	Aging mode control, per port, following per port setting.	0

Chip 0 Port-Based Aging Control Register

Table 185: Chip 0 Port-Based Aging Control Register (Page 43h, Address 08–09d, 08–09h)

Bit	Name	R/W	Description	Default
15:14	RSEV	RO	Reserved.	0
13	FAST_AGE_EN	R/W	Fast aging enable: When set, the fast-aging cycle clears the AGE bit of ARL entries per chip ID 0.	0
12	STATIC_AGING_EN	R/W	Static aging enable: When set, the aging process invalidates all static entries in the ARL table per chip ID 0.	0
10	AGE_EN_CPU	R/W	Per port aging enable for CPU port.	0
9	RSEV	RO	Reserved.	0
8	AGE_EN_MII	R/W	Per port aging enable for MII port.	0
7:0	AGE_EN_PORT[7:0]	R/W	Per port aging enable for PORT[7:0].	00

Chip 1 Port-Based Aging Control Register

Table 186: Chip 1 Port-Based Aging Control Register (Page 43h, Address 10–11d, 0A–0Bh)

Bit	Name	R/W	Description	Default
15:14	RSEV	RO	Reserved.	0
13	FAST_AGE_EN	R/W	Fast aging enable: When set, the fast-aging cycle clears the AGE bit of ARL entries per chip ID 1.	0
12	STATIC_AGING_EN	R/W	Static aging enable: When set, the aging process invalidates all static entries in the ARL table per chip ID 1.	0
10	AGE_EN_CPU	R/W	Per port aging enable for CPU port.	0
9	RSEV	RO	Reserved.	0
8	AGE_EN_MII	R/W	Per port aging enable for MII port.	0
7:0	AGE_EN_PORT[7:0]	R/W	Per port aging enable for PORT[7:0].	00

Chip 2 Port-Based Aging Control Register

Table 187: Chip 2 Port-Based Aging Control Register (Page 43h, Address 12–13d, 0C–0Dh)

Bit	Name	R/W	Description	Default
15:14	RSEV	RO	Reserved.	0
13	FAST_AGE_EN	R/W	Fast aging enable: When set, the fast-aging cycle clears the AGE bit of ARL entries per chip ID 2.	0
12	STATIC_AGING_EN	R/W	Static aging enable: When set, the aging process invalidates all static entries in the ARL table per chip ID 2.	0
10	AGE_EN_CPU	R/W	Per port aging enable for CPU port.	0
9	RSEV	RO	Reserved.	0
8	AGE_EN_MII	R/W	Per port aging enable for MII port.	0
7:0	AGE_EN_PORT[7:0]	R/W	Per port aging enable for PORT[7:0].	00

Chip 3 Port-Based Aging Control Register

Table 188: Chip 3 Port-Based Aging Control Register (Page 43h, Address 14–15d, 0E–0Fh)

Bit	Name	R/W	Description	Default
15:14	RSEV	RO	Reserved.	0
13	FAST_AGE_EN	R/W	Fast aging enable: When set, the fast-aging cycle clears the AGE bit of ARL entries per chip ID 3.	0
12	STATIC_AGING_EN	R/W	Static aging enable: When set, the aging process invalidates all static entries in the ARL table per chip ID 3.	0
10	AGE_EN_CPU	R/W	Per port aging enable for CPU port.	0
9	RSEV	RO	Reserved.	0
8	AGE_EN_MII	R/W	Per port aging enable for MII port.	0
7:0	AGE_EN_PORT[7:0]	R/W	Per port aging enable for PORT[7:0].	00

Mst Table Register

Table 189: MST Table Register (Page 43h, Address 16–143d, 10–8Fh)

Bit	Name	R/W	Description	Default
31:19	RSEV	RO	Reserved	0
18	SPT_AGE_EN	R/W	Spanning tree aging enable	0

Table 189: MST Table Register (Page 43h, Address 16–143d, 10–8Fh) (Cont.)

Bit	Name	R/W	Description	Default
17:16	SPT_STA_PORT_MII	R/W	**Spanning Tree State for PORT MII.** 00 = Disable state 01 = Standby state (blocking) 10 = Unstable state (listing/learning) 11 = Normal state (forwarding or no spanning tree)	00
15:14	SPT_STA_PORT7	R/W	**Spanning Tree State for PORT 7 .** 00 = Disable state 01 = Standby state (blocking) 10 = Unstable state (listing/learning) 11 = Normal state (forwarding or no spanning tree)	00
13:12	SPT_STA_PORT6	R	**Spanning Tree State for PORT 6.** 00 = Disable state 01 = Standby state (blocking) 10 = Unstable state (listing/learning) 11 = Normal state (forwarding or no spanning tree)	00
11:10	SPT_STA_PORT5	R	**Spanning Tree State for PORT 5.** 00 = Disable state 01 = Standby state (blocking) 10 = Unstable state (listing/learning) 11 = Normal state (forwarding or no spanning tree)	00
9:8	SPT_STA_PORT4	R/W	**Spanning Tree State for PORT 4.** 00 = Disable state 01 = Standby state (blocking) 10 = Unstable state (listing/learning) 11 = Normal state (forwarding or no spanning tree)	00
7:6	SPT_STA_PORT3	R/W	**Spanning Tree State for PORT 3.** 00 = Disable state 01 = Standby state (blocking) 10 = Unstable state (listing/learning) 11 = Normal state (forwarding or no spanning tree)	00
5:4	SPT_STA_PORT2	R/W	**Spanning Tree State for PORT 2.** 00 = Disable state 01 = Standby state (blocking) 10 = Unstable state (listing/learning) 11 = Normal state (forwarding or no spanning tree)	00
3:2	SPT_STA_PORT1	R/W	**Spanning Tree State for PORT 1.** 00 = Disable state 01 = Standby state (blocking) 10 = Unstable state (listing/learning) 11 = Normal state (forwarding or no spanning tree)	00

Table 189: MST Table Register (Page 43h, Address 16–143d, 10–8Fh) (Cont.)

Bit	Name	R/W	Description	Default
1:0	SPT_STA_PORT0	R/WO	**Spanning Tree State for PORT 0.** 00 = Disable state 01 = Standby state (blocking) 10 = Unstable state (listing/learning) 11 = Normal state (forwarding or no spanning tree)	00

SPI Registers

Table 190: SPI Registers (Maps Globally to All Pages)

Addr	Bits	Description
F0h	8	SPI Data I/O 0
F1h	8	SPI Data I/O 1
F2h	8	SPI Data I/O 2
F3h	8	SPI Data I/O 3
F4h	8	SPI Data I/O 4
F5h	8	SPI Data I/O 5
F6h	8	SPI Data I/O 6
F7h	8	SPI Data I/O 7
F8h–FDh	Reserved	
FEh	8	SPI Status register

SPI Data I/O n Registers

Table 191: SPI Data I/O n Registers (Maps Globally to All Pages, Addresses 240d–247d, F0h–F7h)

Bit	Name	R/W	Description	Default
8	SPI Data I/O (n = 0-7)	R/W	SPI read/write data	–

SPI Status Register

Table 192: SPI Status Register (Maps Globally to All Pages: Address 254d, FEh)

Bit	Name	R/W	Description	Default
7	SPIF	RO	SPI read/write complete flag	–
6:1	RESERVED	RO	Reserved	
5	RACK	RO (SC)	SPI read data ready acknowledgement (self-clearing)	–

Table 192: SPI Status Register (Maps Globally to All Pages: Address 254d, FEh)

Bit	Name	R/W	Description	Default
4:2	RESERVED	RO	Reserved	
1	RXRDY	RO	SMP Rx ready flag—should check every 8 bytes	–
0	TXRDY	RO	SMP Tx ready flag—should check every 8 bytes	–

Page Register

Table 193: Page Register (Maps to All Registers, Address FFh)

Bit	Name	R/W	Description	Default
7:0	PAGE_REG	R/W	Binary value determines the value of the accessed register page.	0

Section 5: Timing Characteristics

Reset and Clock Timing

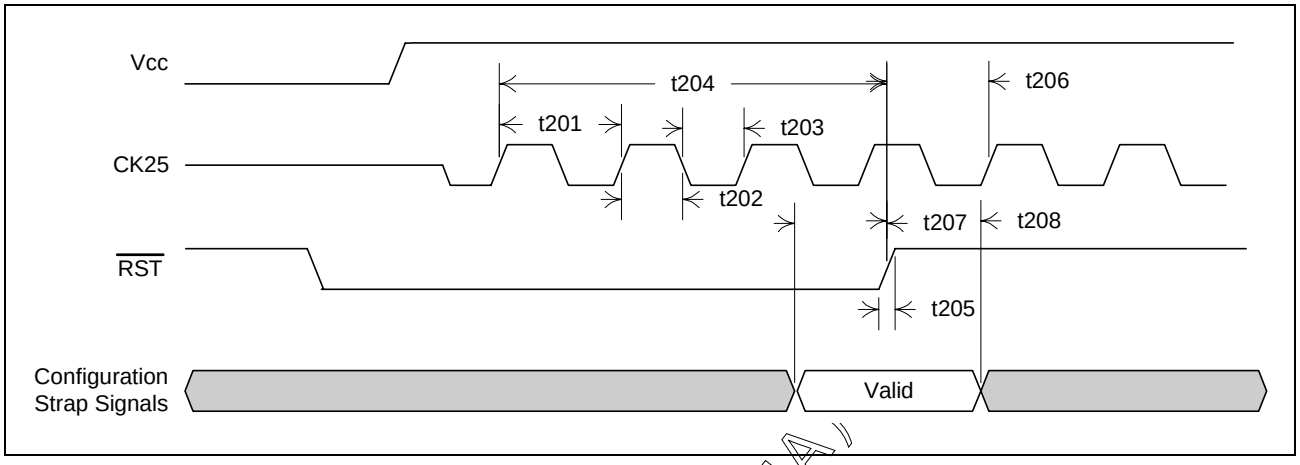


Figure 34: Reset and Clock Timing

Table 194: Reset and Clock Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t201	XTALI/CK25 period	39.998 ns	40 ns	40.002 ns
t202	XTALI/CK25 high time	18 ns	–	22 ns
t203	XTALI/CK25 low time	18 ns	–	22 ns
t204	$\overline{\text{RST}}$ low pulse duration	400 ns	50 ms	–
t207	Configuration valid setup to $\overline{\text{RST}}$ rising	100 ns	–	–
t208	Configuration valid hold from $\overline{\text{RST}}$ rising	–	–	0 ns

Serial LED Timing

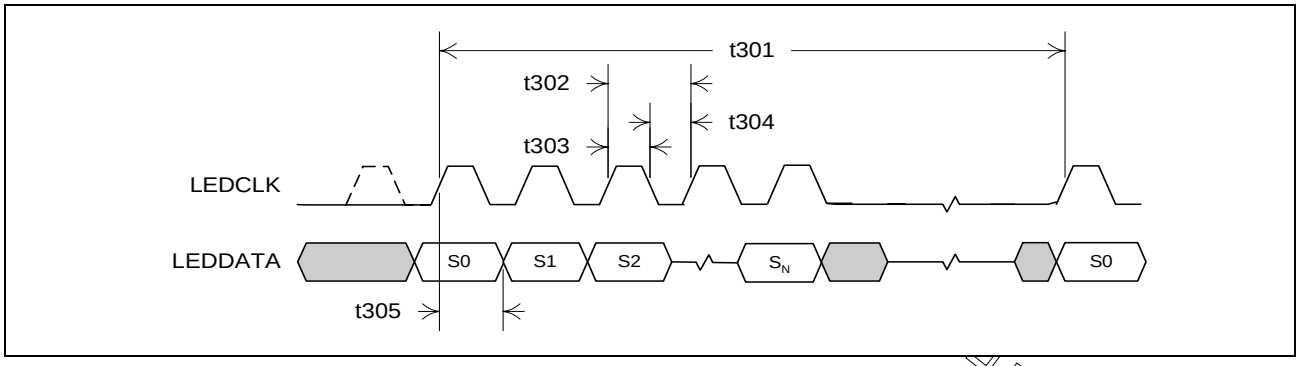


Figure 35: Serial LED Timing

Table 195: Serial LED Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t301	LED UPDATE CYCLE PERIOD	–	42 ms	–
t302	LEDCLK PERIOD	–	640 ns	–
t303	LEDCLK high pulse width	310 ns	–	330 ns
t304	LEDCLK low pulse width	310 ns	–	330 ns
t305	LEDCLK to LEDDATA output time	270 ns	–	340 ns

MII Input Timings

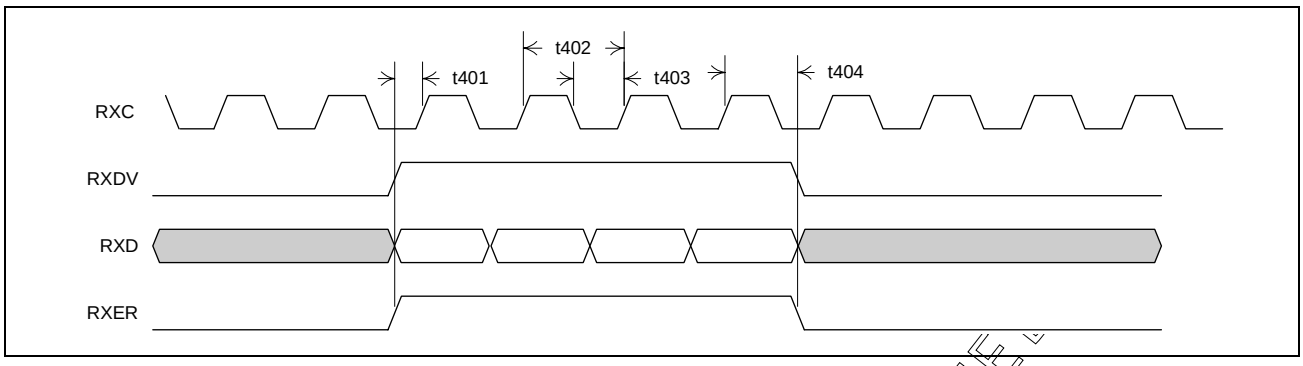


Figure 36: MII Input Timings

Table 196: MII Input Timings

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t401	RXDV, RXD, RXER, to RXC rising setup time	5 ns	–	–
t402	RXC clock period (10BASE-T mode)	–	400 ns	–
	RXC clock period (100BASE-T mode)	–	40 ns	–
t403	RXC high/low time (10BASE-T mode)	160 ns	–	240 ns
	RXC high/low time (100BASE-T mode)	14 ns	–	26 ns
t404	RXDV, RXD, RXER, to RXC rising hold time	5 ns	–	–

RvMII Input Timings

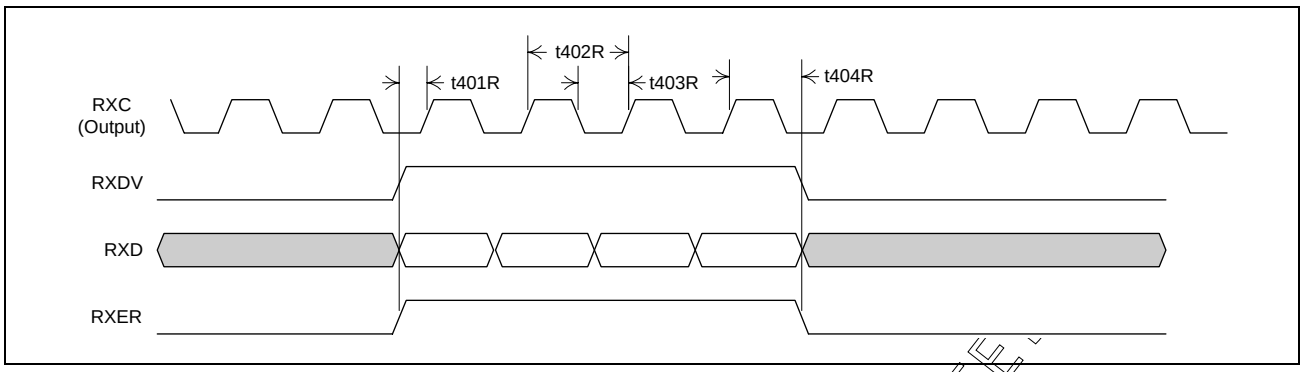


Figure 37: RvMII Input Timings

Table 197: RvMII Input Timings

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t401R	RXDV, RXD, RXER, to RXC rising setup time	10 ns	–	–
t402R	RXC clock period (100BASE-T mode only)	–	40 ns	–
t403R	RXC high/low time (100BASE-T mode only)	14 ns	–	26 ns
t404R	RXDV, RXD, RXER, to RXC rising hold time	0 ns	–	–

MII Output Timings

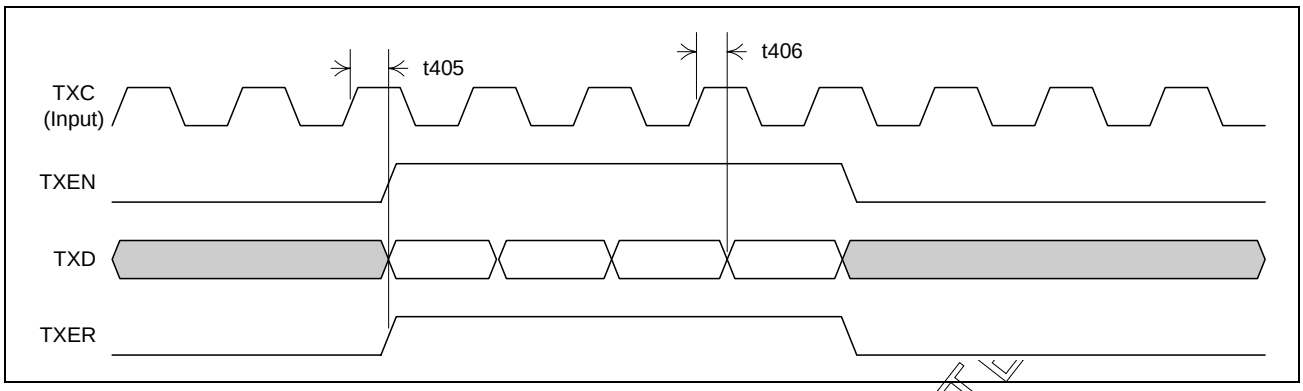


Figure 38: MII Output Timings

Table 198: MII Output Timings

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t405	TXC High to TXEN, TXD, TXER Valid	–	–	22 ns
t406	TXC High to TXEN, TXD, TXER Invalid	3 ns	–	–

RvMII Output Timings

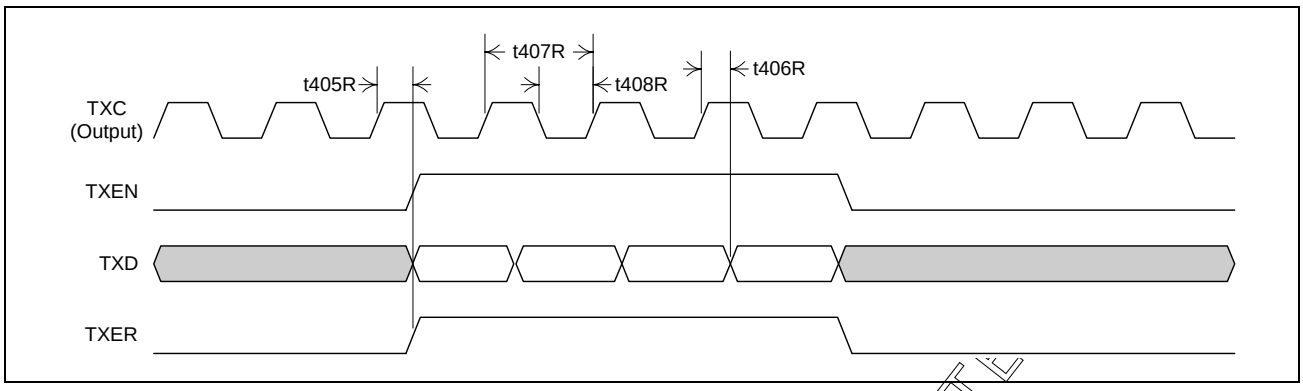


Figure 39: RvMII Output Timings

Table 199: RvMII Output Timings

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t405R	TXC High to TXEN, TXD, TXER valid	–	–	29 ns
t406R	TXC High to TXEN, TXD, TXER invalid	11 ns	–	–
t407R	TXC clock period	–	40 ns	–
t408R	TXC high/low time	14 ns	–	26 ns

SPI Timings

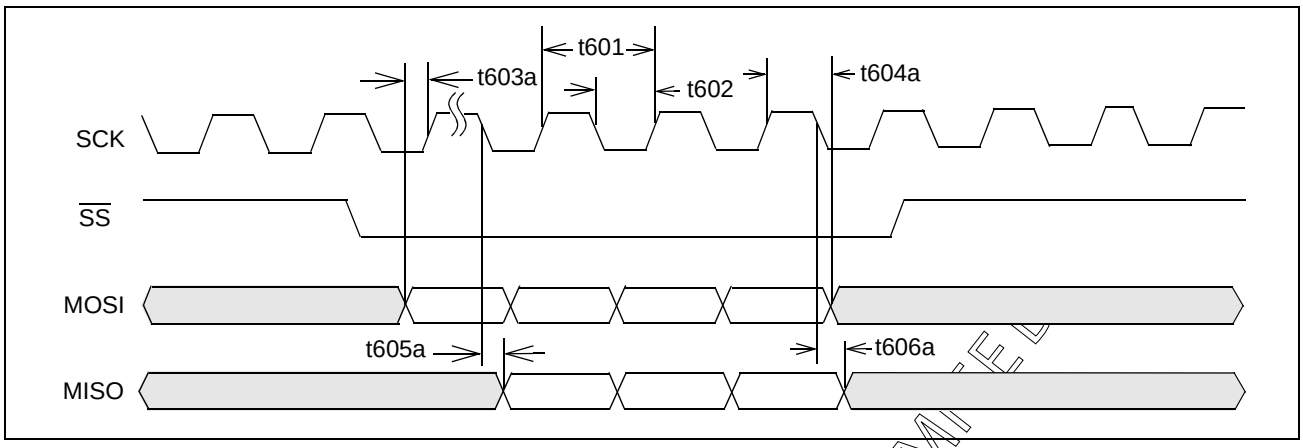


Figure 40: SPI Timings, SS Asserted During SCK High

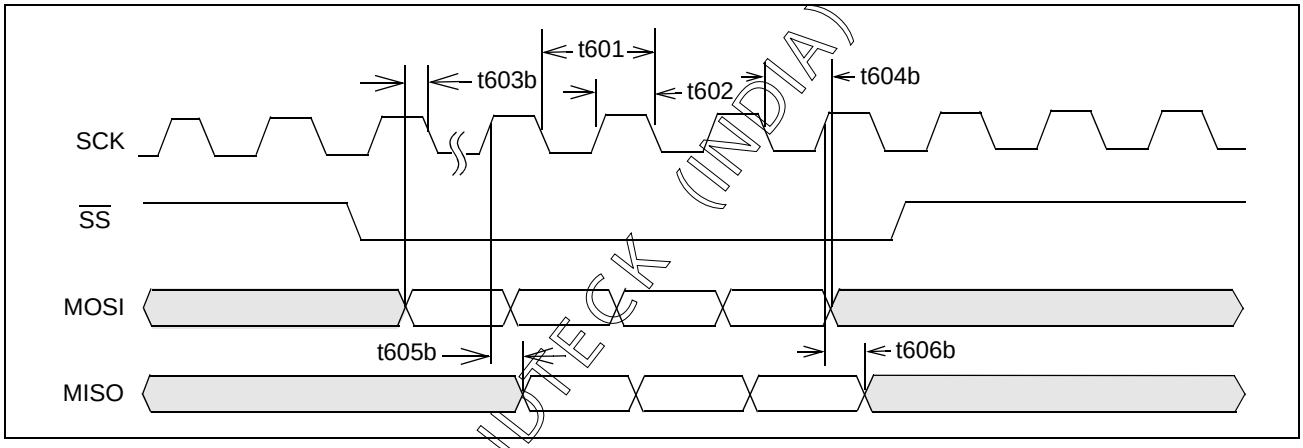


Figure 41: SPI Timings, SS Asserted During SCK Low

Table 200: SPI Timings

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t601	SCK clock period	–	500 ns	–
t602	SCK high/low time	200 ns	–	300 ns
t603a, t603b	MOSI to SCK setup time	5 ns	–	–
t604a, t604b	MOSI to SCK hold time	12 ns	–	–
t605a, t605b	SCK to MISO valid	–	–	25 ns
t606a, t606b	SCK to MISO invalid	0 ns	–	–

Note: The BCM5338M behaves only as a slave device. The $\overline{SS}$ is asynchronous. If $\overline{SS}$ is asserted during SCK high, then the BCM5338M samples data on the rising edge of SCK and references the falling edge to output data. Otherwise, the BCM5338M samples data on the falling edge and outputs data on the rising edge of SCK.

EEPROM Timing

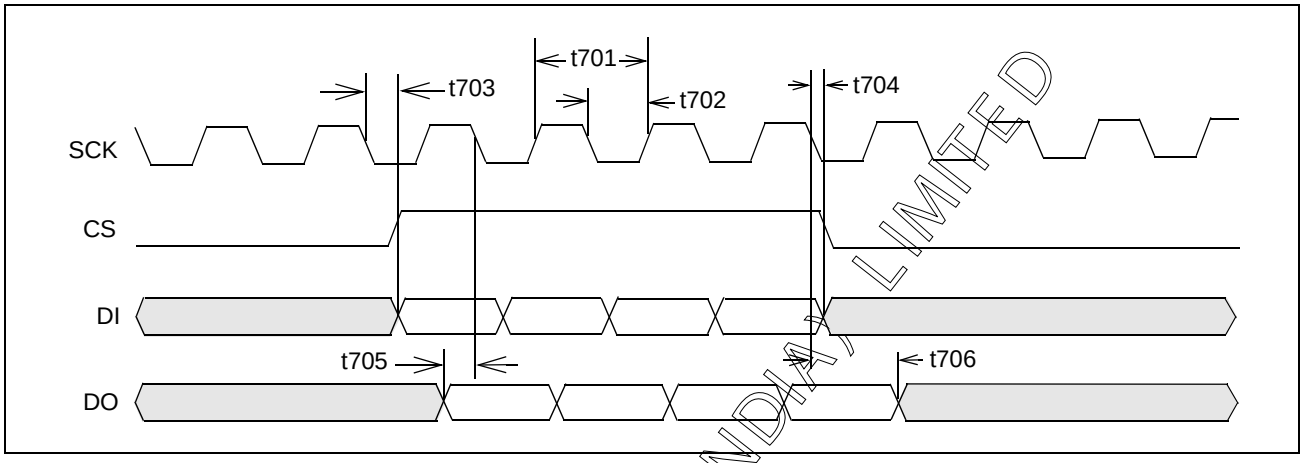


Figure 42: EEPROM Timing

Table 201: EEPROM Timing

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t701	SCK clock frequency	–	100 kHz	–
t702	SCK high/low time	–	5 us	–
t703	SCK low to CS, DI valid	–	–	500 ns
t704	SCK low to CS, DI invalid	500 ns	–	–
t705	DO to SCK falling setup time	200 ns	–	–
t706	DO to SCK falling hold time	200 ns	–	–

Management Data Interface (Slave Mode)

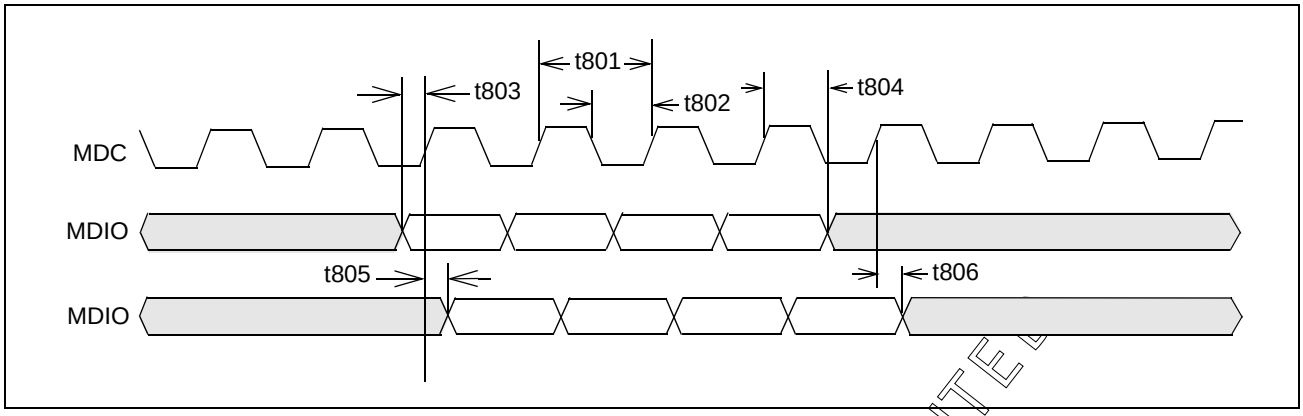


Figure 43: Management Data Interface (Slave Mode)

Table 202: Management Data Interface (Slave Mode)

Parameter	*Description*	*Minimum*	*Typical*	*Maximum*
t801	MDC clock period	–	80 ns	–
t802	MDC high/low time	30 ns	–	50 ns
t803	MDIO to MDC rising setup time	5 ns	–	–
t804	MDIO to MDC rising hold time	5 ns	–	–
t805	MDC rising to MDIO valid	–	–	50 ns
t806	MDC rising to MDIO invalid	10 ns	–	–

Section 6: Electrical Characteristics

Table 203: Absolute Maximum Ratings

Sym	Parameter	Minimum	Maximum	Units
V_{DD}	Supply voltage: VDDC, VDDA, VDDPLL	GND – 0.3	1.98	V
V_I	Supply voltage: VDDP, VDDBIAS, VDDXTAL, input voltage	GND – 0.3	3.60	V
I_I	Input current	–	±10	mA
T_{STG}	Storage temperature	–40	+125	°C
V_{ESD}	Electrostatic discharge	–	1000	V

Note: These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect long-term reliability of the device.

Table 204: Recommended Operating Conditions

Sym	Parameter	Pins	Minimum	Maximum	Units
VDD	Supply voltage	VDDC, VDDA, VDDPLL	1.71	1.89	V
		VDDXTAL	3.135	3.465	V
		VDDP,VDDBIAS	3.135	3.465	V
V_{IH}	High-level input voltage	All Digital Inputs	2.0	–	V
V_{IL}	Low-level input voltage	All Digital Inputs	–	0.8	V
			–	–	
V_{IDIFF}	Differential input voltage	RD± {1:5}	150	–	mV
R_{DAC}	DAC current-setting resistance	RDAC	1.30	1.30	kΩ
T_A	Ambient operating temperature		0	70	°C

Table 205: Electrical Characteristics

Sym	Parameter	Pins	Conditions	Minimum	Typical	Maximum	Units
$I_{DD1.8}$	Total supply current	VDDC, VDDPLL, VDDA	100BASE-TX	–	–	599mA	mA
$I_{DD3.3}$	Total supply for internal current	VDDP, VDDBIAS, VDDXTAL	100BASE-TX	–	–	401mA	mA
	Total supply for front-end current per port	Transformer center taps, termination resistors	100BASE-TX or 10BASE-T	75% –	–	40	mA

Table 205: Electrical Characteristics (Cont.)

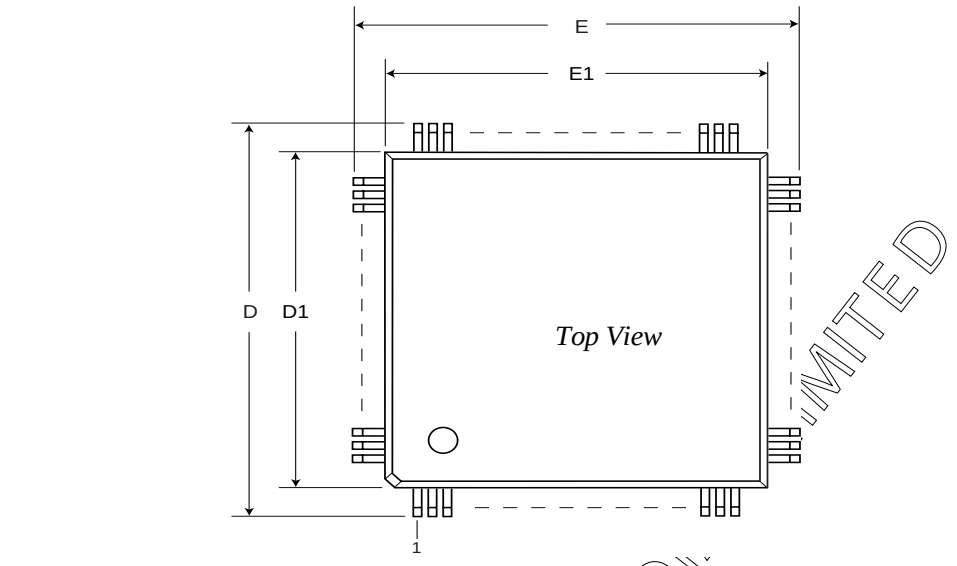
Sym	Parameter	Pins	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	High-level output voltage	$\overline{\text{LEDA}}$, $\overline{\text{LEDB}}$, $\overline{\text{LEDC}}$, LEDDATA, LEDCLK, TXC, TXD, TXEN, TXER, RXC, RXD[0], RXDV, COL, MDIO, MDC, ERDYO, MISO, SCK, CS, DI, TDO	I_{OH} = −8 mA	2.4	–	–	V
		EDO, EVALIDO, ESOFO, TDM_DATA_OUT, TDM_FRM_OUT, QOS_FC_DIS	I_{OH} = −10 mA	2.4	–	–	–
		ECLKO	I_{OH} = −16 mA	2.4	–	–	–
		TD± {1:8}	driving loaded magnetics module	–	–	VDD + 1.5	V
V_{OL}	Low-level output voltage	$\overline{\text{LEDA}}$, $\overline{\text{LEDB}}$, $\overline{\text{LEDC}}$, LEDDATA, LEDCLK, TXC, TXD, TXEN, TXER, RXC, RXD[0], RXDV, COL, MDIO, MDC, ERDYO, MISO, SCK, CS, DI, TDO	I_{OL} =8 mA	–	–	0.4	V
		EDO, EVALIDO, ESOFO, TDM_DATA_OUT, TDM_FRM_OUT, QOS_FC_DIS	I_{OL} =10 mA	–	–	0.4	–
		ECLKO	I_{OL} =16 mA	–	–	0.4	–
		TD± {1:8}	driving loaded magnetics module	VDD − 1.5			V
I_I	Input current	Digital inputs with pullup resistors	V_I = VDDP	–	–	+100	µA
			V_I = GND	–	–	−200	µA
		Digital inputs with pulldown resistors	V_I = VDDP	–	–	+200	µA
			V_I = GND	–	–	−10	µA
		All other digital inputs	GND ≤ V_I ≤ VDDP	–	–	±100	µA
I_{OZ}	High-impedance output current	All three-state outputs	GND ≤ V_O ≤ VDDP	–	–	±10	µA
		All open-drain outputs	V_O = VDDP	–	–	+10	µA
V_{BIAS}	Bias voltage	RDAC	–	1.18	–	1.30	V

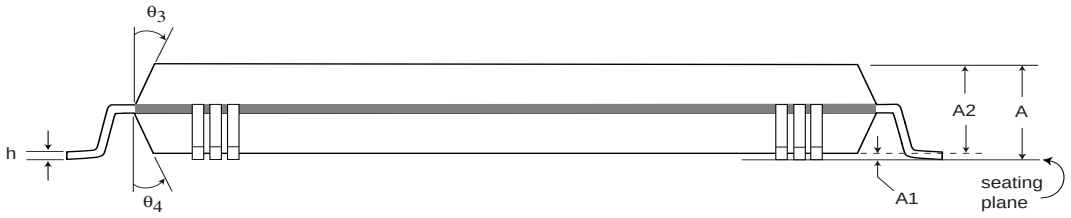
Section 7: Thermal Characteristics

Table 206: Thermal Characteristics

Airflow (LFPM)	*0*	*100*	*200*	*400*	*600*
Theta-JA (^{O}C/W)	17	13.6	12.7	11.5	10.7
Theta-JB (^{O}C/W)	7	–	–	–	–
Theta-JC (^{O}C/W)	4.6	–	–	–	–
Max Junction Temperature T_{JA}	125^{O}C	–	–	–	–

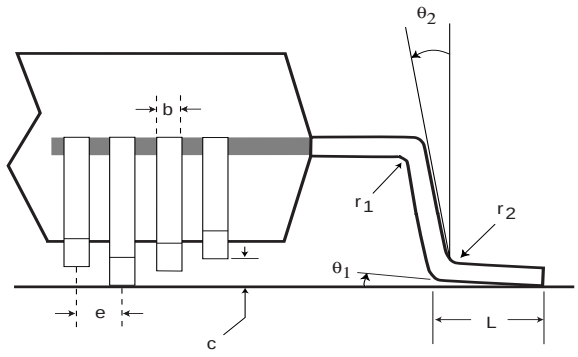
Section 8: Mechanical Information





Symbol	Millimeter		
	Min	Nom	Max
A	—	—	4.10
A1	0.25	0.37	0.50
A2	3.39	3.49	3.59
D	30.35	30.60	30.85
D1	27.90	28.00	28.10
E	30.35	30.60	30.85
E1	27.90	28.00	28.10
L	0.30	0.60	0.75
b	0.15	0.22	0.30
h	0.13		0.23
e	0.50 BSC		
c	—	0.08	0.102
r_1	—	0.20	—
r_2	—	0.30	—
θ_1	0°	—	7°
θ_2	2°	6°	10°
θ_3	—	10°	—
θ_4	—	10°	—

208-pin detail



Notes:

1. Drawings on this page are not to scale
2. All dimensions are in millimeters except where noted
3. Foot length "L" is measured at gage plane, 0.25mm above the seating plane
4. Seating plane is defined by three lowest lead tips

Figure 44: 208-PQFP Package Outline Drawing

Section 9: Ordering Information

Table 207: Ordering Information

Part Number	*Package*	*Ambient Temperature*
BCM5338MKQM	208-MQFP	0°C to 70°C
BCM5338MKQMG	208-MQFP (RoHS-compliant)	0°C to 70°C
BCMI5338MKQMG	208-MQFP (RoHS-compliant)	0°C to 70°C
BCM5338MIQM	208-MQFP	–40°C to 85°C
BCM5338MIQMG	208-MQFP (RoHS-compliant)	–40°C to 85°C
BCMI5338MIQMG	208-MQFP (RoHS-compliant)	–40°C to 85°C

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