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REVISION HISTORY

REV	DATE	AUTHOR	CHANGES
1.0	17 JULY 2011	Akhilesh	
1.1	20 JULY 2011	Akhilesh	R404 and net CLK_CPLD_66M added U53 changed to 25MHz part U3 Address connections updated R405 and R406 added GND connection from J6-C1 removed
2.0	14 SEP 2011	Akhilesh	R344 made DNI U40 replaced with MAX16052. R408 added R399 moved between D25.2 and Q11.3. Q11.2 connected to GND Net USB_STP connected to U39.2. R409 added at U39.18 R147, R148, R149 and R150 replaced with 0402 package C12 and C13 made DNI U24.3 connected to GND R380 moved between D23.2 and Q10.3. Q10.2 connected to GND Nets LED_TSEC1_LINK_ACT and LED_TSEC1_SPD100 swapped
	26 SEP 2011	AJM	Added inverter for RTS signals: U55 and U56; Added RTS_EN# to CTRL INV from CPLD; Removed net DEBUG_LED2 and associated LED; Added GPIO_RTS_EN to CPLD

SHEETS

1. MAIN
2. BLOCK DIAGRAM 1
3. BLOCK DIAGRAM 2
4. P1021_DDR3 MEMORY
5. P1021_FLASH INTERFACE
6. P1021_SYSTEM CONTROL
7. ETHERNET_EEC
8. ETHERNET_IES_ECAT
9. GIGABIT ETHERNET
10. I2C_SPI_SD-CARD
11. ET1100
12. USB_SERIAL
13. P1021_POWER
14. POWER ON STRAPPING - 1
15. POWER ON STRAPPING - 2
16. CPLD_HOT SWAP_LED
17. POWER SUPPLY
18. BACKPLANE INTERFACE

APPROVALS	DATE	COMPRESSOR CONTROLS CORPORATION 4725 121st Street - Des Moines, Iowa 50323			
DRAWN AKHILESH JAISWAL	14-SEP-2011				
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ENGINEER		SIZE C	DWG. NO. 18-600400-001	SHEET 1	PROD REV. 2.0
			FILE APP CARD SCHEMATIC	SCALE	

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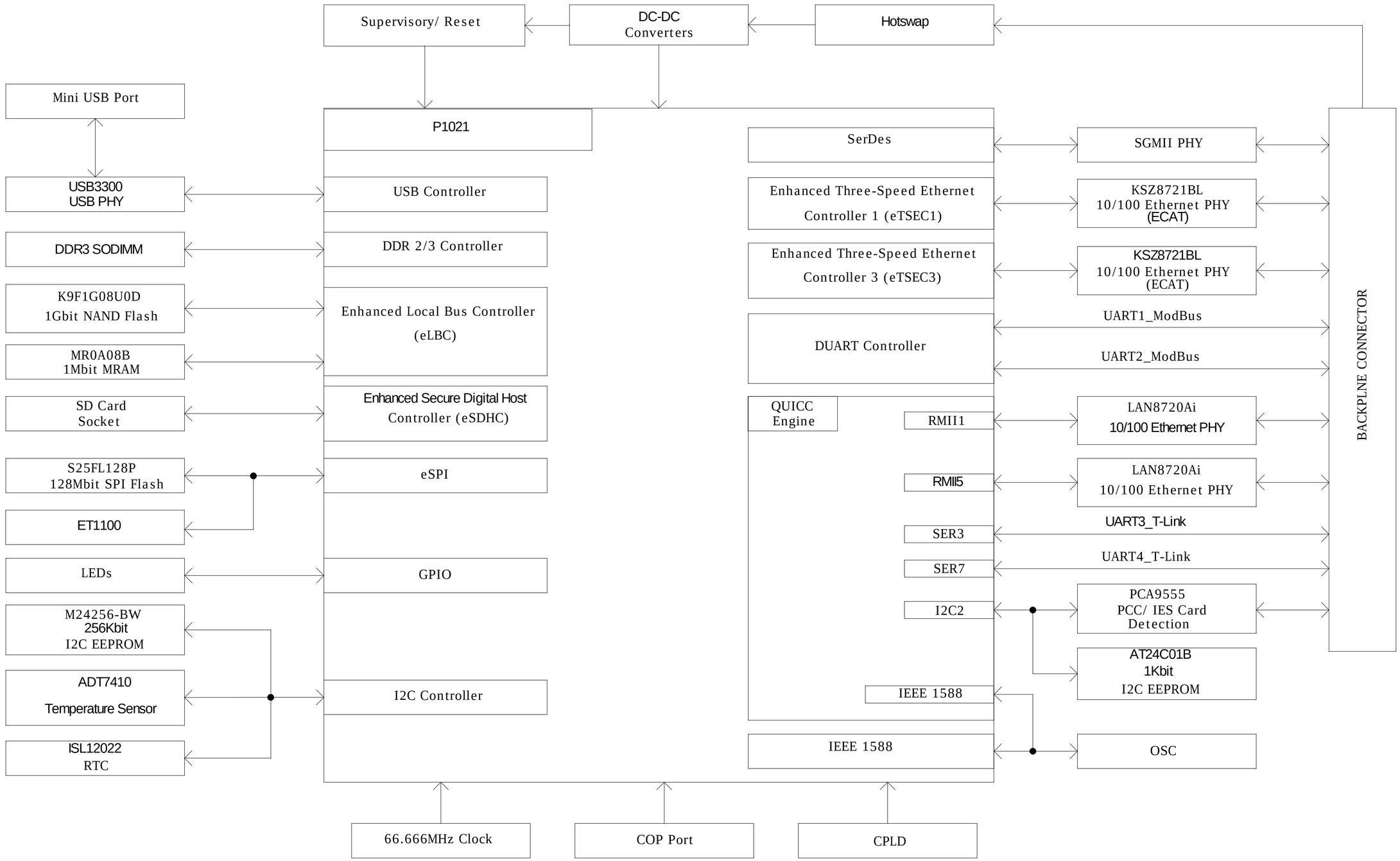
BLOCK DIAGRAM



2.0

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P1021_DDR3

U1-A

AC5	NC75	MDQ00	AJ8	MDQ0
AC6	NC73	MDQ01	AH8	MDQ1
F5	NC74	MDQ02	AH5	MDQ2
F6	NC76	MDQ03	AJ4	MDQ3
G4	NC22	MDQ04	AJ9	MDQ4
G3	NC23	MDQ05	AH9	MDQ5
E2	NC24	MDQ06	AH6	MDQ6
E4	NC25	MDQ07	AJ5	MDQ7
H5	NC26	MDQS00	AJ6	MDQS0
H4	NC27	MDQS_B00	AJ7	MDQS0#
F2	NC28	MDM00	AH7	MDM0
E1	NC29			
C1	NC30	MDQ08	AF8	MDQ8
C3	NC31	MDQ09	AE8	MDQ9
B4	NC32	MDQ10	AF5	MDQ10
A4	NC33	MDQ11	AG4	MDQ11
D1	NC34	MDQ12	AG9	MDQ12
D2	NC35	MDQ13	AF9	MDQ13
B3	NC36	MDQ14	AE6	MDQ14
A3	NC37	MDQ15	AE5	MDQ15
C5	NC38	MDQS01	AF6	MDQS1
E6	NC39	MDQS_B01	AF7	MDQS1#
D9	NC40	MDM01	AE7	MDM1
E9	NC41			
C4	NC42	MDQ16	AH3	MDQ16
E5	NC43	MDQ17	AH2	MDQ17
E8	NC44	MDQ18	AE1	MDQ18
D8	NC45	MDQ19	AE2	MDQ19
A6	NC46	MDQ20	AH4	MDQ20
B7	NC47	MDQ21	AJ3	MDQ21
B10	NC48	MDQ22	AF2	MDQ22
A11	NC49	MDQ23	AF1	MDQ23
A5	NC50	MDQS02	AG2	MDQS2
B6	NC51	MDQS_B02	AG1	MDQS2#
B9	NC52	MDM02	AH1	MDM2
A10	NC53			
G1	NC57	MDQ24	AD4	MDQ24
C2	NC58	MDQ25	AC4	MDQ25
F8	NC59	MDQ26	Y5	MDQ26
A7	NC60	MDQ27	W5	MDQ27
F3	NC61	MDQ28	AF3	MDQ28
B2	NC62	MDQ29	AE4	MDQ29
D7	NC63	MDQ30	AB5	MDQ30
A9	NC64	MDQ31	Y4	MDQ31
F4	NC65	MDQS03	AB3	MDQS3
B1	NC66	MDQS_B03	AB4	MDQS3#
D6	NC67	MDM03	AC1	MDM3
A8	NC68			
J1	NC69	MECC00	AD2	MECC0
G2	NC70	MECC01	AC2	MECC1
U6	NC71	MECC02	W1	MECC2
V2	NC72	MECC03	V3	MECC3
J4	NC77	MECC04	AB2	MECC4
F1	NC78	MECC05	AD1	MECC5
Y15	NC3	MECC06	Y1	MECC6
Y16	NC4	MECC07	V6	MECC7
AE10	NC5	MDQS08	AA1	MDQS8
AF10	NC6	MDQS_B08	AB1	MDQS8#
E14	NC9	MDM08	AA4	MDM8
E13	NC10			
W6	NC15	MA00	L6	MA0
Y14	NC2	MA01	M2	MA1
AE26	NC82	MA02	M1	MA2
AF26	NC83	MA03	M5	MA3
AC29	NC84	MA04	N1	MA4
AA25	NC85	MA05	P1	MA5
AA26	NC87	MA06	N4	MA6
AA24	NC88	MA07	P3	MA7
AG28	NC89	MA08	P2	MA8
AD27	NC90	MA09	R1	MA9
AB26	NC91	MA10	K6	MA10
AC26	NC92	MA11	R4	MA11
AD26	NC93	MA12	T5	MA12
AB27	NC94	MA13	J5	MA13
AD28	NC95	MA14	T3	MA14
AF29	NC96	MA15	U4	MA15
AF28	NC97			
AD29	NC98	MBA00	K5	MBA0
AE28	NC99	MBA01	L5	MBA1
AC29	NC100	MBA02	T4	MBA2
Y24	NC86			
		MCS_B00	J2	MCS0#
		MCS_B01	J6	MCS1#
		MCKE00	U5	MCKE0
		MCKE01	V1	MCKE1
		MODT00	H1	MODT0
		MODT01	H6	MODT1
		MWE_B	K2	MWE#
		MRAS_B	K1	MRAS#
		MCAS_B	J3	MCAS#
		MCK00	U2	
		MCK_B00	U1	
		MCK01	AD8	
		MCK_B01	AD7	
		MCK02	D4	MCK0
		MCK_B02	D5	MCK0#
		MCK03	T2	MCK1
		MCK_B03	T1	MCK1#
		MDIC00	C10	
		MDIC01	F10	
		MAPAR_OUT	R5	NC
		MAPAR_ERR_B	N5	
		MVREF	R6	

P1021

R7 100E (MCK00 / MCK_B00)
R6 100E (MCK01 / MCK_B01)
R2 40.2E 1% (MDIC1)
R1 10K
VREF_DDR3
R3 40.2E 1%
GVDD
C1 0.1uF
C2 0.01uF
GND

DDR3 SODIMM

VREF_DDR3
C3 0.1uF
C4 0.01uF
GND

J1 — 2013310-1

1	VREFDQ		2	GND27	
3	GND1		4	DQ4	MDQ4
5	DQ0	MDQ0	6	DQ5	MDQ5
7	DQ1	MDQ1	8	GND28	
9	GND2		10	DQS0	MDQS0#
11	DM0	MDM0	12	DQS0	MDQS0
13	GND3		14	GND29	
15	DQ2	MDQ2	16	DQ6	MDQ6
17	DQ3	MDQ3	18	DQ7	MDQ7
19	GND4		20	GND30	
21	DQ8	MDQ8	22	DQ12	MDQ12
23	DQ9	MDQ9	24	DQ13	MDQ13
25	GND5		26	GND31	
27	DQS1	MDQS1#	28	DM1	MDM1
29	DQS1	MDQS1	30	RESET	
31	GND6		32	GND32	
33	DQ10	MDQ10	34	DQ14	MDQ14
35	DQ11	MDQ11	36	DQ15	MDQ15
37	GND7		38	GND33	
39	DQ16	MDQ16	40	DQ20	MDQ20
41	DQ17	MDQ17	42	DQ21	MDQ21
43	GND8		44	GND34	
45	DQS2	MDQS2#	46	DM2	MDM2
47	DQS2	MDQS2	48	GND35	
49	GND9		50	DQ22	MDQ22
51	DQ18	MDQ18	52	DQ23	MDQ23
53	DQ19	MDQ19	54	GND36	
55	GND10		56	DQ28	MDQ28
57	DQ24	MDQ24	58	DQ29	MDQ29
59	DQ25	MDQ25	60	GND37	
61	GND11		62	DQS3	MDQS3#
63	DM3	MDM3	64	DQS3	MDQS3
65	GND12		66	GND38	
67	DQ26	MDQ26	68	DQ30	MDQ30
69	DQ27	MDQ27	70	DQ31	MDQ31
71	GND13		72	GND39	
73	CKE0	MCKE0	74	NC/CKE1	MCKE1
75	VDD0		76	VDD9	
77	NC1		78	NC/A15	MA15
79	BA2	MBA2	80	NC/A14	MA14
81	VDD1		82	VDD10	
83	A12	MA12	84	A11	MA11
85	A9	MA9	86	A7	MA7
87	VDD2		88	VDD11	
89	A8	MA8	90	A6	MA6
91	A5	MA5	92	A4	MA4
93	VDD3		94	VDD12	
95	A3	MA3	96	A2	MA2
97	A1	MA1	98	A0	MA0
99	VDD4		100	VDD13	
101	CK0	MCK0	102	CK1	MCK1
103	CK0	MCK0#	104	CK1	MCK1#
105	VDD5		106	VDD14	
107	A10	MA10	108	BA1	MBA1
109	BA0	MBA0	110	RAS	MRAS#
111	VDD6		112	VDD15	
113	WE	MWE#	114	CS0	MCS0#
115	CAS	MCAS#	116	ODT0	MODT0
117	VDD7		118	VDD16	
119	NC/A13	MA13	120	NC/ODT1	MODT1
121	NC/CS1	MCS1#	122	NC2	
123	VDD8		124	VDD17	
125	NC/TEST		126	VREFCA	
127	GND14		128	GND40	
129	DQ32	MECC0	130	DQ36	MECC4
131	DQ33	MECC1	132	DQ37	MECC5
133	GND15		134	GND41	
135	DQS4	MDQS8#	136	DM4	MDM8
137	DQS4	MDQS8	138	GND42	
139	GND16		140	DQ38	MECC6
141	DQ34	MECC2	142	DQ39	MECC7
143	DQ35	MECC3	144	GND43	
145	GND17		146	DQ44	
147	DQ40		148	DQ45	
149	DQ41		150	GND44	
151	GND18		152	DQS5	
153	DM5		154	DQS5	
155	GND19		156	GND45	
157	DQ42		158	DQ46	
159	DQ43		160	DQ47	
161	GND20		162	GND46	
163	DQ48		164	DQ52	
165	DQ49		166	DQ53	
167	GND21		168	GND47	
169	DQS6		170	DM6	
171	DQS6		172	GND48	
173	GND22		174	DQ54	
175	DQ50		176	DQ55	
177	DQ51		178	GND49	
179	GND23		180	DQ60	
181	DQ56		182	DQ61	
183	DQ57		184	GND50	
185	GND24		186	DQS7	
187	DM7		188	DQS7	
189	GND25		190	GND51	
191	DQ58		192	DQ62	
193	DQ59		194	DQ63	
195	GND26		196	GND52	
197	SA0		198	EVENT	IRQ0_DDR3# [6,10]
199	VDDSPD		200	SDA	I2C1_SDA [10]
201	SA1		202	SCL	I2C1_SCL [10]
203	VTT1		204	VTT2	

BYTE0: DQ0–DQ7, DM0, DQS0, DQS0#
BYTE1: DQ8–DQ15, DM1, DQS1, DQS1#
BYTE2: DQ16–DQ23, DM2, DQS2, DQS2#
BYTE3: DQ24–DQ31, DM3, DQS3, DQS3#
BYTE4: DQ32–DQ39, DM4, DQS4, DQS4#
BYTE5: DQ40–DQ47, DM5, DQS5, DQS5#
BYTE6: DQ48–DQ55, DM6, DQS6, DQS6#
BYTE7: DQ56–DQ63, DM7, DQS7, DQS7#
ADDRESS & CNTR: CKE0, CKE1, BA2, BA1, BA0, A12, A11, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0, CK0, CK0#, CK1, CK1#, WE, CAS, RAS, CS0, ODT0, ODT1, A10, A15, A14, A13, BA2, RESET, EVENT, SA0, SA1, SCL, SDA

GVDD
R8 4.7K
Q1 2N7002PW
DDR3_RESET [16]
R9 100K
GND

C12 4.7pF DNI (MCK0 / MCK0#)
C13 4.7pF DNI (MCK1 / MCK1#)

VREF_DDR3
C14 0.1uF
C15 0.01uF
GND

SPD I2C ADDRESS: 51H

3.3V
R4 10K
C9 0.1uF
C8 10uF
C7 0.01uF
C6 0.1uF
R5 0E
VTT_DDR3
C5 0.1uF
C10 0.01uF
C11 10uF

DDR3 SODIMM DECAP

GVDD
C347 10uF, C366 10uF, C367 10uF, C368 10uF
C348–C356 0.1uF
C357–C365 0.01uF
GND

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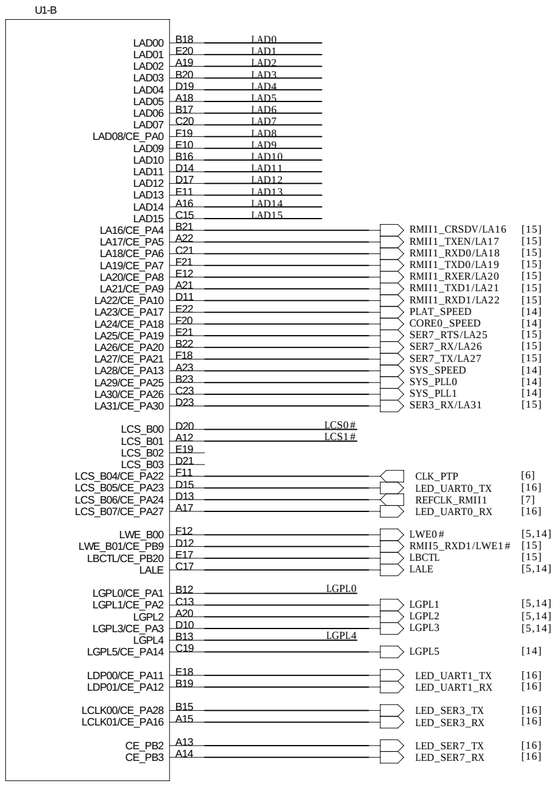
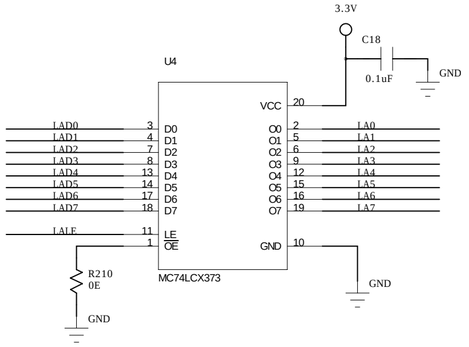
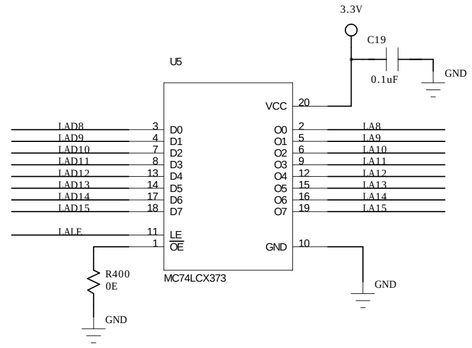
P1021_LOCAL BUS



LOCAL BUS LATCH





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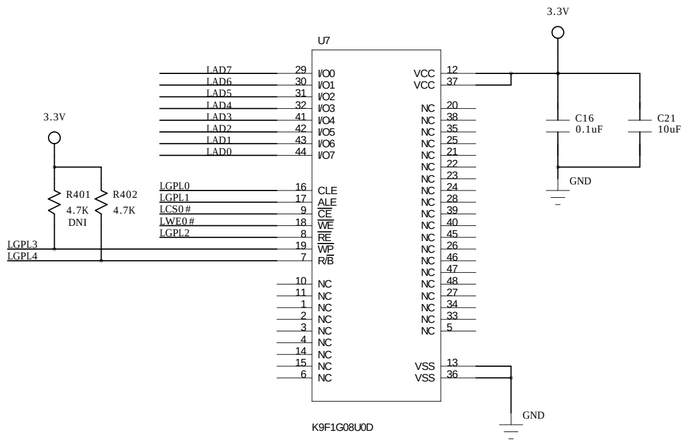
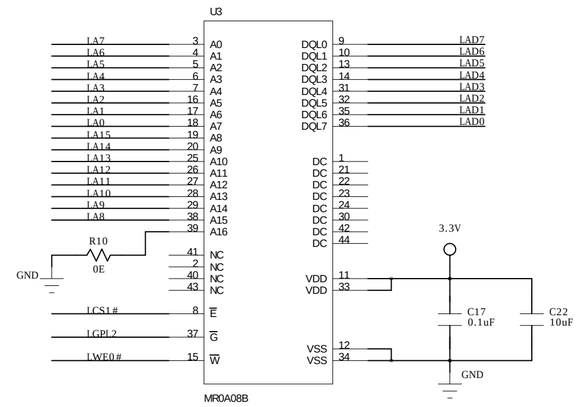


MRAM : 1MBIT



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ENGINEER		

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C	18-600400-001	5	2.0
	FILE: APP CARD SCHEMATIC	SCALE	

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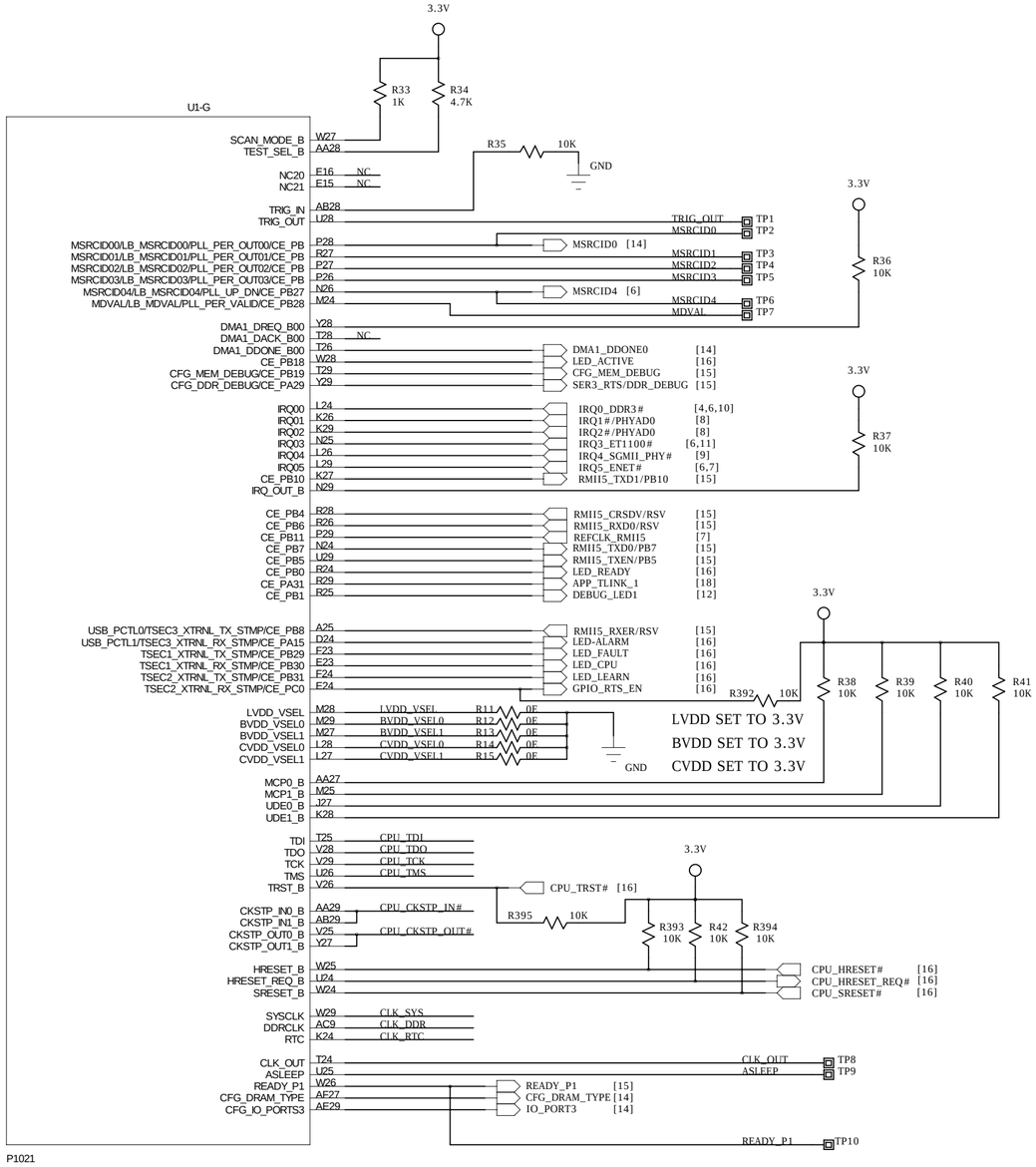
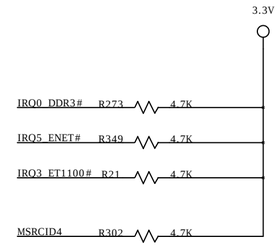
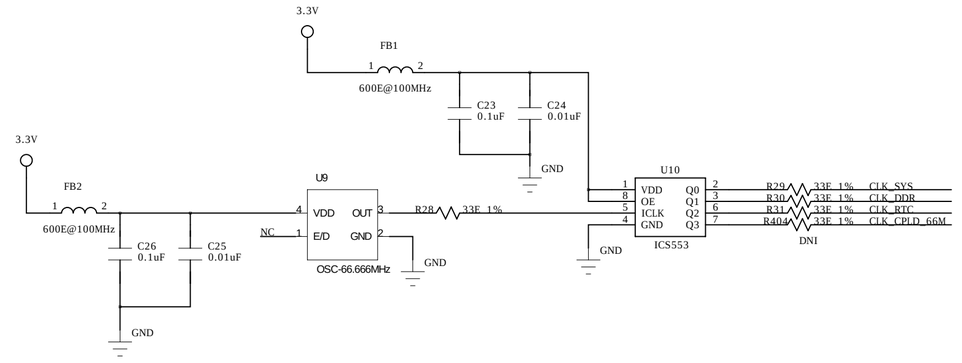
P1021_SYSTEM CONTROL

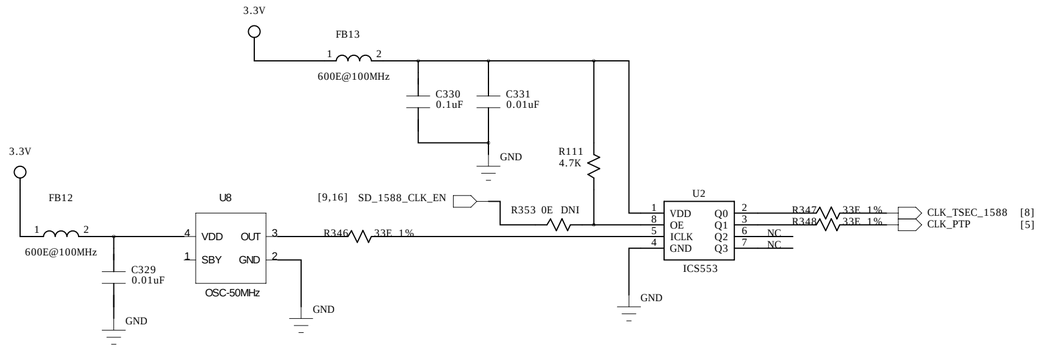




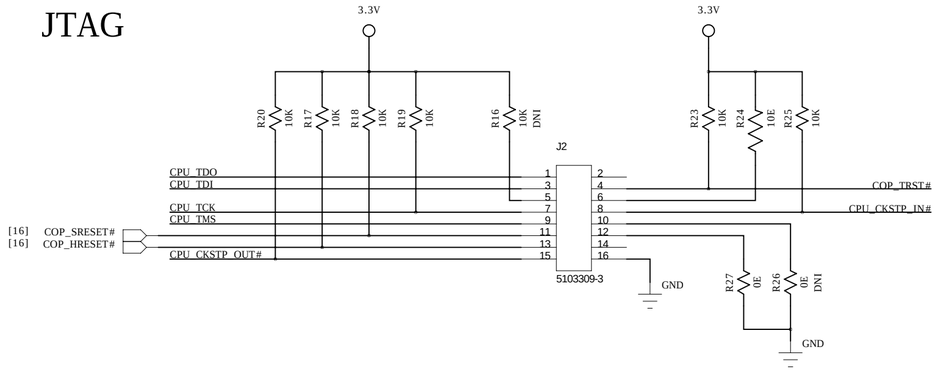
SYSTEM CLOCK



IEEE-1588 CLOCK



JTAG



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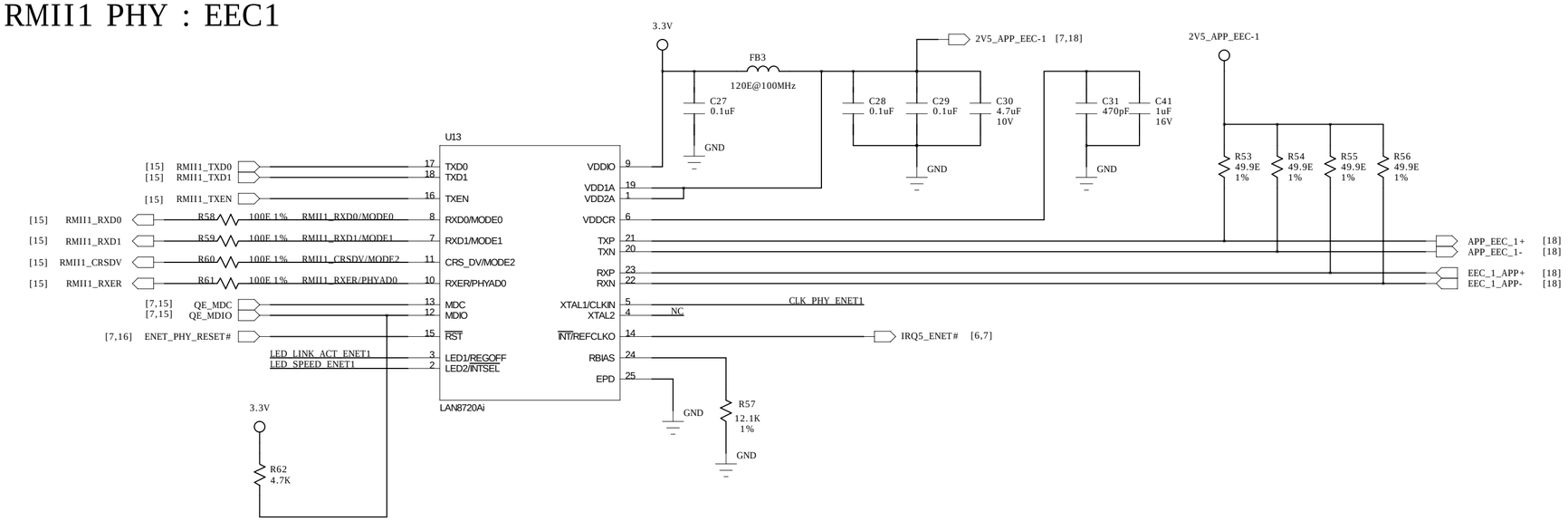
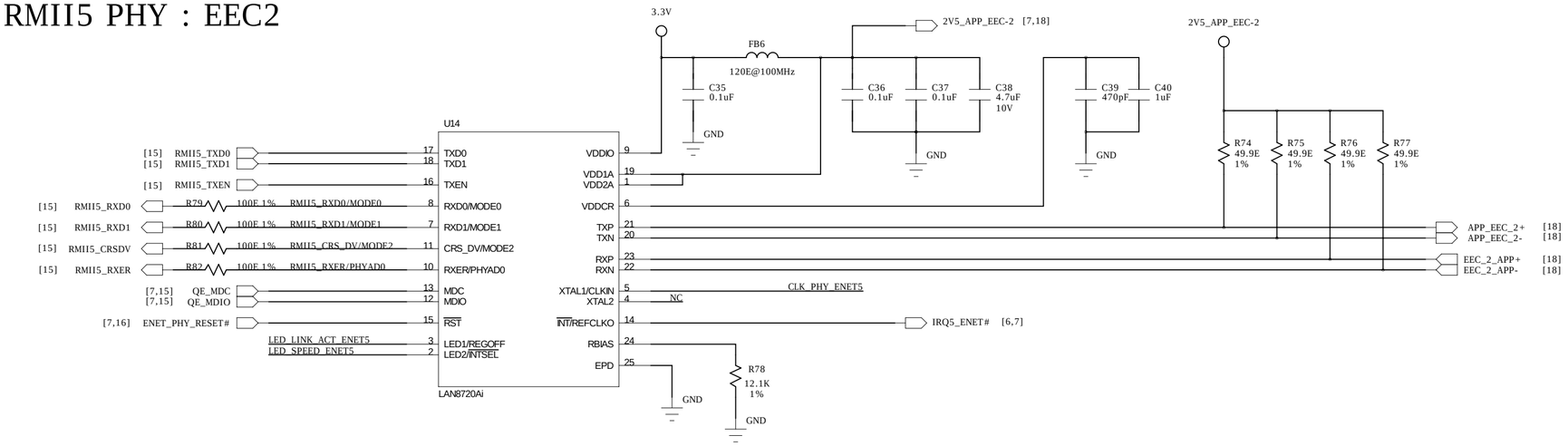
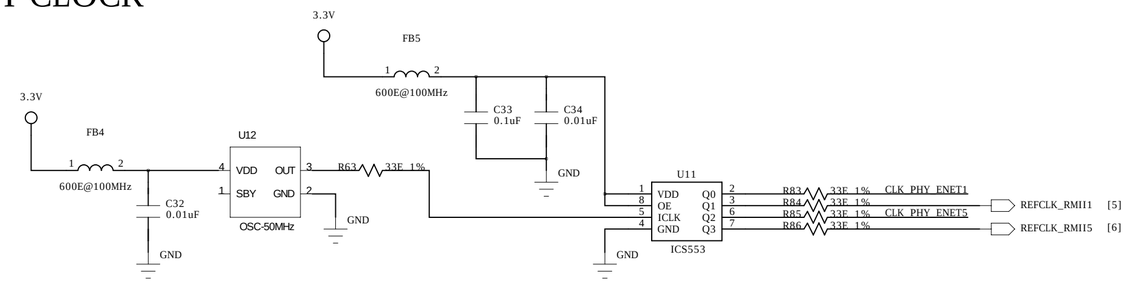
RMII1 PHY : EEC1



RMII5 PHY : EEC2



RMII CLOCK



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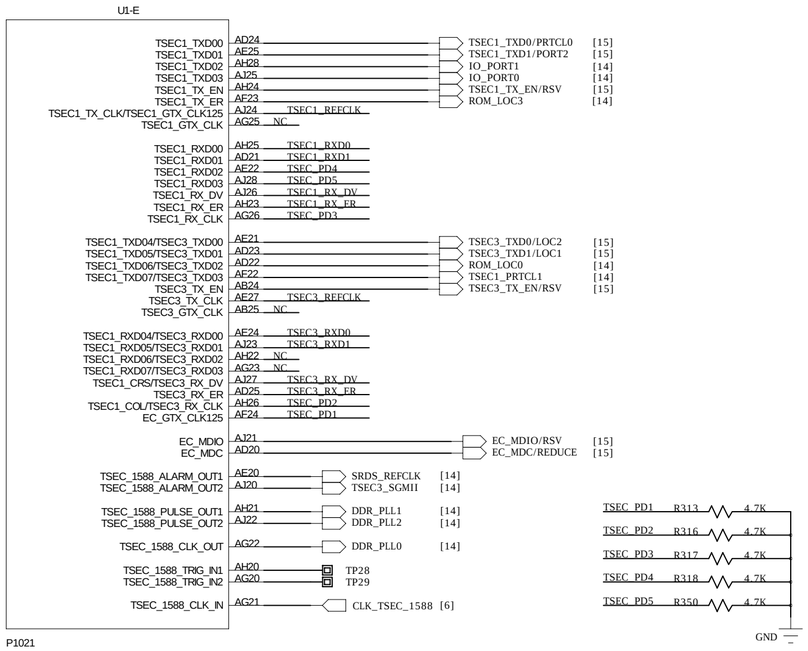
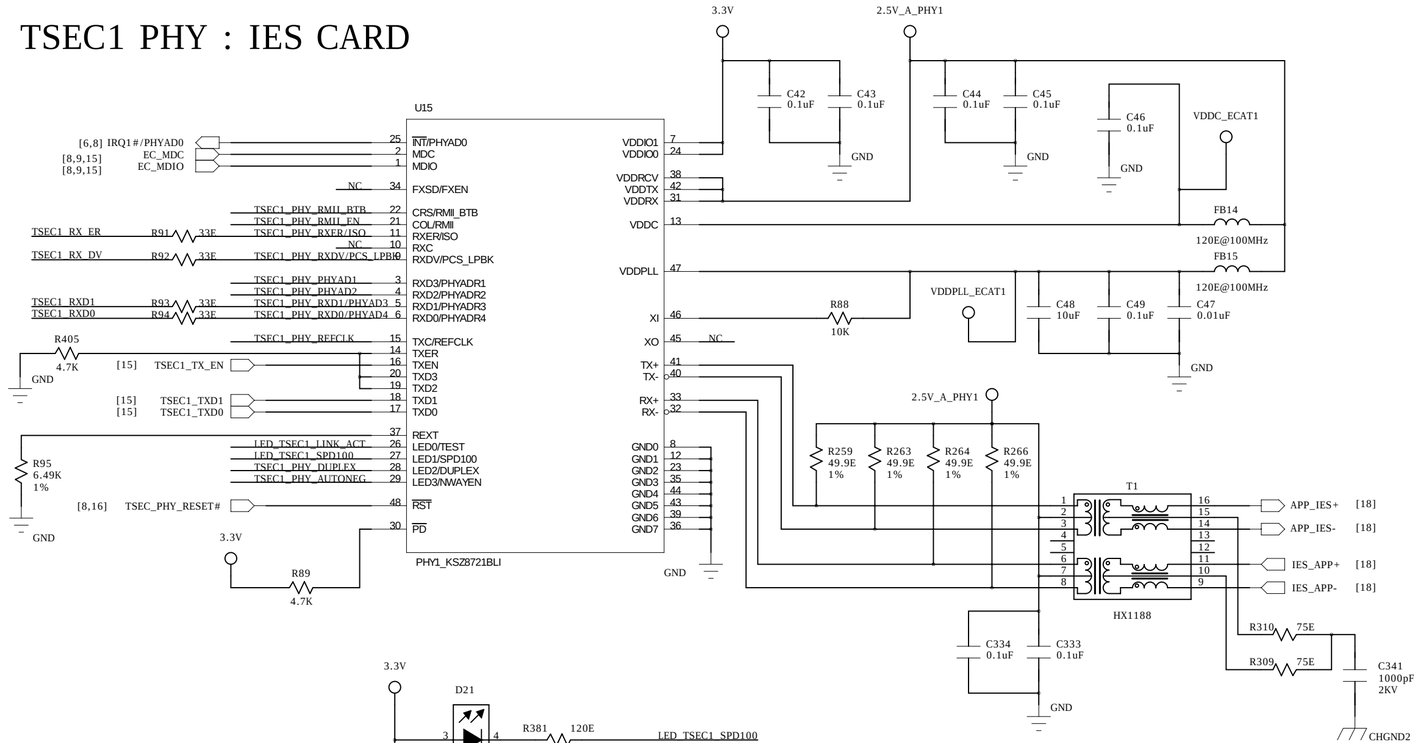
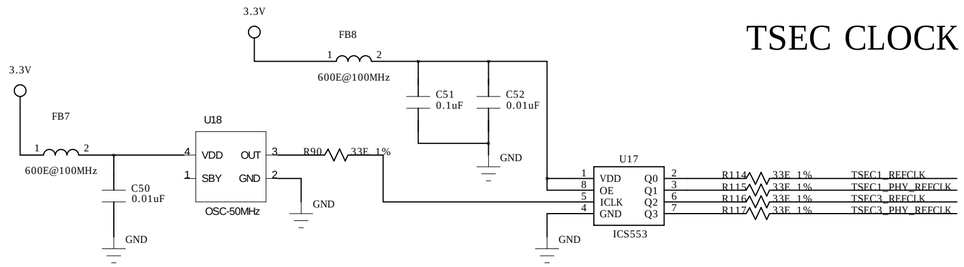
P1021_TSEC

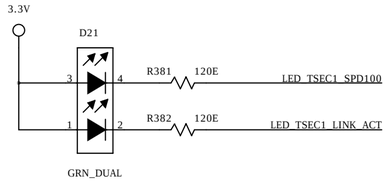


TSEC1 PHY : IES CARD

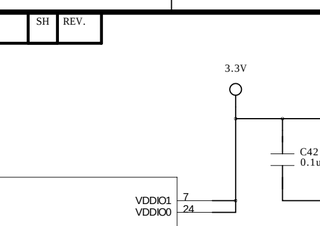


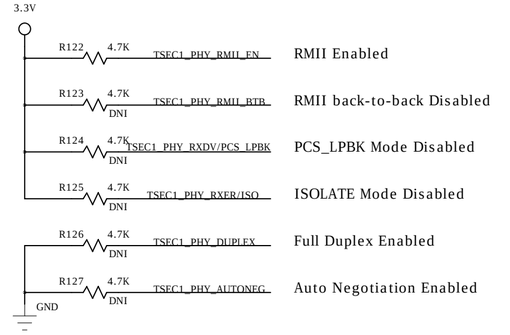
TSEC CLOCK



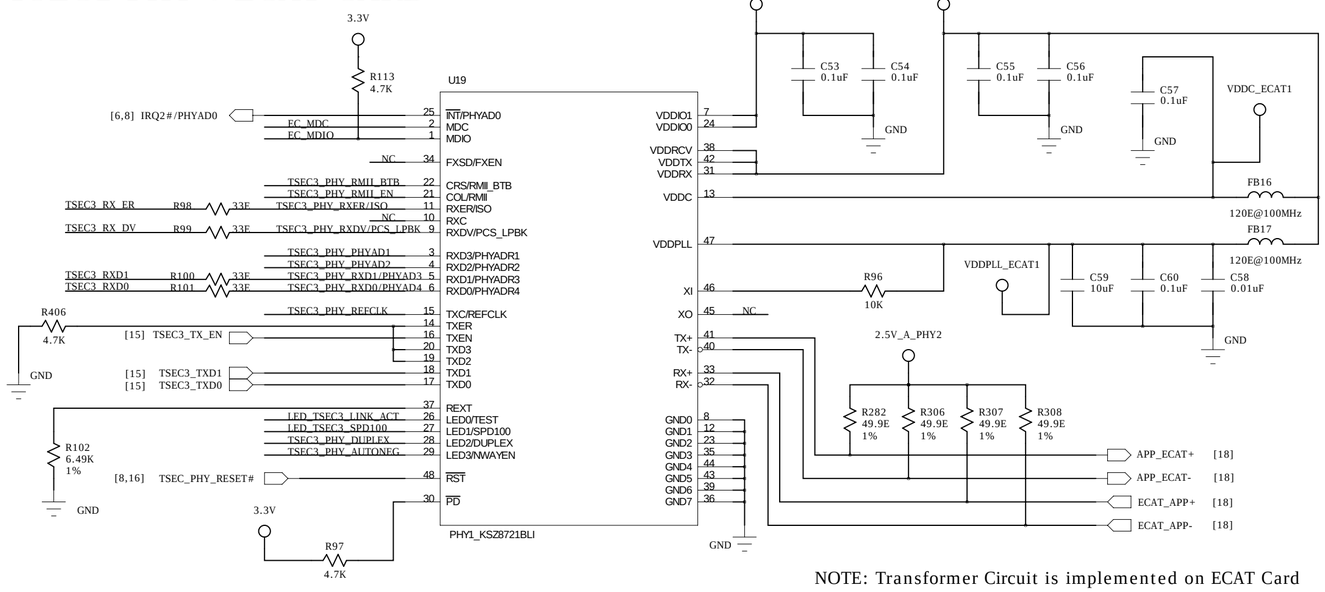


PHY ADDRESS : 00001

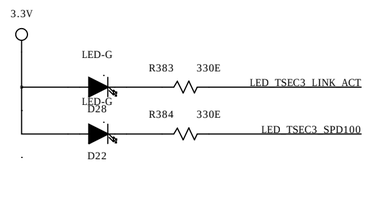


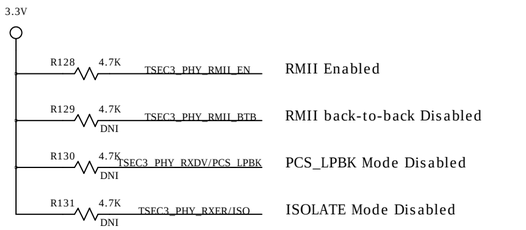


TSEC1 PHY : ECAT CARD

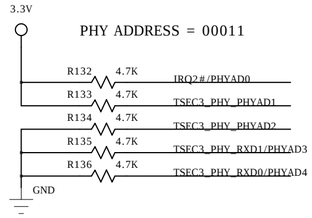


NOTE: Transformer Circuit is implemented on ECAT Card

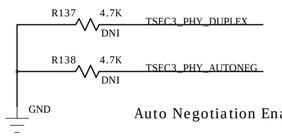




PHY ADDRESS = 00011



Full Duplex Enabled



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DRAWN AKHILESH JAISWAL	14-SEP-2011	4725 121st Street - Des Moines, Iowa 50323
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ENGINEER		SIZE C · DWG. NO. 18-600400-001 · SHEET 8 · PROD REV. 2.0 · FILE APP CARD SCHEMATIC · SCALE

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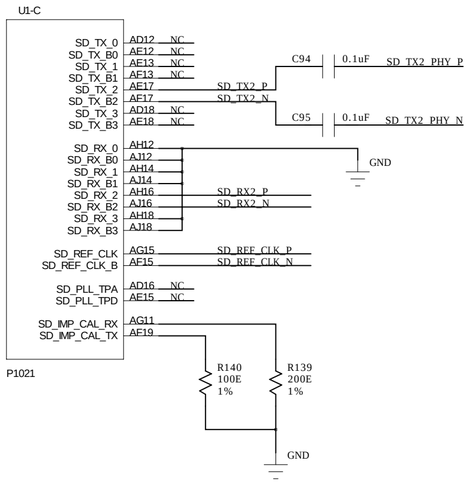
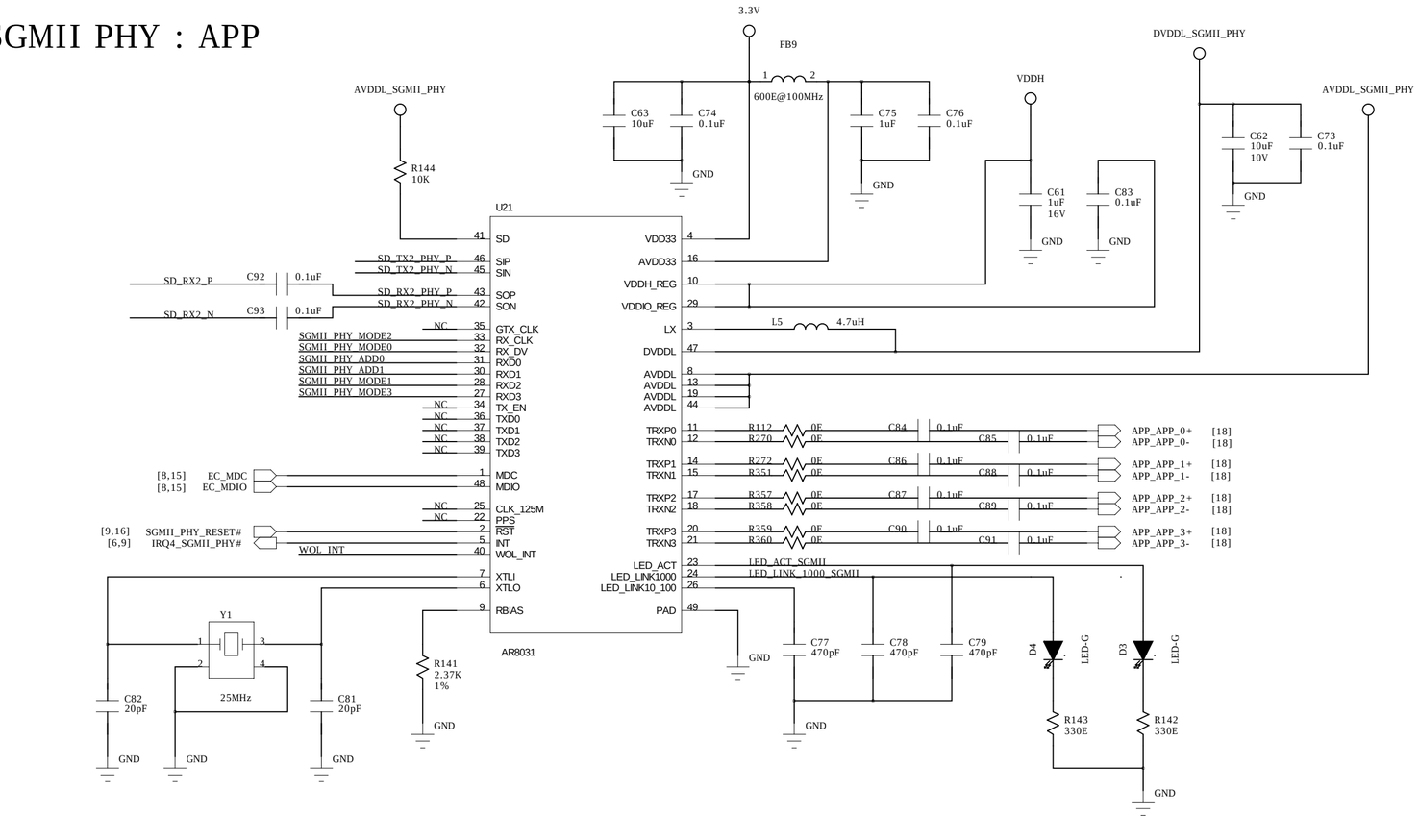
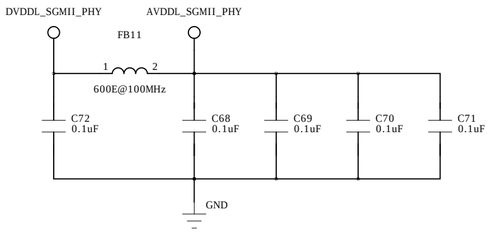
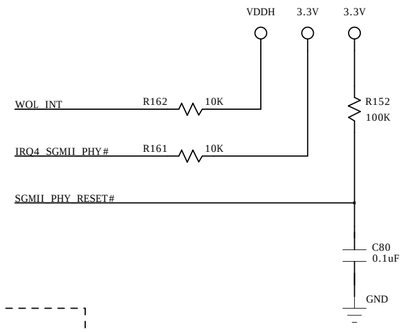
P1021_SGMII



SGMII PHY : APP

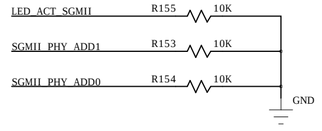




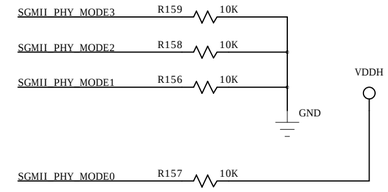


Interrupt Function Enabled on Pin - 5

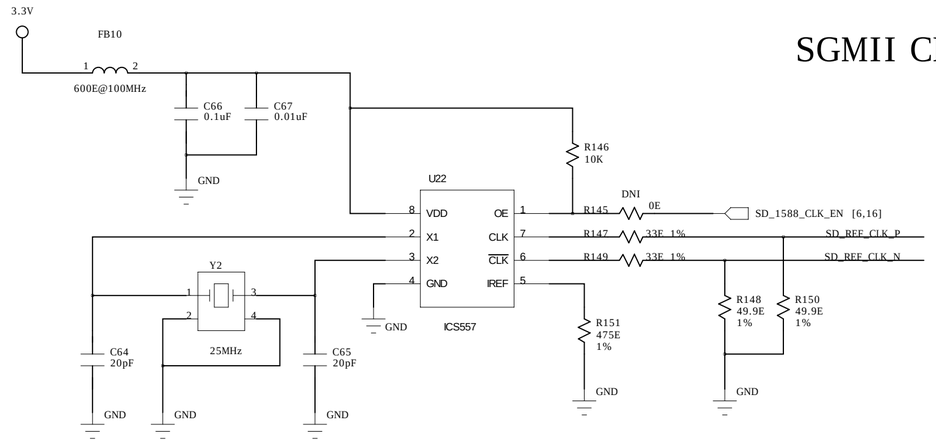
PHY Address Bit [2:0] : 000



AR8031 Mode : 1000 BASE-T, SGMII



SGMII CLOCK



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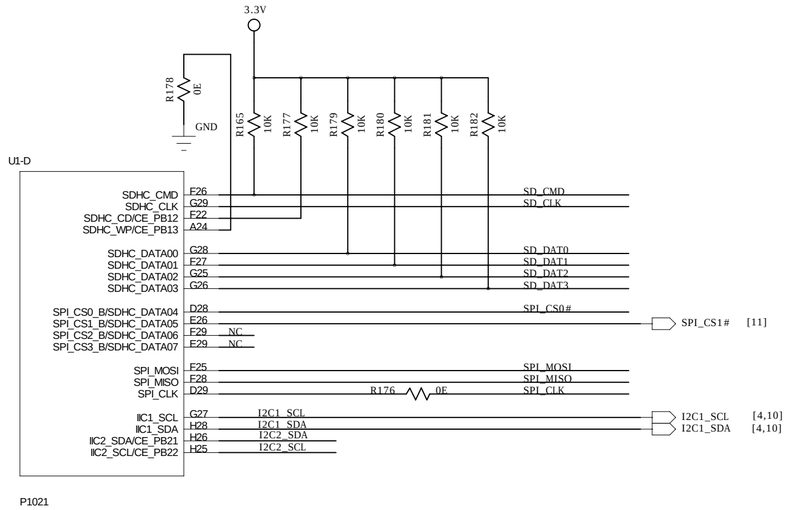
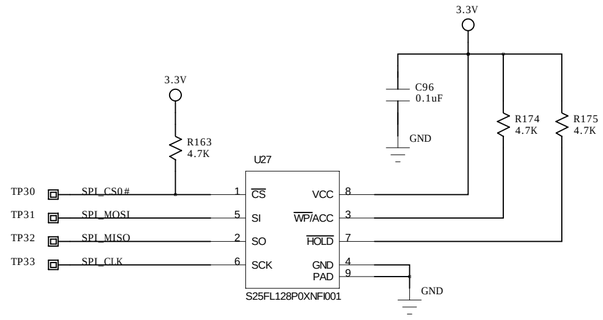
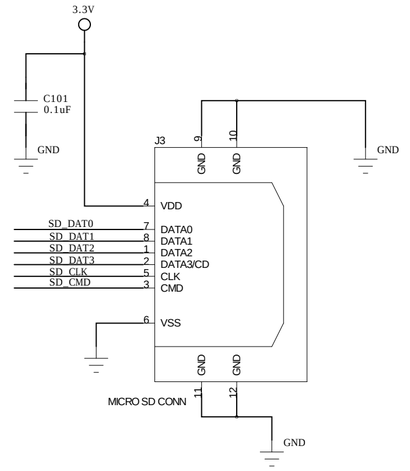
P1021_SPI_I2C



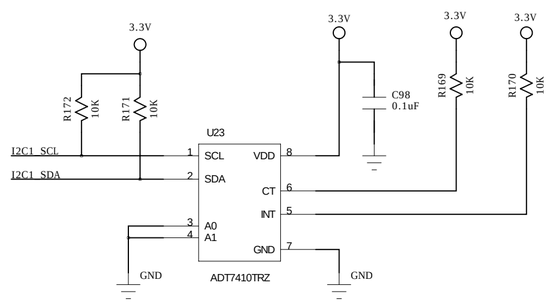
SPI FLASH : 128MBIT



SD CARD SOCKET

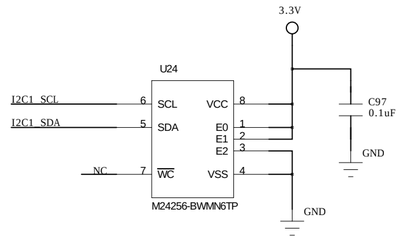


TEMPERATURE SENSOR



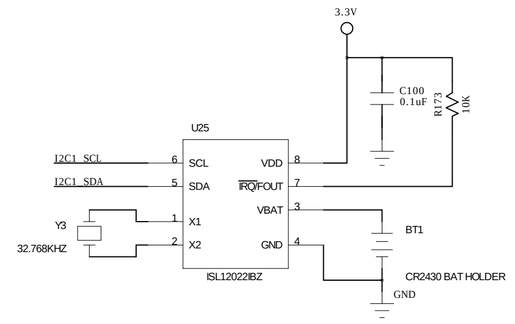
TEMPERATURE SENSOR I2C ADDRESS: 0x48

BOOT EEPROM : 256KBIT



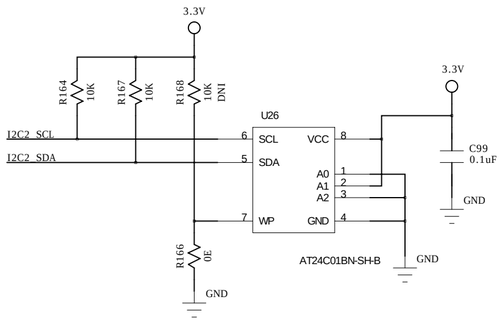
BOOT EEPROM I2C ADDRESS: 0x50

RTC



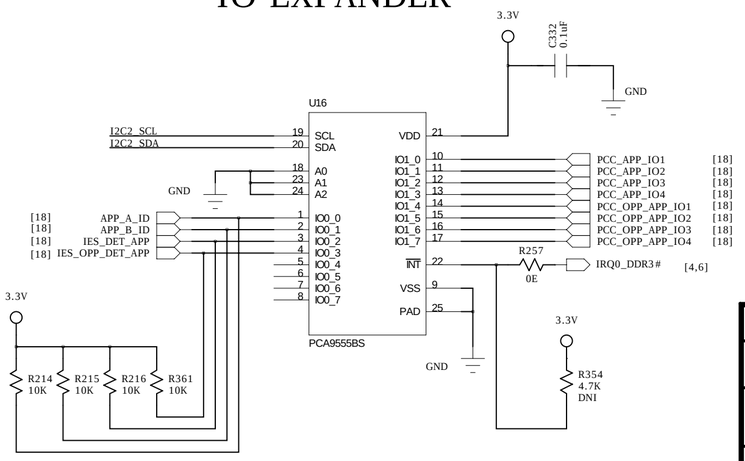
RTC I2C ADDRES: 0x68

BOARD EEPROM : 1KBIT

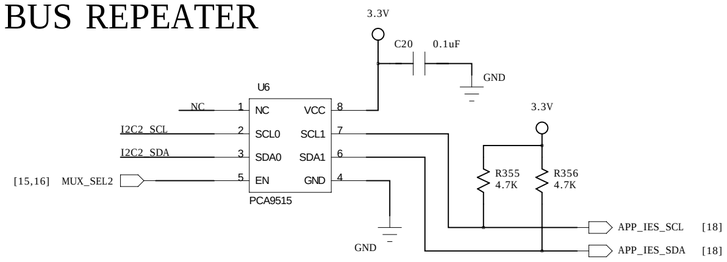


BOARD EEPROM I2C ADDRESS: 0x52

IO EXPANDER



I2C BUS REPEATER



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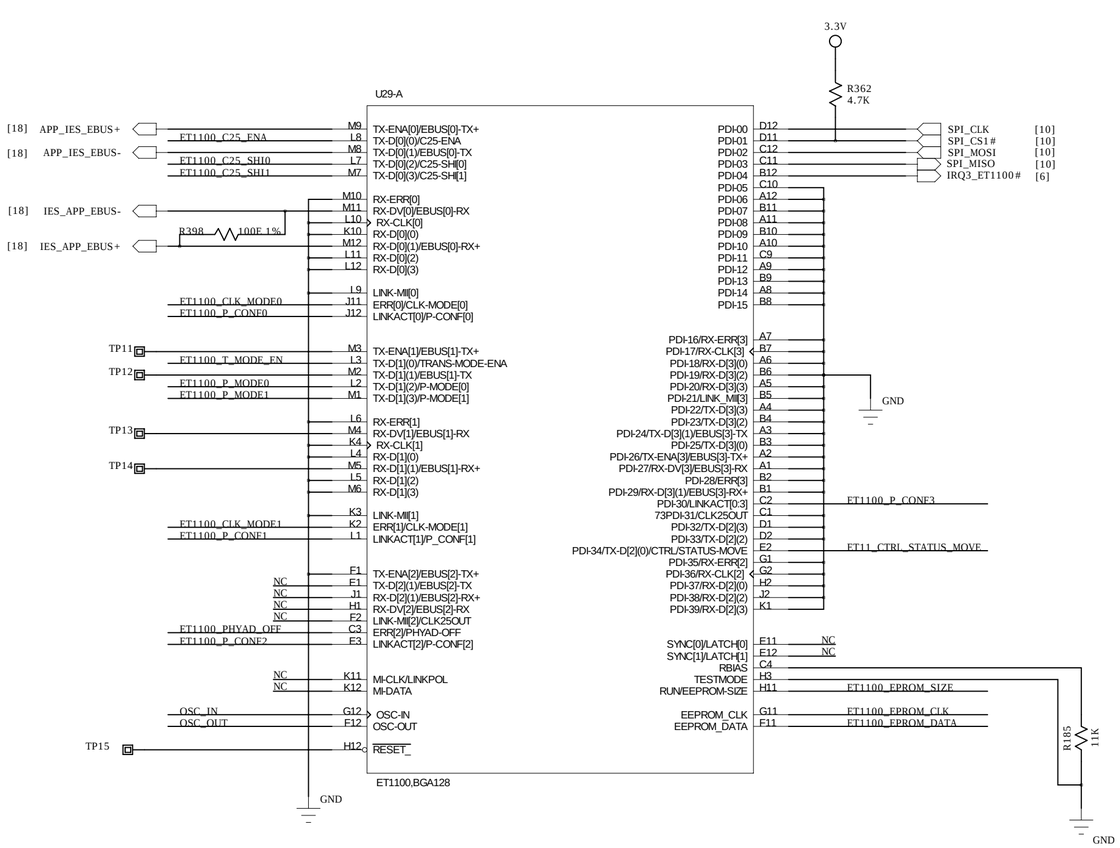
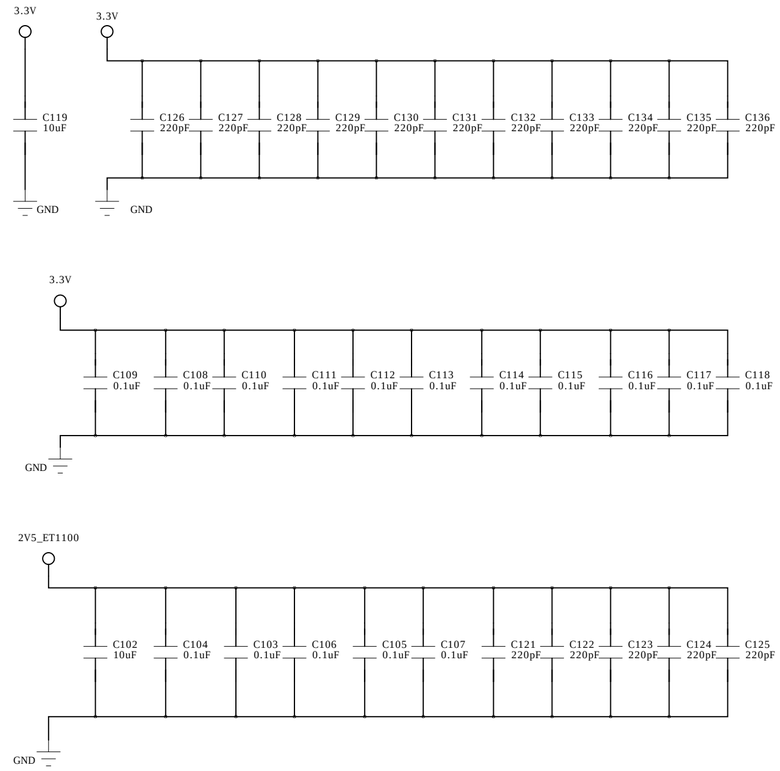
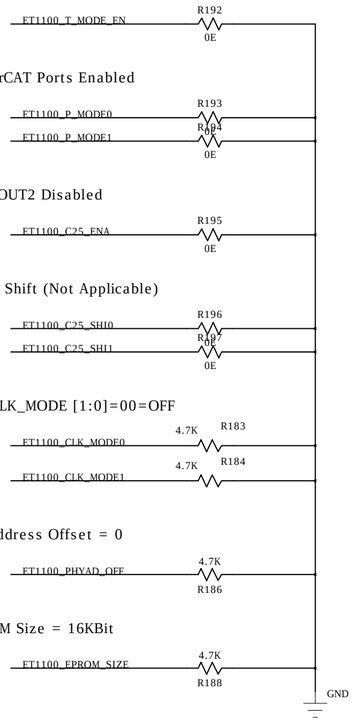
ET1100 : IES CARD





Transparent Mode Disabled



2 EtherCAT Ports Enabled

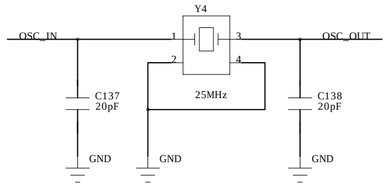
CLK25OUT2 Disabled

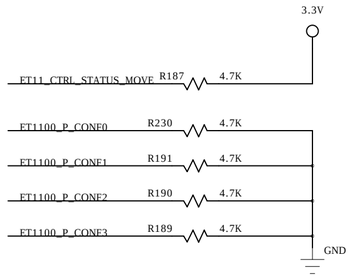
MII TX Shift (Not Applicable)

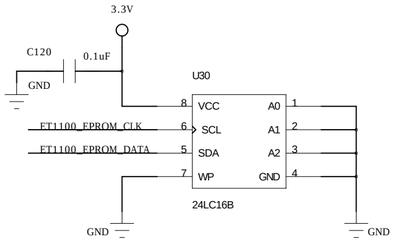
CPU_CLK_MODE [1:0]=00=OFF

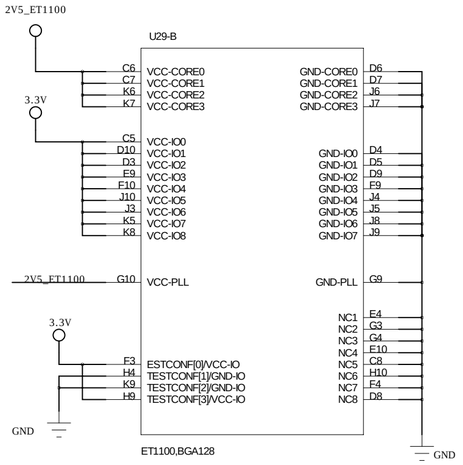
PHY Address Offset = 0

EEPROM Size = 16KBit









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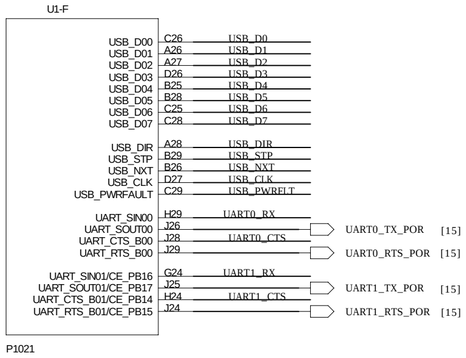
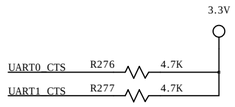
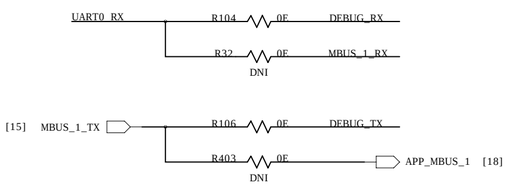
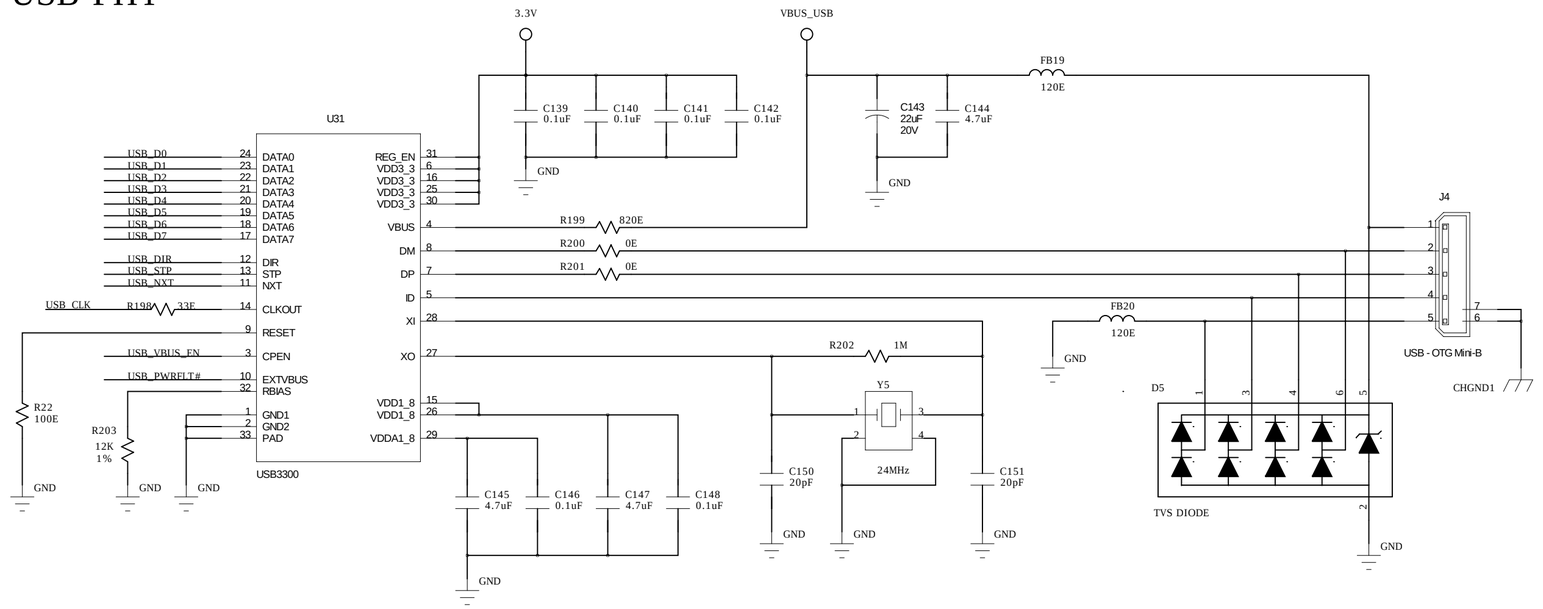
P1021_USB_SERIAL



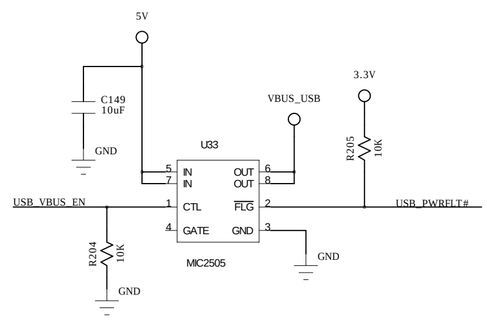




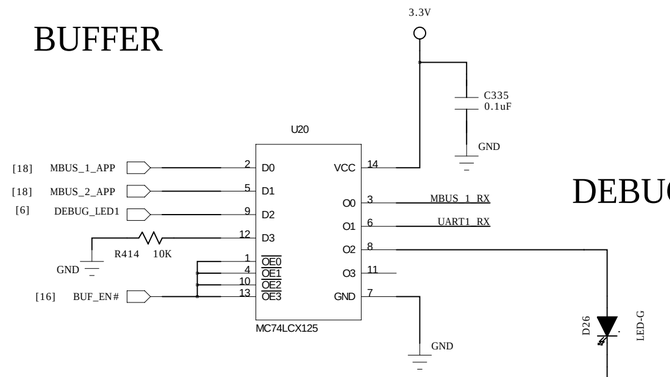
USB PHY



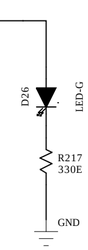
POWER SWITCH



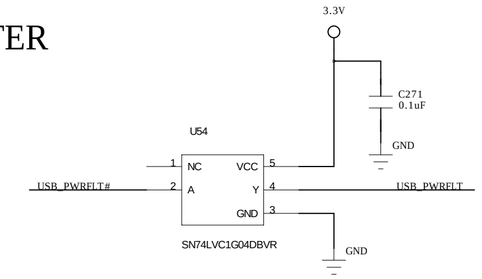
BUFFER



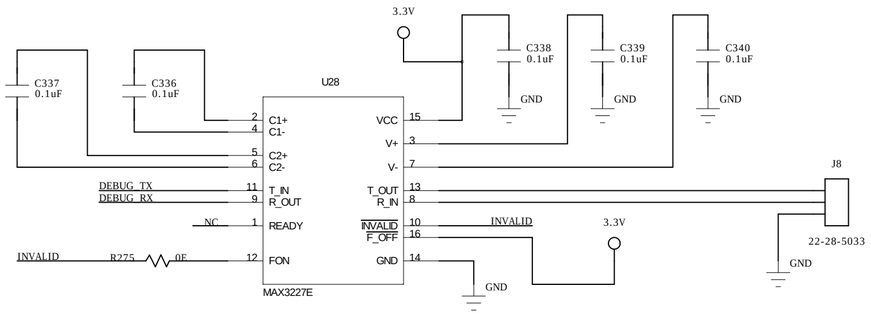
DEBUG LEDS



INVERTER



DEBUG SERIAL PORT



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C	18-600400-001	12	2.0
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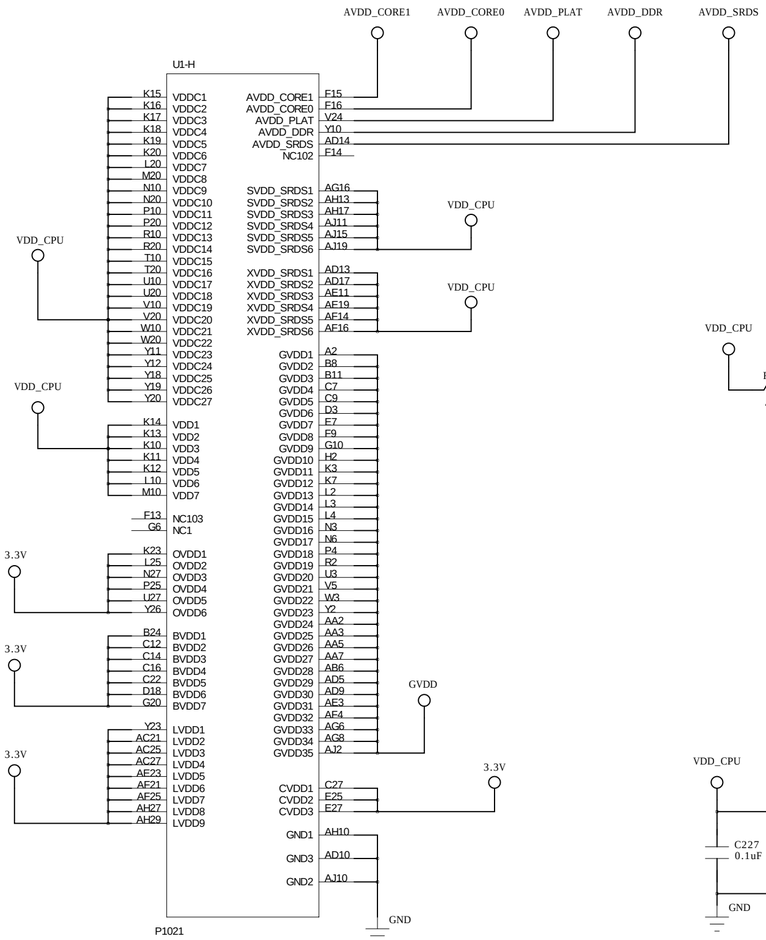
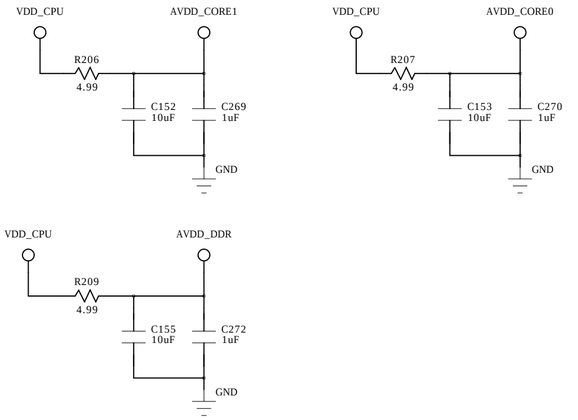
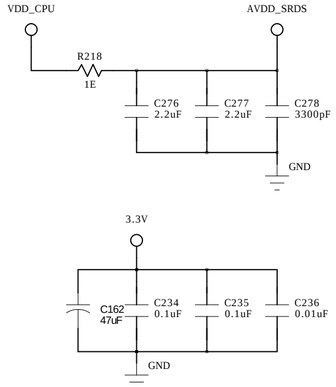
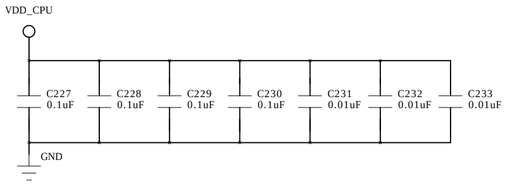
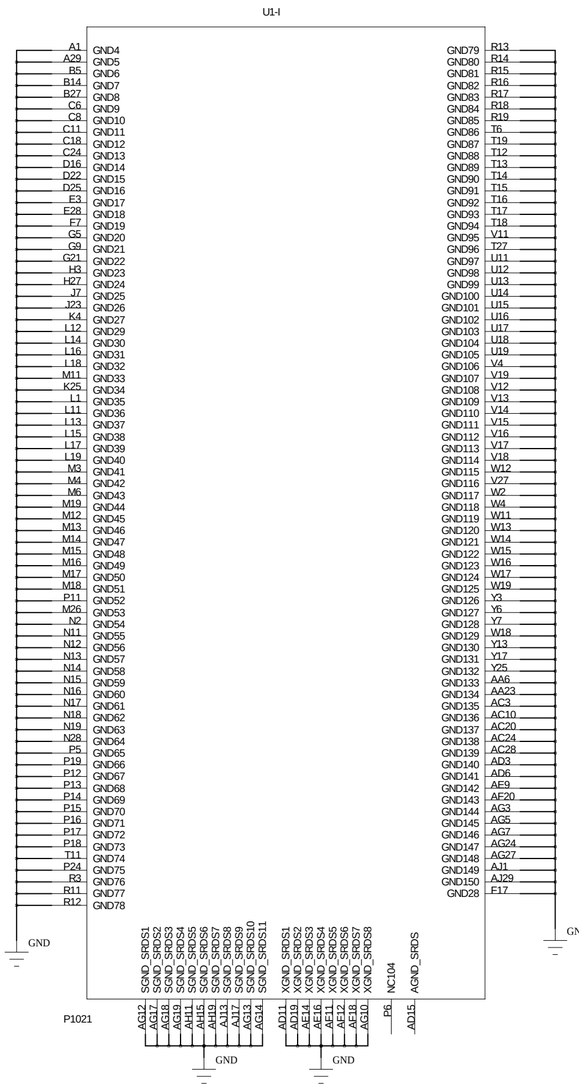
P1021_POWER

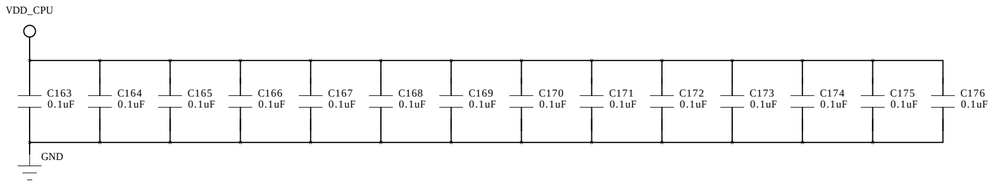


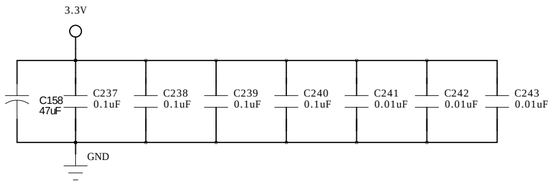


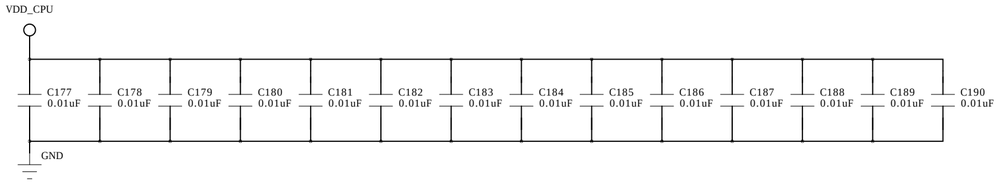


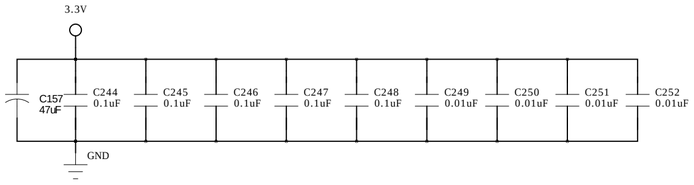


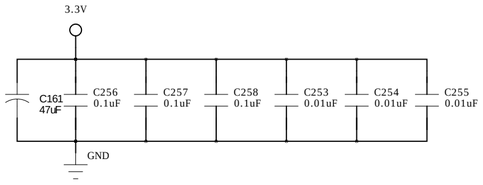


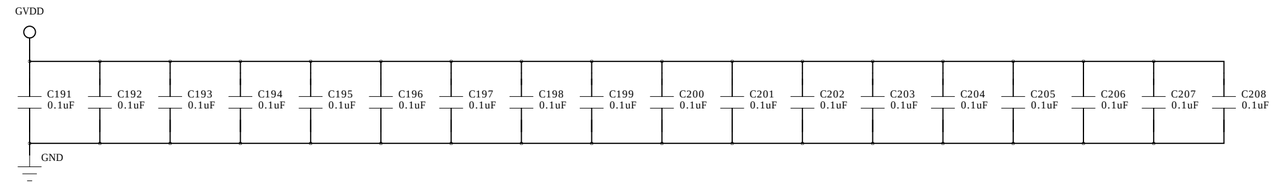


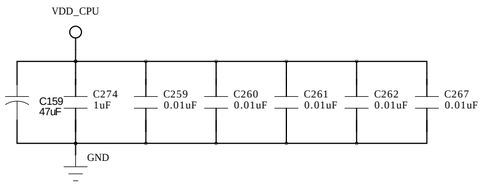


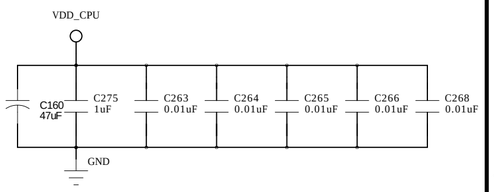


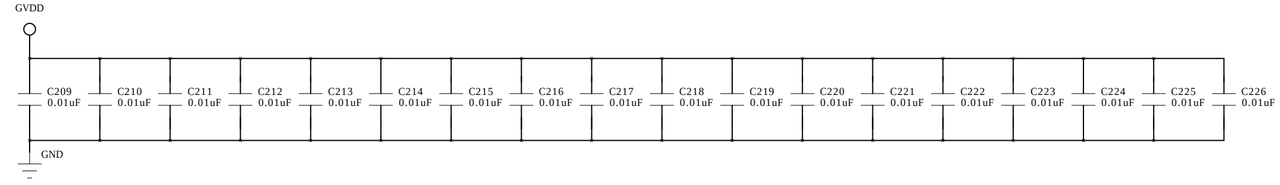












APPROVALS	DATE	COMPRESSOR CONTROLS CORPORATION
DRAWN AKHILESH JAISWAL	14-SEP-2011	4725 121st Street - Des Moines, Iowa 50323
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ENGINEER		SIZE C · DWG. NO. 18-600400-001 · SHEET 13 · PROD REV. 2.0 · FILE APP CARD SCHEMATIC · SCALE

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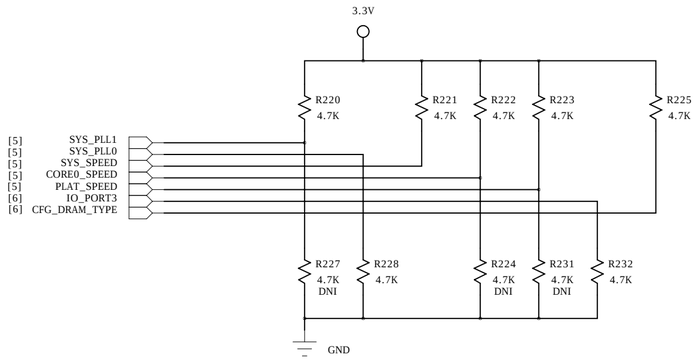

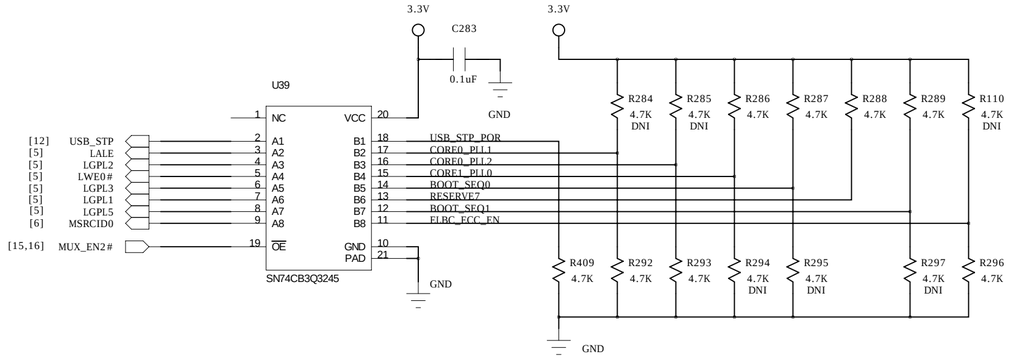

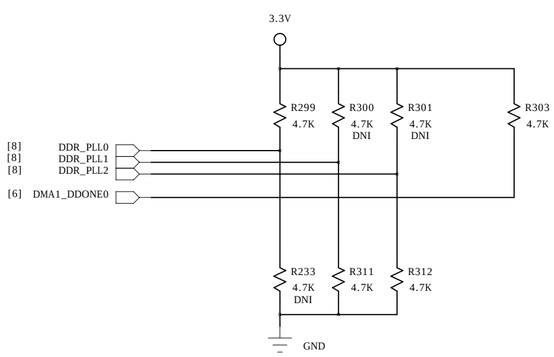

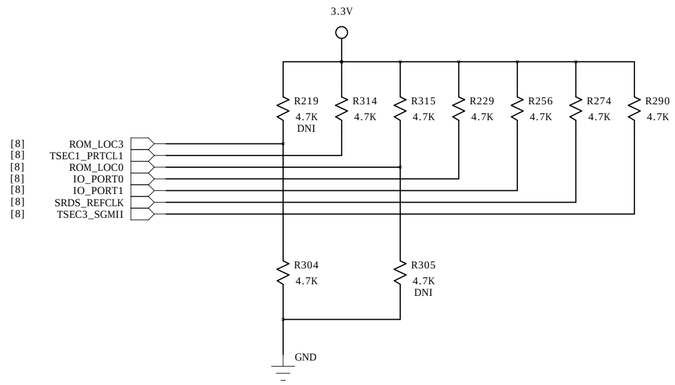

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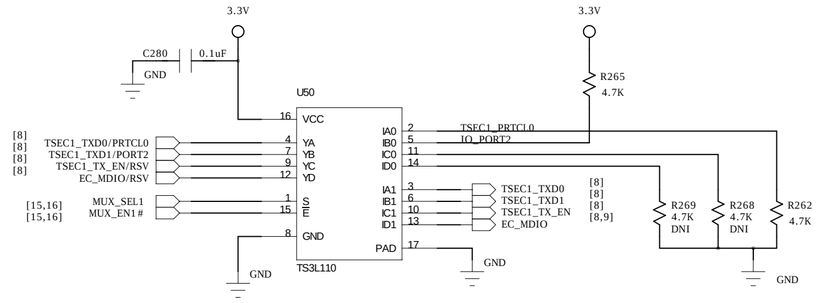

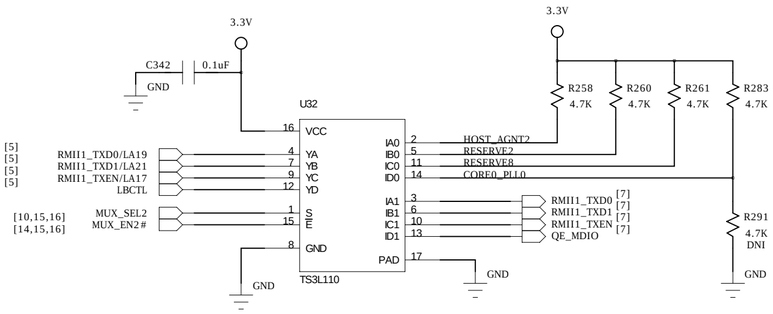

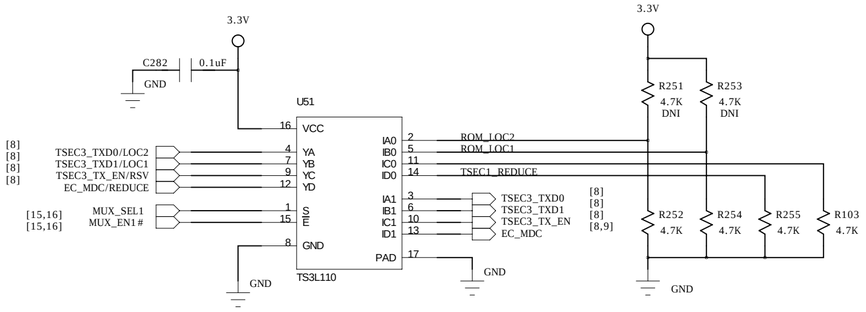

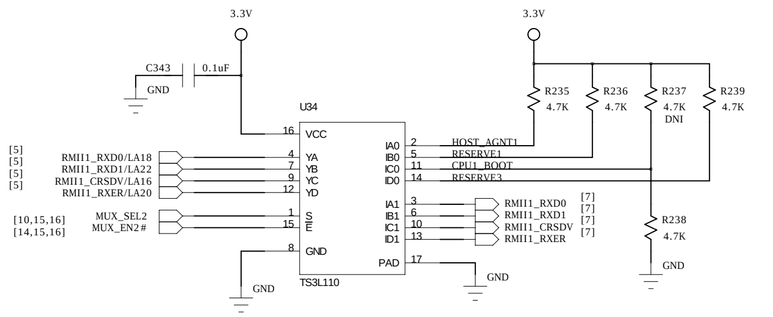

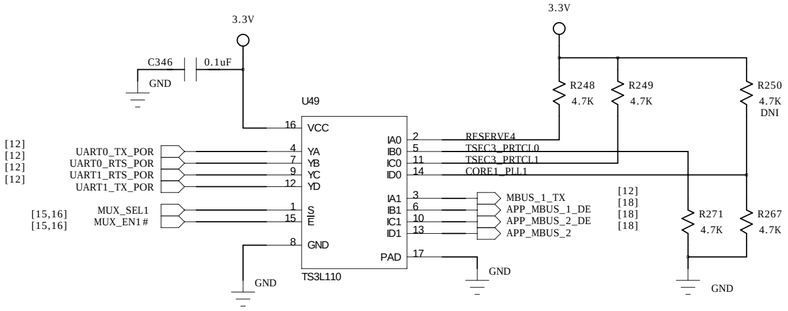

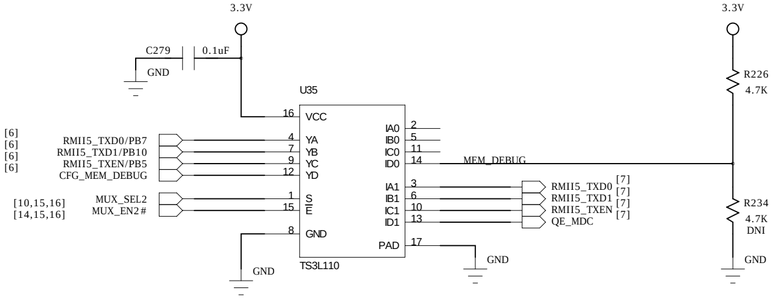

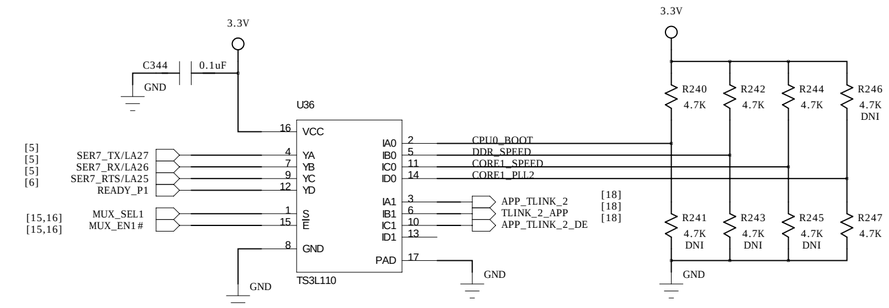

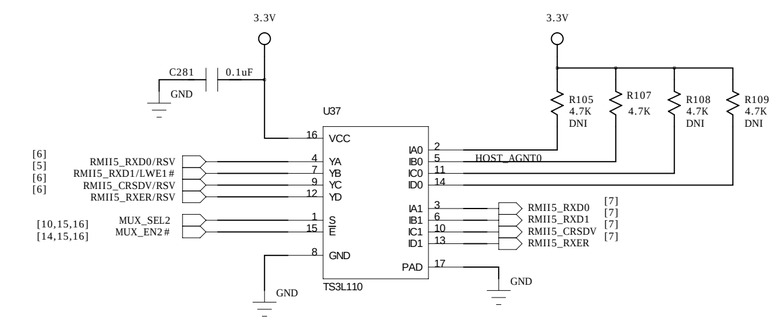

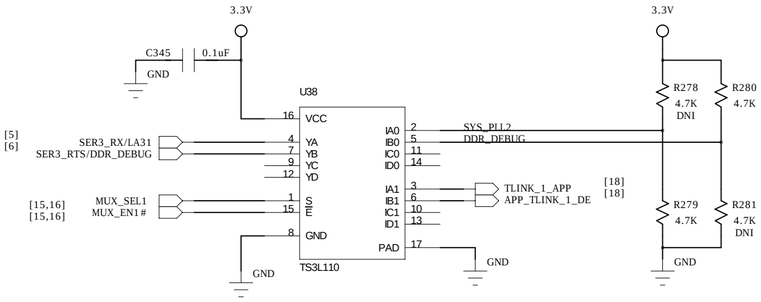

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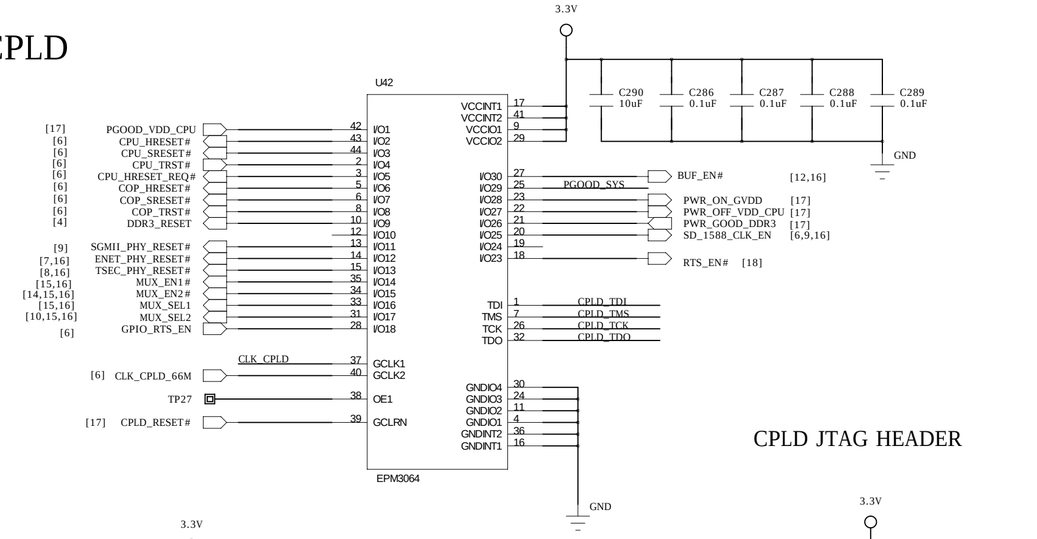
CPLD



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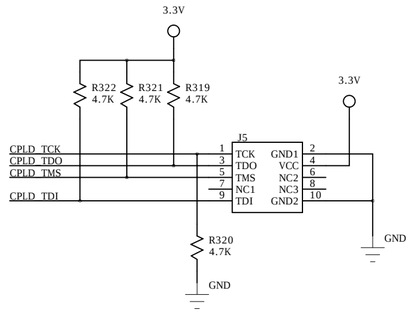

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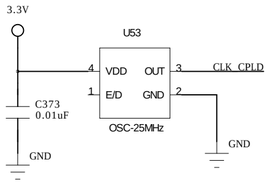
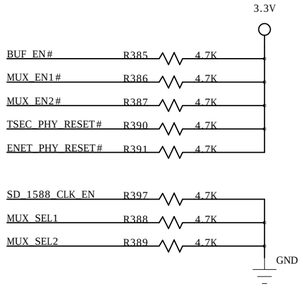
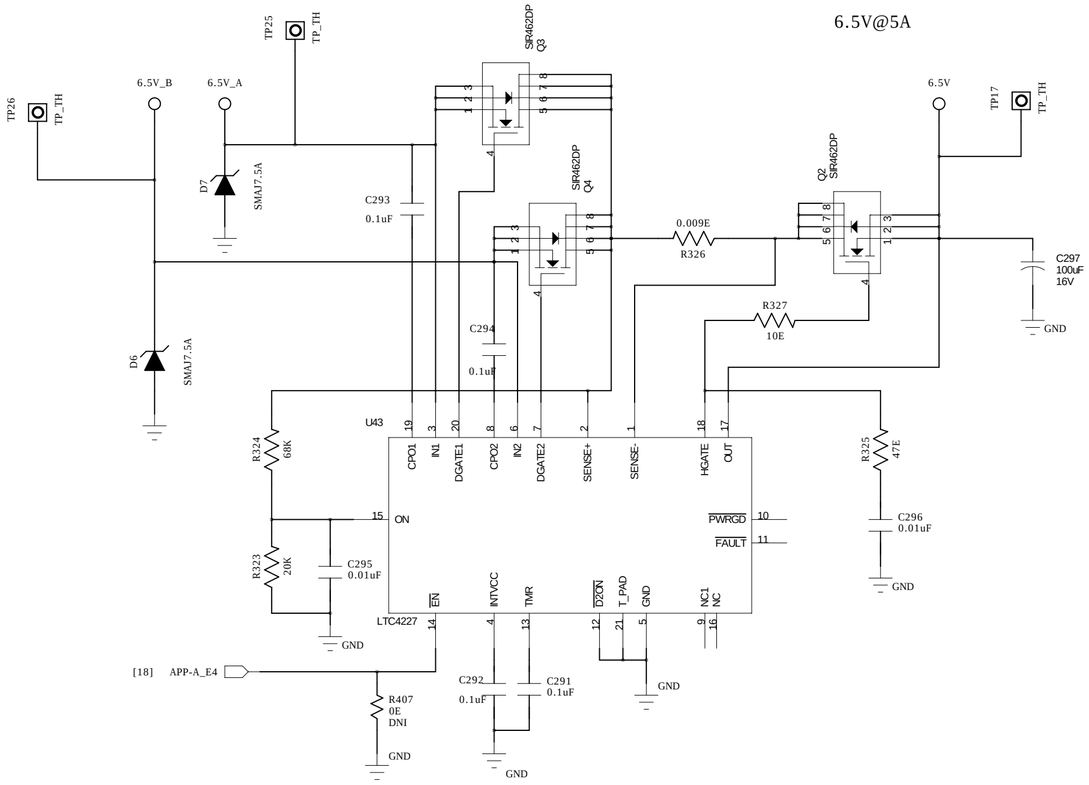


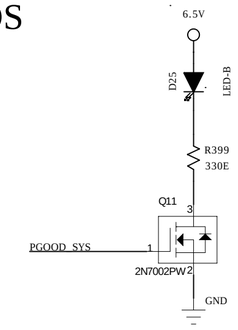


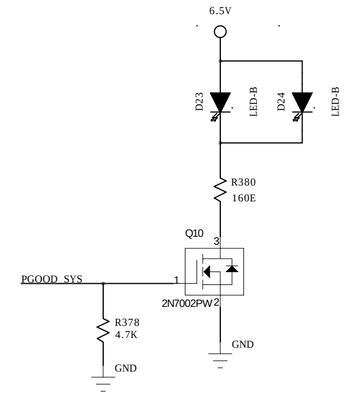
HOT SWAP

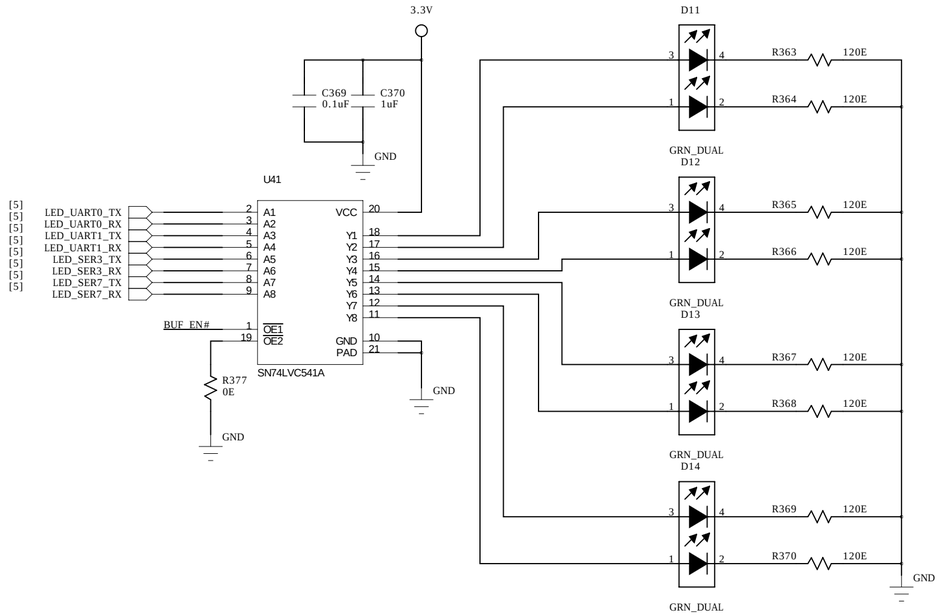
6.5V@5A

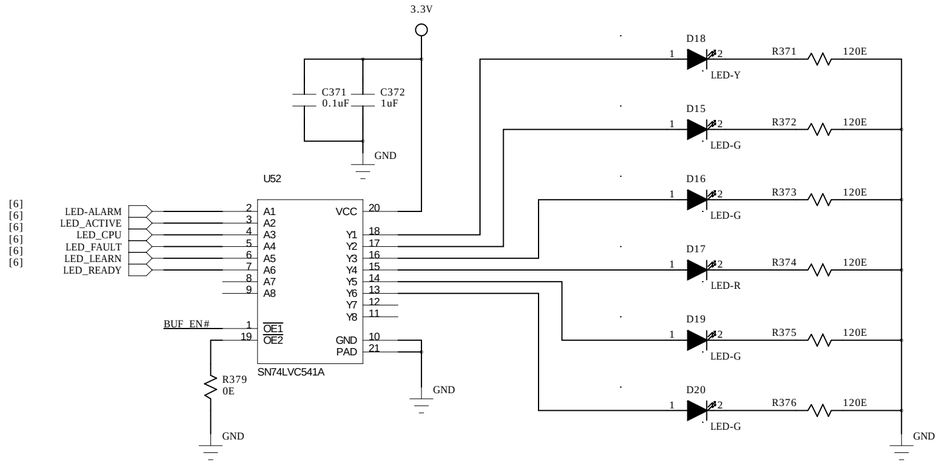


FRONT PANEL LEDS









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	FILE: APP CARD SCHEMATIC	SCALE	

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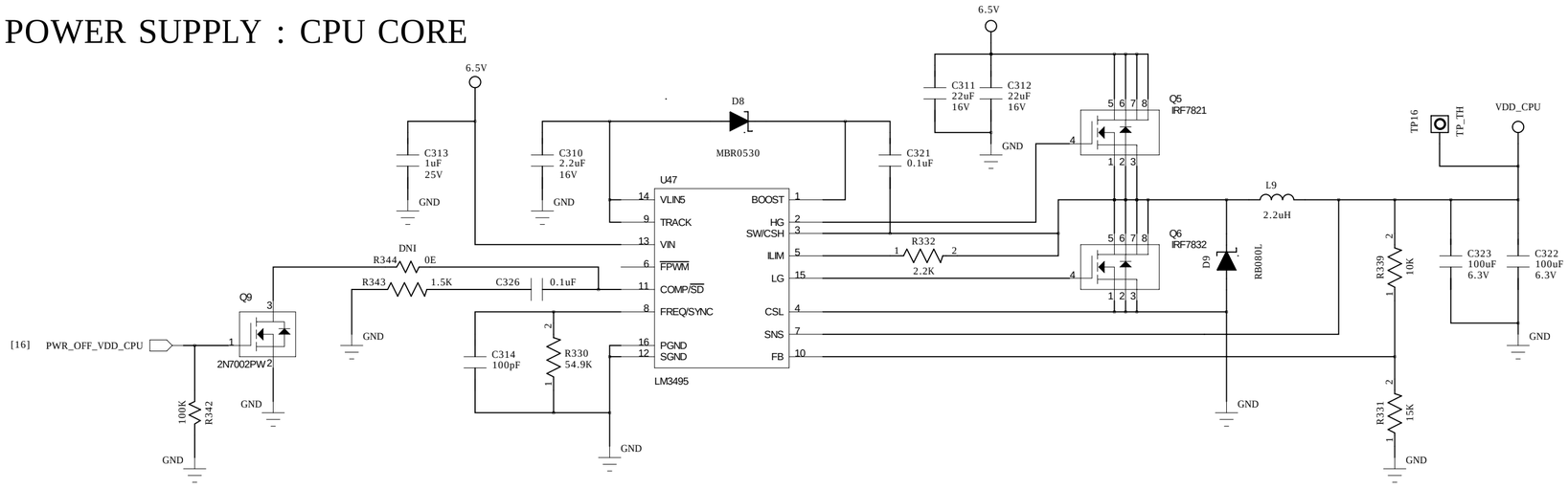
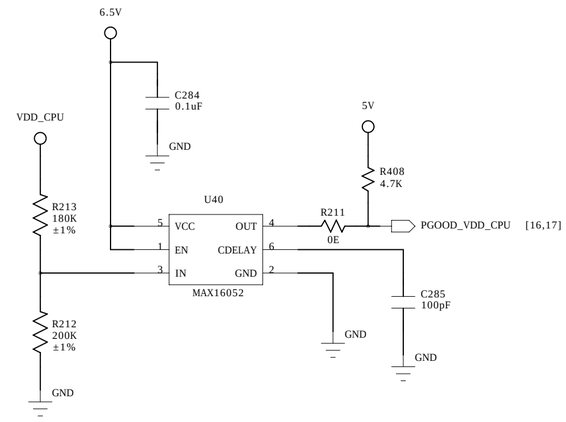
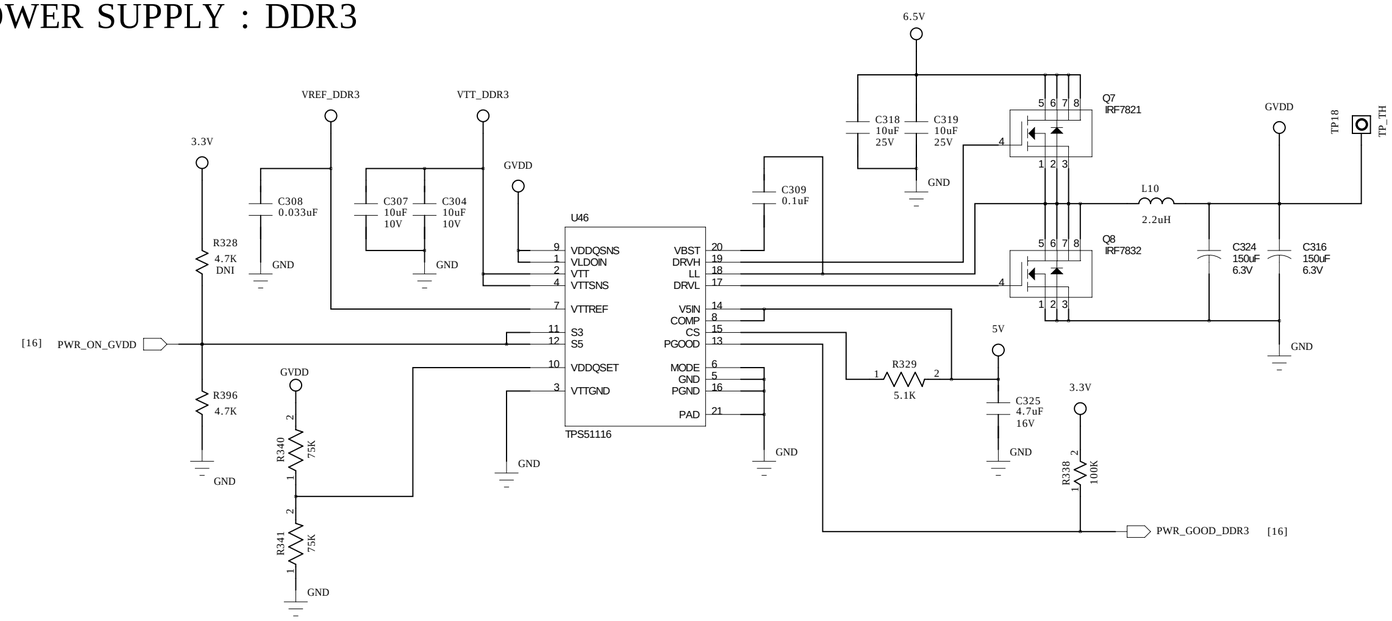
POWER SUPPLY : CPU CORE



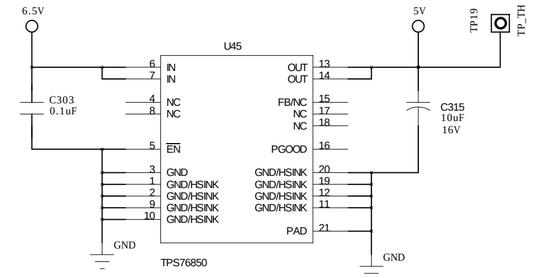
VDD_CPU MONITOR



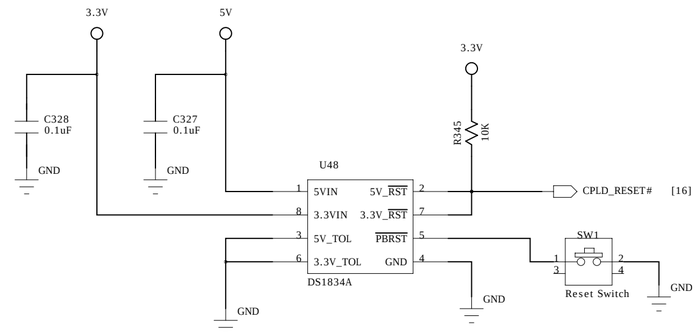
POWER SUPPLY : DDR3



POWER SUPPLY : 5V



3.3V AND 5V MONITOR_RESET CONTROL



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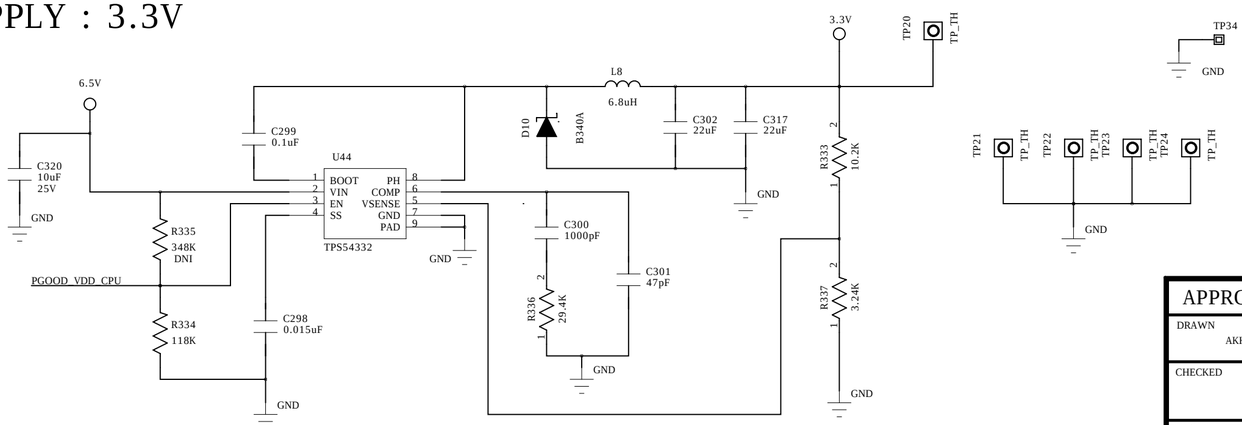

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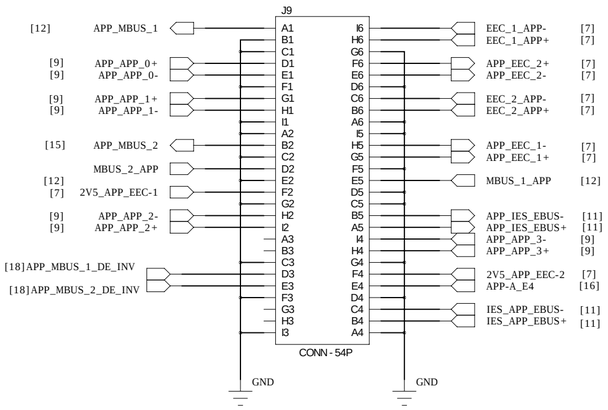
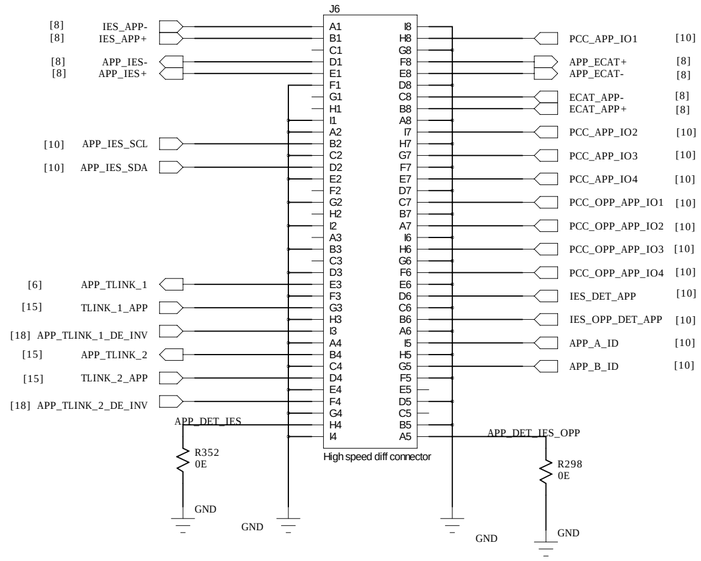
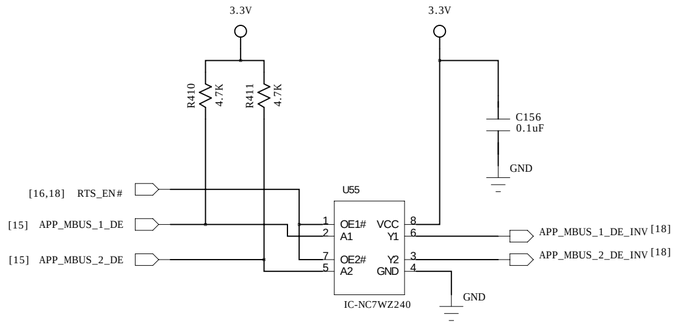
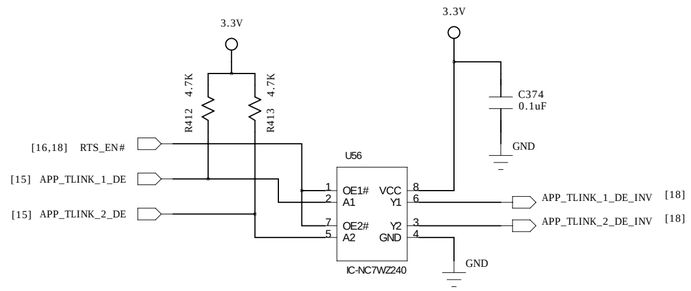
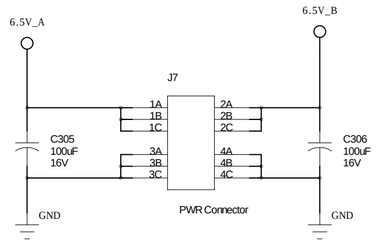
BACKPLANE CONNECTOR

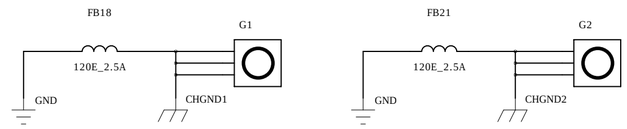












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			FILE APP CARD SCHEMATIC	SCALE	

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