# hynix

## 200pin Unbuffered DDR2 SDRAM SO-DIMMs based on 1Gb version C

This Hynix unbuffered Small Outline Dual In-Line Memory Module(DIMM) series consists of 1Gb version C DDR2 SDRAMs in Fine Ball Grid Array(FBGA) packages on a 200pin glass-epoxy substrate. This Hynix 1Gb version C based Unbuffered DDR2 SO-DIMM series provide a high performance 8 byte interface in 67.60mm width form factor of industry standard. It is suitable for easy interchange and addition.

## FEATURES

- JEDEC standard Double Data Rate 2 Synchronous DRAMs (DDR2 SDRAMs) with 1.8V +/- 0.1V Power Supply

- All inputs and outputs are compatible with SSTL_1.8 interface

- Posted CAS

- Programmable CAS Latency 3 ,4 ,5, and 6

- OCD (Off-Chip Driver Impedance Adjustment) and ODT (On-Die Termination)

- Fully differential clock operations (CK & $\overline{CK}$)

- Programmable Burst Length  4 / 8 with both sequential and interleave mode

- Auto refresh and self refresh supported

- 8192 refresh cycles / 64ms

- Serial presence detect with EEPROM

- DDR2 SDRAM Package: 60 ball(x8) , 84 ball(x16) FBGA

- 67.60 x 30.00 mm form factor

- RoHS compliant

## ORDERING INFORMATION

| Part Name | Density | Organization | # of DRAMs | # of ranks | Materials |
|---|---|---|---|---|---|
| HYMP164S64CP6-C4/Y5/S5/S6 | 512MB | 64Mx64 | 4 | 1 | Lead free |
| HYMP164S64CR6-C4/Y5/S5/S6 | 512MB | 64Mx64 | 4 | 1 | Halogen free |
| HYMP112S64CP6-C4/Y5/S5/S6 | 1GB | 128Mx64 | 8 | 2 | Lead free |
| HYMP112S64CR6-C4/Y5/S5/S6 | 1GB | 128Mx64 | 8 | 2 | Halogen free |
| HYMP125S64CP8-C4/Y5/S5/S6 | 2GB | 256Mx64 | 16 | 2 | Lead free |
| HYMP125S64CR8-C4/Y5/S5/S6 | 2GB | 256Mx64 | 16 | 2 | Halogen free |

## SPEED GRADE & KEY PARAMETERS

|  | C4<br>(DDR2-533) | Y5<br>(DDR2-667) | S6<br>(DDR2-800) | S5<br>(DDR2-800) | Unit |
|---|---|---|---|---|---|
| Speed@CL3 | 400 | 400 | - | 400 | Mbps |
| Speed@CL4 | 533 | 533 | 533 | 533 | Mbps |
| Speed@CL5 | - | 667 | 667 | 800 | Mbps |
| Speed@CL6 | - | - | 800 | - | Mbps |
| CL-tRCD-tRP | 4-4-4 | 5-5-5 | 6-6-6 | 5-5-5 | tCK |

## ADDRESS TABLE

| Density | Organization | Ranks | SDRAMs | # of DRAMs | # of row/bank/column Address | Refresh Method |
|---|---|---|---|---|---|---|
| **512MB** | 64M x 64 | 1 | 64Mb x 16 | 4 | 13(A0~A12)/3(BA0~BA2)/10(A0~A9) | 8K / 64ms |
| **1GB** | 128M x 64 | 2 | 64Mb x 16 | 8 | 13(A0~A12)/3(BA0~BA2)/10(A0~A9) | 8K / 64ms |
| **2GB** | 256M x 64 | 2 | 128Mb x 8 | 16 | 14(A0~A13)/3(BA0~BA2)/10(A0~A9) | 8K / 64ms |

## PIN DESCRIPTION

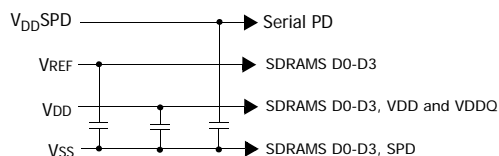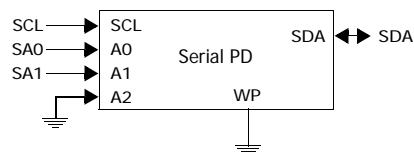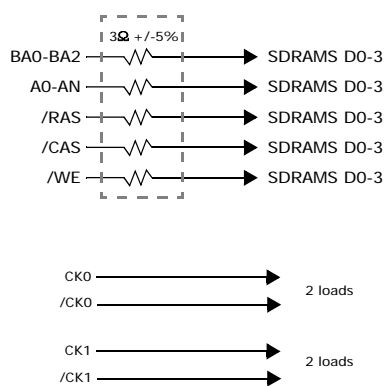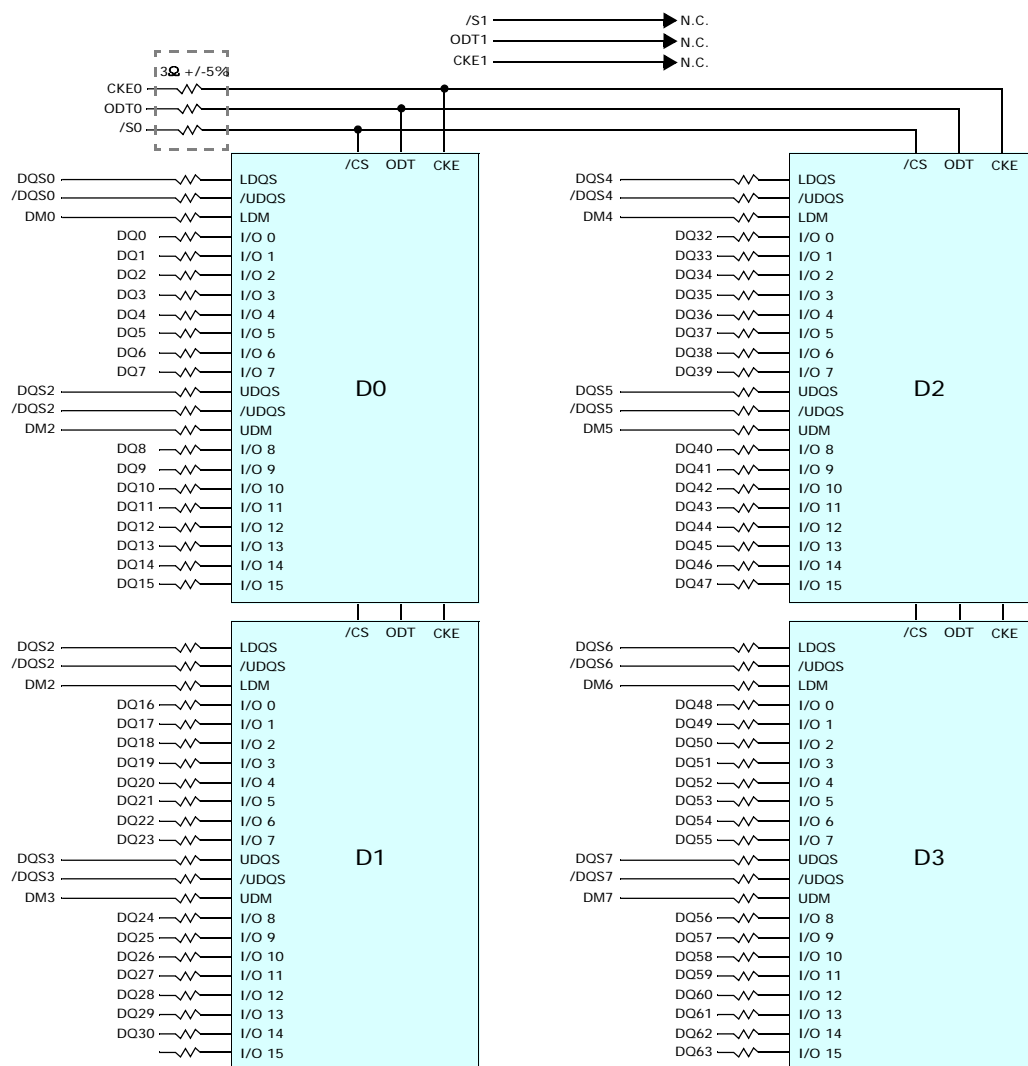| Symbol | Type | Polarity | Pin Description |
|---|---|---|---|
| CK[1:0], $\overline{CK}$[1:0] | Input | Cross Point | The system clock inputs. All adress an commands lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$. A Delay Locked Loop(DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock. |
| CKE[1:0] | Input | Active High | Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low.  By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode. |
| $\overline{S}$[1:0] | Input | Active Low | Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S}$0; Rank 1 is selected by $\overline{S}$1 |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Input | Active Low | When sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$, $\overline{CAS}$, $\overline{RAS}$ and $\overline{WE}$ define the operation to beececuted by the SDRAM. |
| BA[2:0] | Input |  | Selects which DDR2 SDRAM internal bank of four or eight is activated. |
| ODT[1:0] | Input | Active High | Asserts on-die termination for DQ, DM, DQS and $\overline{DQS}$ signals if enabled via the DDR2 SDRAM mode register. |
| A[9:0], A10/AP, A[15:11] | Input |  | During a Bank Activate command cycle, difines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high., autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle., AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge. |
| DQ[63:0] | In/Out |  | Data Input/Output pins. |
| DM[7:0] | Input | Active High | The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. |
| DQS[7:0], $\overline{DQS}$[7:0] | In/Out | Cross point | The data strobe, associated with one data byte, sourced whit data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In  Read mode, the data strobe is sourced by the DDR2 SDRAMs and is sent at leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$. If the module is to be operated in single ended strobe mode, all $\overline{DQS}$ signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed approriately. |
| $V_{DD}$, $V_{DD}$SPD,$V_{SS}$ | Supply |  | Power supplies for core, I/O, Serial Presense Detect, and ground for the module. |
| SDA | In/Out |  | This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resister must be connected to $V_{DD\ t}$o act  as a pull up. |
| SCL | Input |  | This signals is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to VDD to act as a pull up. |
| SA[1:0] | Input |  | Address pins used to select the Serial Presence Detect base address. |
| TEST | In/Out |  | The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules(SODIMMs). |

## PIN ASSIGNMENT

| Pin NO. | Front Side | Pin NO. | Back Side | Pin NO. | Front Side | Pin NO. | Back Side | Pin NO. | Front Side | Pin NO. | Back Side | Pin NO. | Front Side | Pin NO. | Back Side |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VREF | 2 | VSS | 51 | DQS2 | 52 | DM2 | 101 | A1 | 102 | A0 | 151 | DQ42 | 152 | DQ46 |
| 3 | VSS | 4 | DQ4 | 53 | VSS | 54 | VSS | 103 | VDD | 104 | VDD | 153 | DQ43 | 154 | DQ47 |
| 5 | DQ0 | 6 | DQ5 | 55 | DQ18 | 56 | DQ22 | 105 | A10/AP | 106 | BA1 | 155 | VSS | 156 | VSS |
| 7 | DQ1 | 8 | VSS | 57 | DQ19 | 58 | DQ23 | 107 | BA0 | 108 | $\overline{RAS}$ | 157 | DQ48 | 158 | DQ52 |
| 9 | VSS | 10 | DM0 | 59 | VSS | 60 | VSS | 109 | $\overline{WE}$ | 110 | $\overline{S0}$ | 159 | DQ49 | 160 | DQ53 |
| 11 | $\overline{DQS0}$ | 12 | VSS | 61 | DQ24 | 62 | DQ28 | 111 | VDD | 112 | VDD | 161 | VSS | 162 | VSS |
| 13 | DQS0 | 14 | DQ6 | 63 | DQ25 | 64 | DQ29 | 113 | $\overline{CAS}$ | 114 | ODT0 | 163 | NC,TEST | 164 | CK1 |
| 15 | VSS | 16 | DQ7 | 65 | VSS | 66 | VSS | 115 | NC/$\overline{S1}$ | 116 | A13 | 165 | VSS | 166 | $\overline{CK1}$ |
| 17 | DQ2 | 18 | VSS | 67 | DM3 | 68 | $\overline{DQS3}$ | 117 | VDD | 118 | VDD | 167 | $\overline{DQS6}$ | 168 | VSS |
| 19 | DQ3 | 20 | DQ12 | 69 | NC | 70 | DQS3 | 119 | NC/ODT1 | 120 | NC | 169 | DQS6 | 170 | DM6 |
| 21 | VSS | 22 | DQ13 | 71 | VSS | 72 | VSS | 121 | VSS | 122 | VSS | 171 | VSS | 172 | VSS |
| 23 | DQ8 | 24 | VSS | 73 | DQ26 | 74 | DQ30 | 123 | DQ32 | 124 | DQ36 | 173 | DQ50 | 174 | DQ54 |
| 25 | DQ9 | 26 | DM1 | 75 | DQ27 | 76 | DQ31 | 125 | DQ33 | 126 | DQ37 | 175 | DQ51 | 176 | DQ55 |
| 27 | VSS | 28 | VSS | 77 | VSS | 78 | VSS | 127 | VSS | 128 | VSS | 177 | VSS | 178 | VSS |
| 29 | $\overline{DQS1}$ | 30 | CK0 | 79 | CKE0 | 80 | NC/CKE1 | 129 | $\overline{DQS4}$ | 130 | DM4 | 179 | DQ56 | 180 | DQ60 |
| 31 | DQS1 | 32 | $\overline{CK0}$ | 81 | VDD | 82 | VDD | 131 | DQS4 | 132 | VSS | 181 | DQ57 | 182 | DQ61 |
| 33 | VSS | 34 | VSS | 83 | NC | 84 | NC/A15 | 133 | VSS | 134 | DQ38 | 183 | VSS | 184 | VSS |
| 35 | DQ10 | 36 | DQ14 | 85 | BA2 | 86 | NC/A14 | 135 | DQ34 | 136 | DQ39 | 185 | DM7 | 186 | $\overline{DQS7}$ |
| 37 | DQ11 | 38 | DQ15 | 87 | VDD | 88 | VDD | 137 | DQ35 | 138 | VSS | 187 | VSS | 188 | DQS7 |
| 39 | VSS | 40 | VSS | 89 | A12 | 90 | A11 | 139 | VSS | 140 | DQ44 | 189 | DQ58 | 190 | VSS |
| 41 | VSS | 42 | VSS | 91 | A9 | 92 | A7 | 141 | DQ40 | 142 | DQ45 | 191 | DQ59 | 192 | DQ62 |
| 43 | DQ16 | 44 | DQ20 | 93 | A8 | 94 | A6 | 143 | DQ41 | 144 | VSS | 193 | VSS | 194 | DQ63 |
| 45 | DQ17 | 46 | DQ21 | 95 | VDD | 96 | VDD | 145 | VSS | 146 | $\overline{DQS5}$ | 195 | SDA | 196 | VSS |
| 47 | VSS | 48 | VSS | 97 | A5 | 98 | A4 | 147 | DM5 | 148 | DQS5 | 197 | SCL | 198 | SA0 |
| 49 | $\overline{DQS2}$ | 50 | NC | 99 | A3 | 100 | A2 | 149 | VSS | 150 | VSS | 199 | VDDSPD | 200 | SA1 |

## Pin Location



Front Side

Pin #1    Pin #39    Pin #41    Pin #99



Back Side

Pin #2    Pin #40    Pin #42    Pin #200
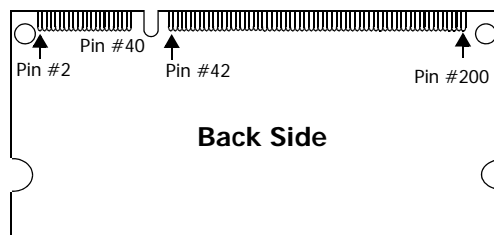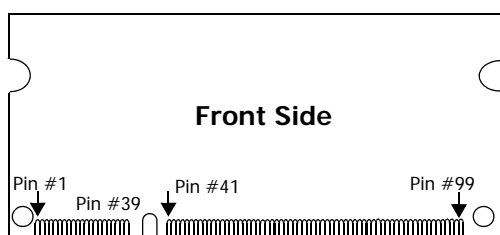
# FUNCTIONAL BLOCK DIAGRAM

## 512MB(64Mbx64) : HYMP164S64CP(R)6

# FUNCTIONAL BLOCK DIAGRAM

## 1GB(128Mbx64): HYMP112S64CP(R)6

22Ω +/-5%

ODT1
ODT0
CKE1
CKE0
/S1
/S0

**D0**

| | |
|---|---|
| DQS0 | LDQS |
| /DQS0 | /UDQS |
| DM0 | LDM |
| DQ0 | I/O 0 |
| DQ1 | I/O 1 |
| DQ2 | I/O 2 |
| DQ3 | I/O 3 |
| DQ4 | I/O 4 |
| DQ5 | I/O 5 |
| DQ6 | I/O 6 |
| DQ7 | I/O 7 |
| DQS2 | UDQS |
| /DQS2 | /UDQS |
| DM2 | UDM |
| DQ8 | I/O 8 |
| DQ9 | I/O 9 |
| DQ10 | I/O 10 |
| DQ11 | I/O 11 |
| DQ12 | I/O 12 |
| DQ13 | I/O 13 |
| DQ14 | I/O 14 |
| DQ15 | I/O 15 |

/CS  CKE  ODT

**D4**

LDQS /UDQS LDM I/O 0 I/O 1 I/O 2 I/O 3 I/O 4 I/O 5 I/O 6 I/O 7 UDQS /UDQS UDM I/O 8 I/O 9 I/O 10 I/O 11 I/O 12 I/O 13 I/O 14 I/O 15

**D2**

| | |
|---|---|
| DQS4 | LDQS |
| /DQS4 | /UDQS |
| DM4 | LDM |
| DQ32 | I/O 0 |
| DQ33 | I/O 1 |
| DQ34 | I/O 2 |
| DQ35 | I/O 3 |
| DQ36 | I/O 4 |
| DQ37 | I/O 5 |
| DQ38 | I/O 6 |
| DQ39 | I/O 7 |
| DQS5 | UDQS |
| /DQS5 | /UDQS |
| DM5 | UDM |
| DQ40 | I/O 8 |
| DQ41 | I/O 9 |
| DQ42 | I/O 10 |
| DQ43 | I/O 11 |
| DQ44 | I/O 12 |
| DQ45 | I/O 13 |
| DQ46 | I/O 14 |
| DQ47 | I/O 15 |

**D6**

LDQS /UDQS LDM I/O 0 I/O 1 I/O 2 I/O 3 I/O 4 I/O 5 I/O 6 I/O 7 UDQS /UDQS UDM I/O 8 I/O 9 I/O 10 I/O 11 I/O 12 I/O 13 I/O 14 I/O 15

**D1**

| | |
|---|---|
| DQS2 | LDQS |
| /DQS2 | /UDQS |
| DM2 | LDM |
| DQ16 | I/O 0 |
| DQ17 | I/O 1 |
| DQ18 | I/O 2 |
| DQ19 | I/O 3 |
| DQ20 | I/O 4 |
| DQ21 | I/O 5 |
| DQ22 | I/O 6 |
| DQ23 | I/O 7 |
| DQS3 | UDQS |
| /DQS3 | /UDQS |
| DM3 | UDM |
| DQ24 | I/O 8 |
| DQ25 | I/O 9 |
| DQ26 | I/O 10 |
| DQ27 | I/O 11 |
| DQ28 | I/O 12 |
| DQ29 | I/O 13 |
| DQ30 | I/O 14 |
| | I/O 15 |

**D5**

LDQS /UDQS LDM I/O 0 I/O 1 I/O 2 I/O 3 I/O 4 I/O 5 I/O 6 I/O 7 UDQS /UDQS UDM I/O 8 I/O 9 I/O 10 I/O 11 I/O 12 I/O 13 I/O 14 I/O 15

**D3**

| | |
|---|---|
| DQS6 | LDQS |
| /DQS6 | /UDQS |
| DM6 | LDM |
| DQ48 | I/O 0 |
| DQ49 | I/O 1 |
| DQ50 | I/O 2 |
| DQ51 | I/O 3 |
| DQ52 | I/O 4 |
| DQ53 | I/O 5 |
| DQ54 | I/O 6 |
| DQ55 | I/O 7 |
| DQS7 | UDQS |
| /DQS7 | /UDQS |
| DM7 | UDM |
| DQ56 | I/O 8 |
| DQ57 | I/O 9 |
| DQ58 | I/O 10 |
| DQ59 | I/O 11 |
| DQ60 | I/O 12 |
| DQ61 | I/O 13 |
| DQ62 | I/O 14 |
| DQ63 | I/O 15 |

**D7**

LDQS /UDQS LDM I/O 0 I/O 1 I/O 2 I/O 3 I/O 4 I/O 5 I/O 6 I/O 7 UDQS /UDQS UDM I/O 8 I/O 9 I/O 10 I/O 11 I/O 12 I/O 13 I/O 14 I/O 15

/CS  CKE  ODT

SCL → SCL
SA0 → A0   Serial PD   SDA ↔ SDA
SA1 → A1
A2                WP

22Ω +/-5%

BA0-BA2 → SDRAMS D0-15
A0-AN → SDRAMS D0-15
/RAS → SDRAMS D0-15
/CAS → SDRAMS D0-15
/WE → SDRAMS D0-15

CK0
/CK0          4 loads

CK1
/CK1          4 loads

$V_{DD}SPD$ → Serial PD
$V_{REF}$ → SDRAMS D0-D3
$V_{DD}$ → SDRAMS D0-D3, $V_{DD}$ and $V_{DDQ}$
$V_{SS}$ → SDRAMS D0-D3, SPD

Note:
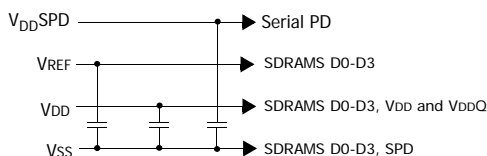1.Resistor values are 22 ohm +/-5%.

## FUNCTIONAL BLOCK DIAGRAM

### 2GB(256Mbx64) : HYMP125S64CP(R)8



Note:
1. Resistor values are 22 ohm +/-5% unless otherwide stated.
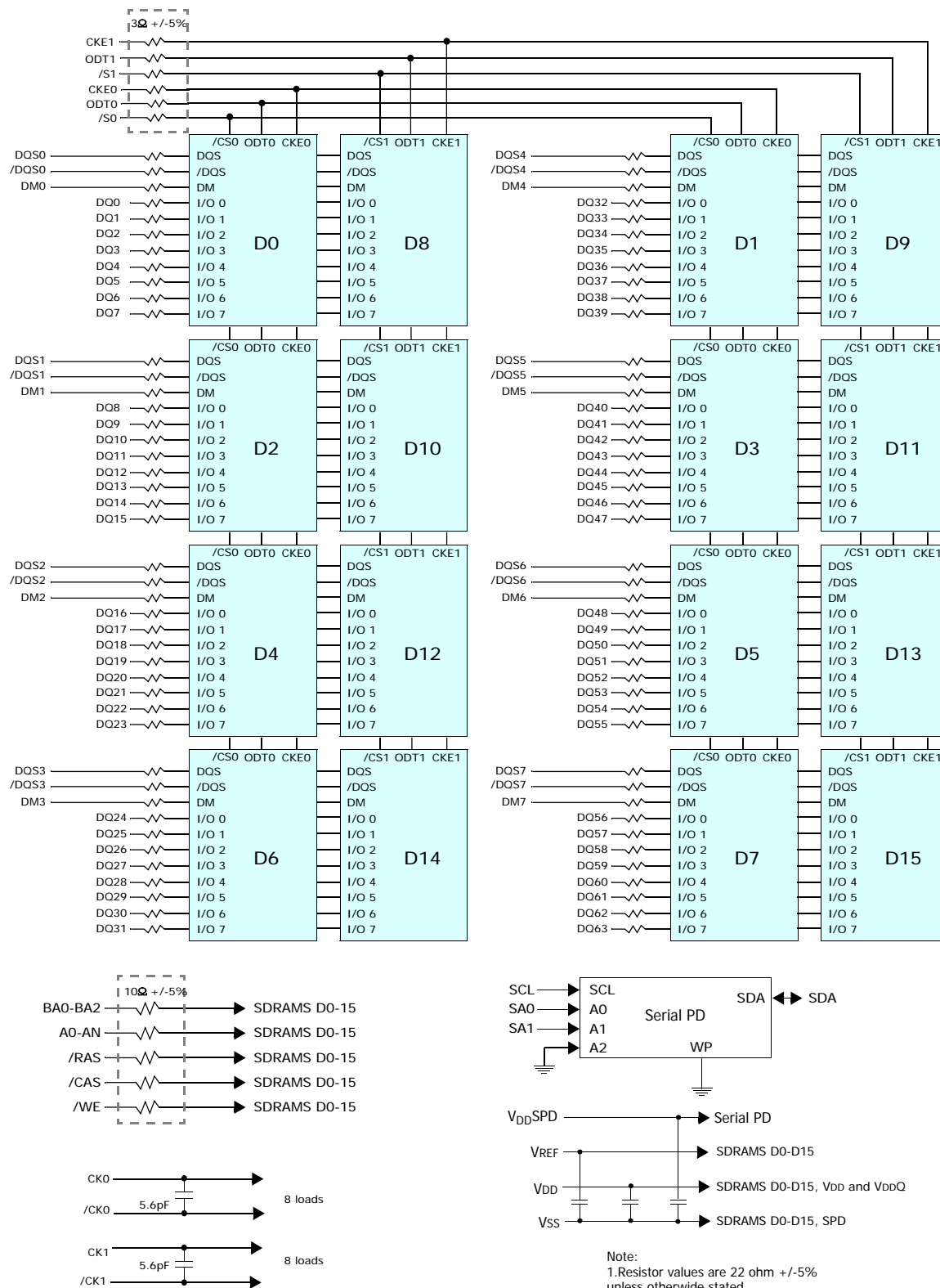
## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| Voltage on $V_{DD}$ pin relative to Vss | $V_{DD}$ | - 1.0 V ~ 2.3 V | V | 1 |
| Voltage on $V_{DDQ}$ pin relative to Vss | $V_{DDQ}$ | - 0.5 V ~ 2.3 V | V | 1 |
| Voltage on VDDL pin relative to Vss | VDDL | -0.5V ~ 2.3 V | V | 1 |
| Voltage on any pin relative to Vss | $V_{IN,}$ $V_{OUT}$ | - 0.5 V ~ 2.3 V | V | 1 |

## Operating Conditions and Environmental Parameters

| Parameter | Symbol | Rating | Units | Notes |
|---|---|---|---|---|
| DIMM Operating  temperature(ambient) | $T_{OPR}$ | 0 ~ +65 | °C | |
| Storage Temperature | $T_{STG}$ | -50 ~ +100 | °C | 1 |
| Storage Humidity(without condensation) | $H_{STG}$ | 5 to 95 | % | 1 |
| DIMM Barometric Pressure(operating & storage) | $P^{BAR}$ | 105 to 69 | K Pascal | 2 |
| DRAM Component Case Temperature Range | $T_{CASE}$ | 0 ~+95 | °C | 3 |

**Notes:**

1. Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating con ditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. If  the DRAM case temperature is Above 85oC, the Auto-Refresh command interval has to be reduced to tREFI=3.9us. For Measurement conditions of TCASE, please refer to the JEDEC document JESD51-2.

## DC OPERATING CONDITIONS (SSTL_1.8)

| Symbol | Parameter | Rating | | | Units | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| VDD | Supply Voltage | 1.7 | 1.8 | 1.9 | V | 1 |
| VDDL | Supply Voltage for DLL | 1.7 | 1.8 | 1.9 | V | 1,2 |
| VDDQ | Supply Voltage for Output | 1.7 | 1.8 | 1.9 | V | 1,2 |
| VREF | Input Reference Voltage | 0.49*VDDQ | 0.50*VDDQ | 0.51*VDDQ | mV | 3,4 |
| VTT | Termination Voltage | VREF-0.04 | VREF | VREF+0.04 | V | 5 |
| VDDSPD | EEPROM Supply Voltage | 1.8 | - | 3.3 | V | |

**Note:**

1. Min. Typ. and Max. values increase by 100mV for C3(DDR2-533 3-3-3) speed option.
2. VDDQ tracks with VDD,VDDL tracks with VDD. AC parameters are measured with VDD,VDDQ and VDD.
3. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track varia- tions in VDDQ.
4. Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).
5. VTT of transmitting device must track VREF of receiving device.

## INPUT DC LOGIC LEVEL

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| dc Input logic HIGH | $V_{IH}$(DC) | $V_{REF}$ + 0.125 | $V_{DDQ}$ + 0.3 | V | |
| dc Input logic LOW | $V_{IL}$(DC) | -0.30 | $V_{REF}$ - 0.125 | V | |

## INPUT AC LOGIC LEVEL

| Parameter | Symbol | DDR2 400/533 | | DDR2 667/800 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| AC Input logic HIGH | $V_{IH}$(AC) | $V_{REF}$ + 0.250 | - | $V_{REF}$ + 0.200 | - | V |
| AC Input logic LOW | $V_{IL}$(AC) | - | $V_{REF}$ - 0.250 | - | $V_{REF}$ - 0.200 | V |

## AC INPUT TEST CONDITIONS

| Symbol | Condition | Value | Units | Notes |
|---|---|---|---|---|
| $V_{REF}$ | Input reference voltage | 0.5 * $V_{DDQ}$ | V | 1 |
| $V_{SWING(MAX)}$ | Input signal maximum peak to peak swing | 1.0 | V | 1 |
| SLEW | Input signal minimum slew rate | 1.0 | V/ns | 2, 3 |

**Notes**:

1. Input waveform timing is referenced to the input signal crossing through the $V_{REF}$ level applied to the device under test.

2. The input signal minimum slew rate is to be maintained over the range from $V_{REF}$ to $V_{IH(ac)\ min}$ for rising edges and the range from $V_{REF}$ to $V_{IL(ac)\ max}$ for falling edges as shown in the below figure.

3. AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.



$$\text{Falling Slew} = \frac{V_{REF} - V_{IL(ac)}\ max}{\text{delta TF}}$$

$$\text{Rising Slew} = \frac{V_{IH(ac)}min - V_{REF}}{\text{delta TR}}$$
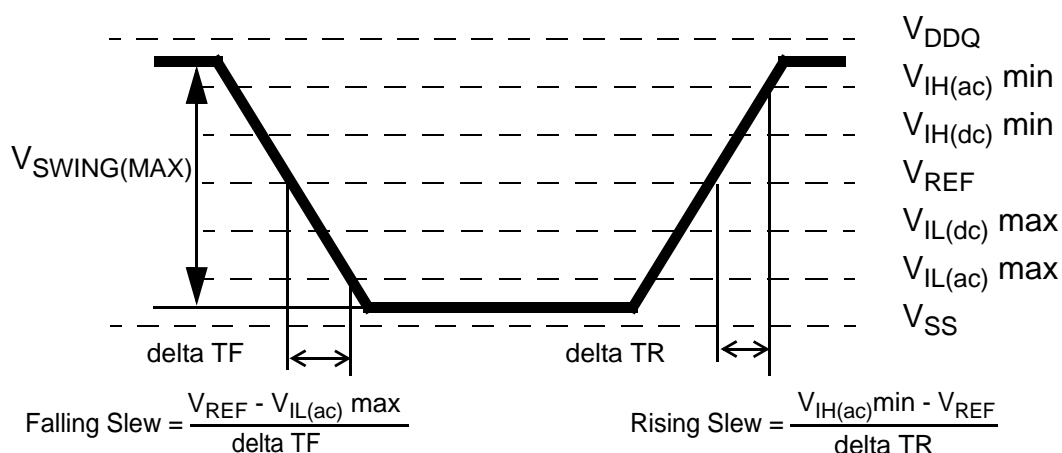
< Figure : AC Input Test Signal Waveform>

## Differential Input AC logic Level

| Symbol | Parameter | Min. | Max. | Units | Note |
|--------|-----------|------|------|-------|------|
| $V_{ID}$ (ac) | ac differential input voltage | 0.5 | $V_{DDQ} + 0.6$ | V | 1 |
| $V_{IX}$ (ac) | ac differential cross point voltage | $0.5 * V_{DDQ} - 0.175$ | $0.5 * V_{DDQ} + 0.175$ | V | 2 |

1. $V_{IN}(DC)$ specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.

2. $V_{ID}(DC)$ specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where $V_{TR}$ is the true input (such as CK, DQS, LDQS or UDQS) level and $V_{CP}$ is the complementary input (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$) level. The minimum value is equal to $V_{IH}(DC) - V_{IL}(DC)$.
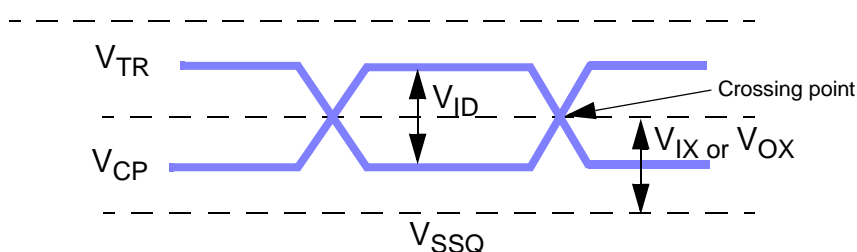


**< Differential signal levels >**

**Notes**:

1. $V_{ID}(AC)$ specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where $V_{TR}$ is the true input signal (such as CK, DQS, LDQS or UDQS) and $V_{CP}$ is the complementary input signal (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$). The minimum value is equal to $V_{IH}(AC) - V_{IL}(AC)$.

2. The typical value of $V_{IX}(AC)$ is expected to be about $0.5 * V_{DDQ}$ of the transmitting device and $V_{IX}(AC)$ is expected to track variations in $V_{DDQ}$. $V_{IX}(AC)$ indicates the voltage at whitch differential input signals must cross.

## DIFFERENTIAL AC OUTPUT PARAMETERS

| Symbol | Parameter | Min. | Max. | Units | Note |
|--------|-----------|------|------|-------|------|
| $V_{OX}$ (ac) | ac differential cross point voltage | $0.5 * V_{DDQ} - 0.125$ | $0.5 * V_{DDQ} + 0.125$ | V | 1 |

**Notes:**

1. The typical value of $V_{OX}(AC)$ is expected to be about $0.5 * V_{DDQ}$ of the transmitting device and $V_{OX}(AC)$ is expected to track variations in $V_{DDQ}$. $V_{OX}(AC)$ indicates the voltage at whitch differential output signals must cross.

## OUTPUT BUFFER LEVELS

### OUTPUT AC TEST CONDITIONS

| Symbol | Parameter | SSTL_18 | Units | Notes |
|--------|-----------|---------|-------|-------|
| $V_{OTR}$ | Output Timing Measurement Reference Level | $0.5 * V_{DDQ}$ | V | 1 |

**Notes:**

1. The VDDQ of the device under test is referenced.

### OUTPUT DC CURRENT DRIVE

| Symbol | Parameter | SSTI_18 | Units | Notes |
|--------|-----------|---------|-------|-------|
| $I_{OH(dc)}$ | Output Minimum Source DC Current | - 13.4 | mA | 1, 3, 4 |
| $I_{OL(dc)}$ | Output Minimum Sink DC Current | 13.4 | mA | 2, 3, 4 |

**Notes:**

1. $V_{DDQ}$ = 1.7 V; $V_{OUT}$ = 1420 mV. ($V_{OUT}$ - $V_{DDQ}$)/$I_{OH}$ must be less than 21 ohm for values of $V_{OUT}$ between $V_{DDQ}$ and $V_{DDQ}$ - 280 mV.

2. $V_{DDQ}$ = 1.7 V; $V_{OUT}$ = 280 mV. $V_{OUT}$/$I_{OL}$ must be less than 21 ohm for values of $V_{OUT}$ between 0 V and 280 mV.

3. The dc value of $V_{REF}$ applied to the receiving device is set to $V_{TT}$

4. The values of $I_{OH}$(dc) and $I_{OL}$(dc) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure $V_{IH}$ min plus a noise margin and $V_{IL}$ max minus a noise margin are delivered to an SSTL_18 receiver.

   The actual current values are derived by shifting the desired driver operating point along a 21 ohm load line to define a convenient driver current for measurement.

**PIN Capacitance** (VDD=1.8V,VDDQ=1.8V, TA=25°…)

### 512MB : HYMP164S64CP(R)6

| Pin | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| CK, $\overline{CK}$ | CCK | 12.5 | 15 | pF |
| CKE, ODT,CS | CI1 | 27 | 30 | pF |
| Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | CI2 | 25 | 32 | pF |
| DQ, DM, DQS, $\overline{DQS}$ | CIO | 6 | 7.5 | pF |

### 1GB : HYMP112S64CP(R)6

| Pin | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| CK, $\overline{CK}$ | CCK | 17 | 20 | pF |
| CKE, ODT,CS | CI1 | 22 | 25 | pF |
| Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | CI2 | 28.5 | 37 | pF |
| DQ, DM, DQS, $\overline{DQS}$ | CIO | 10 | 12 | pF |

### 2GB : HYMP125S64CP(R)8

| Pin | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| CK, $\overline{CK}$ | CCK | 17 | 29 | pF |
| CKE, ODT,CS | CI1 | 24 | 38 | pF |
| Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | CI2 | 31 | 56 | pF |
| DQ, DM, DQS, $\overline{DQS}$ | CIO | 7 | 12 | pF |

**Notes:**

1. Pins not under test are tied to GND.

2. These value are guaranteed by design and  tested on a sample basis only.

## IDD SPECIFICATIONS (T$_{CASE}$ : 0 to 95$^o$C)

### 512MB, 64M x 64 SO-DIMM : HYMP164S64CP(R)6

| Symbol | C4 (DDR2 533@CL4) | Y5 (DDR2 667@CL5) | S5/S6 (DDR2 800@CL5&6) | Unit | Note |
|---|---|---|---|---|---|
| IDD0 | 340 | 360 | 380 | mA | |
| IDD1 | 440 | 460 | 480 | mA | |
| IDD2P | 40 | 40 | 40 | mA | |
| IDD2Q | 108 | 120 | 128 | mA | |
| IDD2N | 140 | 160 | 180 | mA | |
| IDD3P(F) | 80 | 100 | 100 | mA | |
| IDD3P(S) | 48 | 48 | 48 | mA | |
| IDD3N | 180 | 200 | 220 | mA | |
| IDD4R | 640 | 780 | 900 | mA | |
| IDD4W | 640 | 780 | 900 | mA | |
| IDD5B | 660 | 700 | 700 | mA | |
| IDD6 | 40 | 40 | 40 | mA | 1 |
| IDD6(L) | 20 | 20 | 20 | mA | 1 |
| IDD7 | 1040 | 1060 | 1080 | mA | |

### 1GB, 128M x 64 SO-DIMM : HYMP112S64CP(R)6

| Symbol | C4 (DDR2 533@CL4) | Y5 (DDR2 667@CL5) | S5/S6 (DDR2 800@CL5&6) | Unit | Note |
|---|---|---|---|---|---|
| IDD0 | 520 | 560 | 600 | mA | |
| IDD1 | 620 | 660 | 700 | mA | |
| IDD2P | 80 | 80 | 80 | mA | |
| IDD2Q | 216 | 240 | 256 | mA | |
| IDD2N | 280 | 320 | 360 | mA | |
| IDD3P(F) | 160 | 200 | 200 | mA | |
| IDD3P(S) | 96 | 96 | 96 | mA | |
| IDD3N | 360 | 400 | 440 | mA | |
| IDD4R | 820 | 980 | 1120 | mA | |
| IDD4W | 820 | 980 | 1120 | mA | |
| IDD5B | 840 | 900 | 920 | mA | |
| IDD6 | 80 | 80 | 80 | mA | 1 |
| IDD6(L) | 40 | 40 | 40 | mA | 1 |
| IDD7 | 1220 | 1260 | 1300 | mA | |

**Notes:**

1. IDD6 current values are guaranteed up to Tcase of 85°… max.

**2GB, 256M x 64 SO-DIMM : HYMP125S64CP(R)8**

| Symbol | C4<br>(DDR2 533@CL4) | Y5<br>(DDR2 667@CL5) | S5/S6<br>(DDR2 800@CL5&6) | Unit | Note |
|---|---|---|---|---|---|
| IDD0 | 840 | 960 | 1040 | mA | |
| IDD1 | 920 | 1040 | 1120 | mA | |
| IDD2P | 160 | 160 | 160 | mA | |
| IDD2Q | 432 | 480 | 512 | mA | |
| IDD2N | 560 | 640 | 720 | mA | |
| IDD3P(F) | 320 | 400 | 400 | mA | |
| IDD3P(S) | 192 | 192 | 192 | mA | |
| IDD3N | 640 | 800 | 880 | mA | |
| IDD4R | 1320 | 1600 | 1800 | mA | |
| IDD4W | 1320 | 1600 | 1800 | mA | |
| IDD5B | 1640 | 1800 | 1840 | mA | |
| IDD6 | 160 | 160 | 160 | mA | 1 |
| IDD6(L) | 80 | 80 | 80 | mA | 1 |
| IDD7 | 1720 | 1840 | 1920 | mA | |

**Notes:**

1. IDD6 current values are guaranteed up to Tcase of 85°C max.

## IDD Measurement Conditions

| Symbol | Conditions | | Units |
|---|---|---|---|
| IDD0 | **Operating one bank active-precharge current**; $^tCK = {^tCK(IDD)}$, $^tRC = {^tRC(IDD)}$, $^tRAS = {^tRAS}$-min(IDD);CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;Address bus inputs are SWITCHING;Data bus inputs are SWITCHING | | mA |
| IDD1 | **Operating one bank active-read-precharge curren** ; IOUT = 0mA;BL = 4, CL = CL(IDD), AL = 0; $^tCK = {^tCK(IDD)}$, $^tRC = {^tRC (IDD)}$, $^tRAS = {^tRASmin(IDD)}$, $^tRCD = {^tRCD(IDD)}$ ; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands ; Address bus inputs are SWITCHING ; Data pattern is same as IDD4W | | mA |
| IDD2P | **Precharge power-down current** ; All banks idle ; $^tCK = {^tCK(IDD)}$ ; CKE is LOW ; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | | mA |
| IDD2Q | **Precharge quiet standby current**;All banks idle; $^tCK = {^tCK(IDD)}$;CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | | mA |
| IDD2N | **Precharge standby current**; All banks idle; $^tCK = {^tCK(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | mA |
| IDD3P | **Active power-down current**; All banks open; $^tCK = {^tCK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOAT-ING | Fast PDN Exit MRS(12) = 0 | mA |
| | | Slow PDN Exit MRS(12) = 1 | mA |
| IDD3N | **Active standby current**; All banks open; $^tCK = {^tCK(IDD)}$, $^tRAS = {^tRASmax(IDD)}$, $^tRP = {^tRP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | mA |
| IDD4W | **Operating burst write current**; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $^tCK = {^tCK(IDD)}$, $^tRAS = {^tRASmax(IDD)}$, $^tRP = {^tRP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | mA |
| IDD4R | **Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $^tCK = {^tCK(IDD)}$, $^tRAS = {^tRASmax(IDD)}$, $^tRP = {^tRP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING;; Data pattern is same as IDD4W | | mA |
| IDD5B | **Burst refresh current**; $^tCK = {^tCK(IDD)}$; Refresh command at every $^tRFC(IDD)$ interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | mA |
| IDD6 | **Self refresh current**; CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING. IDD6 current values are guaranted up to Tcase of 85 ℃ max. | | mA |
| IDD7 | **Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = $^tRCD(IDD)$-1*$^tCK(IDD)$; $^tCK = {^tCK(IDD)}$, $^tRC = {^tRC(IDD)}$, $^tRRD = {^tRRD(IDD)}$, $^tRCD = 1*^tCK(IDD)$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; - Refer to the following page for detailed timing conditions | | mA |

**Notes:**

1. IDD specifications are tested after the device is properly initialized

2. Input slew rate is specified by AC Parametric Test Condition

3. IDD parameters are specified with ODT disabled.

4. Data bus consists of DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, LDQS, $\overline{LDQS}$, UDQS, and $\overline{UDQS}$. IDD values must be met with all combinations of EMRS bits 10 and 11.

5. Definitions for IDD

   LOW is defined as Vin £ VILAC(max)

   HIGH is defined as Vin Š VIHAC(min)

   STABLE is defined as inputs stable at a HIGH or LOW level

   FLOATING is defined as inputs at VREF = VDDQ/2

   SWITCHING is defined as: inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and

       control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock)

           for DQ signals not including masks or strobes.

## Electrical Characteristics & AC Timings

### Speed Bins and CL,tRCD,tRP,tRC and tRAS for Corresponding Bin

| Speed | DDR2-800 (S5) | DDR2-800 (S6) | DDR2-667 (Y5) | DDR2-533 (C4) | DDR2-400 (E3) | Unit |
|---|---|---|---|---|---|---|
| Bin(CL-tRCD-tRP) | 5-5-5 | 6-6-6 | 5-5-5 | 4-4-4 | 3-3-3 | |
| Parameter | min | min | min | min | min | |
| CAS Latency | 5 | 6 | 5 | 4 | 3 | tCK |
| tRCD | 12.5 | 15 | 15 | 15 | 15 | ns |
| tRP | 12.5 | 15 | 15 | 15 | 15 | ns |
| tRAS | 45 | 45 | 45 | 45 | 40 | ns |
| tRC | 57.5 | 60 | 60 | 60 | 55 | ns |

### AC Timing Parameters by Speed Grade

| Parameter | Symbol | DDR2-400 Min | DDR2-400 Max | DDR2-533 Min | DDR2-533 Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| Data-Out edge to Clock edge Skew | tAC | -600 | 600 | -500 | 500 | ps | |
| DQS-Out edge to Clock edge Skew | tDQSCK | -500 | 500 | -450 | 450 | ns | |
| Clock High Level Width | tCH | 0.45 | 0.55 | 0.45 | 0.55 | CK | |
| Clock Low Level Width | tCL | 0.45 | 0.55 | 0.45 | 0.55 | CK | |
| Clock Half Period | tHP | min (tCL,tCH) | - | min (tCL,tCH) | - | ns | |
| System Clock Cycle Time | tCK | 5000 | 8000 | 3750 | 8000 | ps | |
| DQ and DM input setup time | tDS | 150 | - | 100 | - | ps | 1 |
| DQ and DM input hold time | tDH | 275 | - | 225 | - | ps | 1 |
| DQ and DM input setup time(single-ended strobe) | tDS1 | 25 | - | -25 | - | ps | 1 |
| DQ and DM input hold time(single-ended strobe) | tDH1 | 25 | - | -25 | - | ps | 1 |
| Control & Address input Pulse Width for each input | tIPW | 0.6 | - | 0.6 | - | tCK | |
| DQ and DM input pulse witdth for each input pulse width for each input | tDIPW | 0.35 | - | 0.35 | - | tCK | |
| Data-out high-impedance window from CK, /CK | tHZ | - | tAC max | - | tAC max | ps | |
| DQS low-impedance time from CK/$\overline{CK}$ | tLZ(DQS) | tAC min | tAC max | tAC min | tAC max | ps | |
| DQ low-impedance time from CK/$\overline{CK}$ | tLZ(DQ) | 2*tAC min | tAC max | 2*tAC min | tAC max | ps | |
| DQS-DQ skew for DQS and associated DQ signals | tDQSQ | - | 350 | - | 300 | ps | |
| DQ hold skew factor | tQHS | - | 450 | - | 400 | ps | |
| DQ/DQS output hold time from DQS | tQH | tHP - tQHS | - | tHP - tQHS | - | ps | |
| First DQS latching transition to associated clock edge | tDQSS | -0.25 | +0.25 | -0.25 | +0.25 | tCK | |
| DQS input high pulse width | tDQSH | 0.35 | - | 0.35 | - | tCK | |
| DQS input low pulse width | tDQSL | 0.35 | - | 0.35 | - | tCK | |
| DQS falling edge to CK setup time | tDSS | 0.2 | - | 0.2 | - | tCK | |
| DQS falling edge hold time from CK | tDSH | 0.2 | - | 0.2 | - | tCK | |
| Mode register set command cycle time | tMRD | 2 | - | 2 | - | tCK | |
| Write preamble | tWPRE | 0.35 | - | 0.35 | - | tCK | |
| Write postamble | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | tCK | |
| Data-Out edge to Clock edge Skew | tAC | -600 | 600 | -500 | 500 | ps | |
| Address and control input setup time | tIS | 350 | - | 250 | - | ps | |

*- Continued -*

| Parameter | Symbol | DDR2-400 | | DDR2-533 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Address and control input hold time | tIH | 475 | - | 375 | - | ps | |
| Read preamble | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | tCK | |
| Read postamble | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | tCK | |
| Auto-Refresh to Active/Auto-Refresh command period | tRFC | 127.5 | - | 127.5 | - | ns | |
| Row Active to Row Active Delay for 1KB page size | tRRD | 7.5 | - | 7.5 | - | ns | |
| Row Active to Row Active Delay for 2KB page size | tRRD | 10 | - | 10 | - | ns | |
| Four Activate Window for 1KB page size | tFAW | 37.5 | - | 37.5 | - | ns | |
| Four Activate Window for 2KB page size | tFAW | 50 | - | 50 | - | ns | |
| $\overline{CAS}$ to $\overline{CAS}$ command delay | tCCD | 2 | | 2 | | tCK | |
| Write recovery time | tWR | 15 | - | 15 | - | ns | |
| Auto Precharge Write Recovery + Precharge Time | tDAL | tWR+tRP | - | tWR+tRP | - | tCK | |
| Write to Read Command Delay | tWTR | 10 | - | 7.5 | - | ns | |
| Internal read to precharge command delay | tRTP | 7.5 | | 7.5 | | ns | |
| Exit self refresh to a non-read command | tXSNR | tRFC + 10 | | tRFC + 10 | | ns | |
| Exit self refresh to a read command | tXSRD | 200 | - | 200 | - | tCK | |
| Exit precharge power down to any non-read command | tXP | 2 | - | 2 | - | tCK | |
| Exit active power down to read command | tXARD | 2 | | 2 | | tCK | |
| Exit active power down to read command (Slow exit, Lower power) | tXARDS | 6 - AL | | 6 - AL | | tCK | |
| CKE minimum pulse width (high and low pulse width) | tCKE | 3 | | 3 | | tCK | |
| ODT turn-on delay | tAOND | 2 | 2 | 2 | 2 | tCK | |
| ODT turn-on | tAON | tAC(min) | tAC(max)+1 | tAC(min) | tAC(max)+1 | ns | |
| ODT turn-on(Power-Down mode) | tAONPD | tAC(min)+2 | 2tCK+tAC(max)+1 | tAC(min)+2 | 2tCK+tAC(max)+1 | ns | |
| ODT turn-off delay | tAOFD | 2.5 | 2.5 | 2.5 | 2.5 | tCK | |
| ODT turn-off | tAOF | tAC(min) | tAC(max)+0.6 | tAC(min) | tAC(max)+0.6 | ns | |
| ODT turn-off (Power-Down mode) | tAOFPD | tAC(min)+2 | 2.5tCK+tAC(max)+1 | tAC(min)+2 | 2.5tCK+tAC(max)+1 | ns | |
| ODT to power down entry latency | tANPD | 3 | | 3 | | tCK | |
| ODT power down exit latency | tAXPD | 8 | | 8 | | tCK | |
| OCD drive mode output delay | tOIT | 0 | 12 | 0 | 12 | ns | |
| Minimum time clocks remains ON after CKE asynchronously drops LOW | tDelay | tIS+tCK+tIH | | tIS+tCK+tIH | | ns | |
| Average periodic Refresh Interval | tREFI | - | 7.8 | - | 7.8 | us | 2 |
| | tREFI | - | 3.9 | - | 3.9 | us | 3 |

**Notes:**

1. For details and notes, please refer to the relevant Hynix component datasheet(HY5PS1G8(16)31CFP).

2. 0°C $\leq$ T$_{CASE}$ $\leq$ 85°C

3. 85°C $<$ T$_{CASE}$ $\leq$ 95°C

| Parameter | Symbol | DDR2-667 | | DDR2-800 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | min | max | min | max | | |
| DQ output access time from CK/$\overline{CK}$ | tAC | -450 | +450 | -400 | +400 | ps | |
| DQS output access time from CK/$\overline{CK}$ | tDQSCK | -400 | +400 | -350 | +350 | ps | |
| CK high-level width | tCH | 0.45 | 0.55 | 0.48 | 0.52 | tCK | |
| CK low-level width | tCL | 0.45 | 0.55 | 0.48 | 0.52 | tCK | |
| CK half period | tHP | min(tCL, tCH) | - | min(tCL, tCH) | - | ps | |
| Clock cycle time, CL=x | tCK | 3000 | 8000 | 2500 | 8000 | ps | |
| DQ and DM input setup time (differential strobe) | tDS | 100 | - | 50 | - | ps | 1 |
| DQ and DM input hold time (differential strobe) | tDH | 175 | - | 125 | - | ps | 1 |
| Control & Address input pulse width for each input | tIPW | 0.6 | - | 0.6 | - | tCK | |
| DQ and DM input pulse width for each input | tDIPW | 0.35 | - | 0.35 | - | tCK | |
| Data-out high-impedance time from CK/$\overline{CK}$ | tHZ | - | tAC max | | tAC max | ps | |
| DQS low-impedance time from CK/$\overline{CK}$ | tLZ(DQS) | tAC min | tAC max | tAC min | tAC max | ps | |
| DQ low-impedance time from CK/$\overline{CK}$ | tLZ(DQ) | 2*tAC min | tAC max | 2*tAC min | tAC max | ps | |
| DQS-DQ skew for DQS and associated DQ signals | tDQSQ | - | 240 | - | 240 | ps | |
| DQ hold skew factor | tQHS | - | 340 | - | 300 | ps | |
| DQ/DQS output hold time from DQS | tQH | tHP - tQHS | - | tHP - tQHS | - | ps | |
| First DQS latching transition to associated clock edge | tDQSS | -0.25 | +0.25 | -0.25 | +0.25 | tCK | |
| DQS input high pulse width | tDQSH | 0.35 | - | 0.35 | - | tCK | |
| DQS input low pulse width | tDQSL | 0.35 | - | 0.35 | - | tCK | |
| DQS falling edge to CK setup time | tDSS | 0.2 | - | 0.2 | - | tCK | |
| DQS falling edge hold time from CK | tDSH | 0.2 | - | 0.2 | - | tCK | |
| Mode register set command cycle time | tMRD | 2 | - | 2 | - | tCK | |
| Write preamble | tWPRE | 0.35 | - | 0.35 | - | tCK | |
| Write postamble | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | tCK | |
| Address and control input setup time | tIS | 200 | - | 175 | - | ps | |
| Address and control input hold time | tIH | 275 | - | 250 | - | ps | |
| Read preamble | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | tCK | |
| Read postamble | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | tCK | |
| Activate to precharge command | tRAS | 45 | 70000 | 45 | 70000 | ns | |
| Row Active to Row Active Delay for 1KB page size | tRRD | 7.5 | - | 7.5 | - | ns | |
| Row Active to Row Active Delay for 2KB page size | tRRD | 10 | - | 10 | - | ns | |
| Four Active Window for 1KB page size products | tFAW | 37.5 | - | 35 | - | ns | |
| Four Active Window for 2KB page size products | tFAW | 50 | - | 45 | - | ns | |

*- continued -*

| Parameter | Symbol | DDR2-667 | | DDR2-800 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | min | max | min | max | | |
| CAS to CAS command delay | tCCD | 2 | | 2 | - | tCK | |
| Write recovery time | tWR | 15 | - | 15 | - | ns | |
| Auto precharge write recovery + precharge time | tDAL | WR+tRP | - | WR+tRP | - | tCK | |
| Internal write to read command delay | tWTR | 7.5 | - | 7.5 | - | ns | |
| Internal read to precharge command delay | tRTP | 7.5 | | 7.5 | - | ns | |
| Exit self refresh to a non-read command | tXSNR | tRFC + 10 | - | tRFC + 10 | - | ns | |
| Exit self refresh to a read command | tXSRD | 200 | - | 200 | - | tCK | |
| Exit precharge power down to any non-read command | tXP | 2 | - | 2 | - | tCK | |
| Exit active power down to read command | tXARD | 2 | - | 2 | - | tCK | |
| Exit active power down to read command (Slow exit, Lower power) | tXARDS | 7 - AL | - | 8 - AL | - | tCK | |
| CKE minimum pulse width (high and low pulse width) | tCKE | 3 | - | 3 | - | tCK | |
| ODT turn-on delay | tAOND | 2 | 2 | 2 | 2 | tCK | |
| ODT turn-on | tAON | tAC(min) | tAC(max)+0.7 | tAC(min) | tAC(max)+0.7 | ns | |
| ODT turn-on(Power-Down mode) | tAONPD | tAC(min)+2 | 2tCK+ tAC(max)+1 | tAC(min)+2 | 2tCK+ tAC(max)+1 | ns | |
| ODT turn-off delay | tAOFD | 2.5 | 2.5 | 2.5 | 2.5 | tCK | |
| ODT turn-off | tAOF | tAC(min) | tAC(max)+ 0.6 | tAC(min) | tAC(max)+ 0.6 | ns | |
| ODT turn-off (Power-Down mode) | tAOFPD | tAC(min)+2 | 2.5tCK+ tAC(max)+1 | tAC(min)+2 | 2.5tCK+ tAC(max)+1 | ns | |
| ODT to power down entry latency | tANPD | 3 | - | 3 | - | tCK | |
| ODT power down exit latency | tAXPD | 8 | | 8 | | tCK | |
| OCD drive mode output delay | tOIT | 0 | 12 | 0 | 12 | ns | |
| Minimum time clocks remains ON after CKE asynchronously drops LOW | tDelay | tIS+tCK+tIH | - | tIS+tCK+tIH | - | ns | |
| Average periodic Refresh Interval | tREFI | - | 7.8 | - | 7.8 | us | 2 |
| | tREFI | - | 3.9 | - | 3.9 | us | 3 |

**Notes:**

1. For details and notes, please refer to the relevant Hynix component datasheet(HY5PS1G8(16)31CFP).

2. $0°C \leq T_{CASE} \leq 85°C$

3. $85°C < T_{CASE} \leq 95°C$

# PACKAGE OUTLINE

## 64Mx64 - HYMP164S64CP(R)6
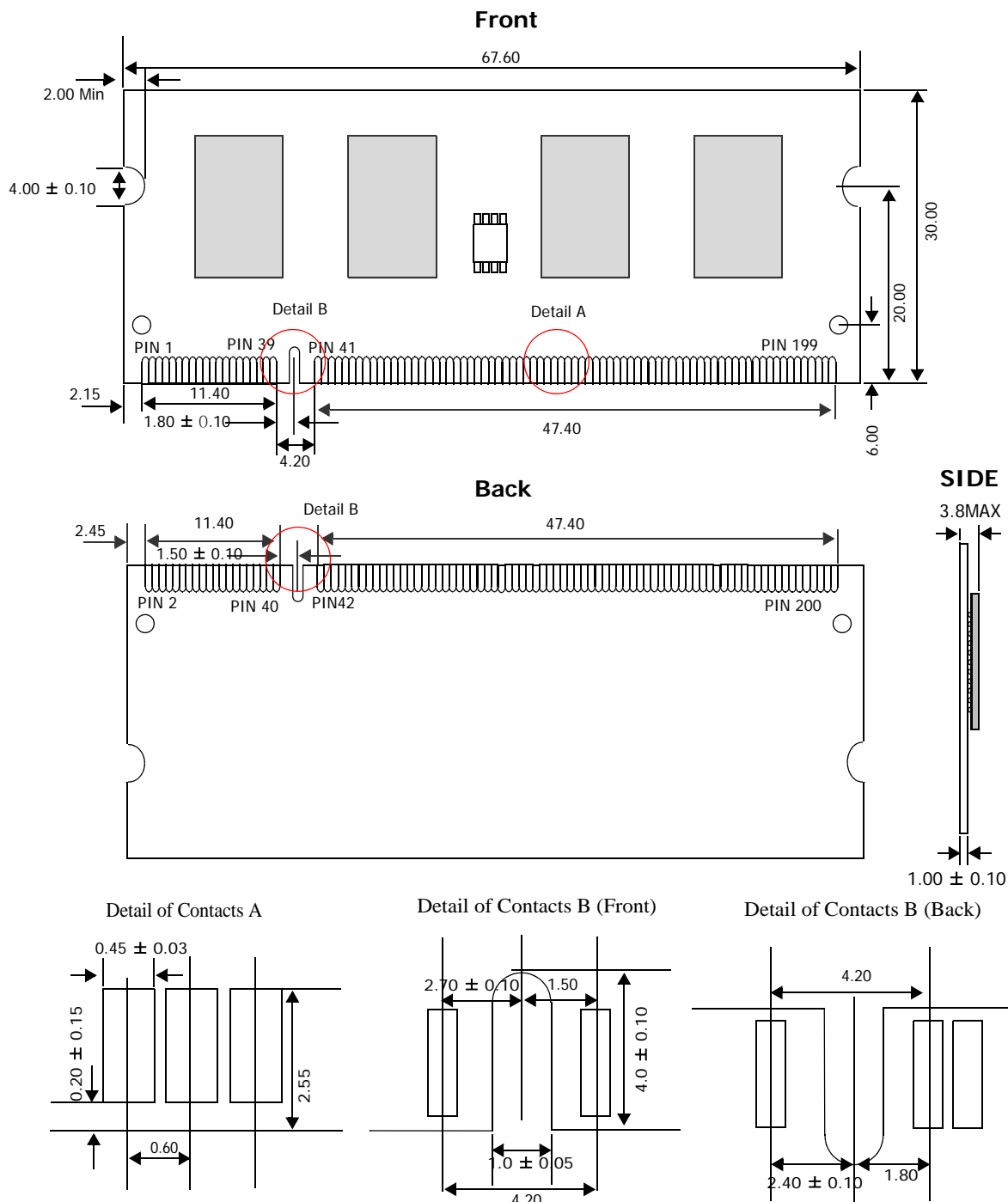
**Front**

67.60

2.00 Min

4.00 ± 0.10

30.00

20.00

Detail B

Detail A

PIN 1    PIN 39    PIN 41    PIN 199

2.15

11.40

1.80 ± 0.10

4.20

47.40

6.00

**Back**

Detail B

2.45

11.40    47.40

1.50 ± 0.10

PIN 2    PIN 40    PIN42    PIN 200

**SIDE**

3.8MAX

1.00 ± 0.10

Detail of Contacts A

0.45 ± 0.03

0.20 ± 0.15

2.55

0.60

Detail of Contacts B (Front)

2.70 ± 0.10    1.50

4.0 ± 0.10

1.0 ± 0.05

4.20

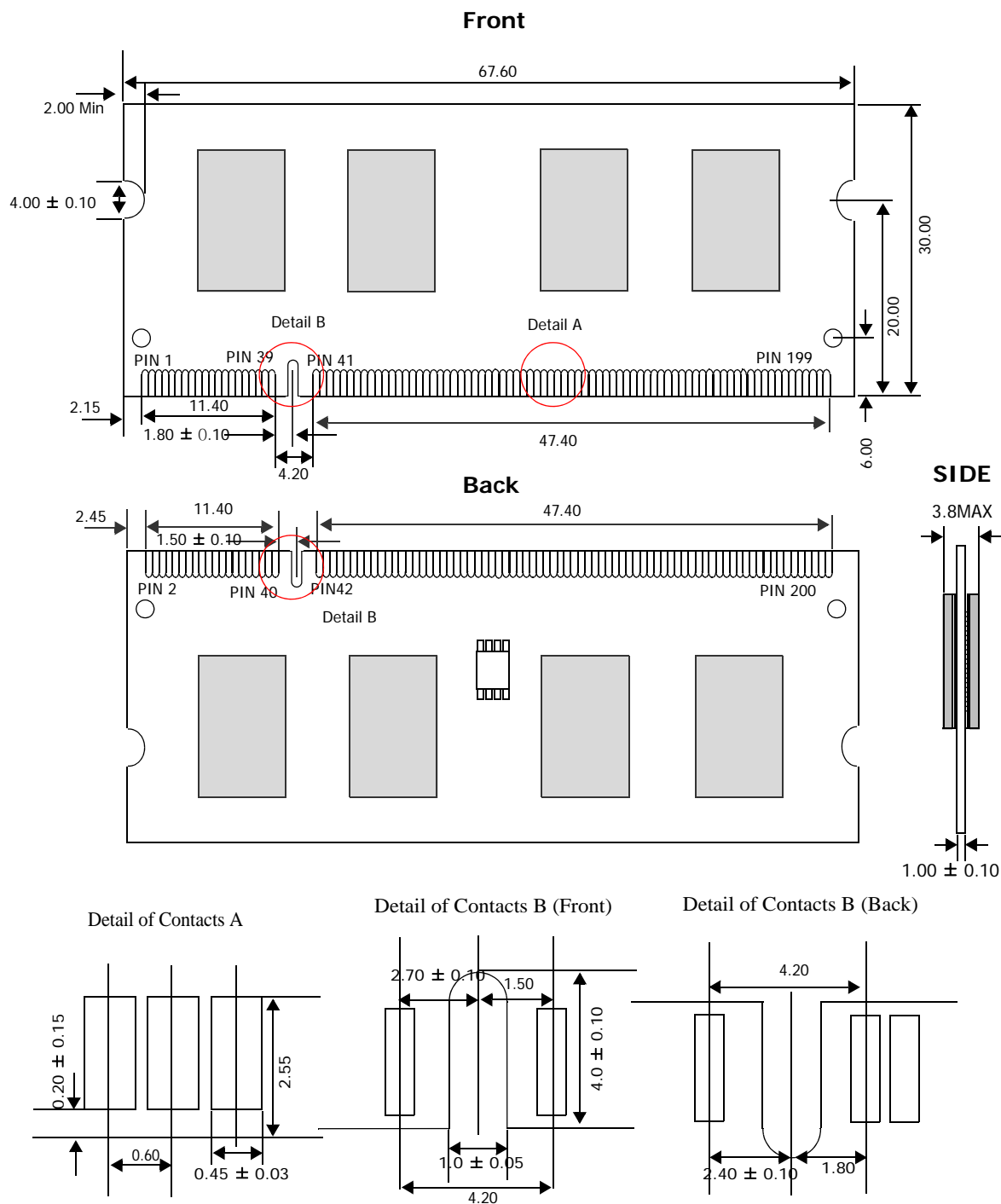Detail of Contacts B (Back)

4.20

2.40 ± 0.10    1.80

Note:
1. All dimensions are in millimeters.
2. All outline dimensions and tolerances follow the JEDEC standard.

# PACKAGE OUTLINE

### 128Mx64 -  HYMP112S64CP(R)6

**Front**



67.60

2.00 Min

4.00 ± 0.10

30.00

20.00

Detail B

Detail A

PIN 1

PIN 39    PIN 41

PIN 199

2.15

11.40

1.80 ± 0.10

47.40

4.20

6.00

**Back**

11.40    47.40

2.45

1.50 ± 0.10

PIN 2    PIN 40    PIN42

PIN 200

Detail B

**SIDE**

3.8MAX

1.00 ± 0.10

Detail of Contacts A

0.20 ± 0.15

2.55

0.60

0.45 ± 0.03

Detail of Contacts B (Front)

2.70 ± 0.10    1.50

4.0 ± 0.10

1.0 ± 0.05

4.20

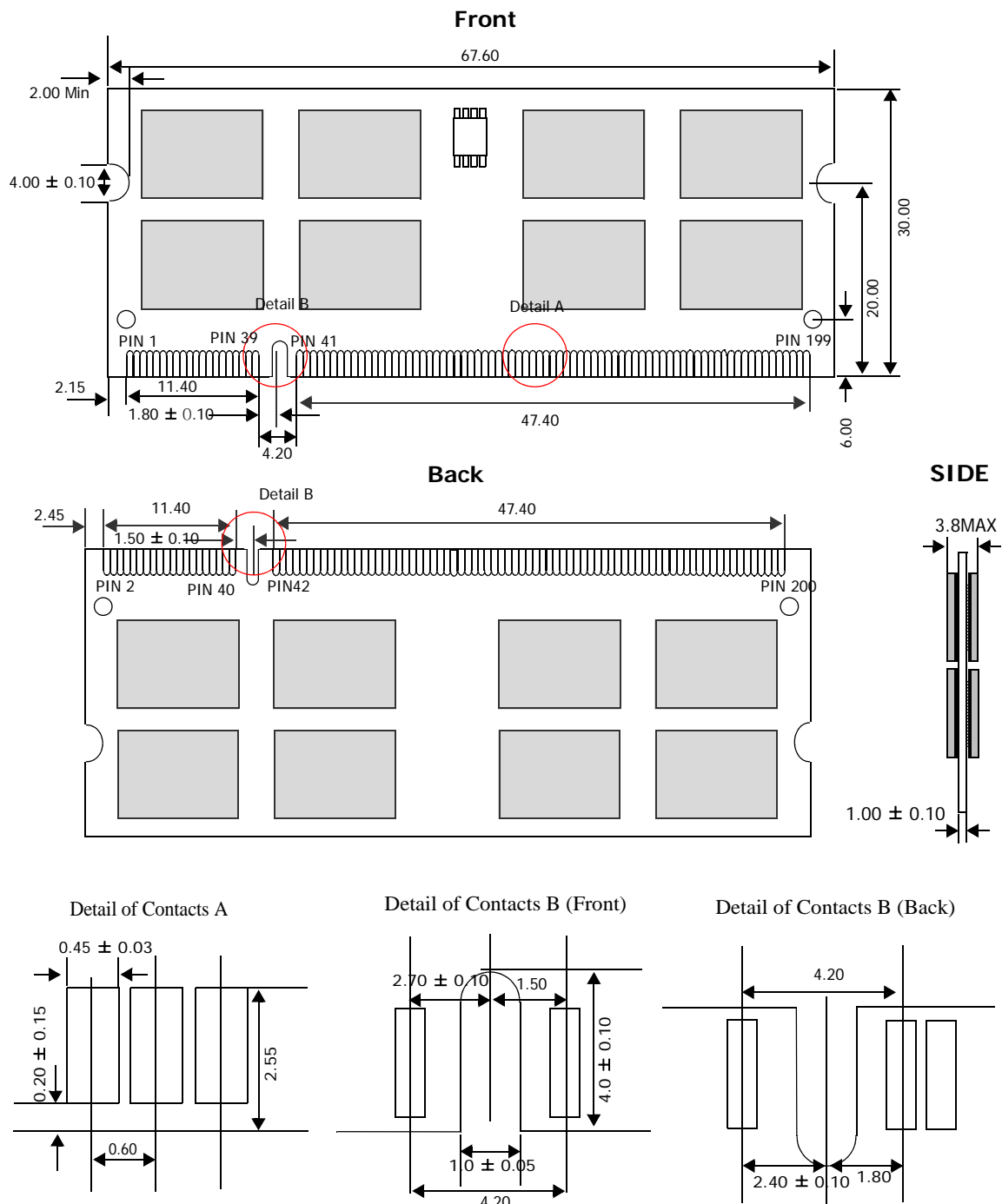Detail of Contacts B (Back)

4.20

2.40 ± 0.10    1.80

Note:
1. All dimensions are in millimeters.
2. All outline dimensions and tolerances follow the JEDEC standard.

## PACKAGE OUTLINE

### 256Mx64 - HYMP125S64CP(R)8

**Front**



**Back**

**SIDE**

Detail of Contacts A          Detail of Contacts B (Front)          Detail of Contacts B (Back)

Note:
1. All dimensions are in millimeters.
2. All outline dimensions and tolerances follow the JEDEC standard.

## REVISION HISTORY

| Revision | History | Date |
|:---:|:---|:---:|
| 0.1 | Initial data sheet released | Jan. 2007 |
| 0.2 | Updated SPEED GRADE & KEY PARAMETERS | Feb. 2007 |
| 0.3 | Updated IDD Spec and corrected typos | May 2007 |
| 0.4 | IDD updated | Jun. 2007 |
| 0.5 | DIMM outline corrected | Aug. 2007 |
| 0.6 | S6 items added | Oct. 2007 |
| 0.7 | DIMM outline corrected | Jan. 2008 |
| 0.8 | DIMM outline & typo corrected & Halogen-free included | Apr. 2008 |
| 1.0 | Udated AC Timing Parameters by Speed Grade | Dec. 2009 |