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AR8031 Integrated 10/100/1000 Gigabit Ethernet Transceiver

General Description

The AR8031 is part of the Arctic family of devices — which includes the AR8031, AR8033, and AR8035. The AR8031 is Atheros' 4th generation, single port, 10/100/1000 Mbps, Tri-speed Ethernet PHY. It supports both RGMII and SGMII interfaces to the MAC

The AR8031 provides a low power, low BOM (Bill of Materials) cost solution for comprehensive applications including enterprise, carrier and home networks such as CPE, home gateway, enterprise switch, carrier switch/router, mobile base station and base station controller, optical module and media converter, industry automation and measurement, etc.

The AR8031 integrates Atheros Green Ethos^{tm} power saving technologies and significantly saves power not only during the work time, but also overtime. Atheros Green Ethos^{tm} power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. The AR8031 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary SmartEEE, which allows legacy MAC/SoC devices without 802.3az support to functions as the complete 802.3az system. Further, the AR8031 supports Wake-on-LAN (WoL) feature to be able to help manage and regulate total system power requirements.

The AR8031 embeds CDT (Cable Diagnostics Test) technology on-chip which allows customers to measure cable length, detect the cable status, and identify remote and local PHY malfunctions, bad or marginal patch cord segments or connectors. Some of the possible problems that can be detected include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and a bad transformer.

The AR8031 requires only a single, 3.3V power supply. On-chip regulators provide all the other required voltages. It integrates the termination R/C circuitry on both the MAC interfaces (RGMII/ SGMII) and the serial resistors for the line side.

The AR8031 device also incorporates an optional 1.25 GHz SERDES. This serial interface may be connected directly to a fiber-optic transceiver for 1000Base-X/100Base-FX mode.

The AR8031 supports both IEEE 1588 v2 and synchronous Ethernet to offer a complete time synchronization solution to meet the next generation network requirements. The key new features supported by the device are:

- clock synchronization between slave and grandmaster by the exchange of PTP packets. Supports IEEE 1588 v2 by offering a 1588 packet parser, accurate time-stamping and insertion to support both one-step and two-step clock modes.
- Supports Synchronous Ethernet by offering configurable recovered clock output from data on the network-line side.

The AR8031 supports IEEE 802.3az Energy Efficient Ethernet (EEE) 2010 standard. The key features supported by the device are:

- 10Base-Te PHY uses reduced transmit amplitude.
- 100Base-Tx and 1000Base-T use Low Power Idle (LPI) mode to turn off unused analog and digital blocks to save power while data traffic is in idle.

Features

- 10/100/1000 Base-T IEEE 802.3 compliant
- Supports 1000 Base-T PCS and auto-negotiation with next page support
- Supports RGMII and/or SGMII interfaces to MAC devices
- Supports Fiber and Copper combo mode when MAC interface works in RGMII mode
- Supports additional IEEE 1000Base-X and 100Base-FX with Integrated Serdes
- RGMII timing modes support internal delay and external delay on both Rx and Tx paths
- Supports Atheros Green Ethos^{tm} power saving modes with internal automatic DSP power saving scheme
- Supports 802.3az (Energy Efficient Ethernet)

- Supports Atheros proprietary SmartEEE, which allows legacy MAC/SoC devices without 802.3az support to functions as the complete 802.3az system
- Supports Wake-on-LAN (WoL) to detect magic packet and notify the sleeping system to wake up
- Fully integrated digital adaptive equalizers, echo cancellers, and near end crosstalk (NEXT) cancellers
- Complete 1588v2 support for both one step and two step clock modes.
- Pulse Per Second (PPS) output for local synchronization reference
- Supports Synchronous Ethernet with selectable recovered clock output
- Robust Cable Discharge Event (CDE) protection of ±6KV
- Error-free operation over up to 140 meters of CAT5 cable
- Automatic channel swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- Jumbo Frame support up to 10KB (full duplex)
- Software programmable LED modes
- Multiple loopback modes for diagnostics
- Robust Surge Protection with ±750V/differential mode and ±2KV/common mode
- Cable Diagnostic Test (CDT) with cable length detection of ±1.0 meter accuracy
- Single power supply: 3.3V, optional for external regulator for core voltage
- 6mm x 6mm, 48-pin QFN package

AR8031 Functional Block Diagram

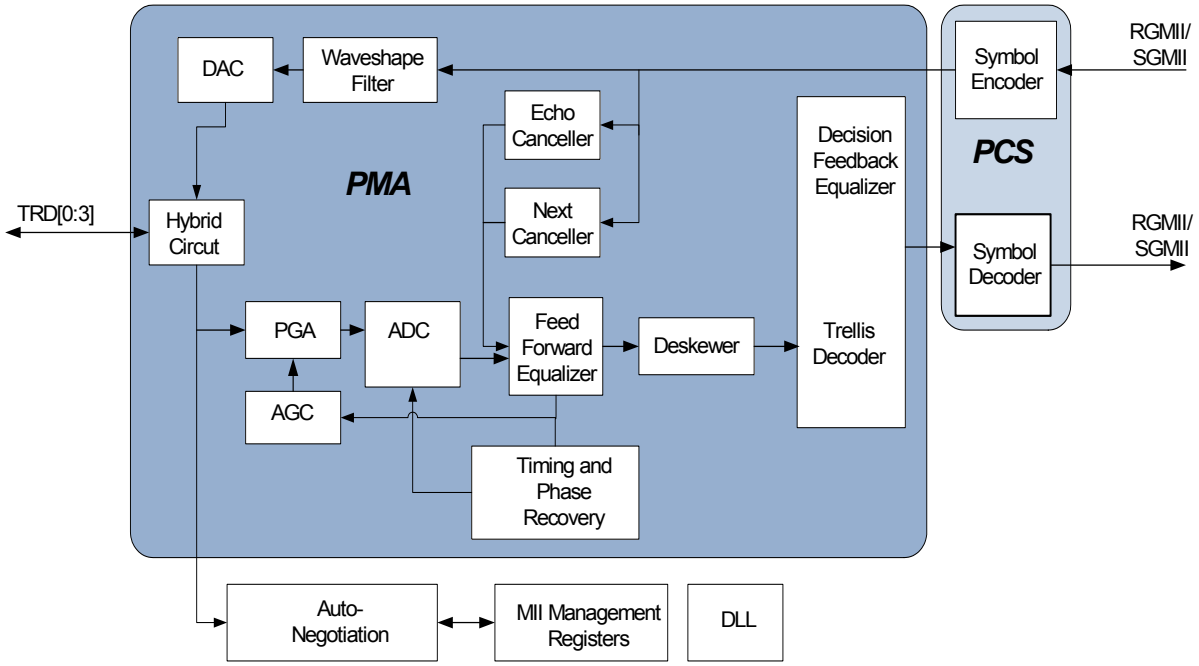


Table of Contents

1. Pin Descriptions

This section contains a package pinout for the AR8031 QFN 48 pin and a listing of the signal descriptions (see Figure 1-1).

The following nomenclature is used for signal names:

NC	No connection to the internal die is made from this pin
n	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates he negative side of a differential signal

The following nomenclature is used for signal types described in Table 1-1:

D	Open drain
IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals from floating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bidirectional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal
PD	Internal pull-down for input
PU	Internal pull-up for input

Figure 1-1 shows the pinout diagram for the AR8031.

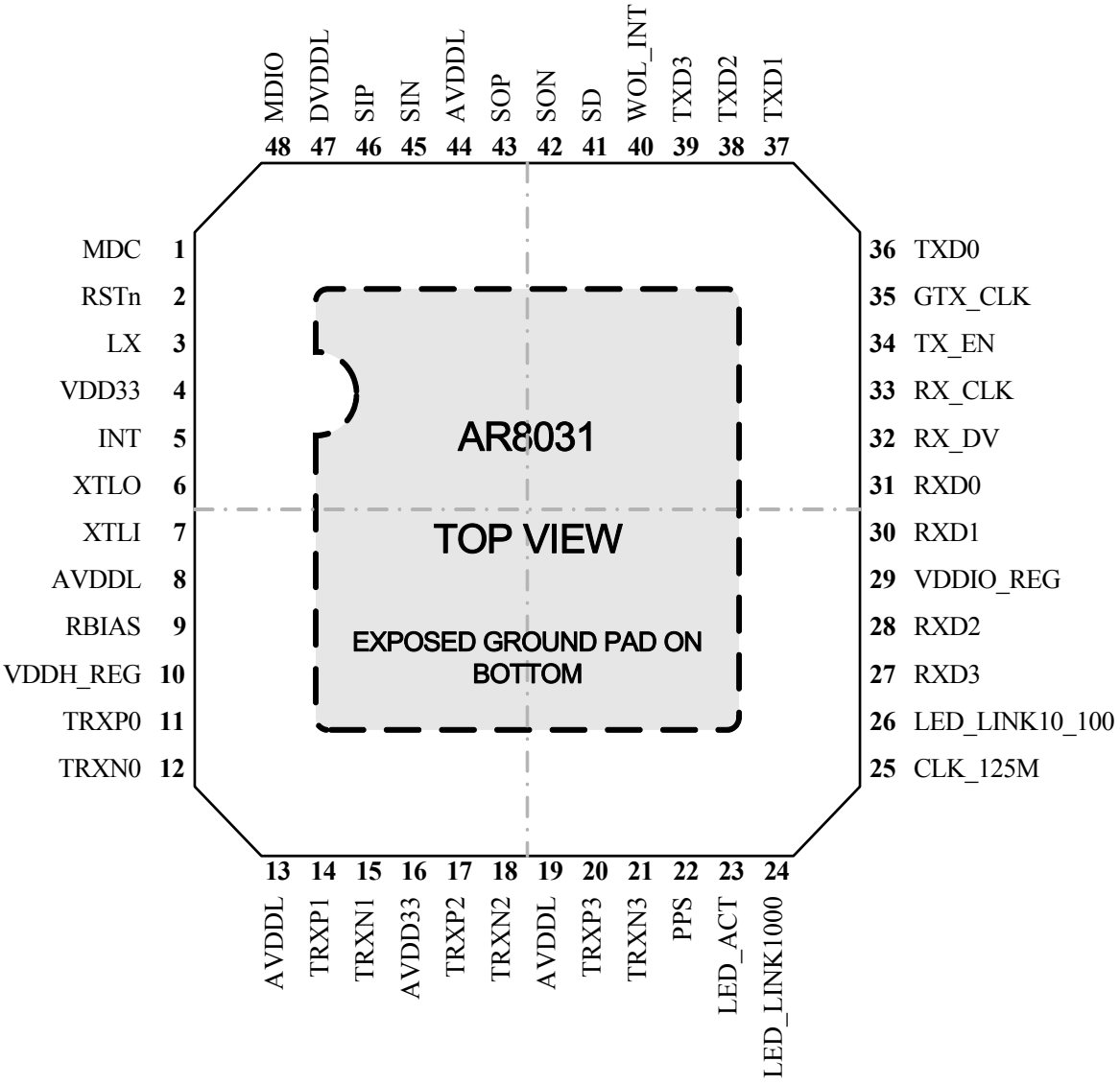


Figure 1-1. **AR8031 48-pin QFN Pinout Diagram (Top View)**

NOTE: There is an exposed ground pad on the back side of the package.

2. Signal to Pin Relationships and Descriptions

Table 2-1. **Signal to Pin Relationships and Descriptions**

Symbol	Pin	Type	Description
MDI			
TRXP0, TRXN0	11, 12	IA, OA, D	Media-dependent interface 0, differential 100 Ω transmission line
TRXP1, TRXN1	14, 15	IA, OA, D	Media-dependent interface 1, differential 100 Ω transmission line
TRXP2, TRXN2	17, 18	IA, OA, D	Media-dependent interface 2, differential 100 Ω transmission line
TRXP3, TRXN3	20, 21	IA, OA, D	Media-dependent interface 3, differential 100 Ω transmission line
RGMII			
GTX_CLK	35	I, PD	RGMII transmit clock, 125 MHz digital
RX_CLK	33	I/O, PD	RGMII receive clock, 125 MHz digital, adding a 22 Ω damping resistor is recommended
RX_DV	32	I/O, PD	RGMII receive data valid, adding a 22 Ω damping resistor is recommended
RXD0	31	I/O, PD	RGMII receive data 0, adding a 22 Ω damping resistor is recommended
RXD1	30	I/O, PD	RGMII receive data 1, adding a 22 Ω damping resistor is recommended
RXD2	28	I/O, PD	RGMII receive data 2, adding a 22 Ω damping resistor is recommended
RXD3	27	I/O, PD	RGMII receive data 3, adding a 22 Ω damping resistor is recommended
TX_EN	34	I, PD	RGMII transmit enable
TXD0	36	I, PD	RGMII transmit data 0
TXD1	37	I, PD	RGMII transmit data 1
TXD2	38	I, PD	RGMII transmit data 2
TXD3	39	I, PD	RGMII transmit data 3
SGMII/1000FX			
SIP/SIN	46, 45	IA	1.25 Gbps transmit differential inputs When this interface is used as a MAC interface, the MAC transmitter's positive output connects to SIP and the MAC transmitter's negative output connects to the SIN. When this interface is used as a fiber interface, the fiber-optic transceiver's positive output connects to the SIP and the fiberoptic transceiver's negative output connects to the SIN
SOP/SON	43, 42	OA	1.25 Gbps receive differential outputs When this interface is used as a MAC interface, the MAC receiver's positive input connects to SOP and the MAC receiver's negative input connects to the SON. When this interface is used as a fiber interface, the fiber-optic transceiver's positive input connects to the SOP and the fiberoptic transceiver's negative input connects to the SON
SD	41	IA	Signal Detect input, External 1.2V

Table 2-1. **Signal to Pin Relationships and Descriptions (continued)**

Symbol	Pin	Type	Description
Management Interface and Interrupt			
MDC	1	I, PU	Management data clock reference
MDIO	48	I/O, D	Management data, 1.5K Ω pull-up to 3.3V
LED			
LED_ACT	23	I/O, PD	Parallel LED output for 10/100/1000 BASE-T activity; active blinking LED active based upon power-on strapping. If pulled up, active low; If pulled-down, active high
LED_LINK_1000	24	I/O, PD	Parallel LED output for 1000 Base-T link; LED active based upon power-on strapping. If pulled up, active low; If pulled-down, active high
LED_LINK10_100	26	I/O, PD	Parallel LED output for 10/100 Base-T link LED active based upon power-on strapping. If pulled up, active low; If pulled-down, active high
System Signal Group/Reference			
CLK_25M	25	I/O	Synchronous Ethernet recovered clock — (25MHz, 50MHz, 62.5MHz or 125MHz) output, or IEEE 1588 reference 50MHz ~ 125MHz clock input, register configurable
PPS	22	O	IEEE 1588 Pulse Per Second output
RSTn	2	IH	System reset, active low
XTLI	7	IA	Crystal oscillator input; 27pF to GND. External 1.2V.
XTLO	6	OA	Crystal oscillator output; 27pF to GND
RBIAS	9	OA	External 2.37K Ω 1% to GND to set bias current
INT	5	I/O, PD	System Interrupt Output; Active high
WOL_INT	40	I/O, PD	Wake-on-LAN interrupt output; Active high
Power			
LX	3	OA	Power, 1.1V requlator output
VDDH_REG	10	OA	2.5V regulator output. A 1uF cap connected between this pin and GND
VDDIO_REG	29	OA	Regulator output for the RGMII I/O voltage. It can be either 1.5V (default) or 1.8V. If 2.5V is intended for the RGMII I/O, simply connect this pin with the 2.5V regulator output at pin 10.
AVDDL	8, 13, 19, 44	P	1.1V analog input. Connect to Pin 47 through a bead
DVDDL	47	P	1.1V digital core input. Connect to power inductor directly and 10uF+0.1uF ceramic caps to GND
VDD33	4	P	3.3V input for switching regulator
AVDD33	16	P	3.3V input for PHY, from VDD33 through a bead
-	-		Exposed ground pad on back of the chip, tie to ground

2.1 Power-on Strapping Pins

Table 2-2 shows the pin-to-PHY core Power-on strapping relationship

Table 2-2. **Power-on Strapping Pins**

PHY Pin	PHY Core Config Signal	Description	Default
RXD0	PHYADDRESS0	RXD1-0 set the lower two bits of the physical address. The upper three bits of the physical address are set to the default, “000”..	0
RXD1	PHYADDRESS1		0
RX_DV	MODE[0]	Mode select bit 0	0
RXD2	MODE[1]	Mode select bit 1	0
RX_CLK	MODE[2]	Mode select bit 2	0
RX_D3	MODE[3]	Mode select bit 3	0
LED_LINK1000	SEL_GPIO_INT	Select pin5 work mode: 0:INT, 1:GPIO	0
LED_ACT	ANA_MOD	Select the core voltage level: 0:1.1V, 1:1.2V	0

NOTE: 0 = Pull-down, 1 = Pull-up with 10K resistor

For AR8031-1L1E, suggest configuring the core to 1.1V.

Mode Definition

Table 2-3 shows the Mode and its Description

Table 2-3. **Mode Definition**

Mode	Description
0000	1000Base-T, RGMII
0001	1000Base-T, SGMII
0010	1000Base-X, RGMII, 50Ω
0011	1000Base-X, SGMII, 75Ω
0100	1000M converter mode, 50Ω
0101	1000M converter mode, 75Ω
0110	100Base-FX, RGMII, 50Ω
0111	100M converter, 50Ω
1000	Reserved
1001	Reserved
1010	Reserved

Table 2-3. **Mode Definition**

Mode	Description
1011	Reserved
1100	100Base-Tx, RMII1 mode
1101	100Base-Tx, RMII2 mode
1110	100Base-FX, RGMII mode, 75Ω
1111	100M converter mode, 75Ω

NOTE: RMII1 is normal RMII mode — whch requires an external 50MHz clock input

NOTE: RMII2 uses a 25MHz crystal or 25MHz clock input and generates a 50MHz clock output

NOTE: 50Ω or 75Ω is the fiber serdes interface output impedance

3. Functional Description

The AR8031 is Atheros's low cost GbE PHY. It is a highly integrated analog front end (AFE) and digital signal transceiver, providing high performance combined with substantial cost reduction. The AR8031 provides physical layer functions for half/full -duplex 10 BASE-Te, 100 BASE-TX and 1000 BASE-T Ethernet to transmit and receive high-speed data over standard category 5 (CAT5) unshielded twisted pair cable.

The AR8031 10/100/1000 PHY is fully 802.3ab compliant, and supports the reduced Gigabit media-independent interface (RGMII) to connect to a Gigabit-capable MAC.

The AR8031 transceiver combines echo canceller, near end cross talk (NEXT) canceller, feed-forward equalizer, joint Viterbi, feedback equalizer, and timing recovery, to enhance signal performance in noisy environments.

See the "AR8031 Functional Block Diagram" on page 2.

Table 3-1 shows a feature comparison across the AR8031, AR8033, and AR8035 family.

Table 3-1. **AR8031, AR8033, and AR8035 Comparison**

Feature	AR8031	AR8033	AR8035
RGMII	yes	yes	yes
SGMII	yes	yes	
Cu Ethernet**	yes	yes	yes
EEE (802.3az)	yes	yes	yes
Wake-on-LAN	yes	yes	yes
SERDES/Fiber	yes***	yes***	
1588v2	yes		
Sync-E	yes	yes	
Packaging	48-pin	48-pin	40-pin

NOTE: AR8031, AR8033 is pin-to-pin compatable

** 10Base-TE, 100Base-TX, 1000Base-T is supported

*** 100Base-FX, and 1000Base-X is supported

The AR8031 is part of the Arctic family of devices — including the AR8031, the AR8033, and the AR8035. The major differences can be seen in the table above.

3.2 Modes of Operation

The AR8031 operates in the following modes, as illustrated below:

Figure 3-1shows the operating mode Copper for the AR8031.

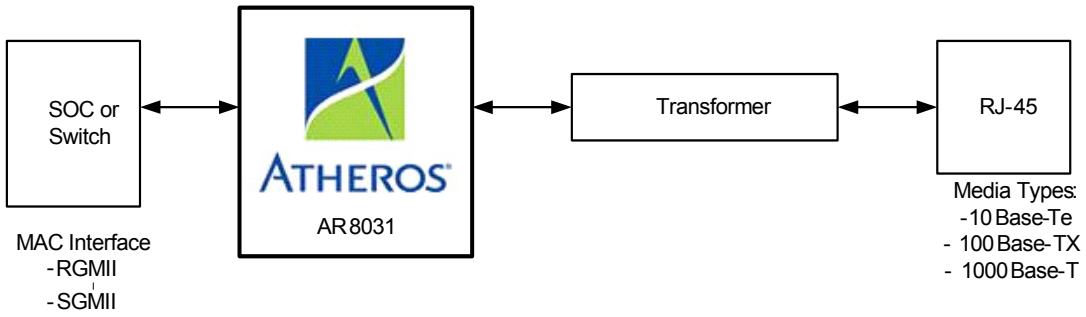


Figure 3-1. **Operating Modes — Copper**

Figure 3-2 shows the operating mode fiber for the AR8031..

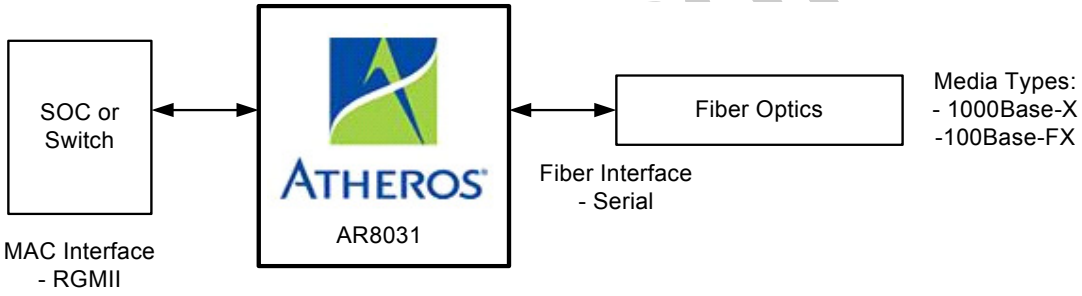


Figure 3-2. **Operating Modes — Fiber**

Figure 3-3 shows the operating mode Media Converter for the AR8031.

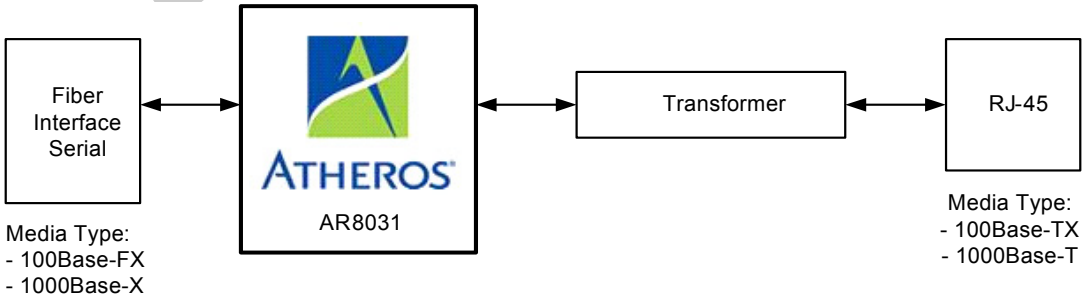


Figure 3-3. **Operating Modes — Media Converter**

3.3 Transmit Functions

Table 3-2 describes the transmit function encoder modes.

Table 3-2. **Transmit Function Encoder Modes**

Encoder Mode	Description
1000BASE-T	In 1000 BASE-T mode, the AR8031 scrambles transmit data bytes from the MAC interfaces to 9-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT5 cable.
100BASE-TX	In 100 BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.
10BASE-Te	In 10 BASE-Te mode, the AR8031 transmits and receives Manchester-encoded data.

3.4 Receive Functions

3.4.1 Decoder Modes

Table 3-3 describes the receive function decoder modes.

Table 3-3. **Receive Function Decoder Modes**

Decoder Mode	Description
1000 BASE-T	In 1000 BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately and data is output to the MAC interfaces.
100 BASE-TX	In 100 BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to the MII receive data pins after data stream delimiters have been translated.
10 BASE-T	In 10 BASE-T mode, the recovered 10 BASE-T signal is decoded from Manchester then aligned.

3.4.7 Auto-Negotiation

3.4.2 Analog to Digital Converter

The AR8031 device employs an advanced high speed ADC on each receive channel with high resolution, which results in better SNR and lower error rates.

3.4.3 Echo Canceller

A hybrid circuit is used to transmit and receive simultaneously on each pair. A signal reflects back as an echo if the transmitter is not perfectly matched to the line. Other connector or cable imperfections, such as patch panel discontinuity and variations in cable impedance along the twisted pair cable, also result in drastic SNR degradation on the receive signal. The AR8031 device implements a digital echo canceller to adjust for echo and is adaptive to compensate for the varied channel conditions.

3.4.4 NEXT Canceller

The 1000 BASE-T physical layer uses all four pairs of wires to transmit data. Because the four twisted pairs are bundled together, significant high frequency crosstalk occurs between adjacent pairs in the bundle. The AR8031 device uses three parallel NEXT cancellers on each receive channel to cancel high frequency crosstalk. The AR8031 cancels NEXT by subtracting an estimate of these signals from the equalizer output.

3.4.5 Baseline Wander Canceller

Baseline wander results from Ethernet links that AC-couple to the transceivers and from AC coupling that cannot maintain voltage levels for longer than a short time. As a result, transmitted pulses are distorted, resulting in erroneous sampled values for affected pulses. Baseline wander is more problematic in the 1000 BASE-T environment than in 100 BASE-TX due to the DC baseline shift in the transmit and receive signals. The AR8031 device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

3.4.6 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

The AR8031 device supports 10/100/1000 BASE-T Copper auto-negotiation in accordance with IEEE

802.3 clauses 28 and 40. Auto-negotiation provides a mechanism for transferring information between a pair of link partners to choose the best possible mode of operation in terms of speed, duplex modes, and master/slave preference. Auto-negotiation is initiated upon any of the following scenarios:

- Power-up reset
- Hardware reset
- Software reset
- Auto-negotiation restart
- Transition from power-down to power-up
- The link goes down

If auto-negotiation is disabled, a 10 BASE-T or 100 BASE-TX can be manually selected using the IEEE MII registers.

3.4.8 Smartspeed Function

The Atheros Smartspeed function is an enhanced feature of auto-negotiation that allows the AR8031 device to fall back in speed based on cabling conditions as well as operate over CAT3 cabling (in 10 BASE-Te mode) or two-pair CAT5 cabling (in 100 BASE-TX mode).

By default, the Smartspeed feature is enabled. Refer to the register "Extended PHY-Specific Control" on page 48, which describes how to set the parameters. Set these register bits to control the Smartspeed feature:

- Bit [5]: 1 = Enables Smartspeed (default)
- Bits [4:2]: Sets the number of link attempts before adjusting
- Bit [1]: Timer to determine the stable link condition

3.4.9 Automatic MDI/MDIX Crossover

During auto-negotiation, the AR8031 device automatically determines and sets the required MDI configuration, eliminating the need for external crossover cable. If the remote device also implements automatic MDI crossover, the crossover algorithm as described in IEEE 802.3 clause 40.4.4 ensures that only one device performs the required crossover.

3.4.10 Polarity Correction

If cabling has been incorrectly wired, the AR8031 automatically corrects polarity errors on the receive pairs in 1000 BASE-T, 1000BASE-TX and 10 BASE-T modes.

3.5 Loopback Modes

3.5.1 Digital Loopback

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in the AR8031 device. The registers are used to determine at which point the signal loops back (for different modes, 10, 100, and 1000, respectively). Figure 3-4 shows a block diagram of digital loopback.

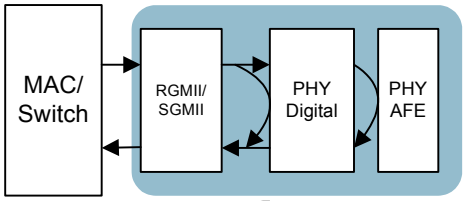


Figure 3-4. **Digital Loopback**

3.5.2 External Cable Loopback

External cable loopback loops RGMII/SGMII Tx to RGMII/SGMII Rx through a complete digital and analog path and an external cable, thus testing all the digital data paths and all the analog circuits. Figure 3-5 shows a block diagram of external cable loopback.

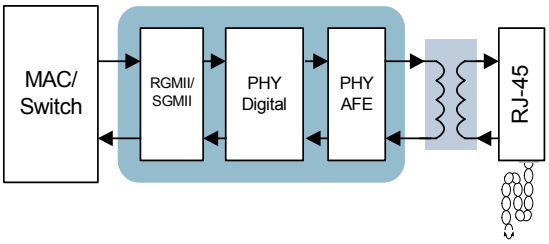


Figure 3-5. **External Cable Loopback**

3.5.3 Remote PHY Loopback

The Remote loopback connects the MDI receive path to the MDI transmit path, thus the remote link partner can detect the connectivity in the resulting loop. The figure below shows the path of the remote loopback.

Figure 3-6 shows a block diagram of external remote PHY loopback.

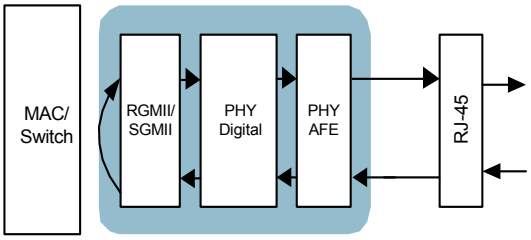


Figure 3-6. **Remote PHY Loopback**

NOTE: AR8031-1L1E does not support.

AR8031-1L1A supports Remote PHY Loopback.

3.6 Cable Diagnostic Test

The Cable Diagnostic Test (CDT) feature in the AR8031 device uses Time Domain Reflectometry (TDR) to identify remote and local PHY malfunctions, bad/marginal cable or patch cord segments, or connectors. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatch, and bad magnetics. The CDT can be performed when there is no link partner or when the link partner is auto-negotiating.

3.7 Fiber Mode Support

Besides standard 10/100/1000Base-T copper port support, Both AR8031 and AR8033 provide additional IEEE 1000Base-X and 100Base-FX support in fiber applications through integrated SERDES. Both the AR8031 and the AR8033 can work in RGMII mode to fiber or 10/100/1000Base-T to fiber.

Besides 1000Base-X and 100Base-FX support, Both devices will support IEEE 802.3 remote Fault Indication and fault propagation in fiber application.

3.7.1 IEEE 802.3 Remote Fault Indication Support

Remote Fault allows stations on a fiber optic link to know when there is a problem on the link. Without Remote Fault, a station can not detect a problem that affects only one fiber (Transmit, for example).

With Remote Fault, the loss of a Receive signal (Link) causes the Transmitter to send a special pattern of data indicating that a fault has occurred. 84 '1's followed by a single '0' is sent three times, in-band, and is readily detectable by the remote station, but is constructed so as to not satisfy the 100BASE-X carrier sense criterion, so the message will not be interpreted as normal traffic. If the remote station has Remote Fault, the link is dropped. If the remote station does not have Remote Fault, the special data pattern is ignored.

The AR8031 indicates whether or not a Remote Fault pattern has been received from the remote station using the "Remote Fault Status Bit". This "Remote Fault Status Bit" can be "Propagated" (see below) to the copper links on both ends of a fiber link. In the event of a detected fault, both ends of the link can be notified of the failure in this way. This is particularly useful given the distances fiber links are generally used over.

3.7.2 Fault Propagation

The AR8031 supports Fault Propagation - this allows the fiber link fault to be propagated to the Twisted-pair copper connections where the "link down" status can be easily and quickly detected.

The following steps describe Fault Propagation (for both 100Base-FX and 1000Base-X):

The AR8031 supports Fault Propagation - this allows the fiber link fault to be propagated to the Twisted-pair copper connections where the "link down" status can be easily and quickly detected.

The following steps describe Fault Propagation (for both 100Base-FX and 1000Base-X):

- The Twisted-pair transmit path will be OFF when the Receive path of the Fiber link has no signal detected or is link down. The two Fiber media types are then handled as described below:
- The Media Converter (in 100Base-FX mode) will transmit Far-End Fault message, on the TX pair, when the Receive path of Fiber has no signal detected or is link down. This alerts the Media Converter on the remote end of the link.
- The Transmit Twisted-pair will then be switched OFF on the remote end of the link.
- The Media Converter (in 1000Base-X mode) will restart auto-negotiation when the Receive path of the Fiber detects no signal or is link down.
- Auto-negotiation will carry remote fault indications from the Transmit fiber and the local station will restart auto-negotiation when its' Receive path has no detected signal or is link down.

- The Twisted-pair transmit path will be OFF when the Receive path of a 1000Base-X learns of the fault from an AN message.

Figure 3-7 shows the Fiber Fault mechanism.

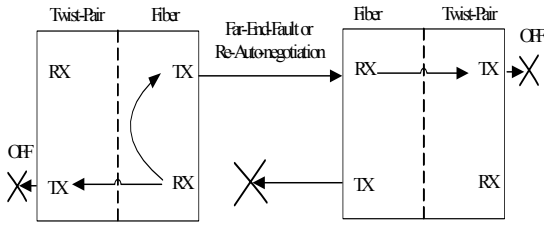


Figure 3-7. **Fiber Fault Propagation or Re-Auto-negotiation**

3.8 LED Interface

The LED interface can either be controlled by the PHY or controlled manually, independent of the state of the PHY. Three status LEDs are available. These can be used to indicate operation speed, duplex mode, and link status. The LEDs can be programmed to different status functions from their default value. They can also be controlled directly from the MII register interface.

3.9 Power Supplies

The AR8031 device requires only one external power supply: 3.3 V.

3.10 Timing Sychronization

3.10.1 IEEE 1588 — Precision Clock Synchronization Protocol

IEEE 1588 provides a mechanism to synchronize the clocks across an Ethernet network by exchanging the IEEE 1588 packets. The slave node can adjust the local clock based on the the timing information calculated from timestamps exchanged. Figure 3-8 shows the top-level use of the AR8031 to build a typical 1588 system.

The AR8031 provides all the key componets to support an IEEE 1588v2 operation. The IEEE 1588 Real Time Clock (RTC) generates and provides time information to other mofules and software, timing information includes Time of Day and PPS.

IEEE 1588 Control accepts control information fom software via MDC/MDIO, generates control signals to other modules, and provides status information to software.

IEEE 1588 Timestamp Unit, packet detction and processing, generates timestamps for IEEE 1588v2 event messages and interrupt signals when receiving or transmitting IEEE 1588 messages.

The AR8031 supports ordinary, boundary and transparent clock modes as defined in IEEE 1588v2

Figure 3-9 shows the top level diagram of AR8031's IEEE 1588v2 module. Also the AR8031 supports time-stamps to be encapsulated into the 1588 packet as explained in the following figure 3-10.

Figure 3-8 shows the Top Level Use of AR8031 in an IEEE 1588v2 system.

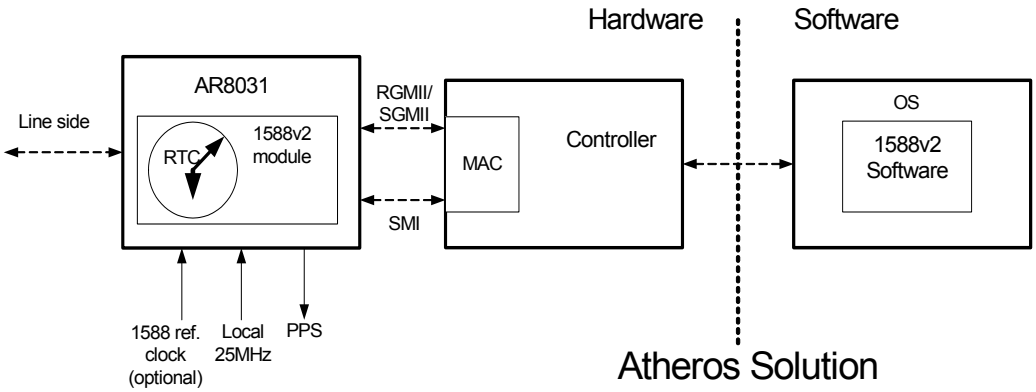


Figure 3-8. **Top Level Use of AR8031 in an IEEE 1588v2 System**

Figure 3-9 shows the Top Level Diagram of the AR8031's IEEE 1588v2 module.

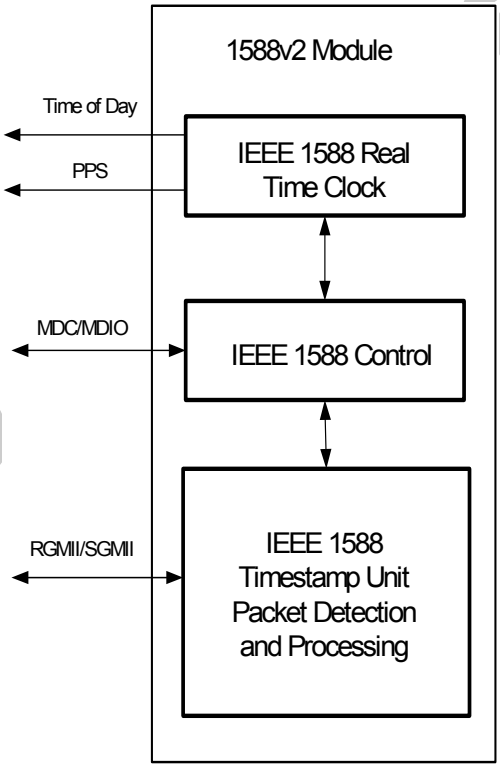


Figure 3-9. **Top Level Diagram of the AR8031's IEEE 1588v2 Module**

On the transmit side, the PHY will monitor and parse the incoming packet from the top layer, upon the request of sending IEEE 1588 packet, it will calculate the accurate time of transmission onto the media and a timestamp accordingly.

The AR8031 supports both one-step and two-step clock modes, as defined in IEEE 1588. No matter where accurate time information is carried — in the follow-up message (two-step clock mode) or in the single event message (one-step clock mode), the AR8031 will support correction filed update and CRC recalculation on the fly.

On the receive side, the PHY will monitor and parse the incoming packet from media, and will generate a

timestamp upon the reception of IEEE 1588 packets. The built-in parser is capable of detecting IEEE 1588 on ethernet layer 2 (including untagged, one VLAN tagged and two VLAN tagged), or layer 3 IPv4/UDP, and IPv6/UDP (including PPPoE and SNAP).

The following IEEE 1588 packets are used to exchange the timing message for the delay request-response mechanism:

- Sync
- Follow_Up
- Delay_Req
- Delay_Resp

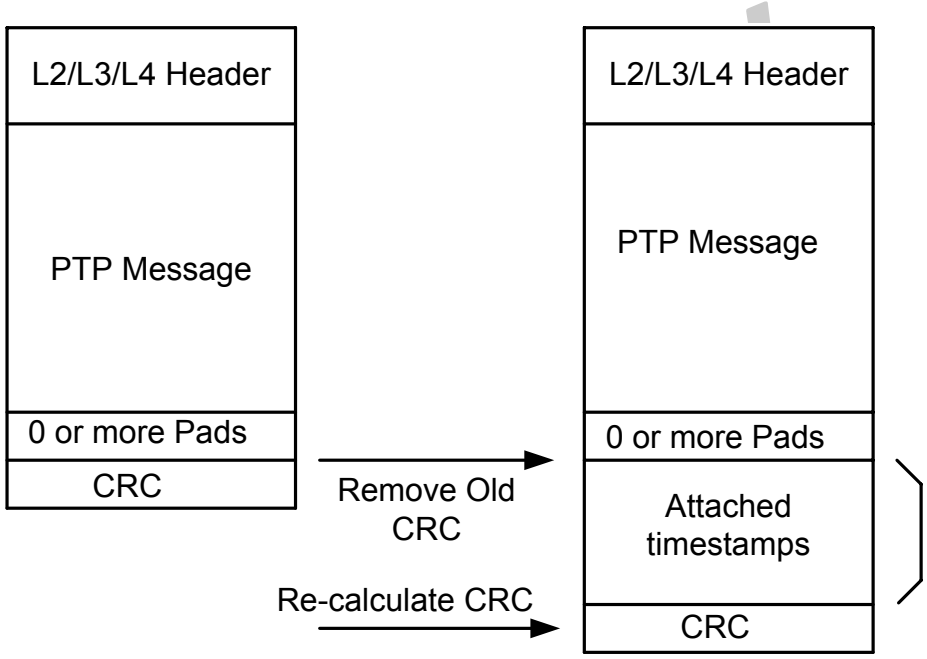
Messages for the Peer Delay are also supported:

- Pdelay_Req
- Pdelay_Resp
- Pdelay_Resp_Follow_Up

The received IEEE 1588 packet along with the timestamp will be forwarded to an external CPU/MAC for further processing via accelerated MDC/MDIO interfaces (running up to 25MHz).

The AR8031 also supports time-stamp encapsultion into the 1588 packet as explained in the following figure 3-10.

Figure 3-10 shows the PTP Timestamp.



1. Event PTP message attach timestamp of itself.
2. General PTP message attach timestamp of associated event PTP message if existed.

Figure 3-10. **PTP Timestamp**

AR8031 provides a Pulse Per Second output, which locks onto the 1588 clock time of the device.

The AR8031 1588 logic allows multiple reference clock sources, including:

- Local 25MHz crystal (default)
- Recovered clock from Sychronous Ethernet
- Dedicated, external 50MHz ~ 125MHz 1588 reference clock

The AR8031 IEEE 1588v2 module is under Tx FIFO, so the FIFO does not affect time stamping giving improved accuracy. Refer to Figure 3-11 below.

Also, the IEEE 1588v2 module can be bypassed by register settings.

Figure 3-11 shows the Block Diagram of the AR8031 1588v2 module.

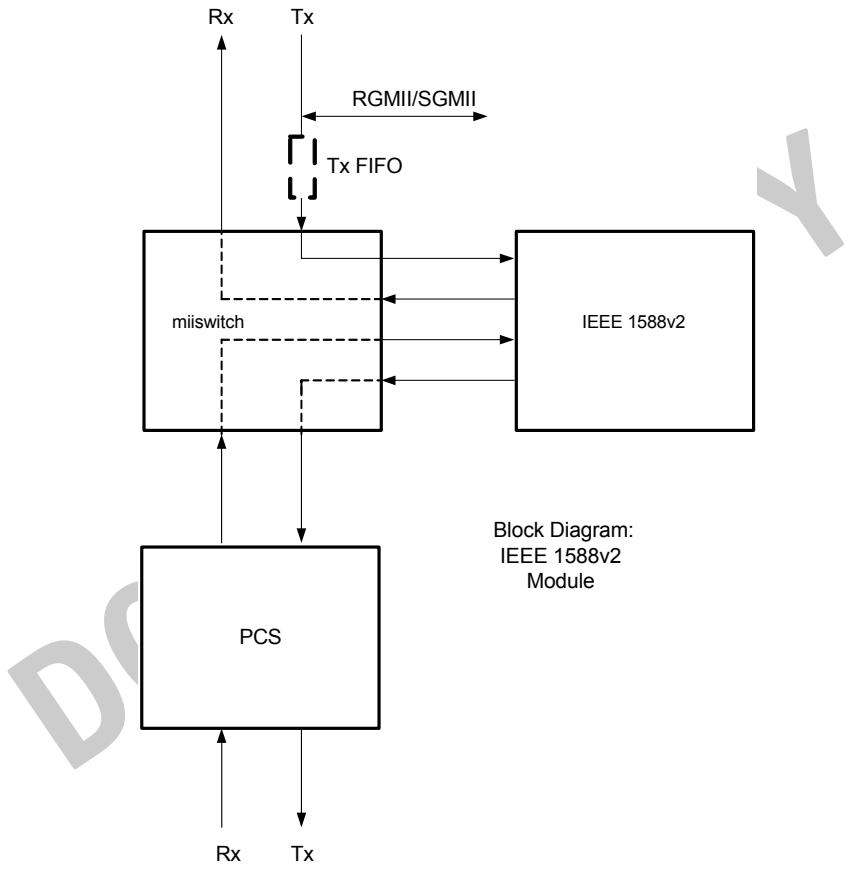


Figure 3-11. **Block Diagram of the AR8031's IEEE 1588v2 Module**

3.10.2 Synchronous Ethernet — Physical Layer Timing Synchronization

The AR8031 supports Synchronous Ethernet for 100Base-T, 1000Base-T, and 1000Base-X applications by offering one recovered clock from the network line-side. This recovered clock output is register configurable to 25MHz (default), 50MHz, 62.5MHz or 125MHz, to meet the ITU-T recommendations G.8261/Y.1361. The network node can use this recovered clock to replace local clock sources and drive the local system. Therefore all distributed nodes the network will use the same network clock to support synchronus and timing sensitive services like T1/E1 service over Ethernet.

3.11 Atheros Green Ethos™

3.11.1 Low Power Modes

The AR8031 device supports the software power-down low power mode. The standard IEEE power-down mode is entered by setting the POWER_DOWN bit (bit [11]) of the register "Control" on page 18 equal to one. In this mode, the AR8031 ignores all MAC interface signals except the MDC/MDIO. It does not respond to any activity on the CAT 5 cable. The AR8031 cannot wake up on its own. It can only wake up by setting the POWER_DOWN bit of the "Control" register to 0. See Table 5.1.1 on page 36.

3.11.2 Shorter Cable Power Mode

The AR8031 can attain an additional 25% power savings when a cable length is detected that is <30M vs. standard power consumption for a 100M Cat5 cable.

3.11.3 Hibernation Mode

The AR8031 device supports hibernation mode. When the cable is unplugged, the AR8031 will enter hibernation mode after about 10 seconds. The power consumption in this mode is very low when compared to the normal mode of operation. When the cable is re-connected, the AR8031 wakes up and normal functioning is restored.

3.12 IEEE 802.3az and Energy Efficient Ethernet

IEEE 802.3az provides a mechanism to greatly save the power consumption between data packets burst. The link partners enter Low Power Idle state by sending short refresh signals to maintain the link.

There are two operating states, Active state for normal data transfer, and Low-power state between the data packet bursts.

In the low-power state, PHY shuts off most of the analog and digital blocks to reserve energy. Due to the bursty traffic nature of Ethernet, system will stay in low-power mode in the most of time, thus the power saving can be more than 90%.

At the link start up, both link partners exchange information via auto neg to determine if both parties are capable of entering LPI mode.

Legacy Ethernet products are supported, and this is made transparent to the user.

3.12.1 IEEE 802.3az LPI Mode

AR8031 works in the following modes when 802.3 az feature is turned on:

- Active: the regular mode to transfer data
- Sleep: send special signal to inform remote link of entry into low-power state
- Quiet: No signal transmitted on media, most of the analog and digital blocks are turned off to reduce energy.
- Refresh: send periodically special training signal to maintain timing recovery and equalizer coefficients
- Wake: send special wakup signal to remote link to inform of the entry back into Active.

The AR8031 supports both 100Base-Tx EEE and 1000Base-T EEE.

100Base-Tx EEE allows asymmetrical operation, which allows each link partner to enter the LPI mode independent of the other partner.

1000Base-T EEE requires symmetrical operation, which means that both link partners must enter the LPI mode simultaneously.

Figure 2-3 shows the 802.3az operating states for the AR8031.

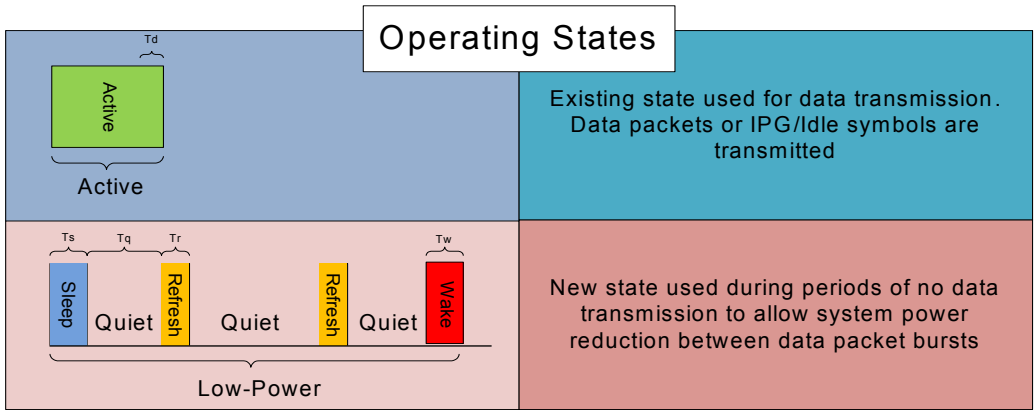


Figure 3-12. **Operating States — 802.3az LPI Mode**

Figure 2-4 shows the 802.3az operating power modes — 802.3az for the AR8036.

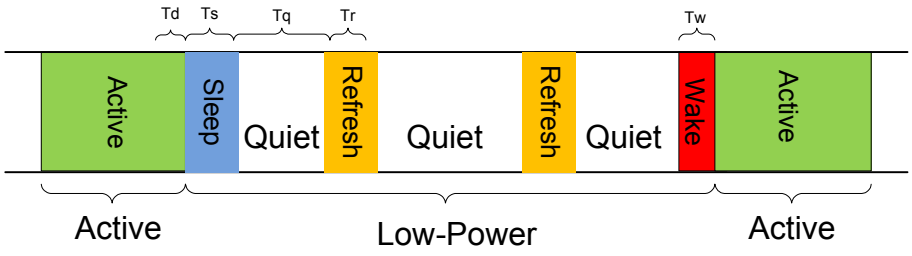


Figure 3-13. **Operating Power Modes — 802.3az LPI Mode**

3.13 Wake On LAN (WoL)

Originally Wake-on-LAN (WoL) was an Ethernet networking standard that allowed a computer to be turned on (or woken up) by a network message for Adminstrator attention, etc. However as part of the latest industry trend towards energy savings, and lower power consumption, WoL gets wide interest to be adopted across networking systems as a mechanism to help to manage and regulate the total power consumed by the network. The AR8031 supports Wake On LAN (WoL):

- Able to enter the sleep/isolate state (PHY's all TX bus (including clock) are in High-Z state, but PHY can still receive packets) by ISOLATE bit in MII register configuration
- Consumes less than 50mW when in sleep/isolate mode.
- Supports automatic detection of magic packets (a specific broadcast frame containing anywhere within its payload: 6 bytes of ones (resulting in hexadecimal FF FF FF FF FF FF), followed by sixteen repetitions of the target computer's MAC address) and notification via dedicated hardware interrupt with pulse width of 32 125MHz clock cycles
- Supports exit from the sleep state by registeer configuration

3.13.1 Control — Fiber Page

Offset: 0x00, or 0d00
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	Type		Description
		Mode	R/W	
		HW Rst.	1	
		SW Rst.	Retain	
		Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
		Mode	R/W	
		HW Rst.	1	
		SW Rst.	Retain	
		Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
		Mode	R/W	
		HW Rst.	2’b10	
		SW Rst.	Retain	
		Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

3.13.1 Status Register — Copper Page

Offset: 0x00, or 0d00
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	Type		Description
15		Mode	R/W	
		HW Rst.	1	
		SW Rst.	Retain	
14		Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
13		Mode	R/W	
		HW Rst.	1	
		SW Rst.	Retain	
12		Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
11		Mode	R/W	
		HW Rst.	2’b10	
		SW Rst.	Retain	
10		Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
9				
8				
7				

Bit	Name	Type		Description
6				
5				
4				
3				
2				
1				
0				

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 summarizes the absolute maximum ratings and Table 4-2 lists the recommended operating conditions for the AR8031. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 4-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max Rating	Unit
V_{DD33}	3.3V analog supply voltage	3.8	V
AVDDL	1.1V analog supply voltage	1.6	V
DVDDL	1.1V digital core supply voltage	1.6	V
T_{store}	Storage temperature	–65 to 150	°C
HBM	Electrostatic discharge tolerance - Human Body Model	TBD	V
MM	Machine Model	TBD	V
CDM	Charge Device Model	TBD	V

4.2 Recommended Operating Conditions

Table 4-2. **Recommended Operating Conditions**

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD33}	3.3V supply voltage	3.0	3.3	3.6	V
DVDDL/AVDDL	1.1V digital core supply voltage	1.04	1.1	1.17	V
$T_{ambient}$	Ambient temperature for normal operation — Commercial chip version AR8031-AL1A	0	—	70	°C
$T_{ambient}$	Ambient temperature for normal operation — Industrial chip version AR8031-AL1B	-40	—	85	°C
T_J	Junction temperature	-40	—	120	°C
Ψ_{JA}	Junction to ambient temperature	—	24.8	—	°C/W

4.3 RGMII Characteristics

Table 4-3 shows the RGMII DC characteristics with 2.5/3.3V I/O supply.

Table 4-3. **RGMII DC Characteristics — 2.5/3.3V I/O Supply**

Symbol	Parameter	Min	Max	Unit
I_{IH}	Input high current	—	15	µA
I_{IL}	Input low current	–15	—	µA
V_{IH}	Input high voltage	1.7	3.5	V
V_{IL}	Input low voltage	—	0.7	V
V_{OH}	Output high voltage	2.0	2.8	V
V_{OL}	Output low voltage	GND – 0.3	0.4	V

Table 4-4 shows the RGMII DC characteristics with 1.8V I/O supply.

Table 4-4. **RGMII DC Characteristics — 1.8V I/O Supply**

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	1.4	—	V
V_{IL}	Input low voltage	—	0.4	V
V_{OH}	Output high voltage	1.5	—	V
V_{OL}	Output low voltage	—	0.3	V

Table 4-5 shows the RGMII DC characteristics with 1.5V I/O supply.

Table 4-5. **RGMII DC Characteristics — 1.5 I/O Supply**

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input high voltage	1.2	—	V
V_{IL}	Input low voltage	—	0.3	V
V_{OH}	Output high voltage	1.3	—	V
V_{OL}	Output low voltage	—	0.2	V

Figure 4-2 shows the RGMII AC timing diagram — no internal delay.

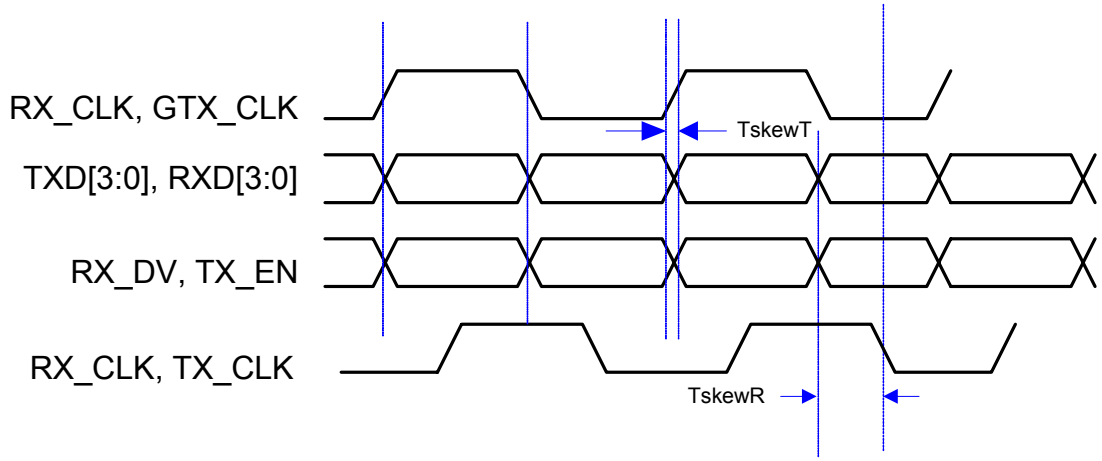


Figure 4-1. **RGMII AC Timing Diagram — no Internal Delay**

Table 4-6 shows the RGMII AC characteristics.

Table 4-6. **RGMII AC Characteristics — no Internal Delay**

Symbol	Parameter	Min	Typ	Max	Unit
T_{skewT}	Data to clock output skew (at Transmitter)	-500	0	500	ns
T_{skewR}	Data to clock output skew (at Receiver)	1	—	—	ns
T_{cyc}	Clock cycle duration	7.2	8.0	8.8	ns
Duty_G	Duty cycle for Gigabit	45	50	55	%
Duty_T	Duty cycle for 10/100T	40	50	60	%
T_r/T_f	Rise/Fall time (20 - 80%)	—	—	0.75	ns

Figure 4-2 shows the RGMII AC timing diagram with internal delay added (default RGMII timing).

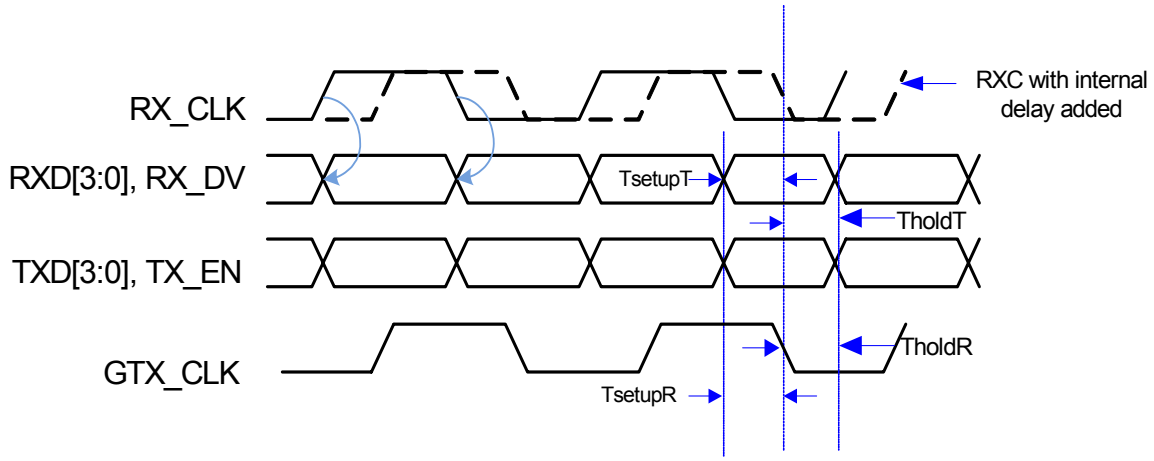


Figure 4-2. **RGMII AC Timing Diagram — With Internal Delay Added (Default)**

Table 4-7 shows the RGMII AC characteristics with delay added.

Table 4-7. **RGMII AC Characteristics — with internal delay added (Default)**

Symbol	Parameter	Min	Typ	Max	Unit
TsetupT	Data to Clock output Setup (at Transmitter — integrated delay)	1.65	2.0	2.2	ns
TholdT	Clock to Data output Hold (at Transmitter — integrated delay)	1.65	2.0	2.2	ns
TsetupR	Data to Clock input setup time (at Receiver — integrated delay)	1.0	2.0		ns
TholdR	Data to Clock output hold time (at Reciever — integrated delay)	1.0	2.0		ns

4.4 SERDES and SGMII Characteristics

Table 4-8 shows the Driver DC characteristics: LVDS.

Table 4-8. **Driver DC Characteristics: LVDS**

Symbol	Parameter	Min	Typical	Max	Unit
Voh	Output voltage high		950	1050	mV
Vol	Output voltage low	500	650		mV
Vring	Output ringing			10	%
|Vod|	Output differential voltage	Programmable #note 1 300 (default)			mV
Vos	Output offset voltage	750	800	850	mV
Ro	Output impedance (single ended) 50ohm termination	40	50	60	ohm
	Output impedance (single ended) 75ohm termination	60	75	90	ohm
Delta Ro	Mismatch in a pair			10	%
Delta Vod	Change in Vod between "0" and "1"			25	mV
Delta Vos	Change in Vos between "0" and "1"			25	mV
Isa,Isb	Output current on short to GND			40	mA
Isab	Output current when a, b are shorted			12	mA
Ixa,Ixb	Power off leakage current			10	mA

NOTE: output differential voltage can be configured by register MMD7 0x8011 [15:13]

Table 4-9 shows the Receiver DC Characteristics

Table 4-9. **Receiver DC Characteristics**

Symbol	Parameter	Min	Typical	Max	Unit
Vio	Internal Offset Voltage	730	825	930	mV
Vih	Input Single Voltage High		1050	1150	mV
Vil	Input Single Voltage Low	500	600		mV
Vidth	Input differential threshold	-50		+50	mV
Vhyst	Input differential hysteresis	25			mV
Rin	Receiver differential input impedance 50ohm termination	80	100	120	ohm
	Receiver differential input impedance 75ohm termination	120	150	180	ohm

Table 4-10 shows the Driver AC characteristics.

Table 4-10. **Driver AC Characteristics**

Symbol	Parameter	Min	Max	Unit
tfall	Vod fall time (20%-80%)	100	200	pSec
trise	Vod rise time (20%-80%)	100	200	pSec
Tskew1	Skew between two members of a differential pair		20	pSec

NOTE: Skew measured at 50% of the transition.

Figure 4-3 shows the MDIO AC timing diagram.

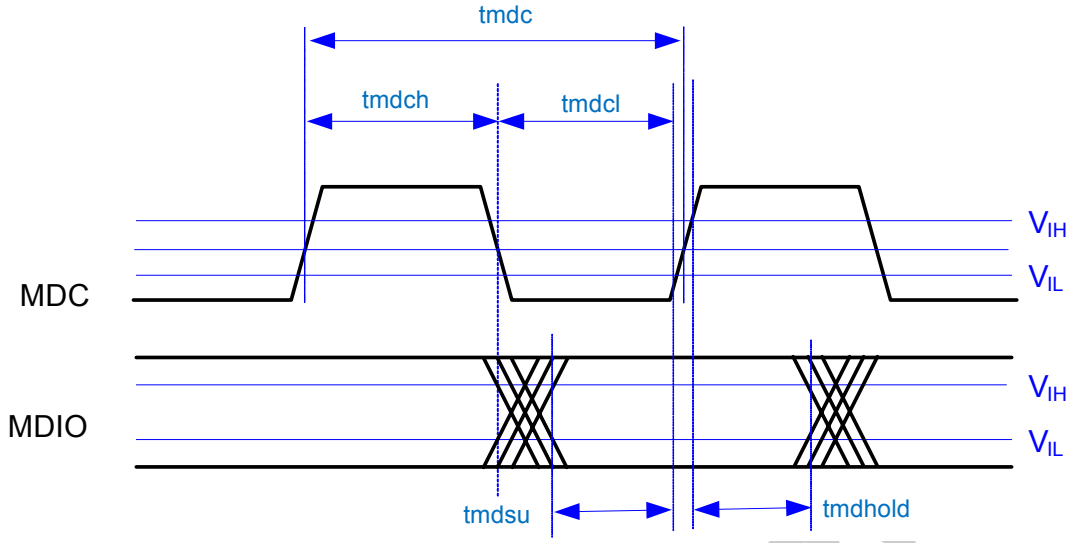


Figure 4-3. **MDIO AC Timing Diagram**

4.5 MDIO Timing table

Table 4-11. **MDIO AC Characteristic**

Symbol	Parameter	Min	Typ	Max	Unit
tmdc	MDC Period	40			ns
tmdcl	MDC Low Period	16			ns
tmdch	MDC High Period	16			ns
tmdsu	MDIO to MDC rising setup time	10			ns
tmdhold	MDIO to MDC rising hold time	10			ns

4.6 MDIO DC characteristic table

Table 4-12. **MDIO DC Characteristic**

Symbol	Parameter	Min	Max	Unit
V_{OH}	Output high voltage	2.4	—	V
V_{OL}	Output low voltage	—	0.4	V
V_{IH}	Input high voltage	2.0	—	V
V_{IL}	Input low voltage	—	0.8	V
I_{IH}	Input high current	—	0.4	mA
I_{IL}	Input low current	-0.4	—	mA

4.7 XTAL/OSC characteristic table

Table 4-13. **XTAL/OSC Characteristic**

Symbol	Parameter	Min	Typ	Max	Unit
T_XI_PER	XI/OSCI Clock Period	40.0 - 50ppm	40.0	40.0 + 50ppm	ns
T_XI_HI	XI/OSCI Clock High	14	20.0		ns
T_XI_LO	XI/OSCI Clock Low	14	20.0		ns
T_XI_RISE	XI/OSCI Clock Rise Time, VIL (max) to VIH (min)			4	ns
T_XI_FALL	XI/OSCI Clock Fall time, VIL (max) TO VIH (min)			4	ns
V_IH_XI	The XCTLI input high level	0.8	1.2	1.5	V
V_IL_XI	The XCTLI input low level voltage	- 0.3	0	0.15	V

4.8 Power Pin Current Consumption

Table 4-14 shows the current consumption for the power pins.

Table 4-14. **Power Pin Consumption**

Symbol	Voltage Range	Current (Max)
AVDDL	1.1V ±5%	50.8 mA
DVDDL	1.1V ±5%	113.7 mA
AVDD33	3.3V ±10%	63.8 mA
VDDIO_REG	Connect VDDH_REG 2.5V	20.9 mA

4.9 Typical Power Consumption Parameters

The following conditions apply to the typical characteristics unless otherwise specified:
VCC = 3.3V (1.1V switching regulator integrated. 50mW RGMII power included).

Table 4-15. **Total System Power**

Symbol	Condition	Total Current (mA)	LED Consumption (mA)	Total Power Consumption w/o LED (mW)
P_{LDPS}	Link Down, Power Saving Mode	10.57	0	34.9
P_{PWD}	Power Down Mode	13	0	42.9
RGMII + Copper mode				
P_{1000F}	1000Base Full Duplex	126	2.7	415.8
$P_{1000idle}$	1000Base Idle	116.1	4	383.1
P_{100F}	100Base Full Duplex	35.5	3.5	117.2
$P_{100idle}$	100Base Idle	34.9	4	115.2
P_{10F}	10Base-Te Full Duplex	34.5	1	113.9
P_{10idle}	10Base-Te Idle	17.8	1.5	58.7
802.az Enabled				
P_{LDPS}	1000M Idle	36.3	4	119.8
P_{LDPS}	100M Idle	16.2	4	53.5
Atheros Proprietary Green Ethos™ Power Savigns Per Cable Length				
P_{1000F} 20m	1000Base Full Duplex 20m cable	121.5	2.7	401
P_{1000F} 20m	1000Base Idle 20m cable	103.8	4	342.5
P_{1000F} 100m	1000Base Full Duplex 100m cable	126	2.7	415.8
P_{1000F} 100m	1000Base Idle 100m cable	116.1	4	383.1
P_{1000F} 140m	1000Base Full Duplex 140m cable	144.2	2.7	475.9
P_{1000F} 140m	1000Base Idle 140m cable	133.8	4	441.5
RGMII + Fiber mode				
P_{1000F}	1000Base-X Full Duplex	45.7	2.7	150.8
$P_{1000idle}$	1000Base-X Idle	38.6	4	127.4
P_{100F}	100Base-X Full Duplex	30.3	3.5	100
$P_{100idle}$	100Base-X Idle	29.5	4	97.4
Converter mode				

Table 4-15. **Total System Power**

Symbol	Condition	Total Current (mA)	LED Consumption (mA)	Total Power Consumption w/o LED (mW)
P_{1000F}	1000Base Full Duplex	145.6	2.7	480.5
$P_{1000Idle}$	1000Base Idle	142.8	4	471.2
P_{100F}	100Base Full Duplex	57.6	3.5	190.1
$P_{100Idle}$	100Base Full Duplex	57.4	4	189.4
SGMII + Copper mode				
P_{1000F}	1000Base Full Duplex	145.6	2.7	480.5
$P_{1000Idle}$	1000Base Idle	143.6	4	178.2
P_{100F}	100Base Full Duplex	54	4	178.2
$P_{100Idle}$	100Base Full Duplex	52.6	4	173.6
802.3az Enabled				
$P_{1000Idle}$	1000Base Idle	44.6	4	147.2
$P_{100Idle}$	100Base Full Duplex	32.9	4	108.6

NOTE: Please note power consumption test results are based on demo board.

5. Register Descriptions

NOTE: the registers for advanced features such as 1588, 802.3az are not described in this document yet. These registers will be added in the next version of this document.

Table 5-1 shows the reset types used in this document.

Table 5-1. **Reset Types**

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to a zero and remains cleared until a read operation is performed through the management interface or a reset occurs.

Table 5-1. **Reset Types (continued)**

Type	Description
Retain	Value written to a register field takes effect without a software reset.
SC	Self-Clear. Writing a one to this register causes the desired function to execute immediately, and the register field clears to zero when the function is complete.
Update	The value written to the register field does not take effect until a software reset is executed. The value can still be read after it is written.

5.1 Register Summary

Table 5-2 summarizes the registers for the AR8031.

Table 5-2. **Register Summary**

Offset (Hex)	Register
0x00	Control (Copper or Fiber Pages)
0x01	Status
0x02	PHY identifier 1
0x03	PHY identifier 2
0x04	Auto-negotiation advertisement
0x05	Link partner ability (base page)
0x06	Auto-negotiation expansion
0x07	Next page transmit
0x08	Link partner next page
0x09	1000 Base-T control
0x0A	1000 Base-T status
0x0B	Reserved
0x0C	Reserved
0x0D	MMD access control
0x0E	MMD access address data
0x0F	Extended status
0x10	Function control
0x11	PHY-specific status
0x12	Interrupt enable
0x13	Interrupt status
0x14	Smart Speed
0x15	
0x16	Cable defect tester control

Table 5-2. **Register Summary (continued)**

Offset (Hex)	Register
0x017	
0x18	LED control
0x19	Manual LED override
0x1A	
0x1B	
0x1C	Cable defect tester status
0x1D	Debug port address offset
0x1E	Debug port data
0x1F	Chip Configure

5.1.1 Control Register — Copper Page

Offset: 0x00
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	Type		Description
15	RESET	Mode	R/W	PHY Software Reset. Writing a "1" to this bit causes the PHY the reset operation is done , this bit is cleared to "0" automatically. The reset occurs immediately. 1= PHY reset 0 =Normal operation
		HW Rst.	0	
		SW Rst.	SC	
14	LOOPBACK	Mode	R/W	When loopback is activated, the transmitter data presented on TXD is looped back to RXD internally. Link is broken when loopback is enabled. 1 = Enable Loopback 0 = Disable Loopback
		HW Rst.	0	
		SW Rst.	0	
13	SPEED SELECTION (LSB)	Mode	R/W	Upon hardware reset , this bit and 0.6 bit depend on anen(bit0.12) and SPEED_PAD(PAD in signal): anen = {0.6 , 0.13} 0 = SPEED_PAD[1:0] 1 = 2'b01 (00:10Mbps,01:100Mbps,10:1000Mbps,11:Reserved) When giga_dis_qual (register20.8) is high, this bit is forced to be low.
		HW Rst.	See Desc.	
		SW Rst.		
12	AUTO_ NEGOTIATION	Mode	RO	Upon hardware reset ,this bit depends on ANEN_PAD. 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
		HW Rst.	0	
		SW Rst.	0	

Bit	Name	Type		Description
11	POWER_DOWN	Mode	R/W	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0.15) and Restart Auto-Negotiation (0.9) are not set by the user. IEEE power down shuts down the chip except for the MAC interface if 16.3 is set to 1. If 16.3 is set to 0, then the MAC interface also shuts down. Power down also has no effect on the 125CLK output if 16.4 is set to 0. 1 = Power down 0 = Normal operation
		HW Rst.	0	
		SW Rst.	0	
10	ISOLATE	Mode	R/W	The GMII/MII/TBI output pins are tristated when this bit is set to 1. The GMII/MII/TBI inputs are ignored. 1 = Isolate 0 = Normal operation Not implemented.
		HW Rst.	0	
		SW Rst.	0	
9	RESTART_AUTO_ NEGOTIATION	Mode	R/W, SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation
		HW Rst.	0	
		SW Rst.	0	
8	DUPLEX MODE	Mode	R/W, SC	Upon hardware reset , this bit bit depend on DUPLEX_MODE_PAD and anen bit(0.12): 0.12 0.8 0 0 1 DUPLEX_MODE_PAD 1:Full Duplex 0 :Half Duplex
		HW Rst.	See Desc	
		SW Rst.		
7	COLLISION TEST	Mode	R/W	Setting this bit to 1 will cause the COL pin to assert whenever the TX_EN pin is asserted. 1 = Enable COL signal test 0 = Disable COL signal test
		HW Rst	0	
		SW Rst	0	
6	SPEED SELECTION (MSB)	Mode	R/W	See bit 0.13. If giga_dis_qual bit (20.10) is 1, then this bit is fixed to 0.
		HW Rst	See Desc.	
		SW Rst	0	
5:0	RES	Mode	R/O	Will always be 00000.
		HW Rst	00000	
		SW Rst	00000	

5.1.1 Control — Fiber Page

Offset: 0x00, or 0d00
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	Type		Description
15	Reset	Mode	R/W	PHY Software Reset. Writing a "1" to this bit causes the PHY the reset operation is done , this bit is cleared to "0" automatically. The reset occurs immediately. 1= PHY reset 0 =Normal operation
		HW Rst.	0	
		SW Rst.	SC	
14	Loopback	Mode	R/W	100fx, 1000bx, sgmii loopback.When loopback is activated, 10bit txd to serdes is looped back to 10bit rxd; 1 = Enable Loopback 0 = Disable Loopback
		HW Rst.	0	
		SW Rst.	0	
13	Speed Selection (LSB)	Mode	R/W	Only for sgmii; Force speed {bit 0.6, this bit} equals : 00 means 10Mbps; 01-means 100Mbps, 10-means1000Mbps 11-means Reserved; These force speed is only valid when 0.12 is 0.
		HW Rst.	1	
		SW Rst.	Retain	
12	Auto-negotiation	Mode	RO	For 1000bx, sgmii: 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process No auto-negotiation in 100fx.
		HW Rst.	0	
		SW Rst.	0	
11	Power Down	Mode	R/W	For 100fx, 1000bx, sgmii mode; When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0.15) and Restart Auto-Negotiation (0.9) are not set by the user. 1 = Power down, shut off serdes 0 = Normal operation
		HW Rst.	2'b10	
		SW Rst.	Retain	

Bit	Name	Type		Description
10	Isolate	Mode	R/W	Not implement.
		HW Rst.	0	
		SW Rst.	0	
9	Restart Auto-negotiation	Mode	R/W, SC	For 1000bx, sgmii.. Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation
		HW Rst.	0	
		SW Rst.	SC	
8	Duplex Mode	Mode	R/W, SC	Take effect in 1000BX auto-negotiation disable(this register bit12 is 0) mode, or 100fx mode, 1:Full Duplex 0 :Half Duplex
		HW Rst.	1	
		SW Rst.		
7	Collision Test	Mode	R/W	N/A
		HW Rst.	0	
		SW Rst.	0	
6	Speed Selection (MSB)	Mode	R/W	See bit 0.13.
		HW Rst.	See Desc.	
		SW Rst.		
5:0	Reserved	Mode	R/W	Will always be 00000.
		HW Rst.	0	
		SW Rst.	0	

5.1.1 Status Register — Copper Page

Offset: 0x01, or 0d01
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	Type		Description
15	100BASE-T4	Mode	RO	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
		HW Rst.	Always 0	
		SW Rst.	Always 0	
14	100BASE-X Full-Duplex	Mode	RO	Capable of 100-Tx Full Duplex operation
		HW Rst.	Always 1	
		SW Rst.	Always 1	
13	100BASE-X Half-Duplex	Mode	RO	Capable of 100-Tx Half Duplex operation
		HW Rst.	Always 1	
		SW Rst.	Always 1	
12	10 Mbps Full-Duplex	Mode	RO	Capable of 10Base-T full duplex operation
		HW Rst.	Always 1	
		SW Rst.	Always 1	
11	10 Mbs Half-Duplex	Mode	RO	Capable of 10Base-T half duplex operation
		HW Rst.	Always 1	
		SW Rst.	Always 1	
10	100BASE-T2 Full-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst.	Always 0	
		SW Rst.	Always 0	

Bit	Name	Type		Description
9	100BASE-T2 Half-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst.	Always 0	
		SW Rst.	Always 0	
8	Extended Status	Mode	RO	Extended status information in register15
		HW Rst.	Always 0	
		SW Rst.	Always 0	
7	Reserved	Mode	RO	Always be 0.
		HW Rst.	Always 0	
		SW Rst.	Always 0	
6	MF Preamble Suppression	Mode	RO	PHY accepts management frames with preamble suppressed
		HW Rst.	Always 1	
		SW Rst.	Always 1	
5	Auto-Negotiation Complete	Mode	RO	1: Auto negotiation process complete 0:Auto negotiation process not complete
		HW Rst.	0	
		SW Rst.	0	
4	Remote Fault	Mode	RO, LH	1: Remote fault condition detected 0:Remote fault condition not detected
		HW Rst.	0	
		SW Rst.	0	
3	Auto-Negotiation Ability	Mode	RO	1 : PHY able to perform auto negotiation
		HW Rst.	0	
		SW Rst.	0	
2	Link Status	Mode	RO, LL	This register bit indicates whether the link was lost since the last read. For the current link status, read register bit 17.10 Link Real Time. 1 = Link is up 0 = Link is down
		HW Rst.	0	
		SW Rst.	0	

Bit	Name	Type		Description
1	Jabber Detect	Mode	RO, LH	1: Jabber condition detected 0: Jabber condition not detected
		HW Rst.	0	
		SW Rst.	0	
0	Extended Capbility	Mode	RO	1: Extended register capabilities
		HW Rst.	Always 1	
		SW Rst.	Always 1	

5.1.1 Status Register — Fiber Page

Offset: 0x01, or 0d01
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	Type		Description
15	100BASE-T4	Mode	RO	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
		HW Rst.	Always 0	
		SW Rst.	Always 0	
14	100BASE-X Full-Duplex	Mode	RO	Capable of 100-Tx Full Duplex operation
		HW Rst.	Always 1	
		SW Rst.	Always 1	
13	100BASE-X Half-Duplex	Mode	RO	Capable of 100-Tx Half Duplex operation
		HW Rst.	Always 1	
		SW Rst.	Always 1	
12	10 Mbps Full-Duplex	Mode	RO	Capable of 10Base-T full duplex operation
		HW Rst.	Always 1	
		SW Rst.	Always 1	
11	10 Mbs Half-Duplex	Mode	RO	Capable of 10Base-T half duplex operation
		HW Rst.	Always 1	
		SW Rst.	Always 1	

Bit	Name	Type		Description
10	100BASE-T2 Full-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst.	Always 0	
		SW Rst.	Always 0	
9	100BASE-T2 Half-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst.	Always 1	
		SW Rst.	Always 1	
8	Extended Status	Mode	RO	Extended status information in register15
		HW Rst.	Always 1	
		SW Rst.	Always 1	
7	Reserved	Mode	RO	Always be 0.
		HW Rst.	Always 1	
		SW Rst.	Always 1	
6	MF Preamble Suppression	Mode	RO	PHY accepts management frames with preamble suppressed
		HW Rst.	Always 0	
		SW Rst.	Always 0	
5	Auto-Negotiation Complete	Mode	RO	1: Auto negotiation process complete 0:Auto negotiation process not complete
		HW Rst.	0	
		SW Rst.	0	
4	Remote Fault	Mode	RO, LH	1: Remote fault condition detected 0:Remote fault condition not detected
		HW Rst.	0	
		SW Rst.	0	
3	Auto-Negotiation Ability	Mode	RO	1 : PHY able to perform auto negotiation
		HW Rst.	Always 1	
		SW Rst.	Always 1	
2	Link Status	Mode	RO, LL	This register bit indicates whether the link was lost since the last read. For the current link status, read register bit 17.10 Link Real Time. 1 = Link is up 0 = Link is down
		HW Rst.	0	
		SW Rst.	0	

Bit	Name	Type		Description
1	Jabber Detect	Mode	RO, LH	1: Jabber condition detected 0: Jabber condition not detected
		HW Rst.	0	
		SW Rst.	0	
0	Extended Capbility	Mode	RO	1: Extended register capabilities
		HW Rst.	Always 1	
		SW Rst.	Always 1	

5.1.1 PHY Identifier

Offset: 0x02, or 0d02
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	Type		Description
15:0	Organizationally Unique Identifier Bit 3:18	Mode	RO	Organizationally Unique Identifier bits 3:18
		HW Rst.	Always 16'h004d	
		SW Rst.	Always 16'h004d	

5.1.1 PHY Identifier2

Offset: 0x03, or 0d03
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	Type		Description
15:0	Organizationally Unique Identifier Bit 3:18	Mode	RO	Organizationally Unique Identifier bits 3:18
		HW Rst.	Always 16'hd0XX	
		SW Rst.	Always 16'hd0XX	

5.1.1 Auto-Negotiation Advertisement Register — Copper Page

Offset: 0x04, or 0d04
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	Type		Description
15	Next page	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down If 1000BASE-T is advertised then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed. 1 = Advertise 0 = Not advertised
		HW Rst.	0	
		SW Rst.	Update	
14	Ack	Mode	RO	Must be 0
		HW Rst.	Always 0	
		SW Rst.	Always 0	
13	Remote Fault	Mode	R/W	1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
		HW Rst.	0	
		SW Rst.	Update	
12	xnp_able	Mode	RO	Extended next page enable control bi: 1 = Local device supports transmission of extended next pages; 0 = Local device does not support transmission of extended next pages.
		HW Rst.	Always 1	
		SW Rst.	Always 1	
11	Asymmetric Pause	Mode	R/w	Upon hardware reset , this bit depends on ASYM_PAUSE_PAD. The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Asymmetric Pause 0 = No asymmetric Pause
		HW Rst.	See Desc.	
		SW Rst.	Update	

Bit	Name	Type		Description
10	PAUSE	Mode	R/W	Upon hardware reset , this bit depends on PAUSE_PAD. The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
		HW Rst.	See Desc.	
		SW Rst.	Update	
9	100BASE-T4	Mode	RO	Not able to perform 100BASE-T4
		HW Rst.	Always 0	
		SW Rst.	Always 0	
8	100BASE-TX Full Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
		HW Rst.	1	
		SW Rst.	Update	
7	100BASE-TX Half Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
		HW Rst.	1	
		SW Rst.	Update	
6	10BASE-TX Full Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
		HW Rst.	1	
		SW Rst.	Update	

Bit	Name	Type		Description
5	10BASE-TX Half Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised
		HW Rst.	1	
		SW Rst.	Update	
4:0	Selector field	Mode	RO	Selector Field mode 00001 = 802.3
		HW Rst.	Always 00001	
		SW Rst.	Always 00001	

5.1.1 Auto-Negotiation Advertisement Register — Fiber Page

Offset: 0x04, or 0d04
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	Type		Description
15	Next page	Mode	R/W	This bit index if additional next pages are needed. 1 = Advertise 0 = Not advertised
		HW Rst.	0	
		SW Rst.	Update	
14	Ack	Mode	RO	Must be 0
		HW Rst.	Always 0	
		SW Rst.	Always 0	
13:12	Remote Fault	Mode	R/W	00 = LINK_OK 01=OFFLINE 10=LINK_FAILURE 11=AUTO_ERROR
		HW Rst.	0	
		SW Rst.	Update	
11:9	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst.	0	
8	Asymmetric Pause	Mode	R/W	Upon hardware reset , this bit depends on ASYM_PAUSE_PAD. 1 = Asymmetric Pause 0 = No asymmetric Pause
		HW Rst.	1	
		SW Rst.	Update	

Bit	Name	Type		Description
7	PAUSE	Mode	R/W	Upon hardware reset , this bit depends on PAUSE_PAD. 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
		HW Rst.	1	
		SW Rst.	Update	
6	1000BASE-X half duplex	Mode	R/W	1000BASEX half duplex ability.
		HW Rst.	See Desc.	
		SW Rst.	Update	
5	1000BASE-X full duplex	Mode	R/W	1000BASEX full duplex ability.
		HW Rst.	1	
		SW Rst.	Update	
4:0	Reserved	Mode	RO	
		HW Rst.	Always 00001	
		SW Rst.	Always 00001	

5.1.1 Link Partner Ability Register — Copper Page

Offset: 0x05, or 0d05
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	Type		Description
15	Next page	Mode	RO	Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
		HW Rst.	0	
		SW Rst.	0	
14	Ack	Mode	RO	Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner does not have Next Page ability
		HW Rst.	0	
		SW Rst.	0	
13	Remote Fault	Mode	RO	Remote Fault Received Code Word Bit 13 1 = Link partner detected remote fault 0 = Link partner has not detected remote fault
		HW Rst.	0	
		SW Rst.	0	
12	Reserved	Mode	RO	Technology Ability Field Received Code Word Bit 12
		HW Rst.	0	
		SW Rst.	0	

Bit	Name	Type		Description
11	Asymmetric Pause	Mode	RO	Technology Ability Field Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
		HW Rst.	0	
		SW Rst.	0	
10	PAUSE	Mode	RO	Technology Ability Field Received Code Word Bit 10 1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation
		HW Rst.	0	
		SW Rst.	0	
9	100BASE-T4	Mode	RO	Technology Ability Field Received Code Word Bit 9 1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable
		HW Rst.	0	
		SW Rst.	0	
8	100BASE-TX Full Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 8 1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable
		HW Rst.	0	
		SW Rst.	0	
7	100BASE-TX Half Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 7 1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner is not 100BASE-TX half-duplex capable
		HW Rst.	0	
		SW Rst.	0	
6	10BASE-TX Full Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 6 1 = Link partner is 10BASE-T full-duplex capable 0 = Link partner is not 10BASE-T full-duplex capable
		HW Rst.	0	
		SW Rst.	0	
5	10BASE-TX Half Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 5 1 = Link partner is 10BASE-T half-duplex capable 0 = Link partner is not 10BASE-T half-duplex capable
		HW Rst.	0	
		SW Rst.	0	
4:0	Selector field	Mode	RO	Selector Field Received Code Word Bit 4:0
		HW Rst.	00000	
		SW Rst.	00000	

5.1.1 Link Partner Ability Register — Fiber Page

Offset: 0x05, or 0d05
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	Type		Description
15	Next page	Mode	RO	Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
		HW Rst.	0	
		SW Rst.	0	
14	Ack	Mode	RO	Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner does not have Next Page ability
		HW Rst.	0	
		SW Rst.	0	
13:12	Remote Fault	Mode	RO	Remote Fault Received Code Word Bit 13,12
		HW Rst.	0	
		SW Rst.	0	
11:9	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
8	Asymmetric Pause	Mode	RO	Technology Ability Field Received Code Word Bit 8 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
		HW Rst.	0	
		SW Rst.	0	
7	PAUSE	Mode	RO	Technology Ability Field Received Code Word Bit 7 1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation
		HW Rst.	0	
		SW Rst.	0	
6	1000BASEX Half duplex	Mode	RO	Technology Ability Field Received Code Word Bit 6 1 = Link partner is 1000BASEX half dupelx capable 0 = Link partner is not 1000BASEX half duplex capable
		HW Rst.	0	
		SW Rst.		
5	1000BASEX full duplex	Mode	RO	Technology Ability Field Received Code Word Bit 6 1 = Link partner is 1000BASEX full dupelx capable 0 = Link partner is not 1000BASEX full duplex capable
		HW Rst.	0	
		SW Rst.	0	
4:0	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

5.1.1 Auto-Negotiation Expansion Register — Copper Page

Offset: 0x06, or 0d06
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	Type		Description
15:5	Reserved	Mode	RO	Reserved. Must be 0.
		HW Rst.	0x000	
		SW Rst.	0x000	
4	Parallel Detection fault	Mode	RO	1: a fault has been detect 0: no fault has been detected
		HW Rst.	0	
		SW Rst.	0	
3	Link partner next page able	Mode	RO	1: Link partner is Next page able 0: Link partner is not next page able
		HW Rst.	0	
		SW Rst.	0	
2	Local Next Page able	Mode	RO	1 = Local Device is Next Page able
		HW Rst.	1	
		SW Rst.	1	
1	Page received	Mode	RO, LH	1: A new page has been received 0: No new page has been received
		HW Rst.	0	
		SW Rst.	0	
0	Link Partner Auto - negotiation able	Mode	RO	1: Link partner is auto negotiation able 0: Link partner is not auto negotiation able
		HW Rst.	0	
		SW Rst.	0	

5.1.1 Auto-Negotiation Expansion Register — Fiber Page

Offset: 0x06, or 0d06
Mode: Read/Write
Hardware Reset: 0
Software Reset: See field descriptions

Bit	Name	Type		Description
15:4	Reserved	Mode	RO	Reserved. Must be 0.
		HW Rst.	0x000	
		SW Rst.	0x000	
3	Link partner next page able	Mode	RO	For 1000bx, sgmii; 1: Link partner is Next page able 0: Link partner is not next page able
		HW Rst.	0	
		SW Rst.	0	
2	Local Next Page able	Mode	RO	For 1000bx, sgmii; 1 = Local Device is Next Page able
		HW Rst.	0	
		SW Rst.	0	
1	Page received	Mode	RO	For 1000bx, sgmii; 1: A new page has been received 0: No new page has been received
		HW Rst.	1	
		SW Rst.	1	
0	Link Partner Auto negotiation able	Mode	RO, LH	For 1000bx, sgmii; 1: Link partner is auto negotiation able 0: Link partner is not auto negotiation able
		HW Rst.	0	
		SW Rst.	0	

5.1.1 Next Page Transmit Register — Copper Page

Offset: 0x07, or 0d07

Bit	Name	Type		Description
15	Next Page	Mode	R/W	Transmit Code Word Bit 15
		HW Rst.	0	
		SW Rst.	0	
14	Reserved	Mode	R/W	Transmit Code Word Bit 14
		HW Rst.	0	
		SW Rst.	0	
13	Message page mode	Mode	R/W	Transmit Code Word Bit 13
		HW Rst.	0	
		SW Rst.	0	
12	Ack2	Mode	R/W	Transmit Code Word Bit 12
		HW Rst.	1	
		SW Rst.	1	
11	Toggle	Mode	RO	Transmit Code Word Bit 11
		HW Rst.	1	
		SW Rst.	1	
10:0	Message/Unformatted Field	Mode	R/W	Transmit Code Word Bit 10:0
		HW Rst.	0x001	
		SW Rst.	0x001	

5.1.1 Next Page Transmit Register — Fiber Page for 1000Base-X, SGMII

Offset: 0x07, or 0d07

Bit	Name	Type		Description
15	Next Page	Mode	R/W	Transmit Code Word Bit 15
		HW Rst.	0	
		SW Rst.	0	
14	Reserved	Mode	R/W	Transmit Code Word Bit 14
		HW Rst.	0	
		SW Rst.	0	
13	Message page mode	Mode	R/W	Transmit Code Word Bit 13
		HW Rst.	0	
		SW Rst.	0	
12	Ack2	Mode	R/W	Transmit Code Word Bit 12
		HW Rst.	1	
		SW Rst.	1	
11	Toggle	Mode	RO	Transmit Code Word Bit 11
		HW Rst.	1	
		SW Rst.	1	
10:0	Message/Unformatted Field	Mode	R/W	Transmit Code Word Bit 10:0
		HW Rst.	0x001	
		SW Rst.	0x001	

5.1.1 Link Partner Next Page Register — Copper Page

Offset: 0x08, or 0d08

Bit	Name	Type		Description
15	Next Page	Mode	R/W	Received Code Word Bit 15
		HW Rst.	0	
		SW Rst.	0	
14	Reserved	Mode	R/W	Received Code Word Bit 14
		HW Rst.	0	
		SW Rst.	0	
13	Message page mode	Mode	R/W	Received Code Word Bit 13
		HW Rst.	0	
		SW Rst.	0	
12	Ack2	Mode	R/W	Received Code Word Bit 12
		HW Rst.	1	
		SW Rst.	1	
11	Toggle	Mode	RO	Received Code Word Bit 11
		HW Rst.	1	
		SW Rst.	1	
10:0	Message/Unformatted Field	Mode	R/W	Received Code Word Bit 10:0
		HW Rst.	0x001	
		SW Rst.	0x001	

5.1.1 Link Partner Next Page Register — Fiber Page for 1000Base-X, SGMII

Offset: 0x08, or 0d08

Bit	Name	Type		Description
15	Next Page	Mode	R/W	Received Code Word Bit 15
		HW Rst.	0	
		SW Rst.	0	
14	Reserved	Mode	R/W	Received Code Word Bit 14
		HW Rst.	0	
		SW Rst.	0	
13	Message page mode	Mode	R/W	Received Code Word Bit 13
		HW Rst.	0	
		SW Rst.	0	
12	Ack2	Mode	R/W	Received Code Word Bit 12
		HW Rst.	1	
		SW Rst.	1	
11	Toggle	Mode	RO	Received Code Word Bit 11
		HW Rst.	1	
		SW Rst.	1	
10:0	Message/Unformatted Field	Mode	R/W	Received Code Word Bit 10:0
		HW Rst.	0x001	
		SW Rst.	0x001	

5.1.1 1000Base-T Control Register

Offset: 0x09, or 0d09

Bit	Name	Type		Description
15:13	Test mode	Mode	R/W	TX_TCLK comes from the RX_CLK pin for jitter testing in test modes 2 and 3. After exiting the test mode, hardware reset or software reset (register 0.15) should be issued to ensure normal operation. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 101, 110, 111 = Reserved
		HW Rst.	000	
		SW Rst.	Retain	
12	Master/Slave Manual configuration Enable	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration
		HW Rst.	0	
		SW Rst.	Update	
11	Master/Slave configuration	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down Register 9.11 is ignored if register 9.12 is equal to 0. 1 = Manual configure as MASTER 0 = Manual configure as SLAVE
		HW Rst.	0	
		SW Rst.	Update	
10	Port Type	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down Register 9.10 is ignored if register 9.12 is equal to 1. 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE)
		HW Rst.	0	
		SW Rst.	Update	

Bit	Name	Type		Description
9	1000BASE-T Full Duplex	Mode	RO	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised When giga_dis_qual(register20.8) is high, this bit is forced to be low.
		HW Rst.	1	
		SW Rst.	Update	
8	1000BASE-T Half-Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: o Software reset is asserted (register 0.15) o Restart Auto-Negotiation is asserted (register 0.9) o Power down (register 0.11) transitions from power down to normal operation o Link goes down 1 = Advertise 0 = Not advertised Note: the default setting is no 1000 baset/half duplex advertised When giga_dis_qual(register20.8) is high, this bit is forced to be low.
		HW Rst.	0	
		SW Rst.	Update	
7:0	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst.	0	

5.1.1 1000Base-T Status Register

Offset: 0x0A, or 0d10

Bit	Name	Type		Description
15	Master/Slave Configuration Fault	Mode	RO, LH	This register bit will clear on read 1: Master/Slave configuration fault detected 0: No fault detected
		HW Rst.	0	
		SW Rst.	0	
14	Master/Slave Configuration Resolution	Mode	RO	This register bit is not valid until register 6.1 is 1. 1: Local PHY cnfiguration resolved to Master 0: Local PHY cnfiguration resolved to Slave
		HW Rst.	0	
		SW Rst.	0	
13	Local Receiver Status	Mode	RO	1:Local Receiver OK 0:Local Receiver Not OK
		HW Rst.	0	
		SW Rst.	0	
12	Remote Receiver Status	Mode	R/W	1:Remote Receiver OK 0:Remote Receiver Not OK
		HW Rst.	0	
		SW Rst.	0	
11	Link Partner 1000Base-T Full Duplex Capability	Mode	RO	This register bit is not valid until register 6.1 is 1. 1: Link Partner is capable of 1000Base-T half duplex 0: Link Partner is not capable of 1000Base-T half duplex
		HW Rst.	0	
		SW Rst.	0	
10	Link Partner 1000Base-T Half Duplex Capability	Mode	R/W	This register bit is not valid until register 6.1 is 1. 1: Link Partner is capable of 1000Base-T full duplex 0: Link Partner is not capable of 1000Base-T full duplex
		HW Rst.	Always 0	
		SW Rst.	0	
9:8	Reserved	Mode	RO	Reserved.
		HW Rst.	Always 0	
		SW Rst.	Always 0	
7:0	Idle Error Count	Mode	RO, SC	MSB of Idle Error Counter These register bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and will not roll over.
		HW Rst.	0	
		SW Rst.	0	

5.1.1 MMD Access Control Register

Offset: 0x0D, or 0d13

Bit	Name	Type		Description
15:14	Function	Mode	RO, LH	00=address 01=data,no post increment 10=data,post increment on reads and writes 11=data,post increment on writes only;
		HW Rst.	0	
		SW Rst.	0	
13:5	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
4:0	DEVAD	Mode	R/W	Device address
		HW Rst.	0	
		SW Rst.	Update	

5.1.1 MMD Access Access Address Data Register

Offset: 0x0E, or 0d14

Bit	Name	Type		Description
15:14	Address data	Mode	R/W	If register13.15:14=00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register
		HW Rst.	00	
		SW Rst.	Retain	

5.1.1 Extended Status Register

Offset: 0x0F, or 0d15

Bit	Name	Type		Description
15	1000BASE-X Full Duplex	Mode	RO	PHY not able to perform 1000BASE-X Full Duplex
		HW Rst.	Always 1	
		SW Rst.	Always 0	
14	1000BASE-X Half Duplex	Mode	RO	PHY not able to perform 1000BASE-X Half Duplex
		HW Rst.	Always 0	
		SW Rst.	Always 0	
13	1000BASE-T Full-Duplex	Mode	RO	PHY able to perform 1000BASE-T Full Duplex
		HW Rst.	Always 1	
		SW Rst.	Always 1	
12	1000BASE-T Half-Duplex	Mode	R/W	PHY not able to perform 1000BASE-T Half Duplex
		HW Rst.	Always 0	
		SW Rst.	Always 0	
11:0	Reserved	Mode	RO	Reserved.
		HW Rst.	Always 0	
		SW Rst.	Always 0	

5.1.1 Extended Status Register

Offset: 0x10, or 0d16

Bit	Name	Type		Description
15:12	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst.	Retain	
11	Assert CRS on Transmit	Mode	RO	This bit has effect only in 10BT half-duplex mode: 1 = assert on Transmitting or receving; 0 = Never assert on Transmitting,only assert on receiving.
		HW Rst.	1	
		SW Rst.	Retain	
10	Force_link	Mode	R/W	1 = when an_en bit (0.12) is 1, force 10BT link up; 0 = Normal mode;
		HW Rst.	0	
		SW Rst.	Retain	
9:7	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst.	Retain	
6:5	MDI Crossover Mode	Mode	R/W	Changes to these bits are disruptive to the normal operation; therefore any changes to these registers must be followed by a software reset to take effect. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
		HW Rst.	11	
		SW Rst.	Update	
4:3	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
2	SQE Test	Mode	R/W	SQE Test is automatically disabled in full-duplex mode regardless of the state of register 16.2 1 = SQE test enabled 0 = SQE test disabled
		HW Rst.	0	
		SW Rst.	Retain	
1	Polarity Reversal	Mode	R/W	If polarity is disabled, then the polarity is forced to be normal in 10BASE-T. 1 = Polarity Reversal Disabled 0 = Polarity Reversal Enabled
		HW Rst.	1	
		SW Rst.	Retain	
0	Disable Jabber	Mode	RO	Jabber has effect only in 10BASE-T half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function
		HW Rst.	0	
		SW Rst.	Retain	

5.1.1 PHY-Specific Status Register — Copper Page

Offset: 0x10, or 0d16

Bit	Name	Type		Description
15:14	Speed	Mode	R/W	These status bits are valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
		HW Rst.	0	
		SW Rst.	Retain	
13	Duplex	Mode	RO	This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
		HW Rst.	1	
		SW Rst.	Retain	
12	Page Received (real-time)	Mode	R/W	1 = Page received 0 = Page not received
		HW Rst.	0	
		SW Rst.	Retain	
11	Speed and Duplex Resolved	Mode	R/W	When Auto-Negotiation is not enabled ,17.11 = 1 for force speed mode. 1 = Resolved 0 = Not resolved
		HW Rst.	0	
		SW Rst.	0	
10	Link (real-time)	Mode	R/W	1 = Link up 0 = Link down
		HW Rst.	0	
		SW Rst.	0	
9:7	Reserved	Mode	RO	Always 0
		HW Rst.	0	
		SW Rst.	0	
6	MDI Crossover Status	Mode	R/W	This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. This bit is 0 or 1 depending on what is written to 16.6:5 in manual configuration mode. Register 16.6:5 are updated with software reset. 1 = MDIX 0 = MDI
		HW Rst.	0	
		SW Rst.	Retain	
5	Wirespeed downgrade	Mode	R/W	1 = Downgrade 0 = No Downgrade
		HW Rst.	1	
		SW Rst.	Retain	
4	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	Retain	

Bit	Name	Type		Description
3	Transmit Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed; While in force mode, this bit is set to be 0. 1 = Transmit pause enabled 0 = Transmit pause disabled
		HW Rst.	0	
		SW Rst.	Retain	
2	Receive Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed; While in force mode, this bit is set to be 0. 1 = Receive pause enabled 0 = Receive pause disabled
		HW Rst.	0	
		SW Rst.	Retain	
1	Polarity (real time)	Mode	RO	1 = Reverted. 0 = Normal
		HW Rst.	0	
		SW Rst.	Retain	
0	Jabber (real time)	Mode	RO	1 = Jabber 0 = No jabber
		HW Rst.	0	
		SW Rst.	Retain	

5.1.1 PHY-Specific Status Register — Fiber Page

Offset: 0x11, or 0d17

Bit	Name	Type		Description
15:14	Speed	Mode	R/W	11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
		HW Rst.	0	
		SW Rst.	Retain	
13	Duplex	Mode	RO	1 = Full-duplex 0 = Half-duplex
		HW Rst.	1	
		SW Rst.	Retain	
12	Page Received (real-time)	Mode	R/W	1 = Page received 0 = Page not received
		HW Rst.	0	
		SW Rst.	Retain	
11	Speed and Duplex Resolved	Mode	R/W	When Auto-Negotiation is not enabled ,17.11 = 1 for force speed mode. 1 = Resolved 0 = Not resolved
		HW Rst.	0	
		SW Rst.	0	
10	Link (real-time)	Mode	R/W	For 1000bx, 100fx; 1 = Link up 0 = Link down
		HW Rst.	0	
		SW Rst.	0	
9	mr_an_complete	Mode	RO	For 1000bx,sgmii: 1=autoneg complete 0=autoneg not complete
		HW Rst.	0	
		SW Rst.	0	
8	Sync_status	Mode	RO	Only for 1000BX 1=sgmii_basex is sync 0=sgmii_basex is not sync
		HW Rst.	0	
		SW Rst.	0	
7:4	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst.	0	
3	Transmit Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed; While in force mode, this bit is set to be 0. 1 = Transmit pause enabled 0 = Transmit pause disabled
		HW Rst.	0	
		SW Rst.	Retain	

Bit	Name	Type		Description
2	Receive Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed; While in force mode, this bit is set to be 0. 1 = Receive pause enabled 0 = Receive pause disabled
		HW Rst.	0	
		SW Rst.	Retain	
1:0	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

5.1.1 Interrupt Enable Register

Offset: 0x12, or 0d18

Bit	Name	Type		Description
15	Auto-Negotiation Error	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
14	Speed Changed	Mode	RO	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
13	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst.	Retain	
12	Page Received	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
11	Link Fail Interrupt	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	0	
10	Link Success Interrupt	Mode	RO	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	0	
9	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
8	Link_fail_bx	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	0	
7	Link_success_bx	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
6	MDI Crossover Changed	Mode	RO	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
5	Wirespeed-downgrade Interrupt	Mode	RO, LH	P1588
		HW Rst.	0	
		SW Rst.	Retain	

Bit	Name	Type		Description
4	int_10ms_ptx	Mode	RO	P1588
		HW Rst.	0	
		SW Rst.	0	
3	Int_rx_ptp	Mode	RO, LH	1 = Polarity Changed 0 = Polarity not changed
		HW Rst.	0	
		SW Rst.	Retain	
2	Int_tx_ptp	Mode	RO, LH	P1588
		HW Rst.	0	
		SW Rst.	Retain	
1	Polarity Changed	Mode	R/W	1 = Polarity Changed 0 = Polarity not changed
		HW Rst.	0	
		SW Rst.	Retain	
0	int_wol_ptp	Mode	R/W	P1588
		HW Rst.	0	
		SW Rst.	Retain	

5.1.1 Interrupt Status Register

Offset: 0x13, or 0d19

Bit	Name	Type		Description
15	Auto-Negotiation Error	Mode	R0, LH	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
14	Speed Changed	Mode	RO, LH	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
13	Reserved	Mode	RO, LH	
		HW Rst.	0	
		SW Rst.	0	
12	Page Received	Mode	RO, LH	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
11	Link Fail Interrupt	Mode	RO, LH	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
10	Link Success Interrupt	Mode	RO	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	0	
9	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
8	Link_fail_bx	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	0	
7	Link_success_bx	Mode	R/W	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
6	MDI Crossover Changed	Mode	RO	1 = Interrupt enable 0 = Interrupt disable
		HW Rst.	0	
		SW Rst.	Retain	
5	Wirespeed-downgrade Interrupt	Mode	RO, LH	P1588
		HW Rst.	0	
		SW Rst.	Retain	

Bit	Name	Type		Description
4	int_10ms_ptx	Mode	RO	P1588
		HW Rst.	0	
		SW Rst.	0	
3	Int_rx_ptp	Mode	RO, LH	1 = Polarity Changed 0 = Polarity not changed
		HW Rst.	0	
		SW Rst.	Retain	
2	Int_tx_ptp	Mode	RO, LH	P1588
		HW Rst.	0	
		SW Rst.	Retain	
1	Polarity Changed	Mode	R/W	1 = Polarity Changed 0 = Polarity not changed
		HW Rst.	0	
		SW Rst.	Retain	
0	int_wol_ptp	Mode	R/W	P1588
		HW Rst.	0	
		SW Rst.	Retain	

5.1.1 Smart Speed Register

Offset: 0x14, or 0d20

Bit	Name	Type		Description
15:11	Rreserved	Mode	R0	Reserved. Must be 00000000.
		HW Rst.	0	
		SW Rst.	0	
10	aneg_now_qual	Mode	R/W	A rise of input pin "aneg_now" will set this bit to 1'b1, and cause PHY to restart auto-negotiation. Self-clear.
		HW Rst.	1’b0	
		SW Rst.	Update	
9	Rev_aneg_qual	Mode	R/W	Make PHY to auto-negotiate in reversed mode. This bit takes its value from the input pin "rev_aneg" upon following: 1 HW reset(fall of rst_dsp_i); 2 PHY SW reset; 3 Rise of input pin aneg_now.
		HW Rst.	1’b0	
		SW Rst.	Update	
8	Giga_dis_qual	Mode	R/W	Make PHY to disable GIGA mode. This bit takes its value from the input pin "giga_dis" upon following: 1 HW reset(fall of rst_dsp_i); 2 PHY SW reset; 3 Rise of input pin aneg_now.
		HW Rst.	1’b0	
		SW Rst.	Update	
7	Cfg_pad_en	Mode	R/W	The default value is zero; if this bit is set to one, then the auto negotiation Arbitration FSM will bypass the LINK_STATUS_CHECK state when the 10 baset/100 baset ready signal is asserted.
		HW Rst.	0	
		SW Rst.	Update	
6	Mr_ltdis	Mode	R/W	The default value is zero; if this bit is set to one, then the NLP Receive Link Integrity Test FSM will stays at the NLP_TEST_PASS state.
		HW Rst.	0	
		SW Rst.	Update	
5	Smartspeed_en	Mode	R/W	The default value is one; if this bit is set to one and cable inhibits completion of the training phase, then After a few failed attempts, the Attansic card automatically downgrades the highest ability to the next lower speed: from 1000 to 100 to 10.
		HW Rst.	1	
		SW Rst.	Update	
4:2	Smartspeed_retry_limit	Mode	R/W	The default value is three; if these bits are set to three, then the Attansic card will attempt five times before downgrading; The number of attempts can be changed through setting these bits.
		HW Rst.	011	
		SW Rst.	Update	
1	Bypass_smartspeed_timer	Mode	R/W	The default value is zero; if this bit is set to one, the Smartspeed FSM will bypass the timer used for stablility.
		HW Rst.	0	
		SW Rst.	Update	
0	reserved	Mode	RO	Reserved. Must be 0.
		HW Rst.	0	
		SW Rst.	0	

5.1.1 Virtual Cable Tester Control Register

Offset: 0x16, or 0d22

Bit	Name	Type		Description
15:10	Reserved	Mode	R0	Reserved.
		HW Rst.	Always 0	
		SW Rst.	Always 0	
9:8	MDI Pair Select	Mode	R/W	Virtual Cable Tester™ Control registers. Use the Virtual Cable Tester Control Registers to select which MDI pair is shown in the Virtual Cable Tester Status register. 00 = MDI[0] pair 01 = MDI[1] pair 10 = MDI[2] pair 11 = MDI[3] pair
		HW Rst.	00	
		SW Rst.	Retain	
7:1	Reserved	Mode	R/W	Always 0
		HW Rst.	0	
		SW Rst.	0	
0	Enable Test	Mode	R/W	When set, hardware automatically disable this bit when VCT is done. 1 = Enable VCT Test 0 = Disable VCT Test
		HW Rst.	0	
		SW Rst.	Retain	

5.1.2 LED Control

Offset: 0x018, or 0d24

Bit	Name	Type		Description	
15	Disable LED	Mode	R/W	Control the output LED pins: led_link10_100n_o, led_link1000n_o(when in attansic mode), led_actn_o.	
		HW Rst.	0	0	Enable
		SW Rst	Retain	1	Disable
14:12	Led on time	Mode	R/W	000 = 5 ms 001 = 10ms 010 = 21 ms 011 = 42ms 100 = 84 ms 101 = 168ms 110 to 111 = 42ms	
		HW Rst.	011		
		SW Rst	Retain		
11	Force Interrupt	Mode	RO	Always 0	
		HW Rst.	0		
		SW Rst	0		
10:8	Led off time	Mode	R/W	000 = 21 ms 001 = 42 ms 010 = 84 ms 011 =168 ms 100 =330 ms 101 = 670 ms 110 to 111 = 168ms	
		HW Rst.	010		
		SW Rst	Retain		
7:5	Reserved	Mode	RO	Reserved	
		HW Rst.	0		
		SW Rst	Always 0		
4:3	LED_LINK control	Mode	R/W	00 = Direct LED mode 11 = Master/Slave LED mode 01, 10 = Combined LED modes	
		HW Rst.	0		
		SW Rst	Retain		
2	LED_DUPLEX control	Mode	R/W	0 = Duplex 1 = Duplex/Collision	
		HW Rst.	0		
		SW Rst	Retain		
1	LED_RX control	Mode	R/W	0 = Receive activity/Link 1 = Receive activity	
		HW Rst.	0		
		SW Rst	Retain		
0	LED_TX Control	Mode	R/W	0 = Activity/Link 1 = Transmit activity	
		HW Rst.	0		
		SW Rst	Retain		

5.1.3 Manual LED override register

Offset: 0x19, or 0d25

Bit	Name	Type		Description
15:14	Conv_led_sel	Mode	R/W	Not used in BASET_RGMII, BASET_RMII, BASET_SGMII mode, in these mode, LED pins controlled by copper. Not used in BX1000_RGMII, FX100_RGMII mode, in these mode, LED pins are controlled by fiber; The two bits control LED behavior In BX1000_CONV, FX100_CONV, convertor mode: 2'b00: LED pins controlled by fiber 2'b11: LED pins controlled by copper; because of convertor's FEF, if fiber is not link up, then copper would also be link down. So there's no probability that only copper is link up. So when both fiber and copper link up, link led is on. 2'b01: When both fiber and copper link up, link led is on 2'b10: either fiber or copper link is up, link led is on
		HW Rst.	00	
		SW Rst.	Retain	
13:12	Reserved	Mode	R/W	Reserved.
		HW Rst.	00	
		SW Rst.	Retain	
11:10	LED_ DUPLEX	Mode	R/W	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
		HW Rst.	00	
		SW Rst.	Retain	
9:8	LED_LINK10	Mode	R/W	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
		HW Rst.	00	
		SW Rst.	Retain	
7:6	LED_LINK100	Mode	R/W	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
		HW Rst.	00	
		SW Rst.	Retain	
5:4	LED_LINK1000	Mode	R/W	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
		HW Rst.	00	
		SW Rst.	Retain	

Bit	Name	Type		Description
3:2	LED_RX	Mode	R/W	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
		HW Rst.	00	
		SW Rst.	Retain	
1:0	LED_TX	Mode	R/W	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
		HW Rst.	00	
		SW Rst.	Retain	

5.1.4 Copper/Fiber Status Register

Offset: 0x01B, or 0d27

Bit	Name	Type		Description
15:14	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst	0	
13	Transmit_pause _en_bx	Mode	R/W	
		HW Rst.	0	
		SW Rst	0	
12	Receive_pause _en_bx	Mode	RO	
		HW Rst.	0	
		SW Rst	0	
11	Link_established _bx	Mode	R/W	link status of fiber
		HW Rst.	0	
		SW Rst	0	
10	fd_mode_bx	Mode	RO	duplex mode of fiber
		HW Rst.	0	
		SW Rst	Always 0	
9:8	speed_mode_bx	Mode	R/W	Speed_mode of fiber, only 2 cases: 2b'10 : 1000Bx 2'b01: 100FX
		HW Rst.	2’b10	
		SW Rst	2’b10	
7:6	Reserved	Mode	R/W	
		HW Rst.	0	
		SW Rst	0	
5	Transmit_pause _en_bt	Mode	R/W	
		HW Rst.	0	
		SW Rst	0	

Bit	Name	Type		Description
4	Receive_pause _en_bt	Mode	R/W	
		HW Rst.	0	
		SW Rst	0	
3	Link_established _bt	Mode	R/W	Link status of copper
		HW Rst.	0	
		SW Rst	0	
2	fd_mode_bt	Mode	R/W	Duplex mode of copper
		HW Rst.	0	
		SW Rst	0	
1:0	speed_mode_bt	Mode	R/W	Speed_mode of copper: 2'b00:10BT, 2'b01:100BT, 2'b10:1000BT, 2'b11:reserved;
		HW Rst.	0	
		SW Rst	0	

5.1.5 Virtual Cable Tester Status register

Offset: 0x1C, or 0d28

Bit	Name	Type		Description
15:10	Reserved	Mode	RO	Reserved.
		HW Rst.	Always 0	
		SW Rst.	Always 0	
9:8	Status	Mode	RO	The content of the Virtual Cable Tester Status Registers applies to the cable pair selected in the Virtual Cable Tester™ Control Registers. 11 = Test Fail 00 = Valid test, normal cable (no short or open in cable) 10 = Valid test, open in cable (Impedance > 333 ohms) 01 = Valid test, short in cable (Impedance < 33 ohms)
		HW Rst.	00	
		SW Rst.	00	
7:0	Delta_Time	Mode	R/W	Delta time to indicate distance.
		HW Rst.	0	
		SW Rst.	0	

5.1.6 Debug port (Address offset set)

Offset: 0x1D, or 0d29

Bit	Name	Type		Description
15:6	Reserved	Mode	RO	The address index of the register will be write or Read.
		HW Rst.	0	
		SW Rst.	0	
5:0	Address Offset	Mode	R/W	The address index of the register will be write or Read.
		HW Rst.	0	
		SW Rst.	0	

5.1.7 Debug port2 (R/W port)

Offset: 0x1E, or 0d30

Bit	Name	Type		Description
15:0	Debug data port	Mode	R/W	The data port of debug register. Before access this register, must set the address offset first.
		HW Rst.	0	
		SW Rst.	0	

5.1.8 Debug port2 (R/W port)

Offset: 0x1E, or 0d30

Bit	Name	Type		Description
15:0	Debug data port	Mode	R/W	The data port of debug register. Before access this register, must set the address offset first.
		HW Rst.	0	
		SW Rst.	0	

5.1.9 Chip Configure Register

Offset: 0x1F, or 0d31

Bit	Name	Type		Description
15	Bt_bx_reg_sel	Mode	R/W	POS pin. Copper_pgae , fiber page select bit: 1'b1, select copper page registers; 1'b0, select fiber page registers;
		HW Rst.	See Desc.	
		SW Rst.	Retain	
14	Reserved	Mode	RO	Reserved.
		HW Rst.	0	
		SW Rst.	0	
13	Sgmii_rximp_ 50_75	Mode	R/W	POS pin. Rx impedance of serdes 1'b1: 75Ω 1'b0: 50Ω
		HW Rst.	0	
		SW Rst.	0	
12	Sgmii_tximp_ 50_75	Mode	R/W	POS pin. Tx impedance of serdes 1'b1: 75Ω 1'b0: 50Ω
		HW Rst.	0	
		SW Rst.	0	
11	Prbs_en	Mode	R/W	Control prbs test in sgmii
		HW Rst.	0	
		SW Rst.	Retain	
10:4	Reserved	Mode	RO	0
		HW Rst.	0	
		SW Rst.	0	
3:0	Mode_cfg	Mode	R/W	POS pin. Chip mode configure bits; 4'b1000: ECNC_TEST; 4'b1001:SCAN_TEST; 4'b1010:IDDQ_TEST; 4'b0000:BASET_RGMII 4'b0001:BASET_SGMII; 4'b1110:FX100_RGMII_75; 4'b0110:FX100_RGMII_50; 4'b1111:FX100_CONV_75; 4'b0111:FX100_CONV_50; 4'b0011:BX1000_RGMII_75; 4'b0010:BX1000_RGMII_50; 4'b0101:BX1000_CONV_75; 4'b0100:BX1000_CONV_50; 4'b1011:CFG_RESV1; 4'b1100:BASET_RMII1; 4'b1101:BASET_RMII2.
		HW Rst.	See Desc.	
		SW Rst.	Retain	

5.2 Debug Register Descriptions

Table 5-3 summarizes the debug registers for the AR8031.

Table 5-3. **Debug Register Summary**

Offset	Register
0x00	Analog test control
0x05	SERDES test and system mode control
0x10	100 BASE-Tx test mode select
0x11	hib timer selection
0x12	Test configuration for 10 BASE-T
0x1F	PHY_Control debug Register0
0x29	Power saving control

5.2.10 Analog Test Control

Offset: 0x00 (Hex), or 0 (Decimal)

Bit	Name	Type		Description
15	Sel_clk125m_dsp	Mode	R/W	Control bit for rgmii interface rx clock delay: 1 = rgmii rx clock delay enable 0 = rgmii rx clock delay disable
		HW Rst.	1	
		SW Rst.	0	
14:0	Reserved	Mode	RO	Reserved
		HW Rst.	15'h2EE	
		SW Rst.	Retain	

5.2.11 SERDES Test and System Mode Control

Offset: 0x05 (Hex) or 05 (Decimal)

Bit	Name	Type		Description
15	Reserved	Mode	R/W	Always 0.
		HW Rst.	See Desc.	
		SW Rst.	Retain	
14:9	Reserved	Mode	RO	Reserved
		HW Rst.	0	
		SW Rst.	0	
8	Serdes_beacon	Mode	R/W	Rgmii tx clock delay control bit: 1 = rgmii tx clock delay enable 0 = rgmii tx clock delay disable. (TX send beacon when high)
		HW Rst.	0	
		SW Rst.	0	
7:0	Reserved	Mode	R/W	Reserved
		HW Rst.	0	
		SW Rst.	0	

5.2.12 Hib ctrl and Auto-Negotiation Test Register

Offset: 0x0B (Hex) or 11 (Decimal)

Bit	Name	Type		Description
15	Ps_hib_en	Mode	R/W	Power hibernate control bit; 1: hibernate enable 0: hibernate disable
		HW Rst.	1	
		SW Rst.	Retain	
14:13	Reserved	Mode	RO	Reserved
		HW Rst.	2'h01	
		SW Rst.	Retain	
12	Hib_pulse_sw	Mode	R/W	1: when hibernate, PHY sends NLP pulse and detects signal from cables. 0: when hibernate, PHY doesn't send NLP pulse ,just detects signal from cables.
		HW Rst.	1	
		SW Rst.	Retain	
11:7	Reserved	Mode	R/W	Reserved
		HW Rst.	5'h18	
		SW Rst.	Retain	
6:5	Gtx_dly_val	Mode	RO	Select the delay of gtx_clk.
		HW Rst.	2'b10	
		SW Rst.	Retain	
4:0	Reserved	Mode	R/W	Reserved
		HW Rst.	5'h0	
		SW Rst.	Retain	

5.2.13 100BASE-TX Test Mode Select

Offset: 0x10

Bit	Name	Type		Description
15:8	Reserved	Mode	RO	Reserved
		HW Rst.	0	
		SW Rst.	Retain	
7	Jitter_test	Mode	R/W	100BT jitter test
		HW Rst.	0	
		SW Rst.	Retain	
6	Os_test	Mode	R/W	100BT over shoot test
		HW Rst.	0	
		SW Rst.	Retain	
5	Dcd_test	Mode	R/W	100BT DCD test
		HW Rst.	0	
		SW Rst.	Retain	
4:0	Reserved	Mode	RO	Reserved
		HW Rst.	0	
		SW Rst.	0	

5.2.14 hib timer selection

Offset: 0x11 (Hex) or 17 (Decimal)

Bit	Name	Type		Description
15:1	Reserved	Mode	R/W	Reserved
		HW Rst.	15'h 3AA9	
		SW Rst.	Retain	
0	Ext_lpbk	Mode	RO	1: enable the PHY's external loopback, namely channel 0<-> channel 1, channel 2 <-> channel 3.
		HW Rst.	2'h01	
		SW Rst.	Retain	

5.2.15 Test Configuration for 10BT

Offset: 0x12 (Hex) or 18 (Decimal)

Bit	Name	Type		Description
15:6	Reserved	Mode	RO	Reserved
		HW Rst.	010011 0000	
		SW Rst.	Retain	
5	Test_mode[2]	Mode	RO	The bit2 of test_mode
		HW Rst.	2'h01	
		SW Rst.	Retain	
4	Reserved	Mode	RO	Reserved
		HW Rst.	2'h01	
		SW Rst.	Retain	
3	Rgmii_mode	Mode	RO	Upon hardware reset, this bit depends on chip_sel and mode_cfg; 1: select RGMII interface with MAC; 0: select GMII/MII interface with MAC.
		HW Rst.	2'h01	
		SW Rst.	Retain	
2	Reserved	Mode	R/W	Reserved
		HW Rst.	1	
		SW Rst.	1	
1:0	Test_mode[1:0]	Mode	R/W	[001]: packet with all ones, 10MHz sine wave, For harmonic test. [010]: pseudo random, for TP_IDLE/Jitter/Differential Voltage test. [011]: normal link pulse only, [100]: 5MHz sin wave. Others: normal mode.
		HW Rst.	0	
		SW Rst.	0	

5.2.16 Power-Saving Control

Offset: 0x29 (Hex) or 41 (Decimal)

Bit	Name	Type		Description
15:2	Top_ps_en	Mode	R/W	1: top level power saving enable 0: top level power saving disable
		HW Rst.	1	
		SW Rst.	Retain	
1	Reserved	Mode	RO	
		HW Rst.	13'h DB7	
		SW Rst.	Retain	
0	ecnc_ps_en	Mode	R/W	
		HW Rst.	2'bo1	
		SW Rst.	Retain	

5.2.17 PHY_Control Debug Register0

Offset: 0x1F (Hex) or 31 (Decimal)

Bit	Name	Type		Description
15:2	Reserved	Mode	RO	Reserved
		HW Rst.	010011 0000	
		SW Rst.	Retain	
1	en_1588_p2	Mode	R/W	1=enable 1588 0=disable 1588
		HW Rst.		
		SW Rst.	Retain	
0	Reserved	Mode	RO	Reserved
		HW Rst.	0	
		SW Rst.	Retain	

5.2.18 PHY_Control Debug Register0

Offset: 0x1F (Hex) or 31 (Decimal)

Bit	Name	Type		Description
15:2	Reserved	Mode	RO	Reserved
		HW Rst.	010011 0000	
		SW Rst.	Retain	
1	en_1588_p2	Mode	R/W	1=enable 1588 0=disable 1588
		HW Rst.		
		SW Rst.	Retain	
0	Reserved	Mode	RO	Reserved
		HW Rst.	0	
		SW Rst.	Retain	

5.2.19 PHY_Control Debug Register0

Offset: 0x1F (Hex) or 31 (Decimal)

Bit	Name	Type		Description
15:2	Reserved	Mode	RO	Reserved
		HW Rst.	010011 0000	
		SW Rst.	Retain	
1	en_1588_p2	Mode	R/W	1=enable 1588 0=disable 1588
		HW Rst.		
		SW Rst.	Retain	
0	Reserved	Mode	RO	Reserved
		HW Rst.	0	
		SW Rst.	Retain	

5.2.20 Hib ctrl and Auto-Negotiation Test Register

Offset: 0x0B (Hex) or 11 (Decimal)

Bit	Name	Type		Description
15	Ps_hib_en	Mode	R/W	Power hibernate control bit; 1: hibernate enable 0: hibernate disable
		HW Rst.	1	
		SW Rst.	Retain	
14:13	Reseved	Mode	RO	
		HW Rst.	2'h01	
		SW Rst.	Retain	
12	Hib_pulse_sw	Mode	R/W	1: when hibernate, PHY sends NLP pulse and detects signal from cables. 0: when hibernate, PHY doesn't send NLP pulse ,just detects signal from cables.
		HW Rst.	1	
		SW Rst.	Retain	
11:7	Reseved	Mode	RO	
		HW Rst.		
		SW Rst.		
6:5	Gtx_dly_val	Mode	RO	Select the delay of gtx_clk.
		HW Rst.	2'b10	
		SW Rst.	Retain	
4:0	Reseved	Mode	RO	
		HW Rst.		
		SW Rst.		

5.2.21 Hib ctrl and rgmii gtx clock delay register

Offset: 0x0B (Hex), or 11 (Decimal)

Bit	Name	Type		Description
15	Ps_hib_en	Mode	R/W	Power hibernate control bit; 1: hibernate enable 0: hibernate disable
		HW Rst.	1	
		SW Rst.	Retain	
14:13	Reseved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
12	Hib_pulse_sw	Mode	R/W	1: when hibernate, PHY sends NLP pulse and detects signal from cables. 0: when hibernate, PHY doesn't send NLP pulse ,just detects signal from cables.
		HW Rst.	1	
		SW Rst.	Retain	
11:7	Reseved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
6:5	Gtx_dly_val	Mode	R/W	Select the delay of gtx_clk.
		HW Rst.	2’b10	
		SW Rst.	Retain	
4:0	Reseved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

5.2.22 1000BT external loopback configure

Offset: 0x11

Bit	Name	Type		Description
15:1	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
0	Ext_lpbk	Mode	RO	1: enable the PHY's external loopback, namely channel 0<-> channel 1, channel 2 <-> channel 3.
		HW Rst.	0	
		SW Rst.	0	

5.2.23 rgmii rx clock delay control

Offset: 0x00 (Hex), or 0 (Decimal)

Bit	Name	Type		Description
15	Sel_clk125m_dsp	Mode	R/W	Control bit for rgmii interface rx clock delay: 1 = rgmii rx clock delay enable 0 = rgmii rx clock delay disable
		HW Rst.	1	
	Reseved	SW Rst.	0	
14:0	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

5.2.24 Rgmii_mode; Test configuration for 10BT

Offset: 0x12

Bit	Name	Type		Description
15:6	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
5	Test_mode[2]	Mode	RO	The bit2 of test_mode
		HW Rst.	0	
		SW Rst.	0	
4	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
3	Rgmii_mode	Mode	RO	Upon hardware reset, this bit depends on chip_sel and mode_cfg; 1: select RGMII interface with MAC; 0: select GMII/MII interface with MAC.
		HW Rst.	0	
		SW Rst.	0	
2	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
1:0	Test_mode[1:0]	Mode	RO	[001]: packet with all ones, 10MHz sine wave, For harmonic test. [010]: pseudo random, for TP_IDLE/Jitter/Differential Voltage test. [011]: normal link pulse only, [100]: 5MHz sin wave. Others: normal mode.
		HW Rst.	0	
		SW Rst.	0	

5.2.25 gpio 1588 control register

Offset: 0x1F

Bit	Name	Type		Description
15:9	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
8	Sel_1p1_lp2 _pos_reg	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
7	Sel_gpio_int_ _pos_reg	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
6:4	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
3	sel_1p5_lp8 _pos_reg	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
2	phy_pll_on _pos_reg	Mode	RO	POS. 1= phy analog end PLL always on; 0=phy analog end PLL is controlled by digital Inner state
		HW Rst.	0	
		SW Rst.	0	
1	en_1588_p2	Mode	RO	1=enable 1588 0=disable 1588
		HW Rst.	0	
		SW Rst.	0	
0	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

5.2.26 gpio 1588 control register

Offset: 0x1F

Bit	Name	Type		Description
15	Pre_code	Mode	R/W	
		HW Rst.	0	
		SW Rst.	Retain	
14	Sel_crs_dv	Mode	RO	
		HW Rst.	1	
		SW Rst.	Retain	
13	Sg_mode	Mode	R/W	
		HW Rst.	0	
		SW Rst.	Retain	
12:0	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

5.2.27 MMD3 (MDIO Manageable Device Address 3 for PCS)

Bit	Name	Description	
0	PCS Control Register		
1	PCS Status Register		
5	PCS package Register		
20	EEE capability		
22	EEE wake error counter		
32786	P1588 control		
32787	P1588 rx_seqid		
32788	P1588 rx_sourcePort_identity		

Bit	Name	Description	
32789	P1588 rx_sourcePort_identity		
32790	P1588 rx_sourcePort_identity		
32791	P1588 rx_sourcePort_identity		
32792	P1588 rx_sourcePort_identity		
32793	P1588 rx_time_stamp		
32794	P1588 rx_time_stamp		
32795	P1588 rx_time_stamp		
32796	P1588 rx_time_stamp		
32797	P1588 rx_time_stamp		
32798	P1588 rx_frac_nano		
32799	P1588 rx_frac_nano		
32800	P1588 tx_seqid		
32801	P1588 tx_sourcePort_identity		
32802	P1588 tx_sourcePort_identity		
32803	P1588 tx_sourcePort_identity		
32804	P1588 tx_sourcePort_identity		
32805	P1588 tx_sourcePort_identity		
32806	P1588 tx_time_stamp		

Bit	Name	Description	
32807	P1588 tx_time_stamp		
32808	P1588 tx_time_stamp		
32809	P1588 tx_time_stamp		
32810	P1588 tx_time_stamp		
32811	P1588 tx_frac_nano		
32812	P1588 tx_frac_nano		
32813	P1588 origin_correction		
32814	P1588 origin_correction		
32815	P1588 origin_correction		
32816	P1588 origin_correction		
32817	P1588 ingress_trig_time		
32818	P1588 ingress_trig_time		
32819	P1588 ingress_trig_time		
32820	P1588 ingress_trig_time		
32821	P1588 tx_latency		
32822	P1588 inc_vaule		
32823	P1588 inc_value		
32824	P1588 nano_offset		
32825	P1588 nano_offset		
32826	P1588 sec_offset		
32827	P1588 sec_offset		
32828	P1588 sec_offset		

Bit	Name	Description	
32829	P1588 real_time		
32830	P1588 real_time		
32831	P1588 real_time		
32832	P1588 real_time		
32833	P1588 real_time		
32834	P1588 rtc_frac_nano		
32835	P1588 rtc_frac_nano		
32842	P1588 loc_mac_addr		
32843	P1588 loc_mac_addr		
32844	P1588 loc_mac_addr		

5.2.28 MMD7 (MDIO Manageable Device Address 7 for Auto-Negotiation)

Bit	Name	Description	
0	AN control		
1	AN status		
5	AN package Register		
22	AN XNP transmit		
23	AN XNP transmit1		
24	AN XNP transmit2		
25	AN XNP ability		
26	AN XNP ability1		

Bit	Name	Description	
27	AN XNP ability2		
60	EEE advertisement		
61	EEE LP advertisement		
32768	EEE ability auto-negotiation result		

6. MDIO Interface Register

6.1 MMD3 - PCS Register

6.1.1 PCS Control 1

Device Address = 3

Offset: 0x0 (Hex)

Bit	Name			Description
15	Pcs_rst	Mode	R/W	Reset bit, self clear. When write this bit 1 : 1, reset the registers(not vender specific) in MMD3/MMD7. 2, cause software reset in mii register0 bit15.
		HW Rst.	0	
		SW Rst.	0	
14:11	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
10	Clock_stoppable	Mode	R/W	Not implement.
		HW Rst.	0	
		SW Rst.	Retain	
9.0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

6.1.2 PCS Status 1

Device Address = 3

Offset: 0x1 (Hex)

Bit	Name			Description
15:12	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
11	Tx lp idle received	Mode	R/W	When read as 1, it indicates that the transmit PCS has received low power idle signaling one or more times since the register was last read. Latch High.
		HW Rst.	0	
		SW Rst.	0	
10	Rx lp idle received	Mode	R/W	When read as 1, it indicates that the recive PCS has received low power idle signaling one or more times since the register was last read. Lach High.
		HW Rst.	0	
		SW Rst.	0	
9	Tx lp idle indication	Mode	R/W	When read as 1, it indicates that the transmit PCS is currently receiving low power idle signals.
		HW Rst.	0	
		SW Rst.	0	
8	Rx lp idle indication	Mode	R/W	When read as 1, it indicates that the receive PCS is currently receiving low power idle signals.
		HW Rst.	0	
		SW Rst.	0	
7:0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

6.1.3 PCS Package

Device Address = 3

Offset: 0x5 (Hex)

Bit	Name			Description
15:8	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
7	auto_neg_ present	Mode	RO	Always 1.
		HW Rst.	0	
		SW Rst.	0	
6:4	Reserved	Mode	RO	Always 0
		HW Rst.	0	
		SW Rst.	0	
3	PCS present	Mode	RO	Always 1.
		HW Rst.	0	
		SW Rst.	0	
2:1	Reserved	Mode	R/W	Always 0.
		HW Rst.	0	
		SW Rst.	0	
0	mii_reg_present	Mode	RO	Always 1
		HW Rst.	0	
		SW Rst.	0	

6.1.4 EEE Capability

Device Address = 3

Offset: 0x14 (Hex)

Bit	Name			Description
15:3	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
2	1000BT EEE	Mode	RO	EEE is supported for 1000Base-T.
		HW Rst.	0	
		SW Rst.	0	
1	100BT EEE	Mode	RO	EEE is supported for 100Base-T.
		HW Rst.	0	
		SW Rst.	0	
0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

6.1.5 EEE Wake Error Counter

Device Address = 3

Offset: 0x16 (Hex)

Bit	Name			Description
15:	EEE wake error counter	Mode	RO	Count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. This counter is clear after read, and hold at all ones in the case of overflow.
		HW Rst.	0	
		SW Rst.	0	

6.1.6 P1588 Control Register

Device Address = 3

Offset: 0x8012 (Hex)

Bit	Name			Description
15:5	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
4	Eth_mode_en	Mode	R/W	Ethernet mode 0=Gigabit Ethernet mode. 1=10/100M Ethernet mode.
		HW Rst.	1'b0	
		SW Rst.	Retain	
3	Bypass	Mode	R/W	0=IEEE1588v2 normal operation. 1=Bypass IEEE1588v2 functions.
		HW Rst.	1'b1	
		SW Rst.	Retain	
2:1	Clock_mode	Mode	R/W	00=ordinary/boundary two-step clock. 01=ordinary/boundary one-step clock. 10= transparent two-step clock. 11=transparent one-step clock.
		HW Rst.	2'b00	
		SW Rst.	Retian	
0	Eth_mode_sw	Mode	R/W	
		HW Rst.	1'b0	
		SW Rst.	Retain	

6.1.7 P1588 RX_seqid

Device Address = 3

Offset: 0x8013 (Hex)

Bit	Name			Description
15:0	Rx_seqid	Mode	RO	sequenceId of the mose recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.8 P1588 rx_sourcePort_identity

Device Address = 3

Offset: 0x8014 (Hex)

Bit	Name			Description
15:0	Rx_sourcePort Identity[79:64]	Mode	RO	The most significant 16 bits ([79:64]) of sourcePortIdentity of the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.9 P1588 rx_sourcePort_identity

Device Address = 3

Offset: 0x8015 (Hex)

Bit	Name			Description
15:0	Rx_sourcePort Identity[63:48]	Mode	RO	Bits [63:48] of sourcePortIdentity of the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.10 P1588 rx_sourcePort_identity

Device Address = 3

Offset: 0x8016 (Hex)

Bit	Name			Description
15:0	Rx_sourcePort Identity[47:32]	Mode	RO	Bits [47:32] of sourcePortIdentity of the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.11 P1588 rx_sourcePort_identity

Device Address = 3

Offset: 0x8017 (Hex)

Bit	Name			Description
15:0	Rx_sourcePort Identity[31:16]	Mode	RO	Bits [31:16] of sourcePortIdentity of the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.12 P1588 rx_sourcePort_identity

Device Address = 3

Offset: 0x8018 (Hex)

Bit	Name			Description
15:0	Rx_sourcePort Identity[15:0]	Mode	RO	Bits [15:0] of sourcePortIdentity of the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.13 P1588 rx_time_stamp

Device Address = 3

Offset: 0x8019 (Hex)

Bit	Name			Description
15:0	Rx_time_ stamp[79:64]	Mode	RO	The most significant 16 [79:64] bits of RX timestamp for the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.14 P1588 rx_time_stamp

Device Address = 3

Offset: 0x801A (Hex)

Bit	Name			Description
15:0	Rx_time_ stamp[63:48]	Mode	RO	Bits [63:48] of RX timestamp for the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.15 P1588 rx_time_stamp

Device Address = 3

Offset: 0x801B (Hex)

Bit	Name			Description
15:0	Rx_time_ stamp[47:32]	Mode	RO	Bits [47:32] of RX timestamp for the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.16 P1588 rx_time_stamp

Device Address = 3

Offset: 0x801C (Hex)

Bit	Name			Description
15:0	Rx_time_ stamp[31:16]	Mode	RO	Bits [31:16] of RX timestamp for the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.17 P1588 rx_time_stamp

Device Address = 3

Offset: 0x801D (Hex)

Bit	Name			Description
15:0	Rx_time_ stamp[15:0]	Mode	RO	Bits [15:0] of RX timestamp for the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.18 P1588 Rx_frac_nano

Device Address = 3

Offset: 0x801E (Hex)

Bit	Name			Description
15:12	Rx_messageType	Mode	RO	messageType of the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	
11:0	Rx_frac_nano[19:8]	Mode	RO	Bits [19:8] of fractional nanoseconds field of RX timestamp for the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.19 P1588 Rx_frac_nano

Device Address = 3

Offset: 0x801F (Hex)

Bit	Name			Description
15:8	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
7:0	Rx_frac_nano[7:0]	Mode	RO	Bits [7:0] of fractional nanoseconds field of RX timestamp for the most recently received IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.20 P1588 Tx_seqid

Device Address = 3

Offset: 0x8020 (Hex)

Bit	Name			Description
15:0	Tx_seqid	Mode	RO	sequenceId of the mose recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.21 P1588 tx_sourcePort_Identity

Device Address = 3

Offset: 0x8021 (Hex)

Bit	Name			Description
15:0	tx_sourcePort Identity[79:64]	Mode	RO	The most significant 16 bits ([79:64]) of sourcePortIdentity of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.22 P1588 tx_sourcePort_Identity

Device Address = 3

Offset: 0x8021 (Hex)

Bit	Name			Description
15:0	tx_sourcePort Identity[79:64]	Mode	RO	The most significant 16 bits ([79:64]) of sourcePortIdentity of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.23 P1588 tx_sourcePort_Identity

Device Address = 3

Offset: 0x8022 (Hex)

Bit	Name			Description
15:0	tx_sourcePort Identity[63:48]	Mode	RO	Bits [63:48] of sourcePortIdentity of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.24 P1588 tx_sourcePort_Identity

Device Address = 3

Offset: 0x8023 (Hex)

Bit	Name			Description
15:0	tx_sourcePort Identity[47:32]	Mode	RO	Bits [47:32] of sourcePortIdentity of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.25 P1588 tx_sourcePort_Identity

Device Address = 3

Offset: 0x8024 (Hex)

Bit	Name			Description
15:0	tx_sourcePort Identity[31:16]	Mode	RO	Bits [31:16] of sourcePortIdentity of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.26 P1588 tx_sourcePort_Identity

Device Address = 3

Offset: 0x8025 (Hex)

Bit	Name			Description
15:0	tx_sourcePort Identity[15:0]	Mode	RO	Bits [15:0] of sourcePortIdentity of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.27 P1588 tx_timestamp

Device Address = 3

Offset: 0x8026 (Hex)

Bit	Name			Description
15:0	tx_time_ stamp[79:64]	Mode	RO	The most significant 16 [79:64] bits of TX timestamp for the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.28 P1588 tx_timestamp

Device Address = 3

Offset: 0x8027 (Hex)

Bit	Name			Description
15:0	tx_time_ stamp[63:48]	Mode	RO	Bits [63:48] of TX timestamp for the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.29 P1588 tx_time_stamp

Device Address = 3

Offset: 0x 8028(Hex)

Bit	Name			Description
15:0	tx_time_ stamp[47:32]	Mode	RO	Bits [47:32] of TX timestamp for the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.30 P1588 tx_time_stamp

Device Address = 3

Offset: 0x8029 (Hex)

Bit	Name			Description
15:0	tx_time_ stamp[31:16]	Mode	RO	Bits [31:16] of TX timestamp for the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.31 P1588 tx_time_stamp

Device Address = 3

Offset: 0x802A(Hex)

Bit	Name			Description
15:0	tx_time_ stamp[15:0]	Mode	RO	Bits [15:0] of TX timestamp for the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	

6.1.32 P1588 Tx_frac_nano

Device Address = 3

Offset: 0x802B (Hex)

Bit	Name			Description
15:12	tx_messageType	Mode	RO	messageType of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	
11:0	tx_frac_nano[19:8]	Mode	RO	Bits [19:8] of fractional nanoseconds field of TX timestamp for the most recently transmitted IEEE1588v2 event message
		HW Rst.	0	
		SW Rst.	0	

6.1.33 P1588 tx_frac_nano

Device Address = 3

Offset: 0x802B (Hex)

Bit	Name			Description
15:12	tx_messageType	Mode	RO	messageType of the most recently transmitted IEEE1588v2 event message.
		HW Rst.	0	
		SW Rst.	0	
11:0	tx_frac_nano[19:8]	Mode	RO	Bits [19:8] of fractional nanoseconds field of TX timestamp for the most recently transmitted IEEE1588v2 event message
		HW Rst.	0	
		SW Rst.	0	

6.1.34 P1588 Orgin_Correction_o

Device Address = 3

Offset: 0x802D(Hex)

Bit	Name			Description
15:0	Origin_ Correction_o[63:48]	Mode	RO	Bits [63:48] of original correctionField of the IEEE1588v2 event message to be transmitted. This is used in one-step clock mode, provide information for hardware operation.
		HW Rst.	0	
		SW Rst.	0	

6.1.35 P1588 Orgin_Correction_o

Device Address = 3

Offset: 0x802E (Hex)

Bit	Name			Description
15:0	Origin_ Correction_o[47:32]	Mode	RO	Bits [47:32] of original correctionField of the IEEE1588v2 event message to be transmitted. This is used in one-step clock mode, provide information for hardware operation.
		HW Rst.	0	
		SW Rst.	0	

6.1.36 P1588 Orgin_Correction_o

Device Address = 3

Offset: 0x802F (Hex)

Bit	Name			Description
15:0	Origin_ Correction_o[31:16]	Mode	RO	Bits [31:16] of original correctionField of the IEEE1588v2 event message to be transmitted. This is used in one-step clock mode, provide information for hardware operation.
		HW Rst.	0	
		SW Rst.	0	

6.1.37 P1588 Orgin_Correction_o

Device Address = 3

Offset: 0x8030 (Hex)

Bit	Name			Description
15:0	Origin_ Correction_o[15:0]	Mode	RO	Bits [15:0] of original correctionField of the IEEE1588v2 event message to be transmitted. This is used in one-step clock mode, provide information for hardware operation.
		HW Rst.	0	
		SW Rst.	0	

6.1.38 P1588 Ingress_trig_time_o

Device Address = 3

Offset: 0x8031 (Hex)

Bit	Name			Description
15:0	Ingress_trig_ Time_o[51:36]	Mode	RO	Bits [31:16] of nanoseconds field of RX timestamp of associate received event message for the IEEE1588v2 event message to be transmitted. This is used in one-step clock mode, provide information for hardware calculation.
		HW Rst.	0	
		SW Rst.	0	

6.1.39 P1588 Ingress_trig_time_o

Device Address = 3

Offset: 0x8032 (Hex)

Bit	Name			Description
15:0	Ingress_trig_ Time_o[51:36]	Mode	RO	Bits [31:16] of nanoseconds field of RX timestamp of associate received event message for the IEEE1588v2 event message to be transmitted. This is used in one-step clock mode, provide information for hardware calculation.
		HW Rst.	0	
		SW Rst.	0	

6.1.40 P1588 Ingress_trig_time_o

Device Address = 3

Offset: 0x8033 (Hex)

Bit	Name			Description
15:0	Ingress_trig_ Time_o[19:4]	Mode	RO	Bits [19:4] of fractional nanoseconds field of RX timestamp of associate received event message for the IEEE1588v2 event message to be transmitted. This is used in one-step clock mode, provide information for hardware calculation.
		HW Rst.	0	
		SW Rst.	0	

6.1.41 P1588 Ingress_trig_time_o

Device Address = 3

Offset: 0x8034 (Hex)

Bit	Name			Description
15:12	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
11:0	Ingress_trig _time_o[3:0]	Mode	RO	Bits [3:0] of fractional nanoseconds field of RX timestamp of associate received event message for the IEEE1588v2 event message to be transmitted.
		HW Rst.	0	
		SW Rst.	Retain	This is used in one-step clock mode, provide information for hardware calculation.

6.1.42 P1588 Tx_latency_o

Device Address = 3

Offset: 0x8035(Hex)

Bit	Name			Description
15:0	Tx_latency_o	Mode	RO	Transmission latency from Tx timestamp reference plan to the physical media, unit in nanoseconds. This is used in one-step clock mode, provide information for hardware calculation.
		HW Rst.	0	
		SW Rst.	Retain	

6.1.43 P1588 Inc_value_o

Device Address = 3

Offset: 0x8036 (Hex)

Bit	Name			Description
15:0	Inc_value_o[25:10]	Mode	RO	Bit [25:10] of increment value for the IEEE1588v2 RTC counter. Software can adjust this value, thus adjust tick rate. Bits [25:20] is nanosecond part, [19:0] is fractional nanoseconds.
		HW Rst.	0	
		SW Rst.	Retain	

6.1.44 P1588 Inc_value_o

Device Address = 3

Offset: 0x8037 (Hex)

Bit	Name			Description
15:10	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
9:0	Inc_vaule_o[9:0]	Mode	RO	Bit [9:0] of increment value for the IEEE1588v2 RTC counter. Software can adjust this value, thus adjust tick rate. Bits [25:20] is nanosecond part, [19:0] is fractional nanoseconds.
		HW Rst.	0	
		SW Rst.	0	

6.1.45 P1588 Nano_offset_o

Device Address = 3

Offset: 0x8038 (Hex)

Bit	Name			Description
15:0	Nano_offset_o[31:16]	Mode	RO	Bits [31:16] of nanoseconds field of time difference between master and slave.
		HW Rst.	0	
		SW Rst.	Retain	

6.1.46 P1588 Nano_offset_o

Device Address = 3

Offset: 0x8039 (Hex)

Bit	Name			Description
15:0	Nano_offset_o[15:0]	Mode	RO	Bits [15:0] of nanoseconds field of time difference between master and slave.
		HW Rst.	0	
		SW Rst.	Retain	

6.1.47 P1588 Sec_offset_o

Device Address = 3

Offset: 0x803A (Hex)

Bit	Name			Description
15:0	Sec_offset_o[47:32]	Mode	RO	Bits [47:32] of seconds field of time difference between master and slave.
		HW Rst.	0	
		SW Rst.	Retain	

6.1.48 P1588 Sec_offset_o

Device Address = 3

Offset: 0x803B (Hex)

Bit	Name			Description
15:0	Sec_offset_o[31:16]	Mode	RO	Bits [31:16] of seconds field of time difference between master and slave.
		HW Rst.	0	
		SW Rst.	Retain	

6.1.49 P1588 Sec_offset_o

Device Address = 3

Offset: 0x803C (Hex)

Bit	Name			Description
15:0	Sec_offset_o[15:0]	Mode	RO	Bits [15:0] of seconds field of time difference between master and slave.
		HW Rst.	0	
		SW Rst.	Retain	

6.1.50 P1588 Real_time_i

Device Address = 3

Offset: 0x803D (Hex)

Bit	Name			Description
15:0	Real_time_i[79:64]	Mode	RO	Bits [79:64] of current RTC counter implemented for IEEE1588v2. Bits [79: 32] corresponding to seconds field, bits [31:0] corresponding to nanoseconds field.
		HW Rst.	0	
		SW Rst.	Retain	

6.1.51 P1588 Real_time_i

Device Address = 3

Offset: 0x803E (Hex)

Bit	Name			Description
15:0	Real_time_i[63:48]	Mode	RO	Bits [63:48] of current RTC counter implemented for IEEE1588v2. Bits [79: 32] corresponding to seconds field, bits [31:0] corresponding to nanoseconds field.
		HW Rst.	0	
		SW Rst.	Retain	

6.1.52 P1588 Real_time_i

Device Address = 3

Offset: 0x803F (Hex)

Bit	Name			Description
15:0	Real_time_i[47:32]	Mode	RO	Bits [47:32] of current RTC counter implemented for IEEE1588v2. Bits [79: 32] corresponding to seconds field. Bits [31:0] corresponding to nanoseconds field.
		HW Rst.	0	
		SW Rst.	0	

6.1.53 P1588 Real_time_i

Device Address = 3

Offset: 0x8040 (Hex)

Bit	Name			Description
15:0	Real_time_i[31:16]	Mode	RO	Bits [31:16] of current RTC counter implemented for IEEE1588v2. Bits [79: 32] corresponding to seconds field. Bits [31:0] corresponding to nanoseconds field.
		HW Rst.	0	
		SW Rst.	0	

6.1.54 P1588 Real_time_i

Device Address = 3

Offset: 0x8041 (Hex)

Bit	Name			Description
15:0	Real_time_i[15:0]	Mode	RO	Bits [15:0] of current RTC counter implemented for IEEE1588v2. Bits [79: 32] corresponding to seconds field. Bits [31:0] corresponding to nanoseconds field.
		HW Rst.	0	
		SW Rst.	0	

6.1.55 P1588 Rtc_frac_nano_i

Device Address = 3

Offset: 0x8042 (Hex)

Bit	Name			Description
15:0	Rtc_frac_nano_i[19:4]	Mode	RO	Bits [19:4] of fractional nanoseconds field of current RTC counter implemented for IEEE1588v2.
		HW Rst.	0	
		SW Rst.	0	

6.1.56 P1588 Rtc_frac_nano_i

Device Address = 3

Offset: 0x8043 (Hex)

Bit	Name			Description
15:12	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
11:0	Rtc_frac_nano_i[3:0]	Mode	RO	Bits [3:0] of fractional nanoseconds field of current RTC counter implemented for IEEE1588v2
		HW Rst.	0	
		SW Rst.	0	

6.1.57 P1588 Offset_valid_r

Device Address = 3

Offset: 0x8044 (Hex)

Bit	Name			Description
15:12	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
11:0	Offset_valid_r	Mode	WO	Write only. Write to this register to adjust local IEEE1588v2 RTC counter abruptly.
		HW Rst.	0	
		SW Rst.	Retain	

6.1.58 Wake-on-Lan loc_mac_addr_o

Device Address = 3

Offset: 0x804A (Hex)

Bit	Name			Description
15:0	Loc_mac_ Addr_o[47:32]	Mode	R/W	Bits [47:32] of local MAC address, used in Wake-on-Lan.
		HW Rst.	0	
		SW Rst.	Retain	

6.1.59 Wake-on-Lan loc_mac_addr_o

Device Address = 3

Offset: 0x804B (Hex)

Bit	Name			Description
15:0	Loc_mac_ Addr_o[31:16]	Mode	R/W	Bits [31:16] of local MAC address, used in Wake-on-Lan.
		HW Rst.	0	
		SW Rst.	Retain	

6.1.60 Wake-on-Lan loc_mac_addr_o

Device Address = 3

Offset: 0x804C (Hex)

Bit	Name			Description
15:0	Loc_mac_ Addr_o[15:0]	Mode	R/W	Bits [15:0] of local MAC address, used in Wake-on-Lan.
		HW Rst.	0	
		SW Rst.	Retain	

6.2 MMD7 - auto-negotiation register

6.2.1 AN control1

Device Address = 7

Offset: 0x0 (Hex)

Bit	Name			Description
15	an_rst	Mode	R/W	Reset bit, self clear. When write this bit 1 : 1, reset the registers(not vender specific) in MMD3/MMD7. 2, cause software reset in mii register0 bit15.
		HW Rst.	0	
		SW Rst.	0	
14	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
13	Xnp_ctrl	Mode	R/W	If mii register4 bit12 is set to 0, setting of this bit shall have no effect. 1 = Local device intends to enable the exchange of extended next page; 0 = Local device does not intend to enable the exchange of extended next page;
		HW Rst.	1'b1	
		SW Rst.	Retain	
12:0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

6.2.1 AN package

Device Address = 7

Offset: 0x5 (Hex)

Bit	Name			Description
15:8	Reserved	Mode	R/W	Always 0.
		HW Rst.	0	
		SW Rst.	0	

Bit	Name			Description
7	auto_neg_ present	Mode	RO	Always 1.
		HW Rst.	0	
		SW Rst.	0	
6:4	Reserved	Mode	RO	Always 0
		HW Rst.	0	
		SW Rst.	0	
3	PCS present	Mode	RO	Always 1.
		HW Rst.	1	
		SW Rst.	1	

6.2.1 AN package

Device Address = 7

Offset: 0x5 (Hex)

Bit	Name			Description
15:8	Reserved	Mode	R/W	Always 0.
		HW Rst.	0	
		SW Rst.	0	
7	auto_neg_ present	Mode	RO	Always 1.
		HW Rst.	0	
		SW Rst.	0	
6:4	Reserved	Mode	RO	Always 0
		HW Rst.	0	
		SW Rst.	0	
3	PCS present	Mode	RO	Always 1.
		HW Rst.	1	
		SW Rst.	1	
2:1	Reserved	Mode	RO	Always 0
		HW Rst.	0	
		SW Rst.	0	

Bit	Name			Description
0	mii_reg_present	Mode	RO	Always 1.
		HW Rst.	1	
		SW Rst.	1	

6.2.1 AN status

Device Address = 7

Offset: 0x1 (Hex)

Bit	Name			Description
15:8	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	
7	Xnp_status	Mode	RO	1 = both Local device and link partner have indicated support for extended next page; 0 = extended next page shall not be used.
		HW Rst.	0	
		SW Rst.	0	
6:0	Reserved	Mode	RO	
		HW Rst.	0	
		SW Rst.	0	

6.2.1 AN XNP transmit

Device Address = 7

Offset: 0x16 (Hex)

Bit	Name			Description
15:0	Xnp_22	Mode	R/W	A write to this register set mr_next_page_loaded.
		HW Rst.	15'h0	
		SW Rst.	Retain	

6.2.1 AN XNP transmit1

Device Address = 7

Offset: 0x17 (Hex)

Bit	Name			Description
15:0	Xnp_23	Mode	R/W	
		HW Rst.	15'h0	
		SW Rst.	Retain	

6.2.1 AN XNP transmit2

Device Address = 7

Offset: 0x18 (Hex)

Bit	Name			Description
15:0	Xnp_24	Mode	R/W	
		HW Rst.	15'h0	
		SW Rst.	Retain	

6.2.1 AN LP XNP ability

Device Address = 7

Offset: 0x19 (Hex)

Bit	Name			Description
15:0	Lp_xnp_1	Mode	R/W	
		HW Rst.	15'h0	
		SW Rst.	15'h0	

6.2.1 AN LP XNP ability1

Device Address = 7

Offset: 0x1A (Hex)

Bit	Name			Description
15:0	Lp_xnp_2	Mode	R/W	Latched when lp_xnp_1 is read
		HW Rst.	15'h0	
		SW Rst.	15'h0	

6.2.1 AN LP XNP ability2

Device Address = 7

Offset: 0x1B (Hex)

Bit	Name			Description
15:0	Lp_xnp_3	Mode	R/W	Latched when lp_xnp_1 is read
		HW Rst.	15'h0	
		SW Rst.	15'h0	

6.2.2 EEE advertisement

Device Address = 7

Offset: 0x3C (Hex)

Bit	Name			Description
15:3	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
2	EEE_1000BT	Mode	RO	If Local device supports EEE operation for 1000BT, and EEE operation is desired, this bit shall be set to 1.
		HW Rst.	0	
		SW Rst.	0	
1	EEE_100BT	Mode	RO	If Local device supports EEE operation for 100BT, and EEE operation is desired, this bit shall be set to 1.
		HW Rst.	0	
		SW Rst.	0	
0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

6.2.3 EEE advertisement

Device Address = 7

Offset: 0x3C (Hex)

Bit	Name			Description
15:3	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
2	EEE_1000BT	Mode	R/W	If Local device supports EEE operation for 1000BT, and EEE operation is desired, this bit shall be set to 1.
		HW Rst.	1'b1	
		SW Rst.	Retain	
1	EEE_100BT	Mode	R/W	If Local device supports EEE operation for 100BT, and EEE operation is desired, this bit shall be set to 1.
		HW Rst.	1'b1	
		SW Rst.	Retain	
0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

6.2.4 EEE LP advertisement

Device Address = 7

Offset: 0x3D (Hex)

Bit	Name			Description
15:3	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	
2	EEE_1000BT	Mode	RO	1 = link partner supports EEE operation for 1000BT, and EEE operation is desired; 0 = link partner does not support EEE operation for 1000BT, or EEE operation is not desired.
		HW Rst.	0	
		SW Rst.	0	
1	EEE_100BT	Mode	RO	1 = link partner supports EEE operation for 100BT, and EEE operation is desired; 0 = link partner does not support EEE operation for 100BT, or EEE operation is not desired.
		HW Rst.	0	
		SW Rst.	0	
0	Reserved	Mode	RO	Always 0.
		HW Rst.	0	
		SW Rst.	0	

7. Package Dimensions

The AR8031 is packaged in a 48-pin 6 x 6 mm QFN package. The package drawings and dimensions are provided in Figure 7-1 and Table 7-1.

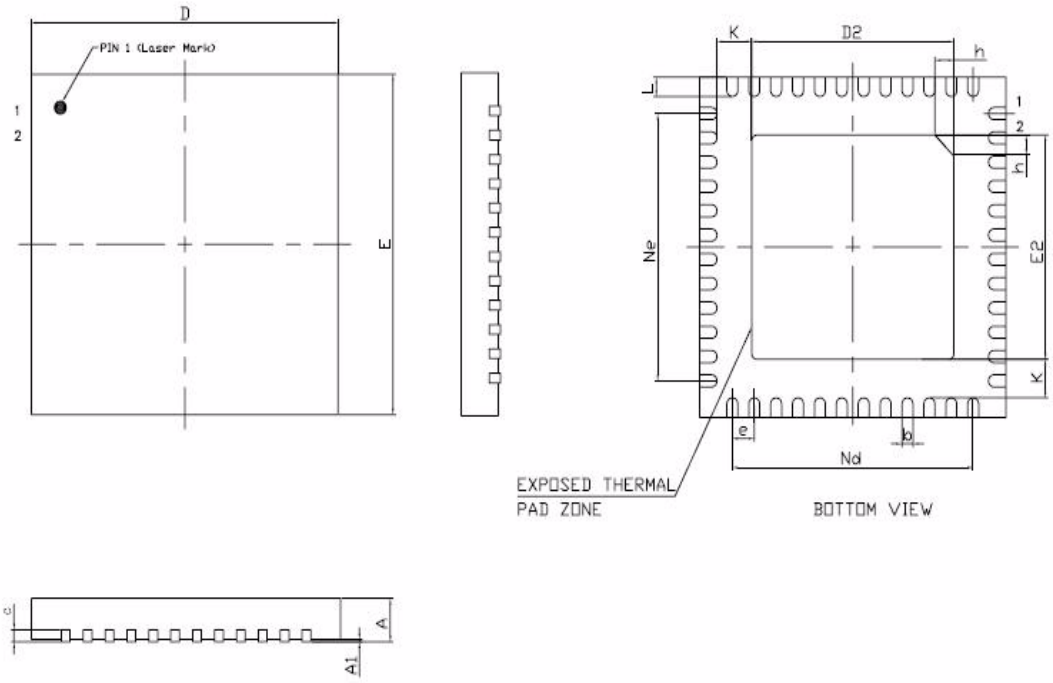


Figure 7-1. **Package Views**

Table 7-1. **Package Dimensions**

Dimension Label	Min	Nom	Max	Unit
A	0.70	0.75	0.80	mm
A1	—	0.01	0.05	mm
b	0.15	0.20	0.25	mm
c	0.18	0.20	0.23	mm
D	5.90	6.00	6.10	mm
D2	3.70	3.80	3.90	mm
e	0.35	0.40	0.45	mm
Ne	4.35	4.40	4.45	mm
Nd	4.35	4.40	4.45	mm
E	5.90	6.00	6.10	mm
E2	3.70	3.80	3.90	mm
K	0.20	—	—	mm
L	0.35	0.40	0.45	mm
h	0.30	0.35	0.40	mm

8. Ordering Information

The order number ***AR8031-AL1A*** specifies a current, **Commercial** version of the AR8031.

The order number ***AR8031-AL1B*** specifies a current, **Industrial** version of the AR8031.

9. Ordering Information

The top-side marking of the ***AR8031*** will be ***the order number,*** as shown in section 7 above.

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