Application Processor Card (APP)

Hardware Design Document (HDD)

Revision 1.0

Ownership Disclaimer

Revision History

Revision	Date	Description	Author
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Approvals

Product Manager Date

Table of Contents

1 Introduction 5
1.1 Purpose 5
1.2 Audience 5
1.3 Scope 5
2 General Description 6
2.1 Board Features 6
2.2 Implementation Block Diagram 7
3 Description of Functional Blocks 8
3.1 Processor 8
3.2 DDR-3 SODIMM 9
3.3 NAND Flash 11
3.4 MRAM 11
3.5 SPI Flash 12
3.6 Micro SD Card Interface 12
3.7 DUART 12
3.8 Enhanced Triple Speed Ethernet Controller (eTSEC) Interface 13
3.9 QUICC Engine RMII1 and RMII5 Interface 16
3.10 EtherCAT Slave Interface 18
3.11 QUICC Engine SER3 and SER7 Interface 18
3.12 USB 18
3.13 I2C 19
3.14 CPLD 20
3.15 Hot Swap Control 23
3.16 Power 23
3.17 Debug Support 25
3.18 Front Panel LEDs 27
3.19 Backplane Connectors 28
4 Schematic Design 32
4.1 Design Tool 32
5 Board Layout Design 32
5.1 Board Thickness 32
5.2 Board Stack-up 32

1 Introduction

1.1 Purpose

The objective of this document is to describe the hardware design of Application Processor Card (APP Card).

1.2 Audience

This document is targeted at Personnel involved in development and testing of board at Mindteck as well as CCC.

1.3 Scope

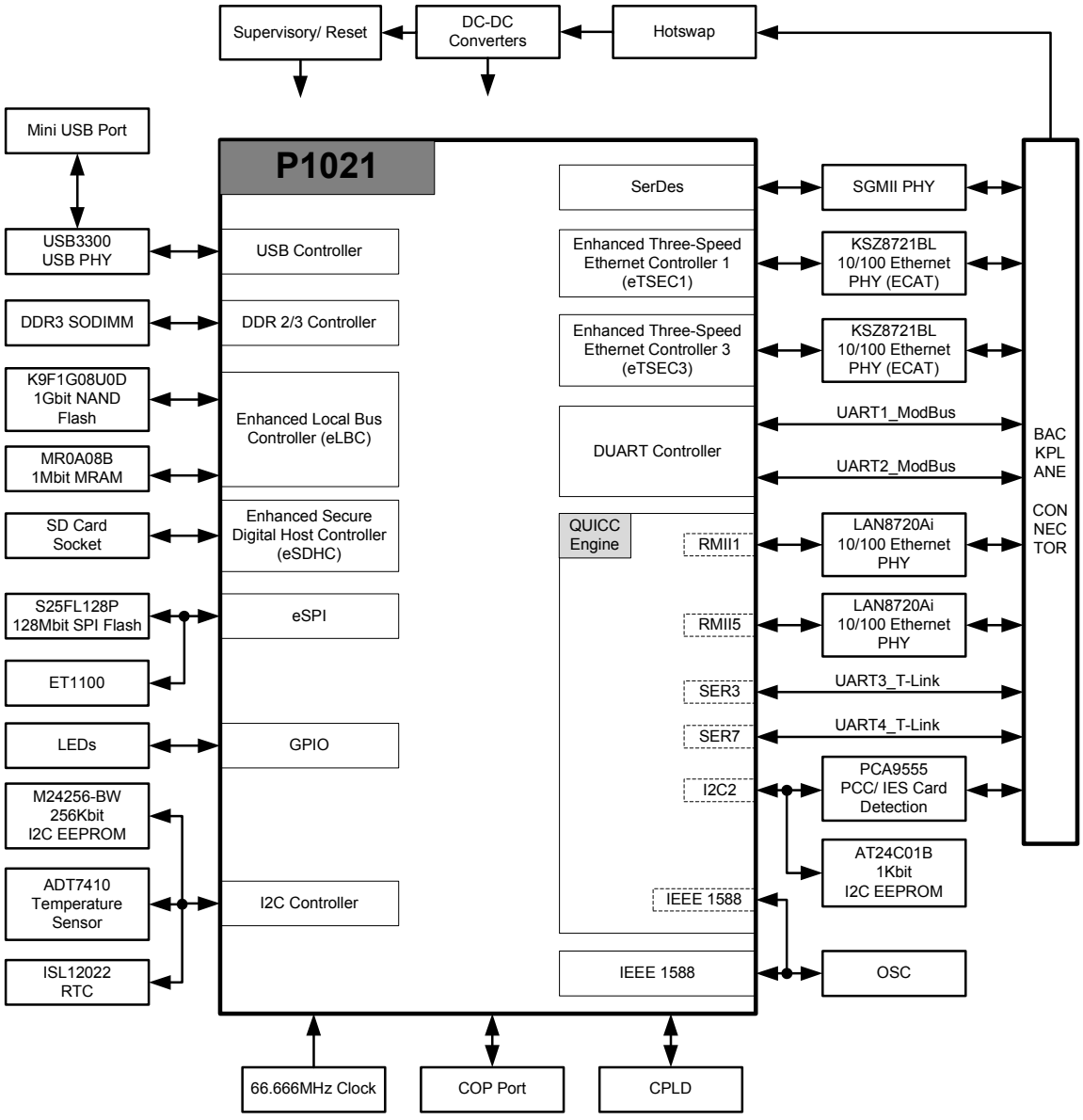
The scope of this document is to describe APP card hardware design in brief. The document details the various functional level block diagrams. Also this document details about the board power budget analysis, any kind of mathematical / simulation analysis.

2 General Description

2.1 Board Features

Sr. No.	Feature	Description
1	Processor	QorIQ P1021 from Freescale
2	DDR-3	204 pin SODIMM Module
3	NAND Flash	1GB Nand flash
4	MRAM	1MBit MRAM (x8)
5	SPI Flash	128 MBit
6	SD Card	Top mounting Micro SD card
7	UART ports	Four UART ports to backplane
8	10/100 Ethernet	Two 10/100 Ethernet ports to backplane
9	EtherCAT Master	Two EtherCAT Master ports to backplane
10	EtherCAT Slave	One EtherCAT slave interface using ET1100
11	SGMII	One SGMII Interface to backplane
12	USB OTG	One USB OTG with on-board mini connector
13	I2C	Two separate I2C interfaces connecting EEPROMs, RTC, Temperature sensor
15	CPLD	One CPLD to control power/reset sequencing
16	Hot-swap Control	Hot-swap compatible
17	Power	Multiple on-board power
18	Debug support	COP connector, debug RS-232 port, debug LEDs, manual reset, test points

2.2 Implementation Block Diagram



3 Description of Functional Blocks

3.1 Processor

P1021 QorIQ processor from Freescale is used as main processing unit. The P1021 integrates dual PowerPC™ e500v2 processor cores with the system logic required for networking, wireless infrastructure, and telecommunications applications. It is a member of the Ultra Low End Dual Core QorIQ™ family that combines system-level support for industry-standard interfaces with processors that implement the PowerPC architecture. The PowerPC cores in the P1021 with its 32 Kbytes of instruction and data cache, implement enhanced PowerPC core instruction set architecture and provide hardware and software debugging support. The key features include

- Dual e500v2 cores with a large L2 cache of 256 Kbytes
- One 32-bit DDR2/DDR3 memory controller with ECC support
- Three-speed (10/100/1000 Mbps) Ethernet controllers
- Flexible enhanced local bus controller
- PCI Express
- SGMII
- USB 2.0 host and device controller
- Enhanced SD/MMC controller
- eSPI controller
- Dual I2C controller
- DUART
- QUICC Engine
- Security engine controller

The P1021 incorporates a single RISC QUICC Engine™ block that provides termination, inter-working, and switching between a wide range of communication protocols including ATM, Ethernet, POS, HDLC, and the IEEE Std.1588™ Precise Time Protocol.

P1021 Critical Performance Parameters

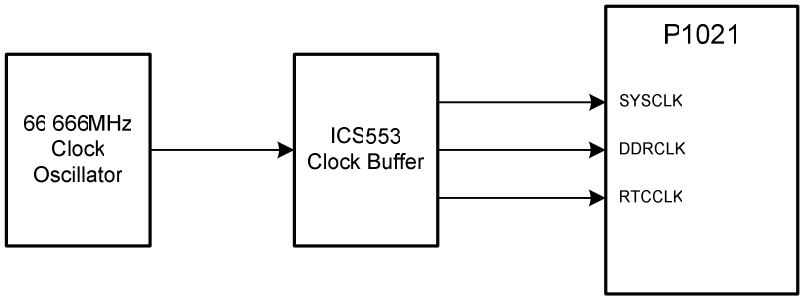
The following list describes the critical performance parameters:

- e500v2 core frequency of 800 MHz at VDD = 1.0 V
- Power consumption of less than 5 W at 800 MHz core speed at VDD = 1.0 V
- 45-nm SOI process technology

- Data rate of up to 800 Mbps for DDR2 and DDR3
- Maximum QUICC Engine block frequency of 400 MHz
- Supply voltages:
  - — Core: 1.0 V
  - — PCI Express, SGMII: 1.0 V
  - — Ethernet: 3.3 or 2.5 V (subject to protocol)
  - — Local bus: 3.3, 2.5, or 1.8 V (Board supports only 3.3 V)
  - — DDR: 1.8 V for DDR2, 1.5 V for DDR3 (conforms to JEDEC standard)
  - — 8-bits of GPIO, I2C, DUART: 3.3 V
  - — SPI, SD/MMC, USB: 3.3 V, 2.5 V, or 1.8 V (Board supports only 3.3 V)
- Operating junction temperature (Tj) range: –40° C to 125° C
- Package: 31 × 31 mm 689-pin TEPGBA II (thermally-enhanced plastic BGA)

P1021 Clocking

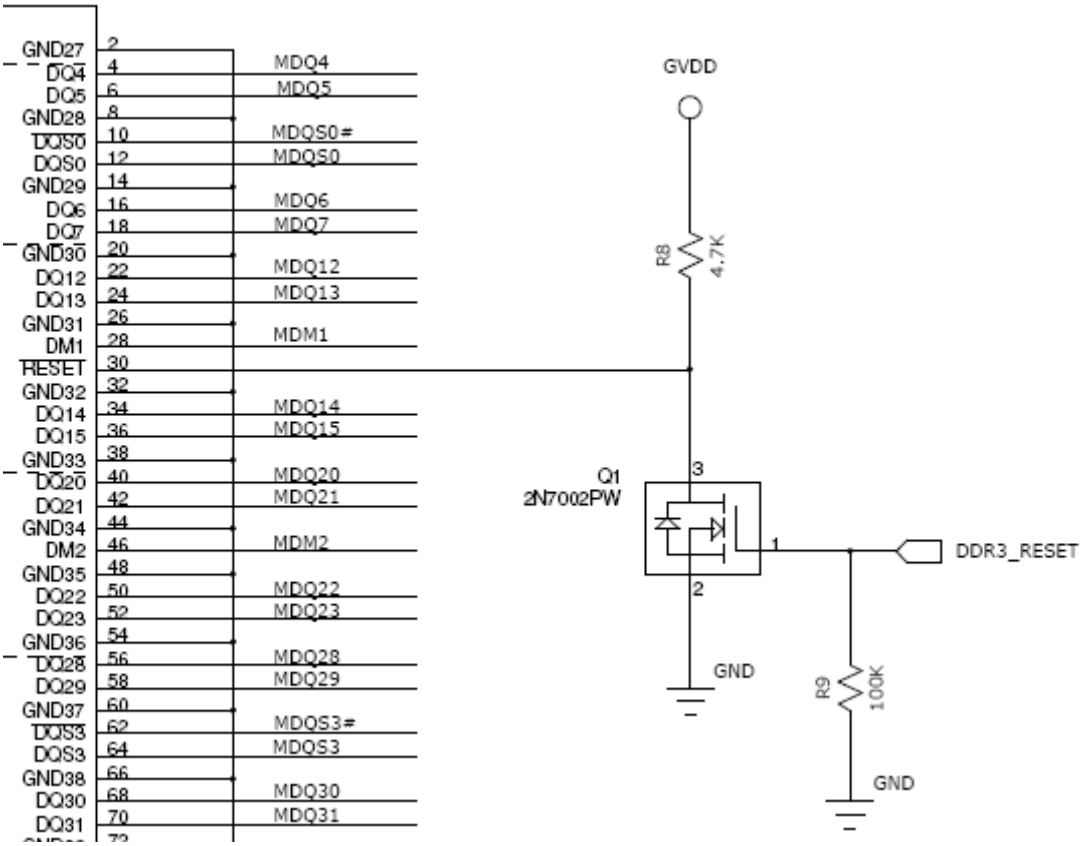
The diagram below shows the processor P1021 clocking implementation on board



3.2 DDR-3 SODIMM

The DDR3 SDRAM interface is implemented with a single, ready-for-operation, 204-pin standard SODIMM socket that supports unbuffered DDR3 SODIMM modules.
The DDR3 SDRAM module operates in 32-bit mode with a clock rate of up to 333MHz MHz (667 MHz data rate) with ECC.
There are four clock pairs MCK[0:3]+/- available on P1021 for DDR3 interface with flexibility of using any of these. On APP card, clock pairs

MCK[2:3]+/- are used. Selection of these pairs is done mainly to help routing.
DDR3 ECC support is provided by connecting MECC[0:7], MDQS8, MDQS8#, and MDQM8 of the memory controller to DQ[32:39], DQS8, DQS8#, and DQM8 of SODIMM.
DDR3 memory needs active low reset on power on. On APP card, this reset is driven from CPLD. Reset generation logic is shown below. R8 is pulled up to GVDD (1.5V) as DDR3 memory runs on this power.



Implementation of the Serial presence-detect (SPD) function is done by connecting the SODIMM's SPD memory to the P1021 device's I2C1 interface.

3.3 NAND Flash

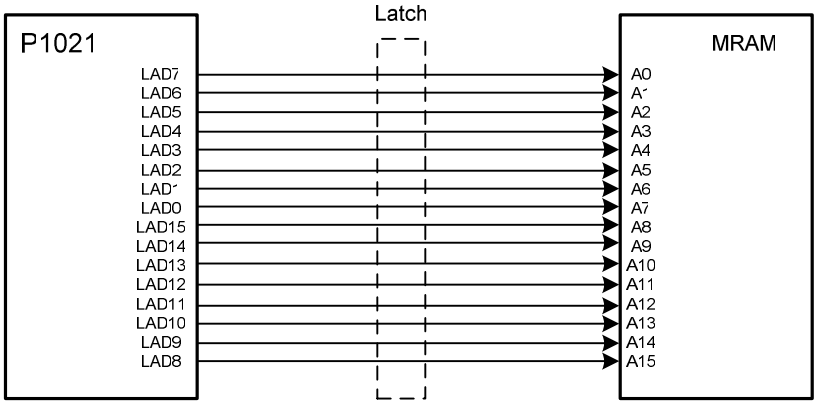
1 Gigabit NAND Flash is implemented on external local bus interface of P1021. To help debug activities, NAND flash socket is assembled on the board. NAND flash socket is footprint compatible NAND flash IC. As P1021 supports big endian, its LAD[7:0] lines are connected to IO[0:7] of flash device.

3.4 MRAM

128K x 8 MRAM memory is implemented on external local bus interface of P1021. There are two limitations while implementing MRAM circuit on APP card.

1. Only 16 address lines can be used on eLBC which can cater to max 64K. This is due to QE implementation on APP card which have pins shared with eLBC
2. Only x8 implementation can be used due to pin multiplexing of ENET5_RXD[1] and LWE1#/LBS1# on PB9 pin. As RMII5 is implemented on APP card, LWE1#/LBS1# is not available. In this case x16 devices on local bus can't be used.

On APP card LAD[0:15] of P1021 are used for interfacing to MRAM device. LA[16:31] can't be used for this purpose as these lines are used for QE Ethernet and serial port implementations. In order to do so It is required to explicitly set LBCR[ABSWP]=1 so that the address LSBs will be driven on LAD[0:15]. And the address multiplexing in case ABSWP=1 is:

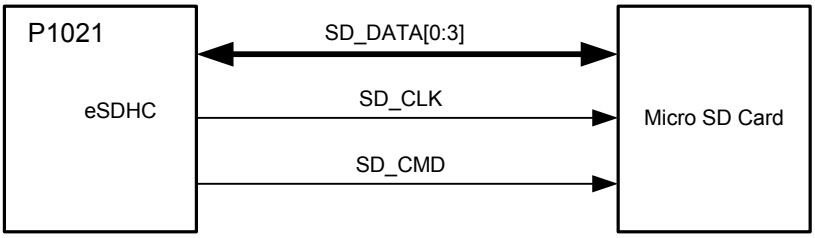


3.5 SPI Flash

128MBit SPI flash is implemented on eSPI Bus. SPI_CS0 is used for selecting this device. The P1021 has the ability to boot from an SPI serial Flash device in addition to supporting other peripheral devices conforming to SPI standard.

3.6 Micro SD Card Interface

The enhanced SD host controller (eSDHC) provides an interface between host system and SD/MMC cards.. For the P1021, booting from on-chip ROM is supported through the eSDHC. A micro SD card socket is provided on the bottom side of the board. This socket support top loading of the micro SD card. Below is the SD card interface diagram



3.7 DUART

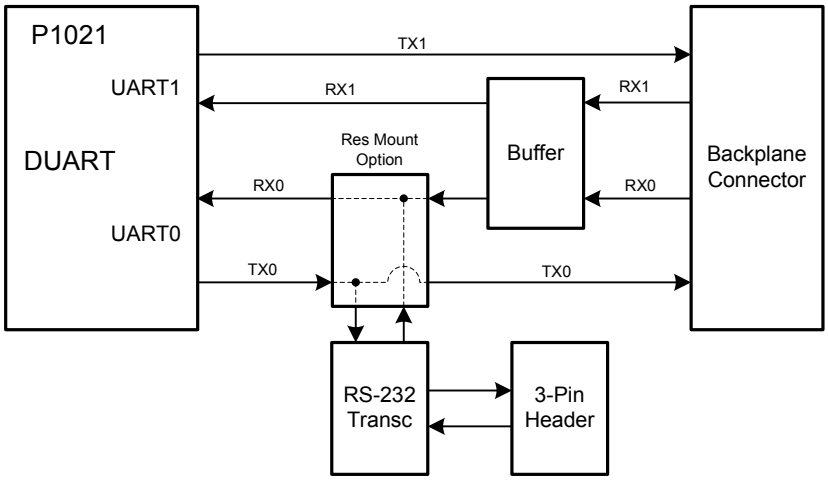
The P1021 has two UART controllers.
The P1021 DUART consists of two independent UARTs and has these distinctive features:

- Full-duplex operation
- Software-programmable baud generators:
- Clear-to-send (CTS) and ready-to-send (RTS) modem control functions
- Software-selectable serial interface data format that includes:
- Overrun, parity, and framing error detection

UART0 signals are not muxed with any other functional signals.
UART1 is muxed with QUICC Engine PortB bit [14–17]. A mux/demux is used to select between the functionalities.
Both UART signals are routed to backplane connectors

For debug activities UART0 is provided with an option to implement RS232 port on APP card.

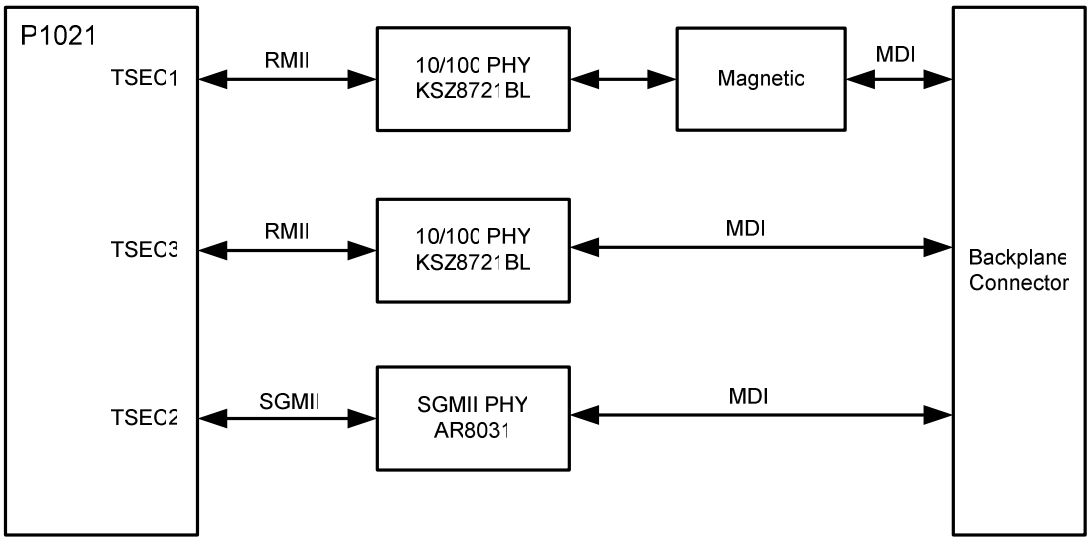
RX lines of UART0 and UART1 are buffered in order to avoid any kind of damage to the P1021. This buffer is enabled only after all the power rails are settled and processor reset is released.



3.8 Enhanced Triple Speed Ethernet Controller (eTSEC) Interface

The P1021 processor supports three eTSEC ports. eTSEC1 supports GMII/RGMII/RTBI/MII/RMII MAC modes; eTSEC2 supports only SGMII; and eTSEC3 supports RGMII/RTBI/RMII.
On the APP card, eTSEC1 and eTSEC3 are implemented in RMII mode while eTSEC2 in SGMII mode. Two on board 10/100 Ethernet PHYs (KSZ8721BL from Micrel) are used to connect to eTSEC1 and eTSEC3 MACs. These PHYs are configured using management interface signals MDC and MDIO.

The diagram below shows the implementation of eTSEC ports on the card



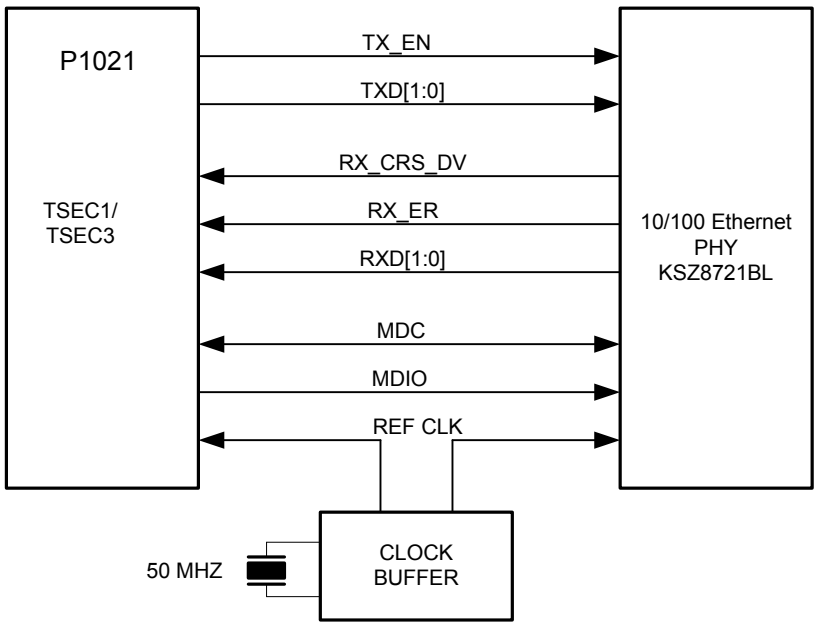
PHY Addresses

TSEC1 PHY: 0x01
TSEC3 PHY: 0x11
TSEC2 PHY: 0x00

RMII Interface

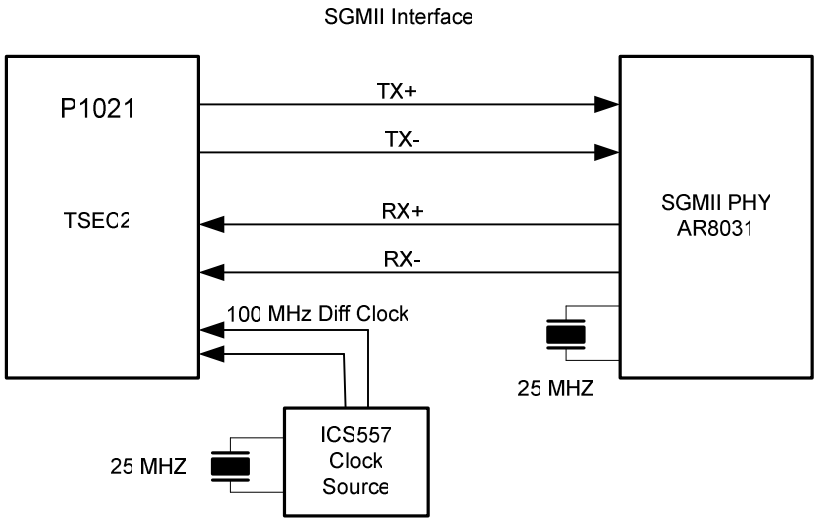
This section describes the reduced media-independent interface (RMII) intended to be used between the PHYs and the GMII MAC. The RMII is a reduced-pin alternative to the IEEE802.3u MII. The RMII reduces the number of signals required to interconnect the MAC and the PHY from a maximum of 18 signals (MII) to 10 signals. To accomplish this objective, the data paths are halved in width and clocked at twice the MII clock frequency, while clocks, carrier sense and error signals have been partly combined.
For 100 Mbps operation, the reference clock operates at 50 MHz, whereas for 10 Mbps operation, the clock remains at 50MHz, but only every 10th cycle is used.
The diagram below depicts the basic components of the reduced media-independent interface and the signals required to establish an eTSEC's connection with a PHY (KSZ8721BL).

RMII Interface



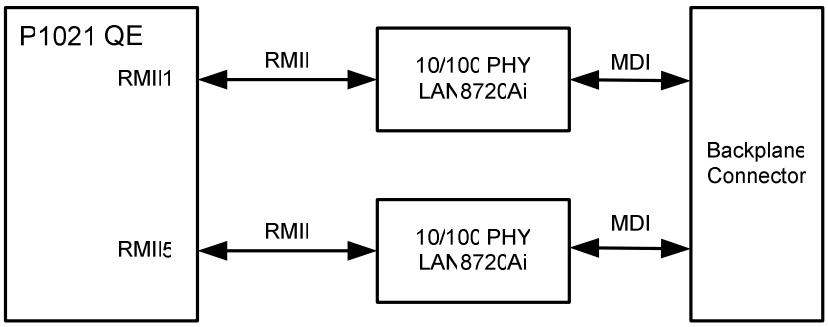
SGMII Interface

This section describes the serial gigabit media-independent interface (SGMII) intended to be used between a SerDes PHY (AR8031) and the eTSEC2 to implement a serial gigabit version of a media-independent interface.
SGMII communication using the eTSEC2 is accomplished through the SerDes interface.
Diagram below depicts the basic components of the SGMII including the signals required to establish eTSEC2 module connection with PHY device (AR8031).



3.9 QUICC Engine RMII1 and RMII5 Interface

The diagram below shows block level implementation of QUICC Engine Ethernet ports RMII1 and RMII5

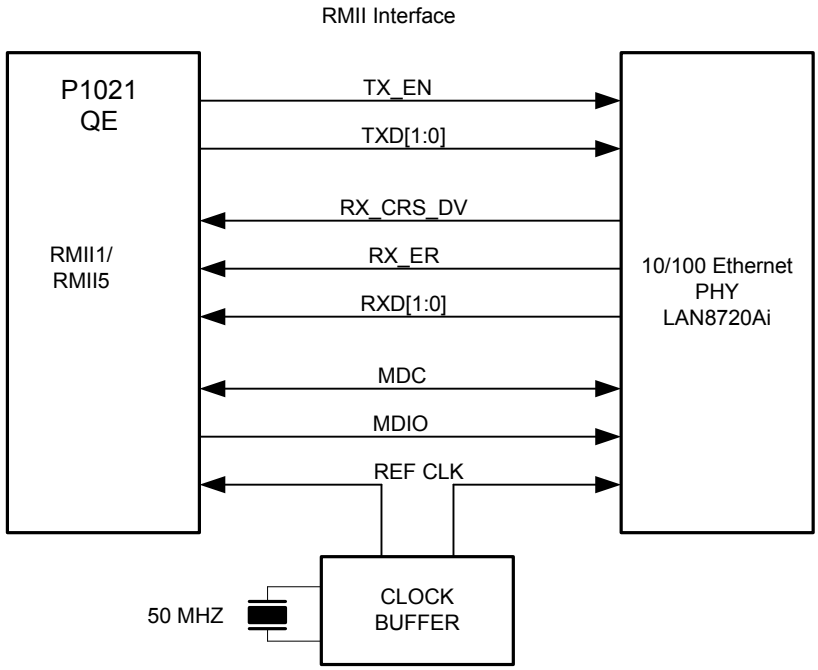


PHY Addresses

RMII1 PHY: 0x0
RMII5 PHY: 0x1

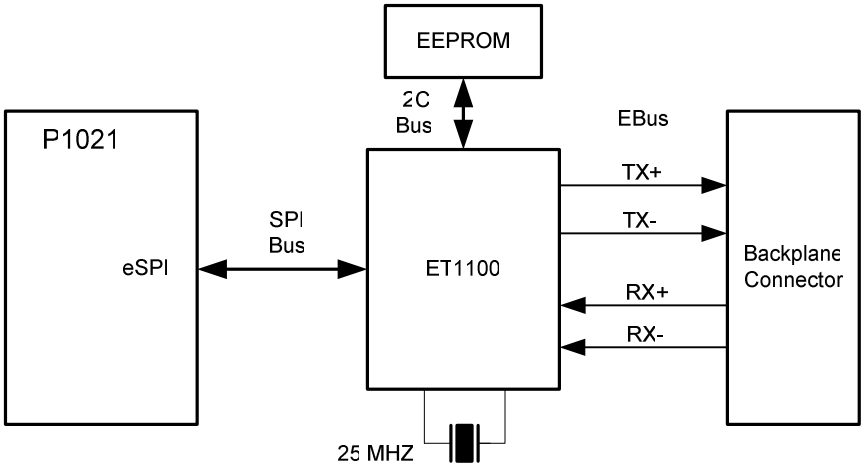
RMII Interface

This section describes the reduced media-independent interface (RMII) intended to be used between the PHYs and the RMII1/RMII5 MAC block of QUICC Engine. The RMII is a reduced-pin alternative to the IEEE802.3u MII. The RMII reduces the number of signals required to interconnect the MAC and the PHY from a maximum of 18 signals (MII) to 10 signals. To accomplish this objective, the data paths are halved in width and clocked at twice the MII clock frequency, while clocks, carrier sense and error signals have been partly combined.
For 100 Mbps operation, the reference clock operates at 50 MHz, whereas for 10 Mbps operation, the clock remains at 50MHz, but only every 10th cycle is used.
The diagram below depicts the basic components of the reduced media-independent interface and the signals required to establish an eTSEC's connection with a PHY (LAN8721Ai).



3.10 EtherCAT Slave Interface

EtherCAT slave interface is implemented using ET1100 on SPI bus of P1021. SPI_CS1 is used as chip select for this interface. ET1100 needs 25MHz crystal for its operation. ET1100 is used in EBus mode. The EBus signals (TX+/- and RX+/-) are routed to backplane connector. There is a 16KBit EEPROM is connected to ET1100 on its local I2C bus. This EEPROM is used for power on configuration of ET1100.



3.11 QUICC Engine SER3 and SER7 Interface

Serial interfaces SER3 and SER7 from QUICC Engine are implemented on board. These ports are directly connected to backplane connector.

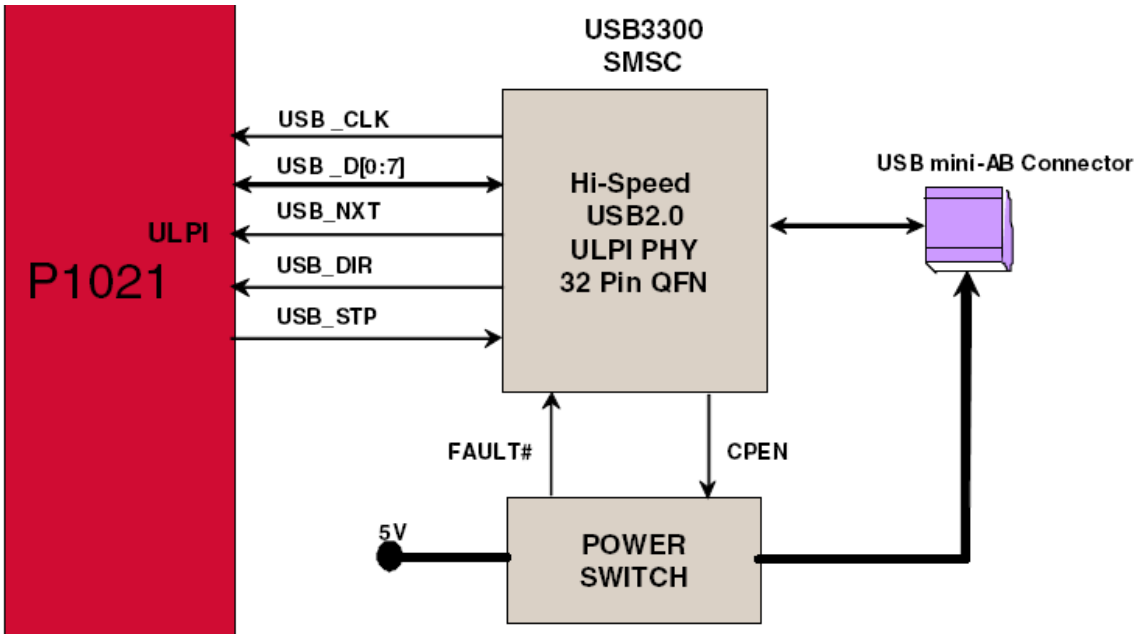
3.12 USB

The P1021 USB 2.0 controller provides point-to-point connectivity complying with the USB specification, Rev 2.0. The USB controller can be configured to operate as a standalone host or device. To complete the USB interface, an external PHY (SMSC's USB3300) is employed and connected to the processor's ULPI signals. The
USB3300 PHY is used. The board features:

- High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation
- Host, device, and OTG modes

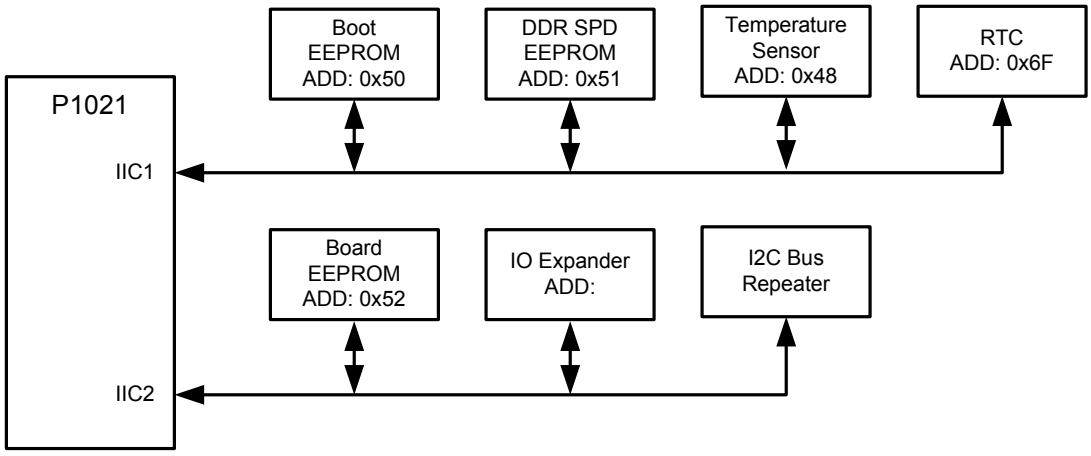
- Mini-AB connector provided in the board

The P1021 supports two USB ports where one port is non-multiplexed and the other is multiplexed with local bus. APP card has a PHY connected to the non-multiplexed port. The other port is not used



3.13 I2C

Figure below shows a block diagram of the I2C interfaces implemented on APP card.



The block diagram illustrates intended I2C1 (non-muxed) bus usage:

- Used with boot sequencer EEPROM
- Read DDR SPD EEPROMs; provides correct information for using SODIMM
- Read board temperature near the P1021
- Obtain Real Time Clock information for application program synchronization

The I2C2 (muxed) bus is intended for use with an on-board BRD EEPROM storing board-related information such as history updates and PCB and CPU revisions. The I2C2 bus is multiplexed with the QUICC Engine bus, and an appropriate mux/demux is used to select between the functionalities.

3.14 CPLD

A CPLD part EPM3064 from Altera is used on board. Here is the list of functions implemented in CPLD

- Power sequencing
- System power good generation
- Reset generation
- P1021 power-on reset configuration control
- Clock control

25MHz clock is supplied to CPLD. There is an option provided to supply 66.666MHz to CPLD.

The table below lists details of the signals implemented on the CPLD

SR NO	SIGNAL	DIR	ACTIVE STATE	Function
1	CPU_HRESET#	OUT	LOW	**On PGOOD_SYS:** Should be asserted LOW for 200uS and then deassert. **ALWAYS:** Pass COP_HRESET# to this pin such that changes in COP_HRESET# is reflected in CPU_RESET#
2	CPU_SRESET#	OUT	LOW	**On PGOOD_SYS:** Should be asserted LOW for 100uS and then deassert. **ALWAYS:** Pass COP_SRESET# to this pin such that changes in COP_SRESET# is reflected in CPU_SRESET#
3	CPU_HRESET_REQ#	IN	LOW	
4	CPU_TRST#	OUT	LOW	**On PGOOD_SYS:** Should be asserted LOW for 100uS and then deassert. **ALWAYS:** Pass COP_TRST# to this pin such that changes in COP_TRST# is reflected in CPU_TRST#
5	COP_HRESET#	IN	LOW	
6	COP_SRESET#	IN	LOW	
7	COP_TRST#	IN	LOW	
8	DDR3_RESET	OUT	HIGH	Drive HIGH at power up. When CPU_HRESET# is deasserted HIGH, start driving it LOW
9	SGMII_PHY_RESET#	OUT	LOW	Drive LOW at power up. After a delay of 100us from CPU_HRESET# going HIGH, start driving it HIGH
10	ENET_PHY_RESET#	OUT	LOW	Drive LOW at power up. After a delay of 100us from CPU_HRESET# going HIGH, start driving it HIGH
11	TSEC_PHY_RESET#	OUT	LOW	Drive LOW at power up. After a delay of 100us from CPU_HRESET# going HIGH, start driving it

				HIGH
12	MUX_EN1#	OUT	LOW	Should be made LOW after PGOOD_SYS becomes HIGH
13	MUX_EN2#	OUT	LOW	Should be made LOW after PGOOD_SYS becomes HIGH
14	MUX_SEL1	OUT	HIGH	At power up, drive it LOW. Drive it HIGH within 5 system clock cycles (66.666MHz) from the CPU_HRESET# going HIGH
15	MUX_SEL2	OUT	HIGH	At power up, drive it LOW. Drive it HIGH within 5 system clock cycles (66.666MHz) from the CPU_HRESET# going HIGH
16	BUF_EN#	OUT	LOW	At power up, drive it LOW. Drive it HIGH within 5 system clock cycles (66.666MHz) from the CPU_HRESET# going HIGH
17	PWR_ON_GVDD	OUT	HIGH	At power up, drive it LOW. Drive it HIGH after sampling PGOOD_VDD_CPU HIGH
18	PWR_OFF_VDD_CPU	OUT	HIGH	RESERVE. Keep it in Z state
19	PWR_GOOD_DDR3	IN	HIGH (OD)	
20	SD_1588_CLK_EN	OUT	HIGH	RESERVE. Keep it in Z state
21	PGOOD_SYS	OUT	HIGH	Should be asserted HIGH after PGOOD_VDD_CPU and PWR_GOOD_DDR3 are HIGH
22	PGOOD_VDD_CPU	IN	HIGH	
23	CPLD_RESET#	IN	LOW	

CPLD JTAG Header

Pin	Function	Pin	Function
1	TCK	2	GND
3	TDO	4	VCC
5	TMS	6	NC

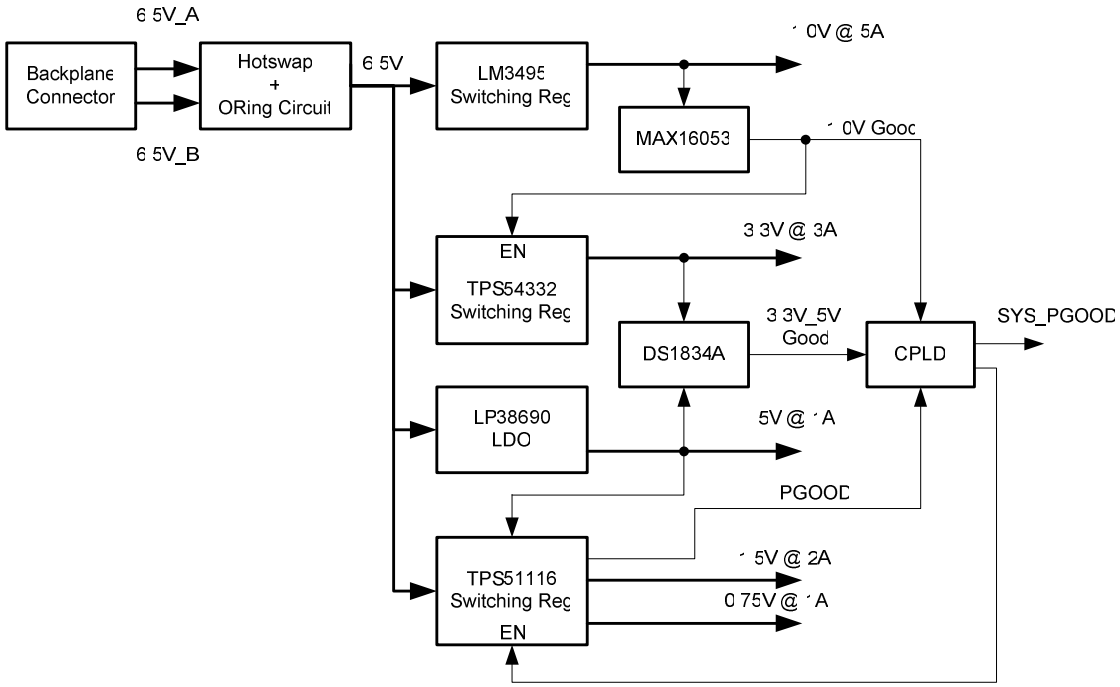
7	NC	8	NC
9	TDI	10	GND

3.15 Hot Swap Control

A hot-swap circuit is used to make this board ready for live insertion and removal in the system. The circuit also provides oring of the two input voltages 6.5A and 6.5B. This circuit is enabled only when it sit properly in the backplane.

3.16 Power

Power delivery diagram along with system power good generation circuit is shown below.



Board Power Requirement

Sr No	Component	Condition	Typ Current (A)	Max Current (A)	Typ Power (W)	Max Power (W)
1V Requirement						
1	P1012 Core	P1012 Core @ 800MHz		2.7		2.7
		PCI Express, x4 Link (SVDD)	0.229	0.321	0.11	
		SGMII (SVDD)	0.096	0.134	0.096	
	Current at 1V			3.155		
1.5V Requirement						
1	P1012 (GVDD)	DDR3 75% utilization @ 667MHz	0.547	0.765	0.82	
2	DDR3 SODIMM 1GB @ 667MHz	All banks interleaved read current		2		
	Current at 1.5V			2.765		
0.75V Requirement						
1	DDR3 SODIMM 1GB @ 667MHz	Termination Voltage Vtt		0.6		
	Current at 0.75V			0.600		
3.3V Requirement						
1	P1012	eLBC (BVDD)	0.014	0.020	0.047	
		eTSEC (RGMII) (LVDD)	0.075	0.105	0.248	
		eSDHC (CVDD)	0.004	0.006	0.014	
		USB (CVDD)	0.004	0.005	0.012	
		eSPI (CVDD)	0.003	0.004	0.01	
		I2C (OVDD)	0.001	0.001	0.002	
		DUART (OVDD)	0.002	0.003	0.006	
		IEEE 1588 (LVDD)	0.002	0.003	0.007	
		QUICC Engine (BVDD)	0.024	0.034	0.08	
2	S25FL128P0XNFI001 SPI Flash	Active Page Program Current		0.026		
3	S29GL01GP11TFIR10 NOR Flash	Active Read Current	0.06	0.11		
4	MR4A16BCMA35 MRAM	AC active supply current - write modes1	0.11	0.154		
5	M24256-BWMN6TP EEPROM	Supply current (Write)		0.005		
6	AT24C01BN-SH-B EEPROM	Supply current (Write)	0.002	0.003		
7	LAN8720Ai Ethernet PHY	100BASE-T /W TRAFFIC (2 Nos)	0.1	0.108	0.164	0.179
8	USB3300 USB PHY	FS Transmit 3.3V Current	0.036	0.042		

9	KSZ8721BLI Ethernet PHY	Normal 100BASE-TX (2 Nos)	0.302	0.423		
10	SD Card			0.2		
11	LED	(12 Nos)		0.12		
12	CPLD			0.3		
	Current at 3.3V			1.672		
5V Requirement						
1	USB Port			0.5		
	Current at 5V			0.500		

Power Sequencing

The processor P1021 requires that its power rails be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:
1. VDD, VDDC, AVDD, BVDD, LVDD, CVDD, OVDD, SVDD_SRDS and, XVDD_SRDS

2. GVDD

All supplies must be at their stable values within 50 ms.
Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

Here is list of list of voltages used for P1021

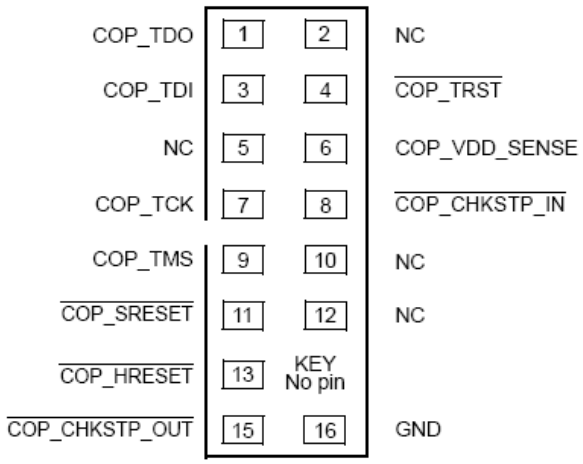
- VDD, VDDC, AVDD, SVDD_SRDS, XVDD_SRDC => 1.0V
- BVDD, LVDD, CVDD, OVDD => 3.3V
- GVDD => 1.5V

3.17 Debug Support

JTAG COP Header

The JTAG header provides a connection between the P1021 device and an external, compatible JTAG converter. The default is the CodeWarrior USB TAP.

The diagram below shows COP connector physical pinouts



Debug RS-232 Port

An RS-232 port is provided on board just for debug purpose only. This is implemented using DUART port0 of P1021. The access to this port is available through 3-pin header. Below is the pin assignment for this header (J8).

PIN #	SIGNAL
1	TX
2	RX
3	GND

Debug LEDs

There are two LEDs provided to help debugging of the board. These are defined as below.

LED	Color	Description
LED1 (D26)	Green	User Programmable
LED2 (D27)	Green	User Programmable

Manual Reset Switch

There is a manual switch (SW1) provided on board to reset the board. This switch is accessible on the front panel. Whenever it is pressed (activated), CPLD gets reset which in turn generates the system reset.

Test Points/ Jumpers

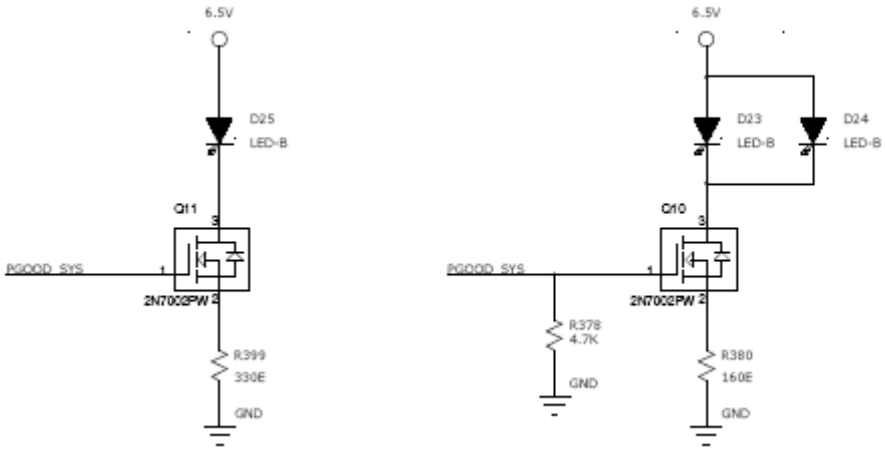
Test points are provided for probing important signals, power and ground nets during debugging/ testing.

3.18 Front Panel LEDs

Table below describes the LEDs used on front panel

Name	Description	Controlled by	Label	Color	No of LEDs
STATUS					
Power	Power Supply(ies) status ok	HW (CPLD)	POWER	Blue	3
Active	Card is controlling output channels	SW	ACTIVE	Green	1
Ready	Card is healthy and has no detectable faults	SW	READY	Green	1
Alarm	Card has a detectable non-critical issue	SW	ALARM	Yellow	1
Fault	Card has a critical error	SW/HW	FAULT	Red	1
CPU	CPU is active/heartbeat	SW	CPU	Green	1
Learn	Card in initializing/booting/learning from peer	SW	LEARN	Green	1
COMMUNICATIONS					
Ecat LINKACT(x)	EtherCAT Link/Activity	HW (U15)		Green	1
Ecat LINKACT(x)	EtherCAT Speed	HW (U15)		Yellow	1
Serial Tx/Rx	Serial port activity - 2/port	HW (U1)	Tx/Rx	Green	8
Ethernet	Ethernet Activity - 2/port	HW (U13, U14)		Green	2
Ethernet	Ethernet Speed	HW (U13, U14)		Yellow	2

All status LEDs excluding "Power" are directly driven by the processor. Power LEDs are driven by the CPLD after confirming all the on board rails are within the specified limit. Below the circuit used to drive power LEDs.



3.19 Backplane Connectors

This section gives the details of the backplane connectors used on the board.

Connector : 1 (54 Pins Connector)		
Pin No.	**Signal Name**	**Description**
A1	APP_IES+	MII interface Transmit data to IES (+)
B1	APP_IES-	MII interface Transmit data to IES(-)
C1	GND	Ground
D1	IES_APP+	MII interface Receive data from IES(+)
E1	IES_APP-	MII interface Receive data from IES(-)
F1	GND	Ground
G1	APP_ECAT+	MII interface Transmit data to ECAT(+)
H1	APP_ECAT-	MII interface Transmit data to ECAT(-)
I1	GND	Ground
A2	GND	Ground
B2	ECAT_APP+	MII interface Receive data from ECAT(+)
C2	ECAT_APP-	MII interface Receive data from ECAT(-)
D2	GND	Ground
E2	NC	NC
F2	NC	NC
G2	GND	Ground
H2	APP_IES_EBUS+	EBUS interface Transmit data to opposite IES(+)

I2	APP_IES_EBUS-	EBUS interface Transmit data to opposite IES(-)
A3	IES_APP_EBUS+	EBUS interface Receive data from opposite IES(+)
B3	IES_APP_EBUS-	EBUS interface Receive data from opposite IES(-)
C3	GND	Ground
D3	APP_MBUS_1_DE	Transmit Enable to MOD BUS Port 1
E3	APP_MBUS_2_DE	Transmit Enable to MOD BUS Port 2
F3	GND	Ground
G3	APP_TLINK_1_DE	Transmit Enable to Train Link Port 1
H3	APP_TLINK_2_DE	Transmit Enable to Train Link Port 2
I3	GND	Ground
A4	GND	Ground
B4	TLINK_APP_2	Receive Data 2 from Train Link
C4	APP_TLINK_2	Transmit Data 2 to Train Link
D4	GND	Ground
E4	APP-A_E4	Connector Short Pin
F4	NC	NC
G4	GND	Ground
H4	TLINK_APP_1	Receive Data 1 from Train Link
I4	APP_TLINK_1	Transmit Data 1 to Train Link
A5	APP_MBUS_2	Transmit Data 2 to MODBUS
B5	MBUS_APP_2	Receive Data 2 from MODBUS
C5	GND	Ground
D5	APP_MBUS_1	Transmit Data 1 to MODBUS
E5	MBUS_APP_1	Receive Data 1 from MODBUS
F5	GND	Ground
G5	APP_APP_3-	GBE between APPs
H5	APP_APP_3+	GBE between APPs
I5	GND	Ground
A6	GND	Ground
B6	APP_APP_2-	GBE between APPs
C6	APP_APP_2+	GBE between APPs
D6	GND	Ground
E6	APP_APP_1-	GBE between APPs
F6	APP_APP_1+	GBE between APPs
G6	GND	Ground
H6	APP_APP_0-	GBE between APPs
I6	APP_APP_0+	GBE between APPs

Connector :2 (72 Pins Connector)		
Pin No.	**Signal Name**	**Description**
A1	APP_EEC1+	10/100 Eth Interface Transmit to EEC1(+)
B1	APP_EEC1-	10/100 Eth Interface Transmit to EEC1(-)
C1	GND	Ground
D1	EEC_APP-1+	10/100 Eth Interface Receive from EEC1(+)
E1	EEC_APP-1-	10/100 Eth Interface Receive from EEC1(-)
F1	GND	Ground
G1	APP_EEC2+	10/100 Eth Interface Transmit to EEC2(+)
H1	APP_EEC2-	10/100 Eth Interface Transmit to EEC2(-)
I1	GND	Ground
A2	GND	Ground
B2	EEC_APP-2+	10/100 Eth Interface Receive from EEC2(+)
C2	EEC_APP-2-	10/100 Eth Interface Receive from EEC2(-)
D2	GND	Ground
E2	GND	Ground
F2	2V5_APP_EEC-1	2.5V supply to EEC1 port
G2	GND	Ground
H2	2V5_APP_EEC-2	2.5V supply to EEC2 port
I2	GND	Ground
A3	NC	NC
B3	GND	Ground
C3	NC	NC
D3	GND	Ground
E3	APP_IES_SCL-A	I2C Clock
F3	GND	Ground
G3	APP_IES_SDA-A	I2C Data
H3	GND	Ground
I3	NC	NC
A4	GND	Ground
B4	NC	NC
C4	GND	Ground
D4	NC	NC
E4	APP-A_E4	Connector Short Pin
F4	NC	NC
G4	GND	Ground
H4	APP_IES_DET	APP board detect signal from same side IES
I4	GND	Ground

A5	APP_IES_DET_OPP	APP board detect signal from opp. Side IES
B5	GND	Ground
C5	NC	NC
D5	GND	Ground
E5	NC	NC
F5	GND	Ground
G5	NC	NC
H5	GND	Ground
I5	NC	NC
A6	GND	Ground
B6	NC	NC
C6	GND	Ground
D6	IES_APP_DET_OPP	Opposite side IES board detect from APP
E6	GND	Ground
F6	IES_APP_DET	Same side IES board detect from APP
G6	GND	Ground
H6	GND	Physical Slot addr 0
I6	GND	Ground
A7	NC	Physical Slot addr 1
B7	GND	Ground
C7	PCC_APP_OPP4	Signal 4 input from opp side PCC
D7	GND	Ground
E7	PCC_APP_OPP3	Signal 3 input from opp side PCC
F7	GND	Ground
G7	PCC_APP_OPP2	Signal 2 input from opp side PCC
H7	GND	Ground
I7	PCC_APP_OPP1	Signal 1 input from opp side PCC
A8	GND	Ground
B8	PCC_APP4	Signal 4 input from same side PCC
C8	GND	Ground
D8	PCC_APP3	Signal 3 input from same side PCC
E8	GND	Ground
F8	PCC_APP2	Signal 2 input from same side PCC
G8	GND	Ground
H8	PCC_APP1	Signal 1 input from same side PCC
I8	GND	Ground

4 Schematic Design

4.1 Design Tool

Schematic entry is done PAD9.3

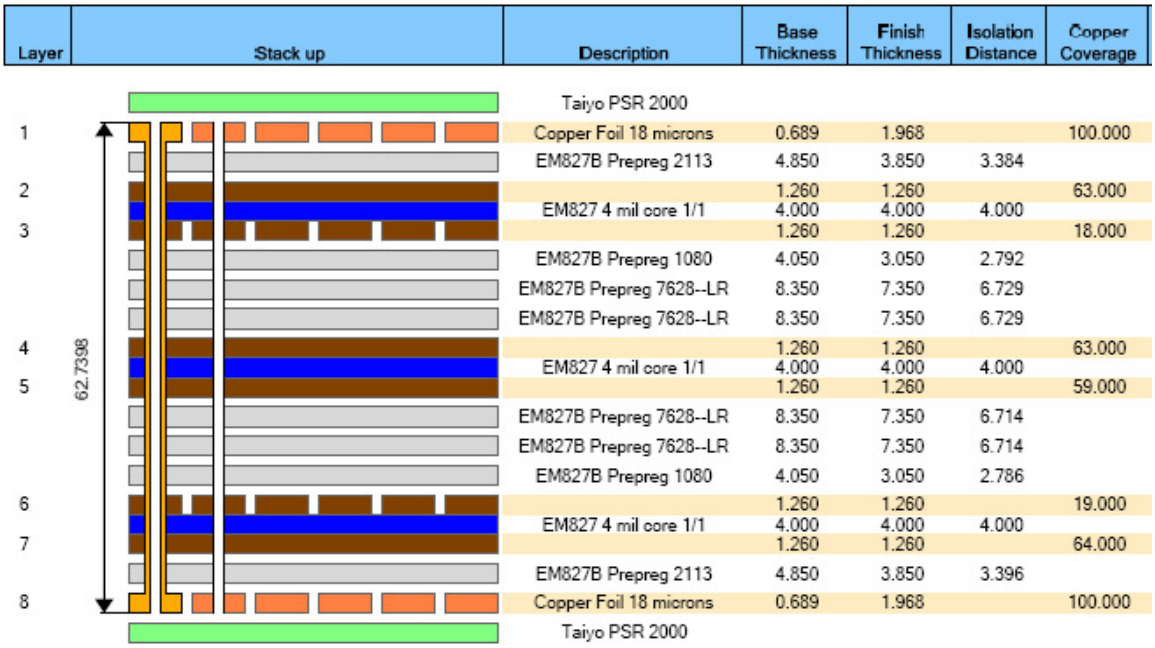
5 Board Layout Design

5.1 Board Thickness

Thickness of the Board designed is 1.6mm±10% [0.063" ± 10%]

5.2 Board Stack-up

The Main Board is designed with four layer stack-up with no blind or buried vias. Most of the components are placed top side of the board except for few discrete which are placed on bottom.



Layer	Stack up	Description	Base Thickness	Finish Thickness	Isolation Distance	Copper Coverage
		Taiyo PSR 2000				
1		Copper Foil 18 microns	0.689	1.968		100.000
		EM827B Prepreg 2113	4.850	3.850	3.384	
2			1.260	1.260		63.000
		EM827 4 mil core 1/1	4.000	4.000	4.000	
3			1.260	1.260		18.000
		EM827B Prepreg 1080	4.050	3.050	2.792	
		EM827B Prepreg 7628--LR	8.350	7.350	6.729	
		EM827B Prepreg 7628--LR	8.350	7.350	6.729	
4			1.260	1.260		63.000
		EM827 4 mil core 1/1	4.000	4.000	4.000	
5			1.260	1.260		59.000
		EM827B Prepreg 7628--LR	8.350	7.350	6.714	
		EM827B Prepreg 7628--LR	8.350	7.350	6.714	
		EM827B Prepreg 1080	4.050	3.050	2.786	
6			1.260	1.260		19.000
		EM827 4 mil core 1/1	4.000	4.000	4.000	
7			1.260	1.260		64.000
		EM827B Prepreg 2113	4.850	3.850	3.396	
8		Copper Foil 18 microns	0.689	1.968		100.000
		Taiyo PSR 2000				

Appendix - A

Power-on Reset strapping options on APP card

System PLL Ratio

Functional Signals	Value (Binary)	CCB Clock : SYSCLK Ratio	APP Inplementation
LA[29:31] No Default	000	4:1	LA29: Pull-down (R228: GND) LA30: Pull-up (R220: 3.3V; R227: DNI) LA31: Pull-down (R279: GND; R278: DNI)
	001	5:1	
	010	6:1	
	other	Reserved	

DDR PLL Ratio

Functional Signals	Value (Binary)	DDR Complex : DDRCLK Ratio	APP Inplementation
TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 No Default	000	3:1	TSEC_1588_CLK_OUT: Pull-up (R299: 3.3V; R233: DNI) TSEC_1588_PULSE_OUT1: Pull-down (R311: GND; R300: DNI) TSEC_1588_PULSE_OUT2: Pull-down (R312: GND; R301: DNI)
	001	4:1	
	010	6:1	
	011	8:1	
	100	10:1	
	101	Reserved	
	110	Reserved	
	111	Synchronous mode	

e500 Core0 PLL Ratios

Functional Signals	Value (Binary)	e500 Core:CCB Clock Ratio	APP Inplementation
LBCTL, LALE, LGPL2/LOE/LFRE No Default	000	Reserved	LBCTL: Pull-up (R283: 3.3V; R291: DNI) LALE: Pull-down (R292: GND; R284: DNI) LGPL2/LOE/LFRE: Pull-down (R293: GND; R285: DNI)
	001	Reserved	
	010	1:1	
	011	3:2 (1.5:1)	
	100	2:1	
	101	5:2 (2.5:1)	
	110	3:1	
	111	Reserved	

e500 Core1 PLL Ratios

Functional Signals	Value (Binary)	e500 Core:CCB Clock Ratio	APP Inplementation
LWE0, UART_SOUT1, READY_P1 No Default	000	Reserved	LWE0: Pull-up (R286: 3.3V; R294: DNI) UART_SOUT1: Pull-down (R267: GND; R250: DNI) READY_P1: Pull-down (R247: GND; R246: DNI)
	001	Reserved	
	010	1:1	
	011	3:2 (1.5:1)	
	100	2:1	
	101	5:2 (2.5:1)	
	110	3:1	
	111	Reserved	

Boot ROM Location

Functional Signals	Value (Binary)	Meaning	APP Inplementation
TSEC3_TXD[2:0], TSEC1_TX_ER Default (1111)	0000	PCI Express 1	TSEC3_TXD2: Pull-up (R315: 3.3V; R305: DNI) TSEC3_TXD1: Pull-down (R254: GND; R253: DNI) TSEC3_TXD0: Pull-down (R252: GND; R251: DNI) TSEC1_TX_ER: Pull-down (R304: GND; R219: DNI)
	0001	PCI Express 2	
	0010	Reserved	
	0011	Reserved	
	0100	DDR controller	
	0101	Reserved	
	0110	On-chip boot ROM—SPI configuration	
	0111	On-chip boot ROM—eSDHC configuration	
	1000	Local bus FCM—8-bit NAND flash small page	
	1001	Reserved	
	1010	Local bus FCM—8-bit NAND flash large page	
	1011	Reserved	
	1100	Reserved	
	1101	Local bus GPCM—8-bit ROM	
	1110	Local bus GPCM—16-bit ROM	
	1111	Local bus GPCM—16-bit ROM (default)	

Host/Agent Configuration

Functional Signals	Value (Binary)	Meaning	APP Inplementation
LWE1, LA[18:19] Default (111)	000	P1021 acts as an agent on all its PCI Express interfaces	LWE1: Pull-up (R107: 3.3V) LA18: Pull-up (R235: 3.3V) LA19: Pull-up (R258: 3.3V)
	001	P1021 acts as an agent on PCI Express 1 and acts as a host on PCI Express 2.	
	010	P1021 acts as a host on PCI Express 1 and acts as an agent on PCI Express 2.	
	011 - 110	Reserved	
	111	P1021 acts as the host processor/root complex for all PCI Express interfaces (default).	

I/O Port Selection

Functional Signals	Value (Binary)	Meaning	APP Inplementation
TSEC1_TXD[3:1], CFG_IO_PORTS3	0000	PCI Express 1 (×1) (2.5Gbps) → SerDes lane 0 SerDes lanes 1–3 powered down	TSEC1_TXD3: Pull-up (R229: 3.3V) TSEC1_TXD2: Pull-up (R256: 3.3V) TSEC1_TXD1: Pull-up (R265: 3.3V) CFG_IO_PORTS3: Pull-down (R232:
	0001	SerDes lanes 0–3 powered down	

Default (1111)	0100-0101	Reserved	GND)
	0110	PCI Express 1 (×4) (2.5 Gbps) → SerDes lanes 0–3	
	0111-1101	Reserved	
	1110	PCI Express 1 (x1) (2.5 Gbps) → SerDes lane 0 PCI Express 2 (x1) (2.5 Gbps) → SerDes lane 1 SGMII eTSEC2 (x1) (1.25Gbps) → SerDes lane 2 SGMII eTSEC3 (x1) (1.25Gbps) → SerDes lane 3	
	1111	PCI Express 1 (x2) (2.5 Gbps) → SerDes lanes 0–1 SGMII eTSEC2 (x1) (1.25Gbps) → SerDes lane 2 SGMII eTSEC3 (x1) (1.25Gbps) → SerDes lane 3 (see Note) (default)	

CPU Boot Configuration

Functional Signals	Value (Binary)	Meaning	APP Inplementation
LA27, LA16 Default (11)	00	CPU boot holdoff mode for both cores. The e500 cores are prevented from booting until configured by an external master	LA27: Pull-up (R240: 3.3V; R241: DNI) LA16: Pull-down (R238: GND; R237: DNI)
	01	e500 core 1 is allowed to boot without waiting for configuration by an external master, while e500 core 0 is prevented from booting until configured by an external master or the other core	
	10	e500 core 0 is allowed to boot without waiting for configuration by an external master, while e500 core 1 is prevented from booting until configured by an external master or the other core	
	11	Both e500 cores are allowed to boot without waiting for configuration by an external master (default)	

Boot Sequencer Configuration

Functional Signals	Value (Binary)	Meaning	
LGPL3/LFWP,	00	Reserved	LGPL3: Pull-up (R287: 3.3V; R295:

LGPL5 Default (11)	01	Normal I2C addressing mode is used. Boot sequencer is enabled and loads configuration information from a ROM on the I2C1 interface. A valid ROM must be present	DNI) LGPL5: Pull-up (R289: 3.3V; R297: DNI)
	10	Extended I2C addressing mode is used. Boot sequencer is enabled and loads configuration information from a ROM on the I2C1 interface. A valid ROM must be present	
	11	Boot sequencer is disabled. No I2C ROM is accessed (default)	

DDR SDRAM Type

Functional Signals	Value (Binary)	Meaning	APP Inplementation
CFG_DRAM_TYPE Default (1)	0	DDR2 1.8 V, CKE low at reset	CFG_DRAM_TYPE: Pull-up (R225: 3.3V)
	1	DDR3 1.5 V, CKE low at reset (default)	

SerDes Reference Clock Configuration

Functional Signals	Value (Binary)	Meaning	APP Inplementation
TSEC_1588_ALARM_OUT1 Default (1)	0	SerDes expects a 125 MHz reference clock frequency	TSEC_1588_ALARM_OUT1: Pull-up (R274: 3.3V)
	1	SerDes expects a 100 MHz reference clock frequency (default)	

eTSEC3 SGMII Mode

Functional Signals	Value (Binary)	Meaning	APP Inplementation
TSEC_1588_ALARM_OUT2 Default (1)	0	eTSEC3 Ethernet interface operates in SGMII mode and uses SGMII SerDes lane 3 pins	TSEC_1588_ALARM_OUT2: Pull-up (R290: 3.3V)
	1	eTSEC3 Ethernet interface operates in standard parallel interface mode and uses the TSEC3_* pins (default)	

eTSEC1 Width

Functional Signals	Value (Binary)	Meaning	APP Inplementation
EC_MDC Default (1)	0	eTSEC1 Ethernet interface operates in reduced pin mode (either RGMII or RMII mode)	EC_MDC: Pull-down (R255: GND)
	1	eTSEC1 Ethernet interface operates in standard width MII mode (default)	

eTSEC1 Protocol

Functional Signals	Value (Binary)	Meaning	APP Inplementation
TSEC1_TXD0, TSEC3_TXD3 Default (11)	00	Reserved	TSEC1_TXD0: Pull-down (R262: GND) TSEC3_TXD3: Pull-up (R314: 3.3V)
	01	The eTSEC1 controller operates using the MII protocol (or RMII if configured in reduced mode as described in “eTSEC1 Width”).	
	10	The eTSEC1 controller operates using the RGMII protocol if configured in reduced mode as described in “eTSEC1 Width”	
	11	Reserved	

eTSEC3 Protocol

Functional Signals	Value (Binary)	Meaning	APP Inplementation
UART_RTS0, UART_RTS1 Default (11)	00	Reserved	UART_RTS0: Pull-down (R271: GND) UART_RTS1: Pull-up (R249: 3.3V)
	01	The eTSEC3 controller operates using the RMII protocol if not configured to operate in SGMII mode	
	10	The eTSEC3 controller operates using the RGMII protocol if not configured to operate in SGMII mode	
	11	Reserved	

Memory Debug Configuration

Functional Signals	Value (Binary)	Meaning	APP Inplementation

CFG_MEM_DEBUG Default (1)	0	Debug information from the enhanced local bus controller (eLBC) is driven on the MSRCID and MDVAL signals	CFG_MEM_DEBUG: Pull-up (R226: 3.3V; R234: DNI)
	1	Debug information from the DDR SDRAM controller is driven on the MSRCID and MDVAL signals (default)	

DDR Debug Configuration

Functional Signals	Value (Binary)	Meaning	APP Inplementation
CFG_DDR_DEBUG Default (1)	0	Debug information is driven on the ECC pins instead of normal ECC I/O. ECC signals from memory devices must be disconnected.	CFG_DDR_DEBUG: Pull-up (R280: 3.3V; R281: DNI)
	1	Debug information is not driven on ECC pins. ECC pins function in their normal mode (default)	

General-Purpose POR Configuration

Functional Signals	Value (Binary)	Meaning	APP Inplementation
LAD[0:15] No Default		General-purpose POR configuration vector to be placed in GPPORCR.	Not Implemented

Engineering Use POR Configuration

Functional Signals	Value (Binary)	Meaning	APP Inplementation
LA[20:22], UART_SOUT[0], MSRCID[4] Default (1_1111)	1_1111	Default operation	LA20: pull-up (R239: 3.3V) LA21: pull-up (R260: 3.3V) LA22: pull-up (R236: 3.3V) UART_SOUT[0]: pull-up (R248: 3.3V) MSRCID[4]: pull-up (R302: 3.3V)
	0_0000-1_1110	Reserved	

eLBC ECC Enable Configuration

Functional Signals	Value (Binary)	Meaning	APP Inplementation
MSRCID0 Default (1)	0	eLBC ECC checking is disabled.	MSRCID0: pull-down (R296: GND; R110: DNI)
	1	Default operation: eLBC ECC checking is enabled	

System Speed

Functional Signals	Value (Binary)	Meaning	APP Inplementation
LA28 Default (1)	0	Reserved	LA28: pull-up (R221: 3.3V)
	1	SYSCLK frequency is at or above 66 MHz (default)	

Platform Speed

Functional Signals	Value (Binary)	Meaning	APP Inplementation
LA23 Default (1)	0	Platform clock frequency is above 267 MHz and below 300 MHz	LA23: pull-up (R223: 3.3V; R231: DNI)
	1	Platform clock frequency is at or above 300 MHz (default)	

Core 0 Speed

Functional Signals	Value (Binary)	Meaning	APP Inplementation
LA24 Default (1)	0	Core 0 clock frequency is less than 500 MHz	LA24: pull-up (R222: 3.3V; R224: DNI)
	1	Core 0 clock frequency is greater than or equal to 500 MHz (default)	

Core 1 Speed

Functional Signals	Value (Binary)	Meaning	APP Inplementation
LA25 Default (1)	0	Core 1 clock frequency is less than 500 MHz	LA25: pull-up (R244: 3.3V; R245: DNI)
	1	Core 1 clock frequency is greater than or equal to 500 MHz (default)	

DDR Speed

Functional Signals	Value (Binary)	Meaning	APP Inplementation
LA26 Default (1)	0	DDR data rate is less than 500 MHz	LA26: pull-up (R242: 3.3V; R243: DNI)
	1	DDR data rate is greater than or equal to 500 MHz (default)	

Appendix - B