

DATE	REVISION NUMBER	INITIALS	DESCRIPTION
12/10/09	ETB-000155-010	Izhou	INITIAL REVISION
06/03/10	ETB-000155-210	FEI GAO	All phy chips and FPGA on board

ETB-000155-210


Atheros Arctic PHY Demo Board
AR8031/AR8033

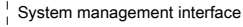
ATHEROS CONFIDENTIAL
PRELIMINARY

Silkscreen on Board:

AR5BEU-08031A rev.010

AR5BEU-08033A rev.010

 Atheros Communications, Inc. 5480 Great America Parkway Santa Clara, CA 95054				Title Title and Rev					
Date	Friday, September 10, 2010	Size	C	Rev	1.0	Sheet	1 of 10	DWG NO	ETB-000155-210



Clock Option:

For all modes except RMII mode 1

- (1) 25MHz crystal with two 22pF Caps;
(2) external 1.2V 25MHz clock input through XTLI; XTLO NC;

For RMII mode 1

- (3) external 50MHz clock input through XTLO;
XTLI use 0.1uF decouple Cap.

Fiber mode SFP connector

Power-on Strapping Pins

MODE2[3:0]

(Default assemble: 0000)

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1100 BaseT, RMI1;
1101 BaseT, RMI2;
1110 100X, RGMII, 75OHMS;
1111 100X, TRANS, 75OHMS;
0000 BaseT, RGMII;
0001 BaseT, SGMI;
0010 1000X, RGMII, 50OHMS;
0011 1000X, RGMII, 75OHMS;
0100 1000X, TRANS, 50OHMS;
0101 1000X, TRANS, 75OHMS;
0110 100X, RGMII, 50OHMS;
0111 100X, TRANS, 50OHMS;
Others Reserved

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