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MODULE decoder

//ma U4F.abl
//Tom Stoll, 4/11/00

//Intended for IOC555 Rev. X.X.X (F)
//Target Reference Designator: U4

//Revisions:
//Rev. A: Original Version                                   4/11/00
//Rev. B: Change name for new conventions                    6/20/00
//Rev. C: New memory Map                                     10/19/00
//Rev. D: Changes for Rev. E: no NVRAM, new DAC's,           10/19/00
//               add Reset Config Word Enable
//Rev. E: Changes for Rev. F I/O card: new 7396 DAC's        03/12/01
//Rev. F: Changes for Rev. F I/O card: use 7247 DAC's        03/21/01
//Rev. G: Changes for Rev. G I/O card: remove AO signals     11/30/01

Declarations

//INPUTS

        A12,A13,A14,A22,A23,A28,A29,A30      pin 40,41,42,43,44,1,2,3;
        CS0,CS2,CS3                          pin 27,8,9;
        RW                                   pin 5;

//OUTPUTS

        DPRAM A, SEM A, DPRAM B, SEM B    pin 10,11,12,13        istype 'com';
//C     NVRAM                            pin 14                 istype 'com';
        AI START, AI READ, AI OE, AI FLAGCLR  pin 15,18,19,20   istype 'com';
//C     AO0, AO1, AO2, AO3, AO4, AO5     pin 21,23,24,30,31,33  istype 'com';
//C     WR01, WR23, WR45                 pin 22,25,32           istype 'com';
//D     DAC1, DAC2, DAC3, DAC A0         pin 22,24,30,32        istype 'com';
//E     nDAC1, nDAC3, nDAC5              pin 21,24,31           istype 'com';
//F     nDAC1, nDAC2, nDAC3              pin 21,22,24           istype 'com';
//F     nDAC4, nDAC5, nDAC6              pin 25,31,32           istype 'com';
//F     DAC12, DAC34, DAC56             pin 23,30,33            istype 'com';
        READRESET                        pin 14                 istype 'com';
        LATCH, LATCH2, RTCLK             pin 34,37,36           istype 'com';
        XOE                              pin 35                 istype 'com';


//INTERNAL NODES

        first,second,third,forth,thirdfourth    node;
        fifth,sixth,seventh,eighth              node;
        io cs3,an in,an out,misc1,misc2         node;
//F     ao1,ao2,ao3,ao4,ao5,ao6                 node;

        H,L,X           = 1,0,.X.;
        MEM ADDR        = [A12,A13,A14];
        IO ADDR         = [A22,A23];
        NUMBER          = [A28,A29,A30];

Equations

//NODE EQUATIONS

        first           = NUMBER == [L,L,L];
        second          = NUMBER == [L,L,H];
        third           = NUMBER == [L,H,L];
        forth           = NUMBER == [L,H,H];
        fifth           = NUMBER == [H,L,L];
        sixth           = NUMBER == [H,L,H];
        seventh         = NUMBER == [H,H,L];

        thirdfourth     = NUMBER == [L,H,X];

        io_cs3          = (MEM_ADDR == [L,L,L]) & !CS3;

        an in           = (IO ADDR == [L,L]) & io cs3;
        an out          = (IO ADDR == [L,H]) & io cs3 & !RW;
        misc1           = (IO ADDR == [H,L]) & io cs3;
        misc2           = (IO_ADDR == [H,H]) & io_cs3;

//E     ao1             = an out & first;
//E     ao2             = an out & second;
//E     ao3             = an out & third;
//E     ao4             = an out & forth;
//E     ao5             = an out & fifth;
//E     ao6             = an_out & sixth;

//B     an in           = (MEM ADDR == [L,L,L]) & (IO ADDR == [L,L]) & !CS3;
//B     an out          = (MEM ADDR == [L,L,L]) & (IO ADDR == [L,H]) & !CS3 & !RW;
//B     misc1           = (MEM_ADDR == [L,L,L]) & (IO_ADDR == [H,L]) & !CS3;

//OUTPUT EQUATIONS

        !DPRAM_A        = (MEM_ADDR == [L,L,L]) & !CS2;
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        !SEM A           = (MEM ADDR == [L,L,H]) & !CS2;
        !DPRAM B         = (MEM ADDR == [L,H,L]) & !CS2;
        !SEM_B           = (MEM_ADDR == [L,H,H]) & !CS2;

//B     !RTCLK           = (MEM ADDR == [H,L,H]) & !CS3;
//B     !NVRAM           = (MEM ADDR == [H,L,L]) & !CS3;

        !RTCLK           = (MEM ADDR == [L,L,H]) & !CS3;
//C     !NVRAM           = (MEM ADDR == [L,H,L]) & !CS3;


        AI START         = an in & first;
        AI READ          = !AI OE;
        !AI OE           = an in & third;
        AI_FLAGCLR       = an_in & forth;

//C     !AO0             = an out & first;
//C     !AO1             = an out & second;
//C     !AO2             = an out & third;
//C     !AO3             = an out & forth;
//C     !AO4             = an out & fifth;
//C     !AO5             = an_out & sixth;

//C     WR01             = AO0 !$ AO1;
//C     WR23             = AO2 !$ AO3;
//C     WR45             = AO4 !$ AO5;

//D     DAC1             = ao1 !$ ao2;
//D     DAC2             = ao3 !$ ao4;
//D     DAC3             = ao5 !$ ao6;
//D     DAC_A0           = (IO_ADDR == [L,H]) & io_cs3 & A30;

//E     nDAC1            = ao1 !$ ao2;
//E     nDAC3            = ao3 !$ ao4;
//E     nDAC5            = ao5 !$ ao6;

//E     DAC12            = an out & !A30;
//E     DAC34            = an out & !A30;
//E     DAC56            = an_out & !A30;

//F     !nDAC1           = an out & first;
//F     !nDAC2           = an out & second;
//F     !nDAC3           = an out & third;
//F     !nDAC4           = an out & forth;
//F     !nDAC5           = an out & fifth;
//F     !nDAC6           = an_out & sixth;

//F     DAC12            = nDAC1 !$ nDAC2;
//F     DAC34            = nDAC3 !$ nDAC4;
//F     DAC56            = nDAC5 !$ nDAC6;

        !LATCH           = misc1 & first;
        !LATCH2          = misc2 & first;
        !READRESET       = misc2 & thirdfourth;
//B     !LATCH2          = misc & seventh;

        XOE              = CS0 & !an out & !misc1 & !misc2 & RTCLK & AI OE;
//B     XOE              = CS0 & !an out & !misc1         & RTCLK & AI OE;
//B     XOE              = CS0 & AO0 & AO1 & AO2 & AO3 & AO4 & AO5 & LATCH & LATCH2 & RTCLK & AI_OE;


        END
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