

FEATURES 1M x 16 MRAM

- +3.3 Volt power supply
- Fast 35 ns read/write cycle
- SRAM compatible timing
- Unlimited read & write endurance
- Data always non-volatile for >20-years at temperature
- RoHS-compliant small footprint BGA and TSOP package

### **BENEFITS**

- One memory replaces FLASH, SRAM, EEPROM and BBSRAM in systems for simpler, more efficient designs
- Improves reliability by replacing battery-backed SRAM





## **INTRODUCTION**

The MR4A16B is a 16,777,216-bit magnetoresistive random access memory (MRAM) device organized as 1,048,576 words of 16 bits. The MR4A16B offers SRAM compatible 35 ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The MR4A16B is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

The MR4A16B is available in small footprint 48-pin ball grid array (BGA) package and a 54-pin thin small outline package (TSOPII). These packages are compatible with similar low-power SRAM products and other nonvolatile RAM products.

The MR4A16B provides highly reliable data storage over a wide range of temperatures. The product is offered with commercial temperature (0 to +70 °C), industrial temperature (-40 to +85 °C), and automotive temperature (-40 to +125 °C) range options.

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# 1. DEVICE PIN ASSIGNMENT

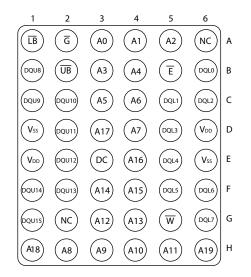
OUTPUT  $\overline{\mathsf{G}}$ UPPER BYTE OUTPUT ENABLE **ENABLE BUFFER** LOWER BYTE OUTPUT ENABLE 10, UPPER A[19:0] **ADDRESS** 8/ BYTE **BUFFER** 10 ROW COLUMN OUTPUT DECODER DECODER 8 BUFFER SENSE CHIP Ē LOWER **AMPS** 8 **ENABLE** 16/ BYTE 8 **BUFFER** OUTPUT 1M x 16 BUFFER BIT UPPER **MEMORY** WRITE BYTE **-**DQU[15:8]  $\overline{\mathsf{W}}$ ARRAY WRITE **ENABLE** DRIVER FINAL **BUFFER** 16 WRITE 8 LOWER **DRIVERS** BYTE DQL[7:0] WRITE DRIVER UB UB UPPER BYTE WRITE ENABLE BYTE **ENABLE** LB  $\overline{\mathsf{LB}}$ **BUFFER** LOWER BYTE WRITE ENABLE

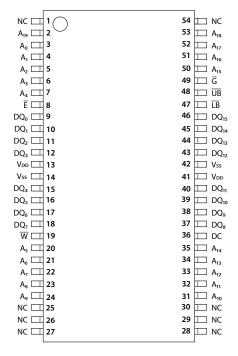
**Figure 1.1 Block Diagram** 

**Table 1.1 Pin Functions** 

Signal Name	Function
А	Address Input
Ē	Chip Enable
$\overline{w}$	Write Enable
G	Output Enable
ŪB	Upper Byte Enable
LB	Lower Byte Enable
DQ	Data I/O
V <sub>DD</sub>	Power Supply
V <sub>ss</sub>	Ground
DC	Do Not Connect
NC	No Connection

Figure 1.2 Pin Diagrams for Available Packages (Top View)





48-Pin BGA

54-Pin TSOP

**Table 1.2 Operating Modes** 

ǹ	<b>G</b> ¹	$\overline{\mathbf{W}}^{1}$	LB <sup>1</sup>	ŪB¹	Mode	V <sub>DD</sub> Current	DQL[7:0] <sup>2</sup>	DQU[15:8] <sup>2</sup>
Н	Х	Х	Х	Х	Not selected	<sub>SB1</sub> ,   <sub>SB2</sub>	Hi-Z	Hi-Z
L	Н	Н	Х	Х	Output disabled	l <sub>DDR</sub>	Hi-Z	Hi-Z
L	Х	Х	Н	Н	Output disabled	l <sub>DDR</sub>	Hi-Z	Hi-Z
L	L	Н	L	Н	Lower Byte Read	l <sub>DDR</sub>	$D_Out$	Hi-Z
L	L	Н	Н	L	Upper Byte Read	l <sub>DDR</sub>	Hi-Z	D <sub>Out</sub>
L	L	Н	L	L	Word Read	l <sub>DDR</sub>	$D_Out$	D <sub>Out</sub>
L	Х	L	L	Н	Lower Byte Write	I <sub>DDW</sub>	$D_{in}$	Hi-Z
L	Х	L	Н	L	Upper Byte Write	I <sub>DDW</sub>	Hi-Z	D <sub>in</sub>
L	Х	L	L	L	Word Write	I <sub>DDW</sub>	D <sub>in</sub>	D <sub>in</sub>

 $<sup>^{1}</sup>$  H = high, L = low, X = don't care

<sup>&</sup>lt;sup>2</sup> Hi-Z = high impedance

## 2. ELECTRICAL SPECIFICATIONS

## **Absolute Maximum Ratings**

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field greater than the maximum field intensity specified in the maximum ratings.

Table 2.1	Absolute	Maximum	Ratings <sup>1</sup>
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Parameter	Symbol	Value	Unit
Supply voltage <sup>2</sup>	V <sub>DD</sub>	-0.5 to 4.0	V
Voltage on an pin²	V <sub>IN</sub>	$-0.5 \text{ to V}_{DD} + 0.5$	V
Output current per pin	I <sub>OUT</sub>	±20	mA
Package power dissipation	$P_{D}$	0.600	W
Temperature under bias MR4A16B (Commercial) MR4A16BC (Industrial) MR4A16BM (Automotive)	T <sub>BIAS</sub>	-10 to 85 -45 to 95 -45 to 130	°C
Storage Temperature	T <sub>stg</sub>	-55 to 150	°C
Lead temperature during solder (3 minute max)	$T_{Lead}$	260	°C
Maximum magnetic field during write MR4A16B (All Temperatures)	H <sub>max_write</sub>	2000	A/m
Maximum magnetic field during read or standby	H <sub>max_read</sub>	8000	A/m

<sup>&</sup>lt;sup>1</sup> Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

<sup>&</sup>lt;sup>2</sup> All voltages are referenced to  $V_{SS}$ . The DC value of  $V_{IN}$  must not exceed actual applied  $V_{DD}$  by more than 0.5V. The AC value of  $V_{IN}$  must not exceed applied  $V_{DD}$  by more than 2V for 10ns with  $I_{IN}$  limited to less than 20mA.

<sup>&</sup>lt;sup>3</sup> Power dissipation capability depends on package characteristics and use environment.

Parameter	Symbol	Min	Typical	Max	Unit
Power supply voltage	V <sub>DD</sub>	3.0 i	3.3	3.6	V
Write inhibit voltage	V <sub>wi</sub>	2.5	2.7	3.0 i	V
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>DD</sub> + 0.3 <sup>ii</sup>	V
Input low voltage	V <sub>IL</sub>	-0.5 <sup>iii</sup>	-	0.8	V
Temperature under bias MR4A16B (Commercial) MR4A16BC (Industrial) MR4A16BM (Automotive)	T <sub>A</sub>	0 -40 -40		70 85 125	°C

**Table 2.2 Operating Conditions** 

## **Power Up and Power Down Sequencing**

MRAM is protected from write operations whenever  $V_{DD}$  is less than  $V_{WI}$ . As soon as  $V_{DD}$  exceeds  $V_{DD}$  (min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The  $\overline{E}$  and  $\overline{W}$  control signals should track  $V_{DD}$  on power up to  $V_{DD}^-$  0.2 V or  $V_{IH}$  (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives  $\overline{E}$  and  $\overline{W}$  should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where  $V_{DD}$  goes below  $V_{WI}$ , writes are protected and a startup time must be observed when power returns above  $V_{DD}$  (min).

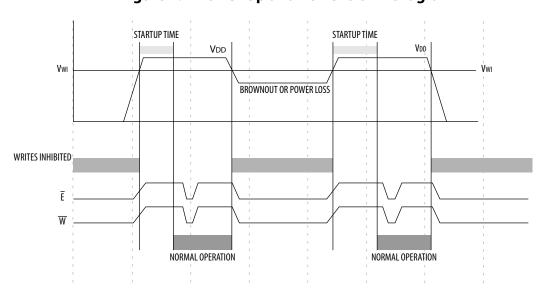


Figure 2.1 Power Up and Power Down Diagram

<sup>&</sup>lt;sup>1</sup> There is a 2 ms startup time once  $V_{DD}$  exceeds  $V_{DD}$  (max). See **Power Up and Power Down Sequencing** below.

<sup>&</sup>quot;  $V_{IH}(max) = V_{DD} + 0.3 V_{DC}$ ;  $V_{IH}(max) = V_{DD} + 2.0 V_{AC}$  (pulse width ≤ 10 ns) for I ≤ 20.0 mA.

 $V_{\parallel}$  (min) = -0.5  $V_{DC}$ ;  $V_{\parallel}$  (min) = -2.0  $V_{AC}$  (pulse width ≤ 10 ns) for I ≤ 20.0 mA.

**Table 2.3 DC Characteristics** 

Parameter	Symbol	Min	Typical	Max	Unit
Input leakage current	l <sub>lkg(I)</sub>	-	-	±1	μΑ
Output leakage current	I <sub>Ikg(O)</sub>	-	-	±1	μΑ
Output low voltage $(I_{OL} = +4 \text{ mA})$ $(I_{OL} = +100 \mu\text{A})$	V <sub>OL</sub>	-	-	0.4 V <sub>ss</sub> + 0.2	V
Output high voltage $(I_{OH} = -4 \text{ mA})$ $(I_{OH} = -100 \mu\text{A})$	V <sub>OH</sub>	2.4 V <sub>DD</sub> - 0.2	-	-	V

**Table 2.4 Power Supply Characteristics** 

Parameter	Symbol	Typical	Max	Unit
AC active supply current - read modes <sup>1</sup> (I <sub>OUT</sub> = 0 mA, V <sub>DD</sub> = max)	I <sub>DDR</sub>	60	TBD	mA
AC active supply current - write modes <sup>1</sup> (V <sub>DD</sub> = max) MR4A16B (Commercial) MR4A16BC (Industrial) MR4A16BV (Extended)	I <sub>DDW</sub>	110 110 110	TBD TBD TBD	mA
AC standby current $(V_{DD} = max, \overline{E} = V_{H})$ no other restrictions on other inputs	I <sub>SB1</sub>	11	14	mA
CMOS standby current $(\overline{E} \ge V_{DD} - 0.2 \text{ V and } V_{In} \le V_{SS} + 0.2 \text{ V or } \ge V_{DD} - 0.2 \text{ V})$ $(V_{DD} = \text{max, } f = 0 \text{ MHz})$	I <sub>SB2</sub>	7	9	mA

<sup>&</sup>lt;sup>1</sup> All active current measurements are measured with one address transition per cycle and at minimum cycle time.

## 3. TIMING SPECIFICATIONS

Table 3.1 Capacitance<sup>1</sup>

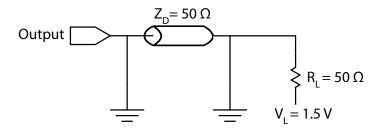
Parameter	Symbol	Typical	Max	Unit
Address input capacitance	C <sub>In</sub>	-	6	pF
Control input capacitance	C <sub>In</sub>	-	6	pF
Input/Output capacitance	C <sub>I/O</sub>	-	8	pF

 $<sup>^1~</sup>$  f = 1.0 MHz, dV = 3.0 V,  $\rm T_A$  = 25 °C, periodically sampled rather than 100% tested.

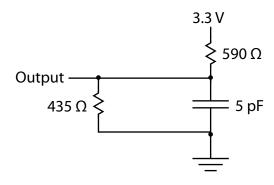
**Table 3.2 AC Measurement Conditions** 

Parameter	Value	Unit
Logic input timing measurement reference level	1.5	V
Logic output timing measurement reference level	1.5	٧
Logic input pulse levels	0 or 3.0	V
Input rise/fall time	2	ns
Output load for low and high impedance parameters	See Figure	3.1
Output load for all other timing parameters	See Figure	3.2

Figure 3.1 Output Load Test Low and High



**Figure 3.2 Output Load Test All Others** 



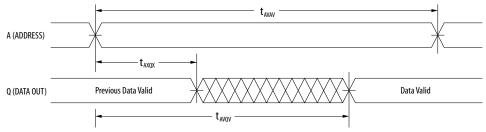
### **Read Mode**

Table 3.3 Read Cycle Timing<sup>1</sup>

Parameter	Symbol	Min	Max	Unit
Read cycle time	t <sub>AVAV</sub>	35	-	ns
Address access time	t	-	35	ns
Enable access time <sup>2</sup>	t	-	35	ns
Output enable access time	t <sub>GLQV</sub>	-	15	ns
Byte enable access time	t <sub>BLQV</sub>	-	15	ns
Output hold from address change	t	3	-	ns
Enable low to output active <sup>3</sup>	t <sub>ELQX</sub>	3	-	ns
Output enable low to output active <sup>3</sup>	t <sub>GLQX</sub>	0	-	ns
Byte enable low to output active <sup>3</sup>	t <sub>BLQX</sub>	0	-	ns
Enable high to output Hi-Z³	t <sub>EHQZ</sub>	0	15	ns
Output enable high to output Hi-Z³	t <sub>GHQZ</sub>	0	10	ns
Byte high to output Hi-Z <sup>3</sup>	t <sub>BHQZ</sub>	0	10	ns

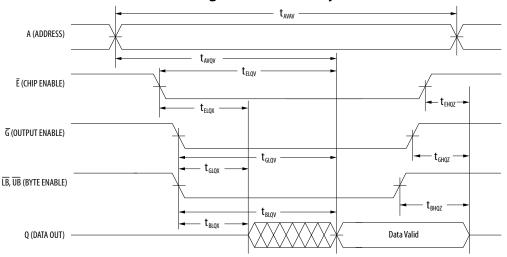
 $<sup>\</sup>overline{W}$  is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.

## Figure 3.3A Read Cycle 1



Note: Device is continuously selected ( $\overline{E} \le V_{||}$ ,  $\overline{G} \le V_{||}$ ).

## Figure 3.3B Read Cycle 2



<sup>&</sup>lt;sup>2</sup> Addresses valid before or at the same time  $\overline{E}$  goes low.

 $<sup>^3</sup>$  This parameter is sampled and not 100% tested. Transition is measured  $\pm 200$  mV from the steady-state voltage.

Table 3.4 Write Cycle Timing 1 (W Controlled)1

Table 5.4 Write Cycle Tilling 1 (W Controlled)							
Parameter	Symbol	Min	Max	Unit			
Write cycle time <sup>2</sup>	t <sub>AVAV</sub>	35	-	ns			
Address set-up time	t <sub>AVWL</sub>	0	-	ns			
Address valid to end of write ( $\overline{G}$ high)	t <sub>avwh</sub>	20	-	ns			
Address valid to end of write $(\overline{\overline{G}} \text{ low})$	t <sub>AVWH</sub>	20	-	ns			
Write pulse width ( $\overline{G}$ high)	t <sub>wlwh</sub> t <sub>wleh</sub>	15	-	ns			
Write pulse width ( $\overline{G}$ low)	t <sub>wlwh</sub> t <sub>wleh</sub>	15	-	ns			
Data valid to end of write	t <sub>DVWH</sub>	10	-	ns			
Data hold time	t <sub>whDX</sub>	0	-	ns			
Write low to data Hi-Z <sup>3</sup>	t <sub>wLQZ</sub>	0	15	ns			
Write high to output active <sup>3</sup>	t <sub>whQX</sub>	3	-	ns			
Write recovery time	t <sub>whax</sub>	12	-	ns			

All write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If  $\overline{G}$  goes low at the same time or after  $\overline{W}$  goes low, the output will remain in a high impedance state. After  $\overline{W}$ ,  $\overline{E}$  or  $\overline{UB}/\overline{LB}$  has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between  $\overline{E}$  being asserted low in one cycle to  $\overline{E}$  being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

- <sup>2</sup> All write cycle timings are referenced from the last valid address to the first transition address.
- This parameter is sampled and not 100% tested. Transition is measured  $\pm 200$  mV from the steady-state voltage. At any given voltage or temperate,  $t_{WLOZ}(max) < t_{WHOX}(min)$

Tanyon

A (ADDRESS)

Town

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Town

Data Valid

Town

Data Valid

Hi -Z

Hi -Z

Figure 3.4 Write Cycle Timing 1 (W Controlled)

Table 3.5 Write Cycle Timing 2 (E Controlled)<sup>1</sup>

Parameter	Symbol	Min	Max	Unit
Write cycle time <sup>2</sup>	t <sub>AVAV</sub>	35	-	ns
Address set-up time	t <sub>AVEL</sub>	0	-	ns
Address valid to end of write $(\overline{G} \text{ high})$	t <sub>AVEH</sub>	20	-	ns
Address valid to end of write (G low)	t <sub>AVEH</sub>	20	-	ns
Enable to end of write $(\overline{G} \text{ high})$	t <sub>ELEH</sub> t <sub>ELWH</sub>	15	-	ns
Enable to end of write $(\overline{G} \text{ low})^3$	t <sub>ELEH</sub>	15	-	ns
Data valid to end of write	t <sub>DVEH</sub>	10	-	ns
Data hold time	t <sub>ehdx</sub>	0	-	ns
Write recovery time	t <sub>EHAX</sub>	12	-	ns

All write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If  $\overline{G}$  goes low at the same time or after  $\overline{W}$  goes low, the output will remain in a high impedance state. After  $\overline{W}$ ,  $\overline{E}$  or  $\overline{UB}$ /  $\overline{LB}$  has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between  $\overline{E}$  being asserted low in one cycle to  $\overline{E}$  being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

- <sup>2</sup> All write cycle timings are referenced from the last valid address to the first transition address.
- If  $\overline{E}$  goes low at the same time or after  $\overline{W}$  goes low, the output will remain in a high-impedance state. If  $\overline{E}$  goes high at the same time or before  $\overline{W}$  goes high, the output will remain in a high-impedance state.

Figure 3.5 Write Cycle Timing 2 (E Controlled)<sup>1</sup>

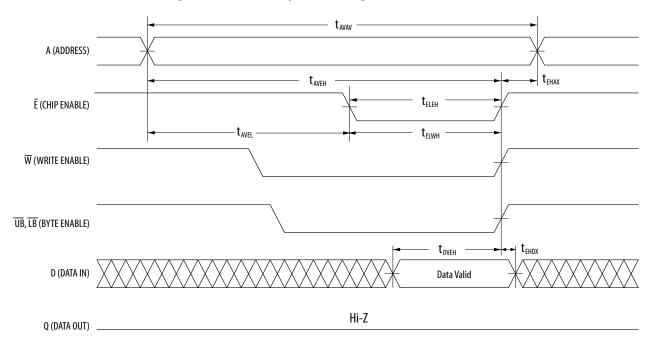
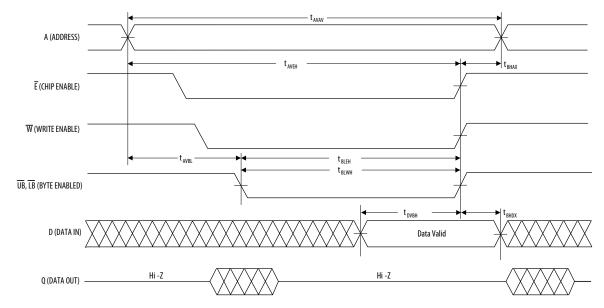


Table 3.6 Write Cycle Timing 3 (LB/UB Controlled)<sup>1</sup>

Parameter	Symbol	Min	Max	Unit
Write cycle time <sup>2</sup>	t <sub>avav</sub>	35	-	ns
Address set-up time	t <sub>AVBL</sub>	0	-	ns
Address valid to end of write ( $\overline{G}$ high)	t <sub>avbh</sub>	20	-	ns
Address valid to end of write $(\overline{G} \text{ low})$	t <sub>avbh</sub>	20	-	ns
Write pulse width ( $\overline{G}$ high)	t <sub>BLEH</sub> t <sub>BLWH</sub>	15	-	ns
Write pulse width (G low)	t <sub>BLEH</sub>	15	-	ns
Data valid to end of write	t <sub>DVBH</sub>	10	-	ns
Data hold time	t <sub>BHDX</sub>	0	-	ns
Write recovery time	t <sub>BHAX</sub>	12	-	ns

All write occurs during the overlap of  $\overline{E}$  low and  $\overline{W}$  low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If  $\overline{G}$  goes low at the same time or after  $\overline{W}$  goes low, the output will remain in a high impedance state. After  $\overline{W}$ ,  $\overline{E}$  or  $\overline{UB}/\overline{LB}$  has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them. The minimum time between  $\overline{E}$  being asserted low in one cycle to  $\overline{E}$  being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.





<sup>&</sup>lt;sup>2</sup> All write cycle timings are referenced from the last valid address to the first transition address.

# **4. ORDERING INFORMATION**

**Figure 4.1 Part Numbering System** 

MR	4	Α	16	В	C	MA	35	R		
									Carrier	Blank = Tray, R = Tape & Reel
									Speed	35 ns
									Package	MA = FBGA, YS = TSOP
									Temperature Range	Blank= 0 to +70 °C, C= -40 to +85 °C, M= -40 to +125 °C
									Revision	
									Data Width	16 = 16-bit
									Туре	A = Asynchronous
									Density	4=16Mb
									Magnetoresistive RAN	Л

**Table 4.1 Available Parts** 

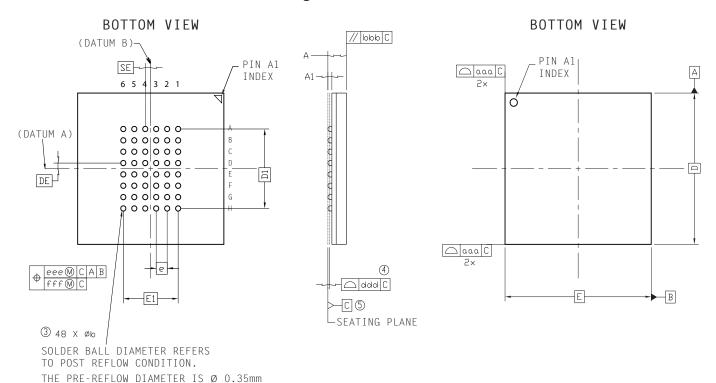
Part Number	Description	Temperature
MR4A16BMA35 <sup>1</sup>	3.3 V 1Mx16 MRAM 48-BGA	Commercial
MR4A16BCMA35 <sup>1</sup>	3.3 V 1Mx16 MRAM 48-BGA	Industrial
MR4A16BMMA35 <sup>1</sup>	3.3 V 1Mx16 MRAM 48-BGA	Automotive
MR4A16BYS35 <sup>1</sup>	3.3 V 1Mx16 MRAM 54-TSOP	Commercial
MR4A16BCYS35 <sup>1</sup>	3.3 V 1Mx16 MRAM 54-TSOP	Industrial
MR4A16BMYS35 <sup>1</sup>	3.3 V 1Mx16 MRAM 54-TSOP	Automotive

Note 1: These products are classified as Preliminary, a product in development and/or qualification that has fixed target specifications that are subject to change pending characterization results.

Document Number: MR4A16B Rev. 4, 3/2010

# 5. MECHANICAL DRAWING

## Figure 5.1 48-FBGA



Ref	Min	Nominal	Max	
Α	1.19	1.27	1.35	
A1	0.22	0.27	0.32	
b	0.31	0.36	0.41	
D	10.00 BSC			
E	10.00 BSC			
D1	5.25 BSC			
E1	3.75 BSC			
DE	0.375 BSC			
SE	0.375 BSC			
е	0.75 BSC			

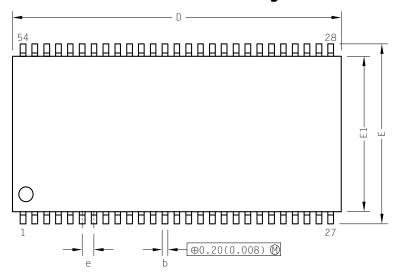
Ref	Tolerance of, from and position
aaa	0.10
bbb	0.10
ddd	0.12
eee	0.15
fff	0.08

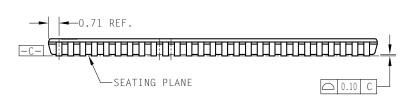
#### **Print Version Not To Scale**

- 1. Dimensions in Millimeters.
- 2. The 'e' represents the basic solder ball grid pitch.
- (3) 'b' is measurable at the maximum solder ball diameter in a plane parallel to datum C.
- 4) Dimension 'ccc' is measured parallel to primary datum C.
- 5 Primary datum C (seating plane) is defined by the crowns of the solder balls.
- 6. Package dimensions refer to JEDEC MO-205 Rev. G.

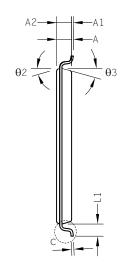
# **5. MECHANICAL DRAWING**

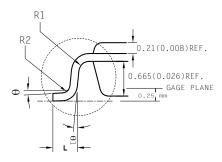
## Figure 5.2 54-TSOP





Ref	Min	Nominal	Max	
Α			1.20	
A1	0.05	0.10	0.15	
A2	0.95	1.00	1.05	
b	0.30	0.35	0.45	
С	0.12		0.21	
D	22.10	22.22	22.35	
Е	11.56	11.76	11.95	
E1	10.03	10.16	10.29	
е	0.80 BSC			
L	0.40	0.50	0.60	
L1		0.80 REF		
R1	0.12	-	-	
R2	0.12	-	0.25	
θ	0°	-	8°	
θ1	0.40	-	-	
θ2	15° REF			
θ3	15° REF			





#### **Print Version Not To Scale**

- 1. Dimensions in Millimeters.
- 2. Package dimensions refer to JEDEC MS-024

#### 6. REVISION HISTORY

Revision	Date	Description of Change	
1	May 29, 2009	Establish Speed and Power Specifications	
2	July 27, 2009	Increase BGA Package to 11 mm x 11 mm	
3	Nov 26, 2009	Changed ball definition of H6 to A19 and G2 to NC in Figure 1.2.	
4	Mar 10, 2010	Changed speed marking and timing specs to 35 ns part. Changed BGA package to 10 mm x 10mm	
5	Apr 7, 2010	Added 54-TSOP package options.	

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