Application Note 102

Avoiding Bus Contention on Configuration

KS8993, KS8995E, KS8997, KS8999

General Description

When programming configuration pins with an FPGA, the following recommendations can minimize bus contention.

These recommendations apply to the KS8993, KS8995E, KS8997, and KS8999 and are referred to as KS899x in this application note.

Scenario

A reset is applied to the KS899x. Shortly after the reset is de-asserted, the KS899x latches strap-in values on the configuration pins as shown in Figure 1.
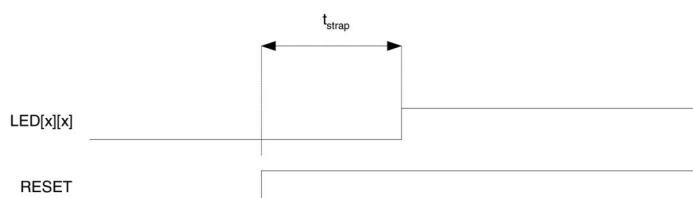

Figure 1. KS899x Strap-In Window

Then the KS899x begins normal operation and may begin driving the configuration pins.

Recommendations

There is a possibility of contention if an FPGA is used to drive these pins and its outputs are not tri-stated before the KS899x begins driving signals on the configuration pins.

To ensure proper strap-in and minimize any contention on the configuration pins, an FPGA driving these signals should remain on after the active low reset signal is de-asserted for the duration of the strap-in window, and then be tri-stated immediately.

Recommendations (continued)

The recommended strap-in window is:

Part Number	t_{strap}
KS8993	30 us
KS8995E	50 us
KS8997	50 us
KS8999	50 us

Also recommended is a series resistor between the FPGA output and the KS899x's configuration pin as shown in Figure 2. This helps to limit the current if some contention should still occur due to the limited control of the FPGA outputs.

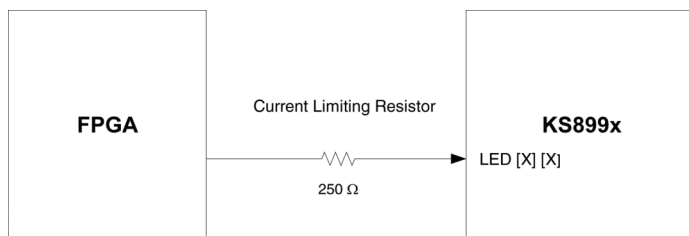For example, a resistor value of 250W would limit a TTL logic high of 2.5V to 10mA.

Figure 2. KS899x Current Limiting Resistor

Please contact your local Micrel FAE or salesperson if you have any questions.

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