Atheros AR8031 AR8033

Design Guide

Version 1.00

28 March 2011

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Revision History

Date	Rev	Description	Author
Mar 28, 2011	1.00	Draft release	Nick Yin

1. Introduction

The AR8031/8033 is part of the Arctic family of Ethernet physical transceiver devices which includes the AR8031, AR8033, AR8030 and AR8035. It is Atheros' 4th generation, single port 10/100/1000 Mbps Tri-speed Ethernet PHY. It supports RGMII/SGMII interface connects to the MAC.

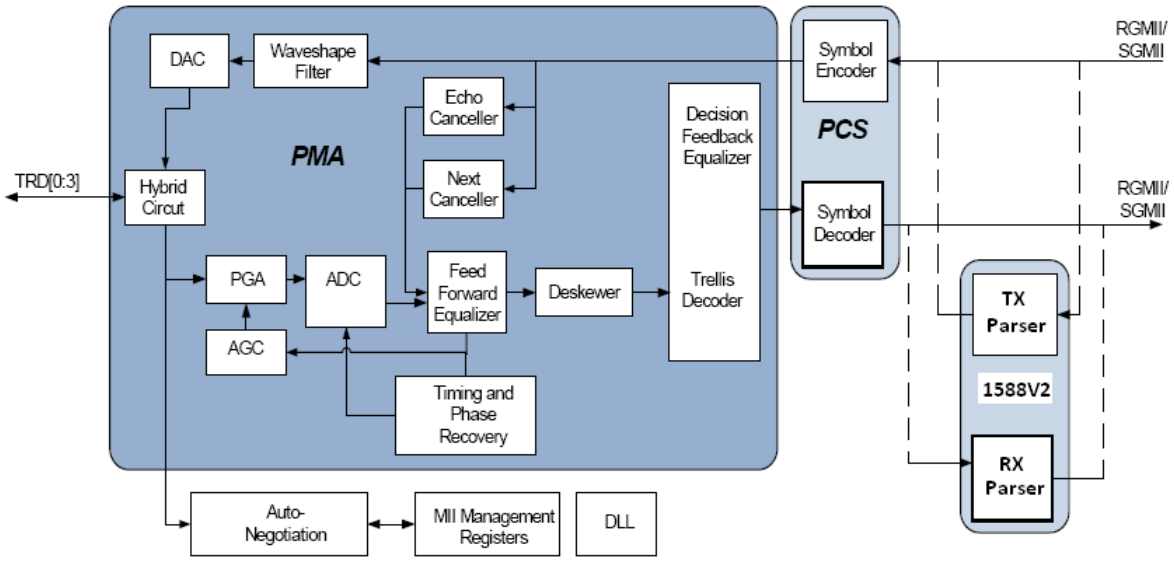
1.1 Features

- 10/100/1000BASE-T IEEE 802.3 compliant
- Supports 1000BASE-T PCS and auto-negotiation with next page support
- Supports 3.3V, 2.5V, 1.8V and 1.5V RGMII interface to MAC devices
- Supports RGMII/SGMII interfaces to MAC devices
- Supports Fiber and Copper combo mode when MAC interface works in RGMII mode
- Supports additional IEEE 1000BASE-X and 100BASE-FX with Integrated Serdes
- Supports 1000M/100M copper to fiber converter mode
- Supports Synchronous Ethernet with selectable recovered clock output
- AR8031 supports 1588v2
- Supports Wake-on-LAN (WoL) to detect magic packet and notify the sleeping system to wake up
- Multiple Loopback modes for diagnostics
- Supports Atheros latest Green Ethos™ power saving modes with internal automatic DSP power saving scheme
- Supports 802.3az (Energy Efficient Ethernet)
- Supports SmartEEE
- Fully integrated digital adaptive equalizers, echo cancellers, and near end crosstalk (NEXT) cancellers
- A robust Cable Discharge Event (CDE) tolerance of ±6kV
- A robust surge protection with ±750V/differential mode and ±4KV/common mode
- Jumbo Frame support up to 10KB (full duplex)
- Automatic channel swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- Cable Diagnostic Test (CDT)
- Single power supply: 3.3V
- 6mm x 6mm, 48-pin QFN package

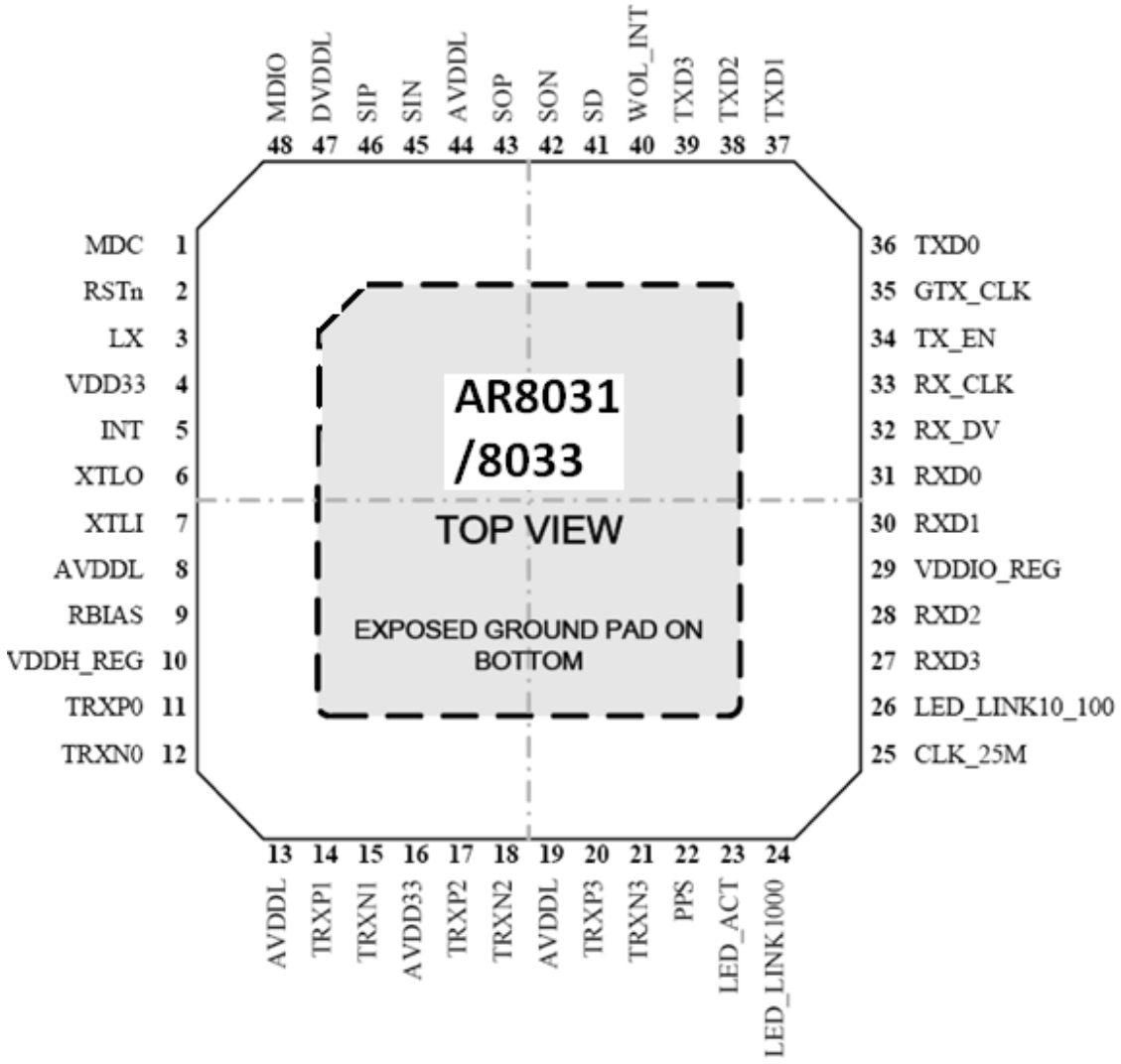
AR8031, AR8033 and AR8035 features comparison

Feature	AR8031	AR8033	AR8035
RGMII	yes	yes	yes
SGMII	yes	yes	
10/100/1000BASE-T	yes	yes	yes
EEE(802.3az)	yes	yes	yes
Smart EEE	yes	yes	yes
Wake-on-LAN	yes	yes	yes
100/1000M SERDES/Fiber	yes	yes	
1588v2	yes		
Sync-E	yes	yes	
Packaging	48-pin	48-pin	40-pin

1.2 Functional Block Diagram



1.3 Pin out diagram



AR8031 and AR8033 are pin-to-pin compatible.
Only difference is AR8033 does not support 1588v2 which AR8031 supports.
PPS is NC and **CLK_25M** is output only in AR8033.
In AR8031 PPS is 1588v2 Pulse Per Second clock output (period 1 second clock signal which is synchronous with internal RTC), CLK_25M can be configured to 1588 reference clock input.

2. Hardware Design Guide

2.1 Power Design

AR8031/8033 only requires single 3.3V power supply.
Inside the chip there are 3.3V rail, 2.5V rail, 1.1V rail and 1.8V/1.5V rail.

2.1.1 Power Rail and Consumption

Symbol	Pin	Description	Total Current (max)	Unit
Input pin				
AVDDL	8,13, 19,44	Analog 1.1V (+/-5%) 0.1uF near each pin; A bead between DVDDL	50.8	mA
DVDDL	47	Digital 1.1V (+/-5%) 10uF+0.1uF close to inductor;0.1uF close to pin	113.7	mA
VDD33	4	Digital 3.3V (+/-5%) 10uF+0.1uF close to pin	70.2	mA
AVDD33	16	Analog 3.3V (+/-5%) 1uF+0.1uF close to pin; A bead between VDD33	63.8	mA
Output pin				
LX	3	Power inductor pin, 4.7uH directly connect to this pin to generate 1.1v(+/-3%) output for AVDDL and DVDDL	164.5	mA
VDDH_REG	10	2.7V (+/-5%) regulator output. When works with 2.5V RGMII I/O, connect this pin to VDDIO_REG to provide 20.9mA I/O current. Add 1uF close to pin. When works with 1.5V/1.8V RGMII I/O, disconnect with VDDIO_REG. Little current appears on the board for pull-up, only need 0.1uF to GND.	20.9	mA
VDDIO_REG	29	1.5V/1.8V (+/-5%) regulator output. When works with 2.5V RGMII I/O, connect VDDH_REG to this pin, add 0.1uF close to pin. If use 1.5V/1.8V RGMII I/O, add 1uF close to pin, little current appears on the board for pull-up.	20.9	mA

Notes: suggest keeping external input power **Ripple** less than **1%** of the power voltage
Noise less than **5%** of the power voltage

AR8031/8033 integrates a switch regulator which converts 3.3V to 1.1V with high efficiency for core power rail.

It is optional for external regulator to provide this core voltage. No special requirement for 1.1V to 3.3V power sequence. After both two power rails are stable, a reliable reset is needed.

AR8031/8033 integrates two on chip LDOs (structure in Figure 1) which can support 2.5V, 1.5V/1.8V RGMII I/O voltage. Also with 2.5V RGMII I/O voltage configuration AR8031/8033 can work with 3.3V MAC RGMII interface. Since the input can bear 3.3V logic signal, and the output logic V_{OH} and V_{OL} can satisfy the 3.3V LVCMOS/LVTTL requirement. The parameter detail is in datasheet electrical characteristics chapter.

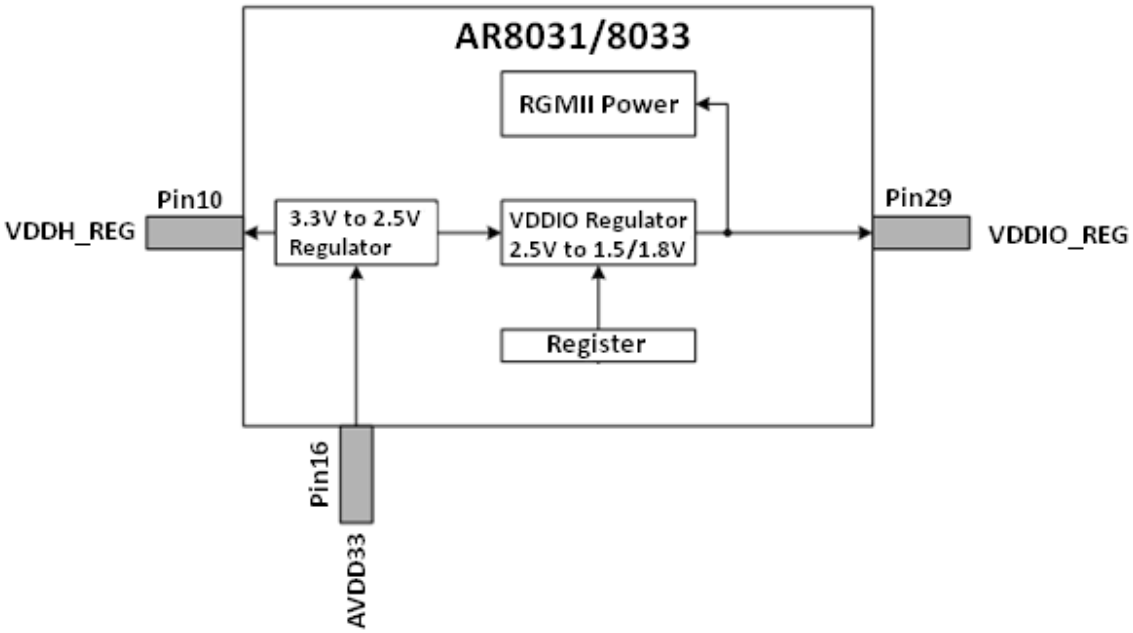


Figure 1. Power Supply Structure

When works in 2.5V RGMII I/O level, need to connect VDDH_REG pin to VDDIO_REG pin. The 2.5V to 1.5V/1.8V regulator can be set to any mode since the output voltage is same as input which causes regulator shutdown.

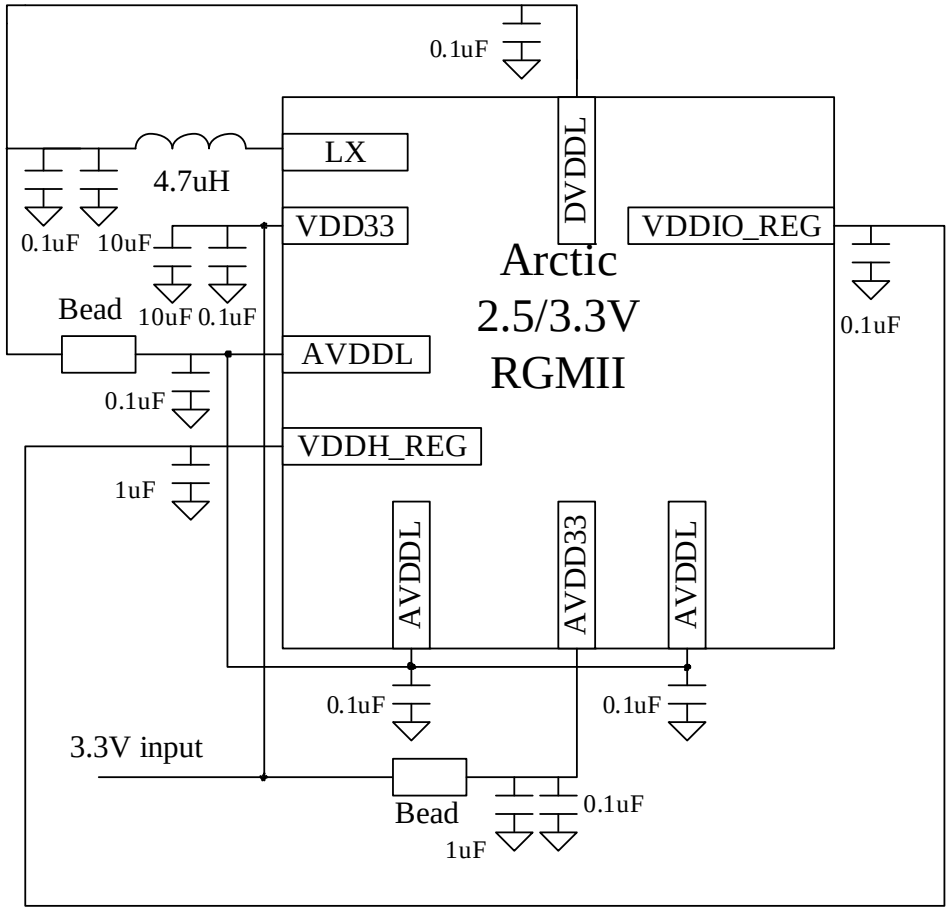


Figure 2. power design with 2.5/3.3V RGMII

When works in 1.5V/1.8V RGMII I/O level, need to disconnect VDDH_REG and VDDIO_REG and set the internal LDO output the right voltage.
The register for 1.5V or 1.8V selection is in debug register 0x1F [3].

Debug register 0x1F definition

Bit	definition	Mode	R/W	Description
3	sel_1p5_lp8 _pos_reg	HW Rst	0	0=1.5v(default) 1=1.8v
		SW Rst	Retain	

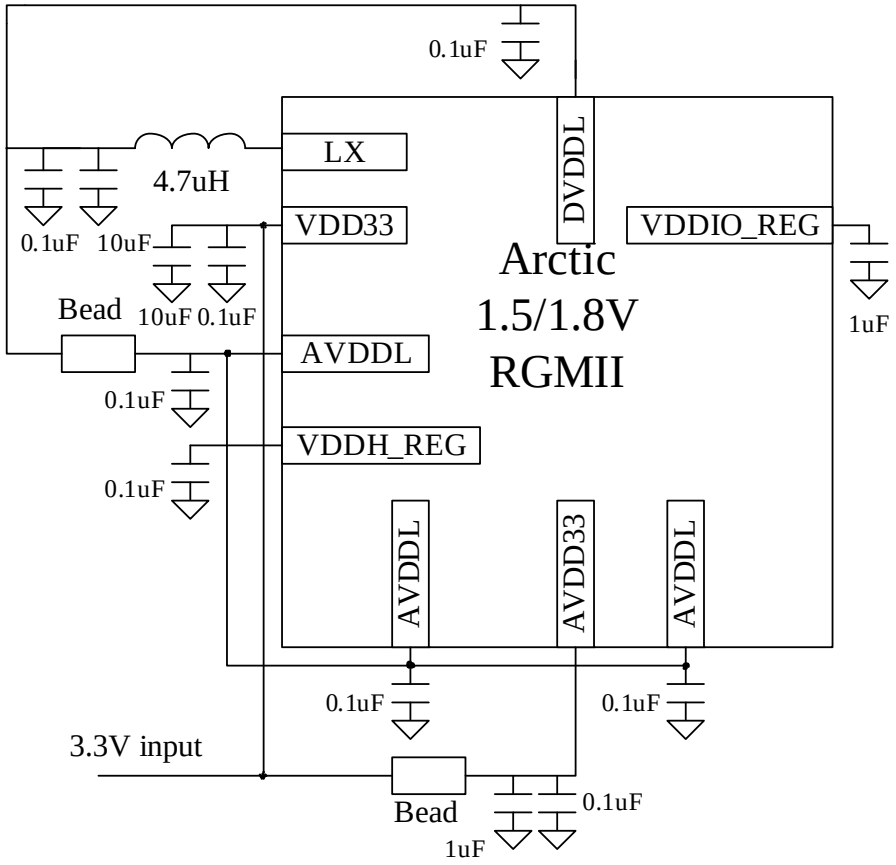


Figure 3. Power design with 1.5V/1.8V RGMII

2.1.2 Component Selection

Inductor Parameters

AR8031/8033 integrates a switch regulator which converts 3.3V to 1.1V with high efficiency. Switching frequency is 1.8MHz.

Need an external 4.7µH inductor directly connect to LX (pin3). Try to put the inductor at the top layer.

Choose an inductor with low DCR will improve the power efficiency. The current parameter of the inductor needs to be larger than 500mA. Prefer 1A.

Demo board inductor parameters for reference:

Inductance(µ H) 100KHz	D.C.R (m Ω) Max.(Typ.) (at20°C)	Saturation Current(A)		Temperature Rise Current(A)
		at 20°C	At 105°C	
4.7+/-30%	116(93)	1.2	0.9	1.5

1. Saturation current: The DC current at which the inductance decreases to 65% of its normal value.
2. Temperature rise current: The DC current at which the temperature rise is 40°C.
3. Package: SMD 4*4*1.8 mm

Bead and Capacitor Parameters

The analog power rail and digital power rail need to be separated by bead.
The power consumption parameters are in table 1, suggest to choose the bead with at least 80% current derating.
AVDDL is from DVDDL through a bead. As the switch regulator output precision is +/-3%, it leaves only 2% margin for layout and bead voltage drop to satisfy the AVDDL -5% demand. So Low ESR<100 m Ω bead is preferred.

To reduce power noise, 0.1uF decoupling capacitors are required for every power pin.
These capacitors should be placed near the related pins.
10uF or 1uF will be needed for large current power rail.
Detail capacitance selection suggestions in table 1 and figure above.

Small package, X5R or X7R, ceramic capacitances are preferred.

2.1.3 Layout Guide

Try to put capacitors near the related pins and on the top layer, save the via between power pin to capacitor to reduce parasite inductance and resistance. Power traces should be wider than 30mil and as short as possible.

*** AR8031/8033 has only one exposed ground pin at the bottom side. This E-pad is the ground reference needs to be connected to the system ground. At the same time, a majority of heat dissipates through this E-pad.
Figure 4 below shows the 3*3 vias to ground which ensure good ground contact and increase heat dissipating.

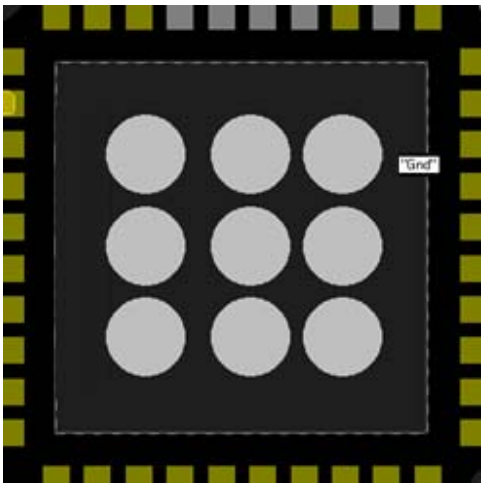


Figure 4. E-pad design

The via dimension is: diameter= 30mil, drill=18mil

The E-pad dimension is: 3.8mm*3.8mm (+/-0.1mm)

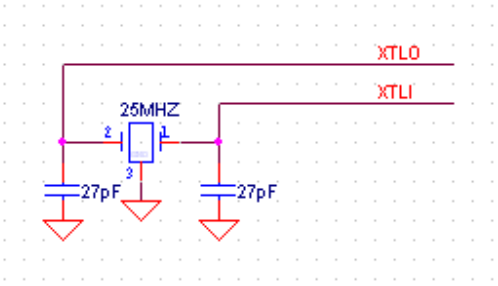
2.2 Clock design

Symbol	Pin	Type	Description
XTLO	6	OA	Crystal oscillator output, 27pf to GND.
XTLI	7	IA	Crystal oscillator input, 27pf to GND. support external 1.2V swing clock input through this pin
CLK_25M	25	I/O	For AR8031: Default 25MHz clock output. This pin can be configured to 50MHz, 62.5MHz or 125MHz output by register. or 1588v2 reference 50MHz ~ 125MHz clock input, register configurable
	25	O	For AR8033: Default 25MHz clock output. This pin can be configured to 50MHz, 62.5MHz or 125MHz output by register.
PPS	22	O	For AR8031: IEEE 1588v2 Pulse Per Second output
	22	NC	For AR8033: Reserved

2.2.1 Frequency and Voltage level

AR8031/8033 clock circuit supports both crystal input and external clock input.

2.2.1.1 Crystal scheme:



The basic principle for selecting the crystal and load capacitance is to make the steady oscillation frequency to be 25MHz+/-50ppm. Crystal with 25MHz+/-30ppm frequency stability/tolerance is preferred. Two 27pF NPO ceramic capacitances are recommended at default. The capacitance value can be adjusted base on final crystal selection and board level test results under full application temperature and voltage ranges.

Recommended Crystal parameters

Symbol	Parameter	Max	Typ	Min	Unit
Ff	Crystal fundamental frequency		25		MHz
Fs	Frequency stability over operating temperature@0-70°C	-30ppm		+30ppm	MHz
Ft	Frequency tolerance@25°C	-30ppm		30ppm	MHz
Fo	Oscillation frequency	-50ppm		50ppm	MHz
Vo	I/O voltage level (For drive level evaluation)		1.2V		V

2.2.1.2 External clock input

AR8031/8033 supports an external 1.2V swing 25MHz non-PLL clock input through XI pin.

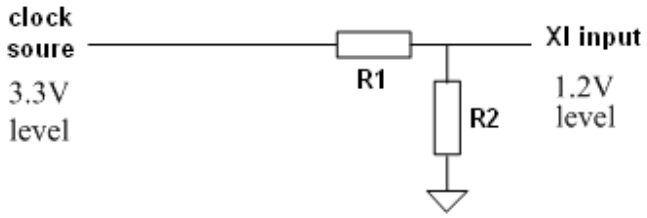
External clock input requirements:

Symbol	Parameter	Max	Typ	Min	Unit
T_XI_PER	XI/OSCI Clock Period	25-50ppm	25	25+50ppm	MHz
T_XI_HI	XI/OSCI Clock High	14	20		ns
T_XI_LO	XI/OSCI Clock Lo	14	20		ns
T_XI_RISE	XI/OSCI Clock Rise Time IL (max) to VIH (min)			4	ns
T_XI_FALL	XI/OSCI Clock Fall time IL (max) to VIH (min)			4	ns
V_IH_XI	The XCTLI input high level	0.8	1.2	1.5	V
V_IL_XI	The XCTLI input low level voltage	-0.3	0	0.15	V
Cin	Load capacitance		1	2	pF
Jitter_rms	Period broadband rms jitter			15	ps
Jitter_pk-pk	Period broadband PK-PK jitter			200	ps

When use an external clock input through XI pin, XO pin can be left floating.

It is noted that the reference clock injected into XI pin should have 1.2V swing, min 0.8V and max 1.5V.
Widely used clock sources are larger than 1.5V, typically 3.3V. Two schemes are provided for voltage level convert.

DC couple:



Split-voltage resistors should be close to the clock input, choose the value base on 0.8V<Vin*R2/(R1+R2) <1.5V.
Too large R1and R2 will affect the rise/fall time of input clock.
Recommendation for 3.3V to 1.2V: R1=1000ohm R2=499ohm

AC couple:

AR8031/8033 XI has internal 0.45V voltage bias. So it supports AC couple without external voltage bias. The input capacitance is typical 1pf. Consider of the trace parasite capacitance between capacitor and PHY = 1.2pf/inch * trace length typical
Recommendation for 3.3V to 1.2V change with 5inch trace, the cap is 5pf.

2.2.1.3 Output Clock: CLK_25M

CLK_25M in reference to power up and reset timing is shown below:

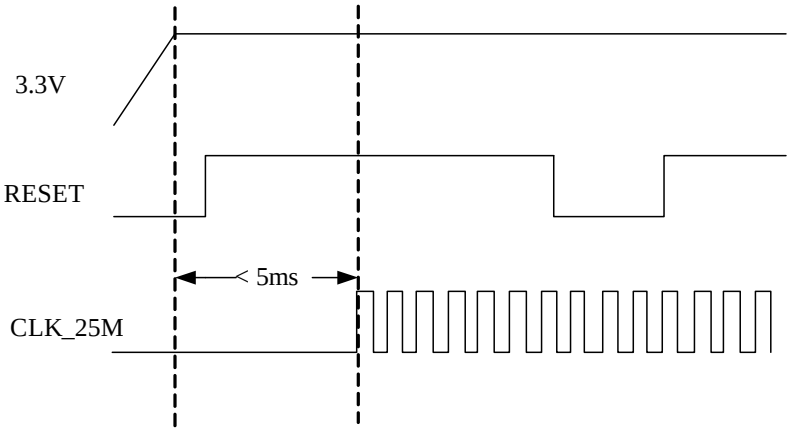


Figure 5. CLK_25M timing

After power is stable, CLK_25M will be stable in 5ms.

CLK_25M is an output clock for system application use. If not used, it can be left floating.

CLK_25M can be configured by register to 50MHz, 62.5MHz or 125MHz.

MMD 7, Address Offset = 0x8016(Hex)

4:2	Select_ clk25m	Mode	RW	CLK_25M output clock select:
		HW Rst	000	000 25MHz (from local Crystal) 001 25 MHz (from DSP source) 010 50 MHz (from local PLL source) 011 50 MHz (from DSP source) 100 62.5 MHz (from local PLL source) 101 62.5 MHz (from DSP source) 110 125 MHz (from local PLL source) 111 125 MHz (from DSP source) When Synchronous Ethernet works, DSP clock is recovered from line side. When synchronous Ethernet does not work, DSP clock will smooth change to local clock.
		SW Rst	Retain	

CLK_25M default outputs 25MHz clock from local crystal. Reset does not affect this clock output. If configure CLK_25M output 50M, 62.5M or 125M, when hardware reset is asserted, the clock will return to default 25MHz.

If CLK_25M output is used as a stable system reference, please configure AR8031/8033 to PLLON mode (debug register 0x1F [2] =1'b1). When in PLLOFF mode, hibernation state (power on without cable connection, PHY will enter power saving mode after about 10Seconds) AR8031/8033 will shutdown internal PLL which will cause CLK_25M output drops periodically.

Debug register 0x1F

Bit	definition	Mode	R/W	Description
2	PLLON/OFF selection	HW Rst	0	0=PLLOFF(default) 1=PLLON
		SW Rst	Retain	

CLK_25M output characteristics				
Symbol	Min	Typ	Max	Unit
Frequency	-50ppm	25, 50, 62.5,125	+50ppm	MHz
Output high voltage	2.3	2.62	2.8V	V
Output low voltage	GND-0.3	0	0.4	V
Jitter (RMS)			15	ps
Jitter (PK-PK)			125	ps

Notes: jitter is broadband period jitter with 100000 samples.

Output frequency stability depends on the crystal circuit oscillation frequency or input clock frequency stability.

If CLK_25M is not used, it can be left floating. If it is used, external 22ohm serial resistor is needed for signal integrity.

If it is used as a chip's reference clock, care about the input requirement, especially the jitter. For reliable application such as Giga switch/PHY reference clock, a jitter attenuation circuit is needed.

CLK_25M can be configured as the 1588 reference clock input by setting register MMD7 0x8017[11] =1'b1 to select external 1588 clock input as reference and the pin works as an input.

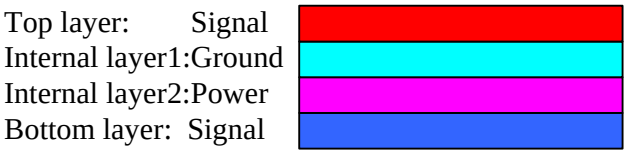
CLK_25M input characteristics as the 1588v2 reference clock				
Symbol	Min	Typ	Max	Unit
Frequency	-50ppm	50~125	+50ppm	MHz
input high voltage	2		2.8	V
input low voltage	GND-0.3		0.8	V
Cin Load capacitance		1	2	pf
Jitter (RMS)			15	ps
Jitter (PK-PK)			200	ps

2.2.1.4 Output Clock: PPS (for AR8031 only)

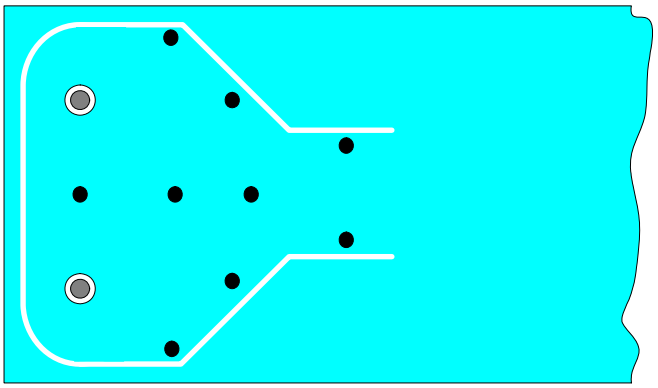
PPS is AR8031 1588v2 internal RTC (real time clock) time of day clock output. The clock period is 1 second so called PPS (Pulse Per Second). RTC has three optional inputs for reference, they are local PLL 125MHz clock, input 1588v2 reference clock and SYN-E recovered clock. When 1588v2 works, in slave mode the PPS is synchronous with master port. This clock output can be used as a system reference to control. Detail information about 1588 please refers to "1588v2 application note".

2.2.2 Layout guide

The system clock is a critical and sensitive signal. It can cause EMI issues if this part of the circuit is not well thought out during the PCB layout process. It also can couple high frequency signals and generate clock noise. *Figure below* shows an example for layout that can minimize EMI issues.



(a) layer stack



(c) Ground layer

Figure 6. Crystal PCB Layout Example

The crystal in demo circuit above is a through-hole one. If it is a surface-mounted crystal, the layout rule is also compatible. On the ground layer, the split gap should be 20mils.
-The XI and XO trace should be around 12mil. Too fat trace will increase the stray capacitance, too slim trace will cause parasitic inductance and resistance.
-Try to keep the other signal far away from XI and XO trace.
-Do not route any other signal below the crystal.
-Place crystal as close as possible to save the XI and Xo trace. Care about the capacitor position to save redundant stub.

2.3 System signals

2.3.1 Reset

Symbol	Pin	Type	Description
RSTn	2	I	System hardware reset, active low

The AR8031/8033 hardware reset needs the clock to take effect. Input clock including the crystal and external input clock should be stable for at least 1ms before RESET is deasserted. For chip reliability, an external clock must be input after the power is stable.

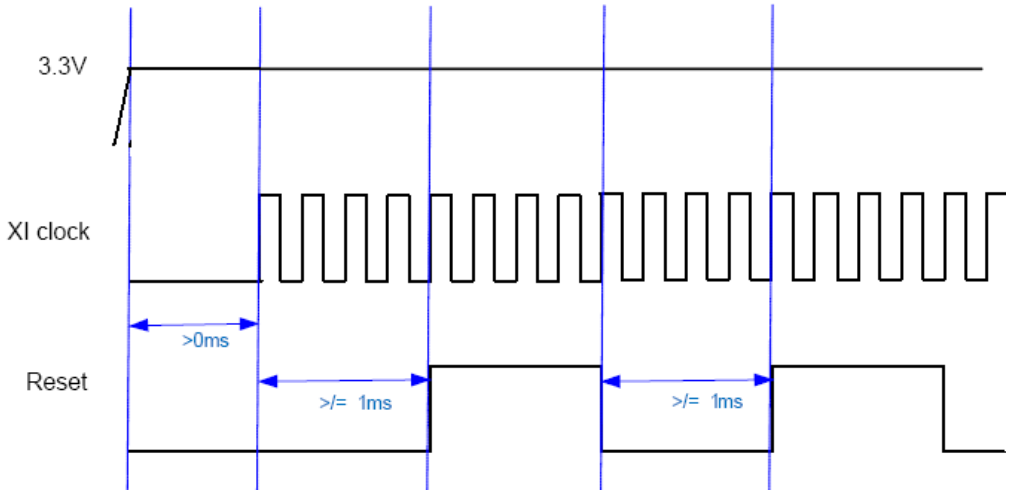


Figure 7. reset timing

When using crystal, the clock is generated internally after power is stable. For a reliable power on reset, suggest to keep asserting the reset low long enough (10ms) to ensure the clock is stable and clock-to-reset 1ms requirement is satisfied.
Hardware warm reset just need to satisfy clock-to-reset 1ms requirement.
Notes: RESET pin needs an external pull-up to 2.5V(VDDH) since there is no internal PU. active low. Vih=2V, Vil=0.8V so it supports 2.5V/3.3V input logic.
For power on reset RC circuit, 100K and 0.1uF is recommended.

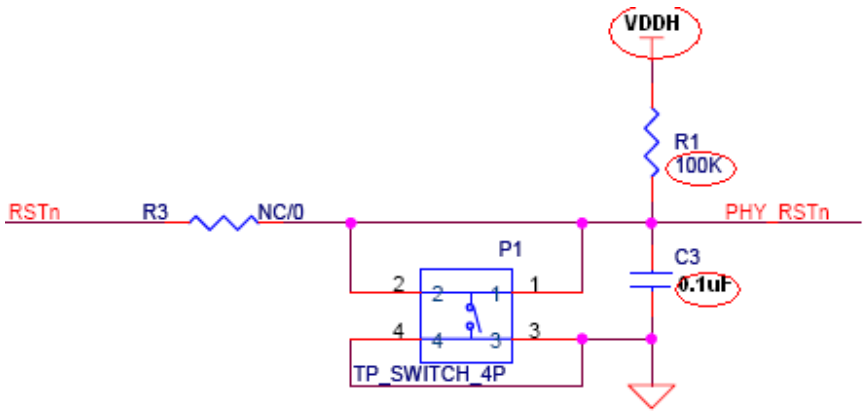


Figure 8. Reset circuit

2.3.2 LED

There are three LED pins to show different work modes of AR8031/8033.

Symbol	Pin	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_10_100	26	off	off	on	on	off	off
LED_1000	24	off	off	off	off	on	on
LED_ACT	23	on	blink	on	blink	on	blink

On=active Off=inactive

The LED_1000 and LED_ACT of AR8031/8033 are power-on strapping pins.

Pin symbol	**Power-on strapping function**	Default status
LED_1000	Select pin5 work mode: Pull-down for Interrupt function selection	With internal Pull-up
LED_ACT	**PHY address bit[2]**	With internal Pull-up

The LED_1000 and LED_ACT also control the LED active status.
When the pin is externally pulled-up, the LED pin will strap the high state and active low.
When the pin is externally pulled-down, the LED pin will strap the low state and active high.
The LED_10_100 active status is also controlled by LED_1000.
So the LED_10_100 and LED_1000 external design should be the same.

For design:
First select the pull-up or pull-down based on power-strapping function.
Then select the LED connection mode.

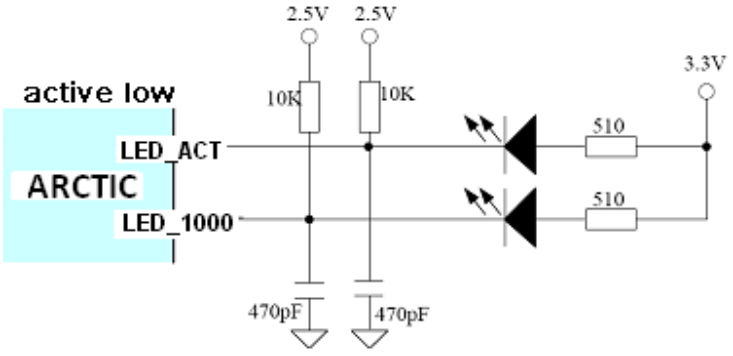


Figure 9. active low

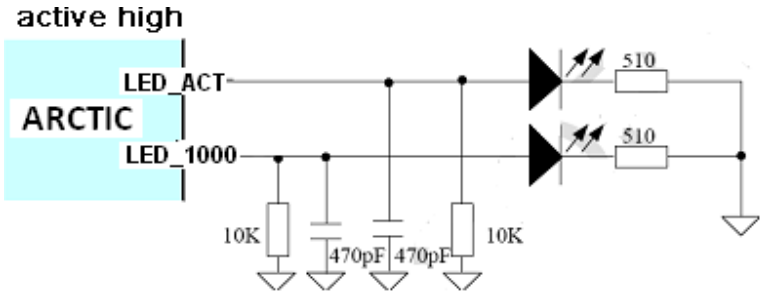


Figure 10. active high

If the LED pins are not used, suggest keep the 470pf cap for EMI design.
The three LED pins are fixed 2.5V logic. So please pull up to **VDDH only if needed.

2.3.3 Interrupt

Symbol	Pin	Type	Description
INT	5	D,PD	Interrupt signal to system, default OD-gate, need an external 10k pull-up, active low;
WOL_INT	40	D,PD	Wake-on-Lan Interrupt signal to system, default OD-gate, need an external 10k pull-up, active low; When PHY received valid Wake-on-Lan packet, WOL_INT will active with a low pulse of 32 link speed clock cycles.

**When hardware reset keeps low, INT pin outputs low.

There are two registers for Interrupt control. If the interrupt happens, corresponding bit in 0x13 is set to 1'b1. If the interrupt enable bit in register 0x12 is enabled, INT pin is active. The INT pin is inactive after register 0x12 is self cleared after reading.

2.3.4 RBIAS

Symbol	Pin	Type	Description
RBIAS	9	OA	External 2.37 KΩ 1% to GND to set bias current

RBIAS pin is connected with 2.37kΩ±1% resistance to ground to set bias current for AR8031/8033 internal analog circuitry. The resistor should be placed close to AR8031/8033 and keep the resistor and trace far away from other routing trace (at least 25mils) for a low noise environment, especially for clock trace and MDI interface trace.

2.4 RGMII interface

Symbol	Pin	Type	Description
RX_CLK	33	I/O,PD POS	RGMII receive clock output, 125MHz/25MHz/2.5MHz digital base on line side link speed, adding a 22Ω serial resistor near the PHY side is recommended.
RX_DV	32	I/O,PD POS	RGMII Receive data valid, no need for external serial damping resistor.
RXD0	31	I/O,PD POS	RGMII Receive data output [0], no need for external serial damping resistor.
RXD1	30	I/O,PD POS	RGMII Receive data output [1], no need for external serial damping resistor.
RXD2	28	I/O,PD POS	RGMII Receive data output [2], no need for external serial damping resistor.
RXD3	27	I/O,PD POS	RGMII Receive data output [3], no need for external serial damping resistor.
GTX_CLK	35	I,PD	RGMII transmit clock output, 125MHz/25MHz/2.5MHz digital base on line side link speed, adding a 22Ω serial resistor near MAC side is recommended to improve EMI. When connecting with 3.3V logic, please add a 500ohm near the PHY input to limit current.
TXEN	34	I,PD	RGMII transmit enable
TXD0	36	I,PD	RGMII transmit data [0]
TXD1	37	I,PD	RGMII transmit data [1]
TXD2	38	I,PD	RGMII transmit data [2]
TXD3	39	I,PD	RGMII transmit data [3]
MDIO	48	I/O,D,PU	Management data, 1.5KΩ pull-up to 3.3V/2.5V
MDC	1	I,PU	Management data clock reference

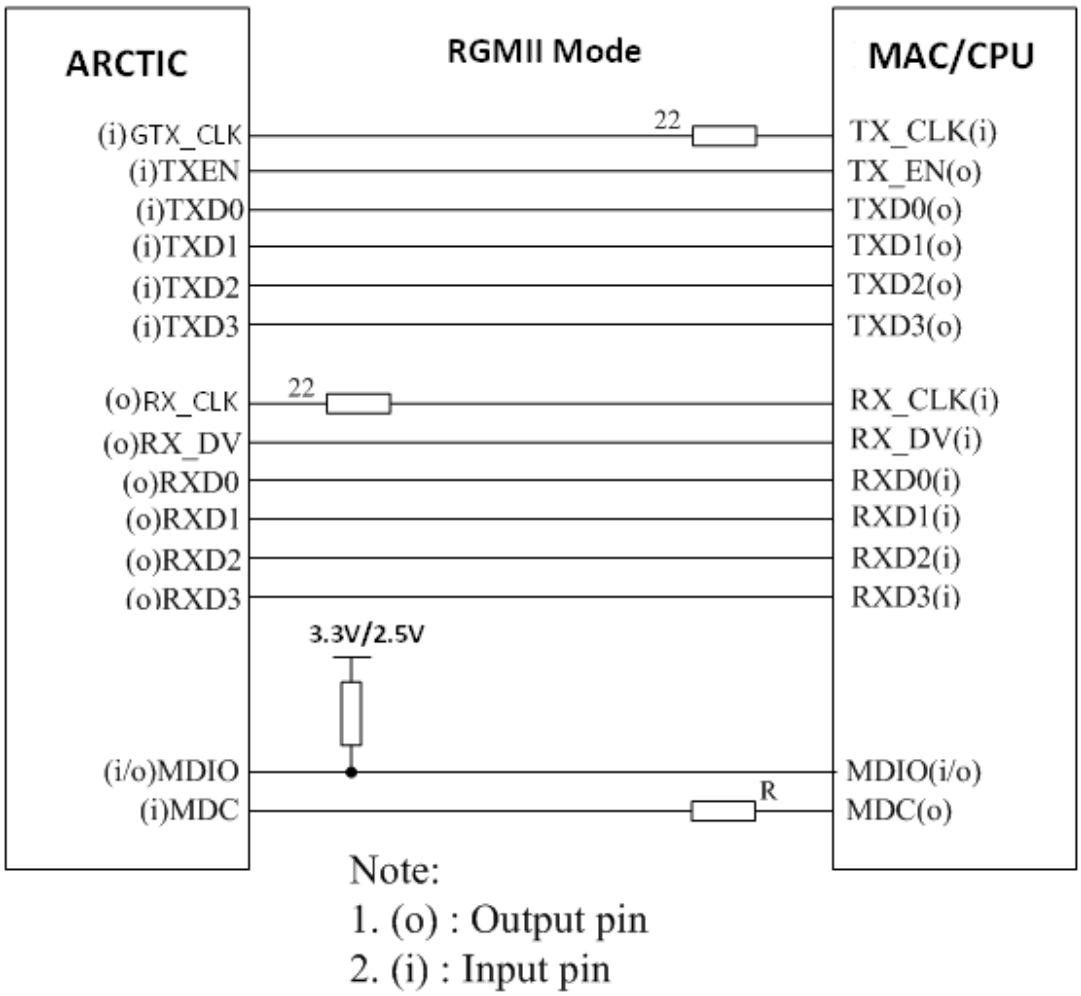


Figure11 RGMII interface

As defined in RGMII standard, the interface signal defined above in the figure. RGMII interface can work at 10/100/1000Mbps base on the line side link speed.
For Gigabit operation, the GTX_CLK/RX_CLK clocks will operate at 125MHz, the data is reference to both rising and falling edge of the clocks.
For 10/100Mbps operation, the clocks will operate at 2.5MHz or 25MHz respectively. The data is reference to the rising edge to GTX_CLK/RX_CLK.

AR8031/8033 supports 2.5V, 1.8V or 1.5V RGMII I/O voltage level. Also with 2.5V RGMII I/O voltage configuration AR8031/8033 can connect with 3.3V RGMII MAC interface. Since the

input can bear 3.3V logic signal, and the output logic VoH and VoL can satisfy the 3.3V LVCMOS/LVTTL requirement.
**If connect with a 3.3V RGMII interface, add a 500ohm near GTX_CLK pin to limit the input current.

AR8031/8033 RGMII interface output pin integrates 30ohm damping resistor, so no need for external serial resistors. Only suggest add two 22ohm serial resistor near the GTX_CLK and RX_CLK output to smooth the clock edge for EMI design.

Power design for different voltage level please refers to chapter 2.1.1.

MDIO/MDC
MDIO/MDC only supports 3.3V or 2.5V input.
MDIO is OD-gate, needs an external 1.5k pull-up to 2.5V/3.3V.

2.4.1 RGMII timing

RGMII standard V2.0 defined two modes of timing. One is transmitter without internal delay between clock and data, the other is transmitter clock integrates delay internally.
Detail timing parameters please refer to datasheet “RGMII AC characteristics” part.
For PHY the transmitter is in reference to RGMII RX direction.

AR8031/8033 integrates internal RX_CLK delay of typical 2ns (fufill min=1.2ns RGMII standard). RX_CLK delay can be disabled by setting debug register 0x0[15] =1’b0; the default value of this bit is 1’b1. So **AR8031/8033 default enables internal RX_CLK delay.**

RGMII interface device should support transmitter side internal delay. Even though the receiver side delay is optional, AR8031/8033 integrates a TX_CLK delay to help system application debugging.
AR8031/8033 TX_CLK delay is between 1.32ns and 3.82ns at default.
Can be enabled by setting debug register 0x5[8]=1’b1, the default value of this bit is 1’b0.

*** Please always use transmitter side internal delay or external trace delay for mass production use.

2.4.2 Layout guide

AR8031/8033 data transmission relies on RGMII interface with MAC. It is parallel to clock signal whose clock frequency is 125MHz. Care must be taken on data bus and clock compatibility during layout to avoid signal cross talk and timing problem.

- Equal trace length (maximum tolerance of GTX_CLK, TXD[3:0] should be **100mils**, maximum tolerance of RX_CLK, RXD[3:0] should be **100mils**) and 45 degree or arc layout cornering are recommended. Do not route trace with 90 degree turns. *Figure 11* shows the trace routing rule.

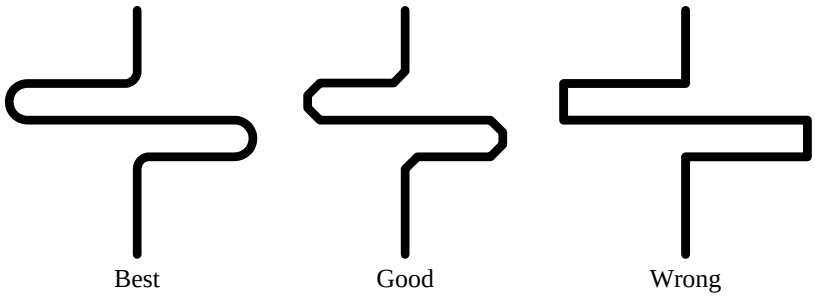


Figure 12: Trace routing rule

- Maximum trace length of RGMII interface is **15 inch**, 50Ω ± 10% single end impedance and typical at least 12mils space for separate trace is needed.
- All RGMII traces should be referenced to an uncut ground or power plane. Especially for RX_CLK and GTX_CLK traces, they are two sensitive and critical signals. It is very important that the two signal routing traces must be separated from other data bus as far as possible. It is suggested to route along with ground trace on both sides. Clock bus should satisfy at least **5W** principle with other signal.

  Notes: W=trace width. 5W principle is two adjacent traces center gap should large than 5 multiple trace width.

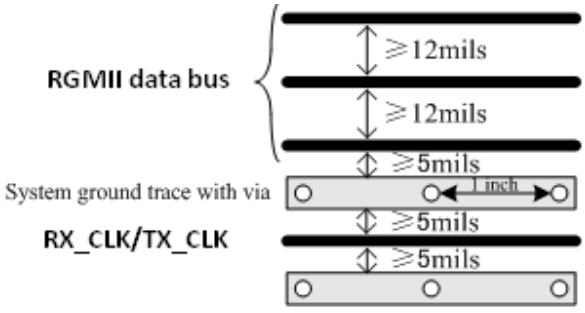


Figure 13: Trace routing rule for RGMII interface

- Because input pins on RGMII interface such as RX_CLK, RX_DV and RXD[3:0] are also multiplexed as power on strapping pins. It is important to layout power on strapping resistors to reduce redundant stub for signal integrity. For more information about power on strapping, please refer to chapter “Power on Strapping”. The layout rules of these signals are illustrated as shown below, using RXD1 as example.

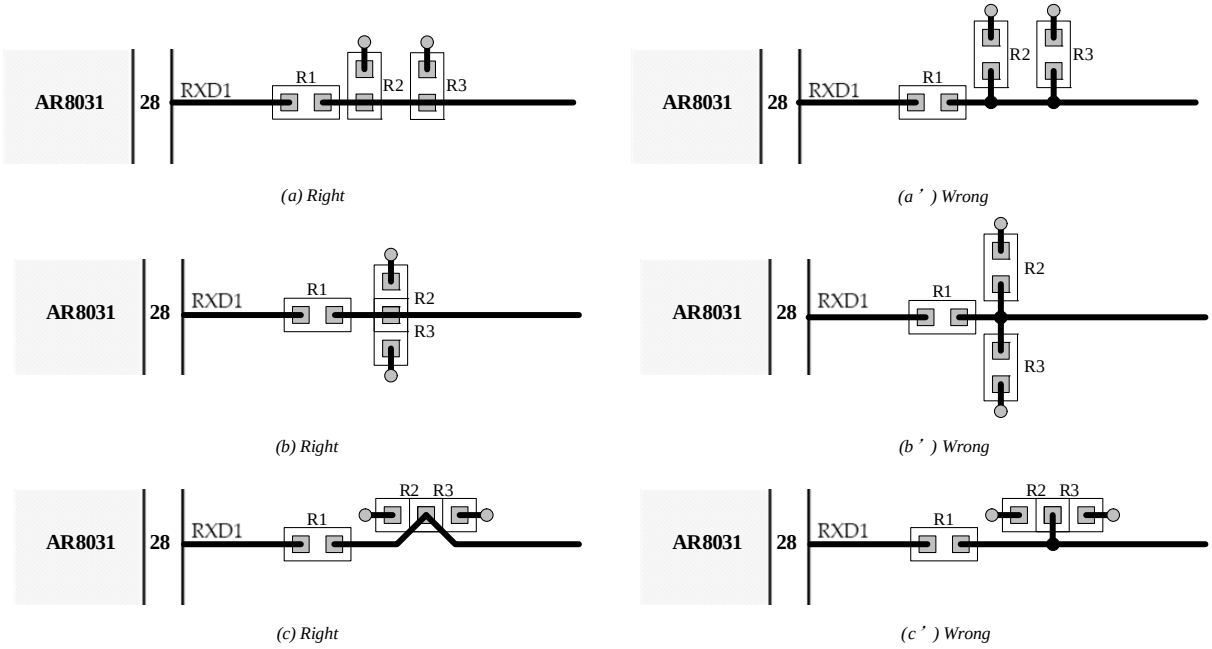


Figure 14: Input RGMII trace routing with pull high or pull down resistor

2.6 MDI interface

MDI interface pin map and description:

Symbol	Pin	Type	Description
TRXP0, TRXN0	11,12	IA,OA	Media Dependent Interface 0, 100ohm transmission line
TRXP1, TRXN1	14,15	IA,OA	Media Dependent Interface 1, 100ohm transmission line
TRXP2, TRXN2	17,18	IA,OA	Media Dependent Interface 2, 100ohm transmission

			line
TRXP3, TRXN3	20,21	IA,OA	Media Dependent Interface 3, 100ohm transmission line

The schematic circuit of MDI interface is shown below:

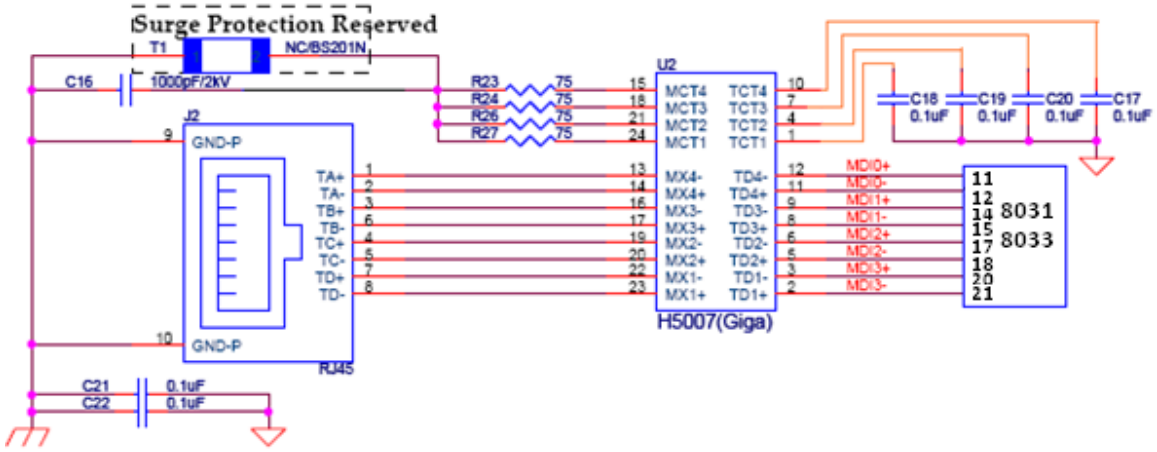


Figure 15. MDI interface schematic

Since AR8031/8033 is voltage drive mode GE PHY, the MDI interface does not need external termination resistors. And the CT point of the magnetic does not need a voltage reference either.

On the RJ45 jack side of the circuit, four 75Ω termination resistors are connected to the center tap of magnetic with a 1nF/2kV capacitor to chassis ground. This termination is named as Bob Smith termination. This circuit is used to enhance EMI and ESD performance of the system. The 75Ω resistor should be close to the magnetic. For detail information of Bob Smith termination you can refer to US patent US005321372. Separate 0.1uF capacitors are used between the chassis ground and system ground to enhance EMI performance.

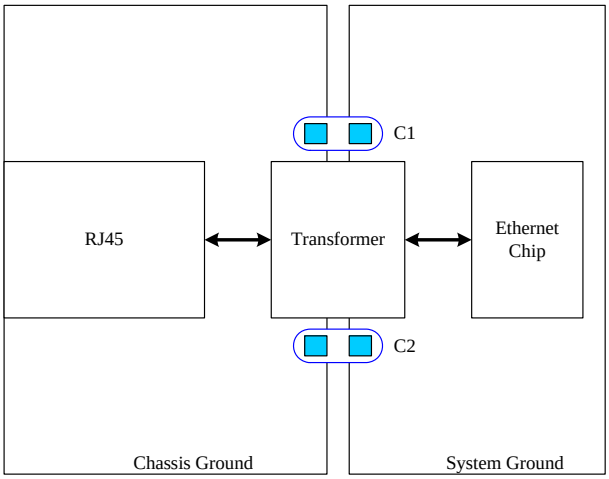


Figure 16. Ground design

Four 0.1uF ceramic capacitors are connected to CT of magnetic near PHY side to minimize common noise. These capacitors can be adjusted base on special design to smooth common noise.

2.6.1 Layout guide

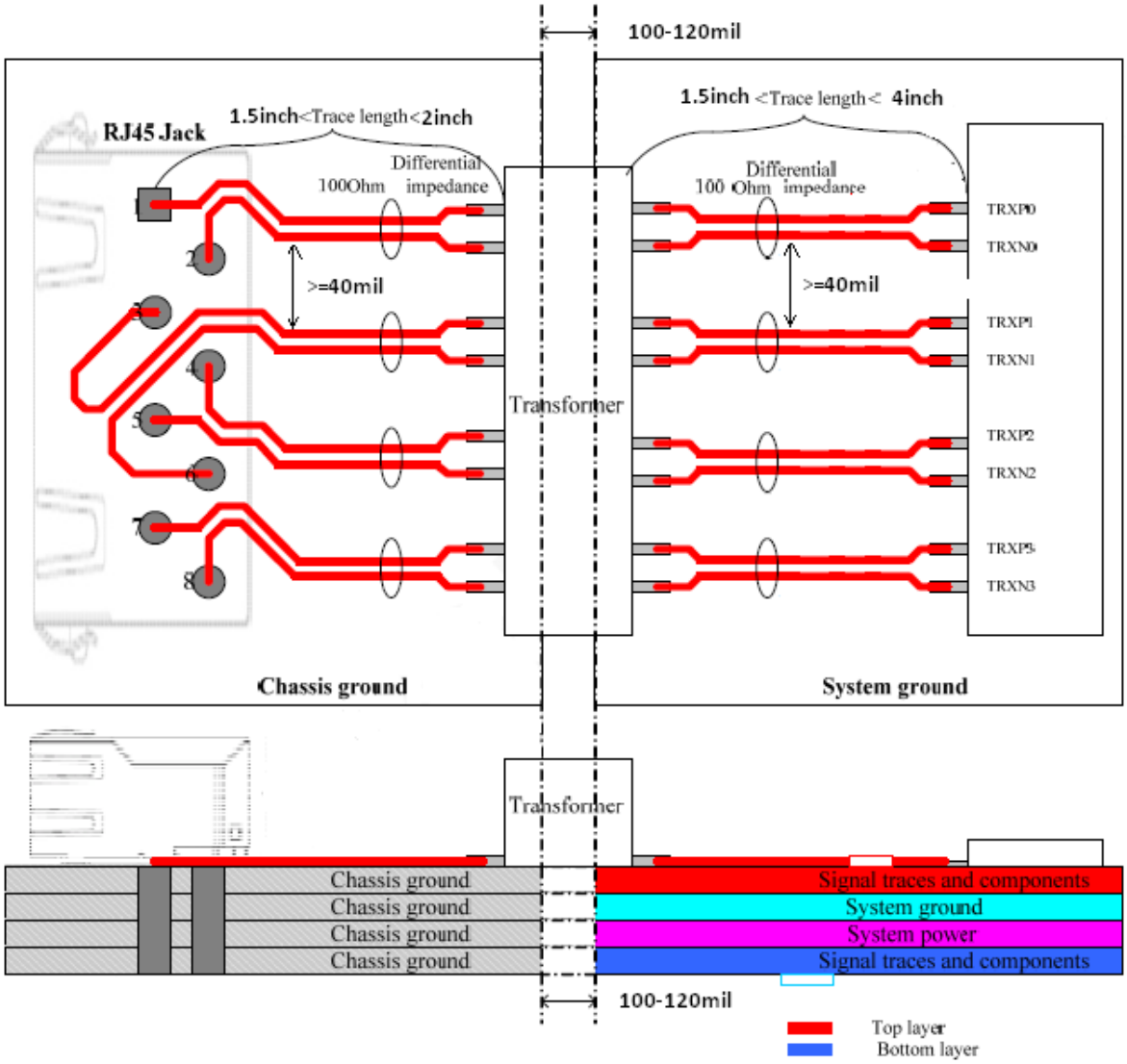


Figure 17. MDI layout example

- Same pair P/N skew should be less than **20mil**.
- Control each pair of the MDI differential signal impedance to 100ohm+/-10%
- To minimize cross talk, the space between separate adjacent pairs that are on the same layer should be 40 mils or more.
- The length between AR8031/8033 and transformer should be at least 1inch and less

than 4inch. Signal attenuation will cause problems for trace longer than 4inch. AR8031/8033 should be placed at least 1inch away from transformer for EMI. The length between RJ45 and magnetic suggest to be between 1.5-2inch.

- The split in ground plane should be at least 100~120mils. The split should run under center of transformer. Differential pairs never cross the split. If PCB is four layers, all layers design should abide by the same layout rule. If product does not separate the chassis ground and system ground, please leave this gap also, connect two parts of ground in the far end.

2.6.2 Transformer Selection

It is a key point to select transformer for AR8031/8033. Good EMI control can be got especially on low frequency bandwidth (30M~100MHz) if 8 core transformer with **common choke on line side** is selected. The performance of 8 core transformer with 3 lines common chokes is better. The performance of 12 core transformer is the best but the price is expensive.

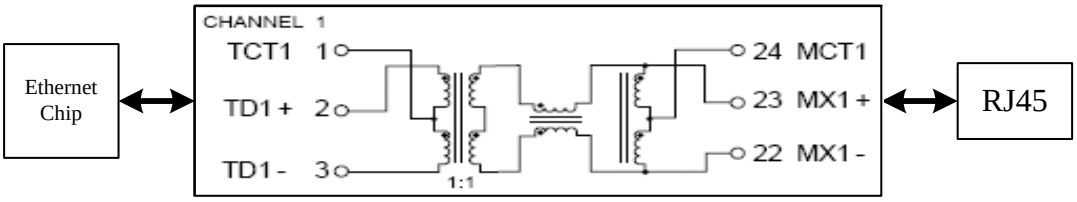


Figure 18: Transformer with 12 cores

2.6.3 Surge &ESD protection

AR8031/8033 can provide:

Differential mode surge	+/- 750V
Common mode surge	+/-4kV
Contact mode ESD	+/-9.6kV Class B
Cable ESD	+/-9.6kV
Cable discharge event	+/-6kV

All data are from demo board without ESD/Surge protection components.
If customer has higher level ESD/Surge requirement, need to add TVS (transient voltage suppressor) diode, GDT, Varistor or other components.

TVS selection:

Figure below shows a typical TVS application to provide differential and common mode ESD/Surge protection. TVS can fast divert over energy to ground/source and thus limit the transient voltage to a safe level.

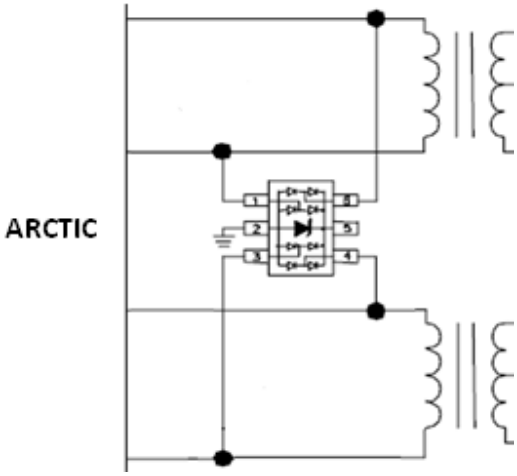


Figure 21. Typical TVS protection circuit for CM/DM

Follow the rules to select TVS can get better performance.
-low breakdown voltage can provide fast protection
-clamping voltage should be as low as possible
-low junction capacitance to avoid affecting MDI signal integrity.
-peak pulse power should be large enough to cover the maximum transient energy under application environment

2.7 Power on strapping

Symbol	PHY configure	Description	Default
RXD0	PHY address0	LED_ACT, LED [1:0] set the lower three bits of the physical address. The upper two bits of the physical address are set to the default "00".	0
RXD1	PHY address1		0
LED_ACT	PHY address2		1
RX_DV	MODE0	Mode select bit 0	0
RXD2	MODE1	Mode select bit 1	0
RX_CLK	MODE2	Mode select bit 2	0
RXD3	MODE3	Mode select bit 3	0
LED_LINK1000	INT Select	Add an external 10K pull-down to select Pin 5 work as an interrupt pin.	1

Notes: 0: internal weak pull-down 1: internal weak pull-up

Power on strapping is a power on work mode selection function. It sets the PHY address, work mode and RGMII I/O voltage LDO output level. Power on strapping state is latched during power-up reset or warm hardware reset.

MODE[3:0]	Description	Detail
0000	BASET_RGMII	RGMII to 10/100/1000BASE-T copper mode
0001	BASET_SGMII	SGMII to 10/100/1000BASE-T copper mode
0010	BX1000_RGMII_50	RGMII to 1000BASE-X fiber mode with 50ohm single end output impedance
0011	BX1000_RGMII_75	RGMII to 1000BASE-X fiber mode with 75ohm single end output impedance
0100	BX1000_CONV_50	1000BASE-T to 1000BASE-X converter mode, SERDES with 50ohm single end output impedance
0101	BX1000_CONV_75	1000BASE-T to 1000BASE-X converter mode, SERDES with 75ohm single end output impedance
0110	FX100_RGMII_50	RGMII to 100BASE-FX fiber mode, SERDES with 50ohm single end output impedance
0111	FX100_CONV_50	100BASE-TX to 100BASE-FX converter mode, SERDES with 50ohm single end output impedance
1011	RG_AUTO_MDET	Combo mode, RGMII to 10/100/1000BASE-T or RGMII to 100/1000BASE-X auto detect mode
1110	FX100_RGMII_75	RGMII to 100BASE-FX fiber mode, SERDES with 75ohm single end output impedance
1111	FX100_CONV_75	100BASE-TX to 100BASE-FX converter mode, SERDES with 75ohm single end output impedance
Others	Reserved	

**Some MAC devices input pins may drive high or low during power-up or reset. So PHY power on strapping status may be affected by the MAC side. In this case an external 10K pull-down/pull-up resistor is needed to ensure a stable expected status.
**RGMII interface power on strapping signal should be pulled-up to VDDIO_REG.

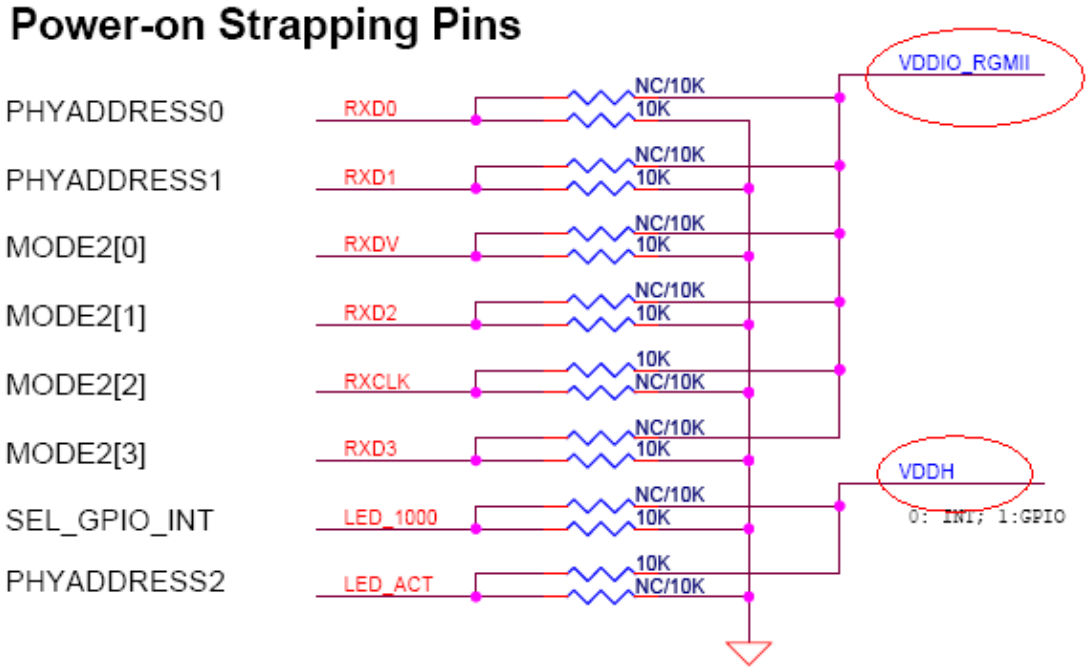


Figure 22. Power on strapping design

2.8 SGMII/SERDES interface

Symbol	Pin	Type	Description
SIP/SIN	46,45	IA	1.25Gbps differential inputs
SOP/SON	43,42	OA	1.25Gbps differential outputs
SD	41	IA	Signal Detect input, 1.2V logic. Typically connected to optical transceiver. Since AR8031/8033 signal detection function is embedded in SERDES, this pin can be left floating. High means signal valid. Low means loss of signal.

AR8031/8033 integrates a **CML** SGMII/SERDES interface to connect with MAC/optical transceiver.

2.8.1 Interface match

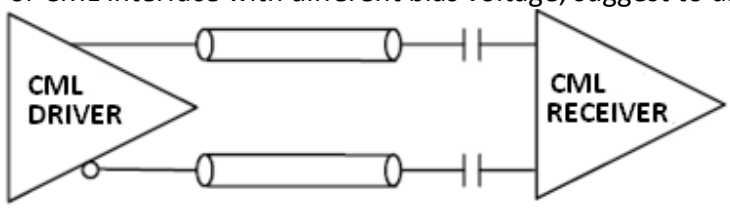
There are many kinds of voltage level SERDES interface, such as LVPECL, CML, LVDS and etc.

CML<->CML

AR8031/8033 SERDES parameters:

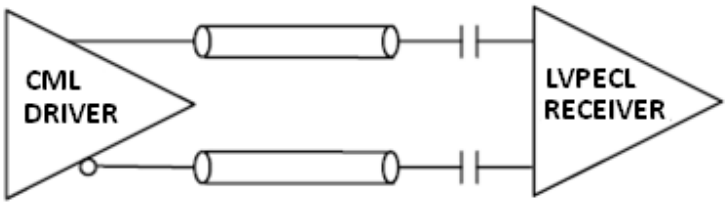
Symbol	Parameter	Min	Typical	Max	Unit
Voh	Output single high		950	1050	mV
Vol	Output single low	500	650		mV
|Vod|	Output differential voltage		300		mV
Vos	Output offset voltage	750	800	850	mV
Vih	Input single high		1050	1150	mV
Vil	Input single low	500	60		mV
Vio	Internal offset voltage	730	825	930	mV

Input and output bias voltage is typical 800mV which is integrated in the chip.
For CML interface with different bias voltage, suggest to use AC couple.



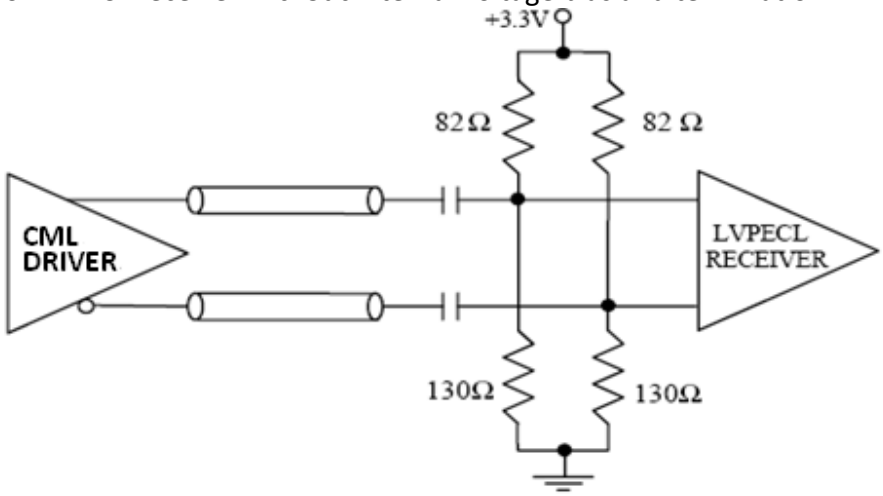
CML<->LVPECL

Typical SFP optical transceiver has a LVPECL SERDES interface. Optical transceiver which is compatible with SFP MSA has 100ohm termination resistor inside TD+/- interface. TD+/- and RD+/- both have AC coupling capacitors inside the transceiver. For receiver with internal voltage bias and termination:



Suggest keeping external 0.01uF AC coupling capacitor for ESD protection although most SFP transceiver has coupling capacitor inside. AR8031/8033 CML output differential voltage is 600mV default which can satisfy LVPECL 500mV input minimum requirement.

For LVPECL receiver **without** internal voltage bias and termination:



3.3*130/ (82+130) provides (VCC-1.3V) bias voltage for the receiver (VCC=3.3V) without on chip bias.
82//130 provides single end 50ohm termination.

AR8031/8033 outputs differential 600mV default with a 100ohm termination. If receiver needs a higher level, can configure it by register MMD7 0x8011 [15:13].

Device address = 7, Address Offset = 0x8011(Hex)

<table>
<tr><td rowspan="3">15:13</td><td rowspan="3">Sgmii_txdr_ctrl</td><td>Mode</td><td>R/W</td><td rowspan="3">[15:13] , driver output Vdiff, Peak to peak
001, 600mv;
010, 700mv;
011, 800mv;
100, 900mv;</td></tr>
<tr><td>HW Rst</td><td>3’b001</td></tr>
<tr><td>SW Rst</td><td>Retain</td></tr>
</table>

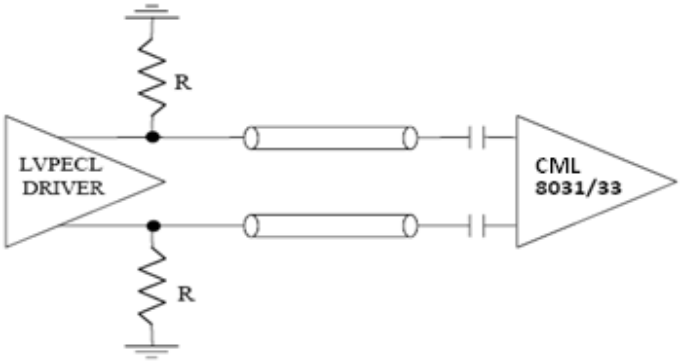
				Others, reserved

LVPECL-> CML

LVPECL common voltage is Vcc-1.3V, so LVPECL transmitter must use AC couple to connect with CML receiver.

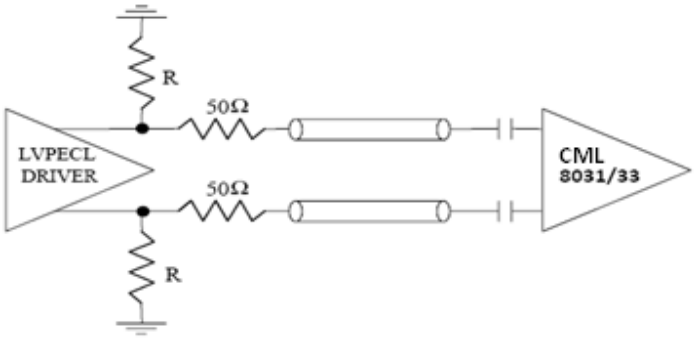
LVPECL output differential level is between 400mV and 1200mV which can satisfy CML input single and differential requirement of AR8031/8033.

For driver without internal bias, R typical 140-200ohm:



If the input differential voltage is higher than 1200mV, please add serial resistor near the LVPECL output to attenuate the signal.

For Driver without internal bias:



LVDS<->CML

AR8031/8033 internal bias voltage is around 0.8V. AR8031/8033 connects with LVDS interface please use AC coupling without any external termination circuit.

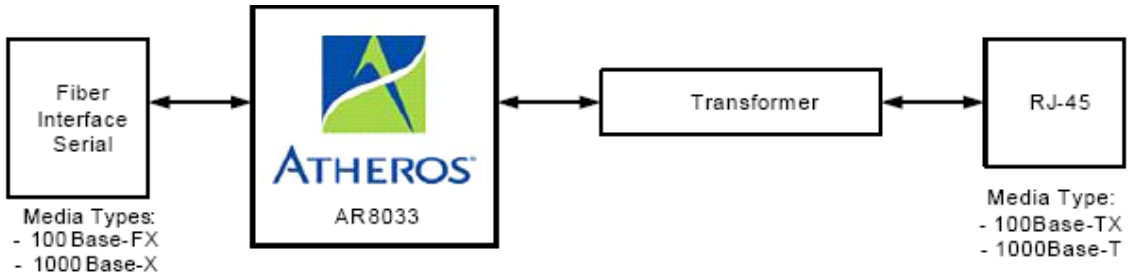
2.8.2 Layout guide

- Same pair P/N skew should be less than 20mil.

- Maximum trace length less than 10 inch.
- Control each pair of the SERDES differential signal impedance to 100ohm+/-10%, single end 50ohm+/-10%. Single end first.
- To minimize cross talk, the space between separate adjacent pairs that are on the same layer should be 40 mils or more.
- Do not suggest to route in top layer for better EMI. Must refer to a solid and complete plane.
- Interface match termination circuit please care about the redundant stub, refer to figure14.

2.9 work modes

2.9.1 Converter mode



AR8031/8033 supports 100BASE-FX fiber to 100BASE-TX copper and 1000BASE-X fiber to 1000BASE-T copper converter mode.

Converter mode can be configured by power on strapping (see power on strapping chapter). Also it can be configured by register 0x1f [3:0]. It takes effect immediately after writing.

3:0	Mode_cfg	Mode	R/W	Chip mode configure bits; Others: reserved 4'b0000:BASET_RGMII 4'b0001:BASET_SGMII; 4'b1110:FX100_RGMII_75; 4'b0110:FX100_RGMII_50; 4'b1111:FX100_CONV_75; 4'b0111:FX100_CONV_50; 4'b0011:BX1000_RGMII_75; 4'b0010:BX1000_RGMII_50;
		HW Rst	Sec.	
		SW Rst	Retain	

				4’b0101:BX1000_CONV_75; 4’b0100:BX1000_CONV_50; 4’b1011:RG_AUTO_MDET;

In converter mode, the fiber and copper interface auto-negotiation is independent of each other. Link status can be checked from copper page and fiber page separately.
Set 0x1f [15] =1’b1 to select copper page, set 0x1f [15] = 1’b0 to select fiber page.
See datasheet register part, offset address 0x0, 0x1, 0x4, 0x5, 0x6, 0x7, 0x8 and 0x11 refers to two register pages each.

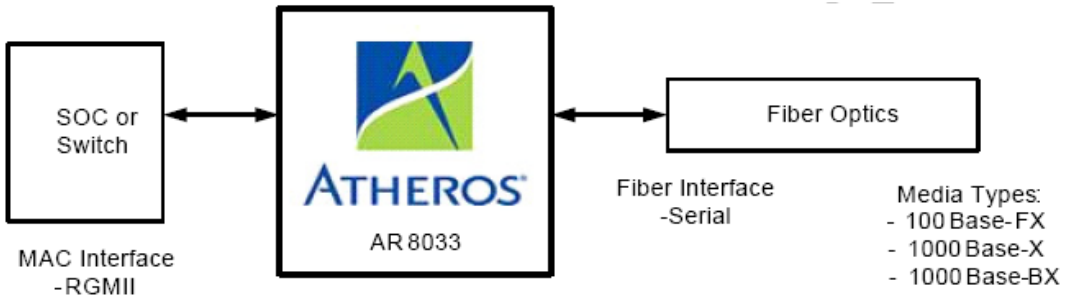
Once the fiber and copper interfaces both link up to the same speed, packets can go through the PHY. When 1000M converter mode (BX1000_CONV) is set, the copper port can still link to 100M with a 100M link partner. But packets can not go through PHY.

Since two interface auto-negotiation separately, need controller to confirm the duplex and pause of two remote link partners matched.

The three LEDs show fiber interface status.

In converter mode, the RGMII interface signal can be left floating.

2.9.2 Fiber mode

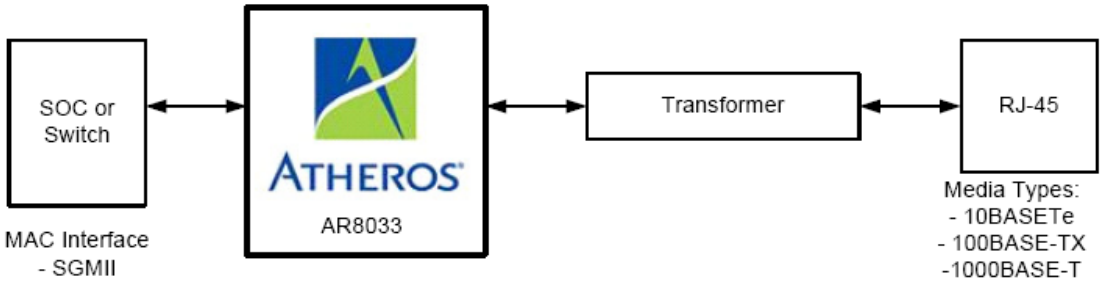


AR8031/8033 supports both 1000BASE-X and 100BASE-FX mode which can be configured by power on strapping (see power on strapping chapter) and by register 0x1F [3:0].
Fiber mode can not auto detect the link speed.
When set 1000BASE-X mode, it works only in 1000Mbps.
When set 100BASE-FX mode, it works only in 100Mbps.
RGMII design guide see chapter2.4.
Fiber port design guide see chapter2.8.

In fiber mode, the MDI+/-[3:0] can be left floating.

2.9.3 SGMII mode

SGMII is serial GMII interface which only use 4 lines to connect with MAC/SOC.
When the copper side link is established, SGMII will pass the copper side link status (link, speed, duplex) to MAC side build the link.



AR8031/8033 SGMII share the same physical SERDES with fiber interface, see chapter2.8 for design guide. In SGMII mode, the SGMII sync, auto-negotiation, link status in register 0x11 fiber page. First need to write 0x1f[15]=1'b0 to select fiber page.

2.9.4 Auto-media detect (combo) mode

AR8031/8033 supports both RGMII to fiber and RGMII to copper work modes.
These two work modes can be enabled at the same time by setting mode bit to 4'b1011 by power on strapping pin or register 0x1F [3:0].
When no fiber or cable is plugged, the two interface will enter power saving mode.
When fiber is connected, the RGMII to fiber mode is working.
When copper cable is plugged in, the RGMII to copper mode is working.
When both media are plugged in, the media with the high priority is working which can be set in register 0x1F [10] (0= prefer copper; 1=prefer fiber).
In auto-media detect mode, the fiber port can be select as 1000M or 100M base on register 0x1F[8](1=1000BASE-X; 0=100BASE-FX) default works in 1000BASE-X.