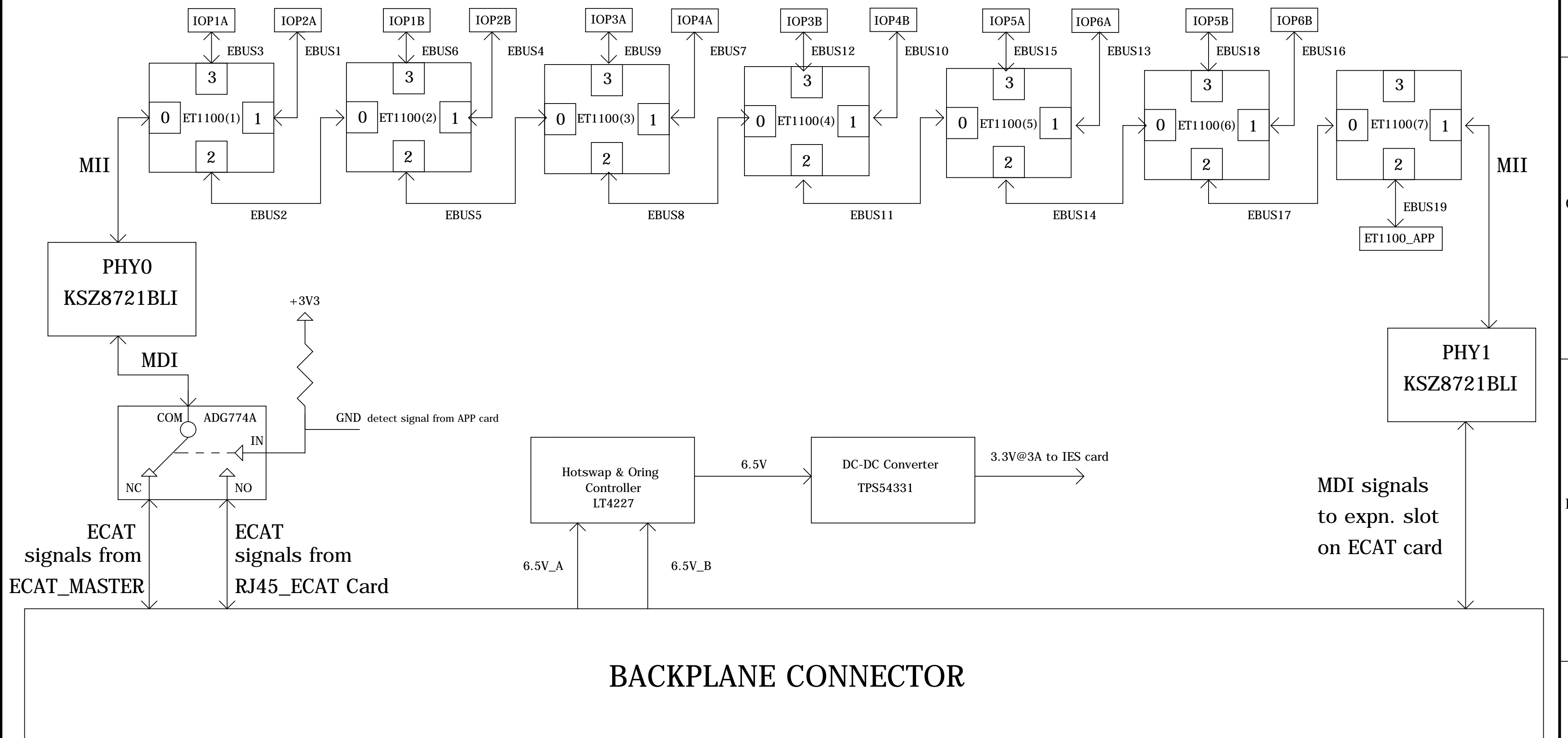


IES CARD BLOCK DIAGRAM

All these IOP EBUS signals will be routed via backplane



APPROVALS		DATE		COMPRESSOR CONTROLS CORPORATION			
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ENGINEER Vijay				SIZE C	DWG. NO. FILE 18-xxxxxx-rev-2.0	SHEET 2 of 12	PROD REV. 3.0

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DWG. NO. SH REV.

D

D

C

C

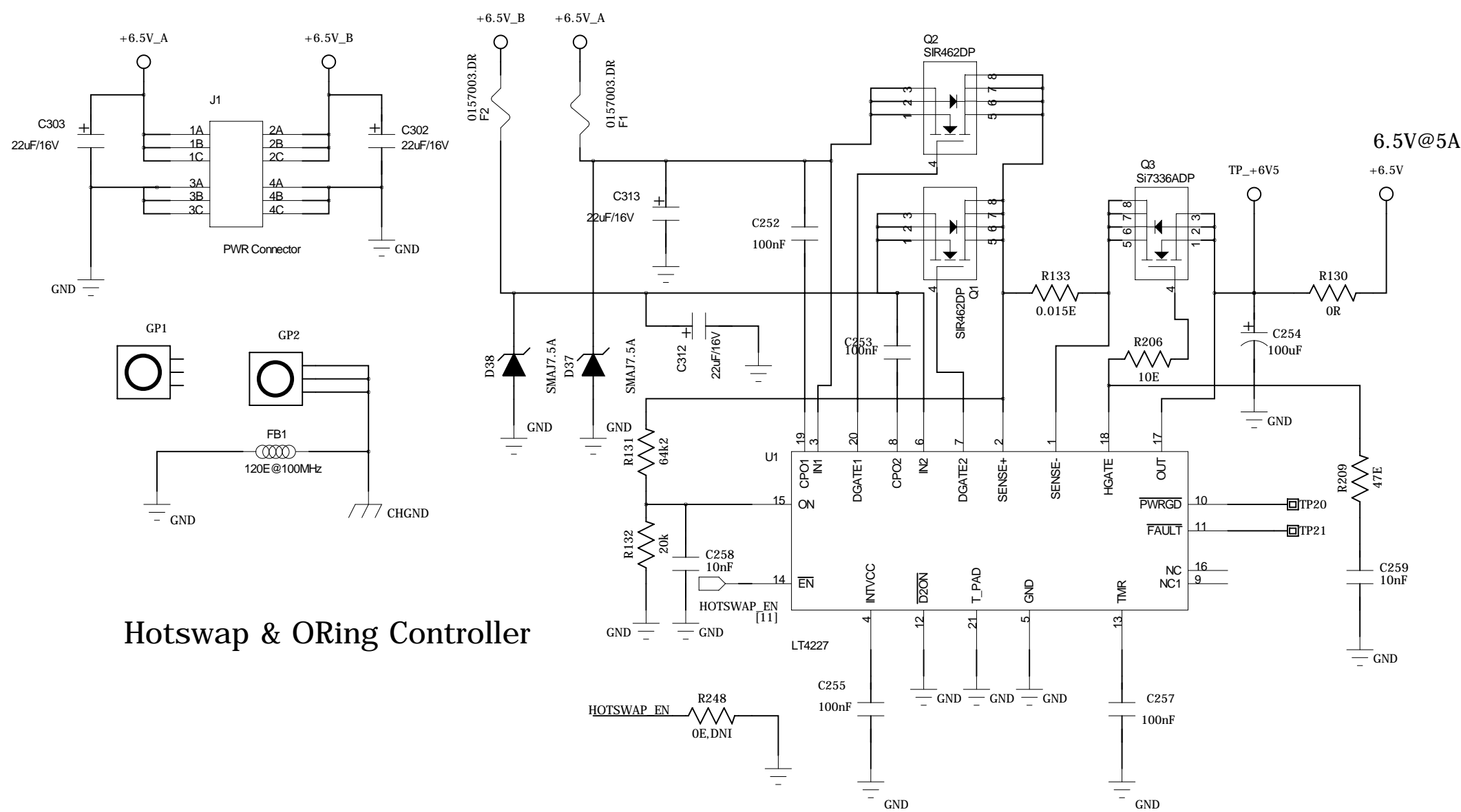
B

B

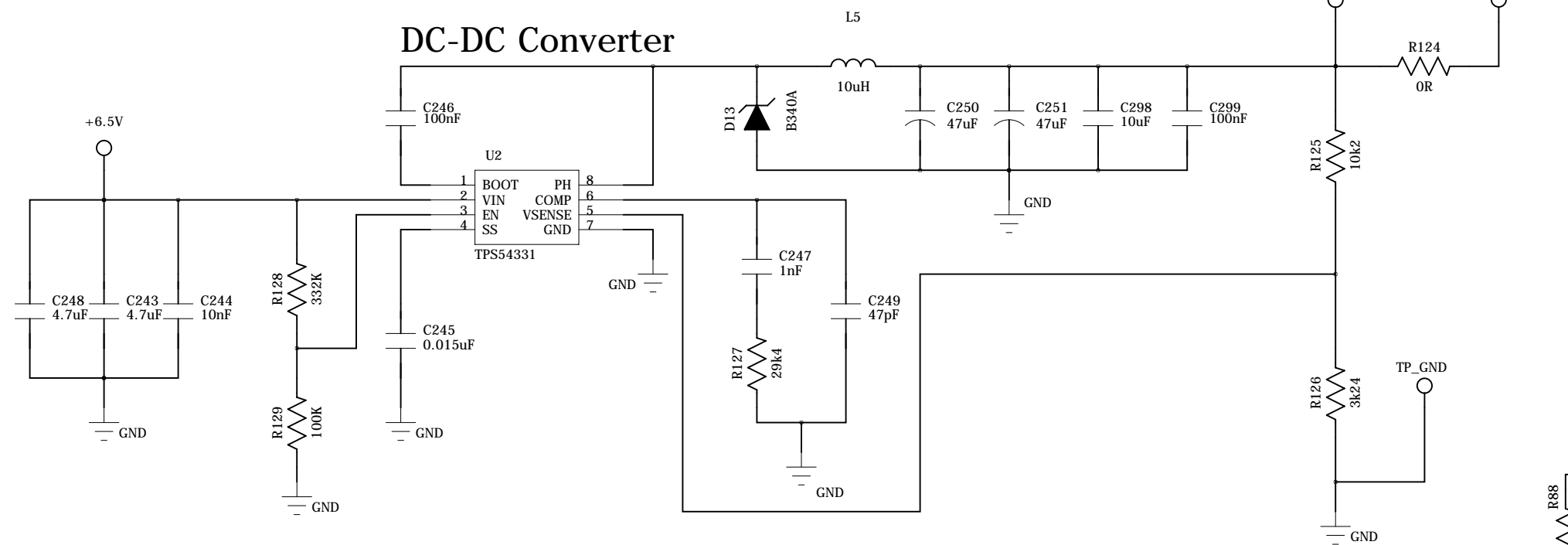
A

A

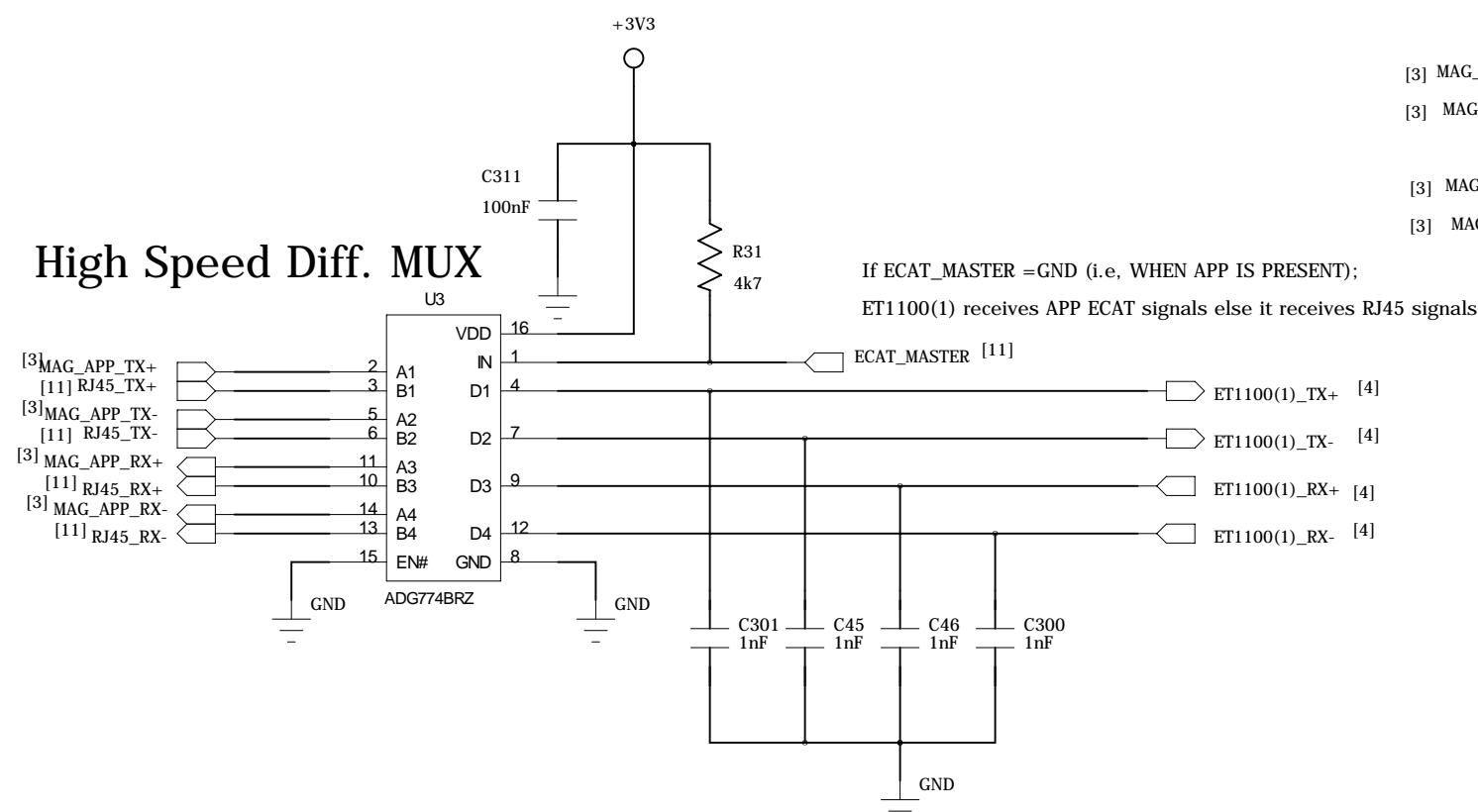
Hotswap & ORing Controller



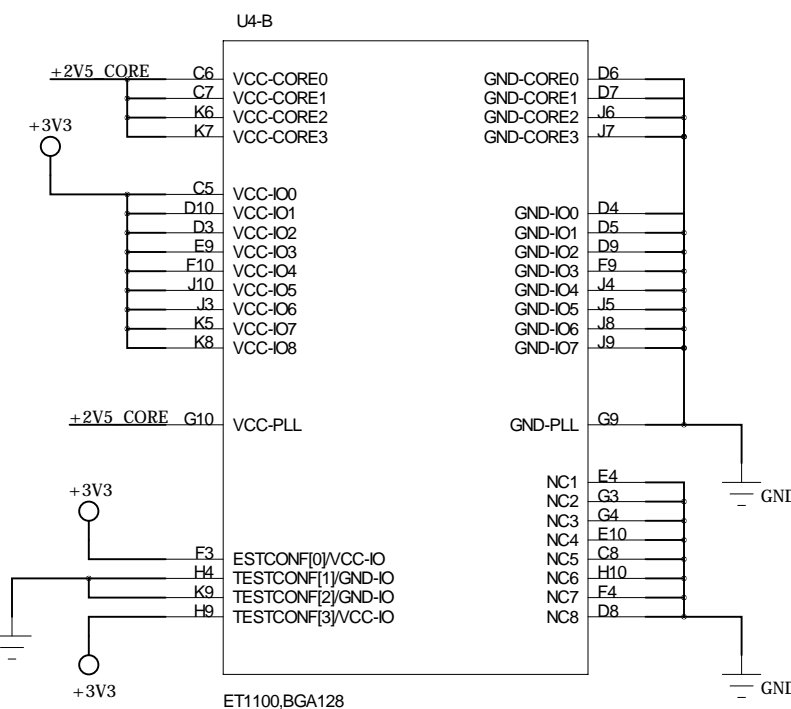
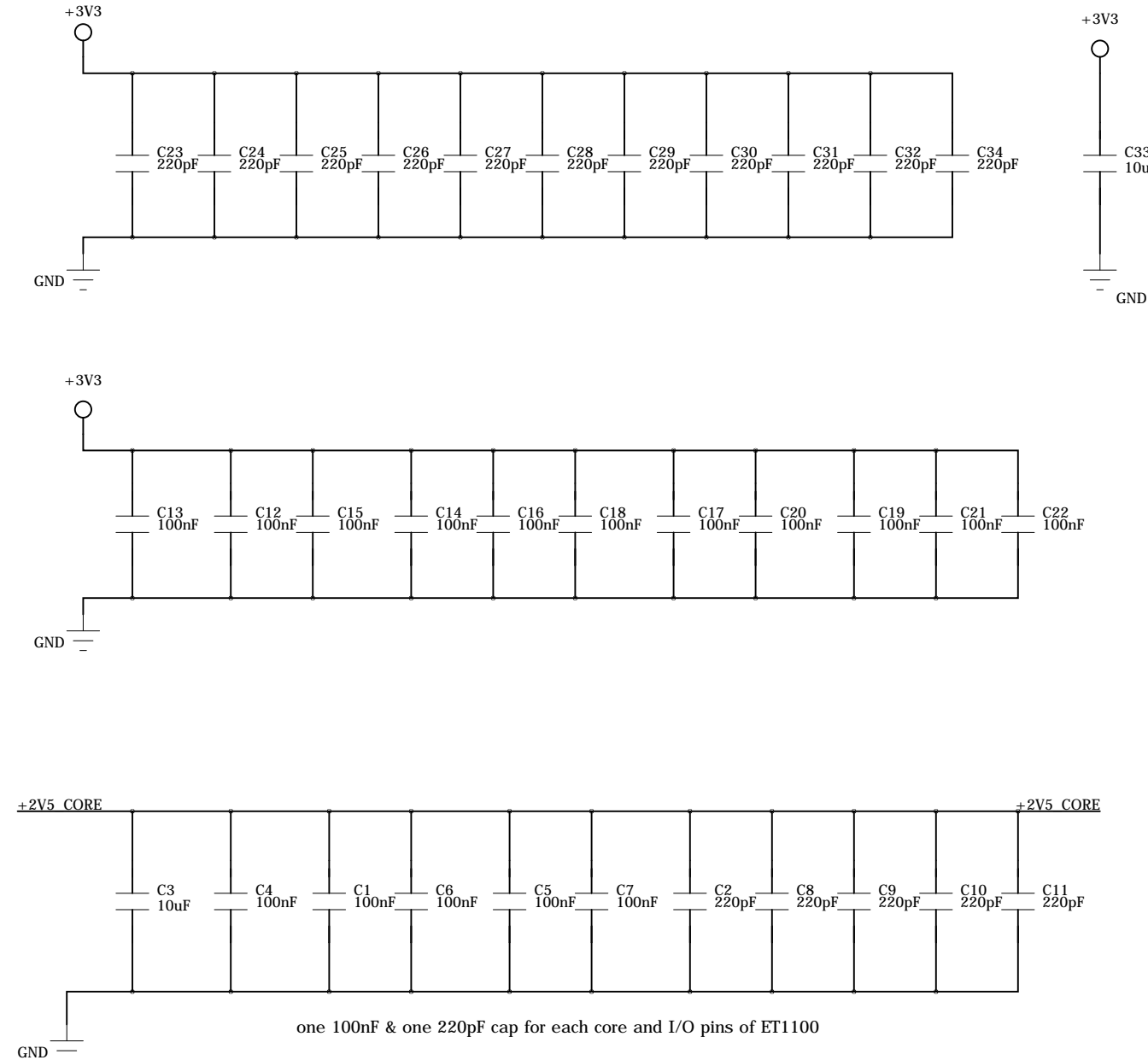
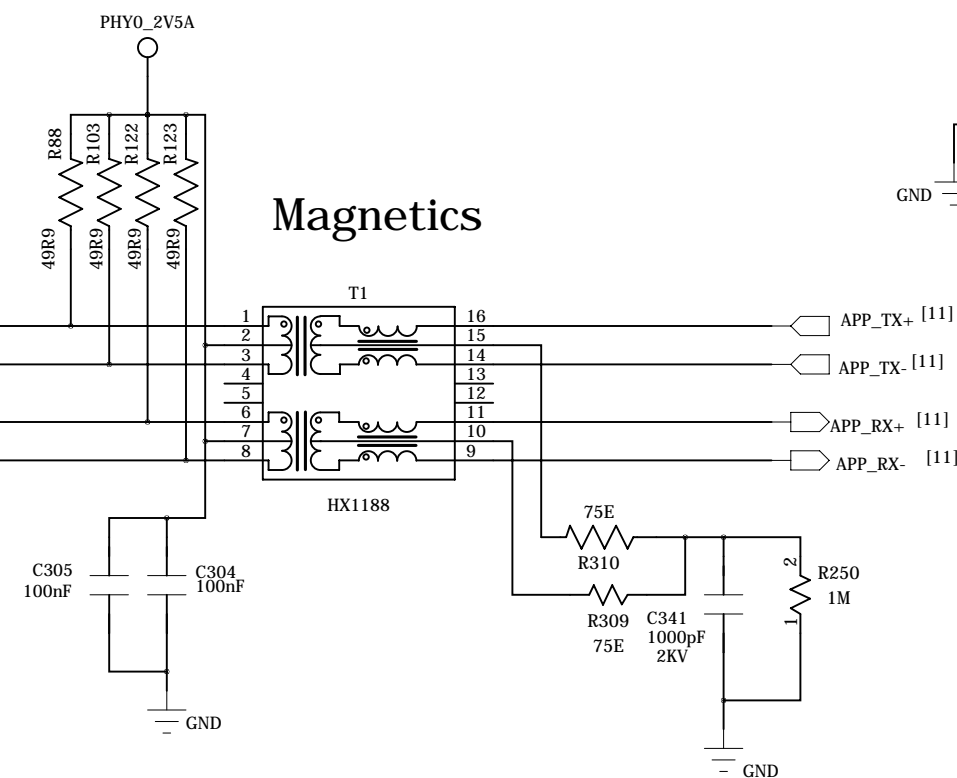
DC-DC Converter



High Speed Diff. MUX



Magnetics



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CHECKED					
ENGINEER	Vijay		SIZE	DWG. NO.	SHEET
			C	18-xxxxxx-rev-2.0	3 of 12
				FILE	SCALE
					PROD. REV.
					3.0

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D

C

B

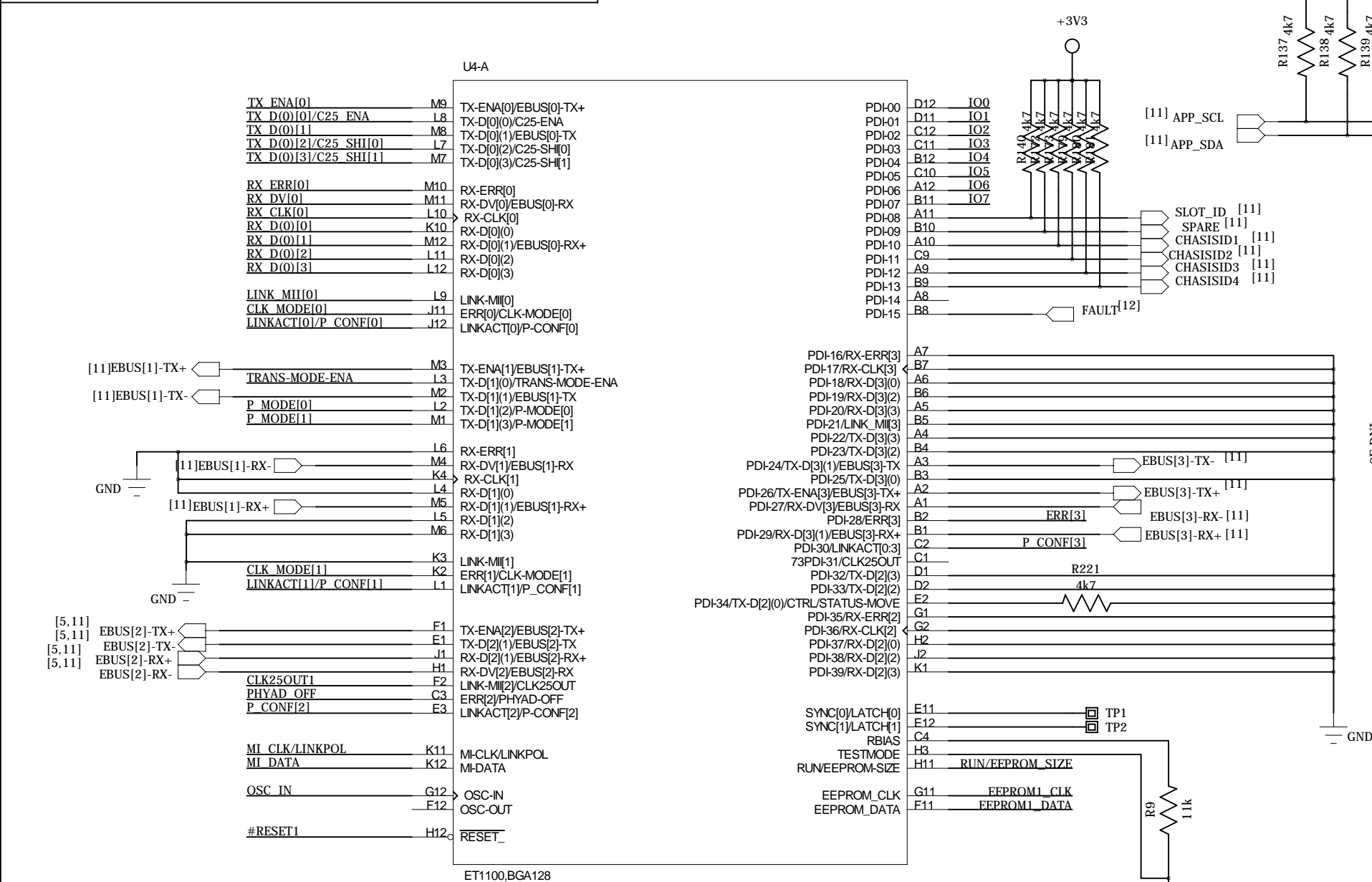
A

D

C

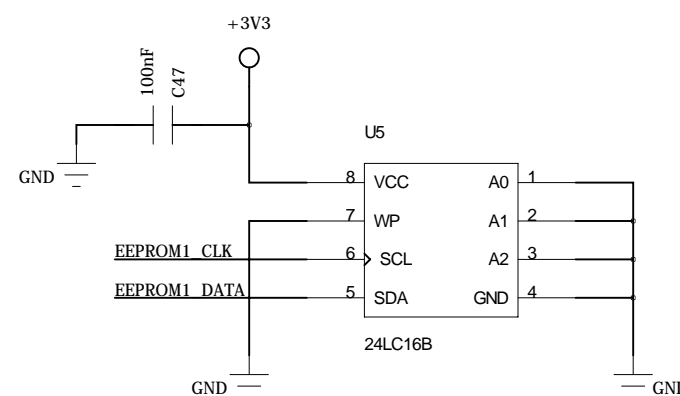
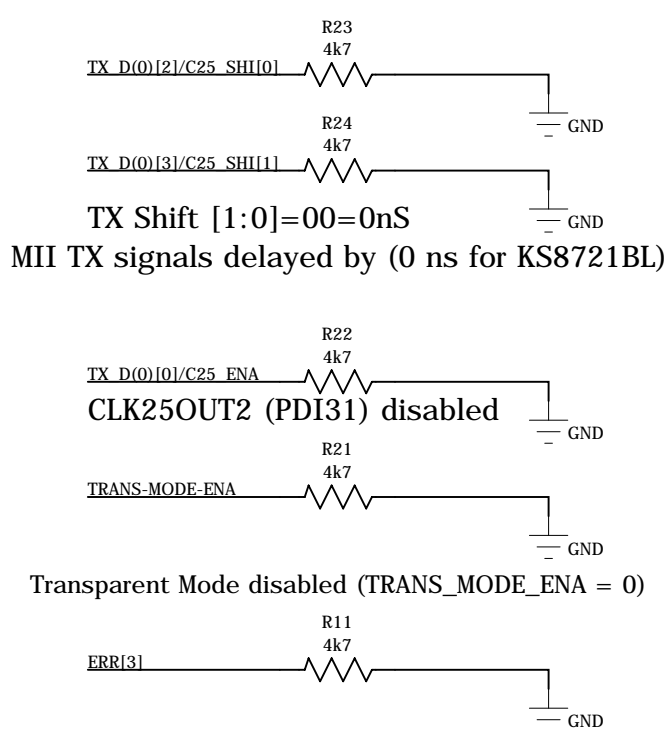
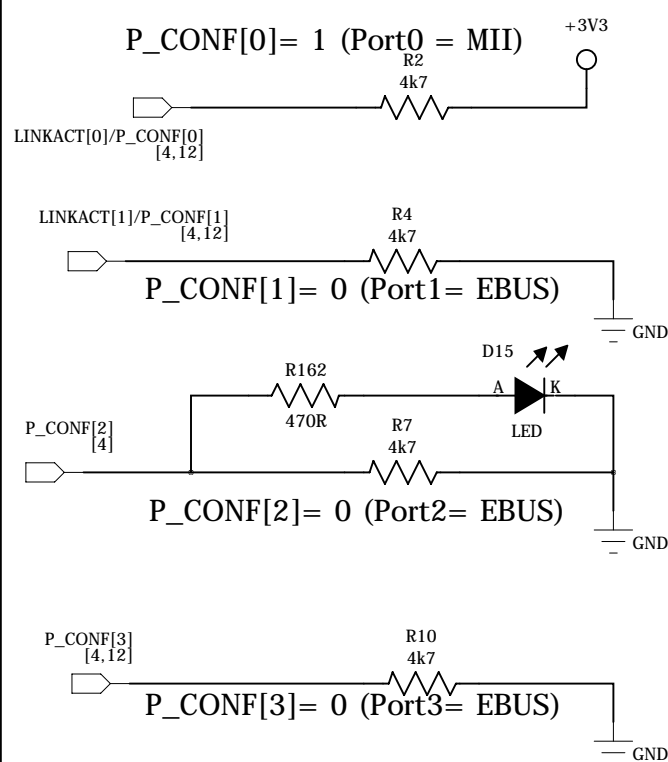
B

A

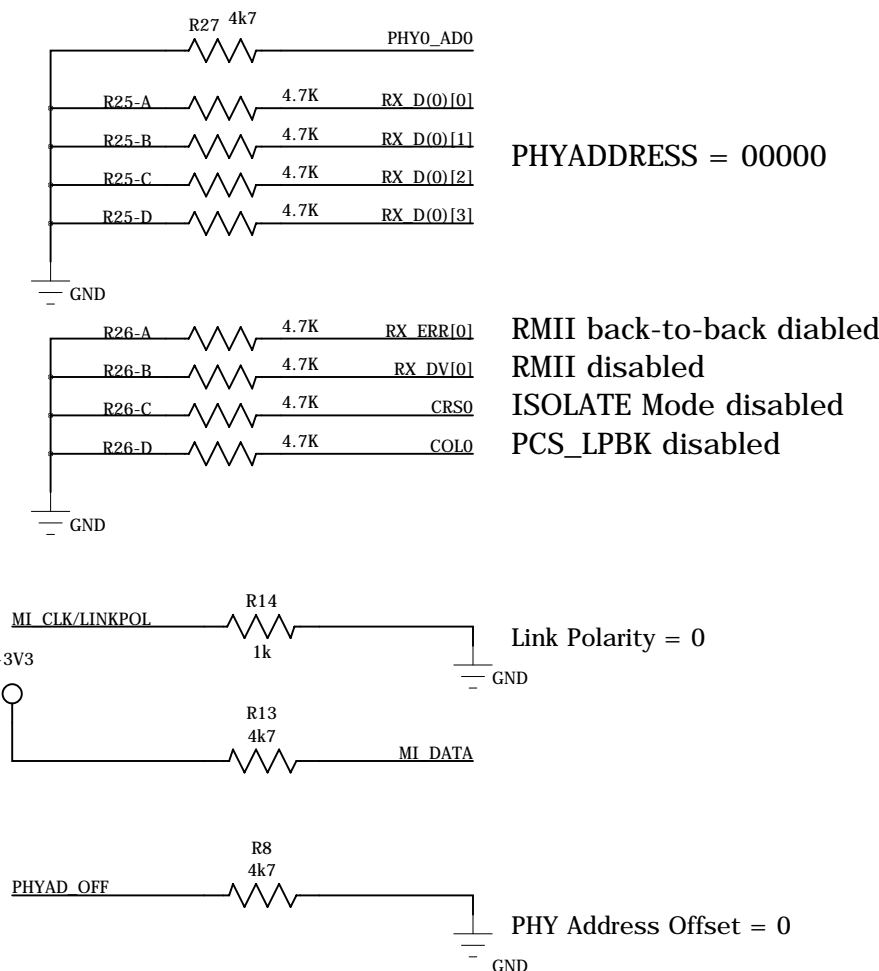
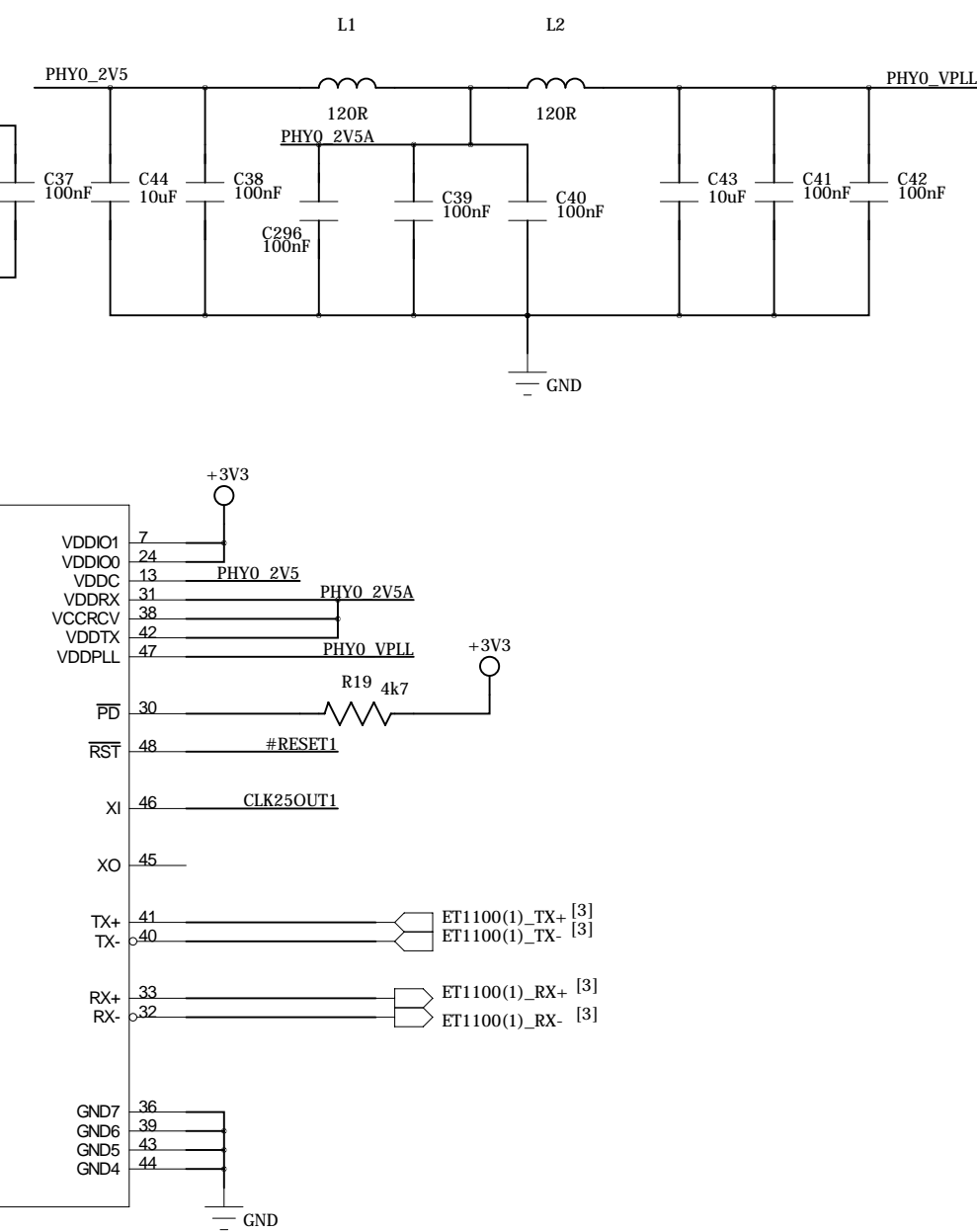
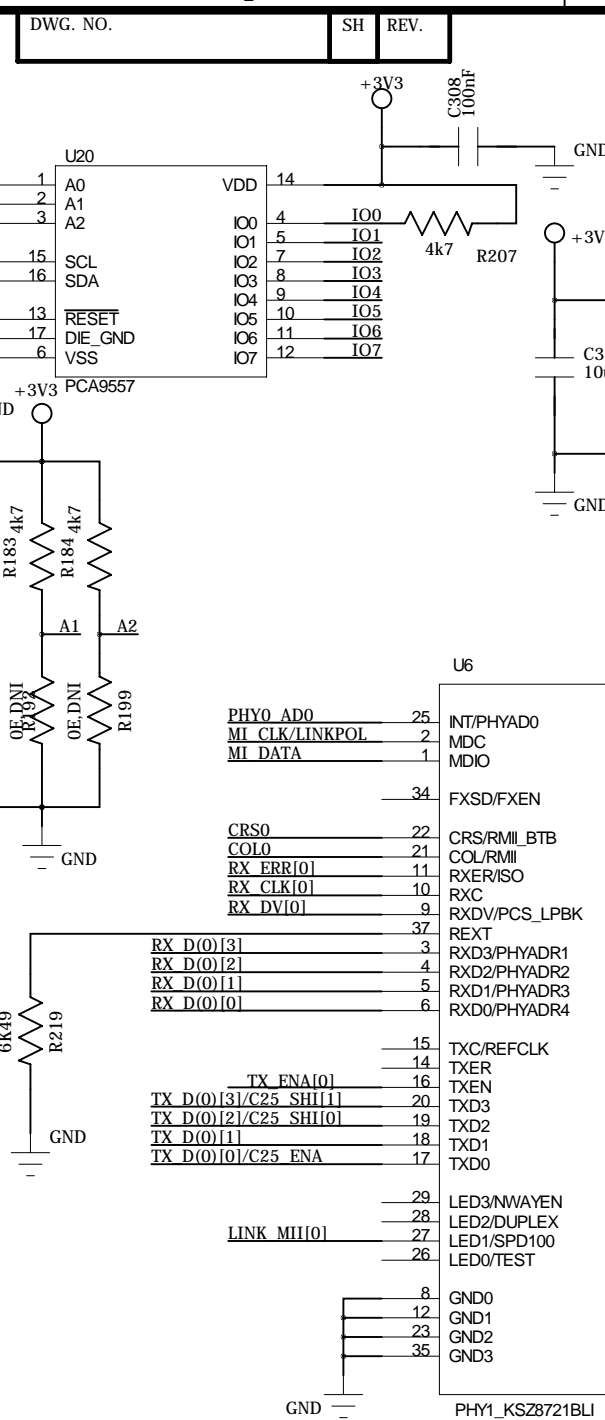
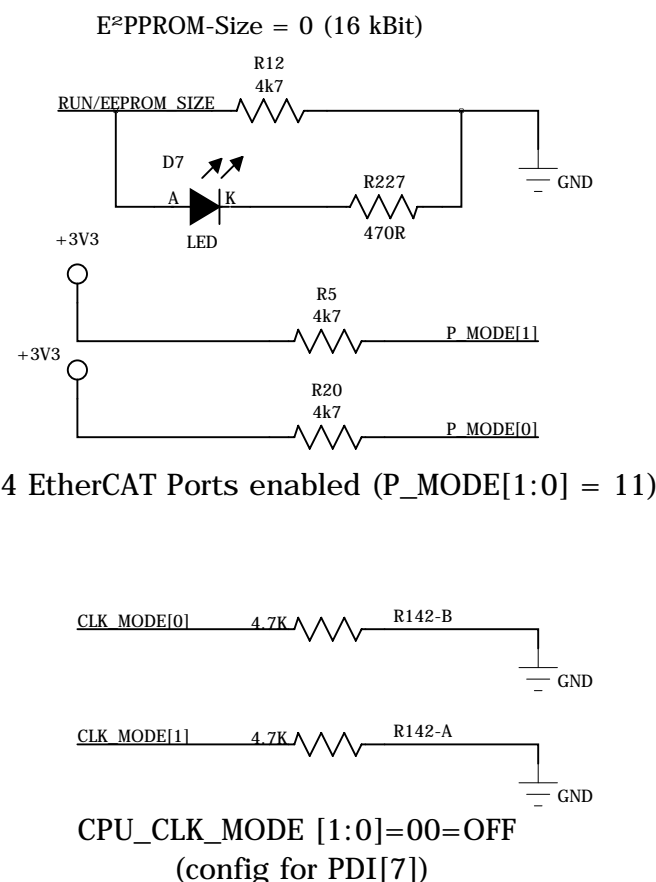


EBUS & PHY traces must be controlled impedance traces
EBUS is strictly 100 ohm
use 4 mil width traces for these signals

Place TCXO as close as possible to ET100 pins



Keep I2C lines as short as possible



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CHECKED					
ENGINEER	Vijay		SIZE	DWG. NO.	SHEET
			C	18-xxxxx-rev-2.0	4 of 12
			FILE	SCALE	PROD REV.
					3.0

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DWG. NO.

SH

REV.

D

C

B

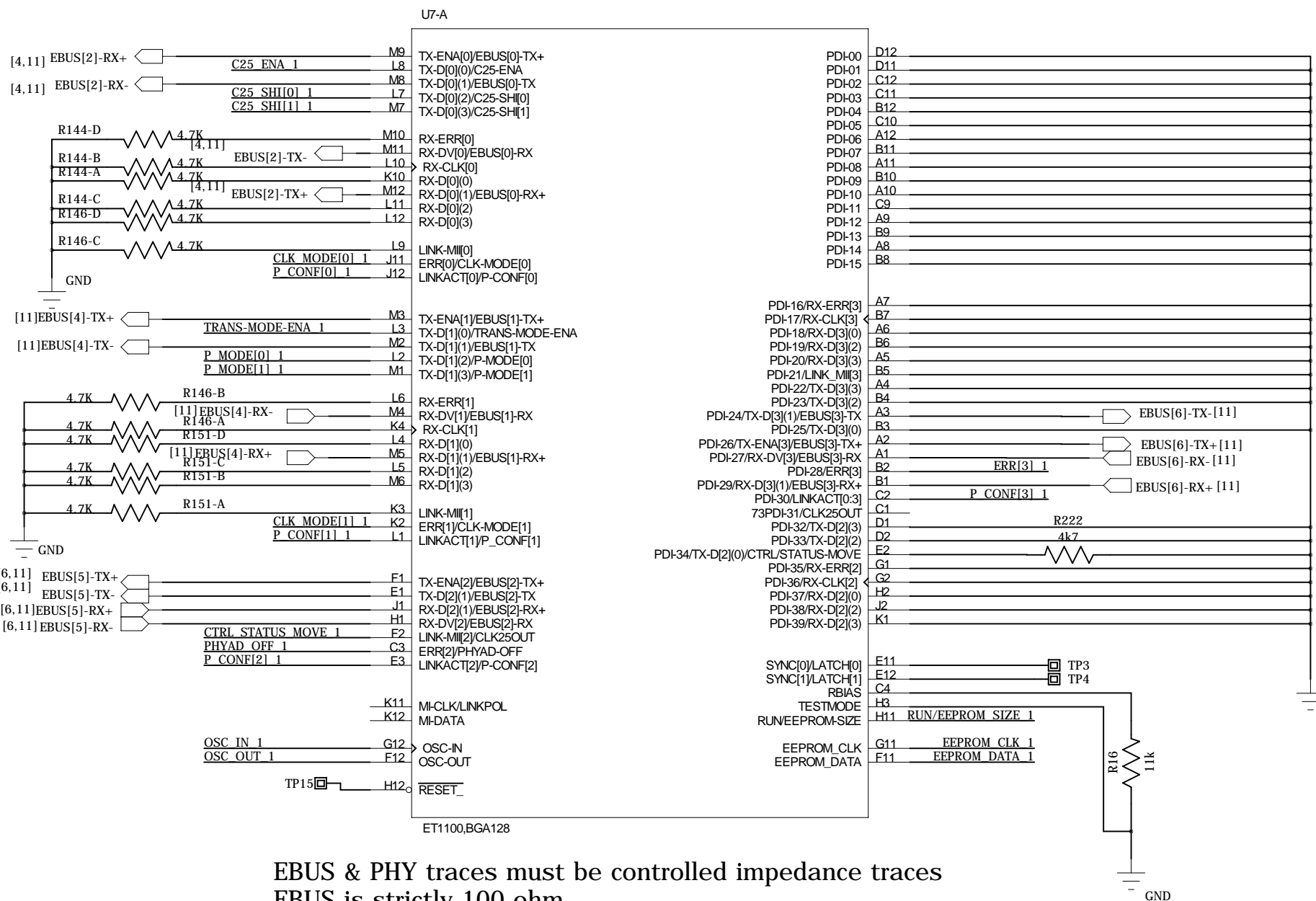
A

D

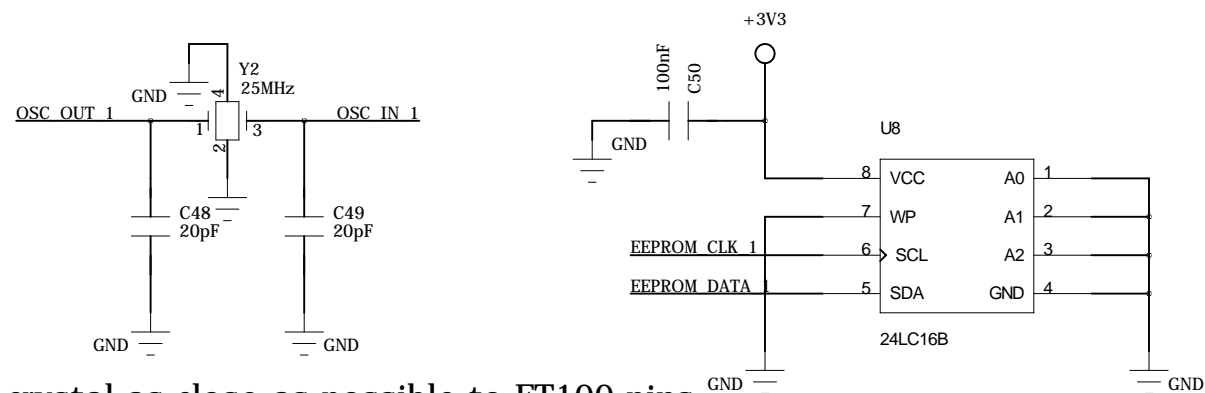
C

B

A



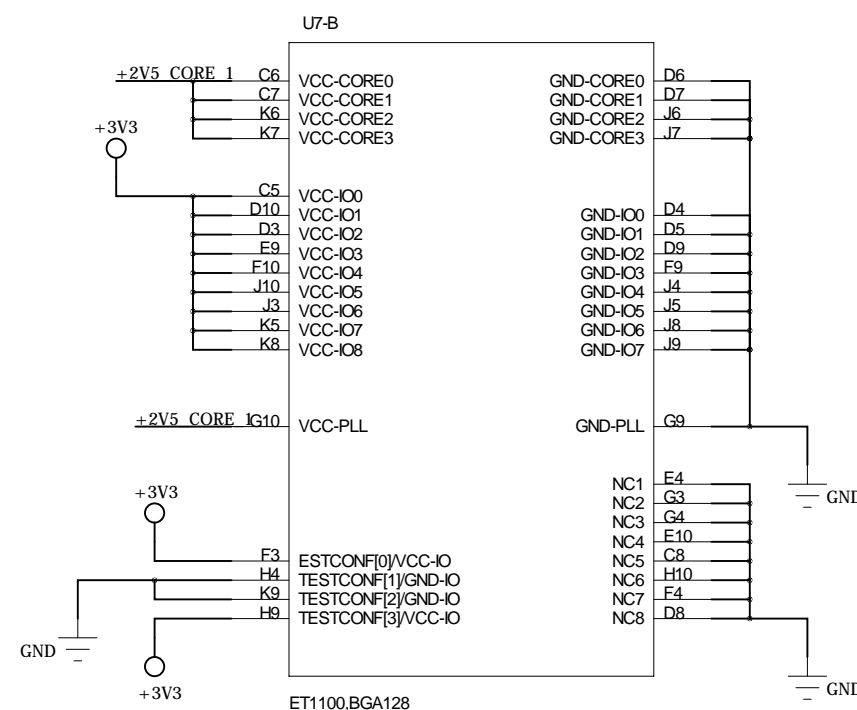
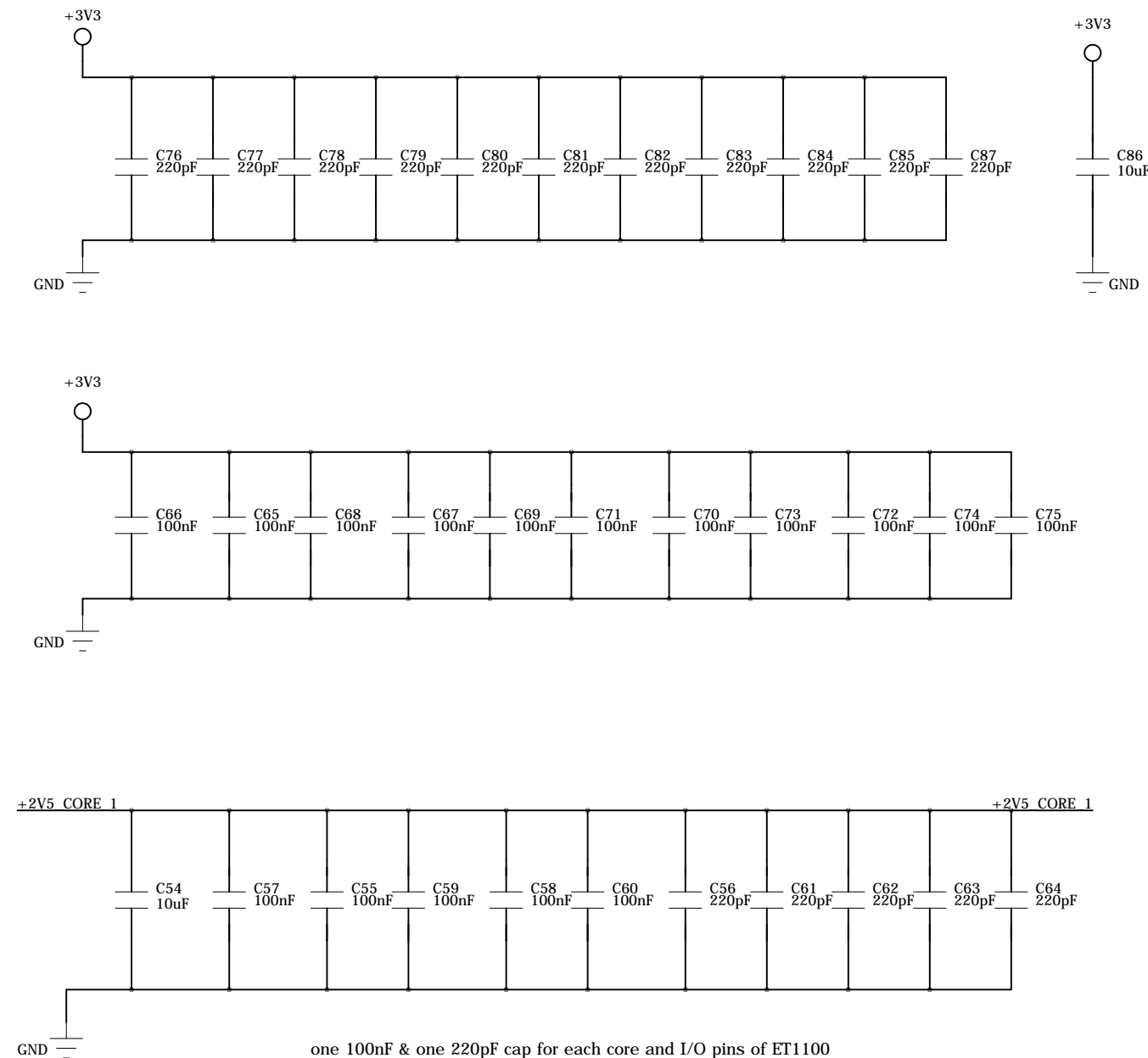
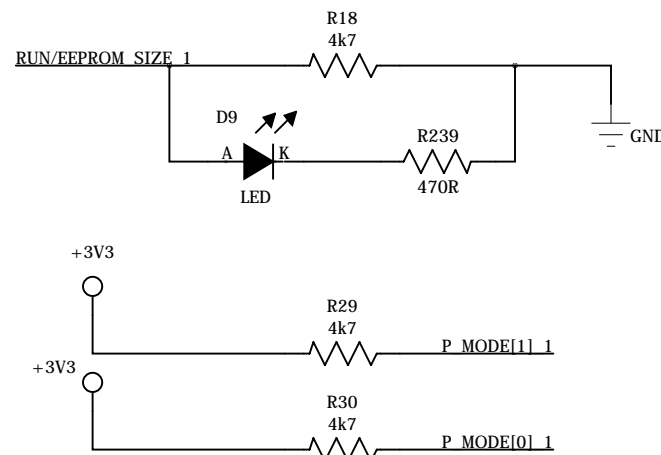
EBUS & PHY traces must be controlled impedance traces
EBUS is strictly 100 ohm
use 4 mil width traces for these signals



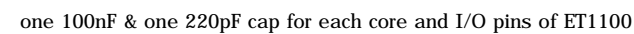
Place the crystal as close as possible to ET100 pins

Keep I2C lines as short as possible

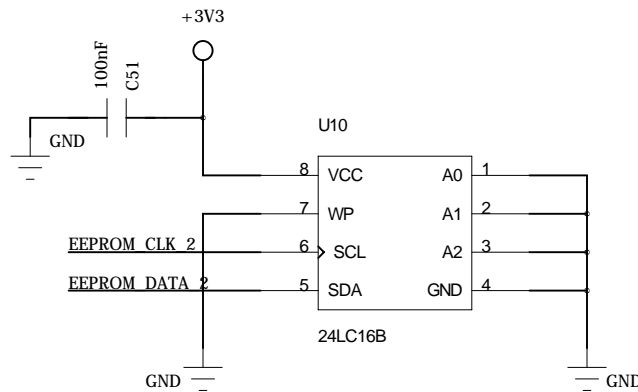
E²PPROM-Size = 0 (16 kBit)



APPROVALS		DATE	COMPRESSOR CONTROLS CORPORATION			
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CHECKED						
ENGINEER	Vijay		SIZE	DWG. NO.	SHEET	PROD REV.
			C		5 of 12	3.0
			FILE	18-xxxxxx-rev-2.0	SCALE	




EBUS & PHY traces must be controlled impedance traces
EBUS is strictly 100 ohm
use 4 mil width traces for these signals



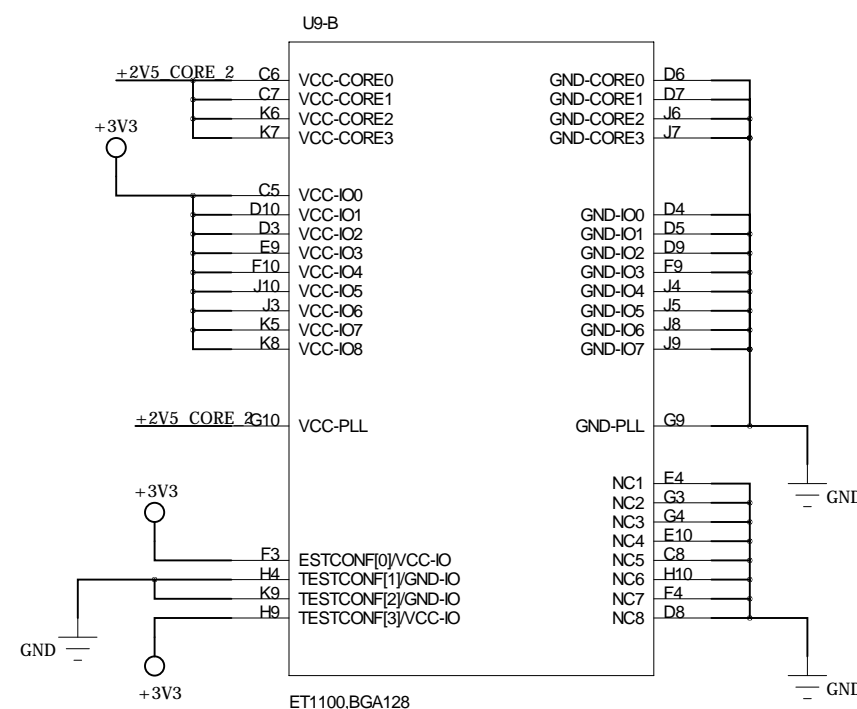
[6,12] P_CONF[3]_2

R60
4k7

← P_CONF[3]= 0 (Port3= EBUS)

ERR[3] 2  R44
4k7

CPU_CLK_MODE [1:0]=00=OFF
(config for PDI[7])



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CHECKED							
ENGINEER Vijay				SIZE <div>C</div>	DWG. NO. <div></div>	SHEET <div>6 of 12</div>	PROD REV. <div>3.0</div>
				FILE <div>18-xxxxxx-rev-2.0</div>	SCALE <div></div>		

D

C

B

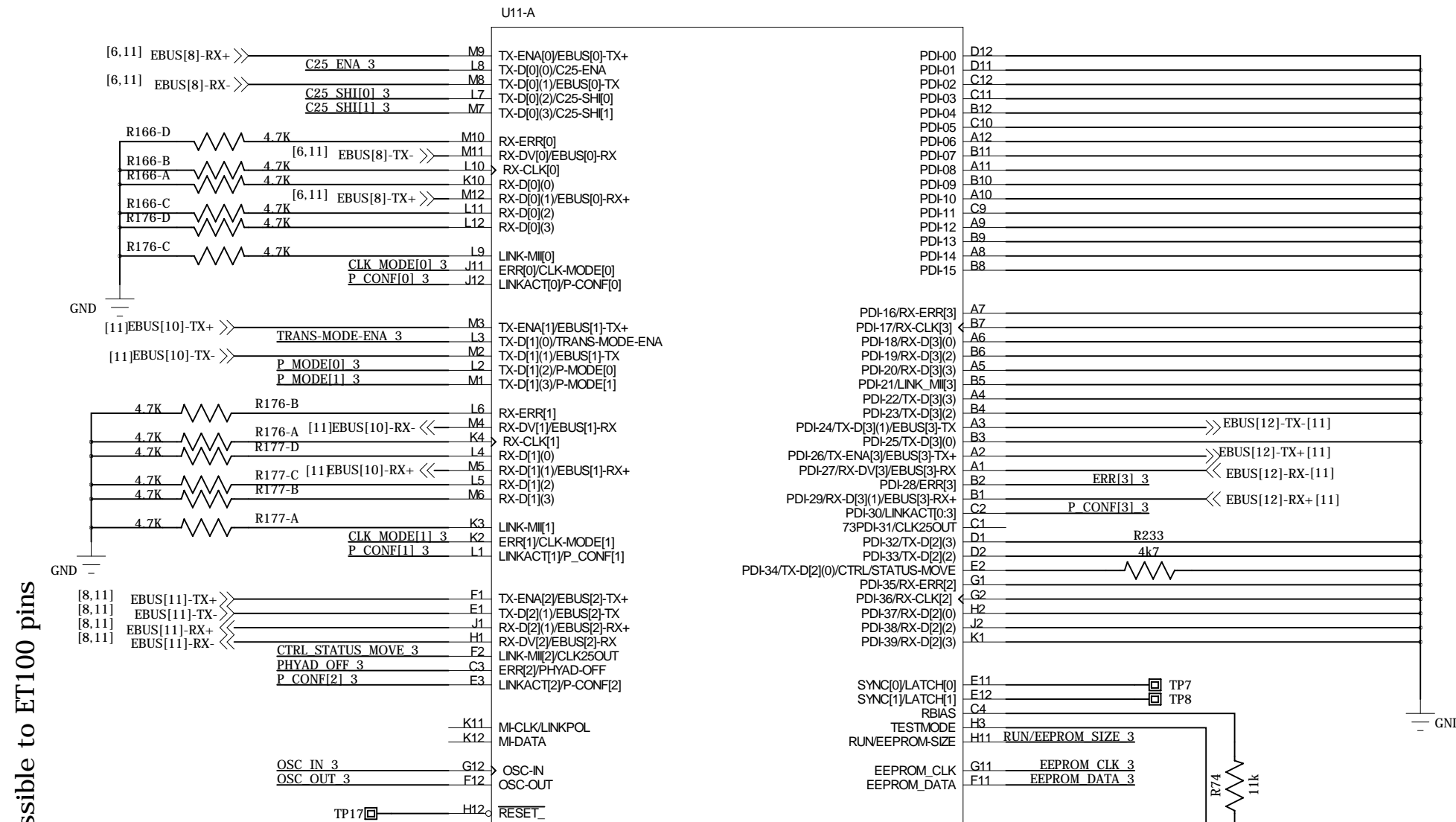
A

D

C

B

A

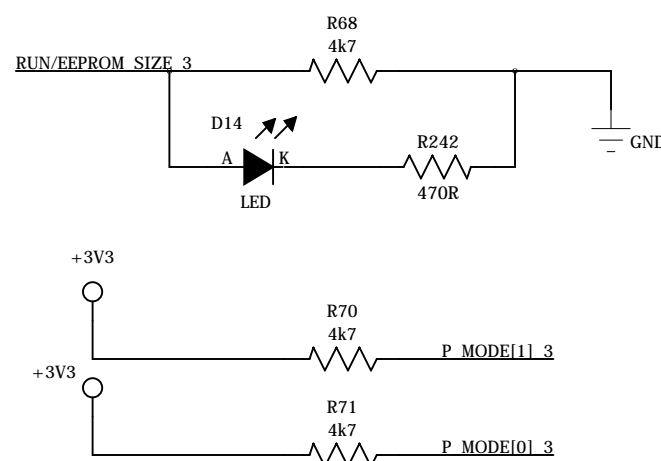


Place the crystal as close as possible to ET100 pins

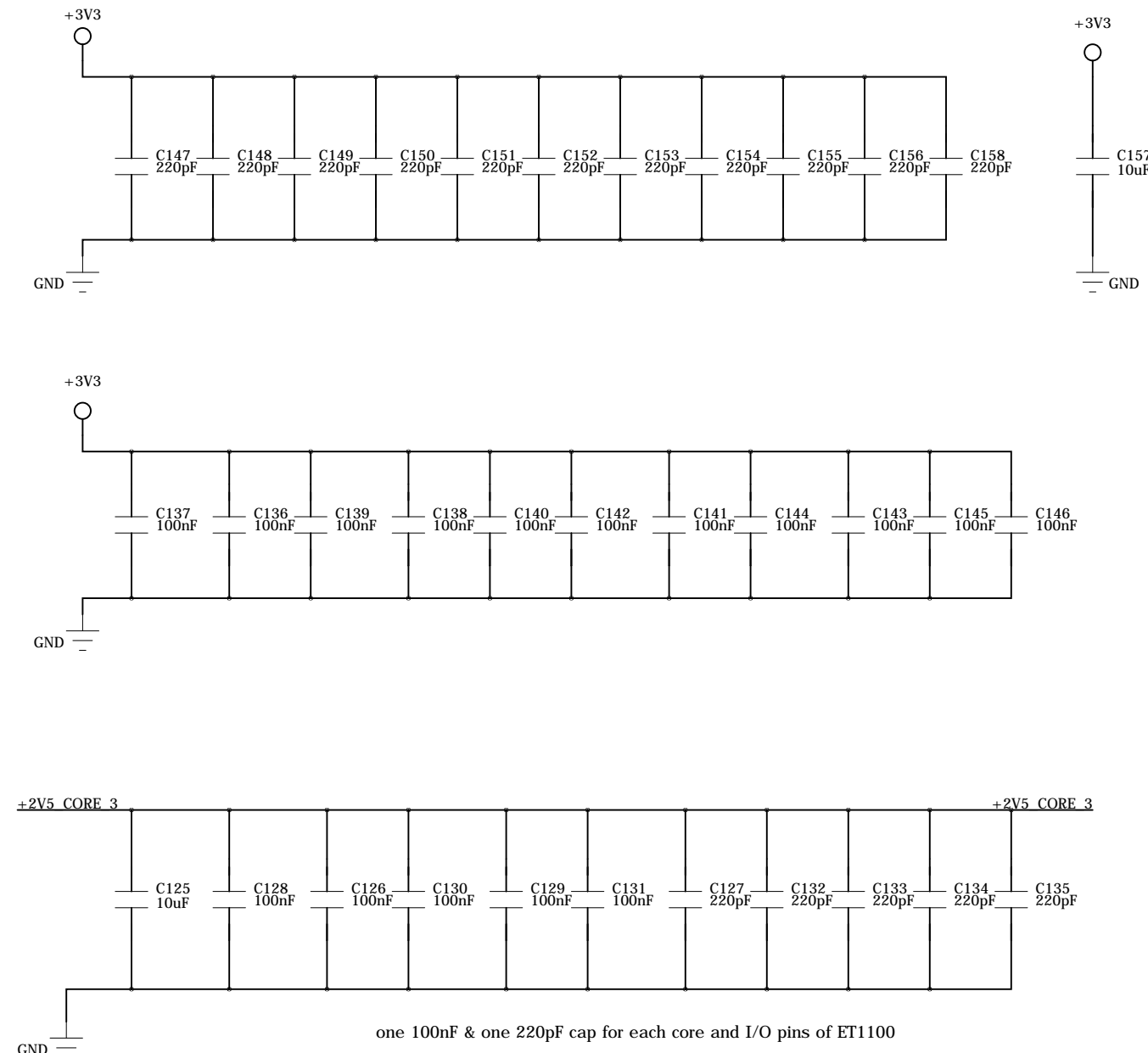
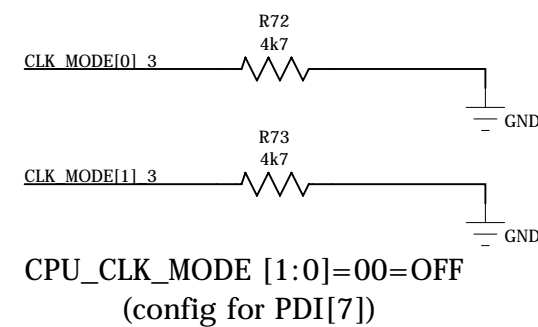
EBUS & PHY traces must be controlled impedance traces
EBUS is strictly 100 ohm
use 4 mil width traces for these signals

Keep I2C lines as short as possible

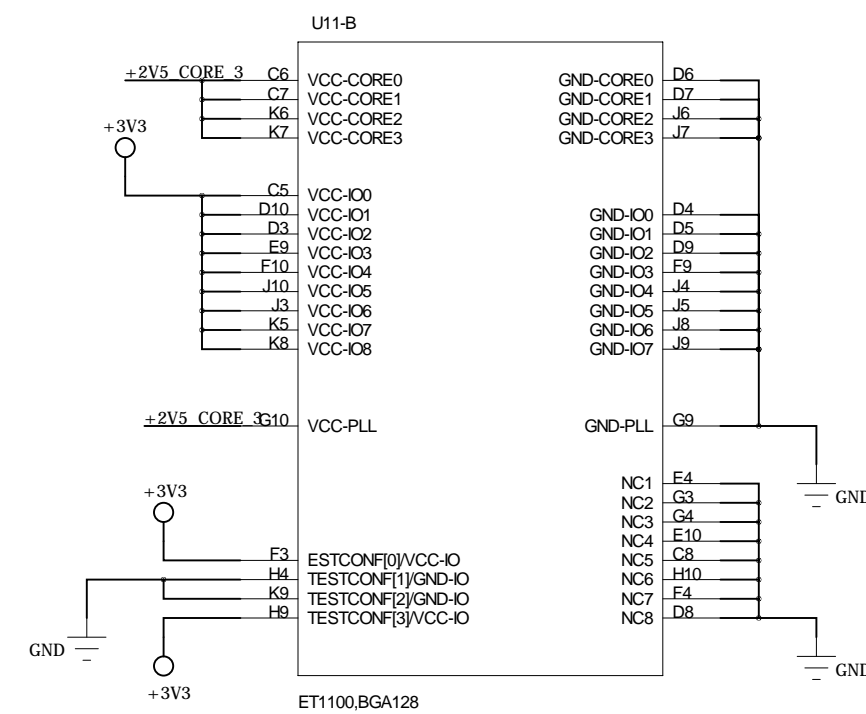
E²PPROM-Size = 0 (16 kBit)



4 EtherCAT Ports enabled (P_MODE[1:0] = 11)



one 100nF & one 220pF cap for each core and I/O pins of ET1100



APPROVALS		DATE	COMPRESSOR CONTROLS CORPORATION			
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ENGINEER	Vijay		SIZE	DWG. NO.	SHEET	PROD REV.
			C	FILE	7 of 12	3.0
				18-xxxxxx-rev-2.0		

D

C

B

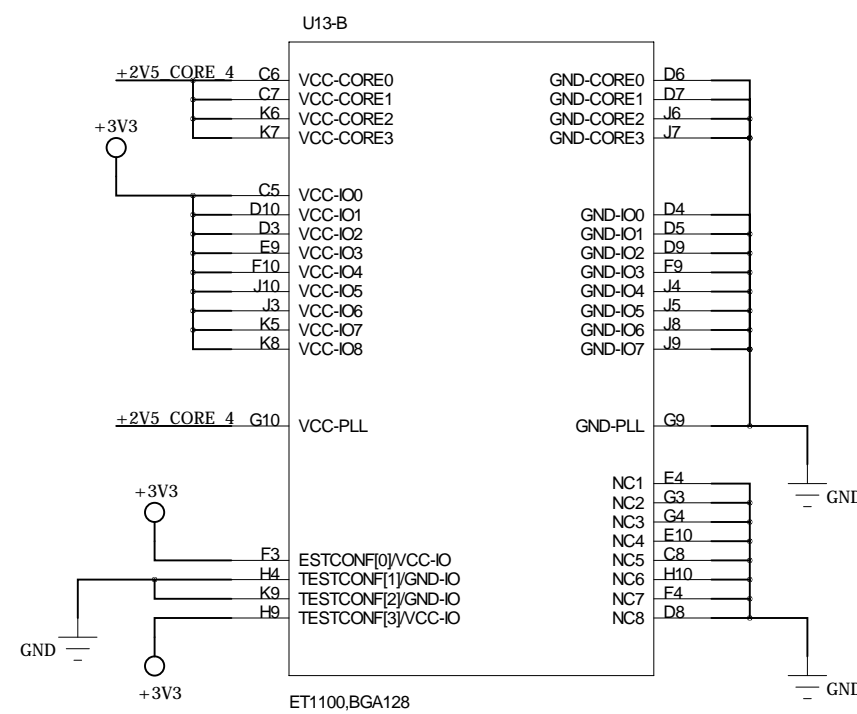
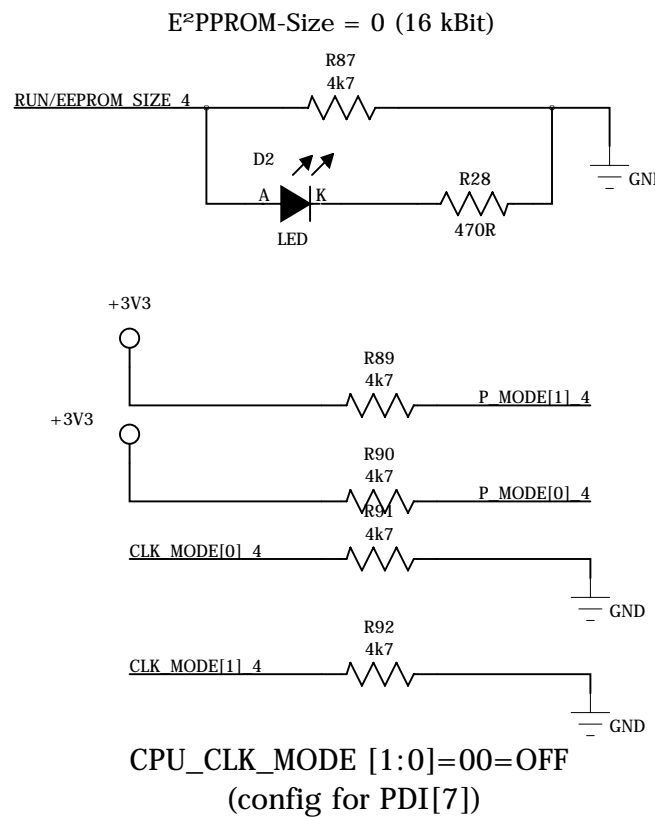
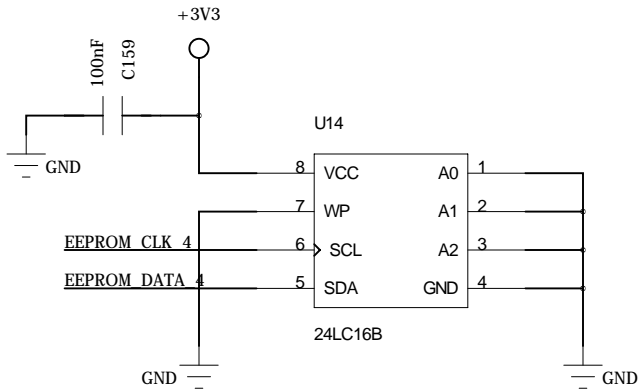
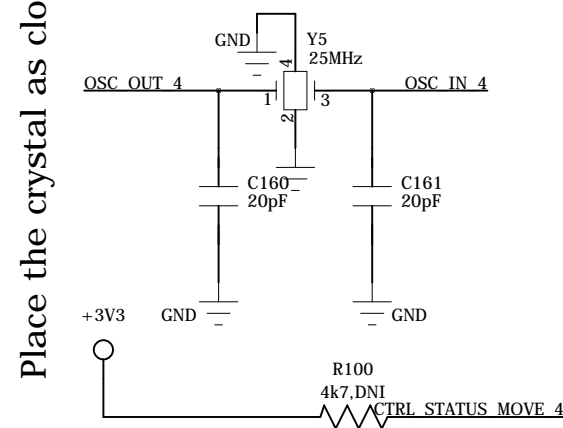
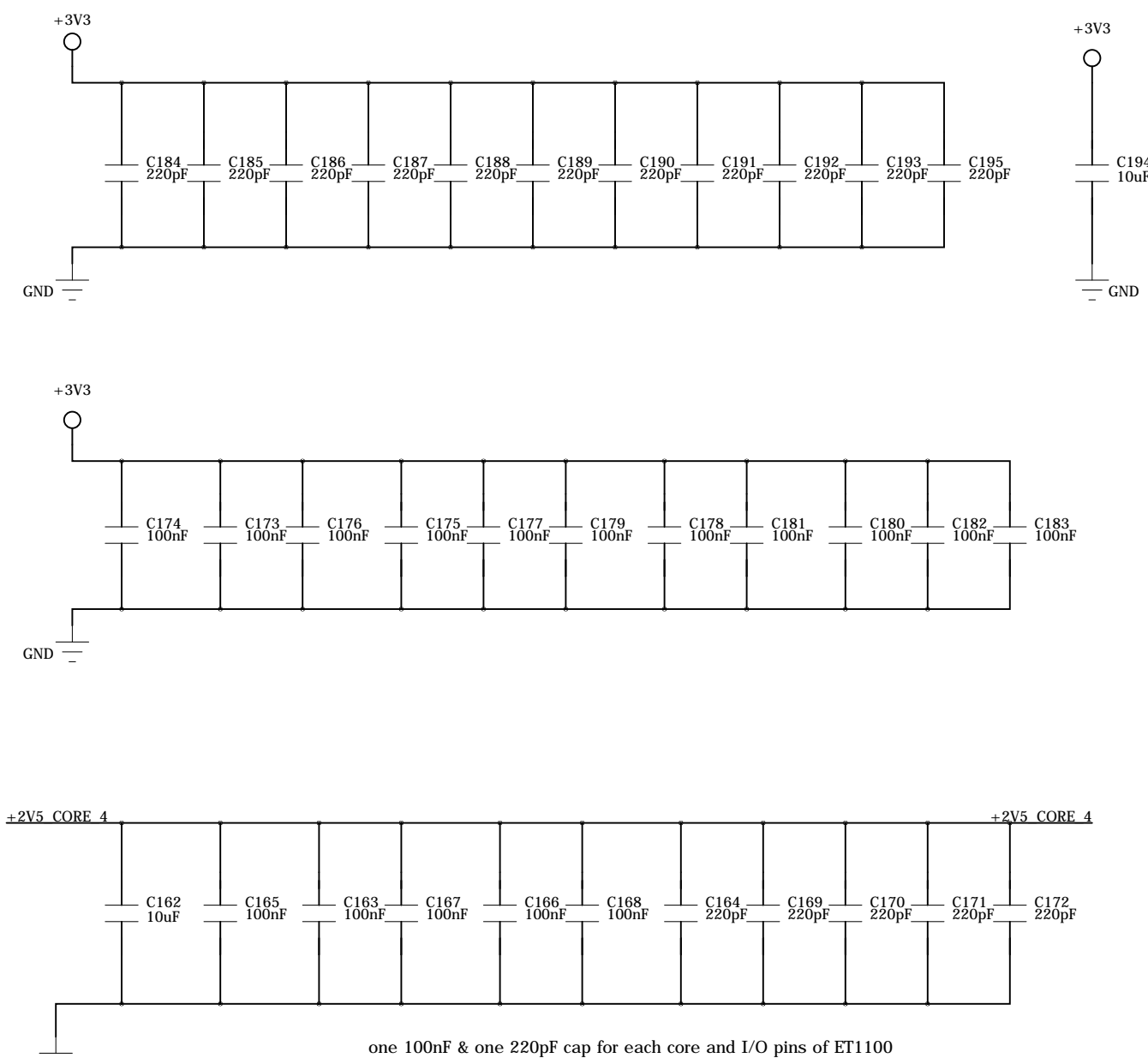
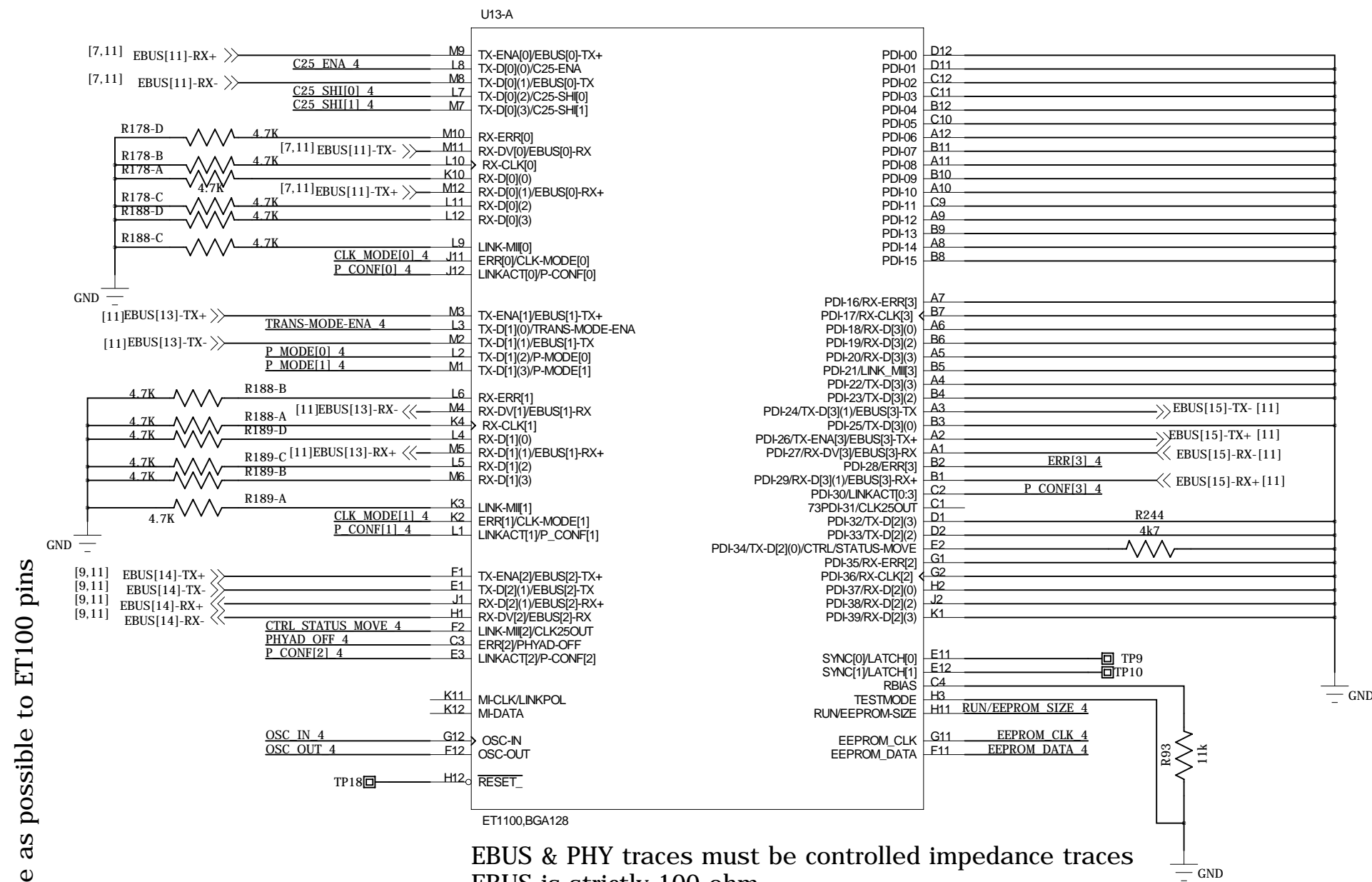
A

D

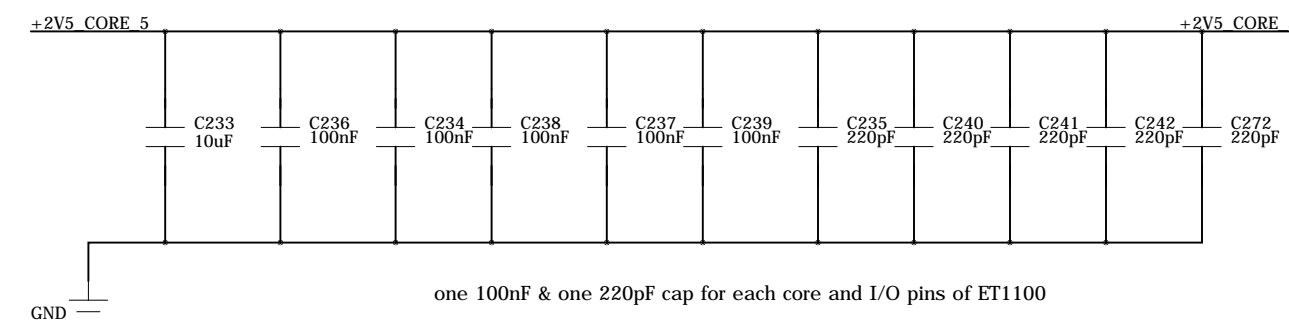
C

B

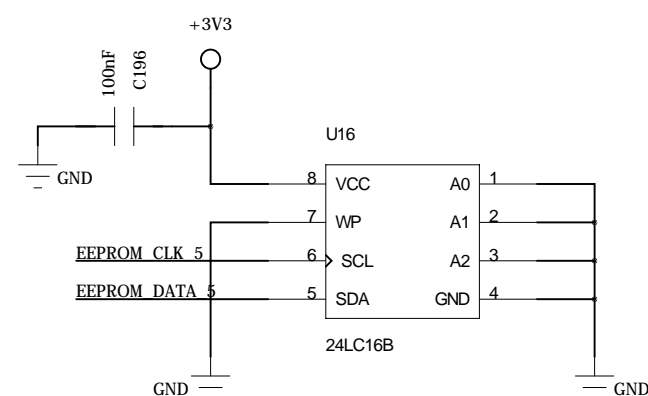
A



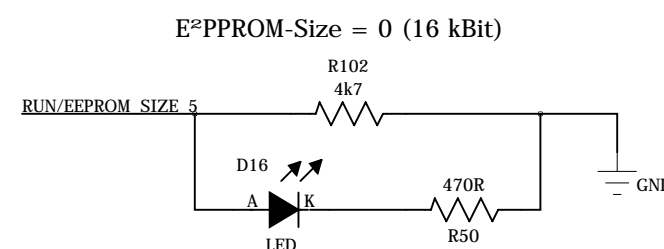
APPROVALS		DATE	COMPRESSOR CONTROLS CORPORATION			
DRAWN	Vijay	19 Sep 2011	4725 121st Street - Des Moines, Iowa 50323			
CHECKED						
ENGINEER	Vijay		SIZE	DWG. NO.	SHEET	8 of 12
			FILE	18-xxxxxx-rev-2.0	SCALE	PROD REV. 3.0



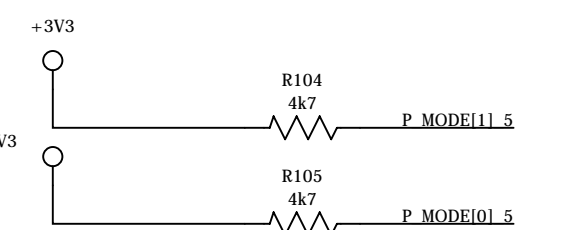
EBUS & PHY traces must be controlled impedance traces
EBUS is strictly 100 ohm
use 4 mil width traces for these signals



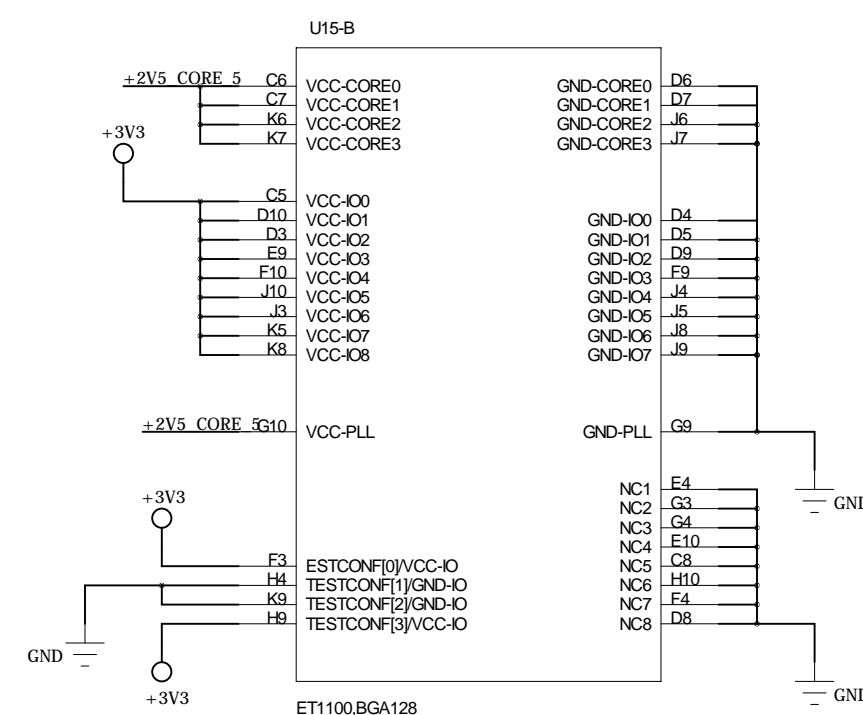
Keep I2C lines as short as possible



E²PPROM-Size = 0 (16 kBit)



CPU_CLK_MODE [1:0]=00=OFF
(config for PDI[7])



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ENGINEER Vijay				SIZE C	DWG. NO. FILE 18-xxxxxx-rev-2.0	SHEET 9 of 12	PROD REV. 3.0

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DWG. NO.

SH

REV.

D

C

B

A

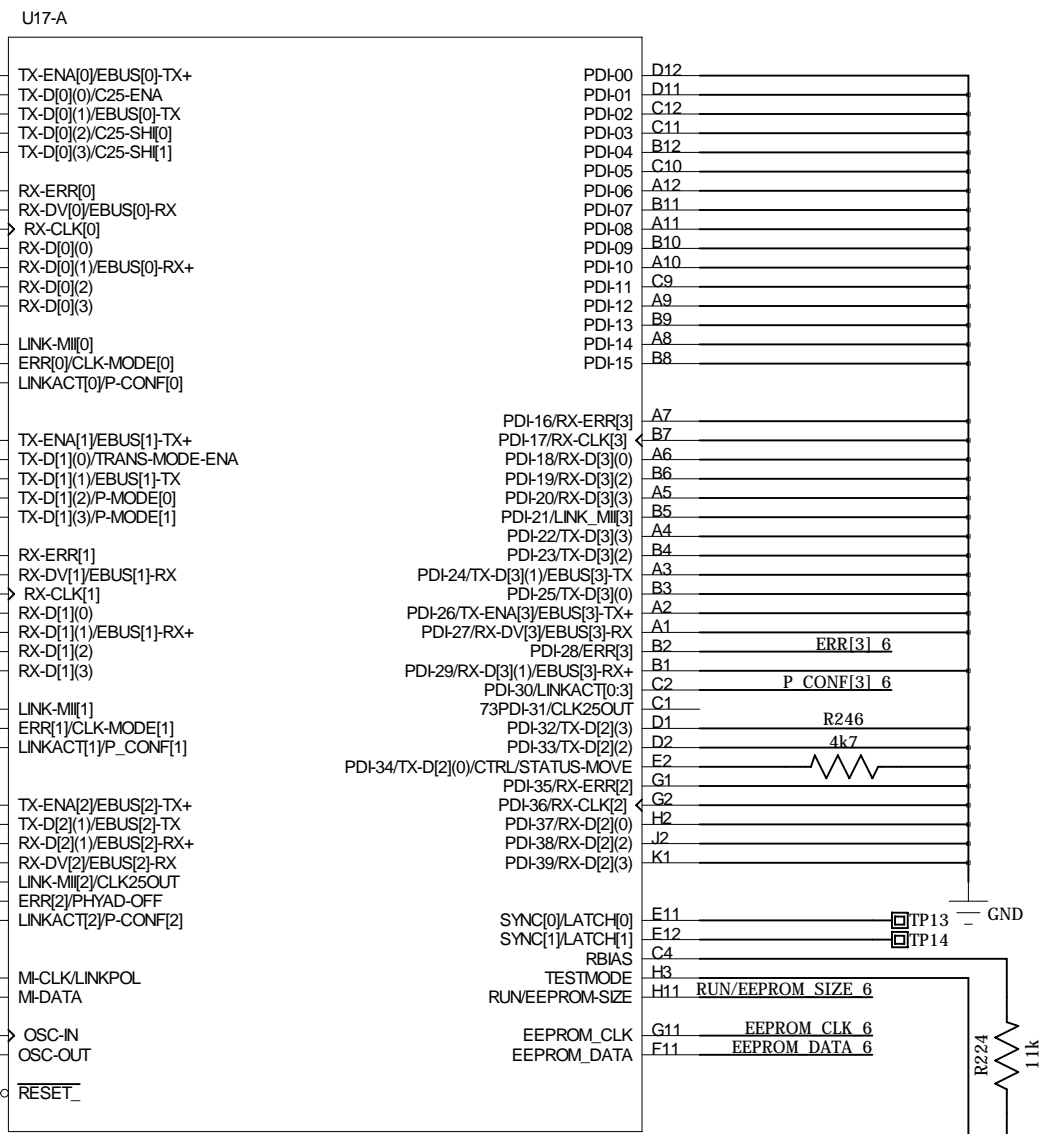
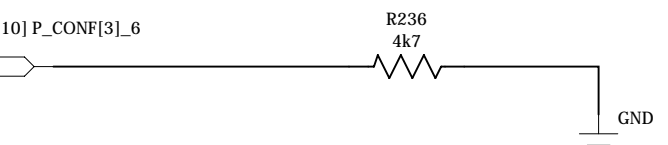
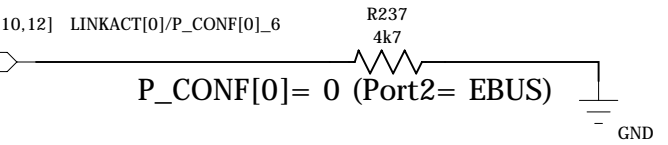
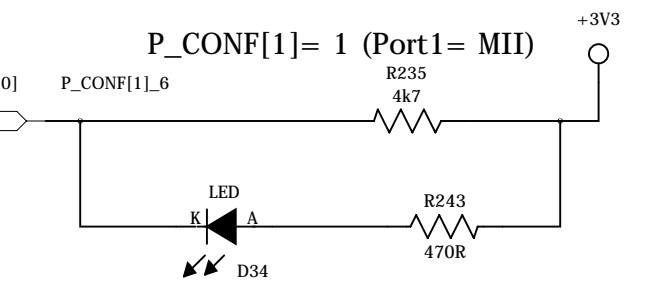
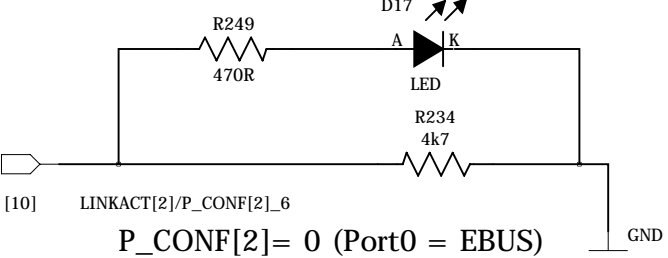
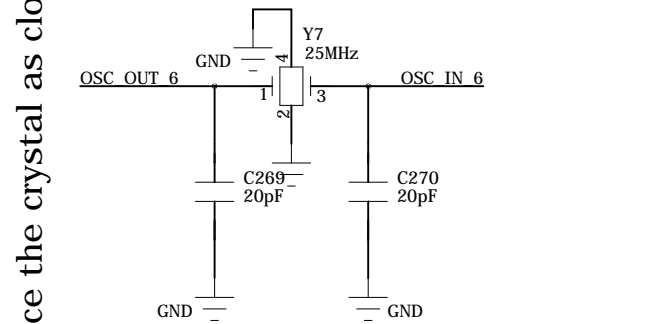
D

C

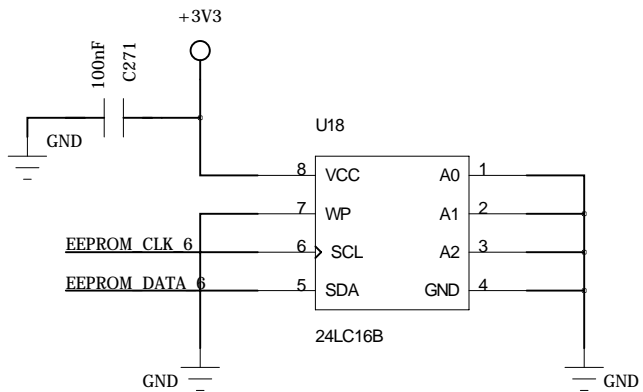
B

A

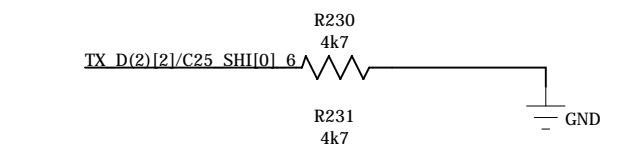
Place the crystal as close as possible to ET100 pins



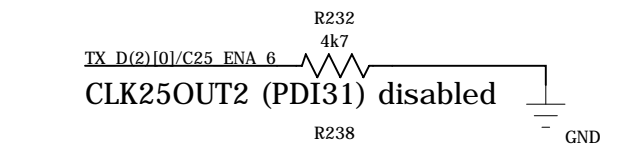
EBUS & PHY traces must be controlled impedance traces
EBUS is strictly 100 ohm
use 4 mil width traces for these signals



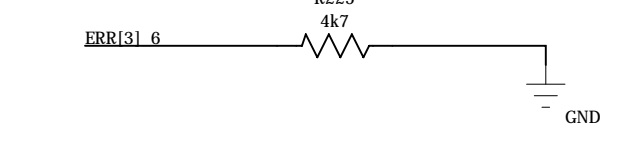
Keep I2C lines as short as possible



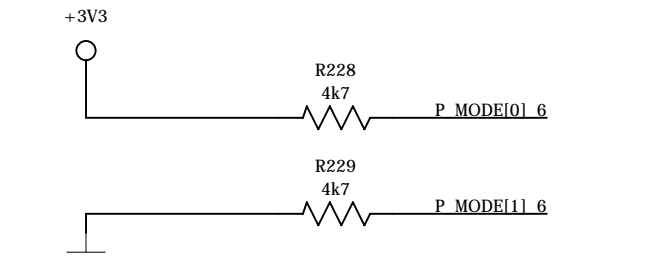
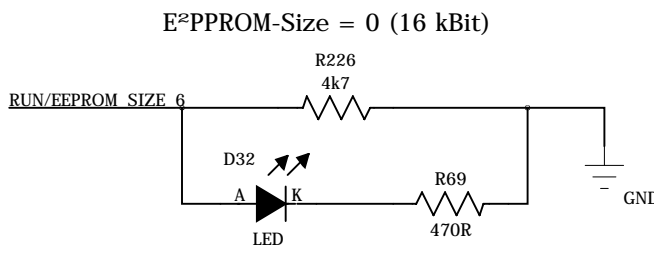
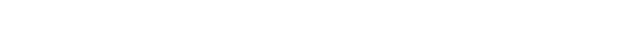
TX Shift [1:0]=00=0nS
MII TX signals delayed by (0 ns for KS8721BL)



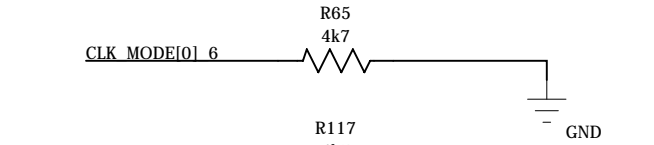
CLK25OUT2 (PDI31) disabled



Transparent Mode disabled (TRANS_MODE_ENA = 0)



3 EtherCAT Ports enabled (P_MODE[1:0] = 01)



CPU_CLK_MODE [1:0]=00=OFF
(config for PDI[7])



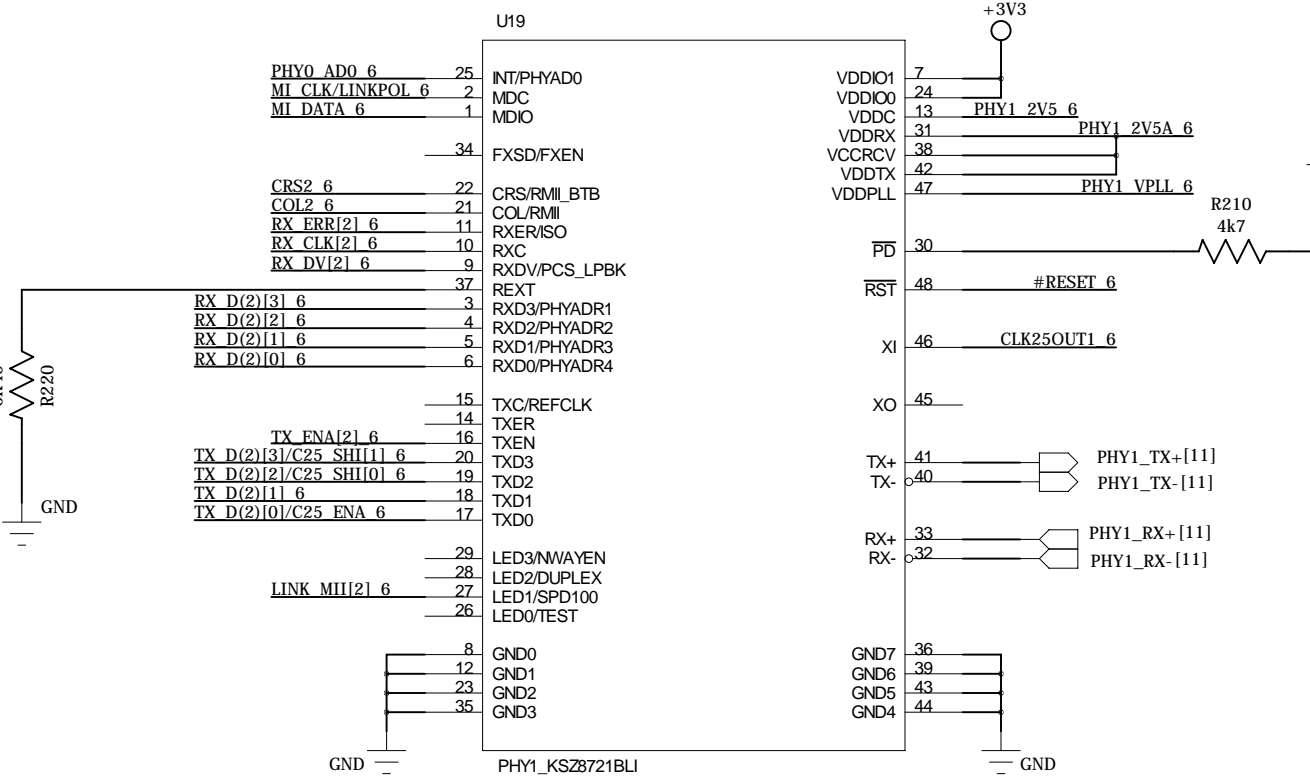
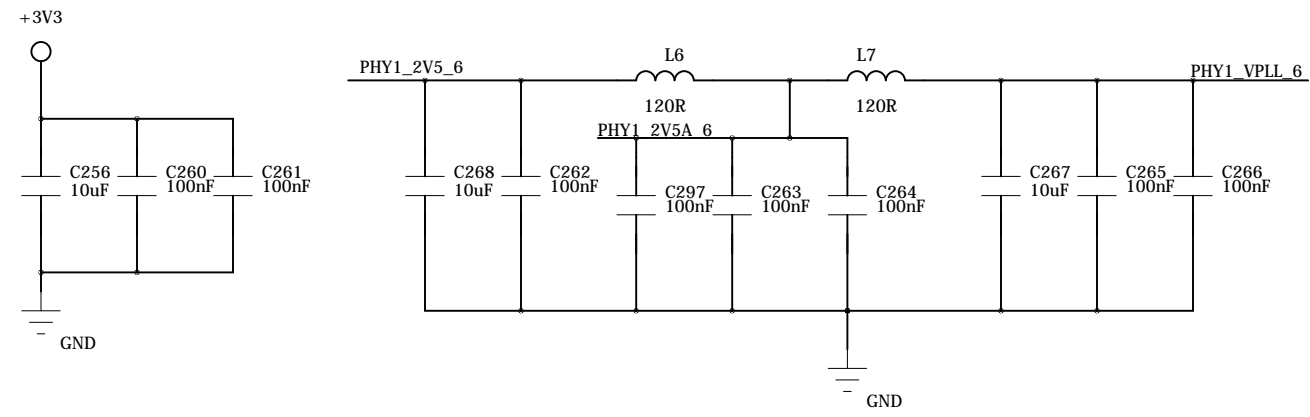
PHYADDRESS = 00001

RMII back-to-back disabled
RMII disabled

ISOLATE Mode disabled
PCS_LPBK disabled

Link Polarity = 0

PHY Address Offset = 0





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ENGINEER Vijay				SIZE C		DWG. NO. FILE 18-xxxxxx-rev-2.0		SHEET 11 of 12		PROD. REV. 3.0	

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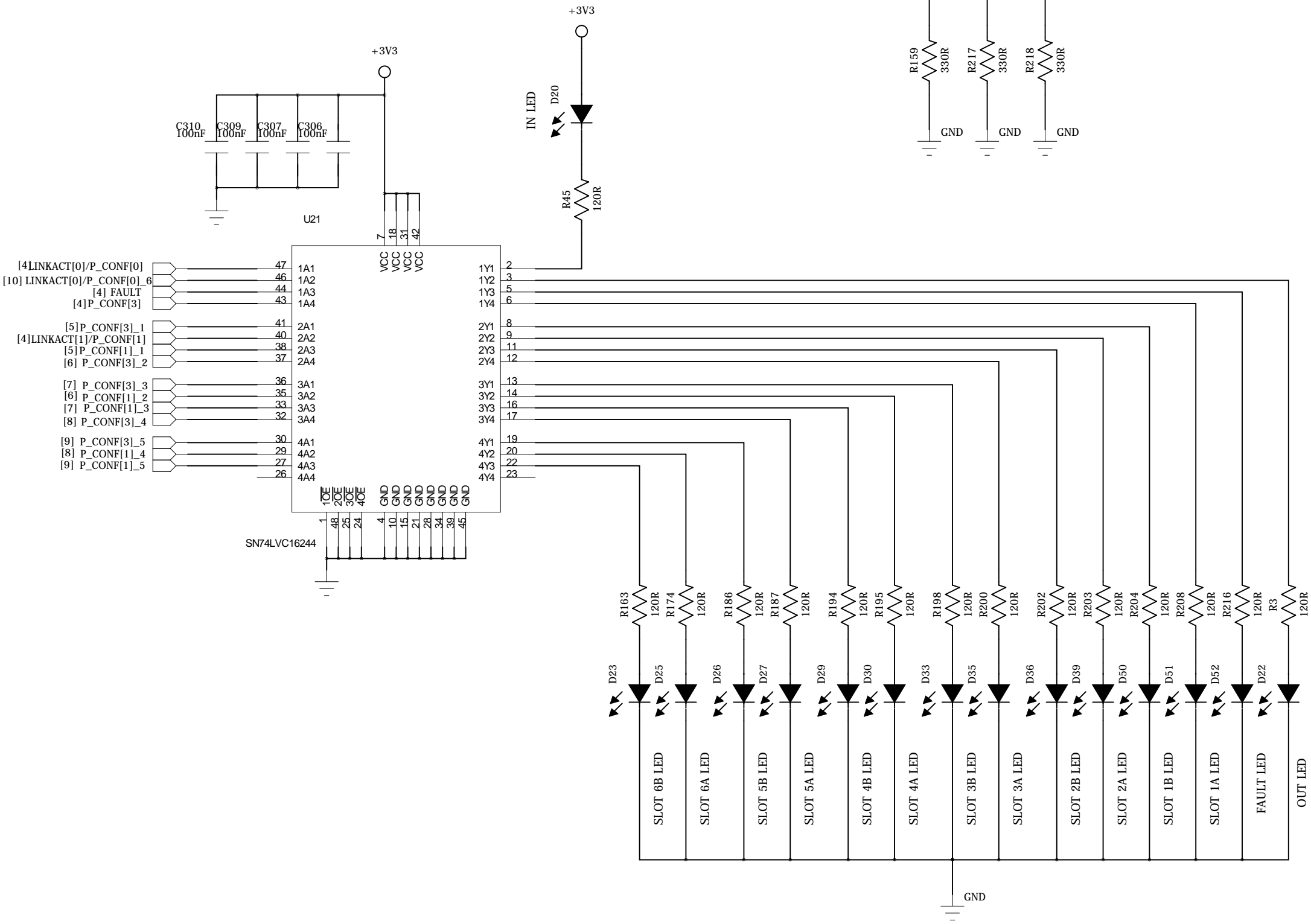
DWG. NO.

SH

REV.

BUFFER for Front panel LEDs

LEDS for LOGO



APPROVALS		DATE	COMPRESSOR CONTROLS CORPORATION			
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ENGINEER	Vijay		SIZE C	DWG. NO. FILE 18-xxxxxx-rev-2.0	SHEET 12 of 12 SCALE	PROD REV. 3.0