MII Interface Operation

The MII (Media Independent Interface) operates in either a MAC or PHY mode. In the MAC mode, the KS8999 MII acts like a MAC and in the PHY mode, it acts like a PHY device. This interface is specified by the IEEE 802.3 committee and provides a common interface between physical layer and MAC layer devices. There are two distinct groups, one being for transmission and the other for receiving. The table below describes the signals used in this interface in MAC and PHY modes.

PHY Mode Connection			MAC Mode Connection	
External MAC Controller Signals	**KS8999 PHY Signals**	**Description**	**External PHY Signals**	**KS8999 MAC Signals**
MTXEN	MTXEN	Transmit enable	MTXEN	MRXDV
MTXER	MTXER	Transmit error	MTXER	Not used
MTXD3	MTXD[3]	Transmit data bit 3	MTXD3	MRXD[3]
MTXD2	MTXD[2]	Transmit data bit 2	MTXD2	MRXD[2]
MTXD1	MTXD[1]	Transmit data bit 1	MTXD1	MRXD[1]
MTXD0	MTXD[0]	Transmit data bit 0	MTXD0	MRXD[0]
MTXC	MTXC	Transmit clock	MTXC	MRXC
MCOL	MCOL	Collision detection	MCOL	MCOL
MCRS	MCRS	Carrier sense	MCRS	MCRS
MRXDV	MRXDV	Receive data valid	MRXDV	SMTXEN
MRXER	Not used	Receive error	MRXER	MTXER
MRXD3	MRXD[3]	Receive data bit 3	MRXD3	MTXD[3]
MRXD2	MRXD[2]	Receive data bit 2	MRXD2	MTXD[2]
MRXD1	MRXD[1]	Receive data bit 1	MRXD1	MTXD[1]
MRXD0	MRXD[0]	Receive data bit 0	MRXD0	MTXD[0]
MRXC	MRXC	Receive clock	MRXC	MTXC

Table 1. MII Signals

This interface is a nibble wide data interface and therefore runs at _ the network bit rate (not encoded). Additional signals on the transmit side indicate when data is valid or when an error occurs during transmission. Likewise, the receive side has indicators that convey when the data is valid and without physical layer errors.

For half-duplex operation there is a signal that indicates a collision has occurred during transmission.

There are three different MII interfaces for KSZ8999 as shown in Figure 1, 2 and 3.

Notes:

1. Both MTXC/MRXC are output clocks when KSZ8999 is PHY mode, these two output clocks are same phase so you can connect MTXC to MTXC and MRXC to MRXC without error.
2. Both MTXC/MRXC are input clocks when KSZ8999 is MAC mode.
3. There is no MRXER output signal from KSZ8999 because the switch is filtering out all error packets.
4. MTXC/MRXC, MCOL, MCRS are always output clocks/signals from PHY device to external MAC device.
5. MRXD[3:0] need external 1K pull-up for default MII setting because the MTXD[3:0] are internal pull-down pins.

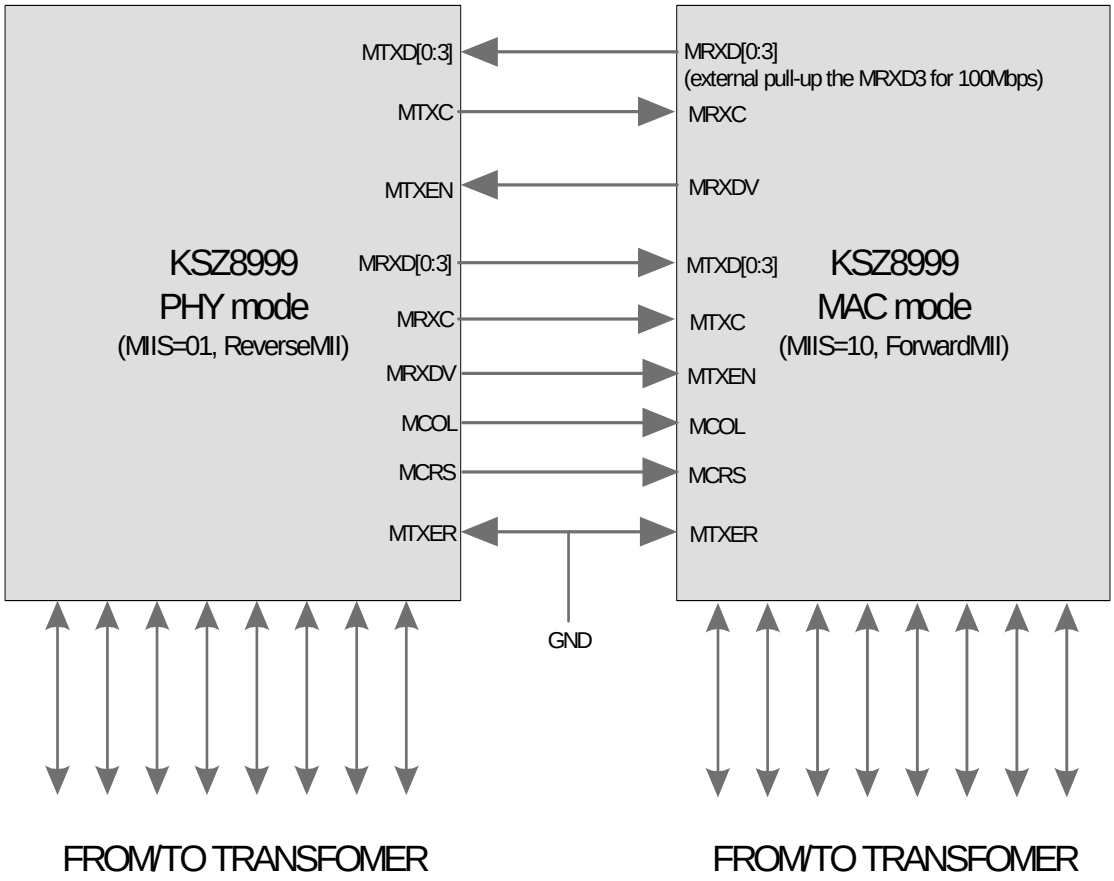

Figure 1: KSZ8999 MAC mode interfacing with KSZ8999 PHY mode

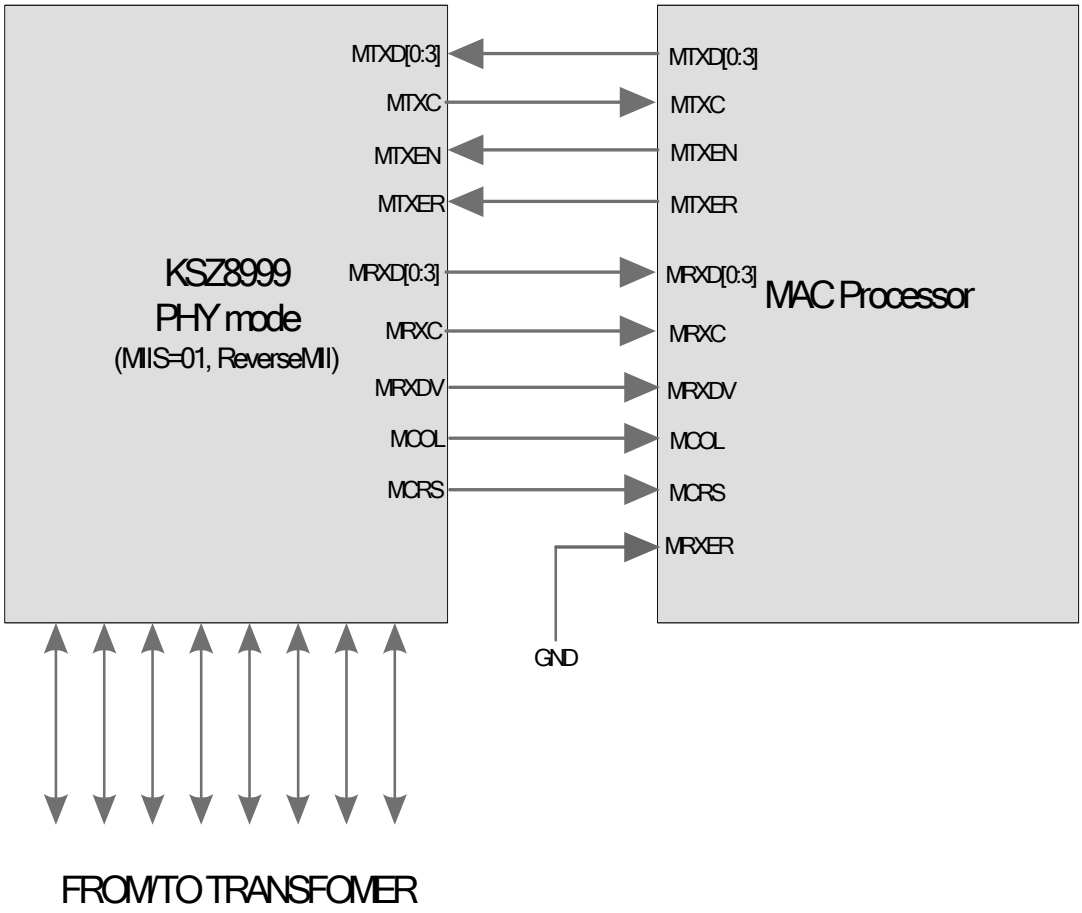

Figure 2: KSZ8999 PHY mode interfacing with External MAC Device

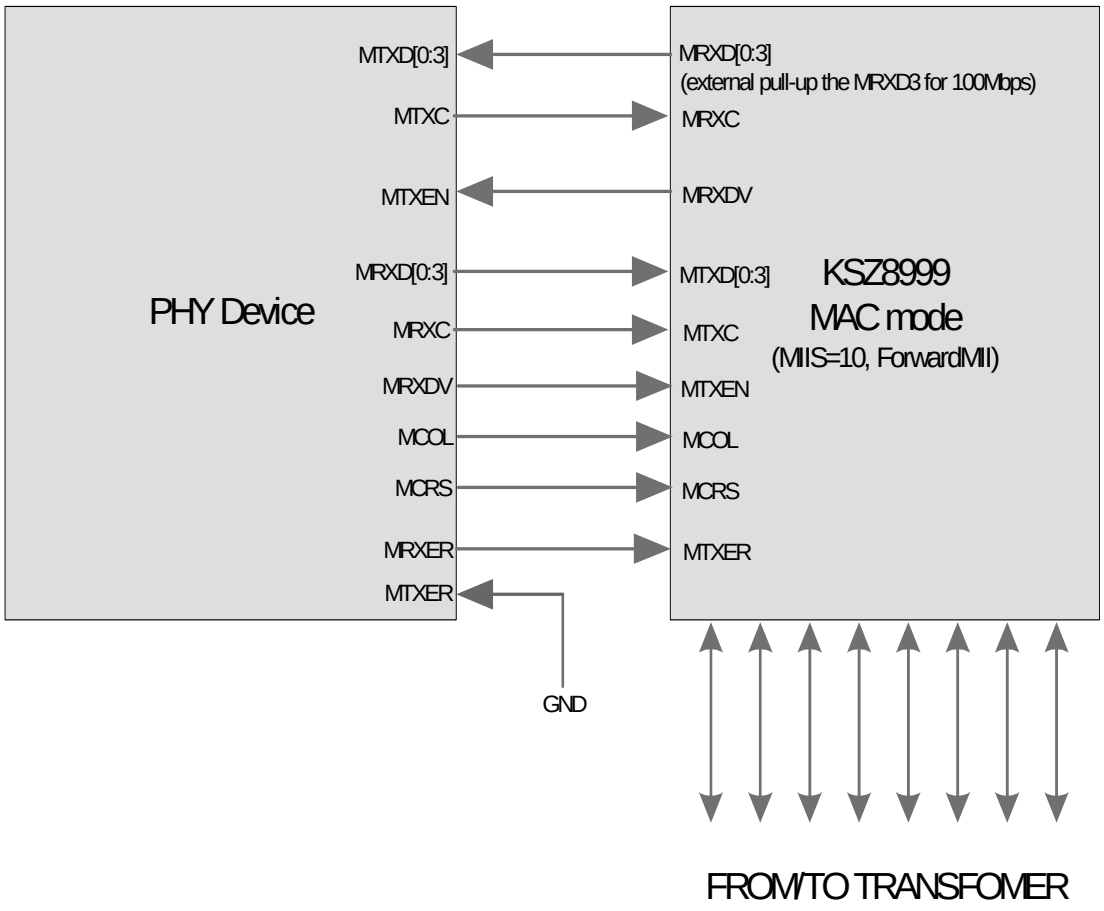

Figure 3: KSZ8999 MAC mode interfacing with External PHY Device