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Application Note

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Power Supplies on the MPC5500

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This application note documents proper use of the on-chip regulator controller and supply control on the MPC5500 devices.

Contents

1 Overview

MPC5500 Family microcontrollers (MCUs) use two supply rails — 5.0 V and 3.3 V. As silicon technology shrinks, the voltage required for the digital logic of the microcontroller (MCU) decreases. To maintain standard supply voltages and hence compatibility, MPC5500 devices include an on-board regulator controller for the core operating voltage. The 3.3 V ± 10% supply voltage remains, and the on-board regulator drops this to the core voltage, which is 1.5 V for today's devices and 1.2 V for future devices.

Most of the current for the device is drawn from the core supply. This current should be included in the capability for the 3.3 V power supply. For the higher performance MCUs, it is essential to share the power dissipation with an external transistor. Even when this is not necessary for power, it is more economical to use an external, standard, high-volume, discrete bypass transistor, rather than form that transistor on high-technology silicon.

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This application note describes the application of such an external transistor. The calculations given are examples, because the exact conditions are dependent upon the application.

Use of the on-chip voltage regulator controller (VRC) is not essential. A combination SMOS supply or standalone commercial single rail regulator, such as ON Semiconductor NCP1117DT15, may be used to source the 1.5 V core current. However, application of such supplies is the responsibility of the user. The monitoring and control features of the VRC can still be activated if the supply pin VRC33 is powered. Indeed, this is recommended, and thresholds discussed in this application note assume these monitors are in operation.

The various analog and digital circuits within the MCU place constraints on the power supply. The MPC5500 Family contains circuits to handle most of these constraints. This document also describes these characteristics and the remaining requirements that are placed on the supply.

2 Requirements

2.1 Sequencing

The MPC5500 VRC33 circuits eliminate sequencing on the power supply rails. There are no time or voltage delta constraints on 1.5 V, 3.3 V, or 5 V power rails if the on chip VRC is used to control the 1.5 V supply. The supply monitor circuits are powered and enabled via VRC33. It is advised that this be connected to a 3.3 V supply even if the internal regulator controller is not being used. Failure to do so will result in sequencing requirements on the supply rails. See the device data sheet and reference manual for the sequencing requirements if the on-chip VRC monitors are not used.

If a pre-regulator is used to supply the external pass transistor of the VRC, it must be ensured that the pre-regulator is not powered up after the 3.3 V rail supplying VRCCTL. Whilst the pre-regulator is switched off and the 3.3 V rail is powered up, it is possible that the base drive current could rise to 40 mA and may feed back into the pre-regulator.

NOTE

Although the circuits are powered via VRC33, it does not matter when during power-up this pin receives power.

There is a possibility of increased current transient if VRC33 leads VDDSYN by more than 600 mV or lags by more than 100 mV. In a typical target system, these will both be connected to the same 3.3 V rail. However, unless the 3.3 V supply is clean, PLL jitter will be increased. Therefore, an RC filter is advised, with values set within the constraints of -600 mV and the rate of rise of the user's 3.3 V supply. Example RC values for the filter are as follows. For a rise time of 66 µs for the 3.3 V supply and using 47 ohms for R and 100 nF for C, VRC33 would be expected to lead VDDSYN by 240 mV. For the same rise time of the 3.3 V supply but using 10 ohms for R and 10 nF for C, VRC33 would be expected to lead VDDSYN by 5 mV. The VDDSYN current is typically approximately 11 mA, but see the device electrical specification for the maximum specification value.

If VRC33 lags VDDSYN, there is a possibility of internal power on reset (POR) circuit oscillation due to supply droop from the increase in current when the clocks start. In such cases, the supplies will recover, so this is advice only.

2.2 Pin State

Pin behavior during power-up is described below, expanded from Tables 5 and 6, “Power Sequence Pin States”, of the MPC5554 data sheet. Fast pins — bus, NEXUS, JTAG, and clocks — behave differently than medium and slow pins. Exactly which pins are fast is defined by a table (“MPC5554 Signal Properties”) in the MPC5553/5554 reference manual. This table also shows the weak pull resistors that apply during power-on reset (POR), and the pin state out of reset.

To find out which VDDE applies to which pin, refer to the table “MPC5554 Power/Ground Segmentation” in the MPC5553/5554 reference manual. X means “don’t care”, and LOW means less than the POR release threshold (see below).

Table 1. Power Sequence Pin States (Fast Pads)

VDDE	VDD33	VDD	pad_fc (Fast) Output Driver State	Comment
LOW	X	X	Low	Functional I/O pins are clamped to VSS and VDDE
VDDE	LOW	X	High	Pad driver with no input drives high
VDDE	VDD33	LOW	High-impedance	POR asserted.
VDDE	VDD33	VDD	Functional	No POR asserted.

Table 2. Power Sequence Pin States (Medium and Slow Pads)

VDDEH	VDD33	pad_mh/pad_sh (Medium and Slow) Output Driver	Medium and Slow Pads
LOW	X	Low	Functional I/O pins are clamped to VSS and VDDEH
VDDEH	LOW	High-impedance	POR asserted
VDDEH	VDD	Functional	No POR asserted

Although the MPC5554 does not care what the sequence of power rails is, the above means that the behavior of the bus pins differs depending on order. If VDDE2 appears last, then it will hold the bus low. If VDDE2 appears first, then the bus will drive high (also if VDD33 and VDDE2 appear together).

The medium and slow pads are either low or high impedance. They may change weak pull state at the point POR negates. The state of the WKPCFG determines the weak pull state of the eMIOS and eTPU pins at reset, however this does not apply to DSPI, eSCI or other slow/medium pins.

Table 3. WKPCFG Settings

WKPCFG	Description
0	Weak pull down applied to eTPU and eMIOS pins at reset
1	Weak pull up applied to eTPU and eMIOS pins at reset

2.3 Power-on Reset

MPC5500 devices contain power-on reset (POR) circuits. These circuits become active as soon as Vt for the FETs is present on VDDSYN (less than 0.7 V). The POR circuits drive reset internally until the release voltages on all the rails, 1.1 V minimum for the 1.5 V rail, and 2.0 V minimum for both 3.3 V and 5 V rails (MPC5554). This ensures established logic supplies, and the ability to read pins such as CONFIG and external reset (RESET). It does not ensure full logic operation and does not provide brown-out protection. Hence, the target system supply monitoring and external reset must be active by 2.0 V, including any ramp/filter delays. The logic switch threshold on the RESET pin is a ratio of the supply voltage and can be pulled to 3.3 V or 5 V. RESET must be held until the supplies are within operating tolerance. VDDEH supplies must be between 3.0 V and 5.25 V. The VDDE supplies must be between 1.62 V and 3.6 V. The 3.3 V supplies must be between 3.0 V and 3.6 V. VDD must be between 1.35 V and 1.65 V. From a functional point of view, this can be achieved by design rather than monitoring.

It is recommended that all 3.3 V pins on the MCU are supplied from the same module power source, since the POR circuit monitors only the VDDSYN supply and one of the other 3.3 V supplies. The other circuits monitor VDDEH6 (Reset power) and VDD.

At the release of POR, CLKOUT, ENGCLK, and RSTOUT become driven. At this point, all configuration pins are sampled. The weak pull resistors may change state on some eTPU and eMIOS pins, depending upon WKPCFG.. The PLL might change mode of operation, depending upon PLLCFG and BOOTCFG.. The pins continue to be sampled until RESET is released by the target system, when their states are latched.

2.4 Ramp Rates

MPC5500 Family devices have a slew rate specification of 50 V/ms on the supply rails. This is to prevent triggering the ESD protection circuits on the pins, and applies during any phase of the ramp-up where more than about a diode drop is present. The specification equates to ramp duration of 30 µs, 66 µs, and 100 µs on the three supply rails from 0 V to operating voltage. In detail, however, only the highest rail has the rate limitation, and this applies up to the 5 V rail being established; for example, if the 3.3 V rail rises first, it has a 50 V/ms limit. The 5 V rail then has no limit until it is above the 3.3 V rail, after which the 50 V/ms limit applies again.

This relatively slow rise time is contrary to the operation of a power supply, where the control loop should be as fast as possible to maintain good regulation and minimize bypass capacitor size. With the drive to minimize capacitor cost, along with increased current drive for faster MCUs, it is possible that uncontrolled supplies may not achieve this specification. Some initial ramp control may be required. Freescale SMOS switching supplies achieve slow rise ramps using a state machine to step the voltage.

2.5 MCU Current

2.5.1 IDD Overview

The core regulator must be able to supply sufficient current to the MCU. The prime drivers of IDD are the amount of logic on the MCU and the rate at which it is clocked. Some modules, such as cache, take a lot of current; others, such as flash, take little. Power saving features such as module disabling and dynamic clock tree switching also affect the current depending upon how the application uses the chip. The smallest MPC5500 Family member takes only 1/5th the current of the highest performance device, and even in typical configurations, the current on one device can vary ±30% depending upon use. Thus, it is necessary to determine the current based on each application. During development, and if spare channels are available, it might be prudent to monitor supply voltages with the ADC for both capability and noise.

A secondary driver of MCU current is core voltage. Control of the core voltage to a tolerance better than the permissible ±10% can be used to reduce the maximum expected current (by around 100 mA on the MPC5554).

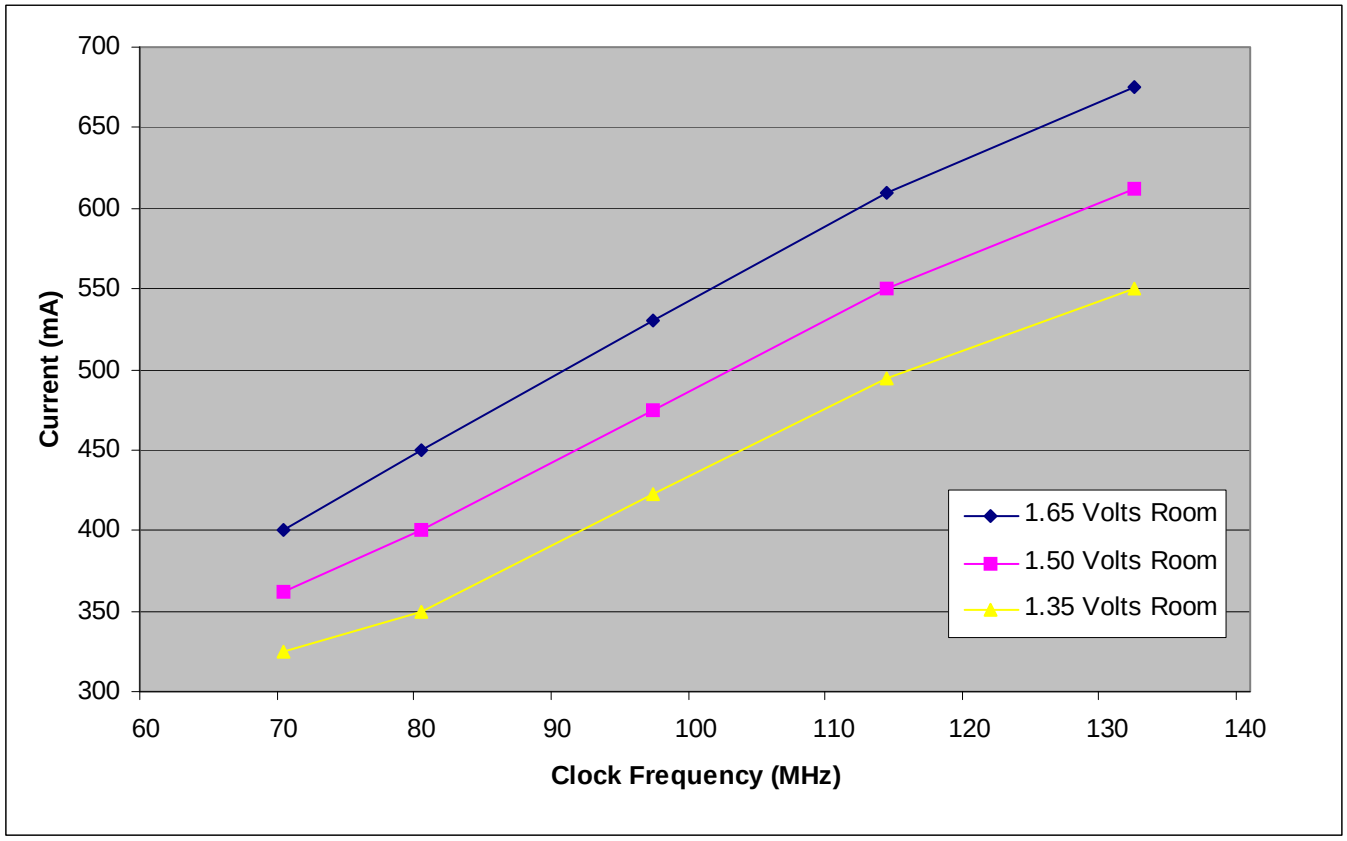

Figure 1. MPC5554 Example V_{DD} Current

NOTE

External loads such as the external bus and NEXUS can be significant, and should be considered in the capability of the target system power supply if this is to supply these features.

2.5.2 Typical and High Use Current

The MPC5554 data sheet identifies two classes of measurements for current on VDD. These are measured using two different routines, which exercise different functions of the MCU based on Powertrain software. This is split into Typical and High use, which exercise the various function of the MCU to a different extent. The code is based on Powertrain software, and the typical use current reflects that for a typical Powertrain application.

Typical Use IDD:

- Cache is enabled in copy-back mode and estimated to have a 10-15% miss rate. BTB turned off, with code performing filters and table lookups.
- No floating point or SPE code was used.
- eTPU running 1 KHz PWM operations on all 64 channels staggered.
- eMIOS running 1 KHz PWM operations on all 24 channels staggered.
- DMA accessing all memories and peripheral modules and generating interrupts.
- eQADC performing 8 conversions each time through IDD pattern loop.
- FlexCAN, SCI, DSPI, EBI not used.

High Use IDD:

- Cache is enabled in copy-back mode with a 0% miss rate. Code chosen is a 2D table lookup with all code and data locked in the cache.
- Code was assembly language using SPE instructions and all stalls from pipeline were attempted to be removed.
- Peripherals run without CPU intervention to allow core to maintain high current condition.
- eTPU running 1 KHz PWM operations on all 64 channels at the same time.
- eMIOS running 5 MHz PWM operations on all 24 channels at the same time.
- DMA moving 128 bytes of data from RAM to RAM constantly by linking to itself.
- eQADC performing 8 conversions each time through IDD pattern loop.
- FlexCAN, SCI, DSPI, EBI not used.

2.6 VDD33 Current

The use of two standard rails, 5 V and 3.3 V, permits the use of existing supply ICs. However, for the higher performance MPC5500 devices, some existing power supply ICs will not have sufficient current capability to supply VDD via the VRC external transistor. It is permissible to use a switching supply as a pre-regulator to the collector of the bypass transistor. Due to the range of available supplies verification is the responsibility of the user, but voltage transients on the collector of 3.0 V to 4.5 V have been simulated on the recommended circuit. Users should verify correct range of the VRC with their chosen pre-regulator and ensure that sufficient smoothing is applied to prevent ripple pushing VDD out of operating limits. Also consider that the average voltage and thus power dissipation in the bipolar may be higher, and that such a pre-regulator would not be covered by the VDD33 POR or other supply monitors.

Refer to Section 2.1, “Sequencing” if using a pre-regulator to supply the collector of the bypass transistor.

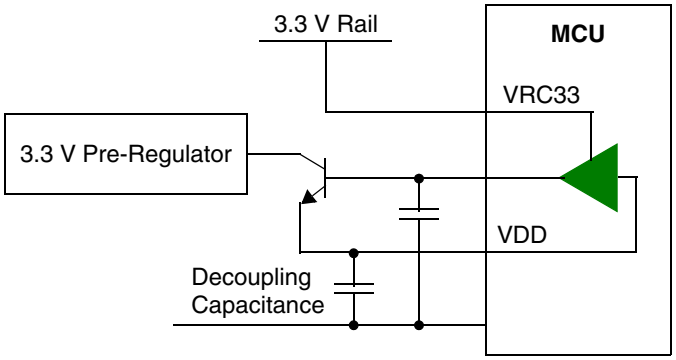

Figure 2. 3.3 V Pre-regulator Supplying VDD via Collector of VRC Transistor

NOTE

Voltage tolerance on VDD33 is ±10%, and all examples herein use 3.0 V as a worst case. However, available current increases if the VRC33 supply has a tolerance better than 10%.

2.7 Transient Current

2.7.1 Ramp Up

About 2/3 of the chip is clocking in reset, so it draws about 2/3 of the running current at the reset frequency (which is 1.5 times the crystal frequency) to avoid transients.

The application has significant control over transients. During ramp-up, it is not desirable to jump directly to full operating frequency. The frequency can be stepped, with delays to allow the power supply to settle. Transients can also be minimized by applying a specific order to enable the cache and set the operating frequency. The recommend procedure for enabling cache at start-up is to enable the cache at the MCU's default frequency, set the flash to cache inhibited using the MMU, ramp up the frequency to the full operating frequency, then finally set the flash to be cacheable. Further transient reduction steps are possible and will be the subject of a future application note.

2.7.2 Operation

The power supply must be able to handle any additional transient current during operation. This means it must possess sufficient gain on the transistor to supply the temporary current, as well as sufficient bulk storage on the bypass capacitors to supply transient current, up to the point where the regulator is able to respond. Transient magnitude depends highly upon use. Capability of the 1.5 V rail must be ensured by design, particularly if there is no external hardware monitor for supply brown-out on the 1.5 V rail.

2.7.3 Reset

Applications that might drive reset when the MCU is at full current must ensure that any voltage surge is within the absolute maximum voltage limits. Where the module controls its own power-off, the same techniques of system frequency stepping can be used to reduce negative current transients and subsequent voltage overshoot during power-down.

2.8 Power Down Monitors

To ensure predictable shut down, internal POR circuits drive reset as the supply voltage falls. This is not supply droop (brown-out) protection, because the thresholds are lower than the minimum guaranteed operation voltage. The 1.5 V VDD is least susceptible to voltage droops on the incoming supply that might cause brown-out, because it is the lowest voltage and internal. However, VDD is susceptible to brown-out due to overload because it carries a high level of current, and large transients can be forced upon it by the application. The on-chip regulator will hold it in range until the 3.3 V rail falls below specification — down to 3.0 V on the MPC5554.

The user should ensure the external reset is driven when the supply rails drop below guaranteed operating range (–10%), and that this is held until the POR circuits drive reset internally (guaranteed to happen by 2.0 V minimum on MPC5554). Reset will be held internally until less than about 1 V is present on VRC33.

NOTE

The POR monitor on the 5 V rail is set below 3.0 V as it is permissible for this supply to be between 3.0 V and 5.25 V. This is to permit supply droop during engine crank. The user should monitor the 5 V power supplying VPP and VDDA and cause an interrupt at 4.5 V, which can be used to suspend Flash writes (i.e., EEPROM emulation) and ADC reads. Except for VPP and VDDA, all of the 5 V (VDDEH) supplies can be run from 3.0 V to 5.25 V. The POR will not assert until 2.85 V maximum. If the 5 V supply returns to within range after the droop, Flash writes and ADC operation can resume. If the target system has other 5 V devices that will not operate through such a supply droop, then the 4.5 V level interrupt signal should be used to reset these devices.

2.9 Standby RAM Integrity

Systems that use standby RAM should ensure the integrity of contents during start up, in case loss of standby power has occurred whilst VDD was not powered. This can be achieved using a CRC check. However, such software takes time, and there are occasions when a reset has occurred but power was applied continuously to the MCU, i.e., a run-time reset. In such a scenario the integrity of the RAM is maintained and boot-up time can be shortened by skipping the CRC check. This can be done when the MPC5500 device registers a cause of reset that is NOT POR. Although this will work on most occasions, note that RAM integrity cannot be guaranteed without considering other methods of corruption. Other mechanisms for reset, such as watchdog or voltage supply monitor, infer possible errant software operation and might also have resulted in RAM corruption.

3 Core Regulator Design

3.1 Circuit Architecture

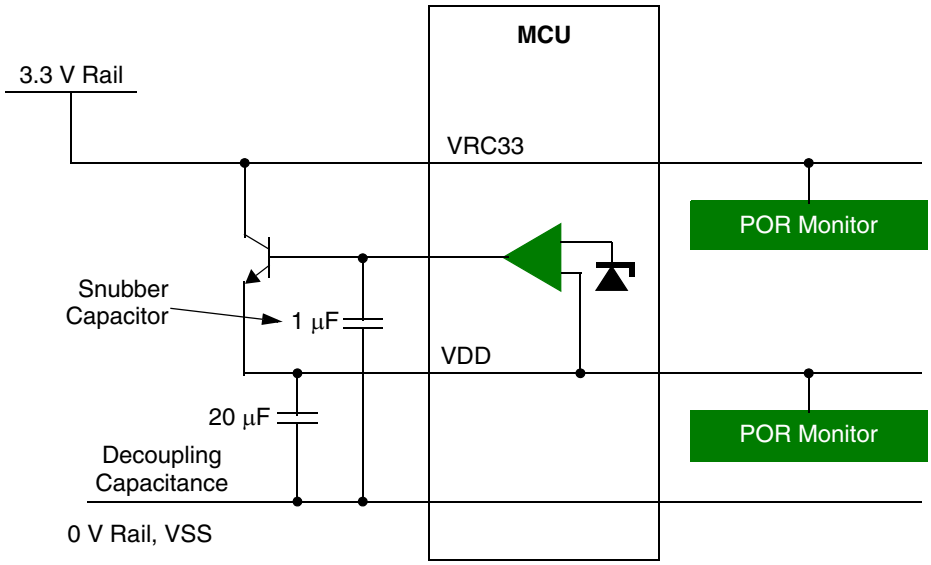

Figure 3. Circuit Architecture

The circuit is a classic emitter follower configuration voltage controlled voltage source. An internal bandgap reference is used. Frequency compensation is controlled through the use of an external ‘snubber’ capacitor; 1µF is recommended. In addition, the output of the external regulator circuitry should have bulk decoupling capacitor; a minimum of 8 µF ceramic decoupling capacitance must be used to ensure VDD stays within specification. It it recommended that a higher ceramic capacitance value of 20 µF (±15%) is used to provide additional decoupling protection.

NOTE

If the VRC is not used to supply VDD, VRCCTL should be left unconnected. This pin will float high internally.

3.2 External Transistor

3.2.1 Parametric Requirements

3.2.1.1 Gain

The gain required of the external transistor is set by the required MCU current and the minimum output current of the VRC. For the smaller devices in the MPC5500 Family, there will be plenty of margin, but for the larger/faster devices, more consideration is required. Table 4 illustrates the range of currents for the devices in the MPC5500 Family.

Table 4. MPC5500 VDD Current Specifications

IDD	Voltage[1]	MPC5534	MPC5553	MPC5554	MPC5565	MPC5566	MPC5567	Unit
Typical Use[2]	1.35V	—	450[3]	600	450[3]	530[3]	450[3]	mA
	1.65V	—	550[3]	700	550[3]	650[3,4]	550	mA
High Use	1.35V	310[3]	490[3]	740	550[3]	630[3,4]	550[3]	mA
	1.65V	380	600[3]	875	600[3]	775[3,4], 695[3,5]	600[3]	mA
Recommended Transistor		BCP68	BCP68	NJD2873	BCP68	NJD2873	BCP68	

1 1.5V is not actually specified (1.35 and 1.65 are specified), but is typical.

2 Typical is not worst case voltage or process parts. Typical use is worst case voltage and temperature.

3 Preliminary Target – actual specification to be determined after characterization.

4 8-way cache.

5 4-way cache or 8-way cache with 4 dedicated to instruction, 4 for data.

Transistor specifications give the minimum and maximum gain. The worst case gain is usually significantly lower than the nominal figure on the cover page. In addition, the data sheet values are usually given at room temperature.

Table 5. Example Gain Table from ON Semiconductor BCP68 Data Sheet (Rev. 4, April 2004)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Current Gain	h_{FE}				—
I_C = 5.0 mAdc, V_{CE} = 10 Vdc		50	—	—	
I_C = 500 mAdc, V_{CE} = 1.0 Vdc		85	—	375	
I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc		60	—	—	

Required gain should be calculated at cold, because a bipolar transistor has minimum gain at low temperature. The worst case gain at cold can be obtained from the transistor manufacturer, or can be estimated using the graphs. There is usually a nominal gain versus temperature plot that shows the reduction in gain at cold. This reduction ratio can be applied to the minimum gain device at room temperature.

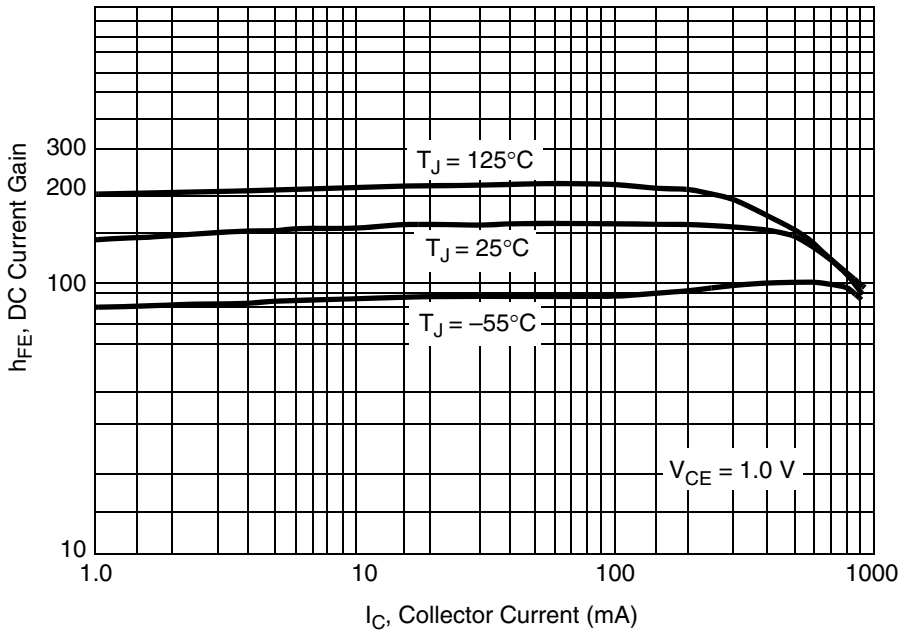

Figure 4. Example Temperature Response from ON Semiconductor BCP68 Data Sheet

For the example data sheets, the minimum gain at room temperature is 85; at 500 mA, the transistor achieves 66% of this (56) at -55°C. ON Semiconductor provided a figure for BCP68 of 54 at -40°C, showing that this method of estimation is reasonable.

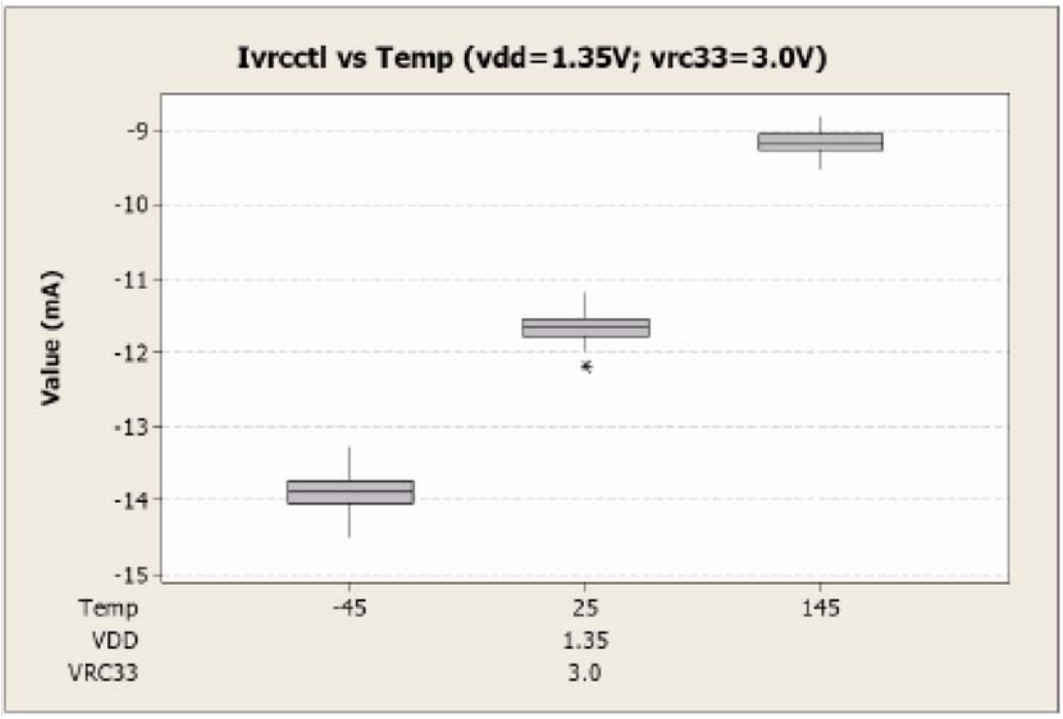

Figure 5. Characterization Data of VRCCTL Base Drive Current versus Temperature

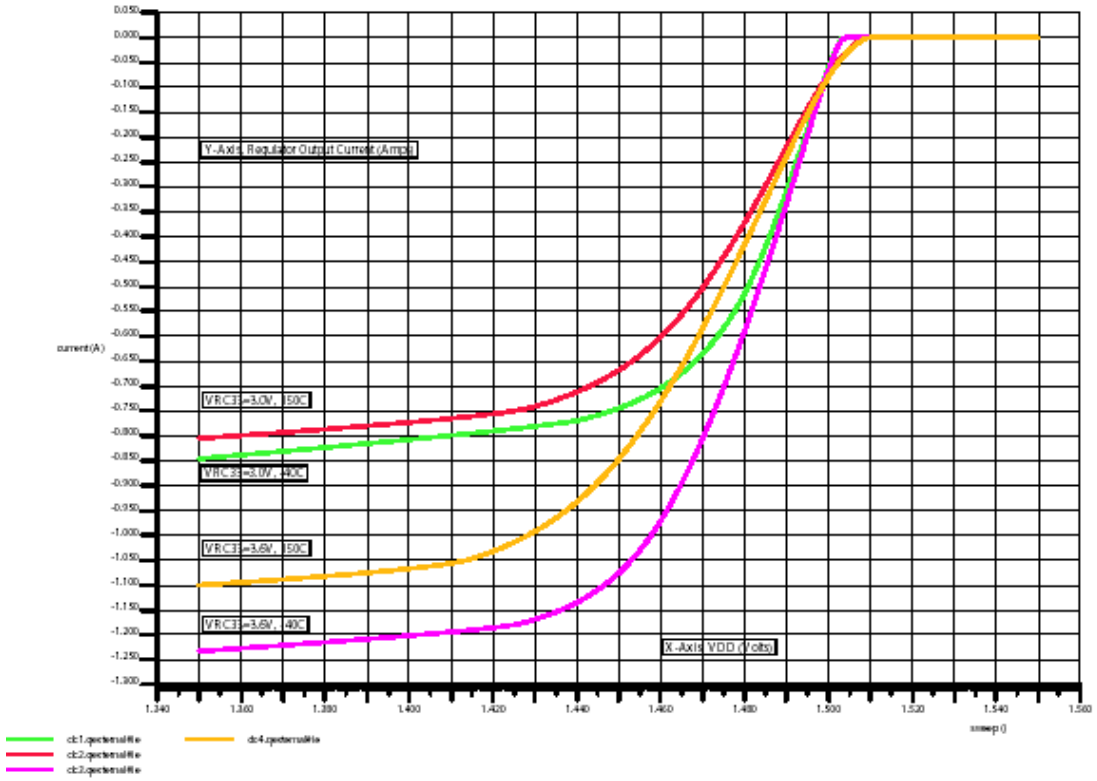

Figure 6. Typical Regulator Output Current versus VDD using BCP68

The VRC output capability rises a little at low temperatures, which helps counteract the reduced bipolar gain.

Calculated gain is maximum transient current divided by VRCCTL base drive current. This calculation is a valid method of estimating the gain but is dependent on the minimum VRC cold output current, which tends to vary in proportion with the required IDD. Thus the BETA values in the data sheet which are measured on a part by part basis provide more realistic and valid value of gain and these should be used to define gain.

If the gain is too high, above about 500, the regulator will become unstable. This occurs if a Darlington transistor is used. The best case hot gain of the proposed transistor should be considered for stability.

3.2.1.2 Power Dissipation

The dissipation required of the bypass transistor is dependent upon the voltage drop across it and the core current. The voltage drop is [VRC33 - VDD]. The absolute maximum voltage is 3.3 V + 10%, and minimum VDD is 1.5 V - 10%, but both regulators will have a greater steady state precision than this, because they need margin to handle current transients. Such transients are not expected to impact power requirements of the bypass transistor and thus can be ignored for power calculations.

The absolute tolerance margins on the 1.5 V rail are lower (± 150 mV) and the minimum voltage will tend towards 1.35 V at higher currents (see example curves below). Medium power transistors will be required for the larger, faster MCUs.

3.2.1.3 VCEsat

To reduce the power dissipation in the transistor, it is permissible to add a series resistor that will drop the collector voltage. If this is used, then the saturation voltage becomes significant; the transistor must remain out of saturation with minimum expected 3.3 V rail and maximum expected 1.5 V rail.

3.2.1.4 Vbe

Vbe in use across temperature and current should be low enough to avoid limiting the VRC output n-FET. In practice, this means 1.0 V, or less, at -40°C.

3.2.1.5 Junction Temperature

The dissipation above applies at all temperatures. The constraint is the maximum junction temperature of the transistor, typically 150°C, although some transistors go up to 165°C. The maximum ambient temperature rating of the target system has a significant effect — typically in the range 85°C to 125°C. The transistor might have an available temperature rise of only 25°C, and thus require good heatsinking. Thermal characteristics of the board and heatsink are required for this calculation.

3.2.2 Recommended Transistors

3.2.2.1 BCP68 NPN Bipolar 1A 2W SOT223

- Available from ON Semiconductor, Philips, Infineon, Fairchild
- Gain banded parts available, e.g. BCP68-25 is minimum gain 160 @ 25°C
- Spice models available online
- Cost effective

This transistor has been simulated with the VRC and should suit many applications. The limit on this device in an application is likely to be low temperature gain or power dissipation. MPC5553/4 systems will require a power sharing resistor and, if run at full speed, high ambient calculations may show the larger DPAK transistor to be required.

Table 6. Gain Table from ON Semiconductor BCP68 Data Sheet

Characteristic	Symbol	Min	Typ	Max	Unit
DC Current Gain	h_{FE}				—
I_C = 5.0 mAdc, V_{CE} = 10 Vdc		50	—	—	
I_C = 500 mAdc, V_{CE} = 1.0 Vdc		85	—	375	
I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc		60	—	—	

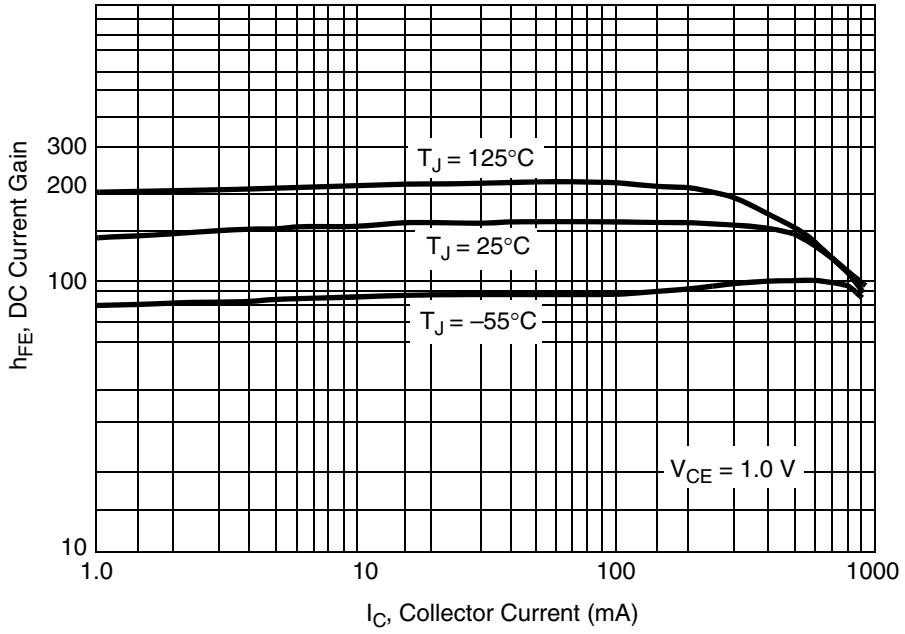

Figure 7. Temperature Response from ON Semiconductor BCP68 Data Sheet

3.2.2.2 NJD2873T4 NPN Bipolar 2 A, 12 W DPAK

- Available from ON Semiconductor
- Higher gain than BCP68 at around 500 mA
- Minimum gain at -40°C specified at 80
- Higher power dissipation than BCP68
- Spice models available online

This transistor should suit limit cases for high MCU current, reduced heatsinking or higher temperatures. It has been simulated with the VRC.

Characteristics	Symbol	Min	Typ	Max	Unit
DC Current Gain	h_{FE}				—
I_C = 500 mAdc, V_{CE} = 2 Vdc		120	—	360	
I_C = 2 Adc, V_{CE} = 2 Vdc		40	—	—	
I_C = 0.75 mAdc, V_{CE} = 1.6 Vdc, –40°C - T_J –150°C		80	—	360	

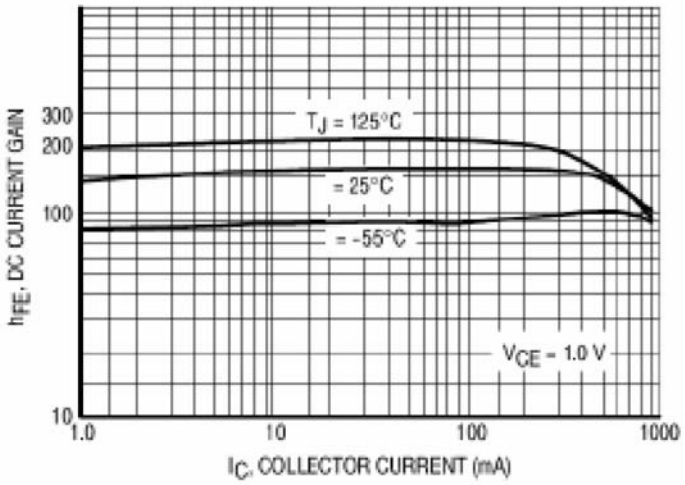

Figure 8. Temperature Response of NJD2873

3.2.3 Examples

Below are some examples to show the calculations required. The numbers are fictional and should not be taken to be specifications for particular systems, but are included to demonstrate the calculations involved.

3.2.3.1 Single-Chip MPC5534, 80 MHz, Cabin-mounted Target System

GAIN:

- MCU maximum transient current 380 mA
- Minimum VRC cold output current 11 mA
- Required gain = 380/11 = 34.5

POWER:

- Maximum steady state MCU current 300 mA
- Maximum collector voltage 3.3 V + 6% = 3.5 V
- Minimum emitter voltage 1.5 V - 5% = 1.43 V
- Required power = (3.5 - 1.43) * 0.3 = 621 mW
- Proposed transistor: BCP68. Min gain cold = 54, PT = 2 W

TEMPERATURE:

- Target system external ambient 85°C
- Target system internal ambient = 85°C + 10 = 95°C
- SOT223 Tjc junction to case = 17K/W
- FR4 with thermal vias for SOT223 = 12K/W
- Heatsink to ambient +3K (depends upon power loading in target system)
- Junction temp = (95°C+3K) + (12K/W+17K/W) * 0.621 W = 78.8°C

3.2.3.2 Single-Chip MPC5554, 112 MHz, Engine Bay Target System

GAIN:

- MCU maximum transient current 700 mA
- Minimum VRC cold output current 11 mA
- Min cold BETA value in data sheet 70
- Required gain = 70

POWER:

- Maximum steady state MCU current 500 mA
- Maximum collector voltage 3.3 V + 5% = 3.45 V
- Minimum emitter voltage = 1.4 V
- Required power = (3.45 - 1.4) * 0.5 = 1.025 W
- Proposed transistor: NJD2873

TEMPERATURE:

- Target system external ambient 105°C
- DPAK Tjc junction to case = 10K/W.
- FR4 with high density thermal vias for DPAK = 8K/W
- Heatsink to ambient +3K
- Junction temp = (105°C+3K) + (10K/W+8K/W) * 1.025 W = 129°C

3.2.3.3 MPC5554, 132 MHz, Engine Mount Target System, Bus, EEPROM Emulation, Cache-Intensive Code

GAIN:

- MCU maximum transient current 875 mA
- Minimum VRC cold output current 11 mA
- Minimum cold, high use BETA value from data sheet 70
- Required gain = 70

POWER:

- Maximum steady state MCU current 600–700 mA
- Maximum collector voltage 3.3 V + 5% = 3.45 V
- Minimum emitter voltage 1.5 V – 10% = 1.35 V
- Required power = (3.45 V-1.35 V) * 0.6A = 1.26 W

RECOMMENDATION 1: BCP68-25 with power sharing resistor

- Min gain cold hfe = 100

RESISTOR:

- Minimum transient voltage 3.3 V - 10% = 3.0 V
- VCEsat minimum circuit limit for Ib = 10 mA, 0.7 V
- Min transient collector voltage = 1.35 V + 0.7 V VCEsat = 2.05 V
- Resistor = (3.0 V - 2.05 V)/0.72 A = 1.3 ohms; use 1.2 ohms 5% total tolerance
- Resistor power max = (0.6 A ^ 2) * (1.2 ohms + 5%) = 0.454 W

TEMPERATURE:

- Target system external ambient 125°C
- Transistor power max = (3.45 V - 1.35 V - (0.6 A * 1.14 ohms)) * 0.6 A = 0.85 W
- SOT223 Tjc junction to case = 15K/W
- FR4 with high density thermal vias for SOT223 = 9K/W
- Heatsink to ambient +3K
- Junction temp = (125C + 3K) + (15K/W+9K/W) * 0.85 W = 148°C

RECOMMENDATION 2: NJD2873.

- Min gain cold hfe = 76.

TEMPERATURE:

- DPAK Tjc junction to case = 10K/W
- FR4 with high density thermal vias for DPAK = 8K/W
- Heatsink to ambient +3K
- Junction temp = (125°C + 3K) + (10K/W + 8K/W) * 1.26 W = 150°C

NOTE

For this example MPC5554 system with a max current transient of 875 mA at cold temp, it is possible to implement the non gain sorted BCP68 transistor by disabling the cache at power up. The cache is a large contributor to the high current on the MPC5554; with the cache disabled at power-on, its Gain requirement would be 50. The minimum gain of the BCP68 at cold is 56, so it can accommodate the requirement. The micro could be run for a short period of time (for example, one second), which would heat up the BCP68. This would raise the gain of the BCP to a minimum of 100. If the cache is enabled after this period in time, the gain requirement of the MPC5554 would raise to 70. The BCP transistor can now handle this new requirement.

3.3 Regulator Controller

3.3.1 Sequencing and Ramp Rate

The regulator does not apply full power to the external transistor until the VRC33 pin is between 2.0 V and 2.85 V (the MPC5554). In order to reduce the ramp rate and therefore 3.3V supply loading, the regulator applies a reduced base drive before this to limit dV/dT of the 1.5 V rail. Since the 3.3 V rail is by definition above the target VRC output voltage, no EMC ramp rate limit applies.

3.3.2 Regulator Voltage

This is designed to be within operating tolerance, as long as the 3.3 V rail remains within specification, i.e., 3.0 V–3.6 V.

3.3.3 Decoupling

The regulator needs output bypass capacitance for stability. For the MPC5554, this should be a minimum of 8 µF; two10 µF ceramic capacitors are recommended for transient capability. Lower current devices require less bypass capacitance than this, 2 µF will provide stability. In addition, for EMC, at least eight 10 nF and two 100 nF capacitors are recommended. A separate application note exists detailing EMC, AN2706.

NOTE

The 8 µF value allows for manufacturing and lifetime derating of the capacitor rating of 50%.

3.3.4 Layout

The distance of the heatsink rail from the MCU on the VRC bypass transistor will lead to inductance in the system. The placement of the transistor will also affect the inductance, due to the length of the VDD trace. This inductance will reduce the phase margin. It is recommended that the overall inductance of the VDD trace is kept below 100 nH. Due to the variation in board type, we cannot give specific details on trace length specification; consequently, we have given an inductance value. Stray capacitance is insignificant compared to bulk capacitance on the base and collector. Trace resistance should be limited as much as possible, given the limitations of the board layout rules.

4 Verification and Validation

4.1 Simulation

The VRC has been verified extensively in simulation using the NJD2873T4 transistor and the BCP68 transistor. Corner cases of VRC output current, VRC33 voltage, temperature, and transistor gain have been covered. Some of the main results from these simulations are shown in this chapter.

4.1.1 NJD2873 Simulations

DC Load Regulation

Conditions:

- Worst Case Conditions
- Temp = -40°C
- NJD2873 Gain = 80, 150

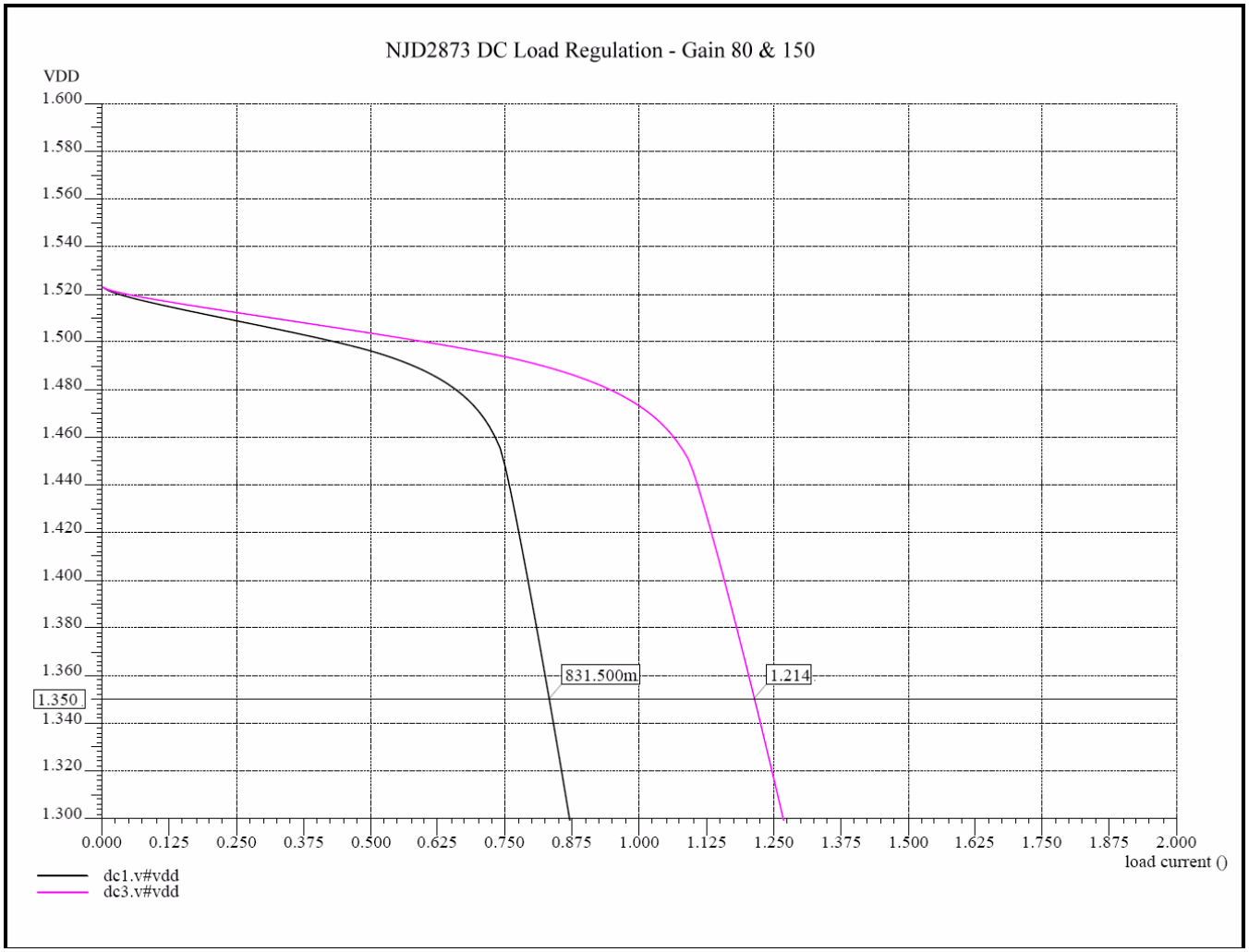

Figure 9. DC Load Regulation of NJD2873 at Gains of 80 and 150

The NJD Load Regulation simulation shows the worst case DC Load Regulation for the VRC circuit using the NJD2873. The black line (dc1) represents VDD at a gain of 80 and a temperature of -40°C. This is worst case gain for the NJD2873 transistor. Under these conditions the transistor is will supply VDD within spec. (Min VDD = 1.35V) for an IDD of up to 831.5 mA. This is sufficient for current requirements of the MPC5554 at -40°C, which is shown in Figure 10 below. Figure 10 contains characterization data of IDD as it varies with temperature and it can be seen that at -40°C IDD does not rise above 831.5 mA.

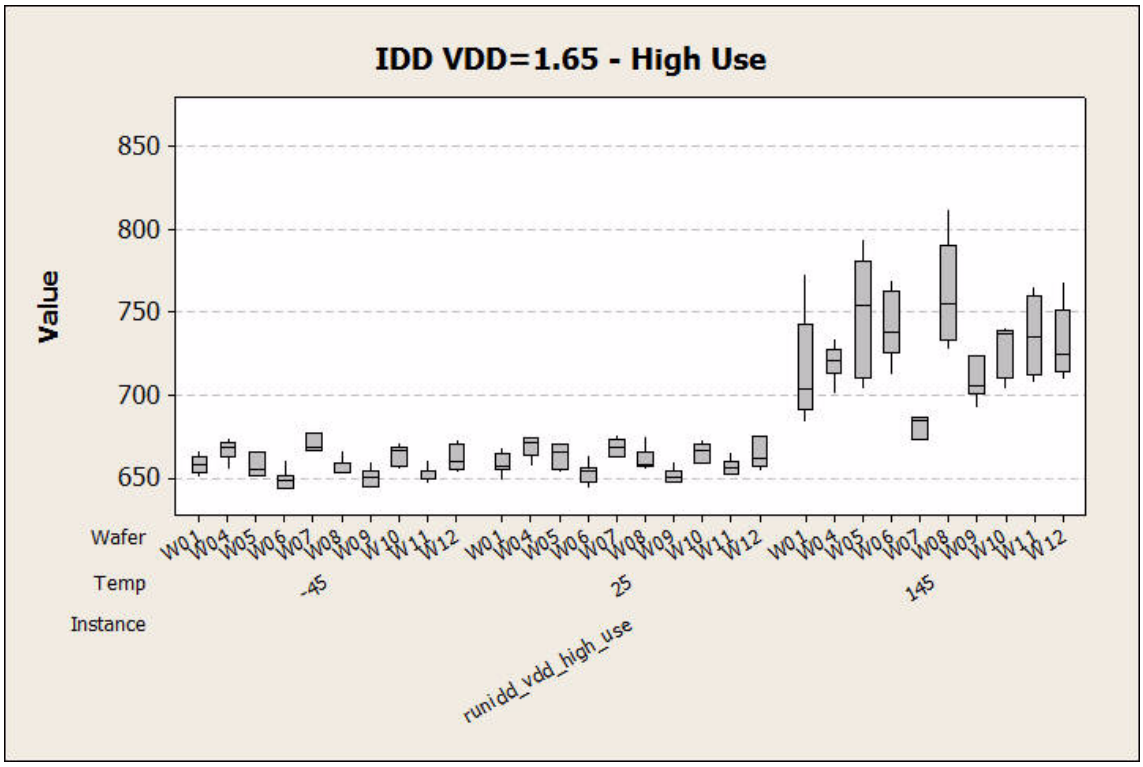

Figure 10. MPC5554 Rev B Characterization Data of Worst Case IDD

As temperature increases, the gain of the NJD2873 increases. This ensures that the transistor is capable of supplying VDD for the maximum IDD of 875mA at 150°C on the MPC5554. This is shown by the pink line (dc3) in the simulations, which illustrates VDD using the NJD2873 with a gain of 150 at -40°C. The simulation shows that it is possible of supplying VDD within specification for an IDD of up to 1.2 A.

DC Transient — 500 mA to 875 mA to 500 mA

Conditions:

- Worst Case Conditions
- Temp = -40°C
- NJD2873 Gain = 80
- 4 µF bulk capacitance.
- IDD Step = 500 mA – 875 mA – 500 mA

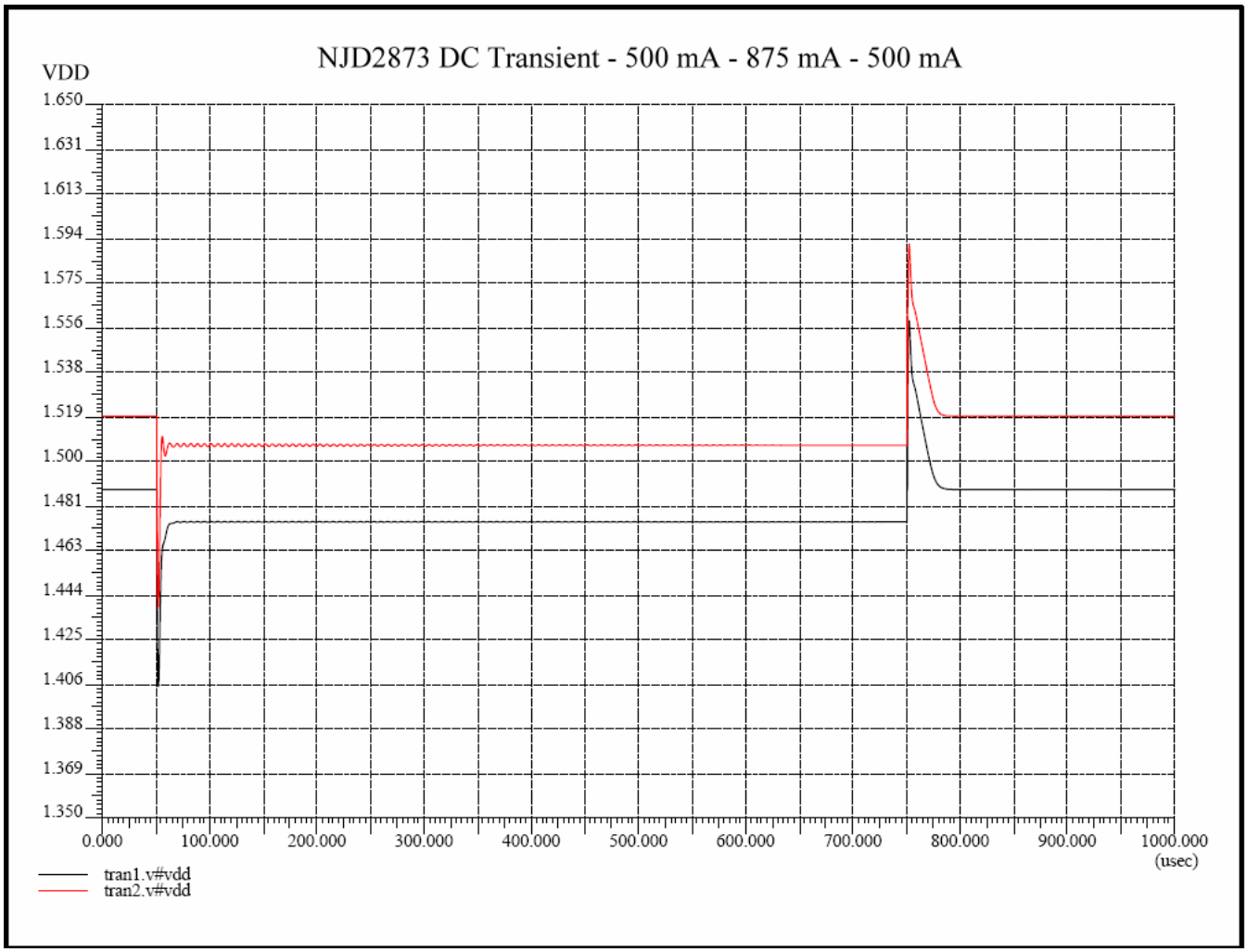

Figure 11. DC Transient of NJD2873, Current step of 500 mA – 875 mA – 500 mA

This NJD Transient simulation shows the upper and lower worst case transient response of VDD using the VRC circuit with the NJD2873 when the current is stepped from 500mA to 875mA to 500mA.

DC Transient — 30 mA to 150 mA to 30 mA

Conditions:

- Worst Case Conditions
- Temp = -40°C
- NJD2873 Gain = 80
- 2 µF bulk capacitance
- IDD Step = 30 mA – 150 mA – 30 mA

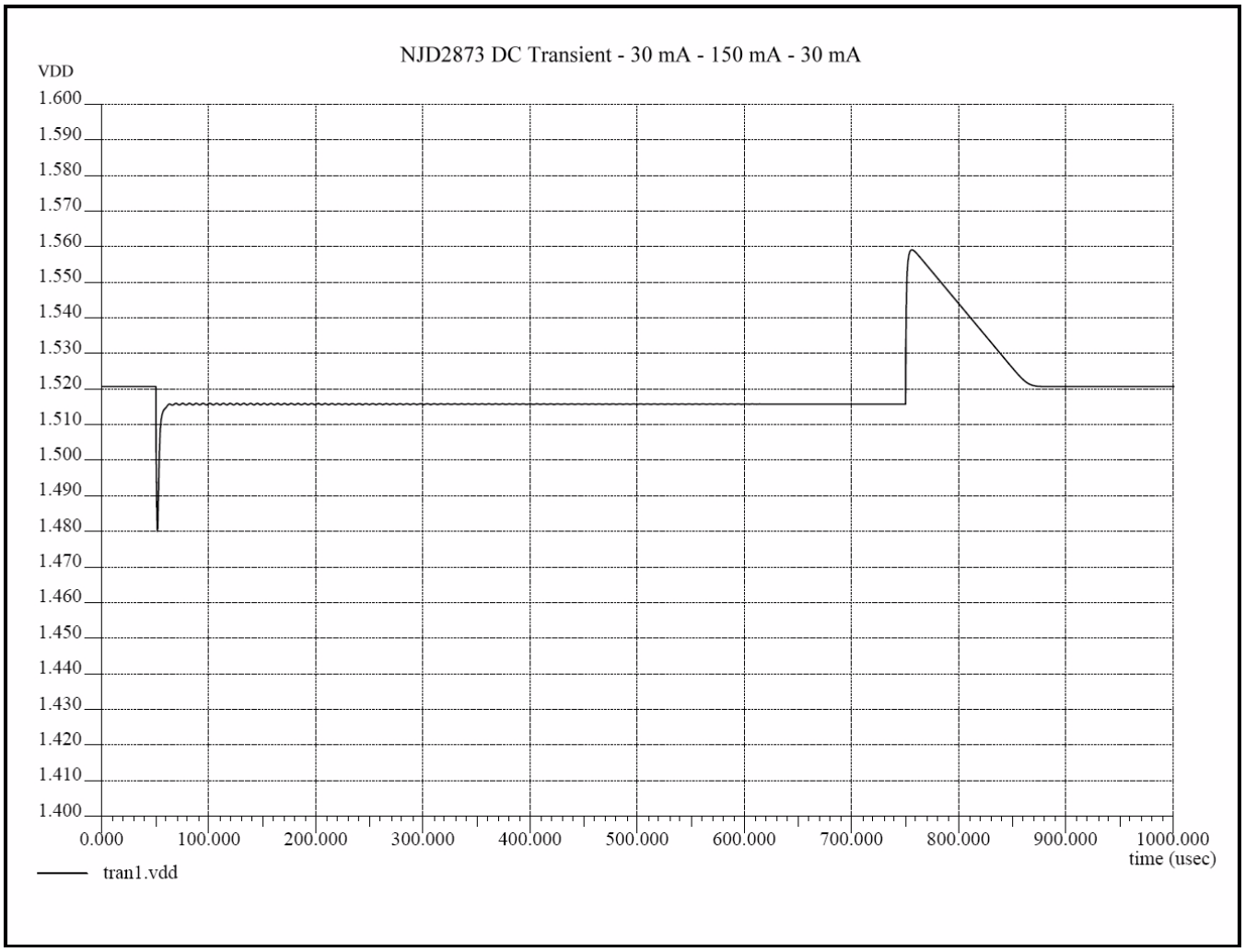

Figure 12. DC Transient of NJD2873, Current step of 30 mA – 150 mA – 30 mA

This NJD Transient simulation shows the transient response of VDD using the VRC circuit with the NJD2873 when the current is stepped from 30m A to 150 mA to 30 mA.

4.1.2 BCP68 Simulations

DC Load Regulation

Conditions:

- Worst Case Conditions
- Temp = -40°C
- BCP68 Gain = 80
- VRC33 = 3.0 V to 3.4 V (100 mV steps)

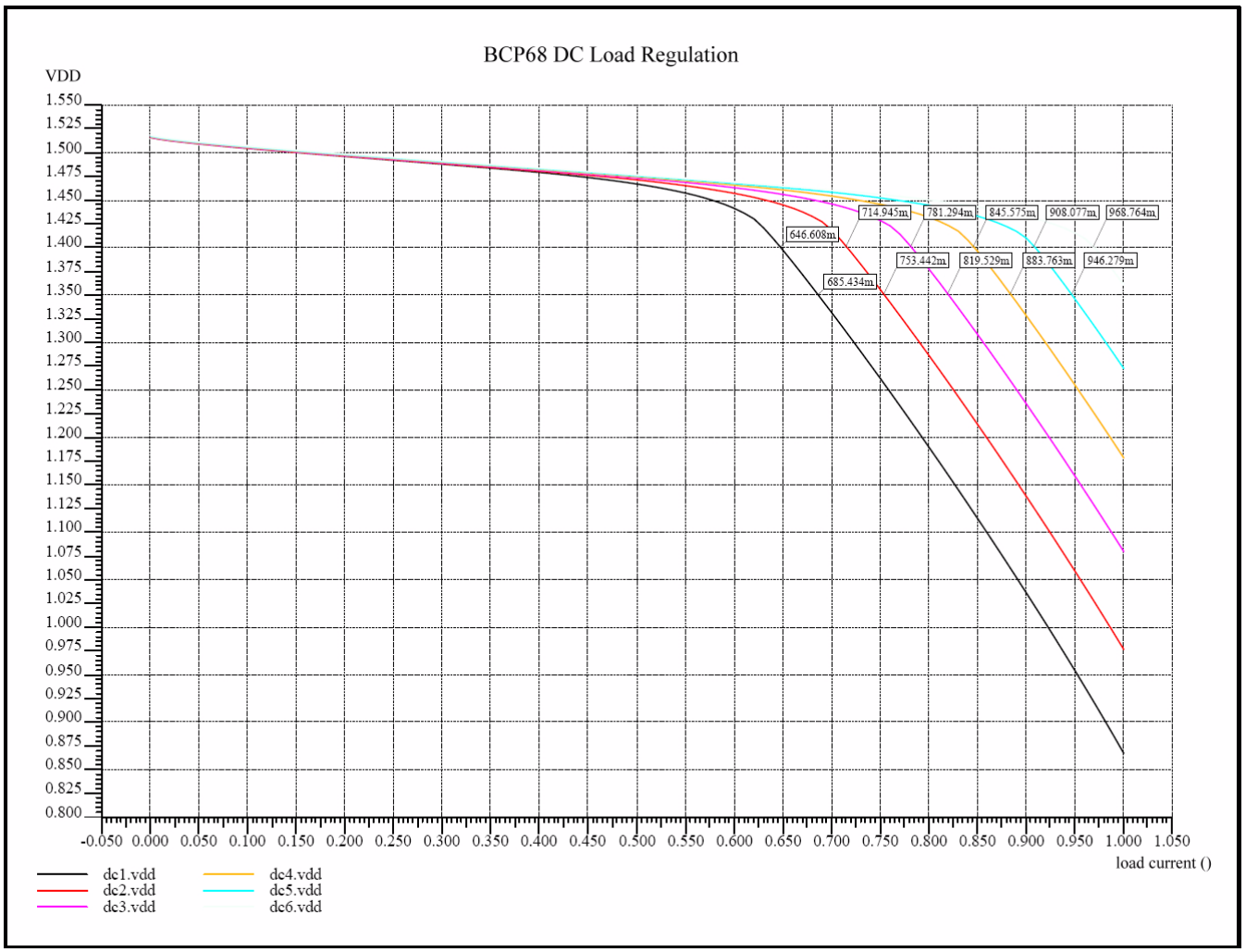

Figure 13. DC load regulation of BCP68

The BCP DC Load Regulation simulation shows the worst case DC Load Regulation for the VRC circuit using the BCP68. This is capable of supplying VDD within specification for an IDD of up to 685mA. This is not suitable for the high use IDD on the MPC5554, the NJD2873 should be used for this, however it is suitable for other members of the MPC5500 that have lower current requirements.

DC Transient 500 mA to 700 mA to 500 mA

Conditions:

- Worst Case Conditions
- 2 µF bulk capacitance
- IDD step: 500 mA – 700 mA – 500 mA

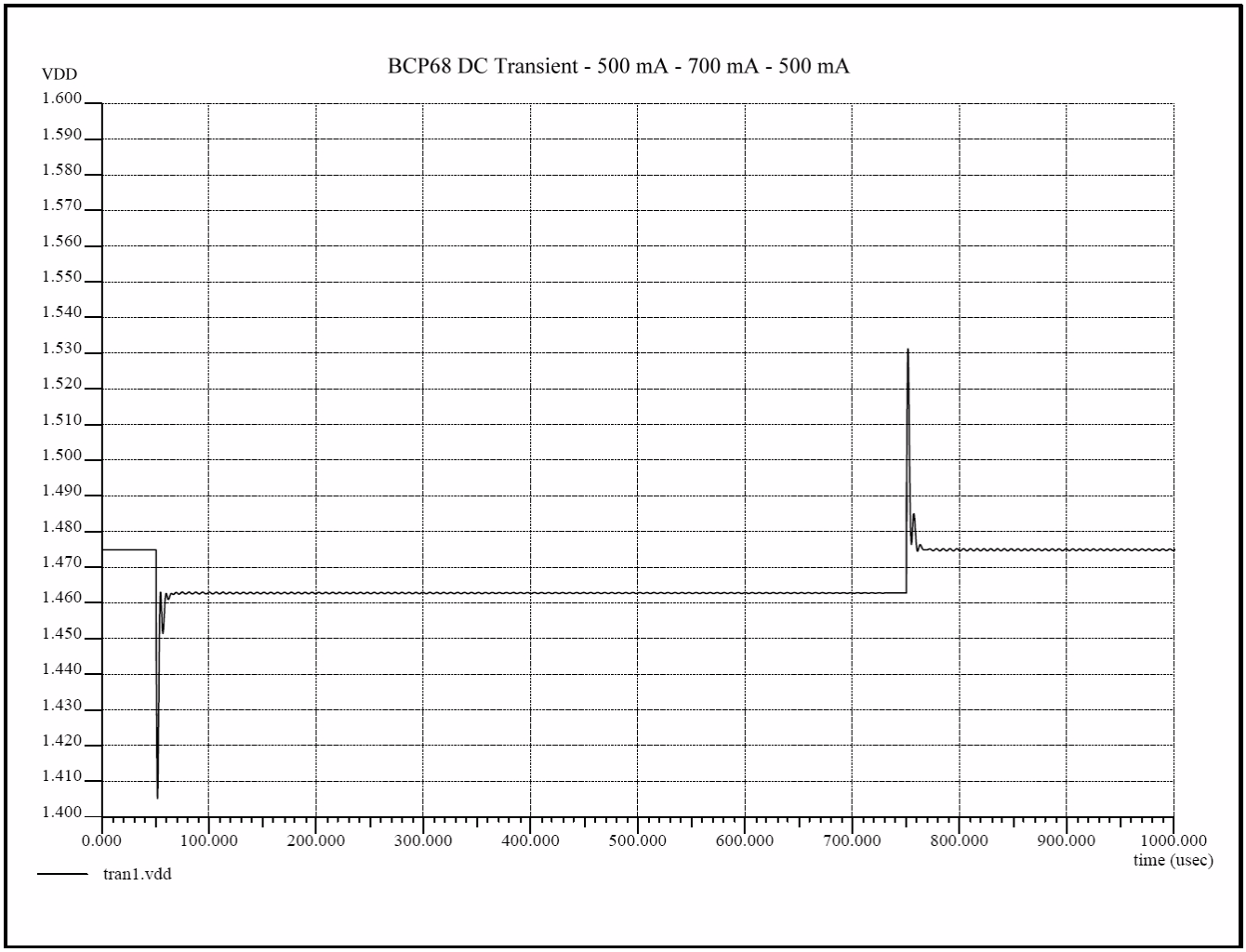

Figure 14. DC Transient of BCP68, Current step of 500 mA – 700 mA – 500 mA

The BCP DC transient simulation shows the transient response of VDD using the VRC circuit with the BCP68 transistor when the current is stepped from 30mA to 150mA to 30mA.

4.2 Characterization

The MPC5554 silicon has been verified to meet the published VRC data sheet limits over production spread, voltage range, and temperature.

4.3 Conclusions

To enable reduced power supply complexity, and compatibility with future silicon, the MPC5500 Family includes an on-board regulator controller. With the addition of an external NPN bipolar transistor, this combination has proved capable of supplying the core current in a wide range of operating installations and conditions.

Appendix A
Detailed Views of Graphs

This appendix provides larger scale and, hence, more detailed views of the graphs in the main body of the application note.

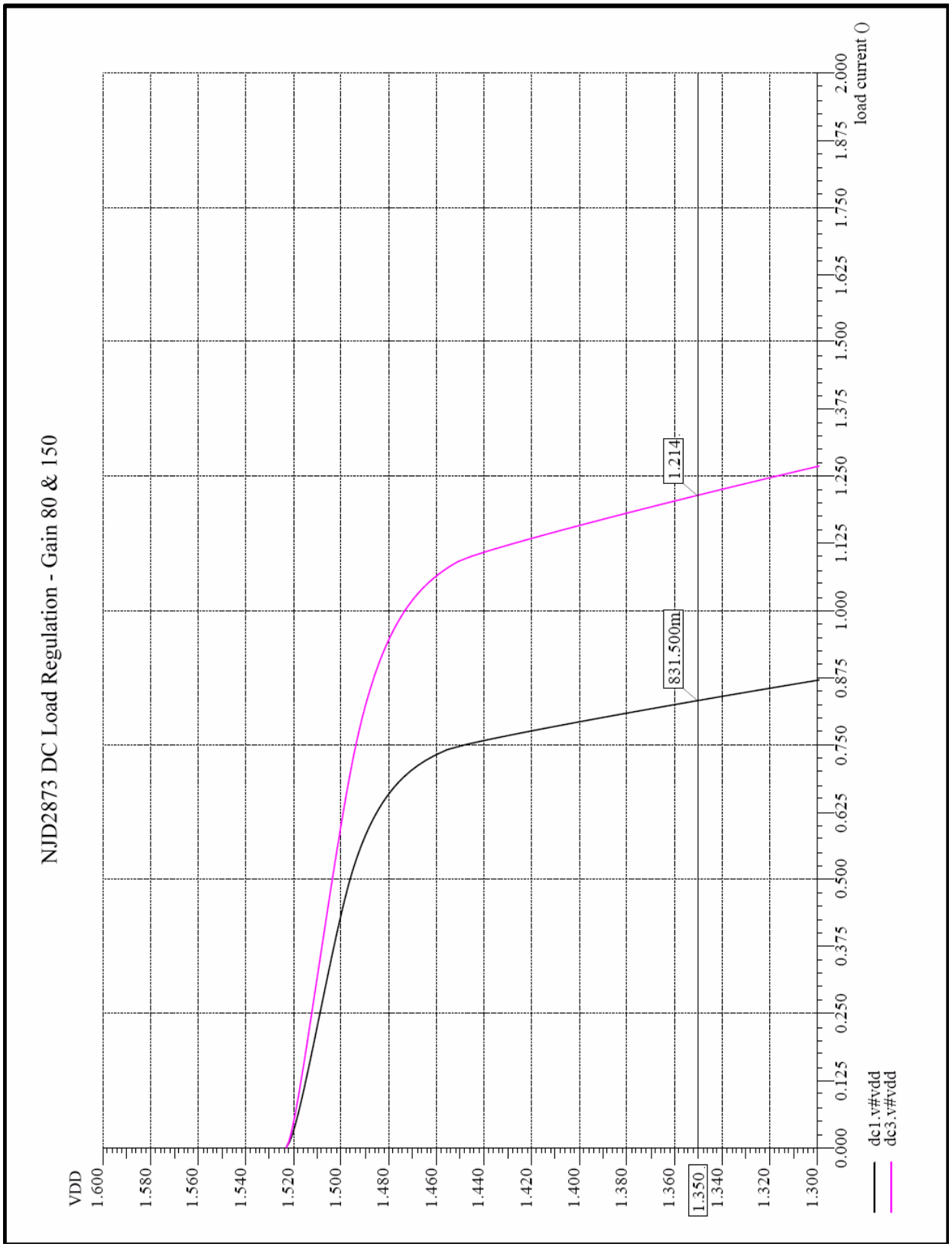

Figure A-1. Detailed View of Figure 9

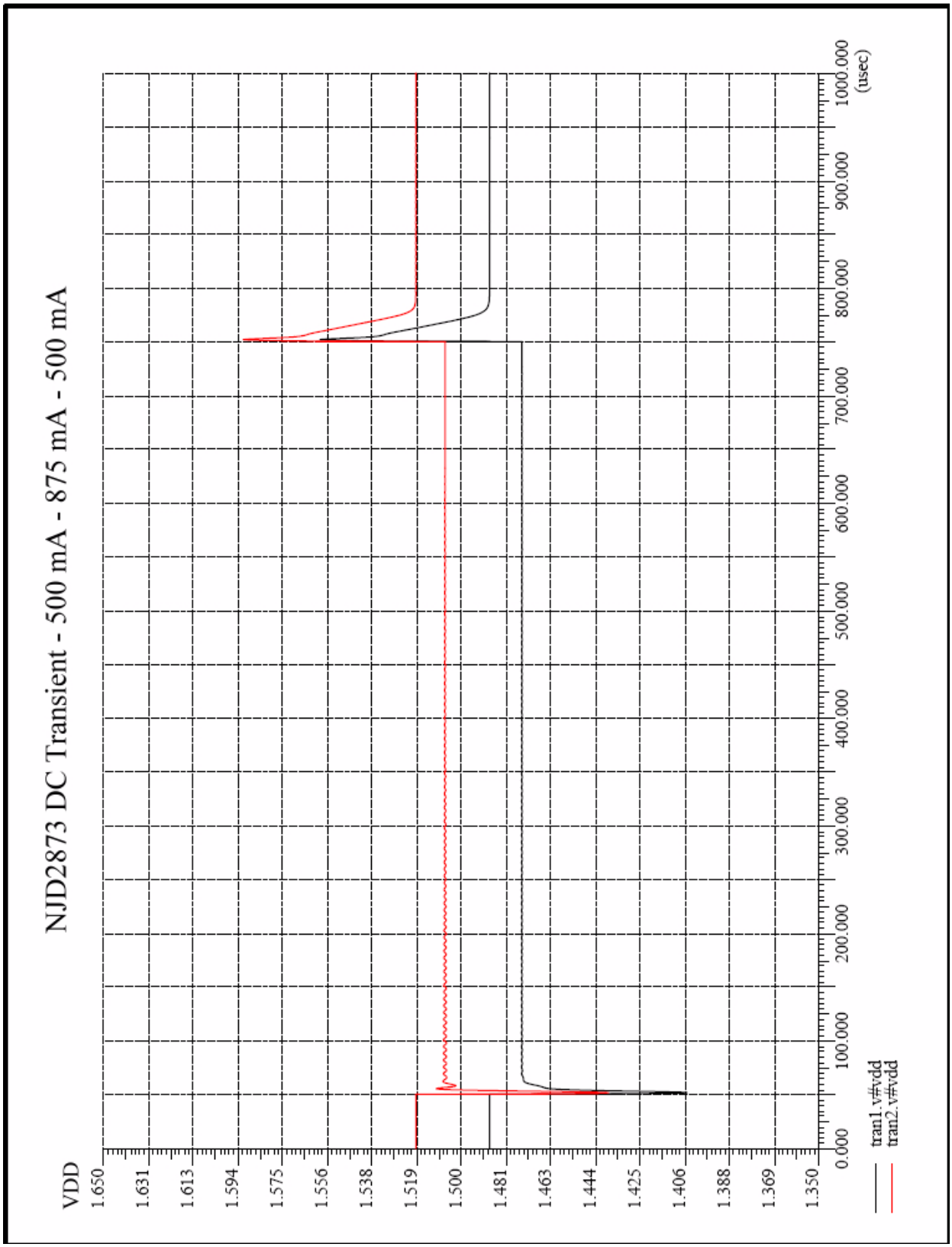

Figure A-2. Detailed View of Figure 11

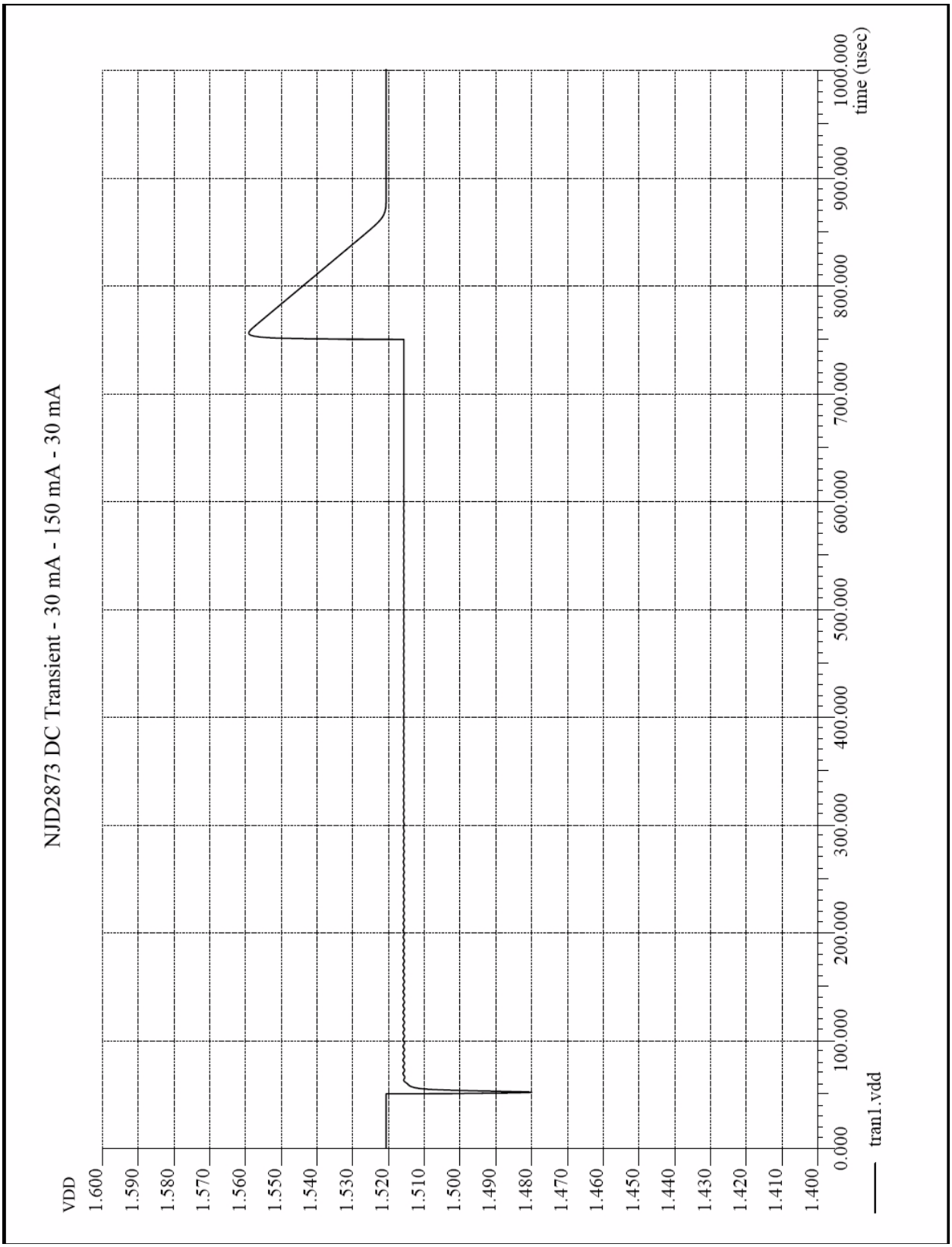

Figure A-3. Detailed View of Figure 12

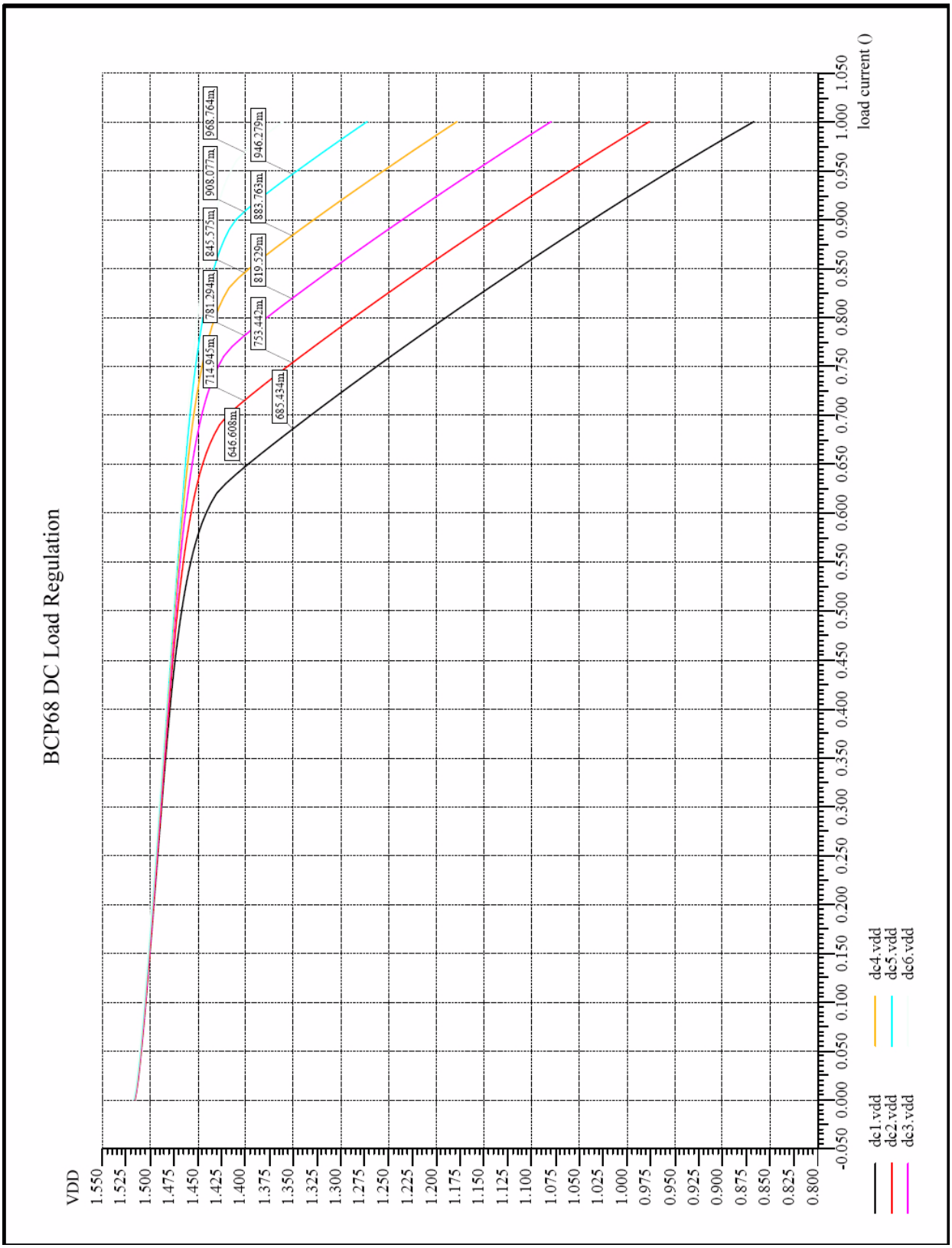

Figure A-4. Detailed View of Figure 13

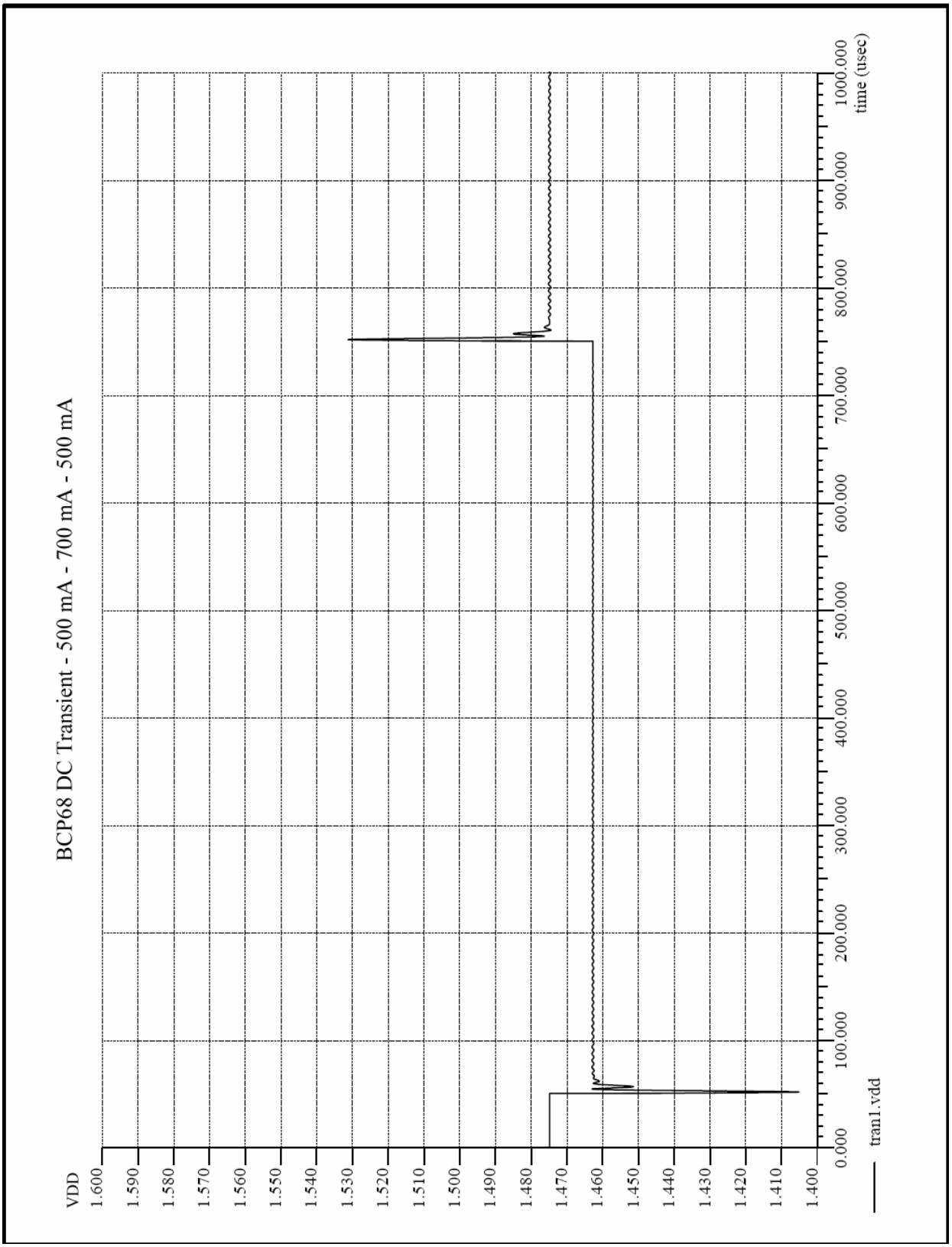

Figure A-5. Detailed View of Figure 14

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