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DOCUMENT DESCRIPTION

Design Guidelines, Ethernet Front End Design Guide For Use With SMSC Products

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Ethernet Front End Design Guide

Purpose

This design guide is supplied to our customers to facilitate the design of a robust PCB for their LAN application. This guide is intended for the review of new designs as well as existing PCB troubleshooting efforts. This design guide, however, should not be the ***only*** source of information in designing a PCB with an SMSC product. This particular design guide simply covers the Ethernet Front End in a generic manner; an all-inclusive PCB design may or may not include additional information concerning our products. The system designer should also review the material listed below to assure a successful design effort:

- Specific SMSC Product Data Sheet
- Specific SMSC Product Reference Schematic
- Specific SMSC Bill of Material
- Any Applicable SMSC Product Application Note
- Specific SMSC Product LANCheck Schematic Checklist
- Specific SMSC Product LANCheck Component Placement Checklist
- Specific SMSC Product LANCheck Routing Checklist
- General PCB Design Guidelines
- General ESD Design Guidelines
- General EMC Design Guidelines

All the information above can be obtained from our website. If any of the above documentation is not available by that means, simply contact any SMSC FAE or SMSC Representative and they should be able to furnish any documentation required.

TX± & RX± Differential Pairs

1. Both RX± and TX± pairs should be routed as differential pairs. This includes the entire length of travel of the traces from the RJ45 connector to the LAN device.

2. RX± and TX± differential pairs should be routed as close together as possible. Typically, when beginning the impedance calculation, the smallest trace space (4 – 5 mils) is selected. The trace width is then adjusted to achieve the necessary impedance.

3. Differential pairs should be constructed as 100-ohm, controlled impedance pairs.

4. Differential pairs should be routed away from all other traces. Try to keep all other high-speed traces at least .300” away from the Ethernet front end.

5. Each trace of the differential pair should be matched in length. The matched lengths of each positive and negative pair should be within 50 mils of each other.

6. The differential pairs should be as short in length as possible.

7. The use of vias is not recommended. If vias are used, keep to a minimum and always match vias so the differential pairs are balanced.

8. Layer changes are also not recommended. Keep the differential pairs referenced to the same power/ground plane whenever possible.

9. For optimum immunity, route Transmit pairs and Receive pairs as far away from each other as possible.

10. Always reference any Transmit terminations to the same reference plane that the Transmit routes are referenced to. Likewise, always reference any Receive terminations to the same reference plane that the Receive routes are referenced to.

11. Precedence should be given to the differential pair routing. Terminations should be added after the routing is determined. The terminations should simply be “dropped” onto the differential routing.

12. All resistive terminations in the Ethernet front end should have values with 1.0% tolerances.

13. All capacitive terminations in the Ethernet front end should have tight tolerances and high quality dielectrics (NPO).

14. For optimum separation, experimentation can be explored with inserting a ground plane island between the Transmit pair and the Receive pair. A separation from this ground plane from any of the traces of 3 – 5 times the dielectric distance should be maintained.

15. This same technique can be used to separate different Ethernet ports if port cross talk is an issue. A ground plane can be inserted between Ethernet channels. The separation space between the two channels should be as wide as possible. Again, a separation from this ground plane from any of the traces of 3 – 5 times the dielectric distance should be maintained.

Unused Cable Pairs

1. The unused cable pairs (pins 4, 5, 7 & 8 on the RJ45 connector) should be properly terminated for common mode considerations.

2. These terminations should be routed with heavy, short traces.

3. Place these terminations as close as possible to the RJ45 connector.

4. Terminate these resistors to a proper chassis ground plane through a high voltage (2KV) capacitor.

RJ45 Connector

1. A shielded, metal enclosed RJ45 connector is recommended.

2. The metal shield should be connected directly to a proper chassis ground plane.

3. To maximize ESD performance, the designer should consider selecting an RJ45 module without LEDs. This will simplify routing and allow greater separation in the Ethernet front end to enhance ESD/susceptibility performance.

4. Another ESD enhancement may be to use of an RJ45 connector with surface mount contacts. This may simplify routing and allow greater separation in the Ethernet front end to enhance ESD/susceptibility performance.

Magnetics

1. There are many different types and configurations of magnetics available for use with any particular LAN device. Different packages, orientations, sizes are all factors that need to be considered when selecting magnetics. For all our SMSC LAN devices, it is our recommendation is to use a qualified, recommended magnetic from our “Suggested Magnetics” application note. This application note is available from our website.

2. If the design engineer chooses to select an alternate magnetic for his application, he should take certain steps to ensure a proper match to our LAN devices. Again, referring to our “Suggested Magnetics” application note, the designer should use a tested and qualified magnetic from that application note as his reference. By obtaining the data sheet for that preferred magnetic and using it for comparison, the alternate magnetic cab be evaluated. By comparing the specifications from the two data sheets, the design engineer can make an informed decision on how the alternate magnetic compares to the recommended and if it is suitable for use with the particular SMSC LAN device.

3. The magnetics should be placed as close as possible to the RJ45 connector.

4. Depending upon which style of magnetic selected (North/South or East/West) will determine the orientation of the magnetics as related to the RJ45 connector. Be certain the network side of the magnetics faces the RJ45 connector and the device side of the magnetics faces the LAN device. This will ensure that the high voltage barrier through the middle of the magnetics can be correctly routed and designed on the PCB.

5. Ideally, the LAN device should then be placed as close as possible to the magnetics. If this is not possible, the RJ45 connector and magnetics must remain in close proximity. The LAN device then can be located somewhat remotely from the RJ45/magnetics area.

6. To maximize ESD performance, the designer should consider selecting a discrete transformer as opposed to an integrated magnetic/RJ45 module. This may simplify routing and allow greater separation in the Ethernet front end to enhance ESD/susceptibility performance.

PCB Layer Strategy

1. In typical applications, power planes and digital ground planes are run from the LAN device to halfway through the magnetics module.

2. Typically, all planes are cleared out on the PCB in the area from halfway through the magnetics to the RJ45 connector. The TX± and RX± pairs should be the only traces in this cleared out region of the PCB. This creates one part of the high voltage barrier required for LAN applications.

3. Then, a chassis ground plane is designed up around the RJ45 connector. Once the plane shape is determined, this same shape should then be mirrored on all layers of the PCB.

4. Keep the chassis ground plane dimensions in a 6:1 ratio. Any sizing smaller than this results in the plane looking and acting more like a trace than a plane.

5. Do not allow any other plane or trace overlap the chassis ground plane. This will reduce the isolation/protection performance of the chassis ground plane.

6. Review basic Chassis Ground Plane Design Guidelines for PCBs before committing to a PCB assembly.

TX/RX Channel Crossover

1. Depending upon RJ45 orientation (Tab-up or Tab-down), the magnetics selected and the LAN device pin-out, a TX/RX channel crossover may be required at the PCB level. This practice is not recommended but when it is unavoidable, it can be accomplished.

2. When designing a crossover at the PCB board level, care should be taken. Typically, the recommendation is to leave the transmit channel intact on the top signal layer referenced to a solid digital ground plane. Since the Receive channel, in general, is more forgiving, the crossover can be performed on the Receive channel.

3. The crossover begins by taking the RX± pins from the LAN device immediately to the bottom layer through matched vias. The pairs can then be run completely on the bottom layer, if necessary, to complete the crossover function.

4. The crossover should have matched vias in each of the RX traces. This will balance the pairs as best as possible. The use of vias should be kept to a minimum for this crossover function.

5. The RX traces should also be matched in length as best as possible.

6. Keep all the routes as short as possible.