XCalibur1002

CompactPCI Single Board Computer based on the IBM750GX and Marvell Discovery III

User's Manual

Revision 060525

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Revision History

Revision	Principal Changes	Date	Board Rev.
041028	Updated Manual Style	October 28, 2004	SC
041123	Added Setup & Troubleshooting Chapter Updated to current manual style	November 23, 2004	SC
050805	Updated Address. Updated processor from 750FX to 750GX	August 5, 2005	SC
060203	Updated Memory Maps, added ordering information, board weight, stacking height specifications. Clarified interrupt routing description. Updated power dissipation numbers and clarified test conditions.	February 3, 2006	SC
060519	Updated Component Maps, Front Panel Map, FPGA register descriptions for Rev. D board.	May 19, 2006	SD
060525	Added FRAM to CPU memory map, added ICTRL FPGA register description.	May 25, 2006	SD

1. Overview

XCalibur1002 is a 6U CompactPCI single board computer with a PICMG 2.16 Gigabit Ethernet backplane interface. An extended operating temperature range of -40C to +85C makes XCalibur well suited for industrial and military applications. With an 800MHz to 1GHz IBM PowerPC Processor, XCalibur is ideal for the high bandwidth processing requirements of today's blade and general computing applications.

XCalibur1002 provides a highly configurable processing platform. 266MHz-400MHz DDR DRAM provides up to 1GB of local memory. An optional CompactFlash interface accepts up to 1GB of non-volatile memory. Two PCI-X PPMC slots are available for high bandwidth IO.

Hot Swap support allows XCalibur1002 to be installed into a live system without disrupting CompactPCI bus activity. In addition, system management bus support allows the card to be powered down and reset remotely through the IPMI interface.

To the system designer, XCalibur1002 provides a feature rich solution to support the next generation of embedded applications.

Board Support Packages are available for the VxWorks, Linux, QNX, INTEGRITY, and OSE Real Time Operating Systems.

1.1 Features

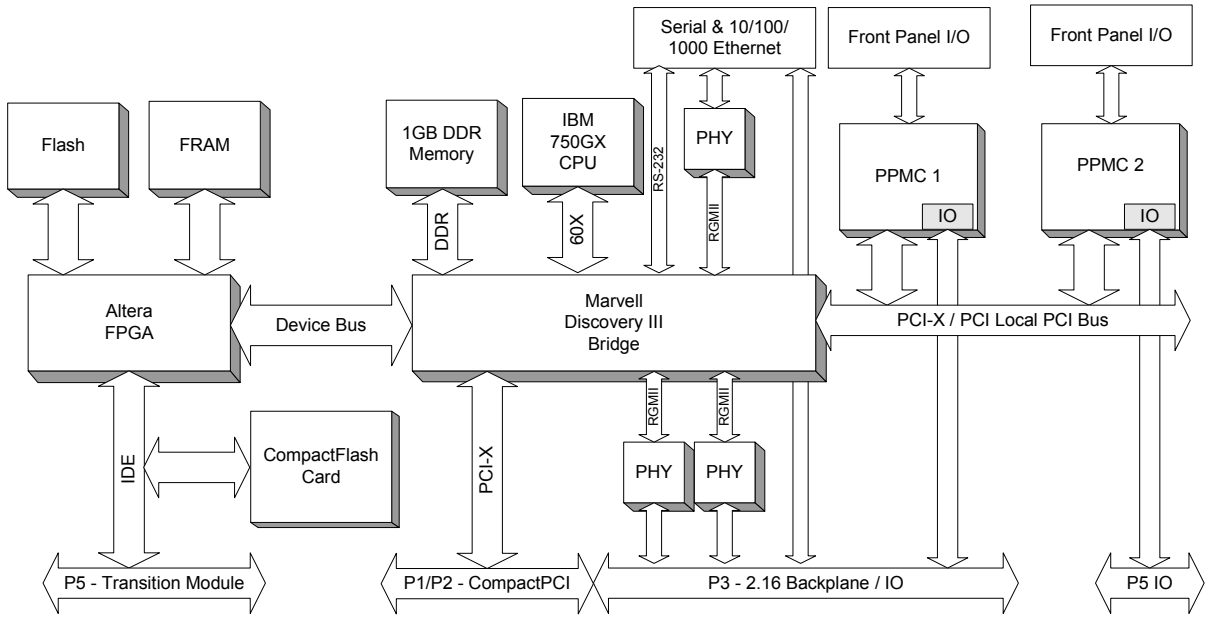
The list below is a brief description of XCalibur1002 features. Refer to the specific section in the manual for additional information.

PowerPC 750GX Processor	The low power / high performance IBM 750GX PowerPC Processors operate internally at up to 1GHz. In addition 32KB L1 instruction and data caches are provided, as well as a on-board 1MB L2 Cache.
Dual PCI-X PrPMC Slots	Two PCI 2.2 compliant PrPMC slots are provided. P14 PMC IO is routed to the J3 and J5 connectors per PICMG 2.3.
Autosense System / Peripheral Slot	XCalibur automatically detects and configures for either CompactPCI system slot or peripheral slot operation.
Hot Swap Support	PICMG 2.1 Hot Swap support allows insertion and removal from an active CompactPCI bus.
DDR SDRAM	XCalibur supports up 1GB of DDR SDRAM operating at 266MHz-400MHz.
FRAM	A 32KB FM18L08 Ramtron FRAM is provided for nonvolatile storage.
Socketed / Soldered Flash	A 512KB socketed flash is provided. Up to 144MB of soldered boot flash is also supported.

CompactFlash Socket	A CompactFlash interface provides up to 1GB of removable non-volatile storage.
Front Panel Serial and Gigabit Ethernet Ports	Front Panel Serial and Gigabit Ethernet ports are provided for debug and communication.
Extended Temperature	Supports operation from -40C to +85C.
RTOS and Protocols	Board Support packages for Wind River System's VxWorks operating system. Driver level initialization, configuration and protocol support for Discovery II and Gigabit Ethernet interfaces. Linux Support Package for Montavista's embedded linux also available, as well as OSE and QNX board support packages.

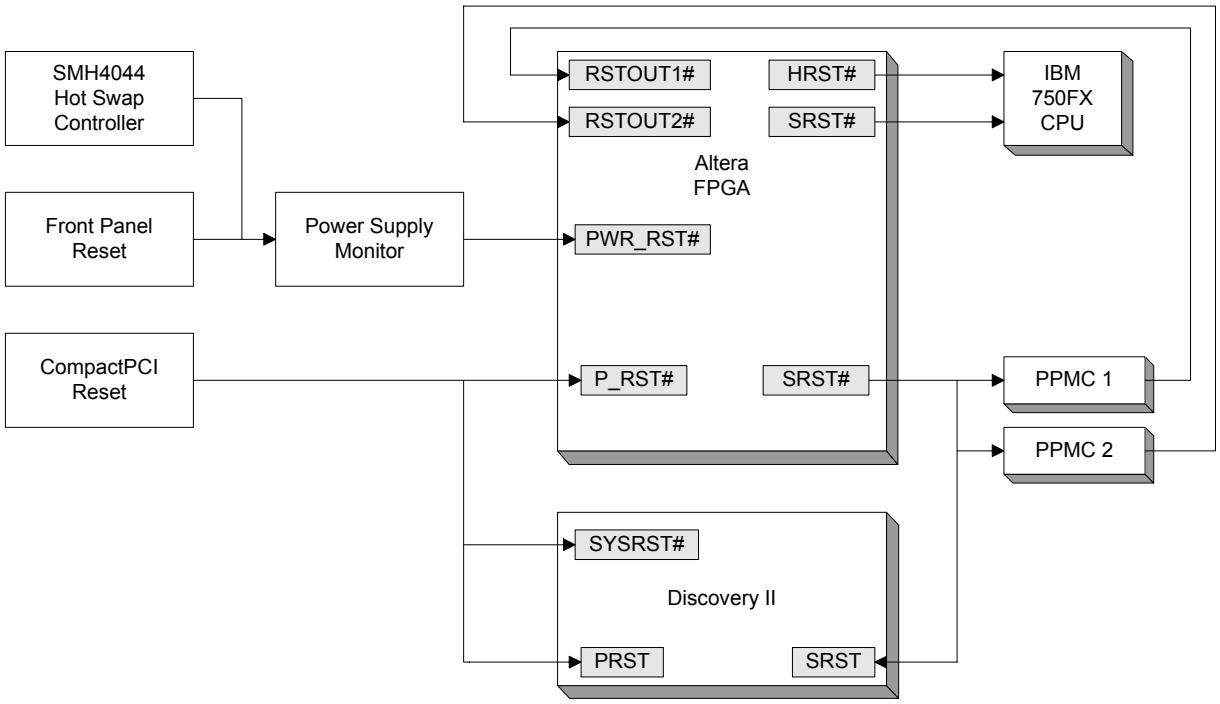
1.2 Block Diagram

Figure 1.2.1: Block Diagram



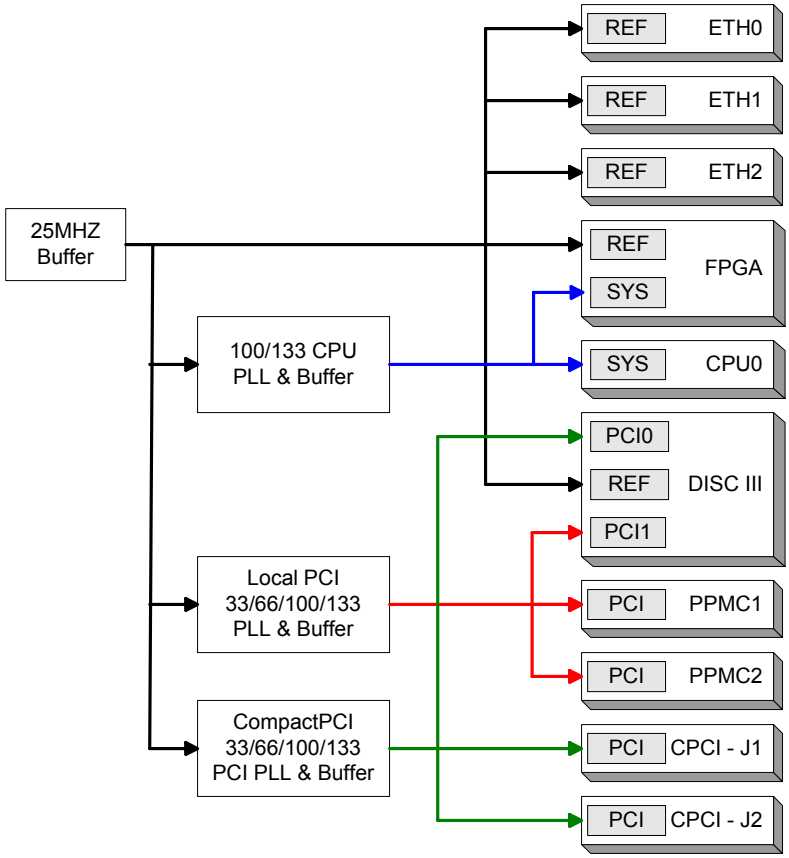
1.3 Reset Diagram

Figure 1.3.1: Reset Diagram



1.4 Clock Diagram

Figure 1.4.1: Clock Diagram



1.5 Terminology / Conventions

Table 1.5.1: Terminology

Term	Definition
byte	8 bits
DMA	Direct Memory Access
double long word	64 bits
DRAM	Dynamic Random Access Memory
JTAG	Joint Test Action Group
long word	32 bits
MII	Media-independent Interface
PCI	Perpherial Component Interconnect
SDRAM	Synchronous Dynamic Random Access Memory
SRAM	Static Random Access Memory
word	16 bits

Table 1.5.2: Conventions

Term	Definition
0x0	This notation denotes a hexadecimal number.
0b0	This notation denotes a binary number.
Active Low Signals	Active Low Signals are listed with a # postfix. IE: RESET#

1.6 Technical Information

The technical information in this manual is intended to describe the unique features of XCalibur1002. It is assumed that the reader has familiarity with the devices and interface standards incorporated into the XCalibur1002. This information can be found in the following manuals and specifications.

PPC750GX	PowerPC 750 RISC Microprocessor User's Manual	IBM	GK21-0263-00, 2/23/1999
	PowerPC 750GX RISC Microprocessor Datasheet Preliminary Electrical Information	IBM	Version 0.9A, 12/19/2001
PCI	PCI Local Bus Specification, Revision 2.2	PCI-SIG	
CompactPCI	PICMG 2.0 CompactPCI Core Specification, Revision 3.0	PICMG	
	PICMG 2.1 CompactPCI Hot Swap Specification, Revision 2.0	PICMG	
	PICMG 2.3 PMC on CompactPCI Specification, Revision 1.0	PICMG	
	PICMG 2.9 CompactPCI System Management Specification, Revision 1.0	PICMG	
	PICMG 2.10 Keying of CompactPCI Boards and BackPlanes Specification, Revision 1.0	PICMG	
	PICMG 2.16 CompactPCI Packet Switching Backplane Specification, Revision 1.0	PICMG	
PMC	IEEE Standard for a Common Mezzanine Card Family: CMC	IEEE	1386-2001
	IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC 2001	IEEE	1386.1-2001
Discovery III	MV64460 System Controller for PowerPC Processors, Revision A	Marvell	MV-S101286-00, 6/19/2002

FPGA	Altera ACEX 1K Programmable Logic Device Family Datasheet	Altera	A-DS-ACEX-3.3, Version 3.3, 11/2001
DS1631	DS1631 Digital Thermometer and Thermostat	Dallas	DS1631, 092502
M41T00	M41T00 Serial Access Timekeeper	STMicro	**M41T00**, 11/2002
FM18L08	FM18L08 256Kb FRAM Parallel Memory, Revision 2.2	Fairchild	FM18L08ds, 7/2004
IPMI	Intelligent Platform Management Interface Specification.	Intel	Version 1.5, 2/20/2002
IPMB	Intelligent Platform Management Bus Communications Protocol Specification	Intel	Version 1.0, 11/15/1999
BCM5461	Broadcom 10/100/1000Base-T Gigabit Ethernet Transceiver	Broadcom	5461-DS06-R, 8/15/2002

1.7 Ordering Information

The XCalibur1002 offers a wide range of configuration options. Before ordering, please review the following options and specify how the XCalibur002 can be configured for your application.

Table 1.7.1: XCalibur1002 Configuration Options

Item	Option
SDRAM	128MB - 1GB, 266MHz - 333MHz (Industrial Temp) or 400MHz (Commercial temp)
CPU	750FX or 750GX, up to 1.0GHz
Soldered Flash	16-128MB
Operating Temperature	Commercial (0 to +55C) or Industrial (-40 to +85C)

1.8 XCalibur1002 Software/Accessories

X-ES offers several software solutions for the XCalibur1002, listed below. Other operating systems can be supported by request, please contact X-ES sales!

Table 1.8.1: Available Software

Operating System	Description
VxWorks	VxWorks BSP
Linux	Linux LSP
QNX	QNX BSP
INTEGRITY	Green Hills INTEGRITY BSP
OSE	Enea OSE BSP
Other / N/A	XCalibur1002 xMon Monitor

The following accessories are available for the XCalibur1002 board. For more information on any of these items please contact X-ES.

Table 1.8.2: Available Accessories

Part Number	Description
90000075	Adapter Cable, Micro-D to D-Sub 9, Female - Male, 3ft

The following additional documentation is available for the XCalibur1002 board. For more information on any of these items please contact X-ES.

Table 1.8.3: Additional Documentation

Manual	Description
xMonXCalibur1002tm.pdf	XCalibur1002 xMon Monitor Manual

2. Printed Circuit Board

This chapter describes details associated with the printed circuit board. These include component maps, installation, ESD handling concerns and environmental and power requirements.

2.1 Electrostatic Discharge

When handling this product, please remember that electrostatic discharge (ESD) can easily damage the components on this module and result in board failure. Unless you ground yourself properly, static can build in your body and cause ESD damage when you touch the board. To ground yourself, wear a grounding wriststrap. Simply placing this module on a static-shielding bag offers no protection -- place it on a grounded ESD-safe mat. Do not place this board on metal or other conductive surfaces. When this board is not in use or in an enclosure, store it in either a static-shielding bag or clamshell provided.

CAUTION: Use proper ESD procedures and handle this board only when absolutely necessary. Always wear a wriststrap while handling this board. Hold this board by the edges. Do not touch any components or circuits. Store in ESD safe bag when not in use.

2.2 Physical Dimensions

Table 2.2.1: XCalibur1002 PCB Dimensions

Parameter	Value
Form Factor	6U Compact PCI
Length	233.35mm
Width	160mm
Board Weight	13.3oz

2.3 Front Panel

The following table describes the features of the front panel.

Figure 2.3.1: Front Panel Map (Rev. D)

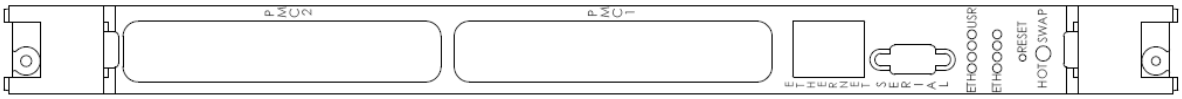


Table 2.3.2: Front Panel Features

Feature	Description
Blue Hot Swap LED	Used as an indicator in hot swap removal and installation.
Ethernet/User Defined LEDs	Provides two user defined LEDs as well as link and activity LEDs for the front panel Ethernet interface.
PICMG 2.16 Link and Activity LEDs.	Provides link and activity LEDs for the two 2.16 (rear panel) Ethernet interfaces.
Ethernet Port	RJ45 connection to 10/100/1000Mbps Ethernet Port.
Serial Port	Micro DB9 RS232 serial port.
PMC 1	PMC 1 Front Panel IO.
PMC 2	PMC 2 Front Panel IO.

2.4 Component Maps

Figure 2.4.1: Front Component Map (Rev D)

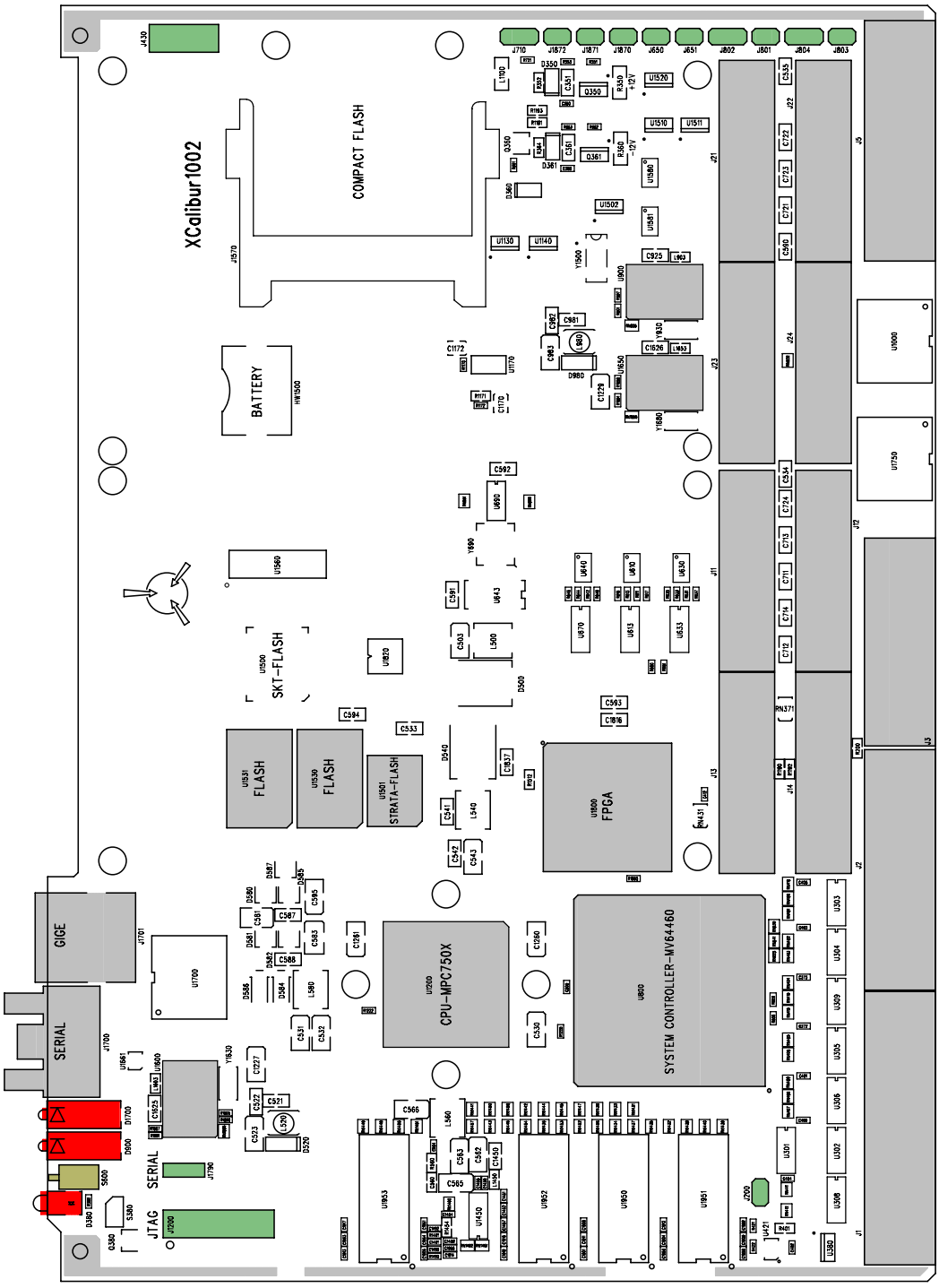
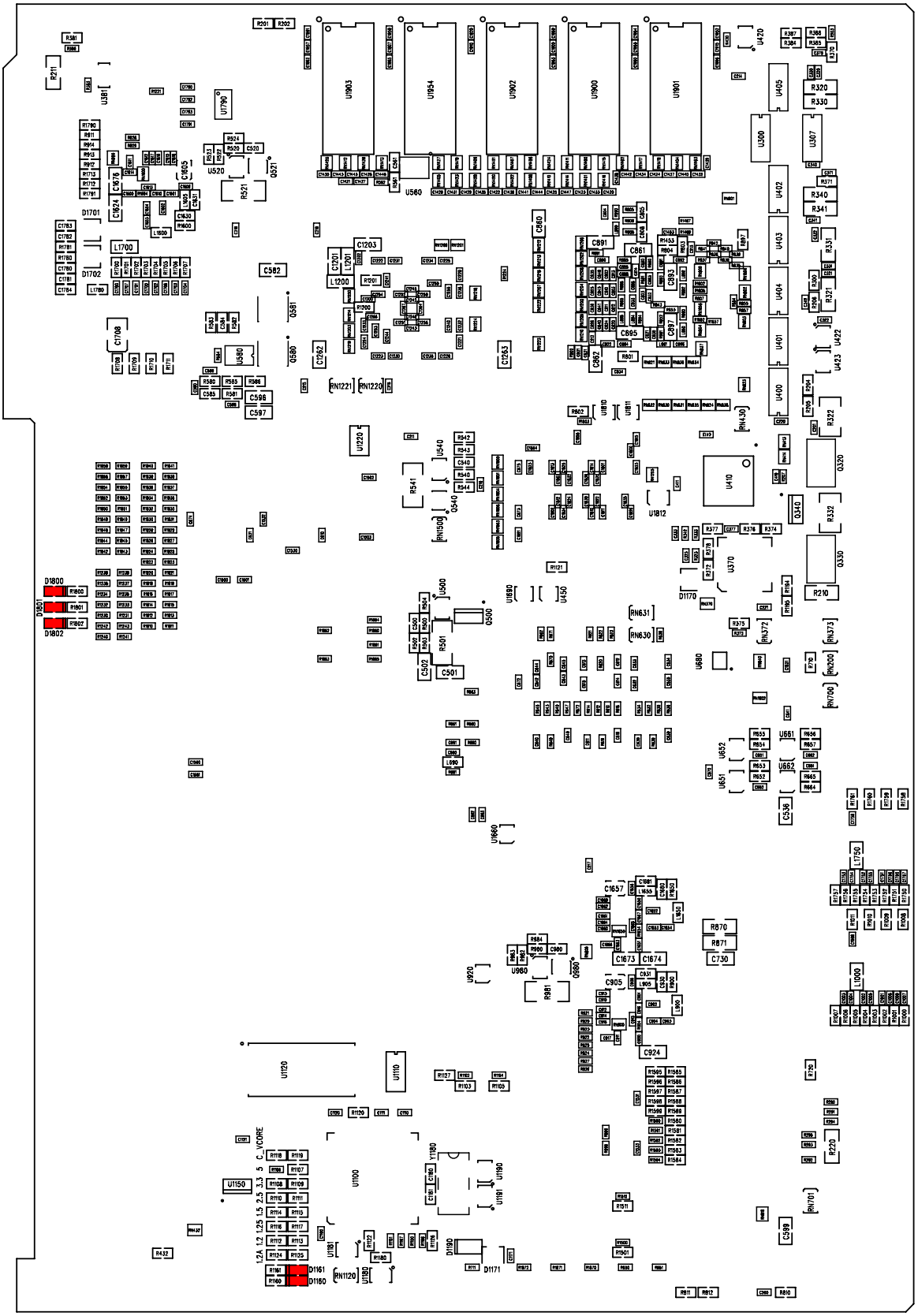


Figure 2.4.2: Back Component Map (Rev D)



2.5 Jumper Definitions

The following table gives a description of jumpers on XCalibur1002.

Table 2.5.1: Jumper Definitions

Jumper	Function
J200	**Force System Slot**. When installed, ignores the system slot auto detection mechanism and enables system slot functions. This is useful when XCalibur1002 is used in a standalone environment. NOTE: This jumper's header is not usually placed due to the potential for misuse.
J650	**Compact PCI-X Rate**. Indicates the maximum operating frequency of the CompactPCI PCI-X interface. When installed the bus is capable of operating at 133MHz, otherwise 100MHz operation is assumed.
J651	**Local PCI-X Rate**. Same function as **J650** (except for Local bus).
J710	**PrPMC MONARCH Selection**. When pins 1 and 2 are jumpered, indicates that PrPMC 1 is to provide local PCI bus enumeration and interrupt handling. When pins 2 and 3 are jumpered, indicates that PrPMC 2 is to provide local PCI bus enumeration and interrupt handling.
J801	**Local PCI Rate**. When installed this jumper forces the local PCI bus to 33MHz operation. When removed auto rate detection is used.
J802	**Local PCI Mode**. This jumper selects from three possible operating modes. When pins 1 and 2 jumpered the local PCI bus is forced to PCI operation. When pins 2 and 3 are jumpered the local PCI bus is forced to PCI-X operation and limited to 66MHz operation. When no jumper is installed auto detection is used to determine the PCI mode.
J803	**Compact PCI Rate**. Same function as **J801** except for Compact PCI.
J804	**Compact PCI Mode**. Same function as **J802** except for Compact PCI.
J1200	**750GX CPU JTAG Port.** Please refer to Section 6.7 "JTAG Debug Interface".
J1790	**IPMI Debug Header**. Serial port for IPMI controller.
J1870	**Socket Boot Flash Select**. When installed, indicates the socketed flash will be used as the boot device. Otherwise, Intel expansion flash will be utilized.
J1871	**CPU Disable**. When installed will prevent CPU from coming out of reset.
J1872	**MV64460 EEPROM boot disable**. When installed, will prevent MV64460 from fetching initialization parameters form an I2C EEPROM.

2.6 Debug Port Descriptions

XCalibur1002 provides headers to access various debug and programming interfaces. These interfaces are not typically used by the application, but are documented in the following table.

Table 2.6.1: Debug Port Descriptions

Header	Function
J430	**PLD JTAG Port**. The PLD JTAG port is used to program the CompactPCI Arbiter PLD on XCalibur1002. Call factory for details on this header.

Header	Function
J1200	**750GX CPU JTAG Port**. The750GX debug port is used to connect to external debug equipment. A detailed description and pin definition is defined in the CPU section of this manual
J1790	**Aux Debug Port**. The Auxiliary debug port is a RS232 serial port that provides access to the MV64460 MPSC1 or IPMB controller serial port.

2.7 Diagnostic LEDs

XCalibur1002 provides three surface mount diagnostic LEDs on the back of the PCB board. These LEDs are controlled by the STS, ACT, ALM bits in the MLED FPGA register. Please refer to the Local Services Chapter for more information.

Table 2.7.1: Diagnostic LEDs

LED	Function
D1800	**Green Status LED**. User definable surface mount LED. Off by default.
D1801	**Yellow Activity LED**. User definable surface mount LED. Off by default.
D1802	**Red Alarm LED**. User definable surface mount LED. On by default.

2.8 Environmental Requirements

Table 2.8.1: Environmental Requirements

Requirement	Specification
Operating Temperature	-40C to +85C, Ambient, At Board (266MHz or 333MHz DDR) 0 to +55C (400MHz DDR)
Humidity	0 to 85%
Storage Temperature	-40C to +85C

2.9 Power Requirements

The following table gives the power requirements of XCalibur1002, Revision D. Note: these power calculations do not include PMC module usage.

Table 2.9.1: Power Requirements*

Voltage	Current	Power
+3.3V	3.03A	10.0W
+5.0V	3.0A	15.0W
+12.0V	0.0A	0.0W
-12.0V	0.0A	0.0W

*Test Conditions: 1.0GHz 750GX CPU, 512MB 400MHz DDR, 30 C Ambient Temperature, 300LFM Airflow. Note that power consumption will increase at higher ambient temperatures.

3. Setup & Troubleshooting

This chapter describes the setup process and how to check for proper operation once the board has been installed. The chapter also includes troubleshooting, service, and warranty information.

3.1 Electrostatic Discharge

When handling this product, please remember that electrostatic discharge (ESD) can easily damage the components on this module and result in board failure. Unless you ground yourself properly, static can build in your body and cause ESD damage when you touch the board. To ground yourself, wear a grounding wriststrap. Simply placing this module on a static-shielding bag offers no protection -- place it on a grounded ESD-safe mat. Do not place this board on metal or other conductive surfaces. When this board is not in use or in an enclosure, store it in either a static-shielding bag or clamshell provided.

CAUTION: Use proper ESD procedures and handle this board only when absolutely necessary. Always wear a wriststrap while handling this board. Hold this board by the edges. Do not touch any components or circuits. Store in ESD safe bag when not in use.

3.2 Setup

You need the following items to set up and check the operation of the XCalibur1002. Items in bold are supplied by or optionally available from X-ES.

Table 3.2.1: Setup Requirements

	Pre-Startup Checklist
❑	**XCalibur1002 module**
❑	Compatible 6U CompactPCI backplane
❑	Chassis and/or Power supply
❑	**XCalibur1002 Serial Cable (optional)**
❑	Terminal

3.3 Check Power Supply

Verify that your power supply or host module is sufficient for the board. See "Power Requirements" on page 2-7 for the XCalibur1002 module's power requirements.

3.4 Installation / Removal

XCalibur1002 is a hot swap CompactPCI card. It can be inserted into and removed from an active CompactPCI backplane. The process for installing and removing XCalibur1002 is indicated in the following tables.

Table 3.4.1: Installation Procedure

Step	Procedure
1	Operator inserts XCalibur1002 card into CompactPCI slot and pushes card into backplane without latching handles. Blue Hot Swap LED lights indicating BD_SEL# has not yet been asserted.
2	Operator fully seats XCalibur1002 in CompactPCI slot and latches hot swap handles. Hardware indicates hardware connection process complete by turning off blue hot swap LED.

Table 3.4.2: Removal Procedure

Step	Procedure
1	Operator unlatches hot swap handles. System detects removal initiated and begins removal process.
2	System software indicates hardware removal process complete by lighting blue hot swap LED.
3	Operator removes XCalibur1002 from system.

CAUTION: To avoid damaging the module and/or baseboard, do not force the module onto the baseboard.

3.5 Troubleshooting

In case of difficulty, use this checklist:

Table 3.5.1: Troubleshooting Checklist

	Troubleshooting Checklist
❑	Be sure the XCalibur1002 is fully seated into the backplane.
❑	Be sure the system is not overheating
❑	Check the cables and connectors to be certain they are secure.
❑	If you are using the XCalibur1002 xMon, check that your terminal is connected to the serial and verify that the baud rate is set to 9600.
❑	If you are using the XCalibur1002 xMon, check the results of the power on self-test (POST). See XCalibur1002 xMon manual for more details.
❑	Check your power supply for proper DC voltages. If possible, use an oscilloscope to look for excessive power supply ripple or noise. On the back of the XCalibur1002 PCB are labeled test points for each of the card voltages.

3.6 Technical Support

If you have verified the above items, send an email to support@xes-inc.com (or call 1-608-833-1155) and ask for technical support from our support system. Please have the following information handy:

- XCalibur1002 board serial number
- Backplane model number
- Operating System and version
- xMon monitor version (if applicable)
- Any custom modifications/additions to your board (i.e. PMCs, etc.)

To determine the serial number of your board, look for the white sticker attached to the PCB. The sticker will contain the product part number (90050030) as well as the 8 digit serial number.

3.7 Service Information

If you plan to return the board to X-ES for service, send an email to support@xes-inc.com (or call 1-608-833-1155) and ask for a Return Merchandise Authorization (RMA) number. We will ask which items you are returning, the board serial numbers, reason for return, plus your purchase order number. If you are returning hardware that is out of warranty, we will require billing information as well. Contact us at support@xes-inc.com for any warranty questions. When returning any product, be sure to enclose it in an anti-static bag or clamshell, such as the original shipping material. Send it pre-paid to:

Extreme Engineering Solutions, Inc.
3225 Deming Way, Ste. 120
Middleton, WI 53562-1408

RMA#_____

Our service department cannot accept material returned without an RMA number.

4. CompactPCI Interface

XCalibur1002 is a 6U CompactPCI card that conforms to the PICMG 2.0 specification.

XCalibur1002 is capable of autosensing between system controller and peripheral slot operation. As system controller, XCalibur1002 provides CompactPCI bus arbitration, reset generation, clock distribution, and bus pullups.

XCalibur1002 complies with the PICMG 2.1 CompactPCI Hot Swap Specification. This board can be installed and removed from an operating CompactPCI bus without disturbing bus activity. In addition, the card can be powered down in a high availability system.

The PCI 2.2 compliant interface is implemented in the Marvell Discovery III system controller. This controller provides a 64 bit interface capable of operating at either 33MHz or 66MHz in PCI mode, and operating at 66MHz to 133MHz in PCI-X mode. Operting the CPCI interface in PCI-X mode requires a hardware build option to let the Discovery III perform bus arbitration instead of the onboard PLD.

4.1 System Controller PCI Memory Map

When installed in the system controller slot, the following default memory map applies to the CompactPCI bus interface at reset.

Table 4.1.1: Default PCI Memory Map

Address	Device
0xFF80,0000 - 0xFFFF,FFFF	Boot CS
0xFF00,0000 - 0xFF7F,FFFF	Device CS3
0xF101,0000 - 0xFEFF,FFFF	Reserved
0xF100,0000 - 0xF100,FFFF	MV64460 Internal Registers
0x4204,0000 - 0xF0FF,FFFF	Reserved
0x4200,0000 - 0x4203,FFFF	Integrated SRAM
0x4000,0000 - 0x41FF,FFFF	CPU
0x2600,0000 - 0x3FFF,FFFF	Reserved
0x2400,0000 - 0x25FF,FFFF	PCI to PCI Memory 1
0x2200,0000 - 0x23FF,FFFF	PCI to PCI Memory 0
0x2000,0000 - 0x21FF,FFFF	PCI to PCI I/O
0x1E00,0000 - 0x1FFF,FFFF	Reserved
0x1D00,0000 - 0x1DFF,FFFF	Device CS2
0x1C80,0000 - 0x1CFF,FFFF	Device CS1
0x1C00,0000 - 0x1C7F,FFFF	Device CS0
0x0200,0000 - 0x1BFF,FFFF	Reserved
0x0180,0000 - 0x01FF,FFFF	SDRAM Bank 3
0x0100,0000 - 0x017F,FFFF	SDRAM Bank 2

Address	Device
0x0080,0000 - 0x00FF,FFFF	SDRAM Bank 1
0x0000,0000 - 0x007F,FFFF	SDRAM Bank 0

When installed in the system controller slot, the following memory map applies to the CompactPCI bus interface as configured by the xMon monitor.

Table 4.1.2: xMon PCI Memory Map (current as of xMon S2.17)

Address	Device
0xF100,1000 - 0xFFFF,FFFF	Reserved
0xF100,0000 - 0xF100,0FFF	GT64460 Internal Registers
0xF000,0000 - 0xF0FF,FFFF	IO Mapped Devices (Autoconfigured)
0xF000,0000 - 0xF07F,FFFF	Reserved
0xA000,0000 - 0xBFFF,FFFF	Memory Mapped Devices (Autoconfigured)
0x4000,0000 - 0x9FFF,FFFF	Reserved
0x0000,0000 - 0x3FFF,FFFF	MV64460 SDRAM (Up to 1GB)

4.2 System Controller Arbitration

When installed in the system controller slot, XCalibur1001 provides CompactPCI bus arbitration. Arbitration can be disabled through the LARB bit of the CPCFG FPGA register. Please refer to the Local Services chapter for more information regarding this bit. The CPCI Bus arbiter is implemented either in an Altera 703A PLD in PCI Mode or by the Marvell MV64460 Discovery III chip when in PCI-X Mode.

Table 4.2.1: PLD Arbiter Assignments in PCI Mode

Arbiter Assignment	CompactPCI Assignment
REQ1 / GNT1	J1 REQ/GNT
REQ2 / GNT2	J2 REQ1/GNT1
REQ3 / GNT3	J2 REQ2/GNT2
REQ4 / GNT4	J2 REQ3/GNT3
REQ5 / GNT5	J2 REQ4/GNT4
REQ6 / GNT6	J2 REQ5/GNT5
REQ7 / GNT7	J2 REQ6/GNT6
REQ8 / GNT8	MV64460 REQ/GNT

Note: When configured as a peripheral card the GNT [1] / REQ [1] pair is used for CPCI bus arbitration.

Table 4.2.2: MV64460 Arbitration Assignments in PCI-X Mode

GPP Pins	Function	CompactPCI Assignment
GPP[16] / GPP[17]	GNT[0] / REQ[0]	J1 REQ/GNT
GPP[18] / GPP[19]	GNT[1] / REQ[1]	J2 REQ1/GNT1

GPP Pins	Function	CompactPCI Assignment
GPP[20] / GPP[21]	GNT[2] / REQ[2]	J2 REQ2/GNT2
GPP[22] / GPP[23]	GNT[3] / REQ[3]	J2 REQ3/GNT3
GPP[24] / GPP[25]	GNT[4] / REQ[4]	J2 REQ4/GNT4
GPP[26] / GPP[27]	GNT[5] / REQ[5]	J2 REQ5/GNT5

4.3 Configuration space

The PCI interface's configuration space defines a standard programming model for configuring PCI devices. The configuration space registers are implemented by the Marvel Discovery III system controller and conforms to 66MHz PCI version 2.2 as well as 133MHz PCI-X. The following table illustrates the configuration space as defined by the PCI bus specification.

Table 4.3.1: PCI Configuration Registers - Function 0

Index	31 21	23 16	15 8	7 0
0	Device ID (0x6480)		Vendor ID (0x11AB)	
4	Status		Command	
8	Class Code (0x0E)	Subclass Code (0x00)	Standard Programming (0x01)	Revision ID
C	BIST Control	Header Type	Latency Timer	Cache Line Size
10	SDRAM CS[0] BAR LSW			
14	SDRAM CS[0] BAR MSW			
18	SDRAM CS[1] BAR LSW			
1C	SDRAM CS[1] BAR MSW			
20	Memory Mapped Internal BAR LSW			
24	Memory Mapped Internal BAR MSW			
28	Reserved			
2C	Subsystem ID		Subsystem Vendor ID	
30	Expansion ROM BAR			
34	Reserved			Cap. Ptr
38	Reserved			
3C	Max Lat.	Min Gnt	Int. Pin	Int. Line

Table 4.3.2: PCI Configuration Registers - Function 1

Index	31 21	23 16	15 8	7 0
0	Device ID (0x6480)		Vendor ID (0x11AB)	
4	Status		Command	
8	Class Code (0x0E)	Subclass Code (0x00)	Standard Programming (0x01)	Revision ID
C	BIST Control	Header Type	Latency Timer	Cache Line Size
10	SDRAM CS[2] BAR LSW			
14	SDRAM CS[2] BAR MSW			
18	SDRAM CS[3] BAR LSW			
1C	SDRAM CS[3] BAR MSW			
20	Internal SRAM BAR LSW			
24	Internal SRAM BAR MSW			
28	Reserved			
2C	Subsystem ID		Subsystem Vendor ID	
30	Reserved			
34	Reserved			Reserved
38	Reserved			
3C	Max Lat.	Min Gnt	Int. Pin	Int. Line

Table 4.3.3: PCI Configuration Registers - Function 2

Index	31 21	23 16	15 8	7 0
0	Device ID (0x6480)		Vendor ID (0x11AB)	
4	Status		Command	
8	Class Code (0x0E)	Subclass Code (0x00)	Standard Programming (0x01)	Revision ID
C	BIST Control	Header Type	Latency Timer	Cache Line Size
10	DevCS[0] BAR LSW			
14	DevCS[0] BAR MSW			
18	DevCS[1] BAR LSW			
1C	DevCS[1] BAR MSW			
20	DevCS[2] BAR LSW			
24	DevCS[2] BAR MSW			
28	Reserved			
2C	Subsystem ID		Subsystem Vendor ID	
30	Reserved			
34	Reserved			Reserved
38	Reserved			
3C	Max Lat.	Min Gnt	Int. Pin	Int. Line

Table 4.3.4: PCI Configuration Registers - Function 3

Index	31 21	23 16	15 8	7 0
0	Device ID (0x6480)		Vendor ID (0x11AB)	
4	Status		Command	
8	Class Code (0x0E)	Subclass Code (0x00)	Standard Programming (0x01)	Revision ID
C	BIST Control	Header Type	Latency Timer	Cache Line Size
10	DevCS[3] BAR LSW			
14	DevCS[3] BAR MSW			
18	BootCS LSW			
1C	BootCS MSW			
20	CPU BAR LSW			
24	CPU BAR MSW			
28	Reserved			
2C	Subsystem ID		Subsystem Vendor ID	
30	Reserved			
34	Reserved			Reserved
38	Reserved			
3C	Max Lat.	Min Gnt	Int. Pin	Int. Line

4.4 Interrupts

XCalibur1002 is capable of receiving interrupts as well as generating interrupts on pins INTA#, INTB#, INTC# and INTD#. Please refer to Local Services chapter for interrupt routing and generation information.

4.5 CompactPCI Pin Assignments

XCalibur1002 supports the CompactPCI standard through connectors J1 and J2. Connector J1 is required to provide power and for a minimum 32 bit wide PCI interface. Connector J2 is required for 64 bit PCI and for system slot functions. The following table defines the pin assignments for connector J1.

Table 4.5.1: J1 Connector Pin Assignments

Pin	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	PCIXCAP	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
14							
13	KEY AREA						
12							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	PCI_RST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND

Table 4.5.2: J2 Connector Pin Assignments

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	RSV	RSV	RSV	GND
20	GND	CLK5	GND	RSV	GND	RSV	GND
19	GND	GND	GND	SMBA-LERT	SMBSCL	SMB_SDA	GND
18	GND	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND
17	GND	BRSVP2A17	GND	PRST#	REQ6	GNT6	GND
16	GND	BRSVP2A16	BRSVP2B16	DEG#	GND	BRSVP2E16	GND
15	GND	BRSVP215	GND	FAL#	REQ5	GNT5	GND
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	V(I/0)	AD[37]	AD[36]	GND
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/BE[5]#	64EN	V(I/O)	C/BE[4]#	PAR64	GND
4	GND	V(I/O)	RSV	C/BE[7]#	GND	C/BE[6]#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Table 4.5.3: J3 Connector Pin Assignments

Pin	Z	A	B	C	D	E	F
19	GND	GND	GND	GND	GND	GND	GND
18	GND	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	GND
17	GND	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
16	GND	LPb_DA+	LPb_DA-	GND	LPb_DC+	LPb_DC-	GND
15	GND	LPb_DB+	LPb_DB-	GND	LPb_DD+	LPb_DD-	GND
14	GND	3.3V	3.3V	3.3V	5V	5V	GND
13	GND	P5	P4	P3	P2	P1	GND
12	GND	P10	P9	P8	P7	P6	GND
11	GND	P15	P14	P13	P12	P11	GND
10	GND	P20	P19	P18	P17	P16	GND
9	GND	P25	P24	P23	P22	P21	GND
8	GND	P30	P29	P28	P27	P26	GND
7	GND	P35	P34	P33	P32	P31	GND
6	GND	P40	P39	P38	P37	P36	GND
5	GND	P45	P44	P43	P42	P41	GND
4	GND	P50	P49	P48	P47	P46	GND
3	GND	P55	P54	P53	P52	P51	GND
2	GND	P60	P59	P58	P57	P56	GND
1	GND	V(I/O)	P64	P63	P62	P61	GND

Table 4.5.4: J5 Connector Pin Assignments

Pin	Z	A	B	C	D	E	F
22	GND	P5	P4	P3	P2	P1	GND
21	GND	P10	P9	P8	P7	P6	GND
20	GND	P15	P14	P13	P12	P11	GND
19	GND	P20	P19	P18	P17	P16	GND
18	GND	P25	P24	P23	P22	P21	GND
17	GND	P30	P29	P28	P27	P26	GND
16	GND	P35	P34	P33	P32	P31	GND
15	GND	P40	P39	P38	P37	P36	GND
14	GND	P45	P44	P43	P42	P41	GND
13	GND	P50	P49	P48	P47	P46	GND
12	GND	P55	P54	P53	P52	P51	GND
11	GND	P60	P59	P58	P57	P56	GND
10	GND	V(I/O)	P64	P63	P62	P61	GND
9	GND	GPIO_I3	GPIO_O1	GPIO_O5	RS232_RX0	RS232_RX1	GND
8	GND	GPIO_I2	GPIO_I5	GPIO_O4	NC	NC	GND
7	GND	GPIO_I1	GPIO_I4	GPIO_O3	RS232_TX0	RS232_TX1	GND
6	GND	IDE_A1	IDE_A0	GPIO_O2	NC	NC	GND
5	GND	IDE_IOR#	IDE_IOW#	IDE_IO16	IDE_CD1#	IDE_A2	GND
4	GND	IDE_D0	IDE_RST#	IDE_CS0#	IDE_CS1#	IDE_INT	GND
3	GND	IDE_D5	IDE_D4	IDE_D3	IDE_D2	IDE_D1	GND
2	GND	IDE_D10	IDE_D9	IDE_D8	IDE_D7	IDE_D6	GND
1	GND	IDE_D15	IDE_D14	IDE_D13	IDE_D12	IDE_D11	GND

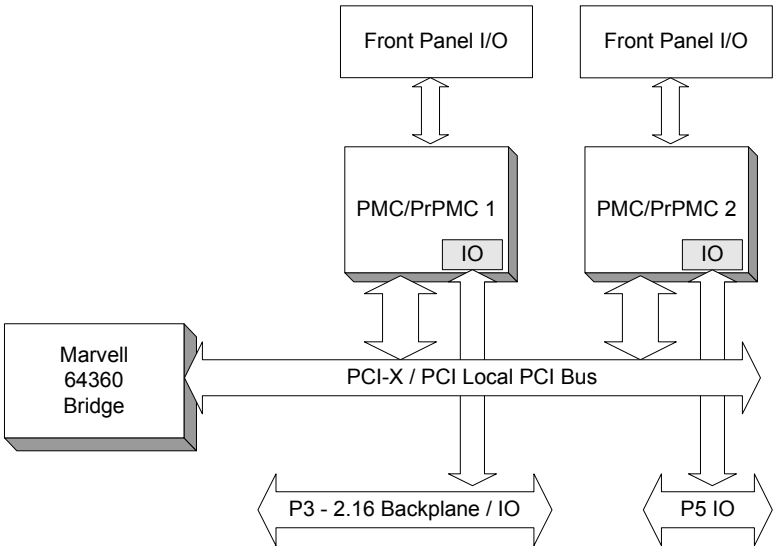
5. Local PCI Interface

XCalibur1002 has a 64 bit local PCI bus used to move data between the processor and peripheral devices. Devices on the local bus include the MV64460 bridge, and two PMC sites.

XCalibur1002 can host two single width PMC modules or a single double width PMC module. Stacking height for these modules is limited to 10mm. These modules can operate at 33MHz or 66MHz PCI, as well as up to 133MHz PCI-X. XCalibur1002 automatically adjusts bus frequency and mode depending on the abilities of the installed modules.

5.1 PCI Bus Block Diagram

Figure 5.1.1: PCI Bus Block Diagram



5.2 PCI Memory Map

Table 5.2.1: Default PCI Memory Map (at Reset)

Address	Device
0xFF80,0000 - 0xFFFF,FFFF	Boot CS
0xFF00,0000 - 0xFF7F,FFFF	Device CS3
0xF400,0000 - 0xFEFF,FFFF	Reserved
0xF200,0000 - 0xF3FF,FFFF	PCI to PCI Memory 1
0xF101,0000 - 0xF1FF,FFFF	Reserved
0xF100,0000 - 0xF100,FFFF	MV64460 Internal Registers
0x4204,0000 - 0xF0FF,FFFF	Reserved
0x4200,0000 - 0x4203,FFFF	Integrated SRAM
0x4000,0000 - 0x41FF,FFFF	CPU
0x1E00,0000 - 0x3FFF,FFFF	Reserved
0x1D00,0000 - 0x1DFF,FFFF	Device CS2
0x1C80,0000 - 0x1CFF,FFFF	Device CS1
0x1C00,0000 - 0x1C7F,FFFF	Device CS0
0x1400,0000 - 0x1BFF,FFFF	Reserved
0x1200,0000 - 0x13FF,FFFF	PCI to PCI Memory 0
0x1000,0000 - 0x11FF,FFFF	PCI to PCI I/O
0x0200,0000 - 0x0FFF,FFFF	Reserved
0x0180,0000 - 0x01FF,FFFF	SDRAM Bank 3
0x0100,0000 - 0x017F,FFFF	SDRAM Bank 2
0x0080,0000 - 0x00FF,FFFF	SDRAM Bank 1
0x0000,0000 - 0x007F,FFFF	SDRAM Bank 0

Table 5.2.2: xMon PCI Memory Map (current as of xMon S2.17)

Address	Device
0xF000,1000 - 0xFFFF,FFFF	Reserved
0xF100,0000 - 0xF000,0FFF	MV64460 Internal Registers
0xF080,0000 - 0xF0FF,FFFF	Reserved
0xF080,0000 - 0xF0FF,FFFF	IO Mapped Device (Autoconfigured)
0xa000,0000 - 0xFFFF,FFFF	Reserved
0x8000,0000 - 0x9FFF,FFFF	Memory Mapped Devices (Autoconfigured)
0x0000,0000 - 0x3FFF,FFFF	MV64460 SDRAM (Up to 1GB)

5.3 Device Configuration

The following PCI configuration address lines are assigned to the PMC sites. The PrPMC specification adds a second set of configuration and arbitration signals. These are connected to the Discovery III's internal PCI-X arbiter.

Table 5.3.1: PCI Configuration Mappings

Device	DEVSEL Address Line	INTA Line
MV64460	AD16	FPGA Interrupt Input
PMC 1A	AD17	INTB
PMC 1B	AD21	INTB
PMC 2A	AD18	INTC
PMC 2B	AD22	INTC

5.4 Mode and Speed Selection

The local PCI bus will automatically adjust mode (PCI versus PCI-X) and speed (33, 66, 100, 133 MHz) depending on the devices installed on the local bus. However, the PCI bus mode and speed can be forced using the following jumpers.

Table 5.4.1: Mode and Speed Selection

J651	**Local PCI-X Rate**. Indicates the maximum operating frequency of the Local PCI-X interface. When installed the bus is capable of operating at 133MHz, otherwise 100MHz operation is assumed.
J801	**Local PCI Rate**. When installed this jumper forces the local PCI bus to 33MHz operation. When removed auto rate detection is used.
J802	**Local PCI Mode**. This jumper selects from three possible operating modes. When pins 1 and 2 jumpered the local PCI bus is forced to PCI operation. When pins 2 and 3 are jumpered the local PCI bus is forced to PCI-X operation and limited to 66MHz operation. When no jumper is installed auto detection is used to determine the PCI mode.

5.5 PMC I/O

PMC P14 I/O is routed to the CompactPCI Connectors J3 and J5 in accordance with the specification PICMG 23. Please refer to the CompactPCI Pin Assignments section for J3 and J5 connector pin assignments. In addition, signals have been routed differentially to support high speed I/O standards. Please refer to the PMC I/O section of this manual.

5.6 PrPMC Support

XCalibur1002 supports the Processor PMC (PrPMC) standard. This includes the following PrPMC signals.

Table 5.6.1: PrPMC Support Signals

PMC	CompactPCI Interface
RESET_OUT#	An open drain output of the PrPMC module, this signal allows the PMC module to reset the system. In CompactPCI system controller mode, this also will reset the CompactPCI backplane.

PMC	CompactPCI Interface
MONARCH	An input of the PrPMC module. Determines if the processor PMC should perform local PCI bus enumeration and interrupt handling. This feature can be enabled through a jumper on the XCalibur1002.
EREADY	An input to a MONARCH PrPMC module which indicates that the carrier card has performed all necessary device configuration. As an output from a non-MONARCH PrPMC module which indicates that the PrPMC is ready to be enumerated on the local PCI bus.
IDSELB	A second IDSEL line for the PrPMC module. This allows the PrPMC module to implement two PCI devices on the bus.
REQB#/GNTB#	A second set of arbitration lines for the PrPMC module. This allows the PrPMC module to implement two PCI devices on the bus.

5.7 PCI-X Support

XCalibur1002 supports the PCI-X standard operating at up to 133MHz. This includes the following PCI-X signals.

Table 5.7.1: PCI-X Support Signals

PMC	CompactPCI Interface
PCIXCAP	Indicates if modules are capable of PCI-X operation and, if so, at what frequency. Conventional cards connect this pin to ground. PCI-X 66MHz cards connect this pin to ground through a 10K ohm resistor. PCI-X 133MHz cards leave this connection open.

5.8 PMC Pin Assignments

Table 5.8.1: J11/J12 Connector Pin Assignments

Pin	J11	J12	Pin	J11	J12
1	-	+12V	2	-12V	-
3	GROUND	-	4	INTA#	-
5	INTB#	-	6	INTC#	GROUND
7	PRESENT#	GROUND	8	+5V	-
9	INTD#	-	10	-	-
11	GROUND	PUP	12	-	+3.3V
13	CLK	RST*	14	GROUND	PDN
15	GROUND	+3.3V	16	GNT#	PDN
17	REQ#	-	18	+5V	GROUND
19	VIO	AD30	20	AD31	AD29
21	AD28	GROUND	22	AD27	AD26
23	AD25	AD24	24	GROUND	+3.3V
25	GROUND	IDSEL	26	C/BE3#	AD23
27	AD22	+3.3V	28	AD21	AD20
29	AD19	AD18	30	+5V	GROUND
31	VIO	AD16	32	AD17	C/BE2#
33	FRAME#	GROUND	34	GROUND	IDSELB
35	GROUND	TRDY#	36	IRDY#	+3.3V
37	DEVSEL#	GROUND	38	+5V	STOP#
39	PCIXCAP	PERR*	40	LOCK#	GROUND
41	-	+3.3V	42	-	SERR#
43	PAR	C/BE1#	44	GROUND	GROUND
45	VIO	AD14	46	AD15	AD13
47	AD12	M66EN	48	AD11	AD10
49	AD9	AD8	50	+5V	+3.3V
51	GROUND	AD7	52	C/BE0#	REQB#
53	AD6	+3.3V	54	AD5	GNTB#
55	AD4	-	56	GROUND	GROUND
57	VIO	-	58	AD3	EREADY
59	AD02	GROUND	60	AD1	RESETOUT#
61	AD0	ACK64#	62	+5V	+3.3V
63	GROUND	GROUND	64	REQ64#	MONARCH#

Table 5.8.2: J13/J14 Connector Pin Assignments

Pin	J13	J14	Pin	J13	J14
1	NC	C[1] / P[0]+	2	GND	A[1] / P[1]+
3	GND	C[2] / P[1]-	4	C/BE[7]#	A[2] / P[2]+
5	C/BE[6]#	C[3] / P[2]-	6	C/BE[5]#	A[3] / P[0]-
7	C/BE[4]#	C[4] / P[3]+	8	GND	A[4] / P[3]-
9	V(I/O)	C[5] / P[4]+	10	PAR64	A[5] / P[4]-
11	AD[63]	C[6] / P[5]+	12	AD[62]	A[6] / P[6]+
13	AD[61]	C[7] / P[6]-	14	GND	A[7] / P[7]+
15	GND	C[8] / P[7]-	16	AD[60]	A[8] / P[5]-
17	AD[59]	C[9] / P[8]+	18	AD[58]	A[9] / P[8]-
19	AD[57]	C[10] / P[9]+	20	GND	A[10] / P[9]-
21	V(I/O)	C[11] / P[10]+	22	AD[56]	A[11] / P[11]+
23	AD[55]	C[12] / P[11]-	24	AD[54]	A[12] / P[12]+
25	AD[53]	C[13] / P[12]-	26	GND	A[13] / P[10]-
27	GND	C[14] / P[13]+	28	AD[52]	A[14] / P[13]-
29	AD[51]	C[15] / P[14]+	30	AD[50]	A[15] / P[14]-
31	AD[49]	C[16] / P[15]+	32	GND	A[16] / P[16]+
33	GND	C[17] / P[16]-	34	AD[48]	A[17] / P[17]+
35	AD[47]	C[18] / P[17]-	36	AD[46]	A[18] / P[15]-
37	AD[45]	C[19] / P[18]+	38	GND	A[19] / P[18]-
39	V(I/O)	C[20] / P[19]+	40	AD[44]	A[20] / P[19]-
41	AD[43]	C[21] / P[20]+	42	AD[42]	A[21] / P[21]+
43	AD[41]	C[22] / P[21]-	44	GND	A[22] / P[22]+
45	GND	C[23] / P[22]-	46	AD[40]	A[23] / P[19]-
47	AD[39]	C[24] / P[23]+	48	AD[38]	A[24]/ P[23]-
49	AD[37]	C[25] / P[24]+	50	GND	A[25] / P[24]-
51	GND	C[26] / P[25]+	52	AD[36]	A[26] / P[26]+
53	AD[35]	C[27] / P[26]-	54	AD[34]	A[27] / P[27]+
55	AD[33]	C[28] / P[27]-	56	GND	A[28] / P[25]-
57	V(I/O)	C[29] / P[28]+	58	AD[32]	A[29] / P[28]-
59	NC	C[30] / P[29]+	60	NC	A[30] / P[29]-
61	NC	C[31] / P[30]+	62	GND	A[31] / P[31]+
63	GND	C[32] / P[31]-	64	NC	A[32] / P[30]-

Note: P14 is routed to support the requirements of high speed differential IO. Each pair is specified by a P[n]+ and P[n]-, where n is the pair number.

6. CPU

This chapter provides a description of the IBM 750GX processor and its on-card resources.

XCalibur1002 utilizes the IBM PowerPC 750GX processor operating internally up to 1GHz. In addition, 32KB L1 instruction and data caches are provided, as well as an on-board 1MB L2 Cache. The CPU 60x bus interface operates at 133MHz-200MHz depending on build options. The 60x bus always runs at the same frequency (single data rate) as the DDR SDRAM interface. I.e. a 200MHz 60x bus translates to a 400MHz DDR SDRAM interface.

6.1 Memory Map

NOTE: The below memory map is only applicable when the card is in reset (i.e. before xMon has booted).

Table 6.1.1: Default Memory Map

Address	Device
0xFF80,0000 - 0xFFFF,FFFF	Socketed Flash (512KB)
0xFF00,0000 - 0xFF7F,FFF	Device 3 (Reserved)
0xF800,0000 - 0xFEFF,FFFF	Reserved
0xF600,0000 - 0xF7FF,FFFF	Compact PCI Memory Space 3
0xF400,0000 - 0xF5FF,FFFF	Compact PCI Memory Space 2
0xF200,0000 - 0xF3FF,FFFF	Compact PCI Memory Space 1
0xF101,0000 - 0xF1FF,FFFF	Reserved
0xF100,0000 - 0xF100,FFFF	MV64460 Internal Registers
0x4204,0000 - 0xF0FF,FFFF	Reserved
0x4200,0000 - 0x4203,FFFF	MV64460 Internal SRAM
0x2A00,0000 - 0x41FF,FFFF	Reserved
0x2800,0000 - 0x29FF,FFFF	Local PCI Memory Space 3
0x2600,0000 - 0x27FF,FFFF	Local PCI Memory Space 2
0x2400,0000 - 0x25FF,FFFF	Local PCI Memory Space 1
0x2200,0000 - 0x23FF,FFFF	Local PCI Memory Space 0
0x2000,0000 - 0x21FF,FFFF	Local PCI IO Space
0x1E00,0000 - 0x1FFF,FFFF	Reserved
0x1D00,0000 - 0x1DFF,FFFF	Device 2 - IDE / CompactFlash Registers
0x1C80,0000 - 0x1CFF,FFFF	Device 1 - FPGA
0x1C00,0000 - 0x1C7F,FFFF	Device 0 - Expansion Flash
0x1400,0000 - 0x1BFF,FFFF	Reserved
0x1200,0000 - 0x13FF,FFFF	Compact PCI Memory Space 0
0x1000,0000 - 0x11FF,FFFF	CompactPCI IO Space
0x0200,0000 - 0x0FFF,FFFF	Reserved
0x0180,0000 - 0x01FF,FFFF	SDRAM Bank 3
0x0100,0000 - 0x017F,FFFF	SDRAM Bank 2
0x0080,0000 - 0x00FF,FFFF	SDRAM Bank 1
0x0000,0000 - 0x007F,FFFF	SDRAM Bank 0

Table 6.1.2: xMon Memory Map (Current as of xMon S2.17)

Address	Device
0xF800,0000 - 0xFFFF,FFFF	Socketed Flash
0xF400,0000 - 0xF7FF,FFFF	Expansion Flash
0xF130,0000 - 0xF3FF,FFFF	Reserved
0xF120,0000 - 0xF12F,FFFF	IDE / CompactFlash Registers
0xF118,8000 - 0xF11F,FFFF	Reserved
0xF118,0000 - 0xF118,7FFF	Ramtron FRAM (32KB)
0xF111,0000 - 0xF117,FFFF	Reserved
0xF110,0000 - 0xF110,FFFF	FPGA Registers
0xF108,0000 - 0xF10F,FFFF	MV64460 Internal SRAM
0xF100,0000 - 0xF100,FFFF	MV64460 Internal Registers
0xF080,0000 - 0xF0FF,FFFF	PCI I/O Space (Marvell PCI1)
0xF000,0000 - 0xF07F,FFFF	PCI I/O Space (Marvell PCI0)
0xE800,0000 - 0xEFFF,FFFF	Expansion Flash/Storage Flash
0xE000,0000 - 0xE7FF,FFFF	Storage Flash
0xC000,0000 - 0xDFFF,FFFF	Reserved
0xA000,0000 - 0xBFFF,FFFF	PCI Memory Space (Marvell PCI0)
0x8000,0000 - 0x9FFF,FFFF	PCI Memory Space (Marvell PCI1)
0x0000,0000 - 0x7FFF,FFFF	SDRAM (Up to 2GB)

6.2 Flash Memory

XCalibur1002 supports up to 16MB of surface mount memory and 512KB of socketed memory. In addition, an IDE interface is provided through the FPGA for bulk storage. Please refer to IDE / CompactFlash chapter for more information regarding the IDE interface.

Table 6.2.1: Flash Devices

Function	Device
Socketed Flash	AMD AM29LV040B
Expansion Flash	Intel StrataFlash 28F128J3A
Storage Flash 0 (optional)	AMD Mirrorbit
Storage Flash 1 (optional)	AMD Mirrobit

6.3 DDR SDRAM Memory

The XCalibur1002 supports up to 1GB of SDRAM. Please refer to the Discovery III user's manual for memory controller configuration.

Table 6.3.1: Memory Map

Memory Address Range	Memory Size
0x0000,0000 to 0x0000,0000	0MB
0x0000,0000 to 0x0800,0000	128MB
0x0000,0000 to 0x1000,0000	256MB
0x0000,0000 to 0x2000,0000	512MB
0x0000,0000 to 0x4000,0000	1GB

6.4 Real-Time Clock

A real-time clock is provided on XCalibur1002 by the ST Microelectronics M41T00 Serial Access Timekeeper. This device utilizes a battery backed real-time clock.

6.5 Boot Mode

When XCalibur1002 is first brought out of reset, the flash interface is initialized in boot-strap mode. In this mode, the first 64KB of the flash boot device is mapped to FFF0,0000. Therefore the first instruction executed is located at offset 0x100 into the flash device. Boot mode is exited when a flash access outside of the 64KB boot window is performed.

An absolute jump instruction to the correct flash memory map must be placed within the first 64KB of the flash to disable boot mode.

6.6 Exception Handling

The XCalibur1002 interrupt controller is implemented in the FPGA and the Discovery III. The Discovery III's interrupt controller is effectively cascaded (by software) into the FPGA interrupt controller, with the FPGA as master (closest to CPU). Access to the FPGA interrupt controller is provided through the device interface bus of the Discovery III. Please refer to the Discovery III user's manual for information on configuring the device interface bus and internal interrupt controller. The following external interrupts (non-Discovery III sourced) are available. Please refer to the Local Services chapter for more information regarding the FPGA.

Table 6.6.1: Interrupt Sources

Interrupt Source	Description
ETH0	Front Panel Gigabit Ethernet Port 0. The source of this interrupt is the INTR# pin on the BCM5421 Gigabit Ethernet PHY.
ETH1	2.16 Gigabit Ethernet Port 0. The source of this interrupt is the INTR# pin on the BCM5421 Gigabit Ethernet PHY.
ETH2	2.16 Gigabit Ethernet Port 1. The source of this interrupt is the INTR# pin on the BCM5421 Gigabit Ethernet PHY.
CF	Compact Flash. The True-IDE mode interrupt source for the CompactFlash Card.
IDE	Transition Module IDE. The True-IDE mode interrupt source for the transition module IDE interface.
ENUM	CompactPCI Enumeration Interrupt. When a hot-swap card is installed, or about to be removed, from a system, this interrupt is asserted.
CPU	CPU Checkstop. Asserted when CPU 0 executes a checkstop.
DISCS	Discovery III Secondary PCI Bus. Asserted when the Discovery II generates a local PCI bus interrupt.
DISCP	Discovery III Primary PCI Bus. Asserted when the Discovery II generates a CompactPCI bus interrupt.
DISCC0	Discovery III CPU 0. Asserted when the Discovery II generates a CPU 0 interrupt.
DISCC1	Discovery III CPU 1. Asserted when the Discovery II generates a CPU 1 interrupt.
IPMI	IPMI Microcontroller. Asserted when the IPMI microcontroller generates an interrupt.
LINT	Local PCI interrupts A-D. Asserted by PMC modules.
CINT	CompactPCI interrupts A-D. Asserted by CompactPCI modules.
DEG	CompactPCI Power Degrade Signal. Asserted by backplane/power supply.
FAL	CompactPCI Power Fail Signal. Asserted by backplane/power supply.

6.7 JTAG Debug Interface

The 750GX implements a JTAG interface to support system debugging. The interface enables the connection of an external debug tools, such as RISCWatch. XCalibur1002 supports this capability by providing a debug header that can be attached to the external debug tools. The pinout of the debug header is defined in the following table.

Table 6.7.1: 750GX JTAG Header Pin Assignment

Pin	Function	Pin	Function
1	TDO	9	TMS
2	-	10	-
3	TDI	11	SRESET#
4	TRST	12	GND
5	-	13	HRESET#
6	2.5 V	14	-
7	TCK	15	CKSTOP_OUT#
8	-	16	GND

Note: The JTAG port uses 2.5V Signaling.

7. System Controller

This chapter provides a description of the Marvell Discovery III and how XCalibur1002 utilizes it's resources.

The Discovery III provides two integrated PCI bus interfaces, a DDR SDRAM memory controller, three integrated gigabit ethernet controllers, a device bus interface, as well as a PowerPC 60x bus interface.

7.1 Reset Configuration

The MV64460 initializes internal registers by sampling IO pins upon removal of reset. The following table describes the configuration as provided by the XCalibur1002. Please refer to the MV64460 manual for specific configuration details.

Table 7.1.1: Reset Configuration Words

Pins	Configuration Value
DEVAD[31:29]	Configured based on CompactPCI Bus Speed and Mode.
DEVAD[28:26]	Configured based on Local PCI Bus Speed and Mode.
DEVAD[25:1]	0b00000111101011000010011001
DEVAD[0]	Configured base on the MV64460 Serial ROM Initialization Enable Jumper (J1872).
DEVWE[3:0]	0b0000
DEVDP[3:0]	0b0000
DEVBA[2:0]	0b101
TXD0[7:0]	0b00000000
TXD1[4:0]	0b00000

7.2 DDR SDRAM Controller

The Discovery III provides an integrated DDR SDRAM controller capable of operating at up 183MHz (366MHz Data Rate). The following table gives the chip select usage for the XCalibur1002. Please refer to the MV64460 manual for more information on configuring and operating the memory interface.

Table 7.2.1: SDRAM Chip Select Assignment

Chip Select	Device
CS 0	Bank 0
CS 1	Not Used
CS 2	Not Used
CS 3	Not Used

7.3 Ethernet Controllers

The Discovery II| provides three integrated gigabit ethernet controllers. The following table gives the ethernet controller assignments on XCalibur1002. Please refer to the Discovery II hardware manual for configuring and operating the ethernet controllers.

Table 7.3.1: Ethernet Controller Assignment

Ethernet Controller	Port Mode	Usage on XCalibur1002
Port 0	RGMII	Front Panel Gigabit
Port 1	RGMII	2.16 Gigabit Port A
Port 2	RGMII	2.16 Gigabit Port B

The three Discovery III ethernet controller ports interface with three Broadcom BCM5421 10/100/1000 Mbps PHYs. The MV64460 provides a serial management interface (SMI) for configuring and monitoring the Ethernet PHYs. The address assignments of the Broadcom BCM5421s can be found in the following table.

Table 7.3.2: Ethernet Controller Assignment

PHY Address	Device
0x04	BCM5461 Ethernet Controller 0
0x08	BCM5461 Ethernet Controller 1
0x10	BCM5461 Ethernet Controller 2

The pinout from the front panel RJ45s can be found in the following table.

Table 7.3.3: Ethernet RJ45 Pinout

Pin	Function
1	MX0+
2	MX0-
3	MX1+
4	MX2+

Pin	Function
5	MX2-
6	MX1-
7	MX3+
8	MX3-

7.4 Serial Controllers

The Discovery III provides two multi-purpose serial controllers (MPSC). The following table gives the serial controller assignments on XCalibur1002. The BClkIn pin (GPP[29]) provides a constant 25MHz clock for baud rate generation.

Table 7.4.1: MPSC Assignment

Serial Controller	Usage on XCalibur1002
MPSC 0	Front / Back Panel RS232
MPSC 1	Back Panel RS232

The MPSC port interfaces with a Maxim 3232 RS232 transceiver. The front panel pinout can be found in the following table.

Table 7.4.2: Front RS232 Micro DB9 Pinout

Pin	Function
1	-
2	RXD(intput)
3	TXD(output)
4	-

Pin	Function
5	GND
6	-
7	-
8	-

Table 7.4.3: Back RS232 J5 Pinout

Serial Controller	Transmit J5 Pin	Receive J5 Pin
MPSC 0	E8	E6
MPSC 1	D8	D6

7.5 I2C Controller

The Discovery III provides an I2C controller. The following devices are located on the I2C bus.

I2C Address	Size	I2C Device Description
1101000	-	STMicroelectronics MT41T00 Real Time Clock.
1010000	512 Bytes	Fairchild FM24C04 I2C EEPROM. Used to store non-volatile configuration information and Discovery II| configuration information.
1010101	256 Bytes	SDRAM Configuration information.
0011000	256 Bytes	Philips PCA9556 GPIO 5 Input Device. Inputs 1-5 are used.
0011001	256 Bytes	Philips PCA9556 GPIO 5 Output Device. Outputs 1-5 are used.

7.6 Device Controller

The Discovery III provides a device bus for interfacing with peripherals. The following table gives the peripherals assigned to the chip selects provided by the Discovery III.

Table 7.6.1: Device Chip Select Assignment

Chip Select	Width	Peripheral Device
Boot Device	32 bit	Boot Device / Socketed Flash
Device 0	32 bit	Expansion Flash
Device 1	32 bit	FPGA
Device 2	16 bit	IDE / CompactFlash
Device 3	32 bit	AMD Mirrorbit Flash (2 Devices, Optional)

7.7 PCI Bus Arbitration

The Discovery III provides internal PCI bus arbiters for the primary and secondary buses. The following tables give the multipurpose port pin assignments for the arbitration signals.

Table 7.7.1: Local PCI Bus Arbitration Assignment

GPP Pins	Function	Local PCI Device
GPP[0] / GPP[1]	GNT[0] / REQ[0]	PrPMC 1A
GPP[2] / GPP[3]	GNT[1] / REQ[1]	PrPMC 1B
GPP[4] / GPP[5]	GNT[2] / REQ[2]	PrPMC 2A
GPP[6] / GPP[7]	GNT[3] / REQ[3]	PrPMC 2B

The Discovery III CompactPCI arbiter should only be used if CompactPCI PCI-X mode is enabled, as the Discovery III only allows arbitration for 6 peripheral CompactPCI slots. The PLD arbiter allows arbitration for all 7 peripheral slots.

Table 7.7.2: CompactPCI Bus Arbitration Assignment

GPP Pins	Function	Local PCI Device
GPP[16] / GPP[17]	GNT[0] / REQ[0]	J1 REQ/GNT
GPP[18] / GPP[19]	GNT[1] / REQ[1]	J2 REQ1/GNT1
GPP[20] / GPP[21]	GNT[2] / REQ[2]	J2 REQ2/GNT2
GPP[22] / GPP[23]	GNT[3] / REQ[3]	J2 REQ3/GNT3
GPP[24] / GPP[25]	GNT[4] / REQ[4]	J2 REQ4/GNT4
GPP[26] / GPP[27]	GNT[5] / REQ[5]	J2 REQ5/GNT5

8. Local Services

This chapter describes details of XCalibur1002 local services. This include the Altera FPGA which performs the following functions:

- Discovery III Device Bus Interface
- Interrupt Controller
- CompactFlash / IDE Interface
- Local control and status registers
- Socketed / Expansion flash Interface

8.1 FPGA Register Interface

The following tables describe the details of each register's individual bits.

Table 8.1.1: Configuration Registers

Name	Description	Offset
MFR	Module Family ID	0000H
MID	Module ID	0010H
MRV	Module Revision	0020H
MGA	Module Geographical Address	0030H
CPCFG	CompactPCI Configuration	0040H
LPCFG	Local PCI Configuration	0050H
MCFG0	Module Configuration 0	0060H
MCFG1	Module Configuration 1	0070H
MCFG2	Module Configuration 2	0080H
MCFG3	Module Configuration 3	0090H
MBM	Module Boot Mode	00A0H
MBME	Module Boot Mode Enable	00B0H

Table 8.1.2: Control Registers

Name	Description	Offset
MRST	Module Reset	0100H
MLED	Module LED Control	0110H

Table 8.1.3: Interrupt Registers

Name	Description	Offset
MIS	Master Interrupt Status	0200H
LIS0	Local Interrupt Status 0	0210H
LIS1	Local Interrupt Status 1	0220H
UIS	User Interrupt Status	0230H
PIS	PCI Interrupt Status	0240H
LIC0	Local Interrupt Control 0	0300H
LIC1	Local Interrupt Control 1	0310H
LIC2	Local Interrupt Control 2	0320H
LIC3	Local Interrupt Control 3	0330H
LIC4	Local Interrupt Control 4	0340H
LIC5	Local Interrupt Control 5	0350H
LIC6	Local Interrupt Control 6	0360H
LIC7	Local Interrupt Control 7	0370H
UIC0	User Interrupt Control 0	0380H
UIC1	User Interrupt Control 1	0390H
UIC2	User Interrupt Control 2	03A0H
UIC3	User Interrupt Control 3	03B0H
PIC0	PCI Interrupt Control 0	03C0H
PIC1	PCI Interrupt Control 1	03D0H
PIC2	PCI Interrupt Control 2	03E0H
PIC3	PCI Interrupt Control 3	03F0H

Table 8.1.4: IPMI Block Transfer Registers

Name	Description	Offset
BTC	BT Interface Control Register	0400H
BTWS	BT Write Size Register	0410H
BTRS	BT Read Size Register	0420H
ICTRL	IPMI Control Register (Rev. D and above)	0430H
BTWBn	BT Write Buffer Registers (255). The write buffer registers bye wide and are offset 0x10 from one another.	1000H-1FE0H
BTRBn	BT Read Buffer Registers (255). The read buffer registers bye wide and are offset 0x10 from one another.	2000H-2FE0H

Table 8.1.5: Software Watchdog Registers

Name	Description	Offset
WDSER	Software Watchdog Control	0x0440

Name	Description	Offset
WDCTL	Software Watchdog Service	0x0450

8.2 Configuration Register Descriptions

Table 8.2.1: MFM (Module Family Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
MFR	R	03H	D7-D0	Module Family Number.

Table 8.2.2: MID (Module Identification Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
MID	R	12H	D7-D0	Module Identification.

Table 8.2.3: MRV (Module Revision Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
MRV	R	13H	D7-D0	Module Revision. Indicates revision of XCalibur Board's FPGA.

Table 8.2.4: MGA (Module Geographical Address Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
SYSEN	R	-	D7	System Controller Indicator. Set to 1 if module is installed in CompactPCI system controller slot.
RSVD	R	0	D6-D5	Reserved
GA	R	-	D4-D0	CompactPCI Geographical Address as presented on J2.

Table 8.2.5: CPCFG (CompactPCI Configuration Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
SYS	R	-	D7	Detected System Enable
DPCI	R	-	D6-4	Detected CompactPCI Bus Configuration 0 - 33 MHz PCI 1 - 66 MHz PCI 2 - 66 MHz PCI-X 3 - 83 MHz PCI-X 4 - 100 MHz PCI-X 5 - 133 MHz PCI-X 6 - Reserved 7 - Reserved
LARB	RW	-	D3	Current Arbitration Enable
CPCI	RW	-	D2-0	Current CompactPCI Bus Configuration 0 - 33 MHz PCI 1 - 66 MHz PCI 2 - 66 MHz PCI-X 3 - 83 MHz PCI-X 4 - 100 MHz PCI-X 5 - 133 MHz PCI-X 6 - Reserved 7 - Reserved

Table 8.2.6: LPCFG (Local PCI Configuration Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7	Reserved
DPCI	R	-	D6-4	Detected Local PCI Bus Configuration 0 - 33 MHz PCI 1 - 66 MHz PCI 2 - 66 MHz PCI-X 3 - 83 MHz PCI-X 4 - 100 MHz PCI-X 5 - 133 MHz PCI-X 6 - Reserved 7 - Reserved
RSVD	R	0	3	Reserved
LPCI	RW	-	D2-0	Current Local PCI Bus Configuration 0 - 33 MHz PCI 1 - 66 MHz PCI 2 - 66 MHz PCI-X 3 - 83 MHz PCI-X 4 - 100 MHz PCI-X 5 - 133 MHz PCI-X 6 - Reserved 7 - Reserved

Table 8.2.7: MCFG0 (Module Configuration Register 0)

Field Name	Access Type	Reset Value	Data Bits	Field Description
CBS	R	-	D7-D6	CPU Bus Speed. Specified by build option. 0 - 166MHz 1 - 200MHz 2 - 100MHz 3 - 133MHz
RSVD	R	00	D5-4	Reserved.
MBS	R	-	D3-2	Expansion Flash Size. Specified by build option. 0 - 8 MB 1 - 16 MB 2 - 32 MB 3 - 64 MB
RSVD	R	0	D1	Reserved.
BFD	R	-	D0	Boot Device Detect 0 - Socketed Flash 1 - Expansion Flash

Table 8.2.8: MCFG1 (Module Configuration Register 1)

Field Name	Access Type	Reset Value	Data Bits	Field Description
P2MON	R	-	D7	PMC 2 MONARCH
P2D	R	-	D6	PMC 2 Card Detect 0 - PMC 2 Card Not Detect 1 - PMC 2 Card Detected
P2ER	R	-	D5	PMC 2 EREADY
P1MON	R	-	D4	PMC 1 MONARCH
P1D	R	-	D3	PMC1 Card Detect 0 - PMC1 Card Not Detect 1 - PMC1 Card Detected
P1ER	R	-	D2	PMC 1 EREADY
IDECD	R	-	D1	IDE Card Detect 0 - P14 IDE Card Not Detect 1 - P14 IDE Card Detected
CFCD	R	-	D0	CompactFlash Card Detect 0 - CompactFlash Card Not Detect 1 - CompactFlash Card Detected

Table 8.2.9: MCFG2 (Module Configuration Register 2)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	00H	D7-0	Reserved.

Table 8.2.10: MCFG3 (Module Configuration Register 3)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	00H	D7-3	Reserved.
RB2	R		D2	AMD Mirrorbit 1 Ready/Busy Status 1 = Flash is Busy; 0 = Flash is Ready
RB1	R		D1	AMD Mirrorbit 0 Ready/Busy Status 1 = Flash is Busy; 0 = Flash is Ready
RB0	R		D0	Intel StrataFlash Ready/Busy Status 1 = Flash is Busy; 0 = Flash is Ready

Table 8.2.11: MBM (Module Boot Mode Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
BMC	RW	0	D7	Boot Mode Cancel 0 - Boot mode functions as normal 1 - Disables boot mode
RSVD	R	0	D6-1	Reserved.
BM	R	1	D0	Indicates that the boot flash has been remapped up to the upper address.

Table 8.2.12: MBME (Module Boot Mode Enable Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
BME	W	00H	D7-0	Boot mode enable. Write 5AH to enable boot mode.

8.3 Configuration Register Descriptions

Table 8.3.1: MRST (Module Reset Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
CINH	R	000	D7	CompactPCI reset inhibit bit. Writing a 1 to this bit location disables CompactPCI resets from reseting the CPU and local devices.
RSVD	R	000	D7-D5	Reserved
SRST	RW	0	D4	Device reset control bit. Writing a 1 to this bit location will cause all devices on the card except the CPU to be reset. Writing a 0 will clear the reset condition.

Field Name	Access Type	Reset Value	Data Bits	Field Description
C1RST	RW	0	D3	CPU reset control bit. Writing a 1 to this bit location will cause CPU 1 to be reset. Writing a 0 will clear the reset condition.
C0RST	RW	0	D2	CPU reset control bit. Writing a 1 to this bit location will cause CPU 0 to be reset. Writing a 0 will clear the reset condition.
IRST	RW	0	D1	IPMI reset control bit. Writing a 1 to this bit location will reset the IPMI controller. Writing a 0 will clear the reset condition.
BRST	RW	0	D0	Board reset control bit. Writing a 1 to this bit location will cause a board level reset. This will also reset the CompactPCI bus in system controller mode. It is self clearing.

Table 8.3.2: MLED (Module LED Control Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-D5	Reserved
CA2	RW	0	D4	Activity LED Enable. Writing a 1 to this bit location will light the user defined LED on the front panel.
CA1	RW	0	D3	Status LED Enable. Writing a 1 to this bit location will light the user defined LED on the front panel.
ALM	RW	1	D2	Red Alarm LED Enable. Writing a 1 to this bit location will light the LED.
ACT	RW	0	D1	Yellow Activity LED Enable. Writing a 1 to this bit location will light the LED.
STS	RW	0	D0	Green Status LED Enable. Writing a 1 to this bit location will light the LED.

8.4 Interrupt Register Descriptions

The following interrupt status registers indicate the state of the pending interrupt from the specified device. A ‘1’ indicates that the interrupt is being driven by the associated device. A ‘0’ indicates that the interrupt is not being driven. Note: The state of the interrupts are always displayed in these registers, even if the interrupt has not been enabled through the interrupt enable registers.

Table 8.4.1: MIS (Master Interrupt Status Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
MI	R	-	D7	Master Interrupt Status.

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	000	D6-4	Reserved.
PIS	R	-	D3	PCI Interrupt Status.
UIS	R	-	D2	User Interrupt Status.
LIS1	R	-	D1	Local Interrupt 1 Status.
LIS0	R	-	D0	Local Interrupt 0 Status.

Table 8.4.2: LIS0 (Local Interrupt Status Register 0)

Field Name	Access Type	Reset Value	Data Bits	Field Description
ENUM	R	-	D7	CompactPCI ENUM# Status.
RSVD	R	-	D6	Reserved.
IDE	R	-	D5	IDE Interrupt Status.
CF	R	-	D4	CompactFlash Interrupt Status.
ETH1	R	-	D3	2.16 Ethernet 0 PHY Interrupt Status.
ETH0	R	-	D2	Front Panel Ethernet PHY Interrupt Status.
RSVD	R	-	D1	Reserved.
ETH2	R	-	D0	2.16 Ethernet 1 PHY Interrupt Status.

Table 8.4.3: LIS1 (Local Interrupt Status Register 1)

Field Name	Access Type	Reset Value	Data Bits	Field Description
IPMI	R	-	D7	IPMI Interrupt Status.
RSVD	R	-	D6	Reserved.
RSVD	R	-	D5	Reserved.
DISCC0	R	-	D4	Discovery CPU Interrupt Status.
DISCP	R	-	D3	Discovery Primary PCI Interrupt Status.
DISCS	R	-	D2	Discovery Secondary PCI Interrupt Status.
RSVD	R	-	D1	Reserved.
CPU	R	-	D0	CPU 0 Checkstop Interrupt Status.

Table 8.4.4: UIS (User Interrupt Status Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7	Reserved.
UINT3	R	-	D6	User Interrupt 3 Status.
RSVD	R	0	D5	Reserved.
UINT2	R	-	D4	User Interrupt 2 Status
RSVD	R	0	D3	CompactPCI FAL# Interrupt Status
UINT1	R	-	D2	User Interrupt 1 Status.
RSVD	R	0	D1	CompactPCI DEG# Interrupt Status
UINT0	R	-	D0	User Interrupt 0 Status.

Table 8.4.5: PIS (PCI Interrupt Status Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
CINTD	R	-	D7	CompactPCI Interrupt D Status.
CINTC	R	-	D6	CompactPCI Interrupt C Status.
CINTB	R	-	D5	CompactPCI Interrupt B Status.
CINTA	R	-	D4	CompactPCI Interrupt A Status.
LINTD	R	-	D3	Local PCI Interrupt D Status.
LINTC	R	-	D2	Local PCI Interrupt C Status.
LINTB	R	-	D1	Local PCI Interrupt B Status.
LINTA	R	-	D0	Local PCI Interrupt A Status.

The following register format applies to the interrupt control registers. Each interrupt control register nibble implements a single interrupt source.

Table 8.4.6: Interrupt Control Register Format

Field Name	Access Type	Reset Value	Data Bits	Field Description
DST	RW	0	D3-0	Interrupt Destination 0x0 - Interrupt Disabled 0x1 - Reserved 0x2 - CPU 0 0x3 - CPU 1 0x4 - Local PCI Interrupt A 0x5 - Local PCI Interrupt B 0x6 - Local PCI Interrupt C 0x7 - Local PCI Interrupt D 0x8 - CompactPCI Interrupt A 0x9 - CompactPCI Interrupt B 0xA - CompactPCI Interrupt C 0xB - CompactPCI Interrupt D 0xC - Aux. Interrupt (to MV64460 MPP13) 0xE - Reserved 0xF - Reserved

Table 8.4.7: LIC0 (Local Interrupt Control Register 0)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	RW	0	D7-4	Reserved.
ETH2	RW	0	D3-0	2.16 Ethernet 1 PHY Interrupt Control.

Table 8.4.8: LIC1 (Local Interrupt Control Register 1)

Field Name	Access Type	Reset Value	Data Bits	Field Description
ETH1	RW	0	D7-4	2.16 Ethernet 0 PHY Interrupt Control.
ETH0	RW	0	D3-0	Front Panel Ethernet 0 PHY Interrupt Control.

Table 8.4.9: LIC2 (Local Interrupt Control Register 2)

Field Name	Access Type	Reset Value	Data Bits	Field Description
IDE	RW	0	D7-4	IDE Interrupt Control.
CF	RW	0	D3-0	CompactFlash Interrupt Control.

Table 8.4.10: LIC3 (Local Interrupt Control Register 3)

Field Name	Access Type	Reset Value	Data Bits	Field Description
ENUM	RW	0	D7-4	CompactPCI ENUM# Interrupt Control.
RSVD	RW	0	D3-0	Reserved.

Table 8.4.11: LIC4 (Local Interrupt Control Register 4)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	RW	0	D7-4	Reserved.
CPU0	RW	0	D3-0	CPU 0 Checkstop Interrupt Control.

Table 8.4.12: LIC5 (Local Interrupt Control Register 5)

Field Name	Access Type	Reset Value	Data Bits	Field Description
DISCP	RW	0	D7-4	Discovery II Primary PCI Interrupt Control.
DISCS	RW	0	D3-0	Discovery II Secondary PCI Interrupt Control.

Table 8.4.13: LIC6 (Local Interrupt Control Register 6)

Field Name	Access Type	Reset Value	Data Bits	Field Description
DISCC1	RW	0	D7-4	Discovery II CPU 1 Interrupt Control.
DISCC0	RW	0	D3-0	Discovery II CPU 0 Interrupt Control.

Table 8.4.14: LIC7 (Local Interrupt Control Register 7)

Field Name	Access Type	Reset Value	Data Bits	Field Description
IPMI	RW	0	D7-4	IPMI Interrupt Control.
RSVD	RW	0	D3-0	Reserved.

Table 8.4.15: UIC0 (User Interrupt Control Register 0)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-4	CompactPCI DEG# Interrupt Control.
UIC0	RW	0	D3-0	User Interrupt 0 Control.

Table 8.4.16: UIC1 (User Interrupt Control Register 1)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-4	CompactPCI FAL# Interrupt Control.
UIC1	RW	0	D3-0	User Interrupt 1 Control.

Table 8.4.17: UIC2 (User Interrupt Control Register 2)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-4	Reserved.
UIC2	RW	0	D3-0	User Interrupt 2 Control.

Table 8.4.18: UIC2 (User Interrupt Control Register 3)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-4	Reserved.
UIC3	RW	0	D3-0	User Interrupt 3 Control.

Table 8.4.19: PIC0 (PCI Interrupt Control Register 0)

Field Name	Access Type	Reset Value	Data Bits	Field Description
LINTB	RW	0	D7-4	Local PCI INTB Interrupt Control.
LINTA	RW	0	D3-0	Local PCI INTA Interrupt Control.

Table 8.4.20: PIC1 (PCI Interrupt Control Register 1)

Field Name	Access Type	Reset Value	Data Bits	Field Description
LINTD	RW	0	D7-4	Local PCI INTD Interrupt Control.
LINTC	RW	0	D3-0	Local PCI INTC Interrupt Control.

Table 8.4.21: PIC2 (PCI Interrupt Control Register 2)

Field Name	Access Type	Reset Value	Data Bits	Field Description
CINTB	RW	0	D7-4	CompactPCI INTB Interrupt Control
CINTA	RW	0	D3-0	CompactPCI INTA Interrupt Control.

Table 8.4.22: PIC3 (PCI Interrupt Control Register 3)

Field Name	Access Type	Reset Value	Data Bits	Field Description
CINTD	RW	0	D7-4	CompactPCI INTD Interrupt Control
CINTC	RW	0	D3-0	CompactPCI INTC Interrupt Control.

8.5 IPMI Block Transfer Registers Description

The IPMI block transfer size registers and the appropriate write buffer registers must be set up prior to starting a transfer. With the Serial Programing Interface (SPI), reads and writes are done simultaneously. A BTWS value of zero means that zero bytes will be written before starting to read bytes.

Table 8.5.1: BTC (Block Transfer Control Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-1	Reserved
SB	RW	0	D0	Start/Busy bit. Written with a 1 to start a transfer, stays one until the transfer is finished.

Table 8.5.2: BTWS (Block Transfer Write Size Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
BTWS	RW	0	D7-0	Number of bytes to be written.

Table 8.5.3: BTRS (Block Transfer Read Size Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
BTRS	RW	0	D7-0	Number of bytes to be read.

Table 8.5.4: ICTRL (IPMI Console Control Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-1	Reserved
SCTL	RW	0	D0	Determines COM2 functionality 0 = COM2 functions as MV64460 MPSC1 1 = COM2 functions as IPMI serial console

Table 8.5.5: BTWBn (Block Transfer Write Buffer Registers)

Field Name	Access Type	Reset Value	Data Bits	Field Description
DATA	RW	-	D7-0	Data Byte to be Written.

Table 8.5.6: BTRBn (Block Transfer Read Buffer Registers)

Field Name	Access Type	Reset Value	Data Bits	Field Description
DATA	R	-	D7-0	Data Byte Read.

8.6 Software Watchdog Register Descriptions

See Section 8.7 “Software Watchdog Reset Timer“ for more information.

Table 8.6.1: WDSER (Software Watchdog Service Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
DATA	W	0	D7-D0	Write 0xCC followed by 0x33 to reset the watchdog timer.

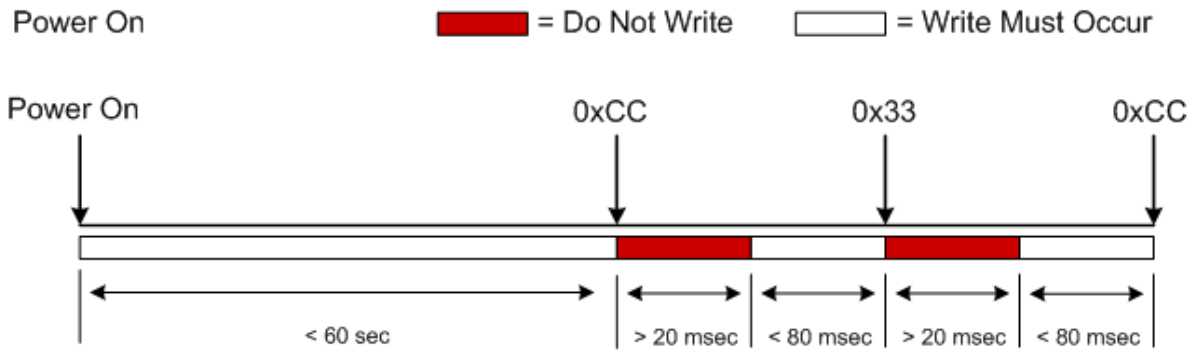
Table 8.6.2: WDCTL (Software Watchdog Control Register)

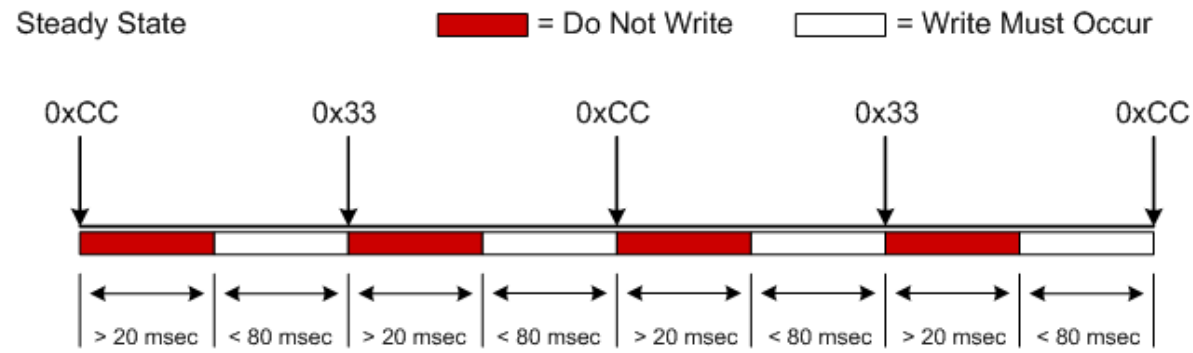
Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-D1	Reserved
EN	RW	1	D0	Enables/Disables the watchdog timer. By default it is enabled, write 0 to disable write 1 to enable.

8.7 Software Watchdog Reset Timer

The FPGA provides a software watchdog reset timer to prevent system lockup in case software becomes trapped in a loop or is stuck in an interrupt handler. The watchdog timer is enabled by default, but xMon disables the watchdog timer in its POST. The software watchdog timer can be enabled by setting the EN bit in the WDSER (Software Watchdog Service Register), but after enabled, the watchdog timer will not trigger a reset for 60 seconds. If the watchdog timer's service routine does not begin within 60 seconds, a board level reset will be issued. After the watchdog service routine starts, the software watchdog timer service sequence must be executed periodically. Without this periodic servicing, the software watchdog timer will timeout and issue a board level reset. The software watchdog timer can be disabled by clearing the EN bit in the WDSER (Software Watchdog Service Register).

During the initial 60 second period after enabled, software must write 0xCC to the WDSER (Software Watchdog Service Register) and wait 50ms +/- 30ms to write the next data in the sequence, 0x33. Before starting the 0xCC/0x33 sequence again, software must again wait for the next time period of 50ms +/- 30ms.





9. Switched Ethernet Backplane

XCalibur1002 supports the PICMG 2.16 switched ethernet backplane via Discovery III bridge ethernet controller.

9.1 Port Assignments

The following table gives the PICMG 2.16 ethernet port pin assignments for each Discovery III port.

Table 9.1.1: Port Assignments

64460 Port	PICMG 2.16	J3
Port 1 MX0+	LPa_DA+	A18
Port 1 MX0-	LPa_DA-	B18
Port 1 MX1+	LPa_DB+	A17
Port 1 MX1-	LPa_DB-	B17
Port 1 MX2+	LPa_DC+	D18
Port 1 MX2-	LPa_DC-	E18
Port 1 MX3+	LPa_DD+	D17
Port 1 MX3-	LPa_DD-	E17

64460 Port	PICMG 2.16	J3
Port 2 MX0+	LPb_DA+	A16
Port 2 MX0-	LPb_DA-	B16
Port 2 MX1+	LPb_DB+	A15
Port 2 MX1-	LPb_DB-	B15
Port 2 MX2+	LPb_DC+	D16
Port 2 MX2-	LPb_DC-	E16
Port 2 MX3+	LPb_DD+	D15
Port 2 MX3-	LPb_DD-	E15

10. IDE / CompactFlash

XCalibur1002 supports an IDE interface through the CompactPCI P5 connector. This allows use of hard drive / CompactFlash transition modules.

In addition, XCalibur1002 supports a single on-card CompactFlash device. Up to 1GB of removable non-volatile storage can be installed.

10.1 IDE Interface Signals

The following table gives a description of the true IDE mode signals supported by the XCalibur1002 IDE interface.

Table 10.1.1: IDE Signals

Signal	Description
A2-A0	Address lines used to select one of eight registers in the Task File.
CS0#	Chip select for the Task File.
CS1#	Chip select for the alternate status register and the device control register.
CSEL#	Used to configure a device as master or slave.
D15-D0	Data lines. All Task File operations occur in byte mode on the low order bus D7-D0 while data transfers are 16 bit using D15-D0.
IORD#	Read strobe.
IOWR#	Write strobe.
IOIS16#	Indicates a 16 bit cycle.
INTRQ	Active high interrupt request.
RESET#	IDE device reset signal.

10.2 IDE Register Map

XCalibur1002 supports an IDE interface for interfacing with the CompactFlash as well as transition module IDE devices. The following tables give the IDE registers and their offsets on the Discovery II device bus.

Table 10.2.1: CompactFlash IDE Registers

Name	Description	Offset
DATA	Data Register	0000H
ERFT	Error / Feature Register	0010H
SECC	Sector Count Register	0020H
SECN	Sector Number Register	0030H
CYL	Cylinder Low Register	0040H
CYH	Cylinder High Register	0050H
DRHD	Drive / Head Register	0060H
STCD	Status / Command Register	0070H
ALTS	Alternate Status Register	0160H
DADR	Drive Address Register	0170H

Table 10.2.2: Transition Module IDE Registers

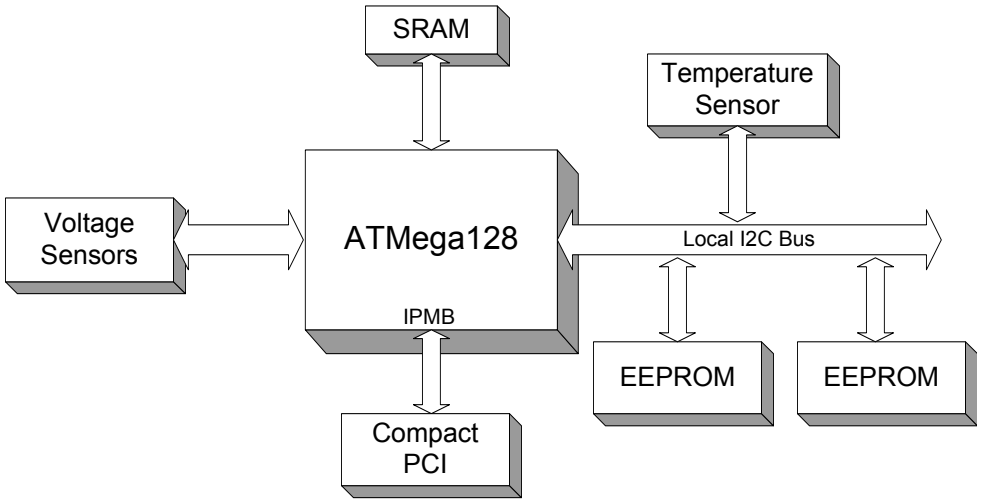
Name	Description	Offset
DATA	Data Register	0200H
ERFT	Error / Feature Register	0210H
SECC	Sector Count Register	0220H
SECN	Sector Number Register	0230H
CYL	Cylinder Low Register	0240H
CYH	Cylinder High Register	0250H
DRHD	Drive / Head Register	0260H
STCD	Status / Command Register	0270H
ALTS	Alternate Status Register	0360H
DADR	Drive Address Register	0370H

11. IPMB

XCalibur1002 supports the IPMB protocol per the PICMG 2.9 CompactPCI System Management Specification. This chapter covers the implementation of IPMB on XCalibur1002.

The IPMI interface is implemented with the Atmel ATMega128 microcontroller. This high-performance, low-power 8-bit AVR microcontroller is capable of up to 8 MIPS at 8MHz. It provides 128K bytes of internal Flash, 4K bytes of internal EEPROM, and 4K bytes of internal SRAM. An additional 64K of external SRAM is provided. A built in I2C controller provides the IPMB interface.

11.1 Block Diagram



11.2 ATMega128 Pin Usage

The ATMega128 microcontroller provides general purpose input and output pins. This following table documents the usage of these pins.

Table 11.2.1: ATMega128 Pin Assignments

Atmel A/D Port	Assignment
PD4	CompactPCI Geographical Address 0
PB7	CompactPCI Geographical Address 1
PB6	CompactPCI Geographical Address 2
PE7	CompactPCI Geographical Address 3
PE6	CompactPCI Geographical Address 4
PD5	Powerdown control line. Driving a logic zero will power down the XCalibur1002.
PD6	Reset control line. Driving a logic zero will reset the XCalibur1002.

11.3 I^2C Interfaces

Two I2C buses are implemented using the Atmel ATMega128. The following table documents the pin usage for this function.

Table 11.3.1: I^2C Pin Assignments

Atmel A/D Port	Assignment
PD0	IPMB SCL
PD1	IPMB SDA
PD2	LOCAL SCL
PD3	LOCAL SDA

11.4 Non-Volatile Storage

The Fairchild FM24C16 EEPROM is used to store IPMB related configuration and log information. This device features 4K bits of electrically erasable nonvolatile memory organized as 2,048 x 8 bits. The I^2C address of this device is 1010000B to 1010111B. The lower three address bits provide page selection.

11.5 Temperature Sensor

The Dallas DS1631 Digital Thermometer is used to monitor ambient temperature on XCalibur1002. This sensor is accurate to 0.5C and has a range from 0C to 70C. The I^2C address of this device is 1001000B.

11.6 Voltage Sensors

The Atmel ATMega128 provides 8 A/D converters. The following have been assigned to voltage level monitoring.

Table 11.6.1: Voltage Sensor Pin Assignments

Atmel A/D Port	Voltage
ADC0	5.0V
ADC1	3.3V
ADC2	2.5V
ADC3	1.8V
ADC4	1.5V
ADC5	1.25V
ADC6	Processor Core
ADC7	Reserved

11.7 Block Transfer Interface

The Block Transfer interface is implemented in FPGA and allows message passing between the microcontroller and the CPUs. See the IPMI Block Transfer Registers Description Section for details.

12. Device Configuration

This chapter gives the recommended register settings for XCalibur1002 devices. These settings are depended on aspects of the hardware design and should not be modified without intimate knowledge of the devices involved.

12.1 Discovery III Configuration

The following table gives the recommended register settings for the Discovery II system controller. Please refer to the Discovery III user's manual for more information regarding the device.

Table 12.1.1: MV64460 Register Settings

Register	Offset	Value
Device Bank 0 Parameters	0x045C	0x0422DE57
Device Bank 1 Parameters	0x0460	0x0422DE57
Device Bank 2 Parameters	0x0464	0x0422DE57
Device Bank 3 Parameters	0x0468	0x0422DE57
Boot Device Bank Parameters	0x046C	0x0422DE57
MPP Control 0	0xF000	0x11111111
MPP Control 1	0xF004	0x00001122
MPP Control 2	0xF008	0x00000000
MPP Control 3	0xF00C	0x00400000