MR4A16B

1M x 16 MRAM

FEATURES

- +3.3 Volt power supply
- Fast 35 ns read/write cycle
- SRAM compatible timing
- Unlimited read & write endurance
- Data always non-volatile for >20-years at temperature
- RoHS-compliant small footprint BGA and TSOP package

BENEFITS

- One memory replaces FLASH, SRAM, EEPROM and BBSRAM in systems for simpler, more efficient designs
- Improves reliability by replacing battery-backed SRAM

INTRODUCTION

The **MR4A16B** is a 16,777,216-bit magnetoresistive random access memory (MRAM) device organized as 1,048,576 words of 16 bits. The **MR4A16B** offers SRAM compatible 35 ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The **MR4A16B** is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

The **MR4A16B** is available in small footprint 48-pin ball grid array (BGA) package and a 54-pin thin small outline package (TSOPII). These packages are compatible with similar low-power SRAM products and other nonvolatile RAM products.

The **MR4A16B** provides highly reliable data storage over a wide range of temperatures. The product is offered with commercial temperature (0 to +70 °C), industrial temperature (-40 to +85 °C), and automotive temperature (-40 to +125 °C) range options.

CONTENTS

1. DEVICE PIN ASSIGNMENT

Figure 1.1 Block Diagram

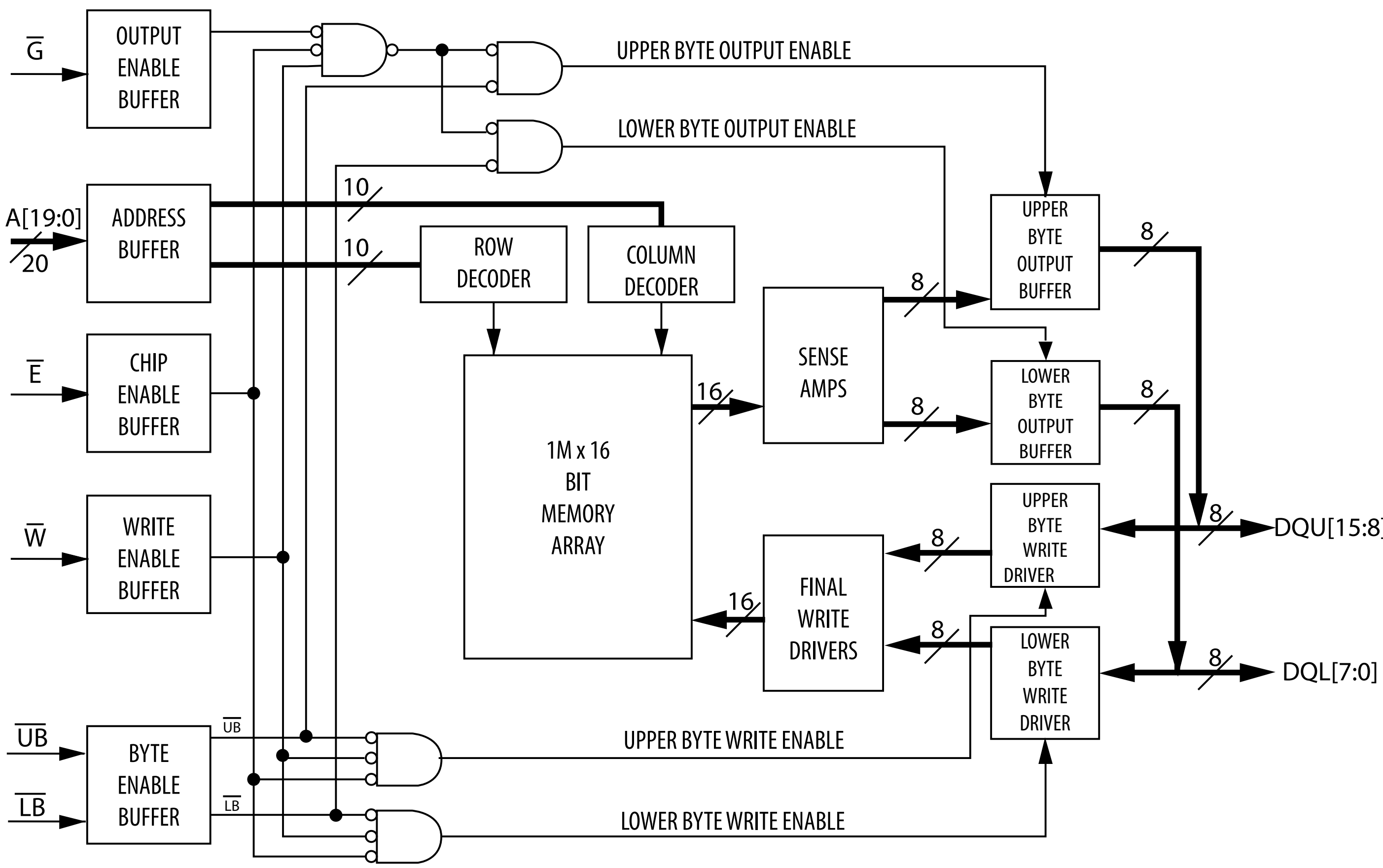
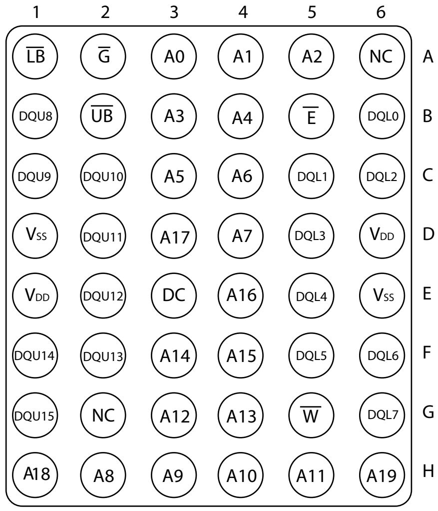


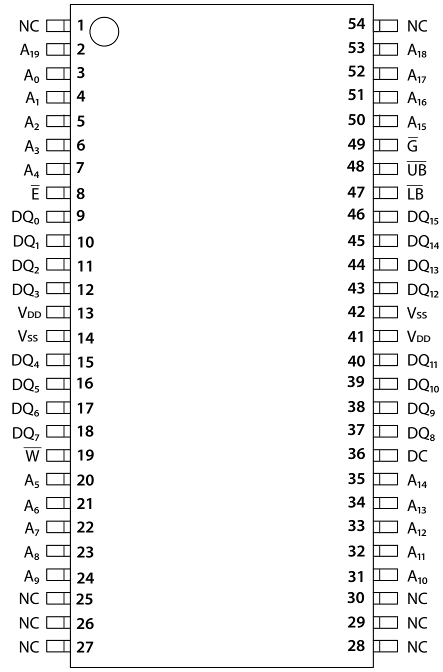
Table 1.1 Pin Functions

Signal Name	Function
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{UB}$	Upper Byte Enable
$\overline{LB}$	Lower Byte Enable
DQ	Data I/O
V_{DD}	Power Supply
V_{SS}	Ground
DC	Do Not Connect
NC	No Connection

Figure 1.2 Pin Diagrams for Available Packages (Top View)



48-Pin BGA



54-Pin TSOP

Table 1.2 Operating Modes

$\overline{E}$[1]	$\overline{G}$[1]	$\overline{W}$[1]	$\overline{LB}$[1]	$\overline{UB}$[1]	Mode	V_{DD} Current	DQL[7:0][2]	DQU[15:8][2]
H	X	X	X	X	Not selected	I_{SB1}, I_{SB2}	Hi-Z	Hi-Z
L	H	H	X	X	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	X	X	H	H	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	L	H	L	H	Lower Byte Read	I_{DDR}	D_{Out}	Hi-Z
L	L	H	H	L	Upper Byte Read	I_{DDR}	Hi-Z	D_{Out}
L	L	H	L	L	Word Read	I_{DDR}	D_{Out}	D_{Out}
L	X	L	L	H	Lower Byte Write	I_{DDW}	D_{in}	Hi-Z
L	X	L	H	L	Upper Byte Write	I_{DDW}	Hi-Z	D_{in}
L	X	L	L	L	Word Write	I_{DDW}	D_{in}	D_{in}

[1] H = high, L = low, X = don't care

[2] Hi-Z = high impedance

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field greater than the maximum field intensity specified in the maximum ratings.

Table 2.1 Absolute Maximum Ratings[1]

Parameter	Symbol	Value	Unit
Supply voltage[2]	V_{DD}	-0.5 to 4.0	V
Voltage on an pin[2]	V_{IN}	-0.5 to V_{DD} + 0.5	V
Output current per pin	I_{OUT}	±20	mA
Package power dissipation	P_D	0.600	W
Temperature under bias MR4A16B (Commercial) MR4A16BC (Industrial) MR4A16BM (Automotive)	T_{BIAS}	 -10 to 85 -45 to 95 -45 to 130	°C
Storage Temperature	T_{stg}	-55 to 150	°C
Lead temperature during solder (3 minute max)	T_{Lead}	260	°C
Maximum magnetic field during write MR4A16B (All Temperatures)	H_{max_write}	2000	A/m
Maximum magnetic field during read or standby	H_{max_read}	8000	A/m

[1] Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.

[2] All voltages are referenced to V_{SS}. The DC value of V_{IN} must not exceed actual applied V_{DD} by more than 0.5V. The AC value of V_{IN} must not exceed applied V_{DD} by more than 2V for 10ns with I_{IN} limited to less than 20mA.

[3] Power dissipation capability depends on package characteristics and use environment.

Table 2.2 Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Power supply voltage	V_{DD}	3.0 [i]	3.3	3.6	V
Write inhibit voltage	V_{WI}	2.5	2.7	3.0 [i]	V
Input high voltage	V_{IH}	2.2	-	V_{DD} + 0.3 [ii]	V
Input low voltage	V_{IL}	-0.5 [iii]	-	0.8	V
Temperature under bias MR4A16B (Commercial) MR4A16BC (Industrial) MR4A16BM (Automotive)	T_A	 0 -40 -40		 70 85 125	°C

[i] There is a 2 ms startup time once V_{DD} exceeds $V_{DD,}$(max). See **Power Up and Power Down Sequencing** below.
[ii] V_{IH}(max) = V_{DD} + 0.3 V_{DC}; V_{IH}(max) = V_{DD} + 2.0 V_{AC} (pulse width ≤ 10 ns) for I ≤ 20.0 mA.
[iii] V_{IL}(min) = -0.5 V_{DC} ; V_{IL}(min) = -2.0 V_{AC} (pulse width ≤ 10 ns) for I ≤ 20.0 mA.

Power Up and Power Down Sequencing

MRAM is protected from write operations whenever V_{DD} is less than V_{WI}. As soon as V_{DD} exceeds V_{DD}(min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The $\overline{E}$ and $\overline{W}$ control signals should track V_{DD} on power up to V_{DD}- 0.2 V or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives $\overline{E}$ and $\overline{W}$ should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where V_{DD} goes below V_{WI}, writes are protected and a startup time must be observed when power returns above V_{DD}(min).

Figure 2.1 Power Up and Power Down Diagram

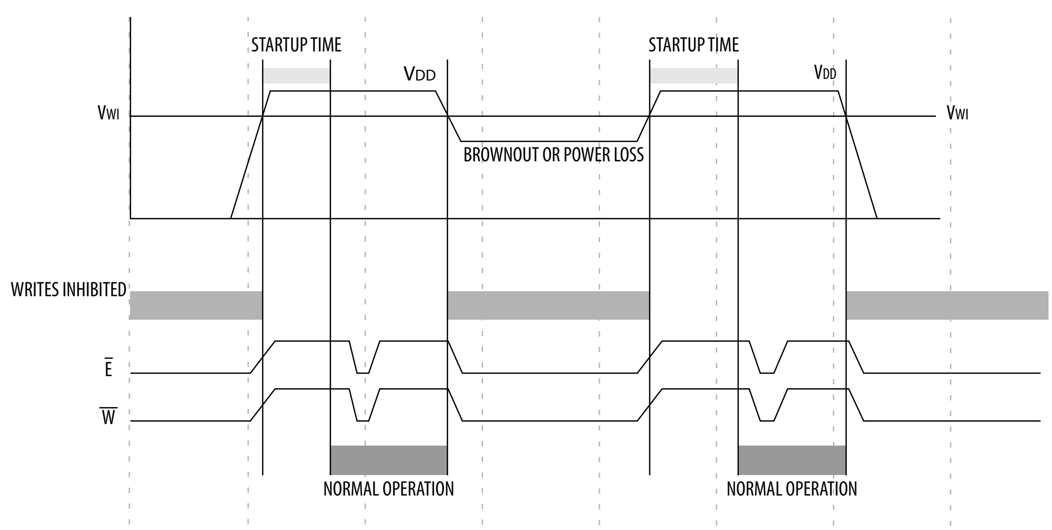


Table 2.3 DC Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Input leakage current	$I_{lkg(I)}$	-	-	±1	µA
Output leakage current	$I_{lkg(O)}$	-	-	±1	µA
Output low voltage (I_{OL} = +4 mA) (I_{OL} = +100 µA)	V_{OL}	-	-	0.4 V_{SS} + 0.2	V
Output high voltage (I_{OH} = -4 mA) (I_{OH} = -100 µA)	V_{OH}	2.4 V_{DD} - 0.2	-	-	V

Table 2.4 Power Supply Characteristics

Parameter	Symbol	Typical	Max	Unit
AC active supply current - read modes[1] (I_{OUT}= 0 mA, V_{DD}= max)	I_{DDR}	60	TBD	mA
AC active supply current - write modes[1] (V_{DD}= max) MR4A16B (Commercial) MR4A16BC (Industrial) MR4A16BV (Extended)	I_{DDW}	110 110 110	TBD TBD TBD	mA
AC standby current (V_{DD}= max, $\overline{E} = V_{IH}$) *no other restrictions on other inputs*	I_{SB1}	11	14	mA
CMOS standby current ($\overline{E} \geq V_{DD}$ - 0.2 V and $V_{In} \leq V_{SS}$ + 0.2 V or $\geq V_{DD}$ - 0.2 V) (V_{DD} = max, f = 0 MHz)	I_{SB2}	7	9	mA

[1] All active current measurements are measured with one address transition per cycle and at minimum cycle time.

3. TIMING SPECIFICATIONS

Table 3.1 Capacitance[1]

Parameter	Symbol	Typical	Max	Unit
Address input capacitance	C_{In}	-	6	pF
Control input capacitance	C_{In}	-	6	pF
Input/Output capacitance	$C_{I/O}$	-	8	pF

[1] f = 1.0 MHz, dV = 3.0 V, T_A = 25 °C, periodically sampled rather than 100% tested.

Table 3.2 AC Measurement Conditions

Parameter	Value	Unit
Logic input timing measurement reference level	1.5	V
Logic output timing measurement reference level	1.5	V
Logic input pulse levels	0 or 3.0	V
Input rise/fall time	2	ns
Output load for low and high impedance parameters	See Figure 3.1	
Output load for all other timing parameters	See Figure 3.2	

Figure 3.1 Output Load Test Low and High

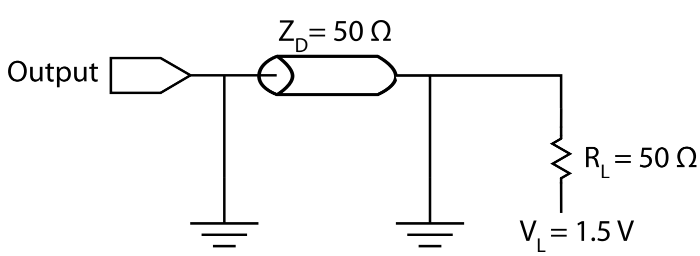
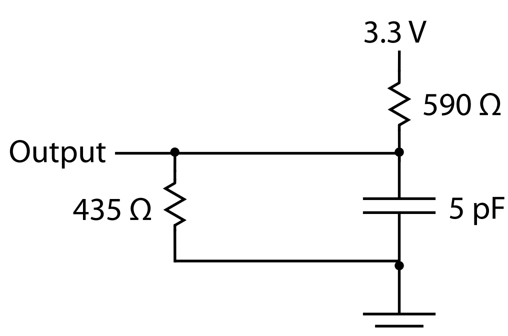


Figure 3.2 Output Load Test All Others



Read Mode

Table 3.3 Read Cycle Timing[1]

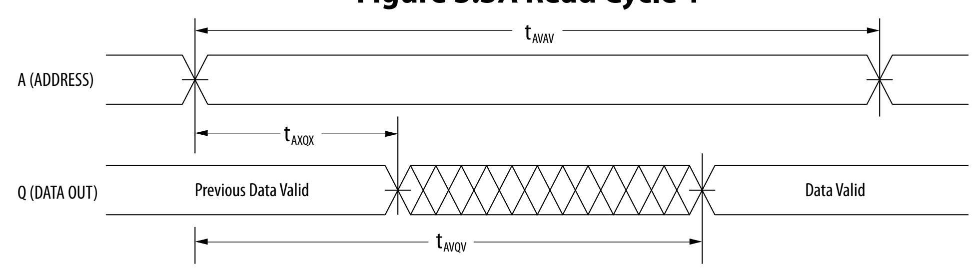
Parameter	Symbol	Min	Max	Unit
Read cycle time	t_{AVAV}	35	-	ns
Address access time	t_{AVQV}	-	35	ns
Enable access time[2]	t_{ELQV}	-	35	ns
Output enable access time	t_{GLQV}	-	15	ns
Byte enable access time	t_{BLQV}	-	15	ns
Output hold from address change	t_{AXQX}	3	-	ns
Enable low to output active[3]	t_{ELQX}	3	-	ns
Output enable low to output active[3]	t_{GLQX}	0	-	ns
Byte enable low to output active[3]	t_{BLQX}	0	-	ns
Enable high to output Hi-Z[3]	t_{EHQZ}	0	15	ns
Output enable high to output Hi-Z[3]	t_{GHQZ}	0	10	ns
Byte high to output Hi-Z[3]	t_{BHQZ}	0	10	ns

1 $\overline{W}$ is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.

2 Addresses valid before or at the same time $\overline{E}$ goes low.

3 This parameter is sampled and not 100% tested. Transition is measured ±200 mV from the steady-state voltage.

Figure 3.3A Read Cycle 1



Note: Device is continuously selected ($\overline{E} \leq V_{IL}$, $\overline{G} \leq V_{IL}$).

Figure 3.3B Read Cycle 2

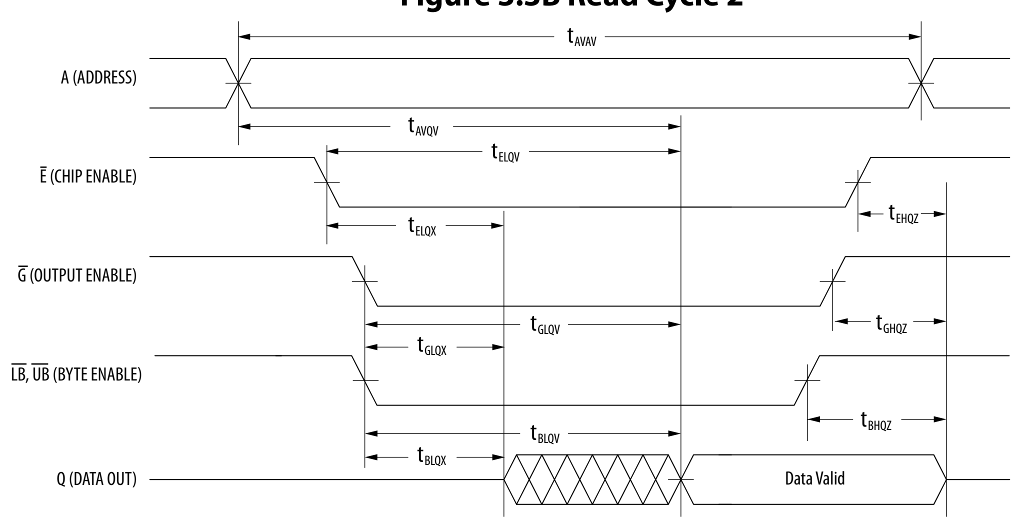


Table 3.4 Write Cycle Timing 1 ($\overline{W}$ Controlled)[1]

Parameter	Symbol	Min	Max	Unit
Write cycle time[2]	t_{AVAV}	35	-	ns
Address set-up time	t_{AVWL}	0	-	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVWH}	20	-	ns
Address valid to end of write ($\overline{G}$ low)	t_{AVWH}	20	-	ns
Write pulse width ($\overline{G}$ high)	t_{WLWH} t_{WLEH}	15	-	ns
Write pulse width ($\overline{G}$ low)	t_{WLWH} t_{WLEH}	15	-	ns
Data valid to end of write	t_{DVWH}	10	-	ns
Data hold time	t_{WHDX}	0	-	ns
Write low to data Hi-Z[3]	t_{WLQZ}	0	15	ns
Write high to output active[3]	t_{WHQX}	3	-	ns
Write recovery time	t_{WHAX}	12	-	ns

1 All write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$, $\overline{E}$ or $\overline{UB}$/$\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

2 All write cycle timings are referenced from the last valid address to the first transition address.

3 This parameter is sampled and not 100% tested. Transition is measured ±200 mV from the steady-state voltage. At any given voltage or temperate, t_{WLQZ}(max) < t_{WHQX}(min)

Figure 3.4 Write Cycle Timing 1 ($\overline{W}$ Controlled)

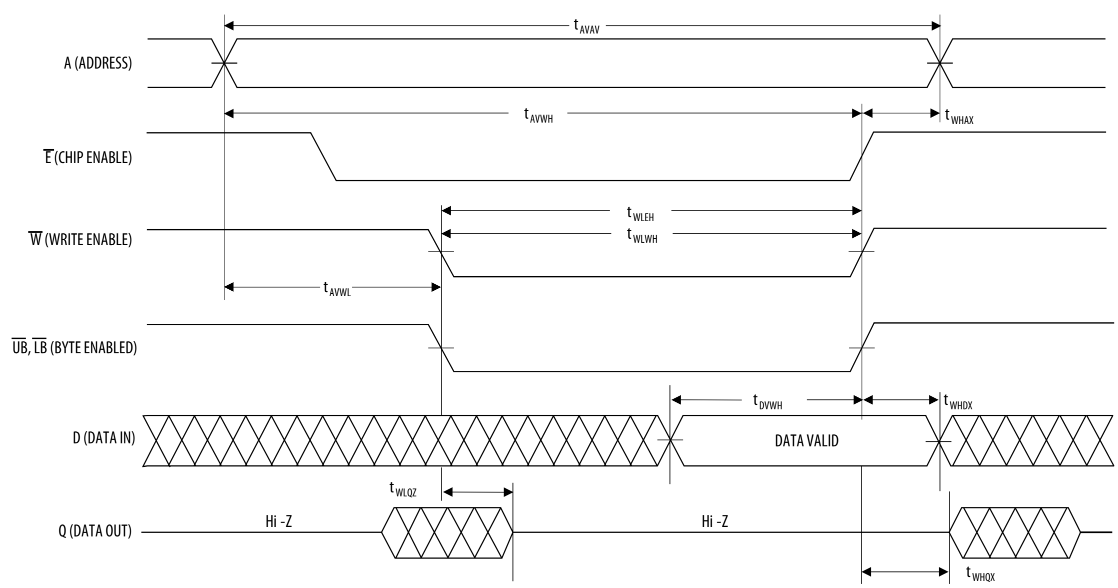


Table 3.5 Write Cycle Timing 2 ($\overline{E}$ Controlled)[1]

Parameter	Symbol	Min	Max	Unit
Write cycle time[2]	t_{AVAV}	35	-	ns
Address set-up time	t_{AVEL}	0	-	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVEH}	20	-	ns
Address valid to end of write ($\overline{G}$ low)	t_{AVEH}	20	-	ns
Enable to end of write ($\overline{G}$ high)	t_{ELEH} t_{ELWH}	15	-	ns
Enable to end of write ($\overline{G}$ low)[3]	t_{ELEH} t_{ELWH}	15	-	ns
Data valid to end of write	t_{DVEH}	10	-	ns
Data hold time	t_{EHDX}	0	-	ns
Write recovery time	t_{EHAX}	12	-	ns

1 All write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$, $\overline{E}$ or $\overline{UB}$/ $\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

2 All write cycle timings are referenced from the last valid address to the first transition address.

3 If $\overline{E}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state. If $\overline{E}$ goes high at the same time or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

Figure 3.5 Write Cycle Timing 2 ($\overline{E}$ Controlled)[1]

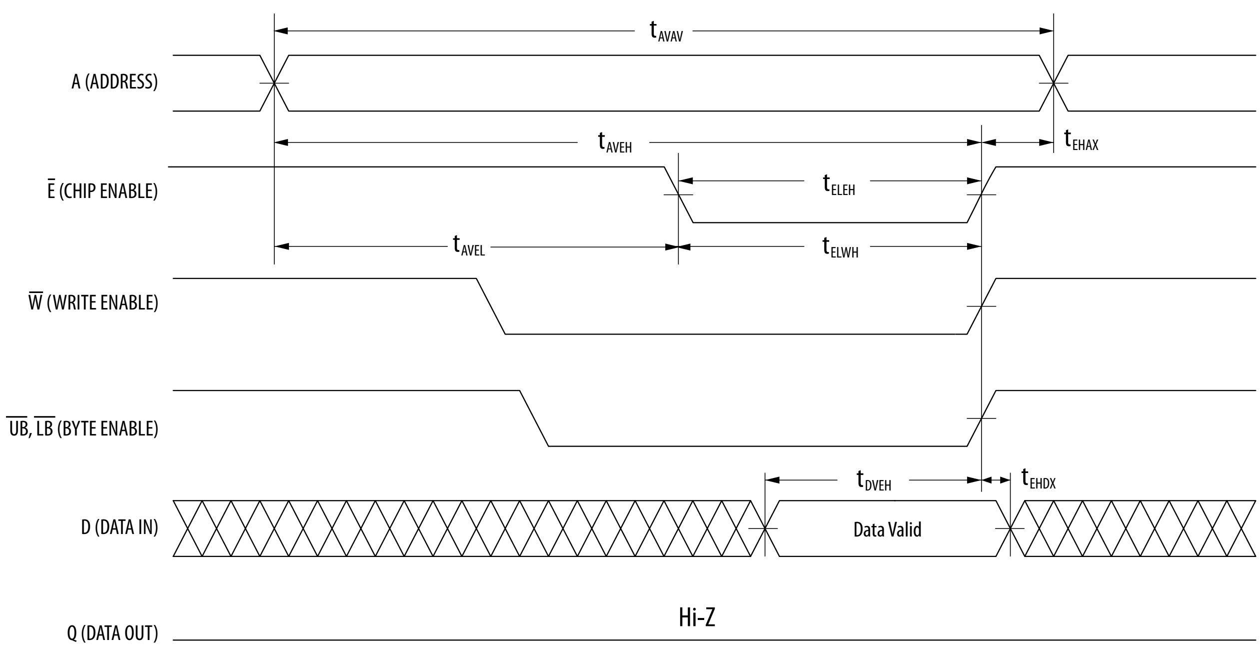


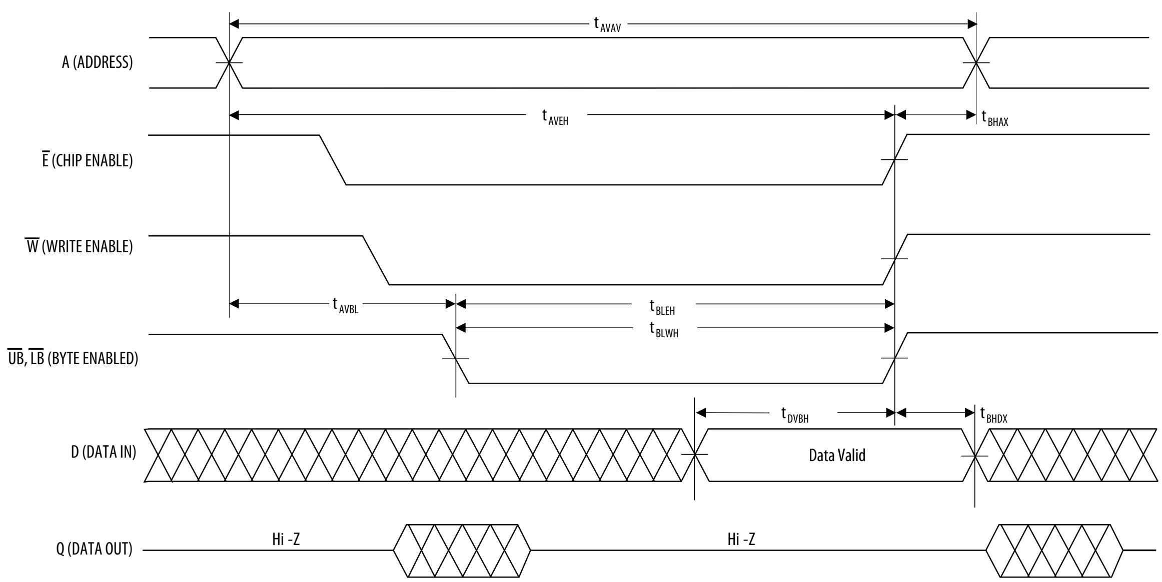
Table 3.6 Write Cycle Timing 3 ($\overline{LB}/\overline{UB}$ Controlled)[1]

Parameter	Symbol	Min	Max	Unit
Write cycle time[2]	t_{AVAV}	35	-	ns
Address set-up time	t_{AVBL}	0	-	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVBH}	20	-	ns
Address valid to end of write ($\overline{G}$ low)	t_{AVBH}	20	-	ns
Write pulse width ($\overline{G}$ high)	t_{BLEH} t_{BLWH}	15	-	ns
Write pulse width ($\overline{G}$ low)	t_{BLEH} t_{BLWH}	15	-	ns
Data valid to end of write	t_{DVBH}	10	-	ns
Data hold time	t_{BHDX}	0	-	ns
Write recovery time	t_{BHAX}	12	-	ns

1 All write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$, $\overline{E}$ or $\overline{UB}/\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

2 All write cycle timings are referenced from the last valid address to the first transition address.

Figure 3.6 Write Cycle Timing 3 ($\overline{LB}/\overline{UB}$ Controlled)



4. ORDERING INFORMATION

Figure 4.1 Part Numbering System

MR	4	A	16	B	C	MA	35	R

Carrier	Blank = Tray, R = Tape & Reel
Speed	35 ns
Package	MA = FBGA, YS = TSOP
Temperature Range	Blank= 0 to +70 °C, C= -40 to +85°C, M= -40 to +125 °C
Revision	
Data Width	16 = 16-bit
Type	A = Asynchronous
Density	4 =16Mb
Magnetoresistive RAM	

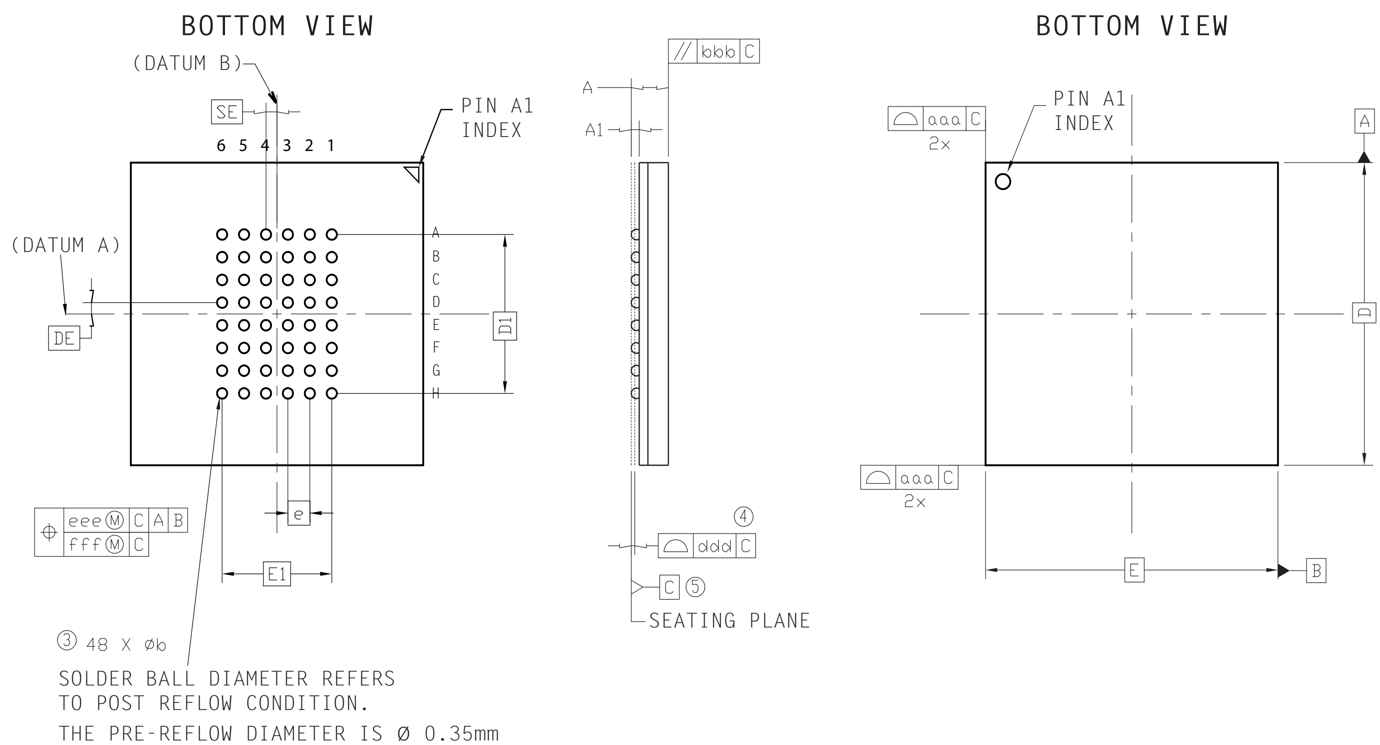
Table 4.1 Available Parts

Part Number	Description	Temperature
MR4A16BMA35[1]	3.3 V 1Mx16 MRAM 48-BGA	Commercial
MR4A16BCMA35[1]	3.3 V 1Mx16 MRAM 48-BGA	Industrial
MR4A16BMMA35[1]	3.3 V 1Mx16 MRAM 48-BGA	Automotive
MR4A16BYS35[1]	3.3 V 1Mx16 MRAM 54-TSOP	Commercial
MR4A16BCYS35[1]	3.3 V 1Mx16 MRAM 54-TSOP	Industrial
MR4A16BMYS35[1]	3.3 V 1Mx16 MRAM 54-TSOP	Automotive

Note 1: These products are classified as Preliminary, a product in development and/or qualification that has fixed target specifications that are subject to change pending characterization results.

5. MECHANICAL DRAWING

Figure 5.1 48-FBGA



Ref	Min	Nominal	Max
A	1.19	1.27	1.35
A1	0.22	0.27	0.32
b	0.31	0.36	0.41
D	10.00 BSC		
E	10.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
DE	0.375 BSC		
SE	0.375 BSC		
e	0.75 BSC		

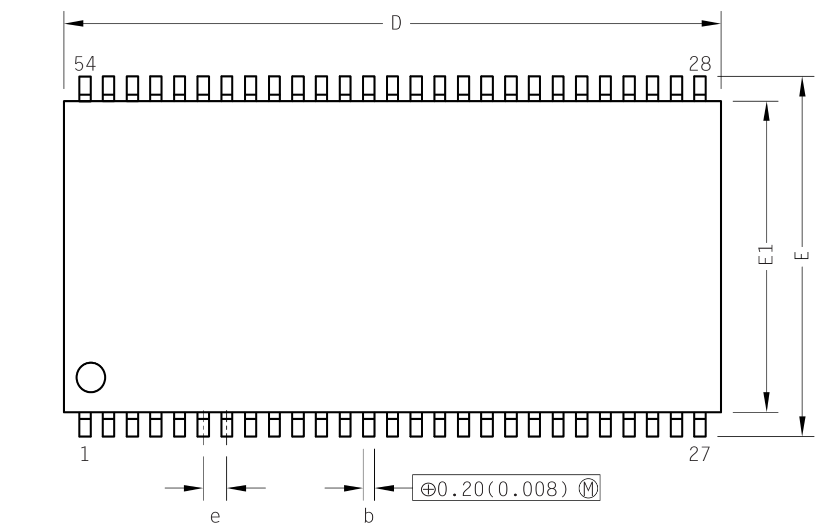
Ref	Tolerance of, from and position
aaa	0.10
bbb	0.10
ddd	0.12
eee	0.15
fff	0.08

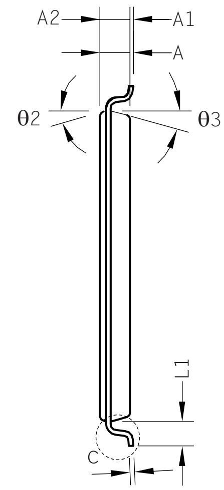
Print Version Not To Scale

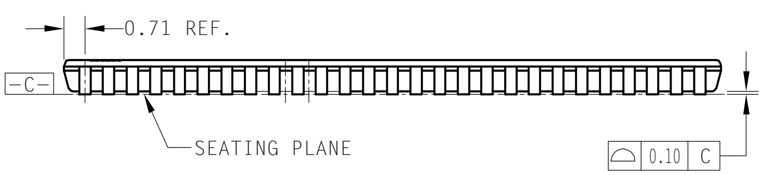
1. Dimensions in Millimeters.
2. The 'e' represents the basic solder ball grid pitch.
3. 'b' is measurable at the maximum solder ball diameter in a plane parallel to datum C.
4. Dimension 'ccc' is measured parallel to primary datum C.
5. Primary datum C (seating plane) is defined by the crowns
of the solder balls.
6. Package dimensions refer to JEDEC MO-205 Rev. G.

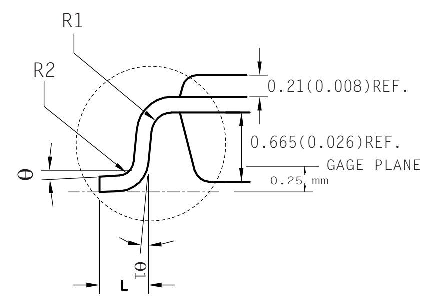
5. MECHANICAL DRAWING

Figure 5.2 54-TSOP









Ref	Min	Nominal	Max
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.30	0.35	0.45
c	0.12		0.21
D	22.10	22.22	22.35
E	11.56	11.76	11.95
E1	10.03	10.16	10.29
e	0.80 BSC		
L	0.40	0.50	0.60
L1	0.80 REF		
R1	0.12	-	-
R2	0.12	-	0.25
θ	0°	-	8°
θ1	0.40	-	-
θ2	15° REF		
θ3	15° REF		

Print Version Not To Scale

1. Dimensions in Millimeters.
2. Package dimensions refer to JEDEC MS-024

6. REVISION HISTORY

Revision	Date	Description of Change
1	May 29, 2009	Establish Speed and Power Specifications
2	July 27, 2009	Increase BGA Package to 11 mm x 11 mm
3	Nov 26, 2009	Changed ball definition of H6 to A19 and G2 to NC in Figure 1.2.
4	Mar 10, 2010	Changed speed marking and timing specs to 35 ns part. Changed BGA package to 10 mm x 10mm
5	Apr 7, 2010	Added 54-TSOP package options.

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