DDR3 SDRAM
Unbuffered SODIMMs
Based on 1Gb T-die

HMT112S6TFR8C
HMT125S6TFR8C

*Hynix Semiconductor reserves the right to change products or specifications without notice.

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Release	Sep.2009	Preliminary
1.0	JEDEC Update	Nov. 2009	Web posting
1.1	Add supported CL5	Jun. 2010	Web posting
1.2	DIMM Outline Corrected	Jul. 2010	Web posting

Description

Hynix Unbuffered Small Outline DDR3 SDRAM DIMMs (Unbuffered Small Outline Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use Hynix DDR3 SDRAM devices. These Unbuffered DDR3 SDRAM SODIMMs are intended for use as main memory when installed in systems such as mobile personal computers.

Features

- VDD=1.5V +/- 0.075V
- VDDQ=1.5V +/- 0.075V
- VDDSPD=3.0V to 3.6V
- Functionality and operations comply with the DDR3 SDRAM datasheet
- 8 internal banks
- Data transfer rates: PC3-10600, PC3-8500, or PC3-6400
- Bi-directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly: BL 8 or BC (Burst Chop) 4
- On Die Termination (ODT) supported
- RoHS compliant

* This product is in compliance with the RoHS directive.

Ordering Information

Part Number	Density	Organization	Component Composition	# of ranks
HMT112S6TFR8C-G7/H9	1GB	128Mx64	128Mx8(H5TQ1G83TFR)*8	1
HMT125S6TFR8C-G7/H9	2GB	256Mx64	128Mx8(H5TQ1G83TFR)*16	2

Key Parameters

MT/s	Grade	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
DDR3-1066	-G7	1.875	7	13.125	13.125	37.5	50.625	7-7-7
DDR3-1333	-H9	1.5	9	13.5	13.5	36	49.5	9-9-9

Speed Grade

Grade	Frequency [MHz]						Remark
	CL5	CL6	CL7	CL8	CL9	CL10	
-G7	667	800	1066	1066			
-H9	667	800	1066	1066	1333	1333	

Address Table

	1GB(1Rx8)	2GB(2Rx8)
Refresh Method	8K/64ms	8K/64ms
Row Address	A0-A13	A0-A13
Column Address	A0-A9	A0-A9
Bank Address	BA0-BA2	BA0-BA2
Page Size	1KB	1KB

Pin Descriptions

Pin Name	Description	Number	Pin Name	Description	Number
CK[1:0]	Clock Input, positive line	2	DQ[63:0]	Data Input/Output	64
$\overline{CK}$[1:0]	Clock Input, negative line	2	DM[7:0]	Data Masks	8
CKE[1:0]	Clock Enables	2	DQS[7:0]	Data strobes	8
$\overline{RAS}$	Row Address Strobe	1	$\overline{DQS}$[7:0]	Data strobes, negative line	8
$\overline{CAS}$	Column Address Strobe	1	$\overline{EVENT}$	Temperature event pin	1
$\overline{WE}$	Write Enable	1	TEST	Logic Analyzer specific test pin (No connect on SODIMM)	1
$\overline{S}$[1:0]	Chip Selects	2	$\overline{RESET}$	Reset Pin	1
A[9:0],A11, A[15:13]	Address Inputs	14	V_{DD}	Core and I/O Power	18
A10/AP	Address Input/Autoprecharge	1	V_{SS}	Ground	52
A12/$\overline{BC}$	Address Input/Burst chop	1			
BA[2:0]	SDRAM Bank Addresses	3	V_{REFDQ}	Input/Output Reference	1
ODT[1:0]	On Die Termination Inputs	2	V_{REFCA}		1
SCL	Serial Presence Detect (SPD) Clock Input	1	V_{TT}	Termination Voltage	2
SDA	SPD Data Input/Output	1	V_{DDSPD}	SPD Power	1
SA[1:0]	SPD Address Inputs	2	NC	Reserved for future use	2
				Total:	**204**

Input/Output Functional Descriptions

Symbol	Type	Polarity	Function
CK0/$\overline{CK0}$ CK1/$\overline{CK1}$	IN	Cross Point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE[1:0]	IN	Active High	Activates the DDR3 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S[1:0]}$	IN	Active Low	Enables the associated DDR3 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$.
ODT[1:0]	IN	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR3 SDRAM mode register.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	IN	Active Low	When sampled at the cross point of the rising edge of CK, signals $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REFDQ} V_{REFCA}	Supply		Reference voltage for SSTL15 inputs.
BA[2:0]	IN	—	Selects which SDRAM internal bank of eight is activated.
A[9:0], A10/AP, A11, A12/$\overline{BC}$ A[15:13]	IN	—	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read of Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge. A12($\overline{BC}$) is samples during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop: LOW, burst chopped).
DQ[63:0]	I/O	—	Data Input/Output pins.
DM[7:0]	IN	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
V_{DD}, V_{DDSPD} V_{SS}	Supply		Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
$\overline{DQS[7:0]}$, $\overline{DQS[7:0]}$	I/O	Cross Point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR3 SDRAMs and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$.
SA[1:0]	IN	—	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.

Symbol	Type	Polarity	Function
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pullup.
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DDSPD} on the system planar to act as a pullup.
$\overline{EVENT}$	OUT (open drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device.The system should guarantee the electrical level requirement is met for the $\overline{EVENT}$ pin on TS/SPD part. No pull-up resister is provided on DIMM.
V_{DDSPD}	Supply		Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation.
$\overline{RESET}$	IN		The $\overline{RESET}$ pin is connected to the $\overline{RESET}$ pin on the register and to the $\overline{RESET}$ pin on the DRAM.
TEST			Used by memory bus analysis tools (unused (NC) on memory DIMMs)

Pin Assignments

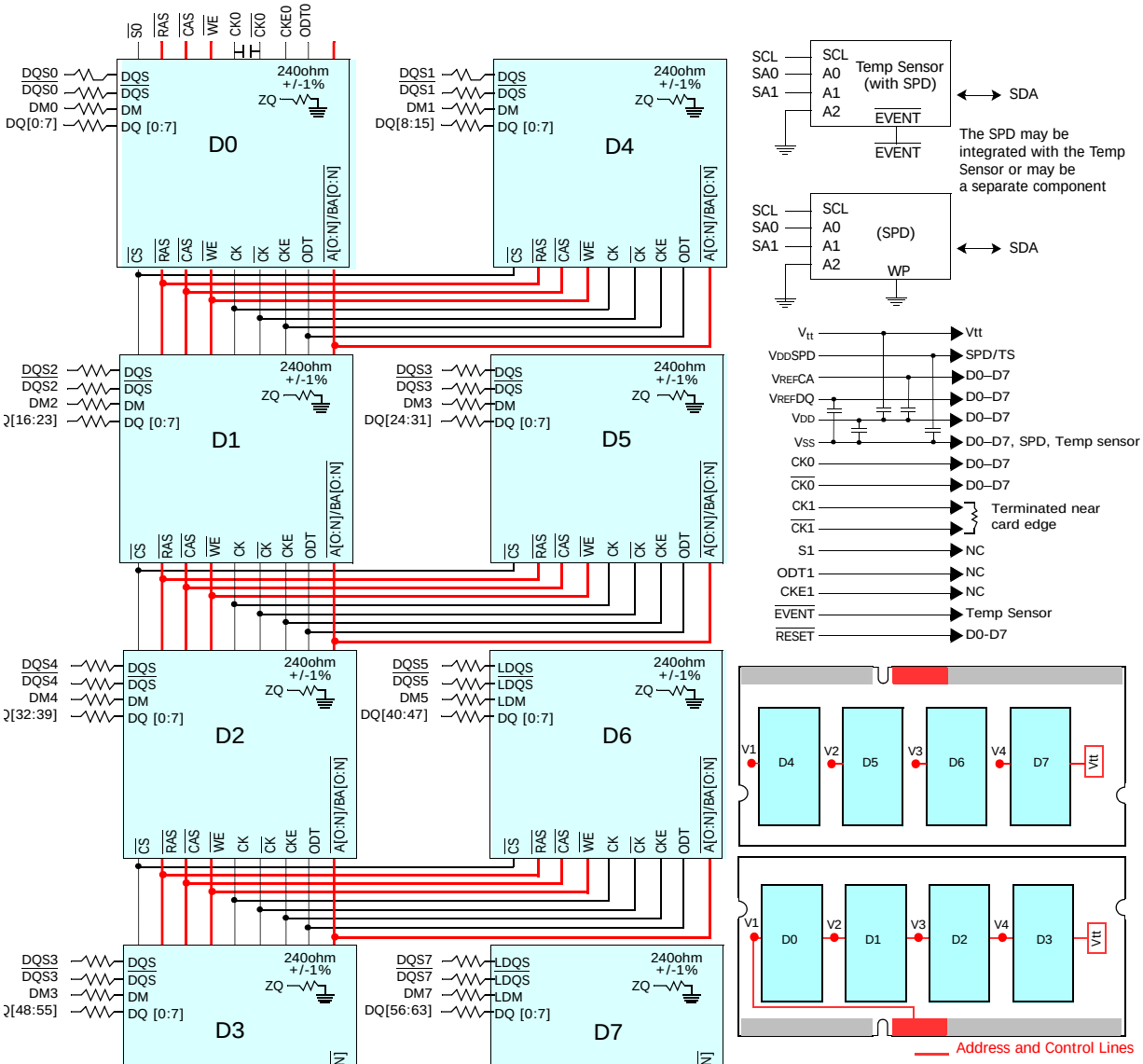
Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	$V_{REF}DQ$	2	V_{SS}	53	DQ19	54	V_{SS}	105	V_{DD}	106	V_{DD}	157	DQ42	158	DQ46
3	V_{SS}	4	DQ4	55	V_{SS}	56	DQ28	107	A10/AP	108	BA1	159	DQ43	160	DQ47
5	DQ0	6	DQ5	57	DQ24	58	DQ29	109	BA0	110	$\overline{RAS}$	161	V_{SS}	162	V_{SS}
7	DQ1	8	V_{SS}	59	DQ25	60	V_{SS}	111	V_{DD}	112	V_{DD}	163	DQ48	164	DQ52
9	V_{SS}	10	$\overline{DQS0}$	61	V_{SS}	62	$\overline{DQS3}$	113	$\overline{WE}$	114	$\overline{S0}$	165	DQ49	166	DQ53
11	DM0	12	DQS0	63	DM3	64	DQS3	115	$\overline{CAS}$	116	ODT0	167	V_{SS}	168	V_{SS}
13	V_{SS}	14	V_{SS}	65	V_{SS}	66	V_{SS}	117	V_{DD}	118	V_{DD}	169	$\overline{DQS6}$	170	DM6
15	DQ2	16	DQ6	67	DQ26	68	DQ30	119	A13[2]	120	ODT1	171	DQS6	172	V_{SS}
17	DQ3	18	DQ7	69	DQ27	70	DQ31	121	$\overline{S1}$	122	NC	173	V_{SS}	174	DQ54
19	V_{SS}	20	V_{SS}	71	V_{SS}	72	V_{SS}	123	V_{DD}	124	V_{DD}	175	DQ50	176	DQ55
21	DQ8	22	DQ12	73	CKE0	74	CKE1	125	TEST	126	$V_{REF}CA$	177	DQ51	178	V_{SS}
23	DQ9	24	DQ13	75	V_{DD}	76	V_{DD}	127	V_{SS}	128	V_{SS}	179	V_{SS}	180	DQ60
25	V_{SS}	26	V_{SS}	77	NC	78	A15[2]	129	DQ32	130	DQ36	181	DQ56	182	DQ61
27	$\overline{DQS1}$	28	DM1	79	BA2	80	A14[2]	131	DQ33	132	DQ37	183	DQ57	184	V_{SS}
29	DQS1	30	$\overline{RESET}$	81	V_{DD}	82	V_{DD}	133	V_{SS}	134	V_{SS}	185	V_{SS}	186	$\overline{DQS7}$
31	V_{SS}	32	V_{SS}	83	A12/$\overline{BC}$	84	A11	135	$\overline{DQS4}$	136	DM4	187	DM7	188	DQS7
33	DQ10	34	DQ14	85	A9	86	A7	137	DQS4	138	V_{SS}	189	V_{SS}	190	V_{SS}
35	DQ11	36	DQ15	87	V_{DD}	88	V_{DD}	139	V_{SS}	140	DQ38	191	DQ58	192	DQ62
37	V_{SS}	38	V_{SS}	89	A8	90	A6	141	DQ34	142	DQ39	193	DQ59	194	DQ63
39	DQ16	40	DQ20	91	A5	92	A4	143	DQ35	144	V_{SS}	195	V_{SS}	196	V_{SS}
41	DQ17	42	DQ21	93	V_{DD}	94	V_{DD}	145	V_{SS}	146	DQ44	197	SA0	198	$\overline{EVENT}$
43	V_{SS}	44	V_{SS}	95	A3	96	A2	147	DQ40	148	DQ45	199	VDD_{SPD}	200	SDA
45	$\overline{DQS2}$	46	DM2	97	A1	98	A0	149	DQ41	150	V_{SS}	201	SA1	202	SCL
47	DQS2	48	V_{SS}	99	V_{DD}	100	V_{DD}	151	V_{SS}	152	$\overline{DQS5}$	203	V_{TT}	204	V_{TT}
49	V_{SS}	50	DQ22	101	CK0	102	CK1	153	DM5	154	DQS5				
51	DQ18	52	DQ23	103	$\overline{CK0}$	104	$\overline{CK1}$	155	V_{SS}	156	V_{SS}				

NC = No Connect; RFU = Reserved Future Use

1. TEST (pin 125) is reserved for bus analysis probes and is NC on normal memory modules.
2. This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

Functional Block Diagram

1GB, 128Mx64 Module(1Rank of x8)

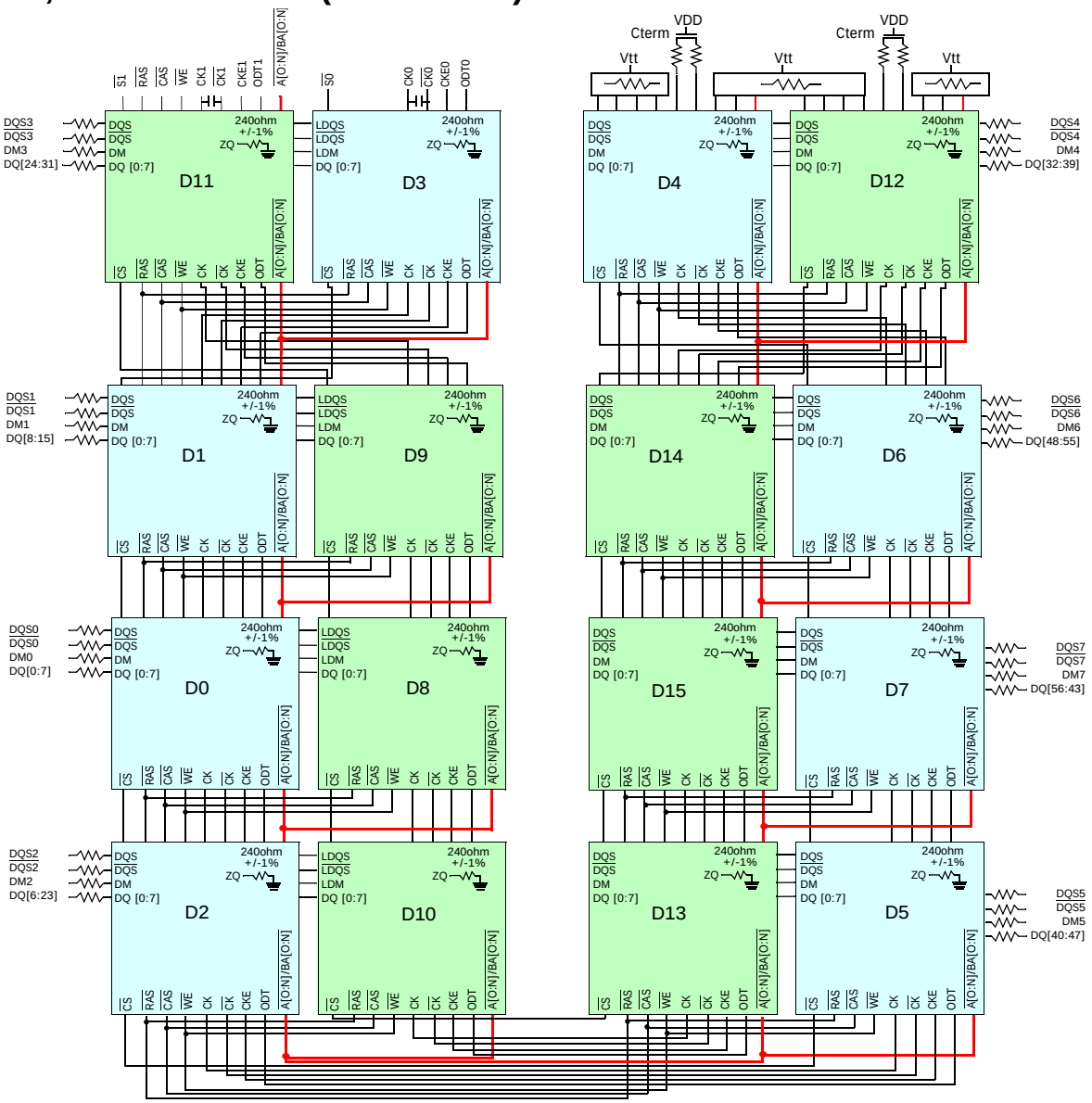


NOTES

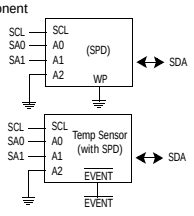
1. DQ wiring may differ from that shown however, DQ, DM, DQS, and DQS relationships are maintained as shown

Rank 0

2GB, 256Mx64 Module(2Rank of x8)

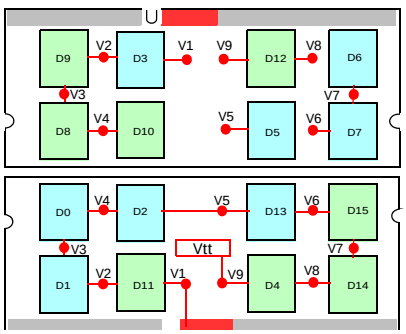


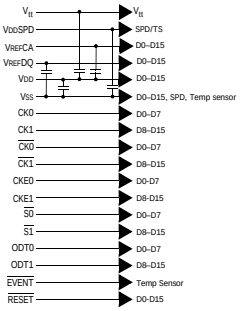
The SPD may be integrated with the Temp Sensor or may be a separate component



NOTES

1. DQ wiring may differ from that shown however, DQ, DM, DQS, and DQS relationships are maintained as shown





Absolute Maximum Ratings

Absolute Maximum DC Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.975 V	V	1,
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.975 V	V	1,
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	^{o}C	1, 2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6XVDDQ,When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

DRAM Component Operating Temperature Range

Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	^{o}C	1,2
	Extended Temperature Range	85 to 95	^{o}C	1,3

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85^{o}C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85^{o}C and 95^{o}C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
   b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). Hynix DDR3 SDRAMs support Auto Self-Refresh and Extended Temperature Range and please refer to Hynix component datasheet and/or the DIMM SPD for tREFI requirements in the Extended Temperature Range.

AC & DC Operating Conditions

Recommended DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

Notes:

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

AC & DC Input Measurement Levels

AC and DC Logic Input Levels for Single-Ended Signals

AC and DC Input Levels for Single-Ended Command and Address Signals

Single Ended AC and DC Input Levels for Command and ADDress

Symbol	Parameter	DDR3-800/1066/1333		Unit	Notes
		Min	Max		
VIH.CA(DC100)	DC input logic high	Vref + 0.100	VDD	V	1
VIL.CA(DC100)	DC input logic low	VSS	Vref - 0.100	V	1
VIH.CA(AC175)	AC input logic high	Vref + 0.175	Note2	V	1, 2
VIL.CA(AC175)	AC input logic low	Note2	Vref - 0.175	V	1, 2
VIH.CA(AC150)	AC Input logic high	Vref + 0.150	Note2	V	1, 2
VIL.CA(AC150)	AC input logic low	Note2	Vref - 0.150	V	1, 2
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4

Notes:

1. For input only pins except $\overline{\text{RESET}}$, Vref = VrefCA (DC).
2. Refer to “Overshoot and Undershoot Specifications” on page 25.
3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefCA(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.

AC and DC Input Levels for Single-Ended Signals

DDR3 SDRAM will support two Vih/Vil AC levels for DDR3-800 and DDR3-1066 as specified in the table below. DDR3 SDRAM will also support corresponding tDS values (Table 41 and Table 47 in " DDR3 Device Operation") as well as derating tables in Table 44 of "DDR3 Device Operation" depending on Vih/Vil AC levels.

Single Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800/1066		DDR3-1333		Unit	Notes
		Min	Max	Min	Max		
VIH.CA(DC100)	DC input logic high	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1
VIL.CA(DC100)	DC input logic low	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1
VIH.CA(AC175)	AC input logic high	Vref + 0.175	Note2	-	-	V	1, 2
VIL.CA(AC175)	AC input logic low	Note2	Vref - 0.175	-	-	V	1, 2
VIH.CA(AC150)	AC Input logic high	Vref + 0.150	Note2	Vref + 0.150	Note2	V	1, 2
VIL.CA(AC150)	AC input logic low	Note2	Vref - 0.150	Note2	Vref - 0.150	V	1, 2
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3, 4

Notes:

1. Vref = VrefDQ (DC).
2. Refer to "Overshoot and Undershoot Specifications" on page 25.
3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.

Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages $_{VRefCA}$ and V_{RefDQ} are illustrated in figure below. It shows a valid reference voltage V_{Ref} (t) as a function of time. (V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise).

V_{Ref} (DC) is the linear average of V_{Ref} (t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in the table "Differential Input Slew Rate Definition" on page 20. Furthermore V_{Ref} (t) may temporarily deviate from $V_{Ref\ (DC)}$ by no more than +/- 1% VDD.

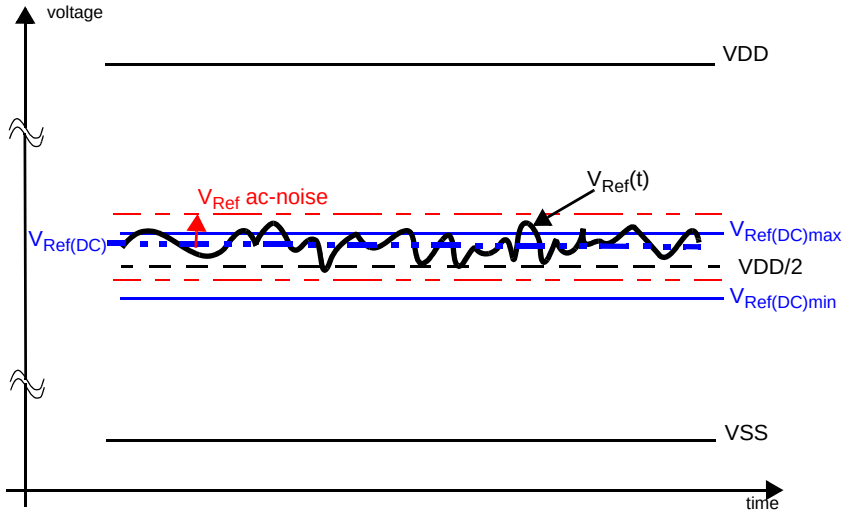


Illustration of $V_{Ref(DC)}$ tolerance and V_{Ref} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$, and $V_{IL(DC)}$ are dependent on V_{Ref}.

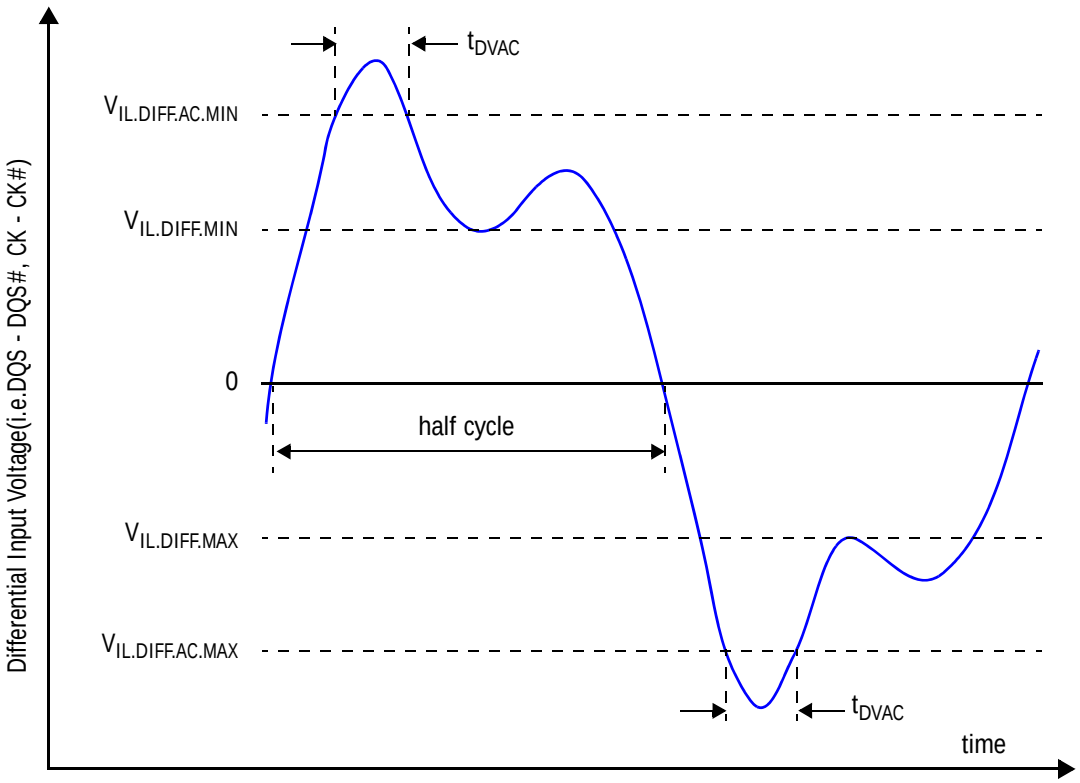
"V_{Ref}" shall be understood as $V_{Ref(DC)}$, as defined in figure above.

This clarifies that dc-variations of V_{Ref} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{Ref(DC)}$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{Ref}ac-noise. Timing and voltage effects due to ac-noise on V_{Ref} up to the specified limit (+/- 1% of VDD) are included in DRAM timings and their associated deratings.

AC and DC Logic Input Levels for Differential Signals

Differential signal definition



Definition of differential ac-swing and "time above ac-level" t_{DVAC}

Differential swing requirements for clock (CK - $\overline{CK}$) and strobe (DQS-$\overline{DQS}$)

Differential AC and DC Input Levels

Symbol	Parameter	DDR3-800, 1066, 1333		Unit	Notes
		Min	Max		
VIHdiff	Differential input high	+ 0.200	Note 3	V	1
VILdiff	Differential input logic low	Note 3	- 0.200	V	1
VIHdiff (ac)	Differential input high ac	2 x (VIH (ac) - Vref)	Note 3	V	2
VILdiff (ac)	Differential input low ac	Note 3	2 x (VIL (ac) - Vref)	V	2

Notes:

1. Used to define a differential signal slew-rate.
2. For CK - $\overline{CK}$ use VIH/VIL (ac) of AADD/CMD and VREFCA; for DQS - $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ use VIH/VIL (ac) of DQs and VREFDQ; if a reduced ac-high or ac-low levels is used for a signal group, then the reduced level applies also here.
3. These values are not defined; however, the single-ended signals Ck, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits (VIH (dc) max, VIL (dc) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to “Overshoot and Undershoot Specifications” on page 25.

Allowed time before ringback (tDVAC) for CK - $\overline{CK}$ and DQS - $\overline{DQS}$

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff (ac)| = 350mV		tDVAC [ps] @ |VIH/Ldiff (ac)| = 300mV	
	min	max	min	max
> 4.0	75	-	175	-
4.0	57	-	170	-
3.0	50	-	167	-
2.0	38	-	163	
1.8	34	-	162	-
1.6	29	-	161	-
1.4	22	-	159	-
1.2	13	-	155	-
1.0	0	-	150	-
< 1.0	0	-	150	-

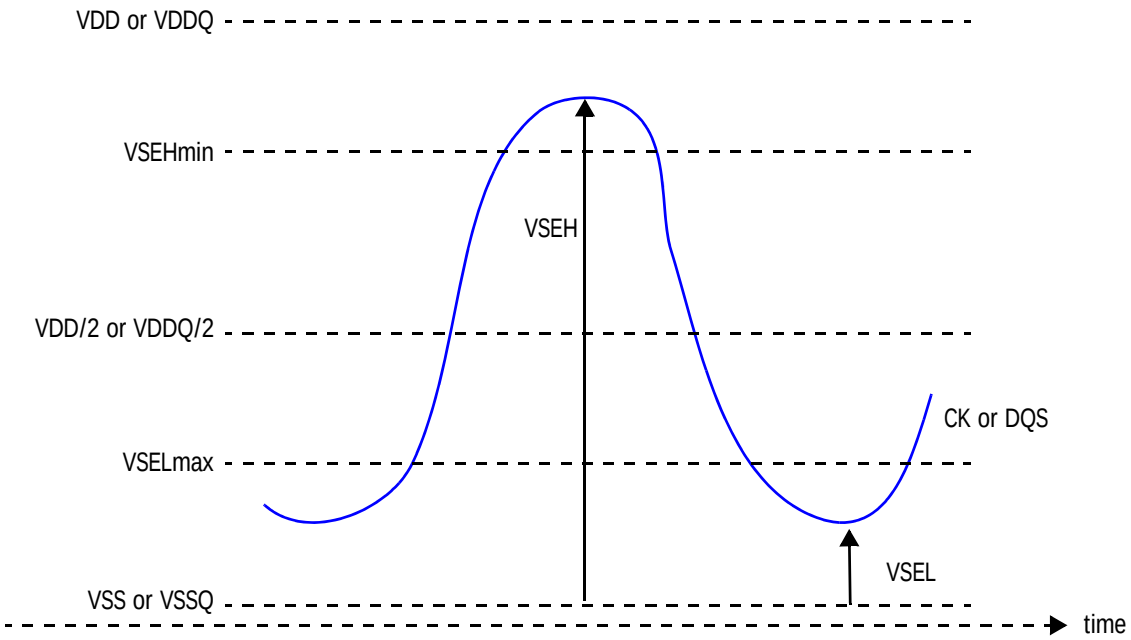
Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$, of $\overline{DQSU}$) has also to comply with certain requirements for single-ended signals.

CK and CK have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH (ac) / VIL (ac)) for ADD/CMD signals) in every half-cycle.

DQS, DQSL, DQSU, $\overline{DQS}$, $\overline{DQSL}$ have to reach VSEHmin / VSELmax (approximately the ac-levels (VIH (ac) / VIL (ac)) for DQ signals) in every half-cycle preceding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g., if VIH.CA(AC150)/VIL.CA(AC150) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and $\overline{CK}$.



Single-ended requirements for differential signals.

Note that, while ADD/CMD and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. the transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-ended levels for CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$ or $\overline{DQSU}$

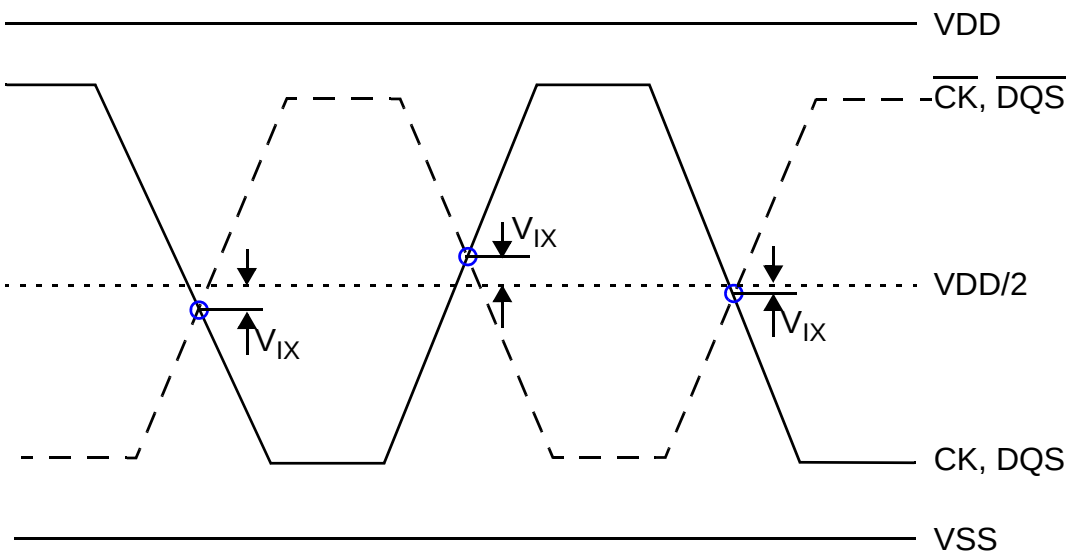
Symbol	Parameter	DDR3-800, 1066, 1333		Unit	Notes
		Min	Max		
VSEH	Single-ended high level for strobes	(VDD / 2) + 0.175	Note 3	V	1,2
	Single-ended high level for Ck, $\overline{CK}$	(VDD /2) + 0.175	Note 3	V	1,2
VSEL	Single-ended low level for strobes	Note 3	(VDD / 2) = 0.175	V	1,2
	Single-ended low level for CK, $\overline{CK}$	Note 3	(VDD / 2) = 0.175	V	1,2

Notes:

1. For CK, $\overline{CK}$ use VIH/VIL (ac) of ADD/CMD; for strobes (DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$) use VIH/VIL (ac) of DQs.
2. VIH (ac)/VIL (ac) for DQs is based on VREFDQ; VIH (ac)/VIL (ac) for ADD/CMD is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined; however, the single-ended signals Ck, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits (VIH (dc) max, VIL (dc) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to “Overshoot and Undershoot Specifications” on page 25.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in the table below. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS



Vix Definition

Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	DDR3-800, 1066, 1333		Unit	Notes
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2 for CK, $\overline{CK}$	-150	150	mV	
		-175	175	mV	1
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2 for DQS, $\overline{DQS}$	-150	150	mV	

Notes:

1. Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and $\overline{CK}$ are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-250 mV, and when the differential slew rate of CK - $\overline{CK}$ is larger than 3 V/ns.
2. Refer to the table “Single-ended levels for CK, DQS, DQSL, DQSU, CK, DQS, DQSL or DQSU” on page 18 for VSEL and VSEH standard values.

Slew Rate Definitions for Single-Ended Input Signals

See 7.5 “Address / Command Setup, Hold and Derating” on page 137 in “DDR3 Device Operation” for single-ended slew rate definitions for address and command signals.

See 7.6 “Data Setup, Hold and Slew Rate Derating” on page 144 in “DDR3 Device Operation” for single-ended slew rate definition for data signals.

Slew Rate Definitions for Differential Input Signals

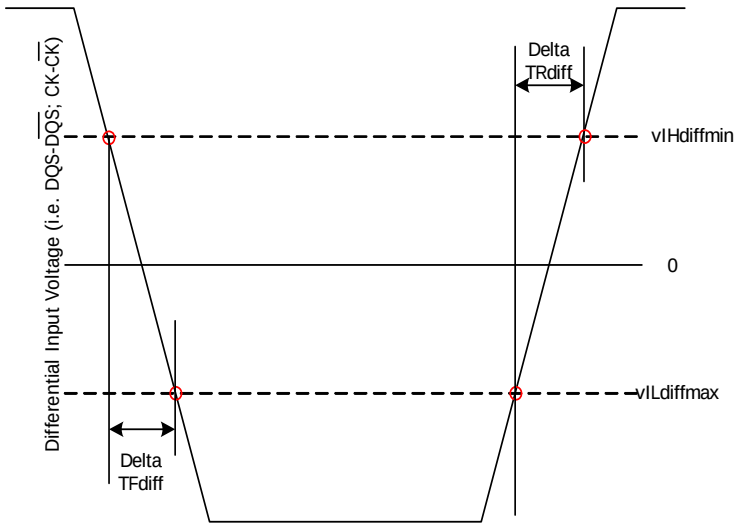
Input slew rate for differential signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) are defined and measured as shown in table and figure below.

Differential Input Slew Rate Definition

Description	Measured		Defined by
	Min	Max	
Differential input slew rate for rising edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VILdiffmax	VIHdiffmin	[VIHdiffmin-VILdiffmax] / DeltaTRdiff
Differential input slew rate for falling edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	VIHdiffmin	VILdiffmax	[VIHdiffmin-VILdiffmax] / DeltaTFdiff

Notes:

The differential signal (i.e. CK-$\overline{CK}$ and DQS-$\overline{DQS}$) must be linear between these thresholds.



Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#

Differential Input Slew Rate Definition for DQS, $\overline{DQS}$ and CK, $\overline{CK}$

AC & DC Output Measurement Levels

Single Ended AC and DC Output Levels

Table below shows the output levels used for measurements of single ended signals.

Single-ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, 1066, 1333	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	V_{TT} + 0.1 x V_{DDQ}	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	V_{TT} - 0.1 x V_{DDQ}	V	1

Notes:

1. The swing of ± 0.1 x V_{DDQ} is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT} = V_{DDQ} / 2.

Differential AC and DC Output Levels

Table below shows the output levels used for measurements of single ended signals.

Differential AC and DC Output Levels

Symbol	Parameter	DDR3-800, 1066, 1333	Unit	Notes
$V_{OHdiff\ (AC)}$	AC differential output high measurement level (for output SR)	+ 0.2 x V_{DDQ}	V	1
$V_{OLdiff\ (AC)}$	AC differential output low measurement level (for output SR)	- 0.2 x V_{DDQ}	V	1

Notes:

1. The swing of ± 0.2 x V_{DDQ} is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.

Single Ended Output Slew Rate

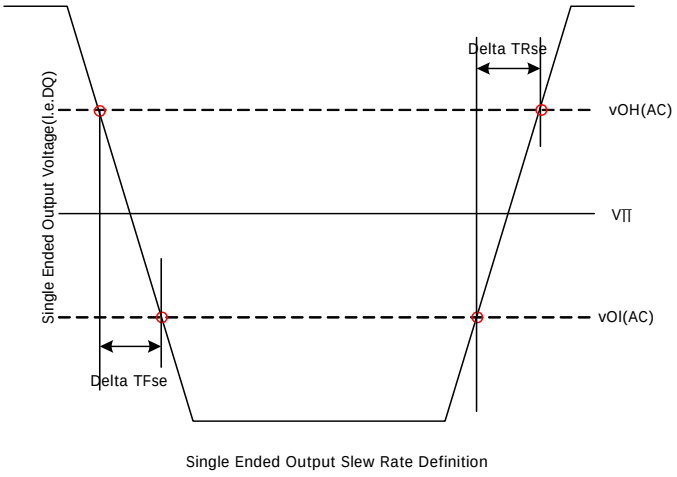
When the Reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals are shown in table and figure below.

Single-ended Output slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)}-V_{OL(AC)}]$ / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)}-V_{OL(AC)}]$ / DeltaTFse

Notes:

1. Output slew rate is verified by design and characterisation, and may not be subject to production test.



Single Ended Output slew Rate Definition

Output Slew Rate (single-ended)

		DDR3-800		DDR3-1066		DDR3-1333		Units
Parameter	Symbol	Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5	2.5	5	V/ns

Description: SR; Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

Differential Output Slew Rate

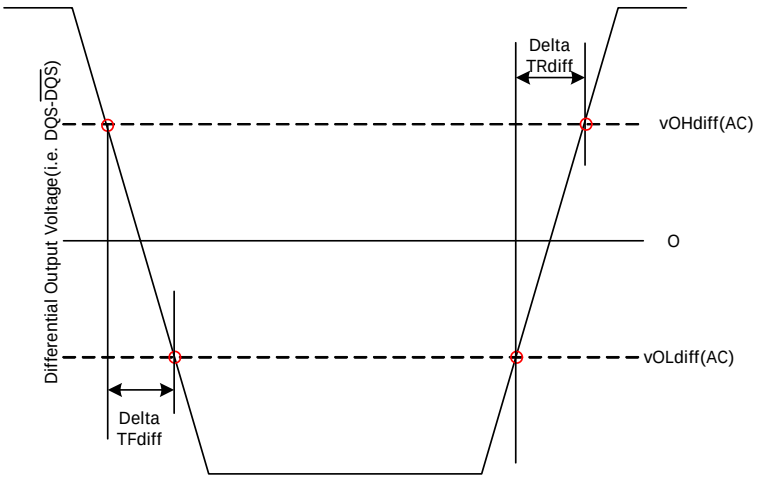
With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff (AC) and VOHdiff (AC) for differential signals as shown in table and figure below.

Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff\ (AC)}$	$V_{OHdiff\ (AC)}$	$[V_{OHdiff\ (AC)}-V_{OLdiff\ (AC)}]$ / DeltaTRdiff
Differential output slew rate for falling edge	$V_{OHdiff\ (AC)}$	$V_{OLdiff\ (AC)}$	$[V_{OHdiff\ (AC)}-V_{OLdiff\ (AC)}]$ / DeltaTFdiff

Notes:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.



Differential Output Slew Rate Definition

Differential Output slew Rate Definition

Differential Output Slew Rate

		DDR3-800		DDR3-1066		DDR3-1333		Units
Parameter	Symbol	Min	Max	Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	5	10	5	10	5	10	V/ns

Description: SR; Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

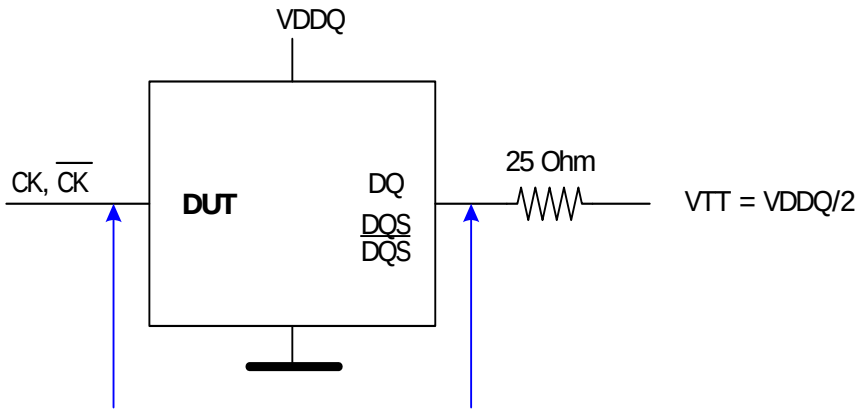
se: Single-ended Signals

For Ron = RZQ/7 setting

Reference Load for AC Timing and Output Slew Rate

Figure below represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



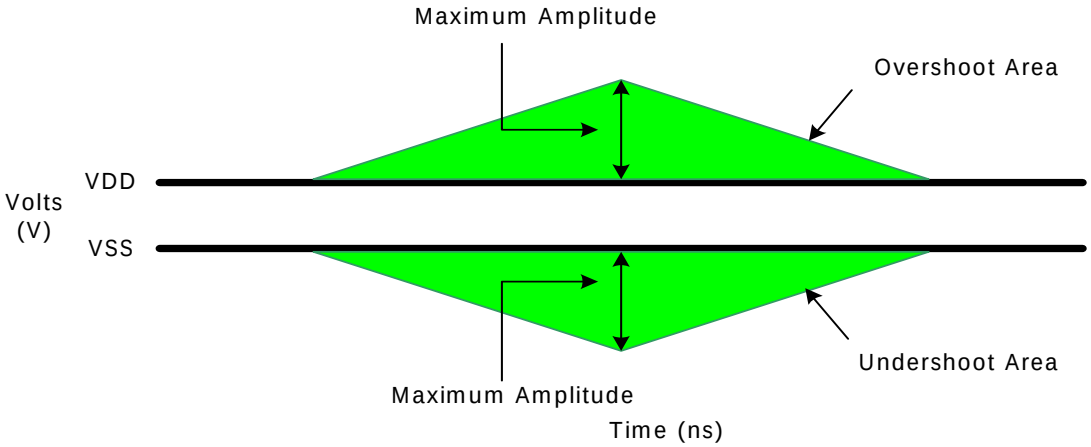
Reference Load for AC Timing and Output Slew Rate

Overshoot and Undershoot Specifications

Address and Control Overshoot and Undershoot Specifications

AC Overshoot/Undershoot Specification for Address and Control Pins

Parameter	DDR3-800	DDR3-1066	DDR3-1333	Units
Maximum peak amplitude allowed for overshoot area. (See figure below)	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area. (See figure below)	0.4	0.4	0.4	V
Maximum overshoot area above VDD (See figure below)	0.67	0.5	0.4	V-ns
Maximum undershoot area below VSS (See figure below)	0.67	0.5	0.4	V-ns
(A0-A15, BA0-BA3, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT) See figure below for each parameter definition				



Address and Control Overshoot and Undershoot Definition

Address and Control Overshoot and Undershoot Definition

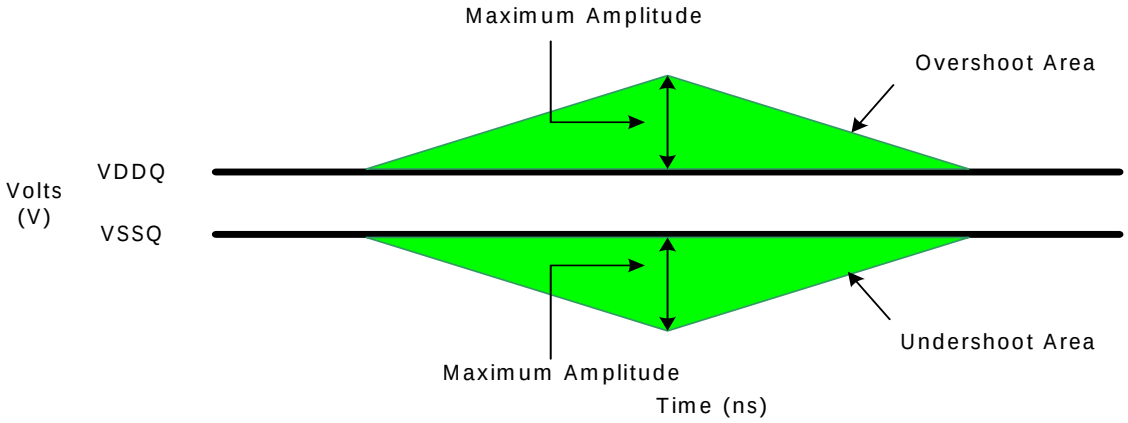
Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask

Parameter	DDR3-800	DDR3-1066	DDR3-1333	Units
Maximum peak amplitude allowed for overshoot area (See figure below)	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area (See figure below)	0.4	0.4	0.4	V
Maximum overshoot area above VDD (See figure below)	0.25	0.19	0.15	V-ns
Maximum undershoot area below VSS (See figure below)	0.25	0.19	0.15	V-ns

(CK, $\overline{CK}$, DQ, DQS, $\overline{DQS}$, DM)

See figure below for each parameter definition



Clock, Data Strobe and Mask Overshoot and Undershoot Definition

Clock, Data, Strobe and Mask Overshoot and Undershoot Definition

Refresh parameters by device density

Refresh parameters by device density

Parameter	RTT_Nom Setting		512Mb	1Gb	2Gb	4Gb	8Gb	Units
REF command ACT or REF command time	tRFC		90	110	160	300	350	ns
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85 °C	7.8	7.8	7.8	7.8	7.8	us
		85 °C < T_{CASE} ≤ 95 °C	3.9	3.9	3.9	3.9	3.9	us

Standard Speed Bins

DDR3 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

DDR3-800 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 31.

Speed Bin			DDR3-800E		Unit	Notes
CL - nRCD - nRP			6-6-6			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	15	—	ns	
PRE command period		t_{RP}	15	—	ns	
ACT to ACT or REF command period		t_{RC}	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	ns	1, 2, 3, 4, 10
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1, 2, 3
Supported CL Settings			5, 6		n_{CK}	10
Supported CWL Settings			5		n_{CK}	

DDR3-1066 Speed Bins

For specific Notes See “Speed Bin Table Notes” on page 31.

Speed Bin			DDR3-1066F		Unit	Note
CL - nRCD - nRP			7-7-7			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.125	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.125	—	ns	
PRE command period		t_{RP}	13.125	—	ns	
ACT to ACT or REF command period		t_{RC}	50.625	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	ns	1, 2, 3, 4, 6, 10
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1, 2, 3, 6
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1, 2, 3, 4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1, 2, 3
Supported CL Settings			5, 6, 7, 8		n_{CK}	10
Supported CWL Settings			5, 6		n_{CK}	

DDR3-1333 Speed Bins

For specific Notes See “Speed Bin Table Notes” on page 31.

Speed Bin			DDR3-1333H		Unit	Note
CL - nRCD - nRP			9-9-9			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.5 (13.125)[8]	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.5 (13.125)[8]	—	ns	
PRE command period		t_{RP}	13.5 (13.125)[8]	—	ns	
ACT to ACT or REF command period		t_{RC}	49.5 (49.125)[8]	—	ns	
ACT to PRE command period		t_{RAS}	36	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	ns	1, 2, 3, 4, 7, 10
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1, 2, 3, 7
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1, 2, 3, 4, 7
			(Optional)[5]			
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1, 2, 3, 7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1, 2, 3, 4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1, 2, 3
			(Optional)		ns	5
Supported CL Settings			5, 6, 8, (7), 9, (10)		n_{CK}	
Supported CWL Settings			5, 6, 7		n_{CK}	

Speed Bin Table Notes

Absolute Specification (T_{OPER}; V_{DDQ} = V_{DD} = 1.5V +/- 0.075 V);

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to Hynix DIMM data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Hynix DDR3 SDRAM devices supporting optional down binning to CL=7 and CL=9, and tAA/tRCD/tRP must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333H devices supporting down binning to DDR3-1066F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600K devices supporting down binning to DDR3-1333H or DDR3-1600F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accordingly. For example, 49.125ns (tRASmin + tRPmin = 36 ns + 13.125 ns) for DDR3-1333H and 48.125ns (tRASmin + tRPmin = 35 ns + 13.125 ns) for DDR3-1600K.
10. For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD coding.

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating temperature	0 to 65	^{o}C	1, 3
H_{OPR}	Operating humidity (relative)	10 to 90	%	1
T_{STG}	Storage temperature	-50 to +100	^{o}C	1
H_{STG}	Storage humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2

Note:

1. Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Expousure to absolute maximum rating conditions for extended periods may affect reliablility.
2. Up to 9850 ft.
3. The designer must meet the case temperature specifications for individual module components.

Pin Capacitance (VDD=1.5V, VDDQ=1.5V)

1GB: HMT112S6TFR8C

Pin	Symbol	Min	Max	Unit
CK0, $\overline{CK0}$	C_{CK}	TBD	TBD	pF
CKE, ODT, $\overline{CS}$	C_{CTRL}	TBD	TBD	pF
Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_I	TBD	TBD	pF
DQ, DM, DQS, $\overline{DQS}$	C_{IO}	TBD	TBD	pF

2GB: HMT125S6TFR8C

Pin	Symbol	Min	Max	Unit
CK0, $\overline{CK0}$	C_{CK}	TBD	TBD	pF
CKE, ODT, $\overline{CS}$	C_{CTRL}	TBD	TBD	pF
Address, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_I	TBD	TBD	pF
DQ, DM, DQS, $\overline{DQS}$	C_{IO}	TBD	TBD	pF

Note:

1. Pins not under test are tied to GND.
2. These value are guaranteed by design and tested on a sample basis only.

IDD and IDDQ Specification Parameters and Test Conditions

IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 1. shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- ”0” and “LOW” is defined as VIN <= $V_{ILAC(max)}$.
- ”1” and “HIGH” is defined as VIN >= $V_{IHAC(max)}$.
- “MID_LEVEL” is defined as inputs are VREF = VDD/2.
- Timing used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 1.
- Basic IDD and IDDQ Measurement Conditions are described in Table 2.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 3 through Table 10.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  Qoff = 0_B (Output Buffer enabled in MR1);
  RTT_Nom = RZQ/6 (40 Ohm in MR1);
  RTT_Wr = RZQ/2 (120 Ohm in MR2);
  TDQS Feature disabled in MR1
- Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, LOW, LOW, LOW}

Define $\overline{D}$ = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, HIGH, HIGH, HIGH}

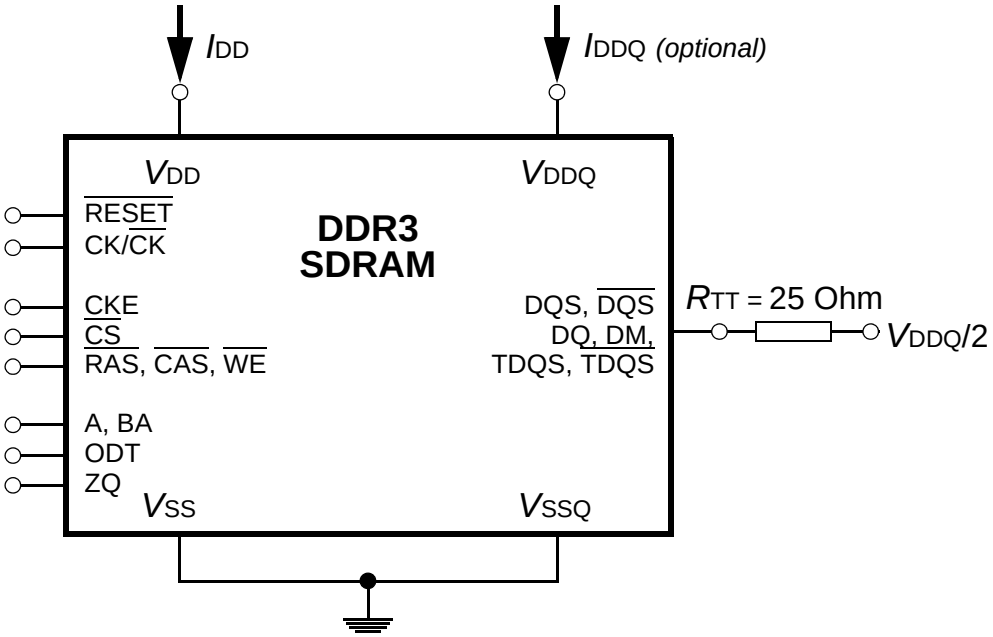


Figure 1 - Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements
[Note: DIMM level Output test load condition may be different from above

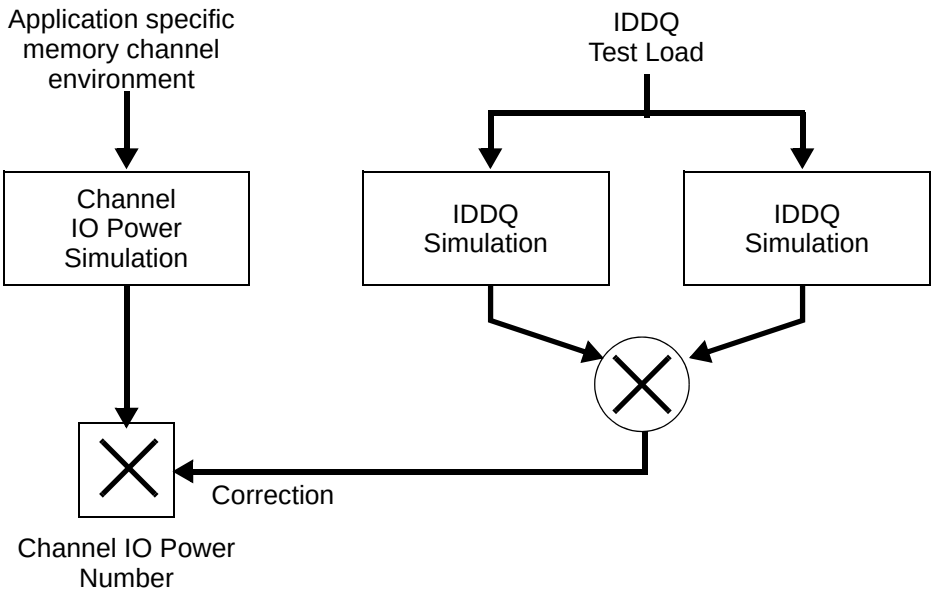


Figure 2 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

Table 1 -Timings used for IDD and IDDQ Measurement-Loop Patterns

Symbol		DDR3-1066	DDR3-1333	Unit
		7-7-7	9-9-9	
t_{CK}		1.875	1.5	ns
CL		7	9	nCK
n_{RCD}		7	9	nCK
n_{RC}		27	33	nCK
n_{RAS}		20	24	nCK
n_{RP}		7	9	nCK
n_{FAW}	1KB page size	20	20	nCK
	2KB page size	27	30	nCK
n_{RRD}	1KB page size	4	4	nCK
	2KB page size	6	5	nCK
n_{RFC} -512Mb		48	60	nCK
n_{RFC}-1 Gb		59	74	nCK
n_{RFC}- 2 Gb		86	107	nCK
n_{RFC}- 4 Gb		160	200	nCK
n_{RFC}- 8 Gb		187	234	nCK

Table 2 -Basic IDD and IDDQ Measurement Conditions

Symbol	Description
I_{DD0}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 3; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 3.
I_{DD1}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between ACT, RD and PRE; Command, Address; Bank Address Inputs, Data IO: partially toggling according to Table 4; DM: stable at 0; Bank Activity: Cycling with on bank active at a time: 0,0,1,1,2,2,... (see Table 4); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 4.

Symbol	Description
I_{DD2N}	Precharge Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 5.
I_{DD2NT}	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 6; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: toggling according to Table 6; Pattern Details: see Table 6.
I_{DD2P0}	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit[c]
I_{DD2P1}	Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit[c]
I_{DD2Q}	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0
I_{DD3N}	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 5.
I_{DD3P}	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0

Symbol	Description
I_{DD4R}	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between RD; Command, Address, Bank Address Inputs: partially toggling according to Table 7; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...(see Table 7); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 7.
I_{DD4W}	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between WR; Command, Address, Bank Address Inputs: partially toggling according to Table 8; Data IO: seamless read data burst with different data between one burst and the next one according to Table 8; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...(see Table 8); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at HIGH; Pattern Details: see Table 8.
I_{DD5B}	Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between REF; Command, Address, Bank Address Inputs: partially toggling according to Table 9; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: REF command every nREF (see Table 9); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 9.
I_{DD6}	Self-Refresh Current: Normal Temperature Range T_{CASE}: 0 - 85 °C; Auto Self-Refresh (ASR): Disabled[d];Self-Refresh Temperature Range (SRT): Normal[e]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: MID_LEVEL
I_{DD6ET}	Self-Refresh Current: Extended Temperature Range T_{CASE}: 0 - 95 °C; Auto Self-Refresh (ASR): Disabled[d];Self-Refresh Temperature Range (SRT): Extended[e]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: MID_LEVEL

Symbol	Description
I_{DD6TC}	Auto Self-Refresh Current T_{CASE}: 0 - 95 °C; Auto Self-Refresh (ASR): Enabled[d];Self-Refresh Temperature Range (SRT): Normal[e]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: MID_LEVEL
I_{DD7}	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, NRRD, nFAW, CL: see Table 1; BL: 8[a,f]; AL: CL-1; $\overline{CS}$: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to Table 10; Data IO: read data burst with different data between one burst and the next one according to Table 10; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different address-ing, wee Table 10; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 10.

a) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

b) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B

c) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12 = 1B for Fast Exit

d) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature

e) Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range

f) Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B

Table 3 - IDD0 Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1, 2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3, 4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 1*nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 2*nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.

b) DQ signals are MID-LEVEL.

Table 4 - IDD1 Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRCD - 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until nRC + nRCE - 1, truncate if necessary												
			1*nRC+nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			...	repeat pattern nRC + 1,...4 until nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until *2 nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID_LEVEL.

Table 5 - IDD2N and IDD3N Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	8-11	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	12-15	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	16-19	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	20-23	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	24-17	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	28-31	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.

b) DQ signals are MID-LEVEL.

Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1												
		2	8-11	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2												
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3												
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4												
		5	20-23	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5												
		6	24-17	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.

b) DQ signals are MID-LEVEL.

Table 7 - IDD4R and IDDQ4R Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 8 - IDD4W Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to WR Commands, otherwise MID-LEVEL.
b) Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 9 - IDD5B Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	-
		1	1.2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			5...8	repeat cycles 1...4, but BA[2:0] = 1												
			9...12	repeat cycles 1...4, but BA[2:0] = 2												
			13...16	repeat cycles 1...4, but BA[2:0] = 3												
			17...20	repeat cycles 1...4, but BA[2:0] = 4												
			21...24	repeat cycles 1...4, but BA[2:0] = 5												
			25...28	repeat cycles 1...4, but BA[2:0] = 6												
			29...32	repeat cycles 1...4, but BA[2:0] = 7												
		2	33...nRFC-1	repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary.												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
b) DQ signals are MID-LEVEL.

Table 10 - IDD7 Measurement-Loop Pattern[a)]

ATTENTION! Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD+1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD+2	D	1	0	0	0	0	1	00	0	0	F	0	-
			...	repeat above D Command until 2* nRRD - 1												
		2	2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4*nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
				Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW+nRRD	repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW+2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW+3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 7												
		9	nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
				Assert and repeat above D Command until 2* nFAW - 1, if necessary												
		10	2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
			2&nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2* nFAW + nRRD - 1												
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2&nFAW+nRRD+2	D	1	0	0	0	0	1	00	0	0	0	0	-
				Repeat above D Command until 2* nFAW + 2* nRRD - 1												
		12	2*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 2												
		13	2*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 3												
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	3	00	0	0	0	0	-
				Assert and repeat above D Command until 3* nFAW - 1, if necessary												
		15	3*nFAW	repeat Sub-Loop 10, but BA[2:0] = 4												
		16	3*nFAW+nRRD	repeat Sub-Loop 11, but BA[2:0] = 5												
		17	3*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 6												
		18	3*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 7												
		19	3*nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	0	0	-
				Assert and repeat above D Command until 4* nFAW - 1, if necessary												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

IDD Specifications (Tcase: 0 to 95°C)

* Module IDD values in the datasheet are only a calculation based on the component IDD spec.
The actual measurements may vary according to DQ loading cap.

1GB, 128M x 64 SO-DIMM: HMT112S6TFR8C

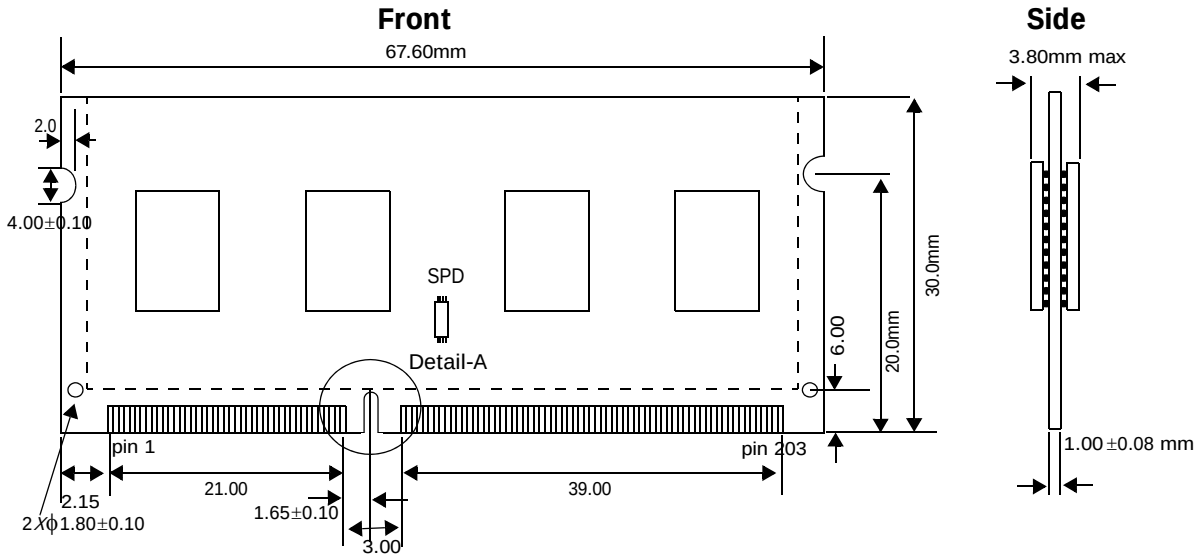
Symbol	DDR3 1066	DDR3 1333	Unit	note
IDD0	360	400	mA	
IDD1	480	520	mA	
IDD2N	240	280	mA	
IDD2NT	280	320	mA	
IDD2P0	80	80	mA	
IDD2P1	200	280	mA	
IDD2Q	240	280	mA	
IDD3N	280	320	mA	
IDD3P	160	200	mA	
IDD4R	720	840	mA	
IDD4W	720	840	mA	
IDD5B	1080	1120	mA	
IDD6	80	80	mA	
IDD6ET	96	96	mA	
IDD6TC	96	96	mA	
IDD7	1040	1280	mA	

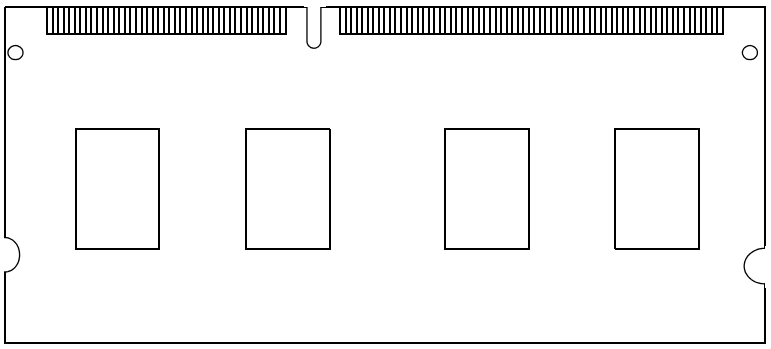
2GB, 256M x 64 SO-DIMM: HMT125S6TFR8C

Symbol	DDR3 1066	DDR3 1333	Unit	note
IDD0	600	680	mA	
IDD1	720	800	mA	
IDD2N	480	560	mA	
IDD2NT	560	640	mA	
IDD2P0	160	160	mA	
IDD2P1	400	560	mA	
IDD2Q	480	560	mA	
IDD3N	560	640	mA	
IDD3P	320	400	mA	
IDD4R	960	1120	mA	
IDD4W	960	1120	mA	
IDD5B	1320	1400	mA	
IDD6	160	160	mA	
IDD6ET	192	192	mA	
IDD6TC	192	192	mA	
IDD7	1280	1560	mA	

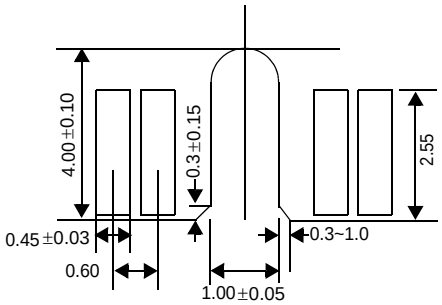
Module Dimensions

128Mx64 - HMT112S6TFR8C





Detail of Contacts A

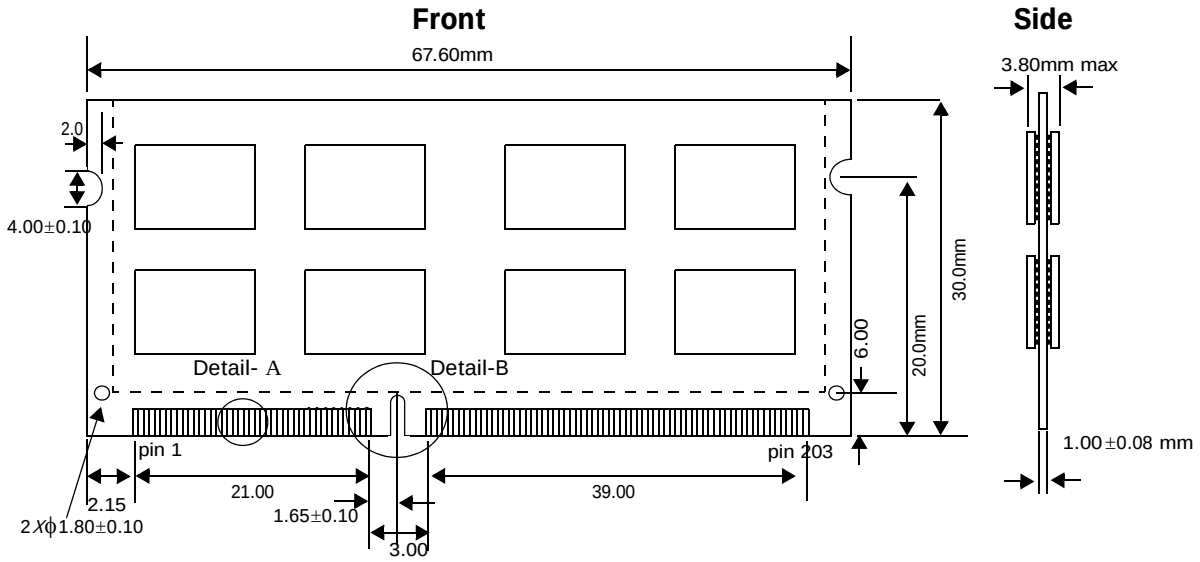


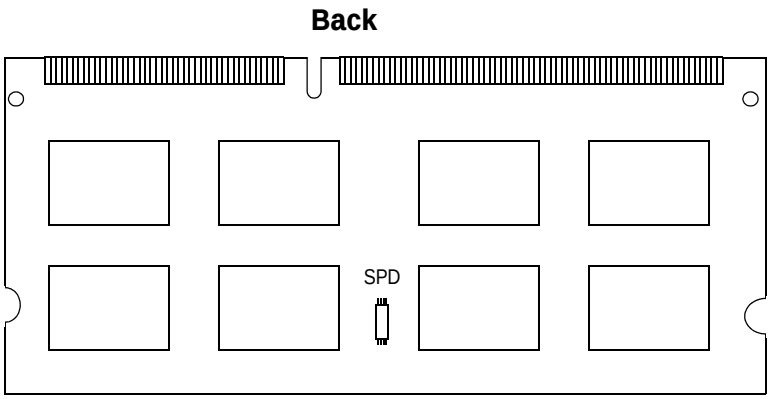
Note:

1. ±0.13 tolerance on all dimensions unless otherwise stated.

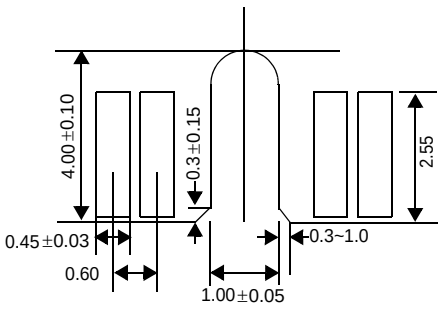
Units: millimeters

256Mx64 - HMT125S6TFR8C





Detail of Contacts A



Note:

1. ±0.13 tolerance on all dimensions unless otherwise stated.

Units: millimeters