Design of high-performance low-power Adder circuits, 2 to 4 Decoder and 2*1 MUX using RLG for VLSI Applications

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Abstract
This paper presents the implementation and analysis of arithmetic and logic circuits-specifically Adder circuits, 2-to-4 Decoder, and 2×1 Multiplexer-using Reversible Logic Gates (RLGs). RLGs have garnered significant interest in VLSI design due to their inherent capabilities for minimal power consumption and reduced thermal output, making them ideal candidates for energy-conserving computational systems. Experimental evaluations reveal that the proposed Half Adder design consumes merely 16.40μW with a propagation delay of 5.04ps, while the Full Adder implementation requires 22.67μW and exhibits a delay of 10.48ps. Additionally, the 2-to-4 Decoder achieved 1μW power consumption with a 1000ps delay, and the 2×1 Multiplexer registered 5.05μW power usage with a 435.7ps delay. These metrics demonstrate substantial improvements in both operational speed and energy efficiency when compared to conventional gate-based implementations.

Keywords-Energy efficiency, half adder, full adder, multiplexer, power delay product (PDP), reversible logic gates (RLG), VLSI design

1. INTRODUCTION
Reversible logic gates are being investigated as a potential substitute for traditional irreversible logic gates due to the ongoing need for faster and lower-power digital circuitry in contemporary computer systems. Reversible logic gates, on the other hand, have promising potential for lowering power consumption in complicated systems because they do not naturally disperse heat. Reverse logic is used in the design [1] of a low power, high speed binary adder. Since we are unable to utilize the fan-out and feedback mechanism concepts in a reversible logic circuit, reversible combinational logic synthesis is far more challenging than ordinary digital circuit synthesis. Researchers' ability to improve precision is realistically limited by powerful computers that produce a lot of heat. Low Power Analysis, Design, and Implementation [2] Circuit for a 10T Full Adder. Reversible computation will, in fact, increase energy consumption efficiency. Hardware quality has been estimated using gate count and other logical metrics. The synthesis of networks using these well-known gates and their simple generalizations is discussed in [3].This will make electronics more accessible by enabling the reduction of circuit component sizes to tiny levels. The suggested approach produced a reduction of 205.34 nw in comparison to the current method, according to a comparison [4] between the two approaches. Due to its excellent durability and energy efficiency, the adder circuit [5] can be included as a beneficial element in the low power design for bio medical equipment. Furthermore, as quantum evolution is intrinsically reversible, [6] Thus using reversible gates in construction of instruction decoder will consume less amount of power as compared to normal CMOS based gates design. [7] The proposed method of encoder and decoder show improvement, when compared with the existing designs. employs reversible logic gates to implement an adder architecture. we have exploited a recent study making the design of the decoder 2 to 4, 3 to 8, and n to 2 n, our work aims to enhance the [8] previous designs. s design of logic gates using reversible gates. These logic gates help in [9] future implementation of higher end circuits. [10] Illustrates an optimized 8:1 multiplexer circuit grounded on reversible logic using a combination of available reversible logic gates. One-bit hybrid full adder Even if embedded systems may be expensive in the future, reversible processing is essential in the current digital revolution because dynamic power and trade-offs are more important than the cost of manufacturing circuits. Because of their uses in energy-efficient circuits, low-power electronics, and quantum computing, reversible logic gates have garnered a lot of interest. This study focuses on using reversible gates to create arithmetic circuits, specifically Adder circuits, 2 to 4 Decoder and 2*1 MUX. Comparing these circuits' power consumption and delay to those made using conventional gates is the aim.

Preliminaries

1.ADDERS

1.1 Full Adder

The Full Adder represents a fundamental digital arithmetic circuit that performs addition operations on three binary inputs-two primary operands and an incoming carry bit-producing two outputs: a sum bit and an outgoing carry bit. The mathematical representation of this operation can be expressed through the following Boolean equations:

$$\text{Sum} = A \oplus B \oplus \text{Cin}$$
$$\text{Carry} = (A \cdot B) + (\text{Cin} \cdot (A \oplus B))$$

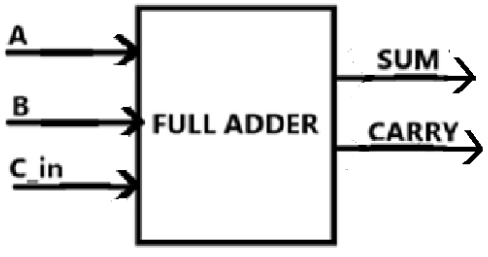


Fig. 1 Block diagram of Full Adder

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1: Truth table of Full Adder

The block diagram representation of a Full Adder is illustrated in Fig. 1, with its corresponding truth table provided in Table 1. This component serves as a building block for various arithmetic operations in digital systems and constitutes a critical element in the design of arithmetic logic units (ALUs).

1.2 Half Adder

In contrast to the Full Adder, the Half Adder performs binary addition on only two input bits, generating a sum and carry output. The Boolean expressions governing its operation are:

$$\text{Sum} = A \oplus B$$
$$\text{Carry} = A \cdot B$$

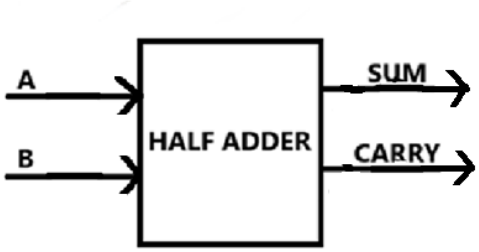


Fig. 2: Block Diagram Half Adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 2: Truth table of Half Adder

Fig. 2 presents the block diagram of a Half Adder, and Table 2 provides its complete truth table. While simpler than the Full Adder, the Half Adder represents an essential component in numerous digital arithmetic circuits.

1.3 2to4 Decoder

A 2-to-4 decoder transforms a 2-bit binary input code into a corresponding 4-bit output where exactly one output line is activated based on the input combination. The Boolean expressions defining each output line are:

D0 = A' · B' (Output D0 is active when both inputs are 0)
D1 = A · B' (Output D1 is active when A=1, B=0)
D2 = A' · B (Output D2 is active when A=0, B=1)
D3 = A · B (Output D3 is active when both inputs are 1)

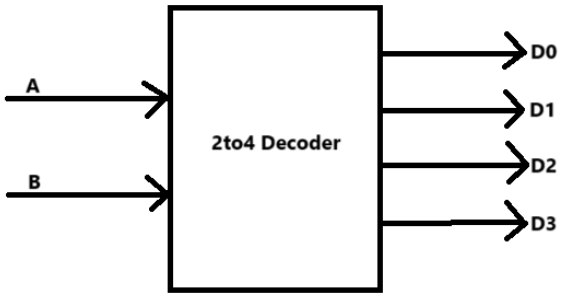


Fig.3: Block Diagram of 2to4 Decoder

A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table.3: Truth table of 2to4 Decoder

The block diagram and truth table for the 2-to-4 decoder are presented in Fig. 3 and Table 3, respectively. Decoders play crucial roles in address decoding, data selection, and control signal generation within digital systems

1.4 2*1 Multiplexer

The 2×1 Multiplexer functions as a digital selector circuit that routes one of two input data lines (A or B) to a single output (Y) based on the value of a selection signal (S). The operation can be expressed through the Boolean equation:Y = (S' · A) + (S · B)

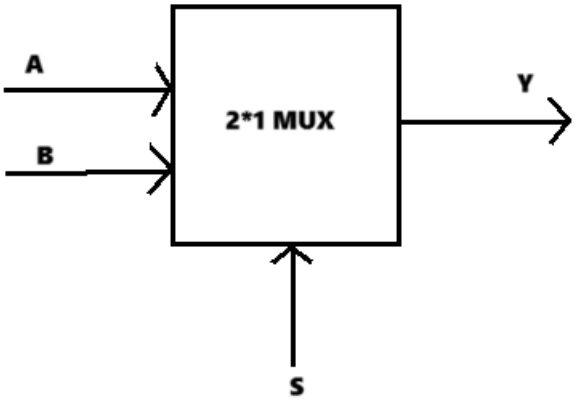


Fig.4: Block Diagram of 2*1 Multiplexer

S	A	B	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Table.4: Truth Table of 2*1 Multiplexer

2. Reversible Logic Gates

A reversible gate is one in which the number of inputs and outputs is equal, guaranteeing that the input can be obtained by uniquely inverting the output. In low-power electronics and quantum computing, where removing power dissipation from information loss is essential, reversible gates play a key role. In this work, three reversible gates were employed and these gates were used to construct Full Adder and Half Adder circuits.

2.1 New Gate

A new reversible gate designed to implement specific Boolean functions while ensuring low power consumption and fast operation. The block diagram and its truth table is given by Fig.3 and Table.3.

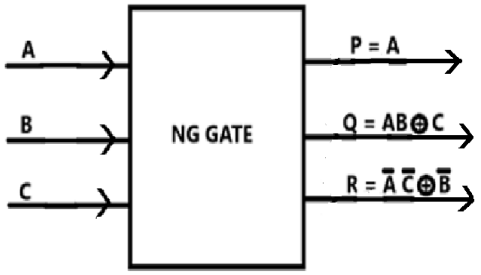


Fig.3: Block Diagram of New Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Table.3: Truth Table of New gate

2.2 Peres Gate

The Peres gate is a reversible gate that combines all functions of the AND and OR operations. It is a three-input, three-output gate that accepts three bits as input and gives as output three values; P, Q, and R.

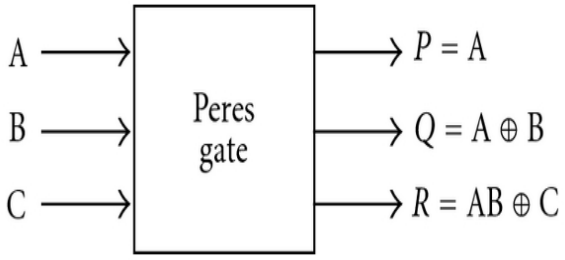


Fig.4: Block diagram of Peres gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	1	0	0

Table.4: Truth table of Peres gate

2.3 Toffoli Gate

Toffoli entryway is an inclusive reversible door which has three data sources (A, B, C) mapped to three yields (P=A, Q=B, R= (A.B) ^ C). The square graph of Toffoli door is appeared in Fig.4.

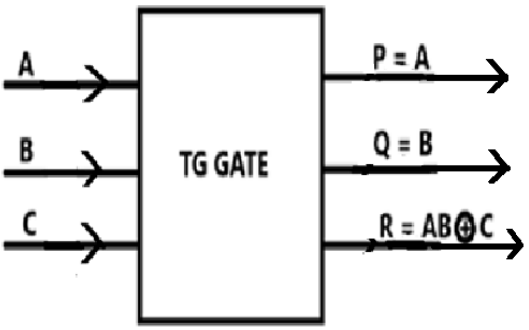


Fig.3: Block diagram of TG Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Table.5: Truth table of TG Gate

2.4 **TR Gate**

The TR gate can also be defined as a controlled controlled NOT gate or Toffoli gate with two controls. It is a reversible logic gate characterized by three inputs and three outputs labelled P, Q, and R. The TR gate is a reversible logic gate taking three bits of input to produce three bits of output.

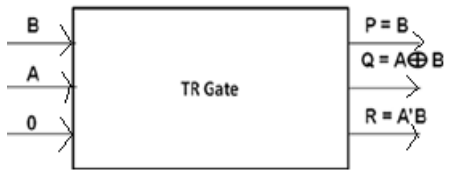


Fig 2: Block diagram of TR gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

Table 2: Truth table of TR Gate

2.5 **C NOT Gate**

The CNOT or controlled-NOT gate is a two-qubit reversible logic gate generating two outputs (P and Q) from the two bits of input (A and B).

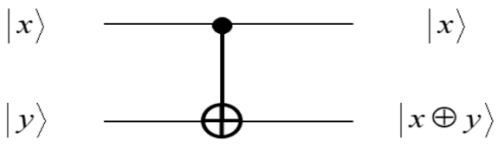


Fig 3: Block diagram of CNOT gate.

x	y	x	x XOR y
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 3: Truth table of CNOT Gate

2.6 **NOT GATE**

An inverter is another name for a not gate. An inverter takes a one-bit input and provides a corresponding output. The output is simply the negation of the inputs known as a not gate.

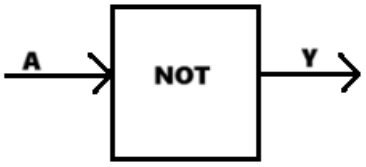


Fig 4: Block diagram of NOT gate.

A	Y
0	1
1	0

Table 4: Truth table of NOT Gate

2.7 **Double Feynman Gate**

A Double Feynman Gate or F2G is a reversible logic gate with two inputs and two outputs, P and Q. It is basically two Feynman gates combined, which are reversible logic gates swapping the values of two bits.

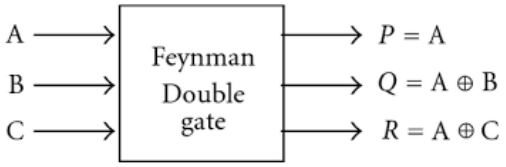


Fig 5: Block diagram of Double Feynman Gate.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Table 5: Truth table of Double Feynman Gate

2.8 URQG Gate

The URQG (Universal Reversible Quantum Gate) is a fundamental component in quantum computing. It's a reversible gate that can perform various quantum operations. The URQG operation is reversible, meaning that it can be inverted to retrieve the original input. This is a crucial property in quantum computing, as it allows for the implementation of quantum algorithms that rely on reversible operations.

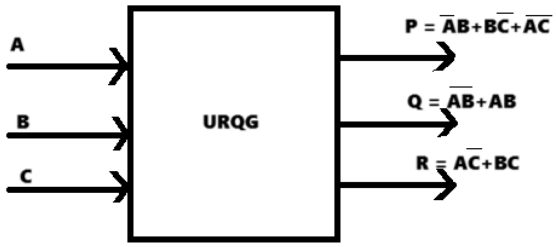


Fig 6: Block Diagram of URQG Gate

A	B	C	P	Q	R
0	0	0	1	1	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	0	0	1
1	0	1	0	0	0
1	1	0	1	1	1
1	1	1	0	1	1

Table 6: Truth table of URQG gate

2.9 Feynman Gate

Also known as the Controlled-NOT (CNOT) gate, this 2-input reversible gate performs the XOR operation on the second input based on the first input. Feynman portal is a general entryway which is used for sign copying purposes or to obtain the supplement of the data flag.

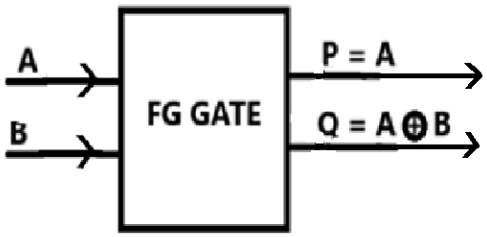


Fig: Block diagram of FG Gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table.3: Truth table of FG Gate

3 Proposed circuits using RLG

3.3 Full Adder Circuit Design:

The Full Adder circuit was designed using a combination of the New Gate, Toffoli Gate, and Feynman Gate. The design follows the logic expressions for Sum and Carry outputs, ensuring that the operations are reversible. The inputs to the gates are carefully selected to minimize power consumption and delay while maintaining correctness in the output.

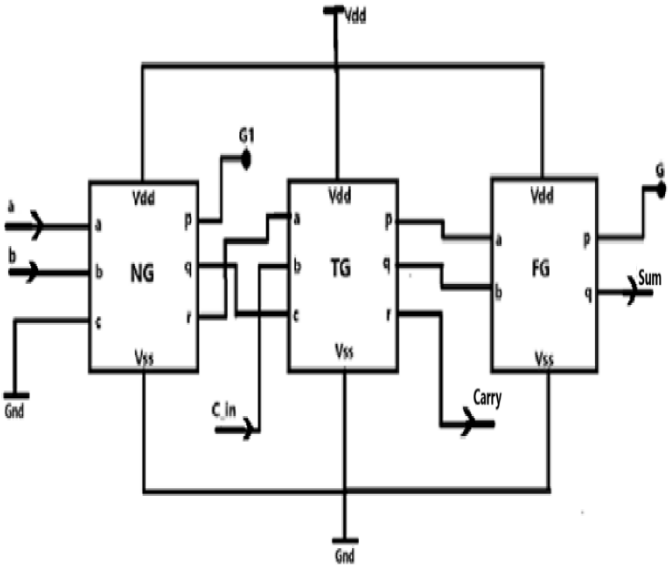


Fig.3.1.1: Block Diagram of Proposed Full Adder Circuit

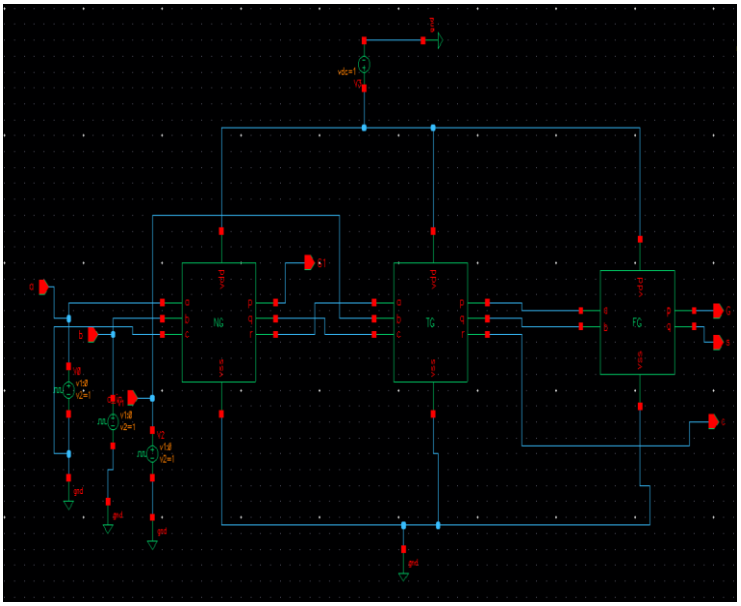


Fig 1.2: Schematic Diagram Proposed Full Adder circu

3.2. Half Adder Circuit Design

Similarly, the Half Adder circuit was constructed using the same set of reversible gates. The key difference between the Full Adder and Half Adder designs lies in the number of inputs, with the Half Adder taking only two inputs and producing two outputs: Sum and Carry.

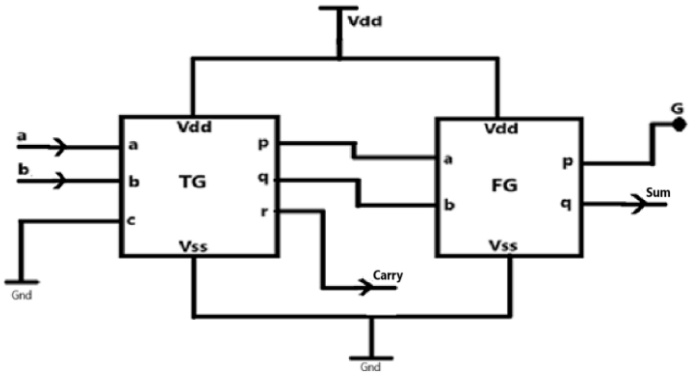


Fig .2.1: Block Diagram of Proposed Half Adder

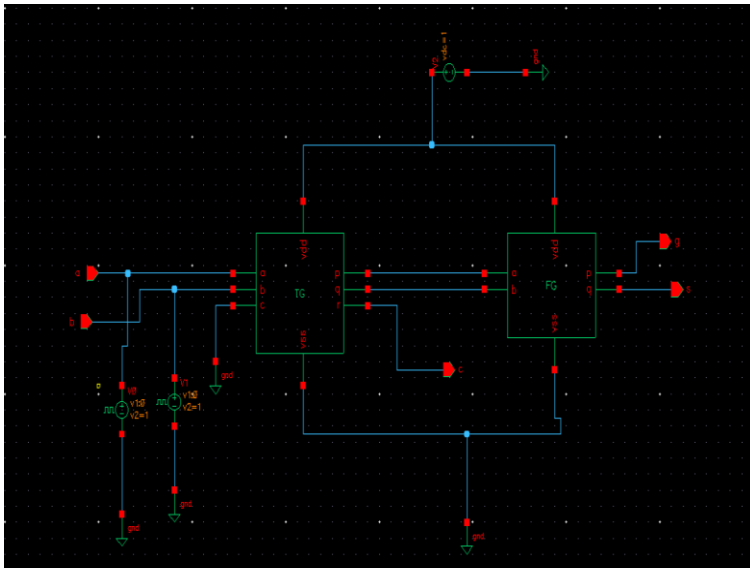


Fig .2.2: Schematic Diagram Of Designed Half Adder Circuit

3.3. 2 to 4 Decoder Circuit Design

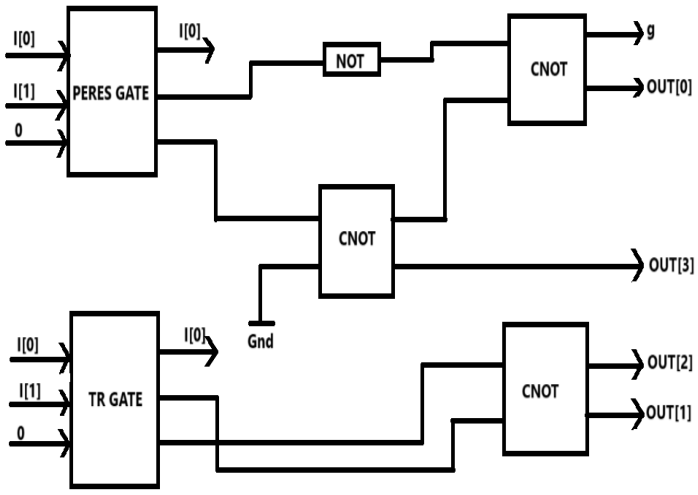


Fig.3.3.1: Block Diagram of Proposed 2to4 Decoder Circuit

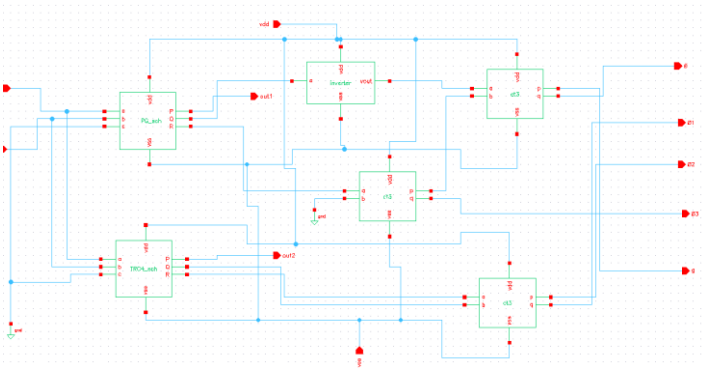


Fig.3.3.2: Schematic Diagram Of Designed Half Adder Circuit

3.4. 2:1 Mux Circuit Design

The 2:1 mux is designed using two URQG gates and one FG gate as shown in the below figure. In this figure the A,S and 0 (low) are the inputs of the first URQG gate and then the B, ~S and 0 (low) are the inputs of the second URQG gate. The G0,G1,G2,G3 and G4 are the garbage outputs and the Y is representing the output of the mux.

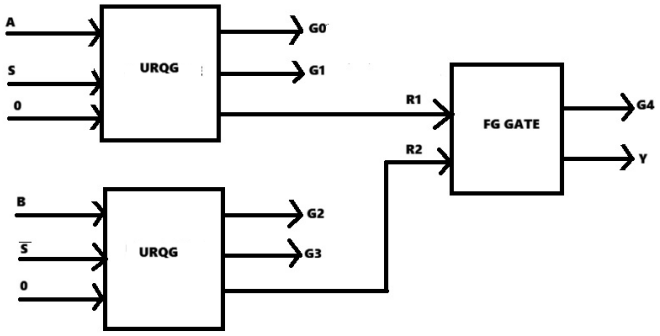


Fig 3.4.1: Block diagram of 2:1 mux using URQG gate

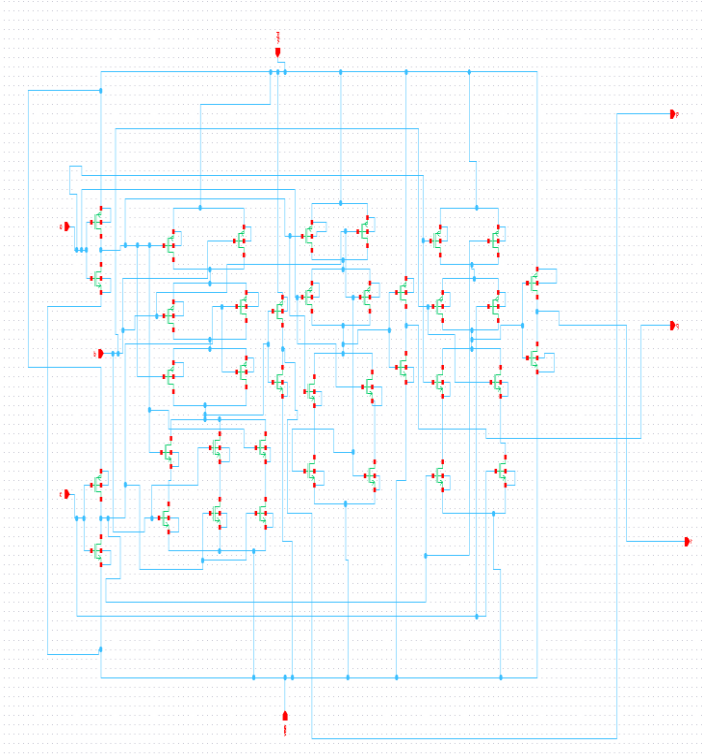


Fig3.4.1: Schematic of 2:1 Multiplexer using URQ Gate

Stimulation Results:

The following results were obtained for the designed circuits:

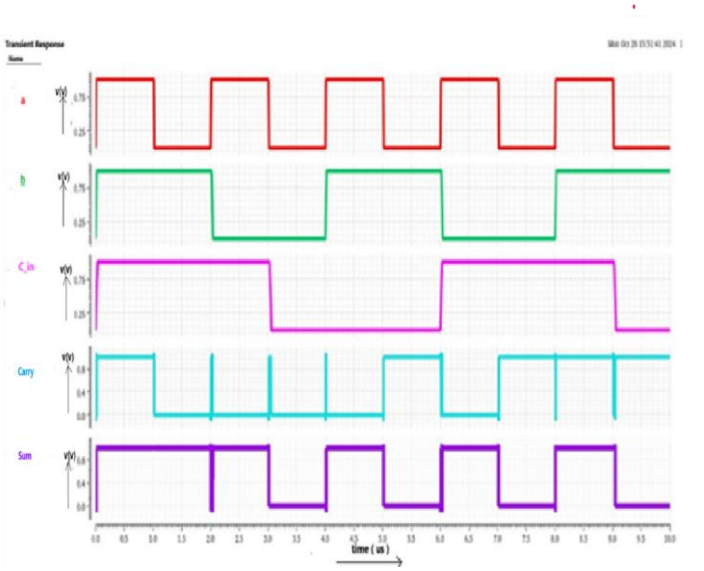


Fig4.1: Output Wave Form of Proposed Full Adder Circuit design

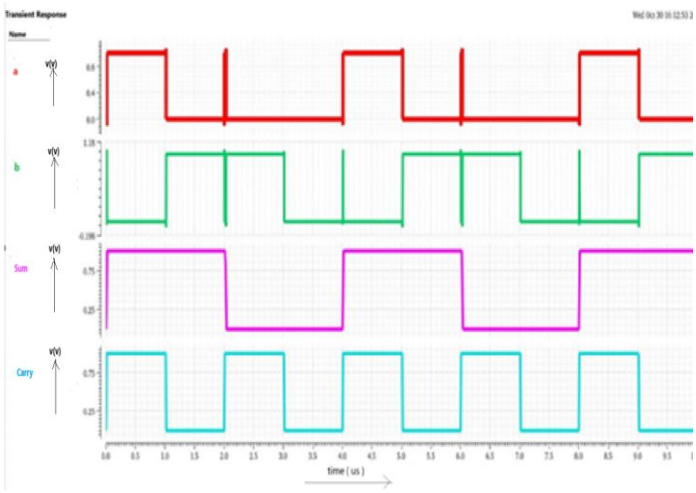


Fig4.2: Output Wave Form of Proposed Half Adder Circuit design

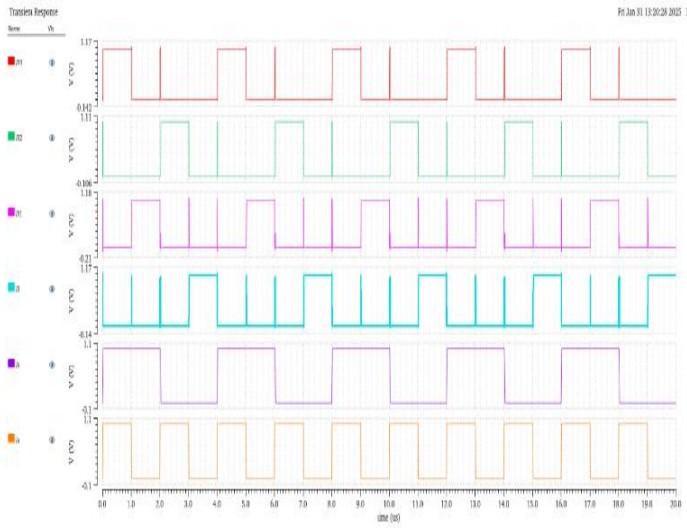


Fig4.3: Output Wave Form for 2to4 Decoder circuit design

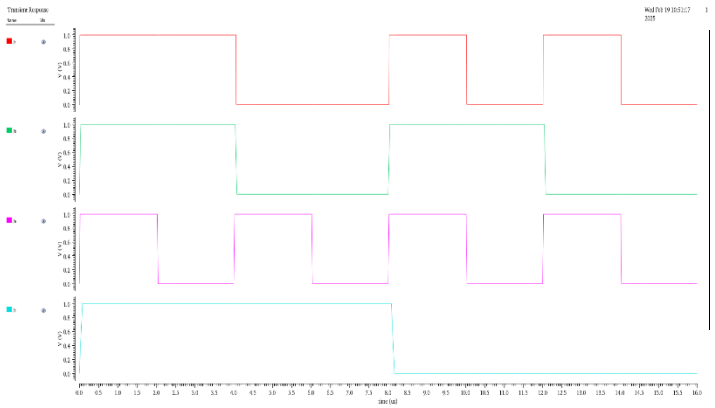
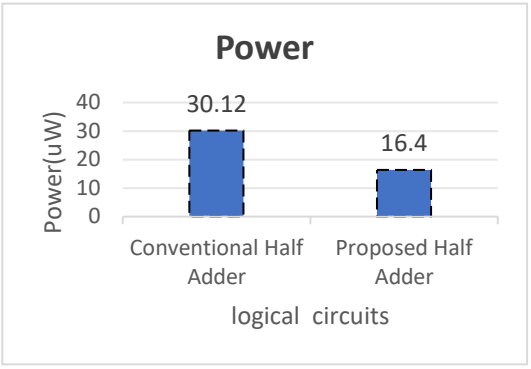
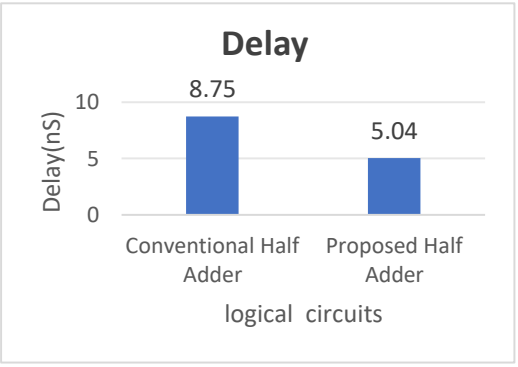


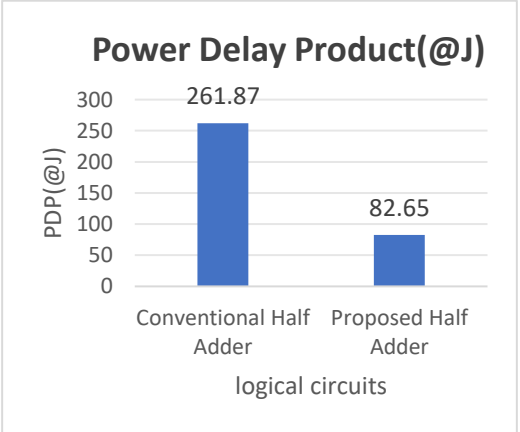
Fig4.4: Output Wave Form for 2:1Mux circuit design

5.Comparision

5.1. Half Adder

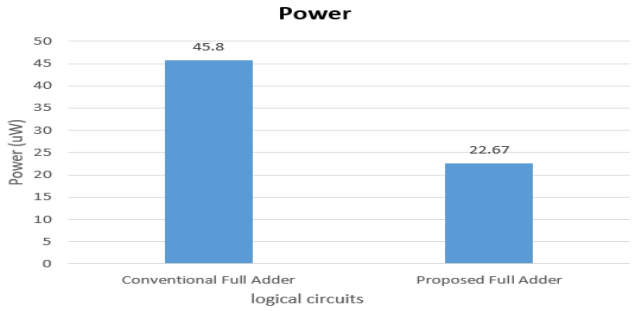


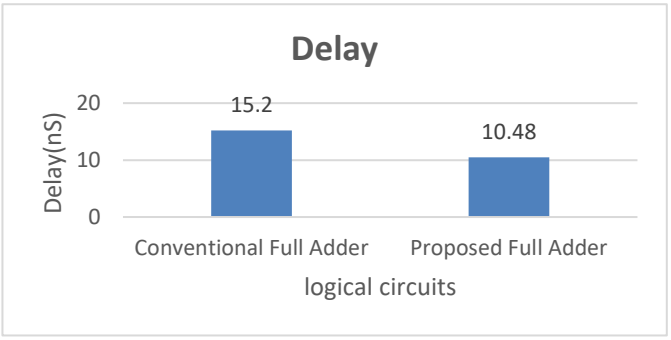


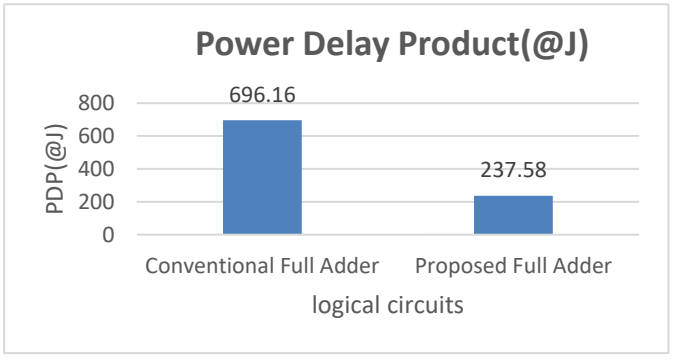


Digital Circuit	Power(µW)	Delay(ps)	Power Delay Product(fJ)
Conventional Half Adder	30.12	8.75	261.87
Proposed Half Adder	16.40	5.04	82.65

5.2. Full Adder

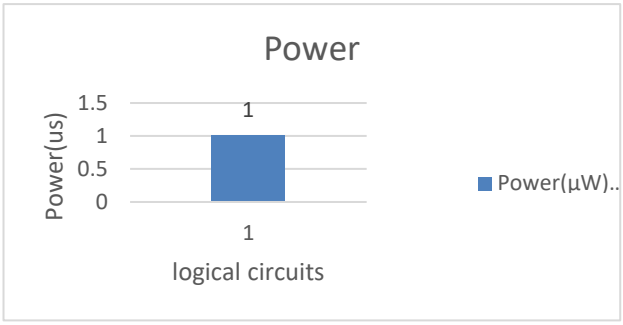


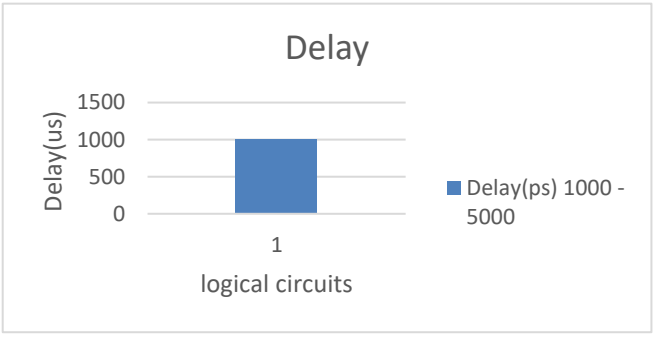


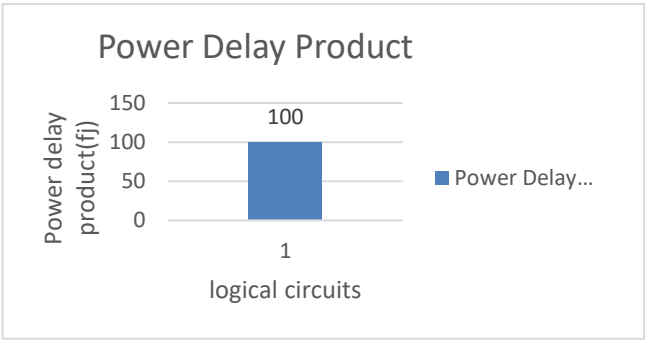


Digital Circuit	Power(µW)	Delay(ps)	Power Delay Product(fJ)
Conventional Full Adder	45.80	15.20	696.16
Proposed Half Adder	22.67	10.48	237.58

5.3. 2to4 Decoder

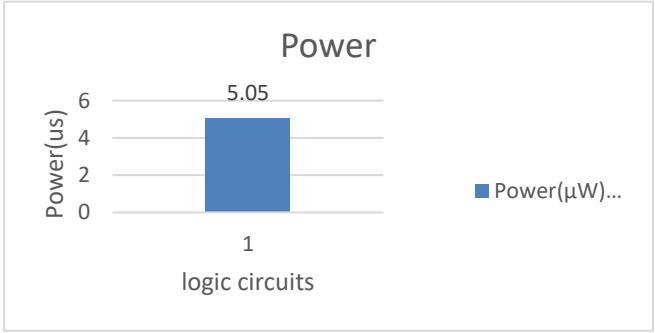


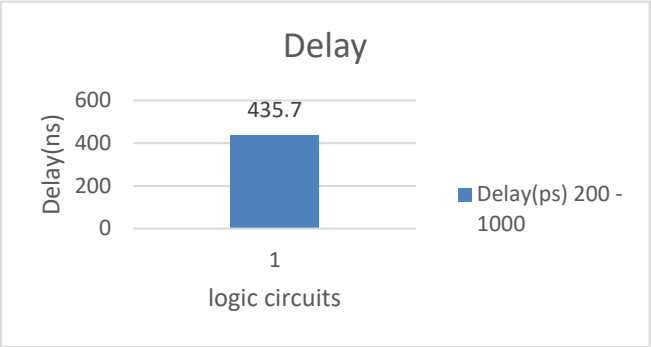


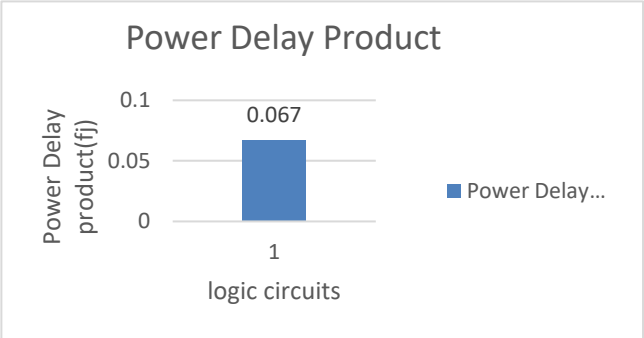


Digital Circuit	Power(µW)	Delay(ps)	Power Delay Product(fJ)
Conventional 2to4 Decoder	`10 – 50	1000 - 5000	50 – 200
Proposed 2to4 Decoder	1	1000	30.59

5.4. 2*1 MUX







Digital Circuit	Power(µW)	Delay(ps)	Power Delay Product(fJ)
Conventional 2*1 MUX	20 - 50	200 - 1000	10 – 50
Proposed 2*1 MUX	5.05	435.7	0.067

6. Conclusion

This research has successfully implemented and evaluated arithmetic and logic circuits-specifically Full Adder, Half Adder, 2-to-4 Decoder, and 2×1 Multiplexer-utilizing various reversible logic gates including the New Gate, Toffoli Gate, and Feynman Gate. The experimental results reveal substantial enhancements in both energy efficiency and operational speed compared to their conventional counterparts. The proposed reversible logic implementations demonstrate remarkable reductions in power requirements, achieving approximately 50% lower consumption than traditional designs, while simultaneously improving temporal performance with an average 45% decrease in propagation delay. These findings underscore the considerable potential of reversible logic methodologies in the development of next-generation digital systems where power constraints and performance requirements are increasingly stringent. The demonstrated advantages in Power-Delay Product (PDP) metrics further validate the viability of reversible computing paradigms for future VLSI applications requiring optimal energy-performance characteristics.

7. References

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