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<div>NOTES: UNLESS OTHERWISE SPECIFIED</div> <div>1. SPECIFICATIONS/TOLERANCES:<div>A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES<div>B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.</div>C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.<div>D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.</div>E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.</div>F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.</div> <div>2 DIELECTRIC MATERIAL:<div>A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS).</div>B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF .076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.</div> C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK. <div>3. DRILLING:<div>A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+-.0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.</div>B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.</div> <div>4. SOLDER MASK:<div>A. APPLY LPI SOLDER MASK USING PROVIDED DATA.</div>B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLUE.</div> C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED. <div>5. MARKING:<div>A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.</div>B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.</div> C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE. <div>6. ELECTRICAL TEST:<div>A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.</div>B. ALL PCBS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.</div> C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT. <div>7 FINAL FINISH:<div>A. FINAL FINISH ON ALL EXPOSED CONDUCTORS SHALL BE IMMERSION SILVER PER IPC-4553, .15 - .38 MICROMETERS [6 - 15 MICROINCHES] THICK.</div></div> <div>8. IMPEDANCE:<div>A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.</div>B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.</div> <div>9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBS SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.</div>																		REVISIONS														
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																		AHUY-21		1.0	03/07/19		INITIAL RELEASE				YJUN		MILI		MILI	
																		MILI68		2.0	06/03/19		DESIGN UPDATE				YJUN		MILI		MILI	
																		MILI76		3.0	08/08/19		DESIGN UPDATE				ISJP		MILI		MILI	
MILI81		4.0	02/11/20		DESIGN UPDATE				ISJP		MILI		MILI																			
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