Laboratory Report #1

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Laboratory Exercise Title: Half Adder Circuit

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 1C:

The synthesis of a half adder circuit was performed in this exercise with the use of the Intel® Quartus® Prime Lite Edition software.

Figure 1. Half Adder Circuit Entity Diagram

The basic function of a half adder circuit is to take the binary sum of two single-bit inputs to produce a sum and carry output (Figure 1). The inputs and outputs used in this exercise are further shown in Table 1.

Table 1. Half Adder Circuit I/O

I/O	Variable	Description
Inputs	x	First single-bit input
	y	Second single-bit input
Outputs	C	Carry
	S	Sum

In single-bit binary addition, the sum is 0 if both inputs are 0, the sum is 1 with a 0 carry out if only one input has the value of 1, and lastly if both inputs are equal to 1, then the sum is 0 with a carry out

value of 1. By indicating all possible sum and carry outcomes of the single-bit binary addition of inputs x and y, the truth table may be formulated likewise:

Table 2. Half Adder Circuit Truth Table

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

By taking the sum of products for the C and S outputs (Table 3), the corresponding logic circuit for the half adder may be constructed (Figure 2).

Table 3. Half Adder Circuit Sum of Products

Output	SOP
C	$xy = x\ AND\ y$
S	$x'y + xy' = x \oplus y = x\ XOR\ y$

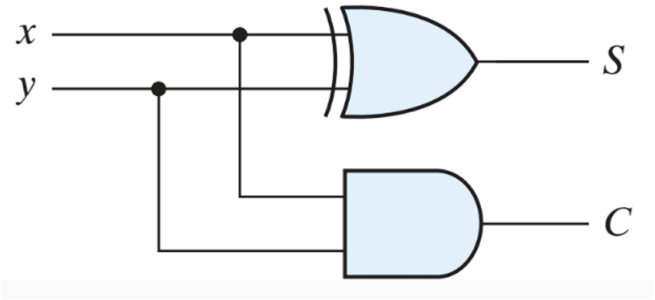

Figure 2. Half Adder Circuit Logic Diagram

Exercise Screenshots:

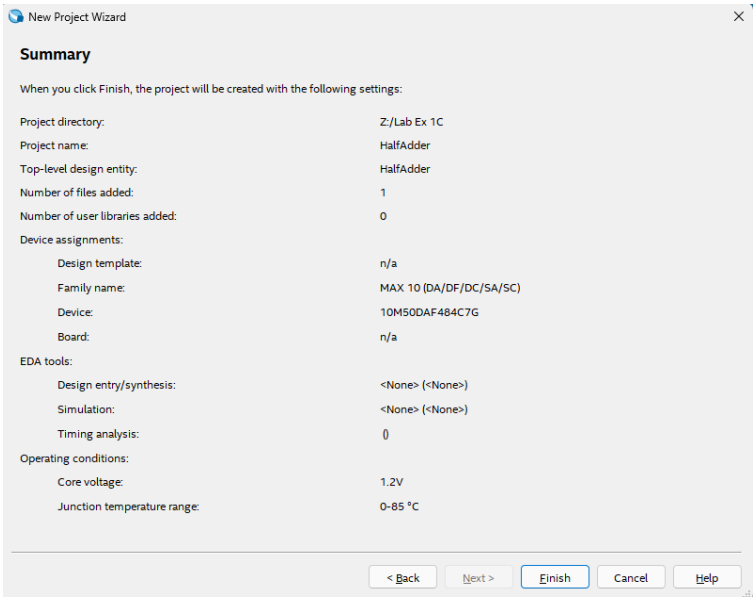

Figure 3. Project Settings Summary

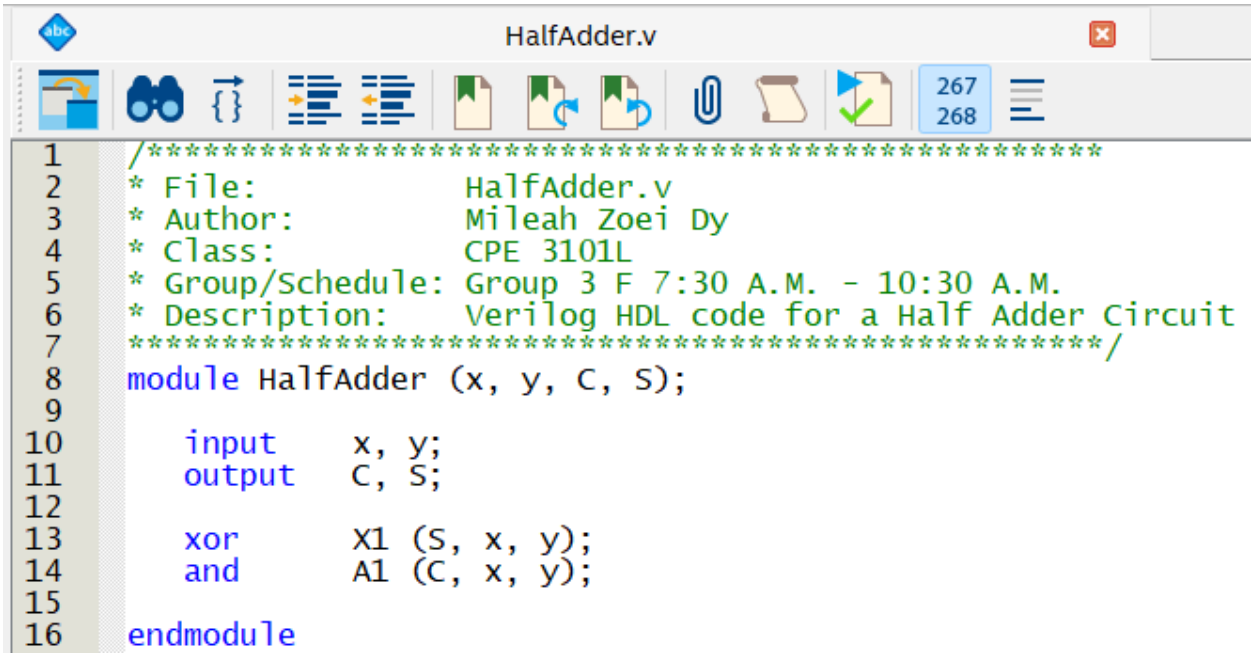

Figure 4. Verilog HDL Design Entry

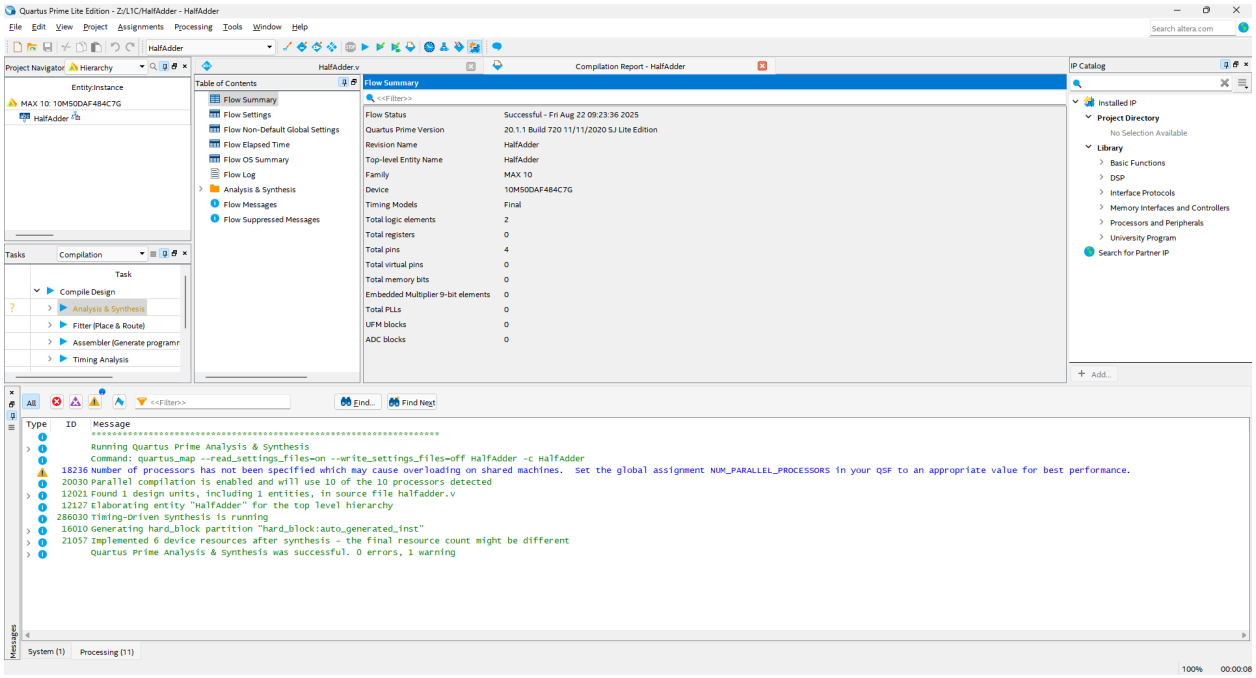

Figure 5. Flow Summary

- Total logic elements used: 2
- Total pins used: 4

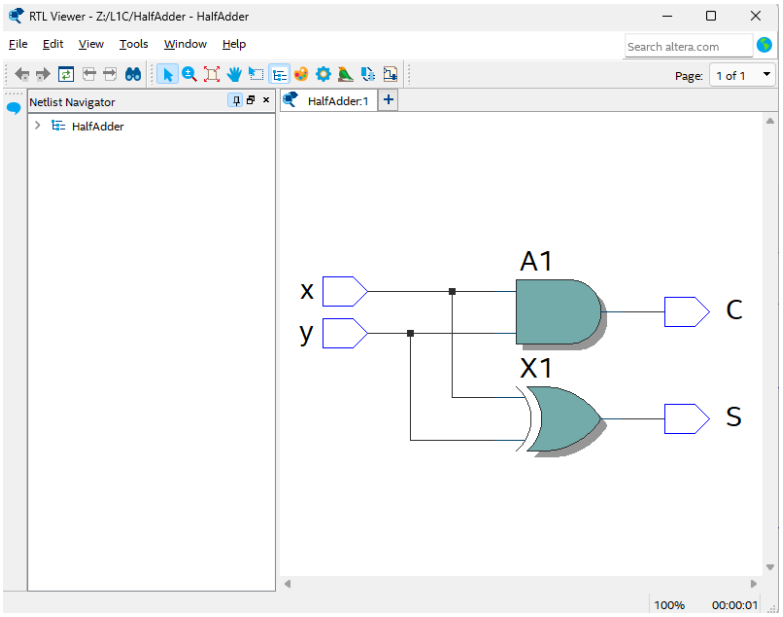

Figure 6. Schematic Diagram of Synthesized Circuit using RTL Viewer