Laboratory Report # 6-2

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Laboratory Exercise Title: Behavioral Modeling of Sequential Circuits

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 6C: Clock Divider

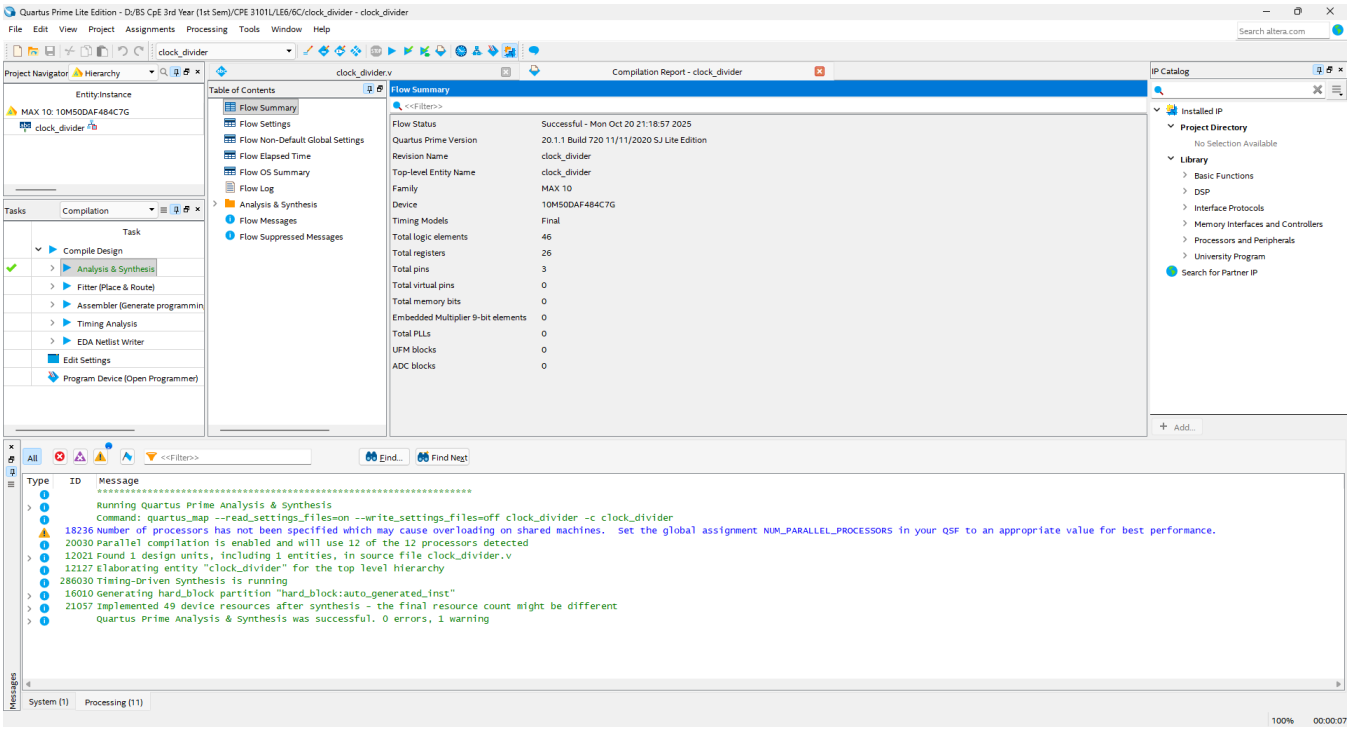


Figure 1. Design Synthesis Result of Clock Divider

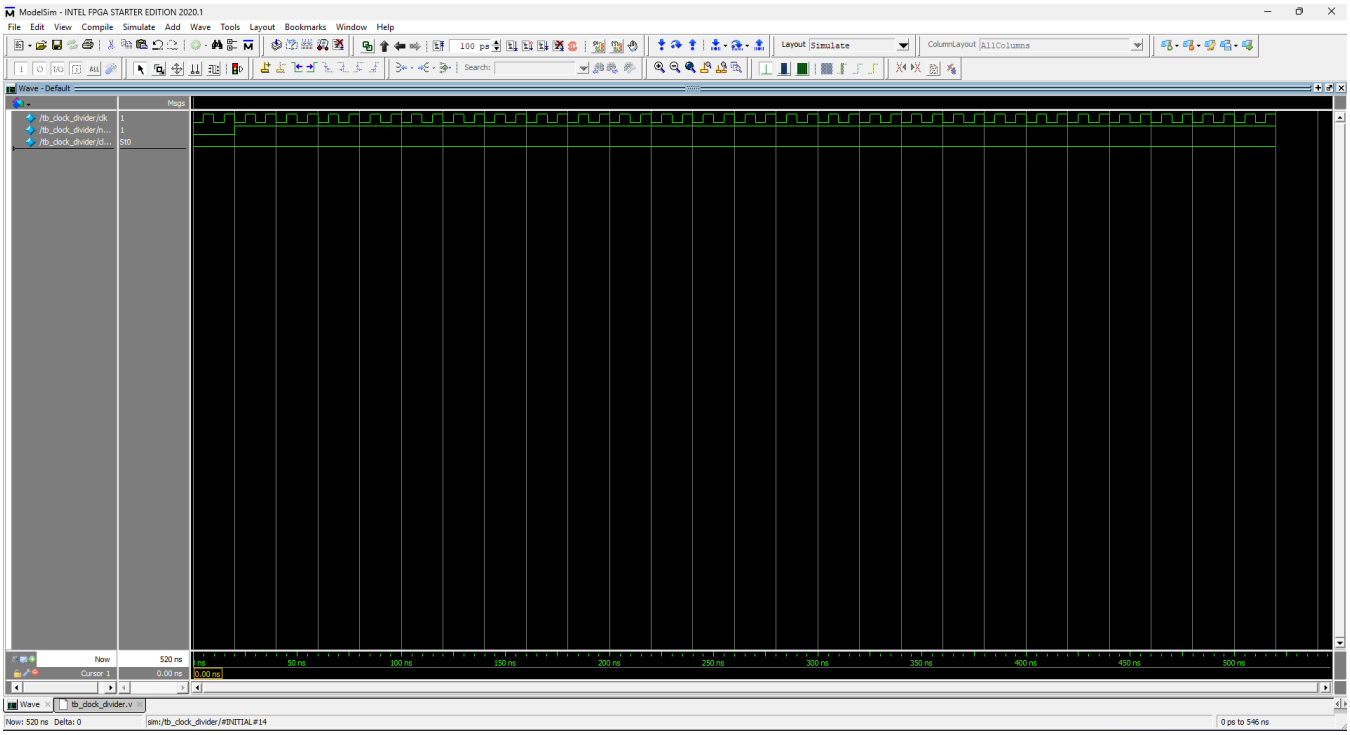


Figure 2. Simulation Results of Clock Divider

Exercise 6D: Hexadecimal Digit Counter

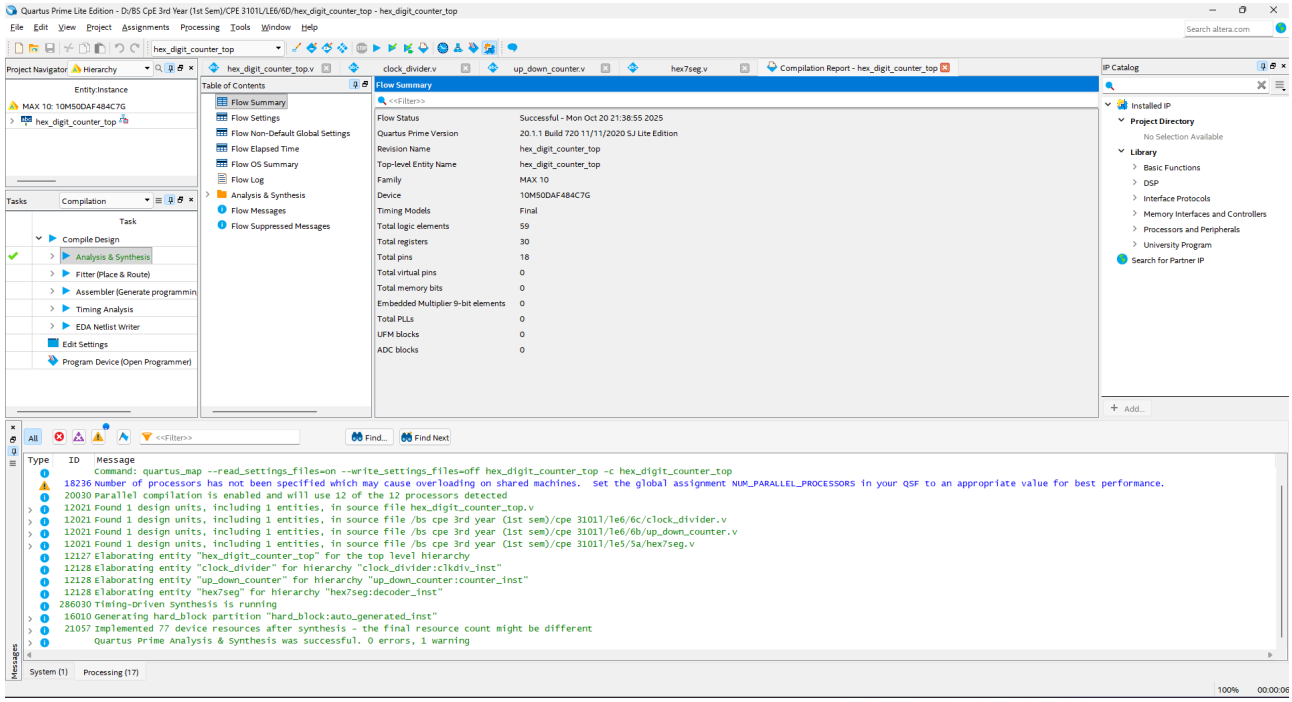


Figure 3. Design Synthesis Result of Hexadecimal Digit Counter

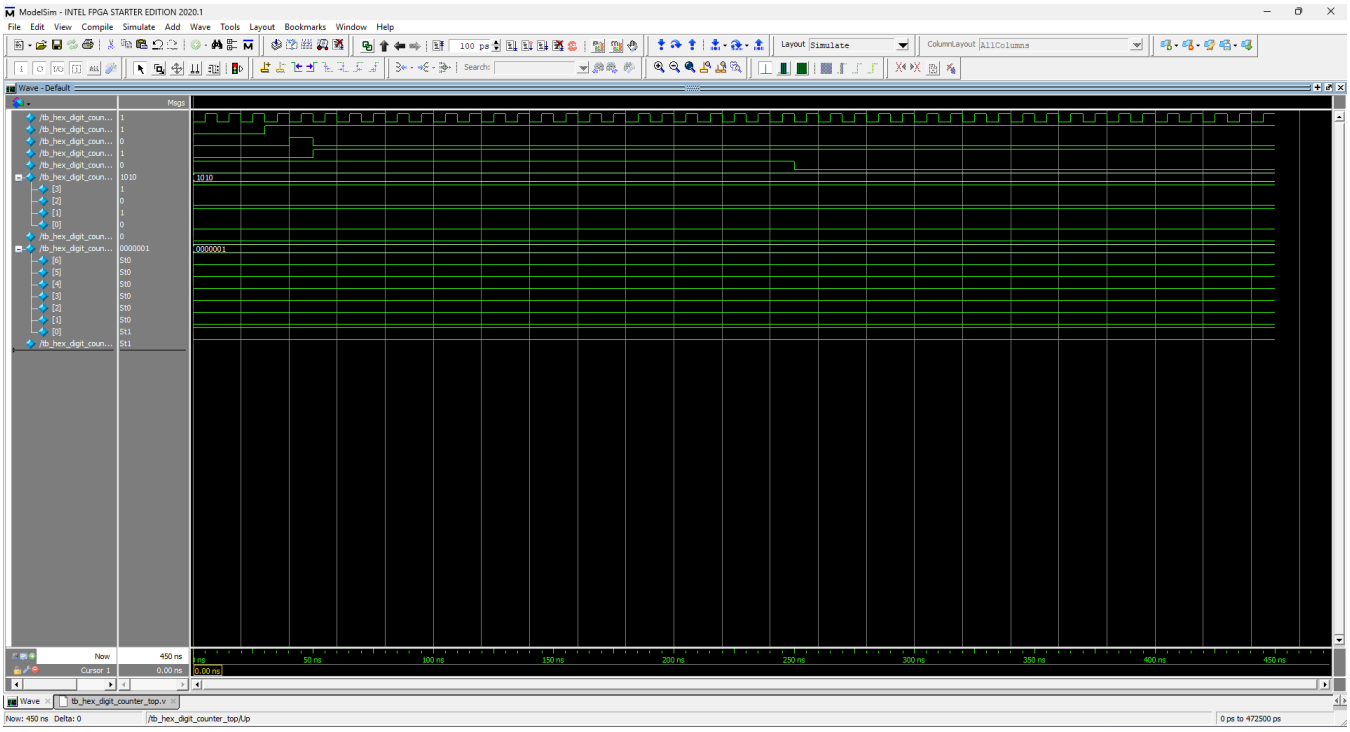
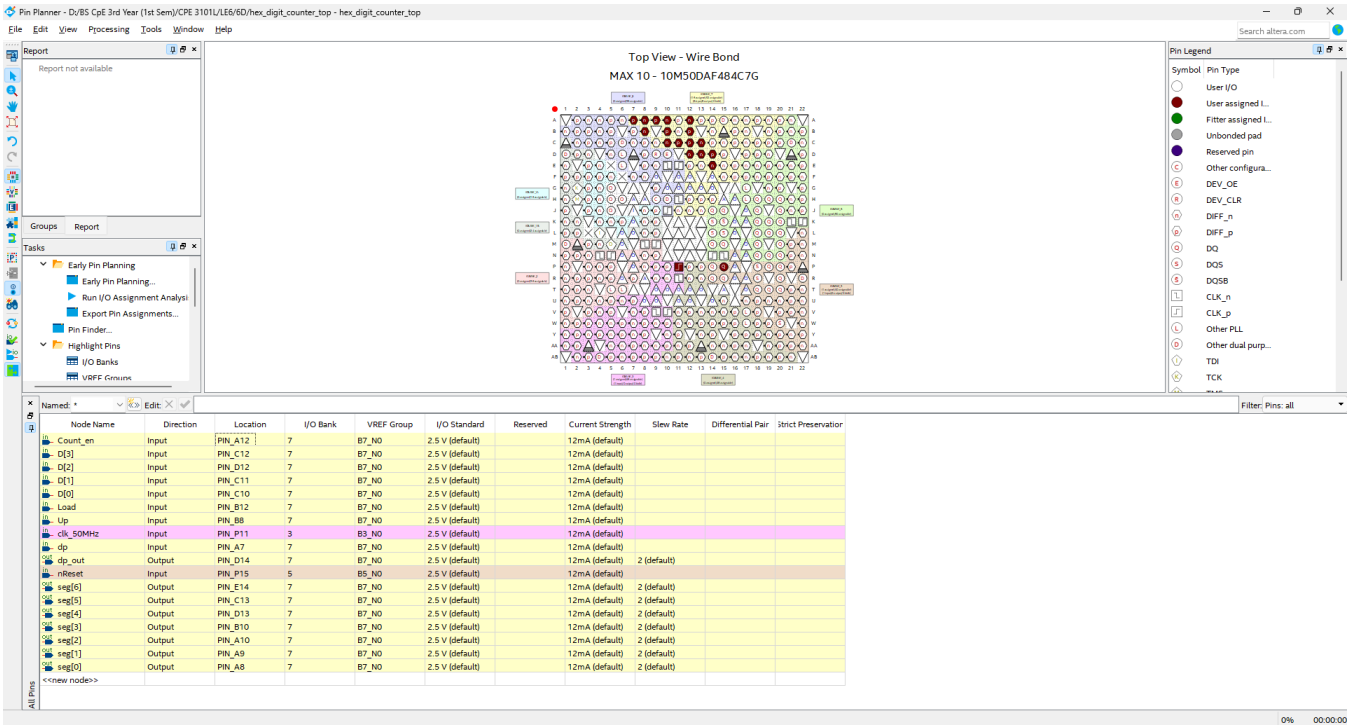


Figure 4. Simulation Results of Hexadecimal Digit Counter



Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservation
Count_en	Input	PIN_A12	7	B7_N0	2.5 V (default)		12mA (default)			
D[3]	Input	PIN_C12	7	B7_N0	2.5 V (default)		12mA (default)			
D[2]	Input	PIN_D12	7	B7_N0	2.5 V (default)		12mA (default)			
D[1]	Input	PIN_C11	7	B7_N0	2.5 V (default)		12mA (default)			
D[0]	Input	PIN_C10	7	B7_N0	2.5 V (default)		12mA (default)			
Load	Input	PIN_B12	7	B7_N0	2.5 V (default)		12mA (default)			
Up	Input	PIN_B8	7	B7_N0	2.5 V (default)		12mA (default)			
clk_50MHz	Input	PIN_P11	3	B3_N0	2.5 V (default)		12mA (default)			
dp	Input	PIN_A7	7	B7_N0	2.5 V (default)		12mA (default)			
dp_out	Output	PIN_D14	7	B7_N0	2.5 V (default)		12mA (default)	2 (default)		
nReset	Input	PIN_P15	5	B5_N0	2.5 V (default)		12mA (default)			
seg[6]	Output	PIN_E14	7	B7_N0	2.5 V (default)		12mA (default)	2 (default)		
seg[5]	Output	PIN_C13	7	B7_N0	2.5 V (default)		12mA (default)	2 (default)		
seg[4]	Output	PIN_D13	7	B7_N0	2.5 V (default)		12mA (default)	2 (default)		
seg[3]	Output	PIN_B10	7	B7_N0	2.5 V (default)		12mA (default)	2 (default)		
seg[2]	Output	PIN_A10	7	B7_N0	2.5 V (default)		12mA (default)	2 (default)		
seg[1]	Output	PIN_A9	7	B7_N0	2.5 V (default)		12mA (default)	2 (default)		
seg[0]	Output	PIN_A8	7	B7_N0	2.5 V (default)		12mA (default)	2 (default)		
<<new node>>										

Figure 5. Pin Assignments of Hexadecimal Digit Counter

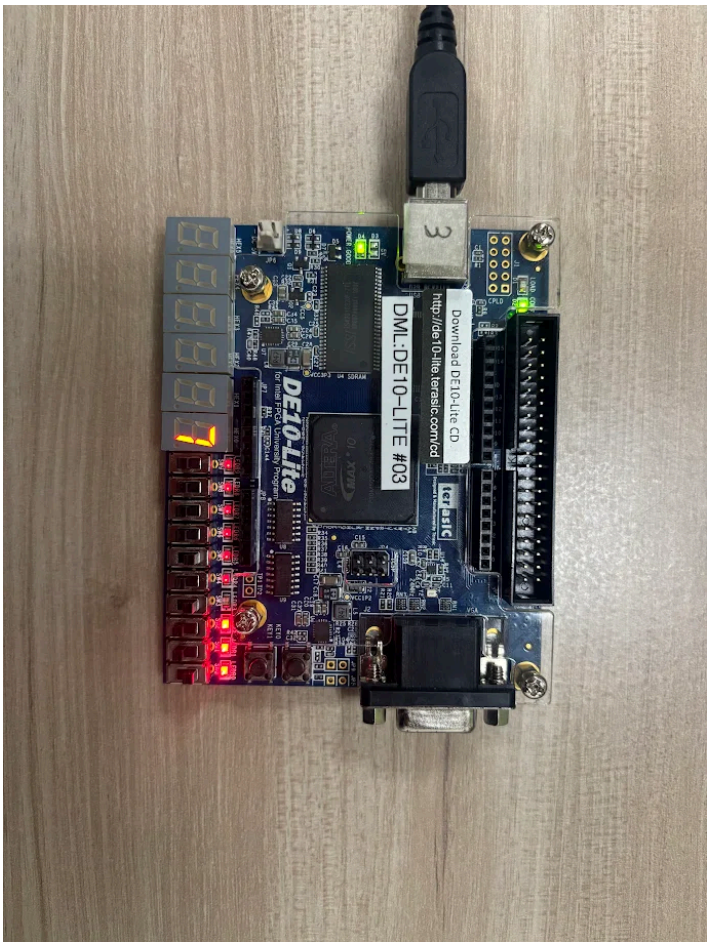


Figure 6. FPGA Implementation of Hexadecimal Digit Counter