Laboratory Report # 1

Name: Lauron, John Enrico D. **Date Completed:** August 22, 2025

Laboratory Exercise Title: Design Flow of Digital Systems

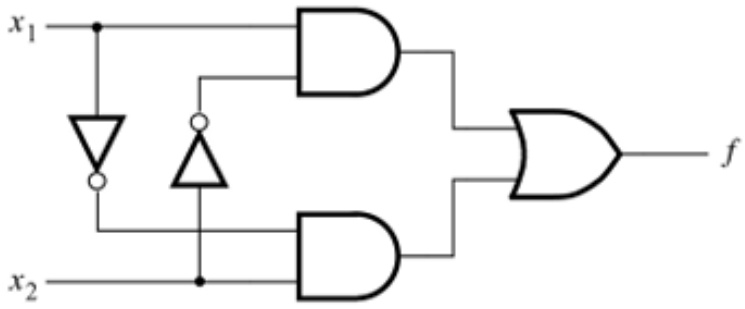
Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

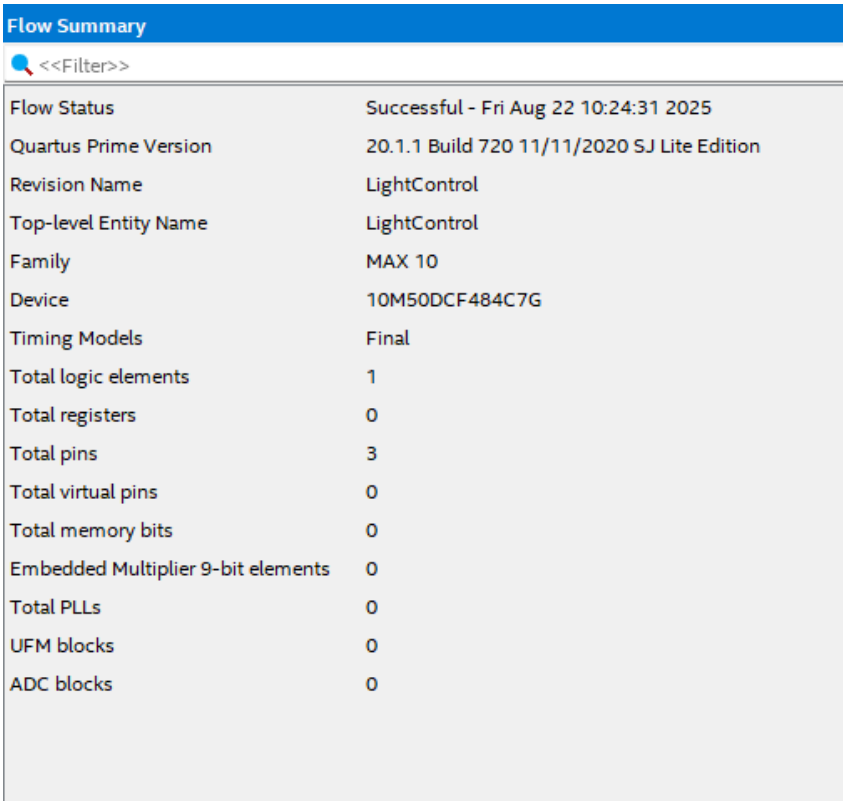
Exercise 1B: Design Entry and Synthesis with Verilog HDL

In this exercise, we were able to design a two-way light controller circuit by using Verilog HDL in Quartus Prime Lite.



x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	0

Figure 1. Two-Way Light Controller and Truth Table

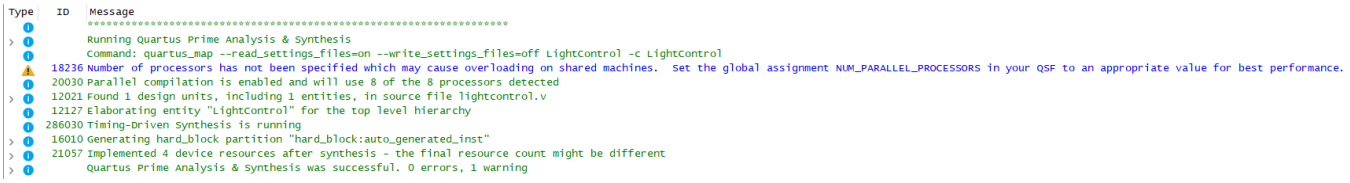


Flow Summary

<<Filter>>

Flow Status	Successful - Fri Aug 22 10:24:31 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	LightControl
Top-level Entity Name	LightControl
Family	MAX 10
Device	10M50DCF484C7G
Timing Models	Final
Total logic elements	1
Total registers	0
Total pins	3
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0

Figure 2. Flow Summary of Light Control



Type	ID	Message
		**********
		Running Quartus Prime Analysis & Synthesis
		Command: quartus_map --read_settings_files=on --write_settings_files=off LightControl -c LightControl
⚠	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
	20030	Parallel compilation is enabled and will use 8 of the 8 processors detected
	12021	Found 1 design units, including 1 entities, in source file lightcontrol.v
	12127	Elaborating entity "LightControl" for the top level hierarchy
	286030	Timing-Driven Synthesis is running
	16010	Generating hard_block partition "hard_block:auto_generated_inst"
	21057	Implemented 4 device resources after synthesis - the final resource count might be different
		Quartus Prime Analysis & Synthesis was successful. 0 errors, 1 warning

Figure 3. Synthesis Results of Light Control

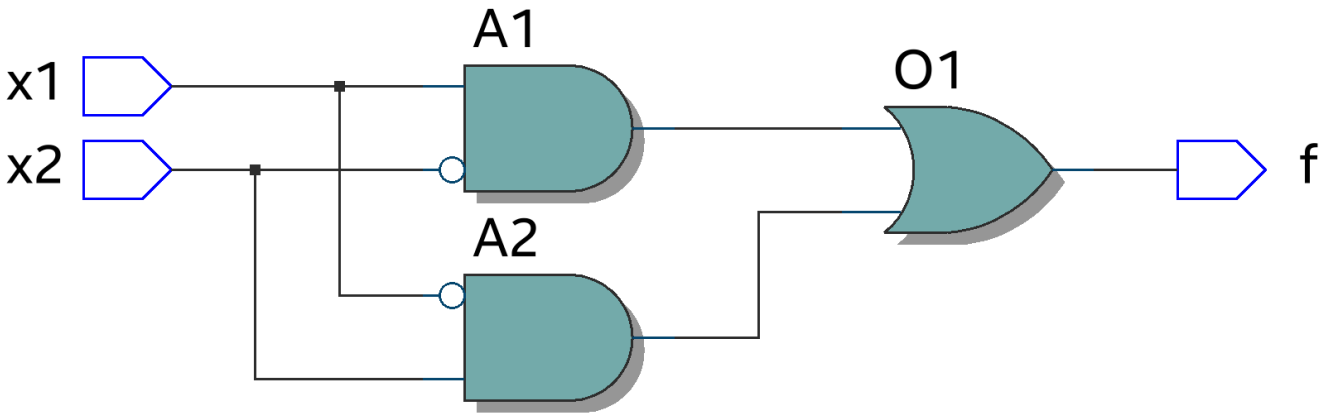


Figure 4. RTL View of Light Control

LightControl.v

```
1   //
2   // Verilog HDL for a two-way light controller
3   //
4   module LightControl (x1, x2, f);
5
6      input x1, x2;
7      output f;
8
9      wire wN1_out, wN2_out, wA1_out, wA2_out;
10
11     not   N1 (wN1_out, x1);
12     not   N2 (wN2_out, x2);
13     and   A1 (wA1_out, x1, wN2_out);
14     and   A2 (wA2_out, wN1_out, x2);
15     or    O1 (f, wA1_out, wA2_out);
16
17  endmodule
18
```

Figure 5. Verilog HDL code of the two-way light controller

Exercise 1C: Half Adder Circuit

In this exercise, we designed a Half Adder Circuit in Quartus Prime using Verilog HDL. The circuit takes two inputs (x, y) and produces the sum (S) and carry (C) outputs.

I / O	Variable	Description
Inputs	x	First single-bit input
	y	Second single-bit input
Outputs	C	Carry
	S	Sum

Table 1. Half Adder Circuit I/O

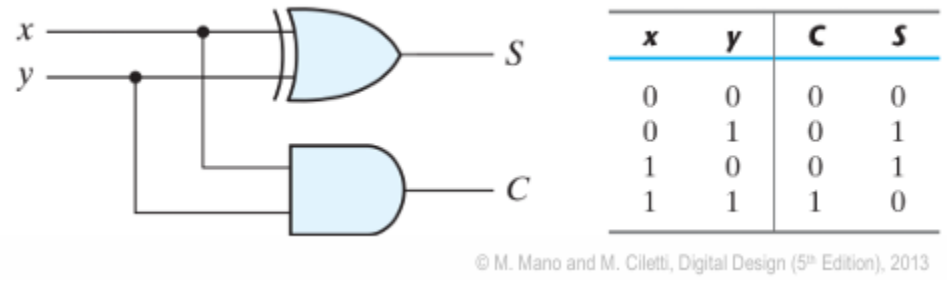


Figure 6. Half Adder Circuit and Truth Table

Flow Status	Successful - Fri Aug 22 10:12:11 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	HalfAdder
Top-level Entity Name	HalfAdder
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	2
Total registers	0
Total pins	4
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0
UFM blocks	0
ADC blocks	0

Figure 7. Flow Summary of Half Adder Circuit

Type	ID	Message
		**********
		Running Quartus Prime Analysis & Synthesis
		Command: quartus_map --read_settings_files=on --write_settings_files=off HalfAdder -c HalfAdder
⚠	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
	20030	Parallel compilation is enabled and will use 8 of the 8 processors detected
	12021	Found 1 design units, including 1 entities, in source file halfadder.v
	12127	Elaborating entity "HalfAdder" for the top level hierarchy
	286030	Timing-Driven Synthesis is running
	16010	Generating hard_block partition "hard_block:auto_generated_inst"
	21057	Implemented 6 device resources after synthesis - the final resource count might be different
		Quartus Prime Analysis & Synthesis was successful. 0 errors, 1 warning
		**********
		Running Quartus Prime Netlist Viewers Preprocess
		Command: quartus_npp HalfAdder -c HalfAdder --netlist_type=sgate
⚠	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value for best performance.
		Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning

Figure 8. Synthesis Results of Half Adder Circuit

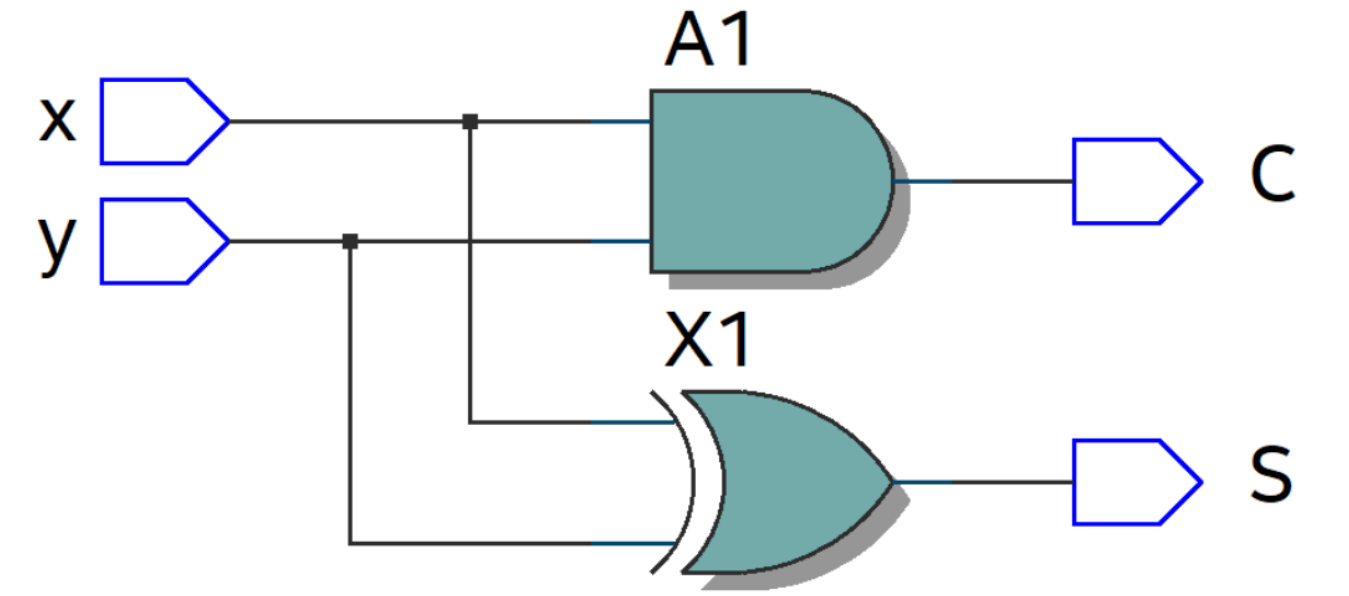


Figure 9. RTL View of Half Adder Circuit

HalfAdder.v

```
1  //
2  // Verilog HDL code for a half adder circuit
3  //
4  module HalfAdder (x, y, C, S);
5
6     input    x, y;
7     output   C, S;
8
9     xor      X1 (S, x, y);
10    and      A1 (C, x, y);
11
12 endmodule
13
```

Figure 10. Verilog HDL code of Half Adder Circuit