Laboratory Report # 4

Name: Lauron, John Enrico D. **Date Completed:** September 19, 2025

Laboratory Exercise Title: Dataflow Modeling of Combinational Circuits

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 4A: 4-Bit Comparator

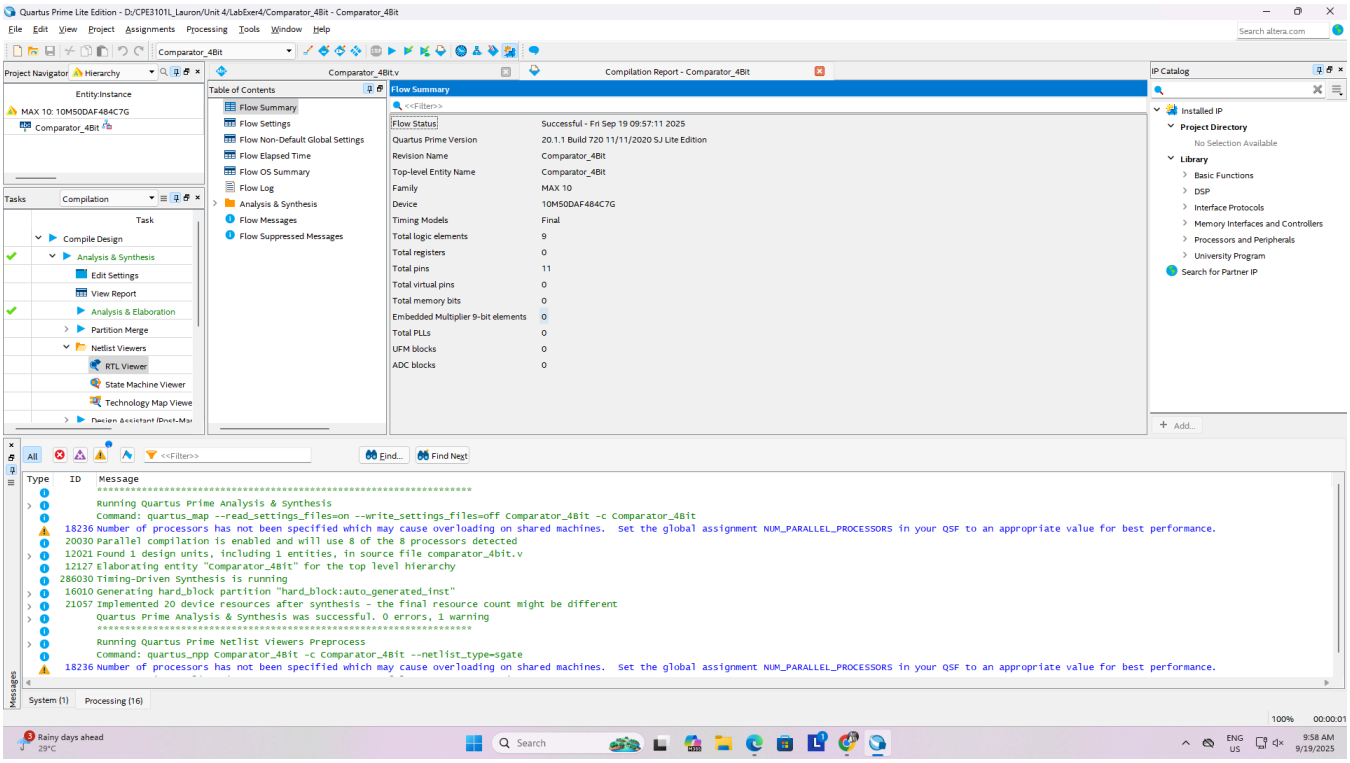

Figure 1. Design Synthesis Result of 4-Bit Comparator

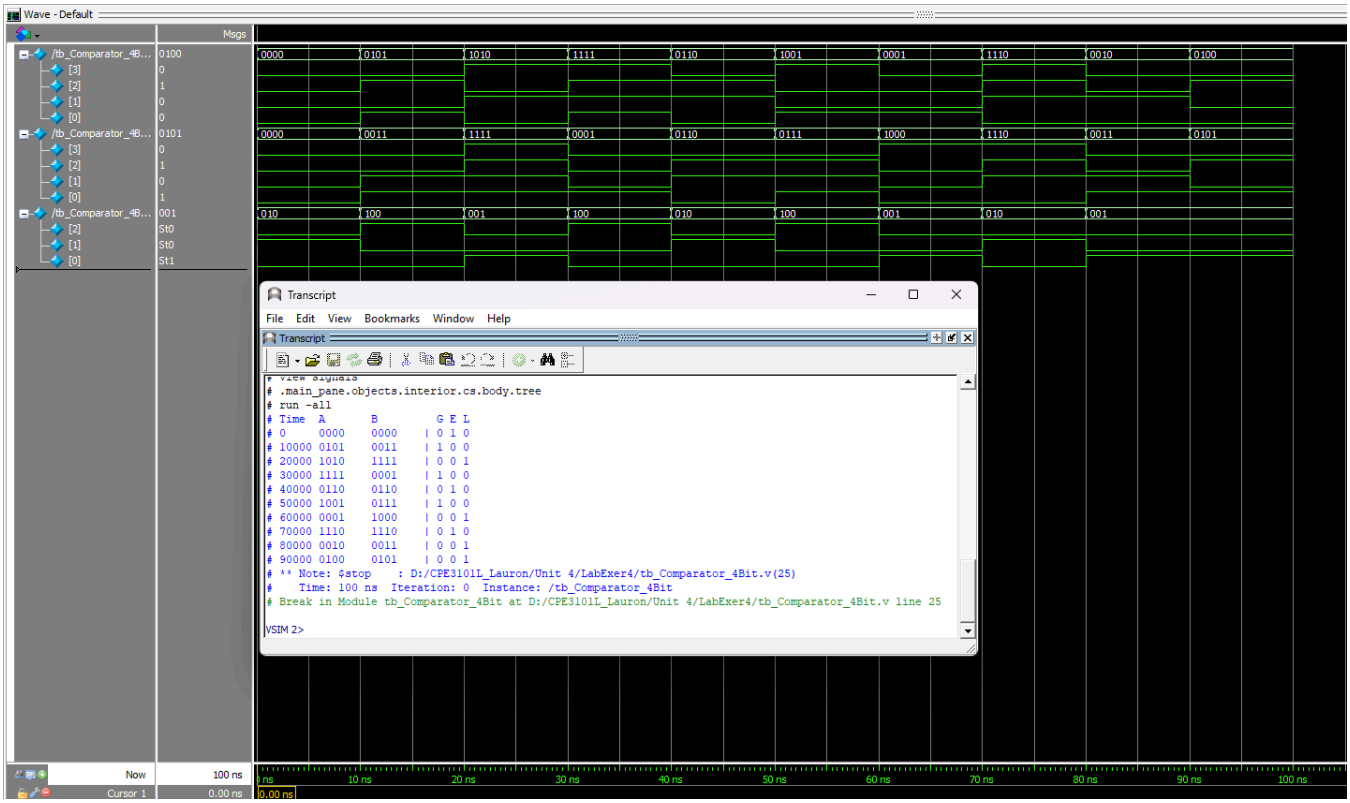

Figure 2. Simulation Results of 4-Bit Comparator (with annotations)

Exercise 4B: n-Bit 4-to-1 Line Multiplexer

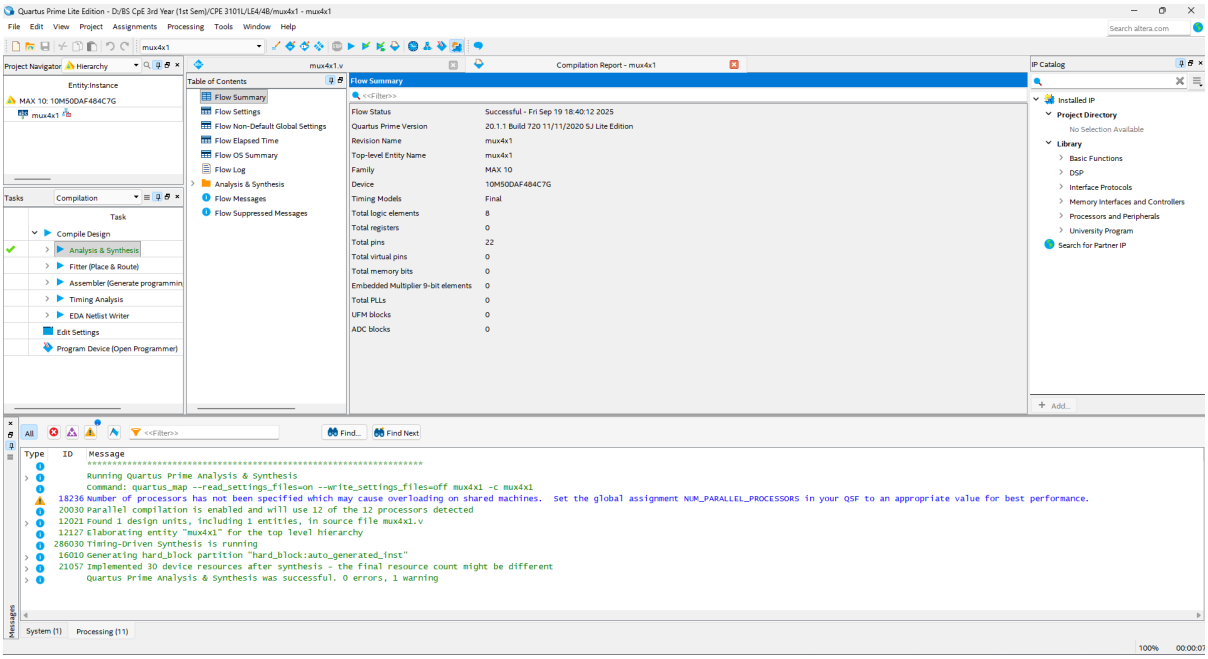

Figure 3. Design Synthesis of 4-Bit Multiplexer (with parameterized n-bit)

Part 1: 4-bit 4x1 Multiplexer

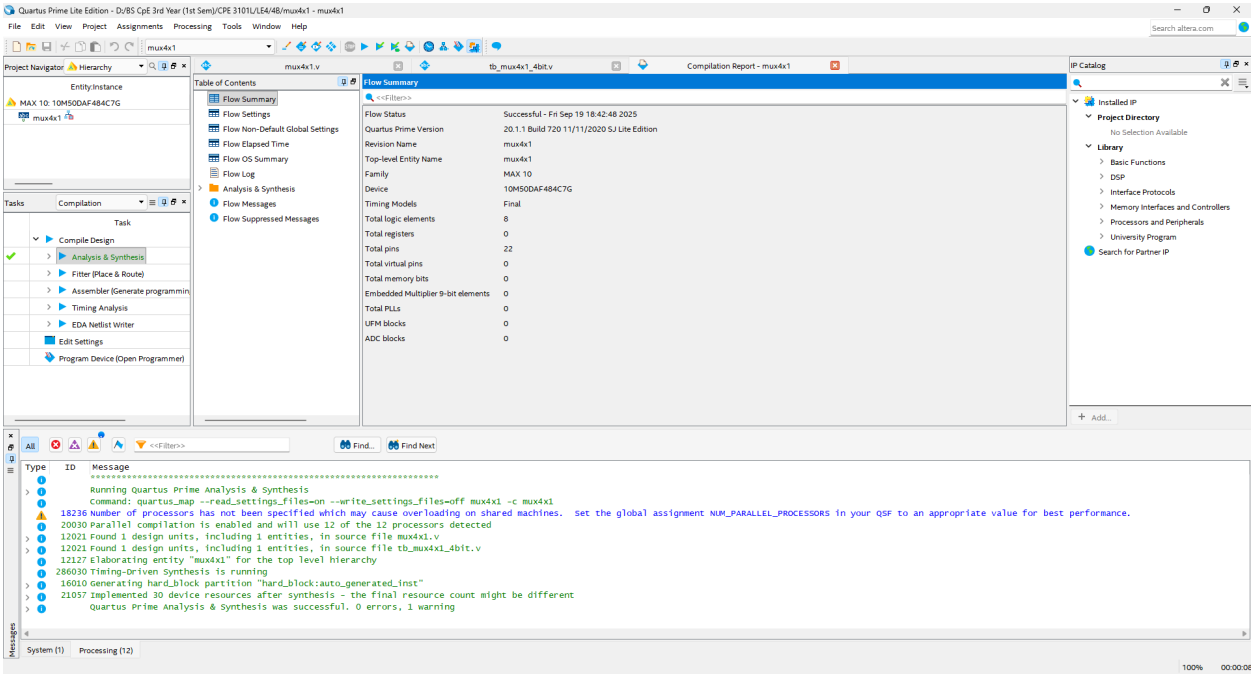

Figure 4 Design Synthesis of tb_mux4x1_4bit (4-bit 4x1 Multiplexer)

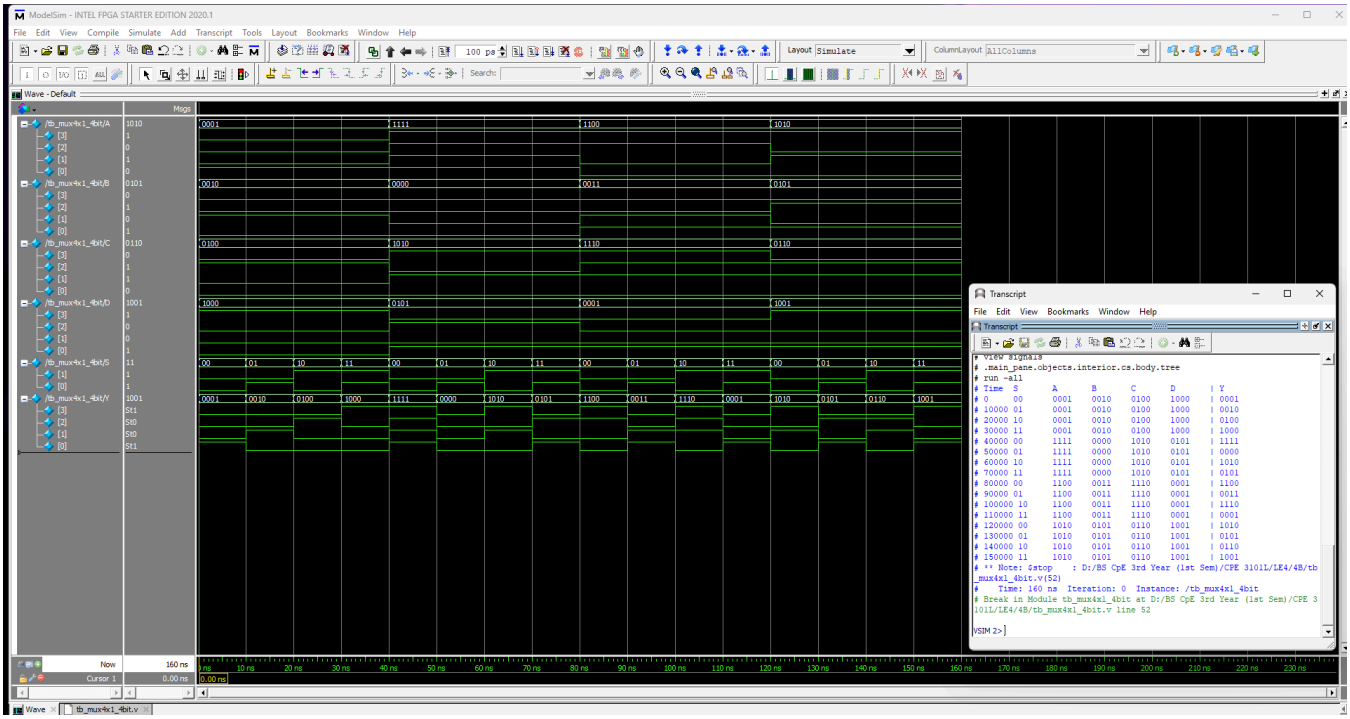

Figure 5 Simulation Results of 4-bit 4x1 Multiplexer (with annotations)

Part 2: 8-bit 4x1 Multiplexer

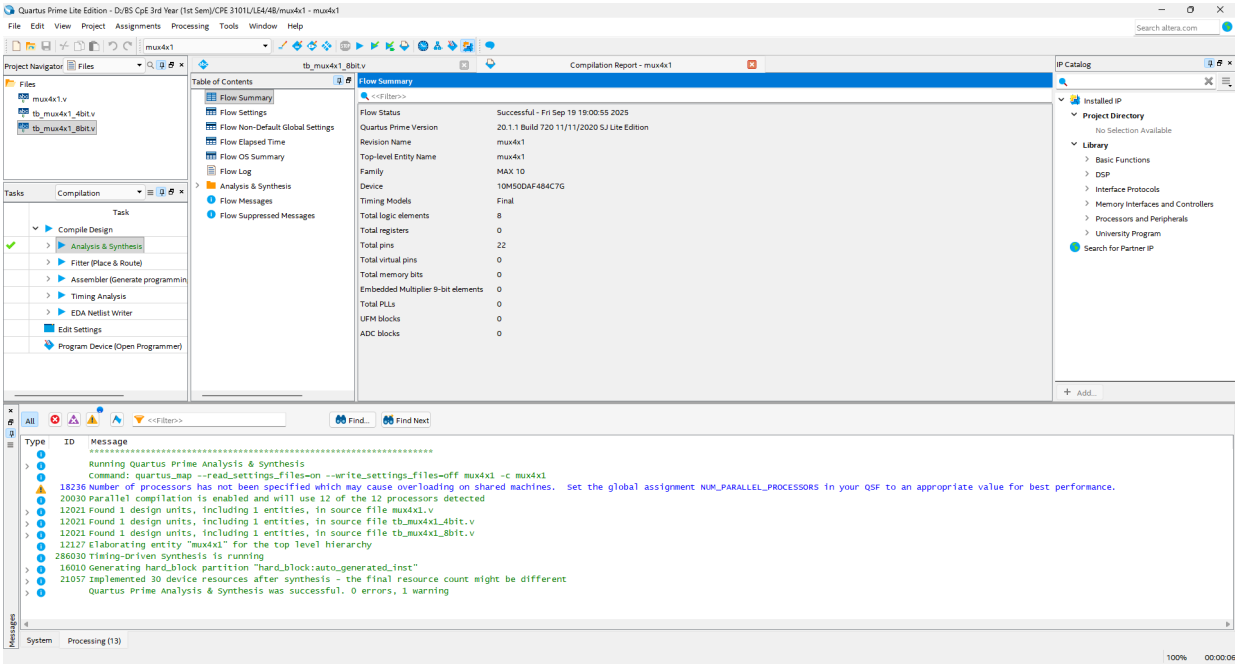

Figure 6. Design Synthesis of tb_mux4x1_8bit (8-bit 4x1 Multiplexer)

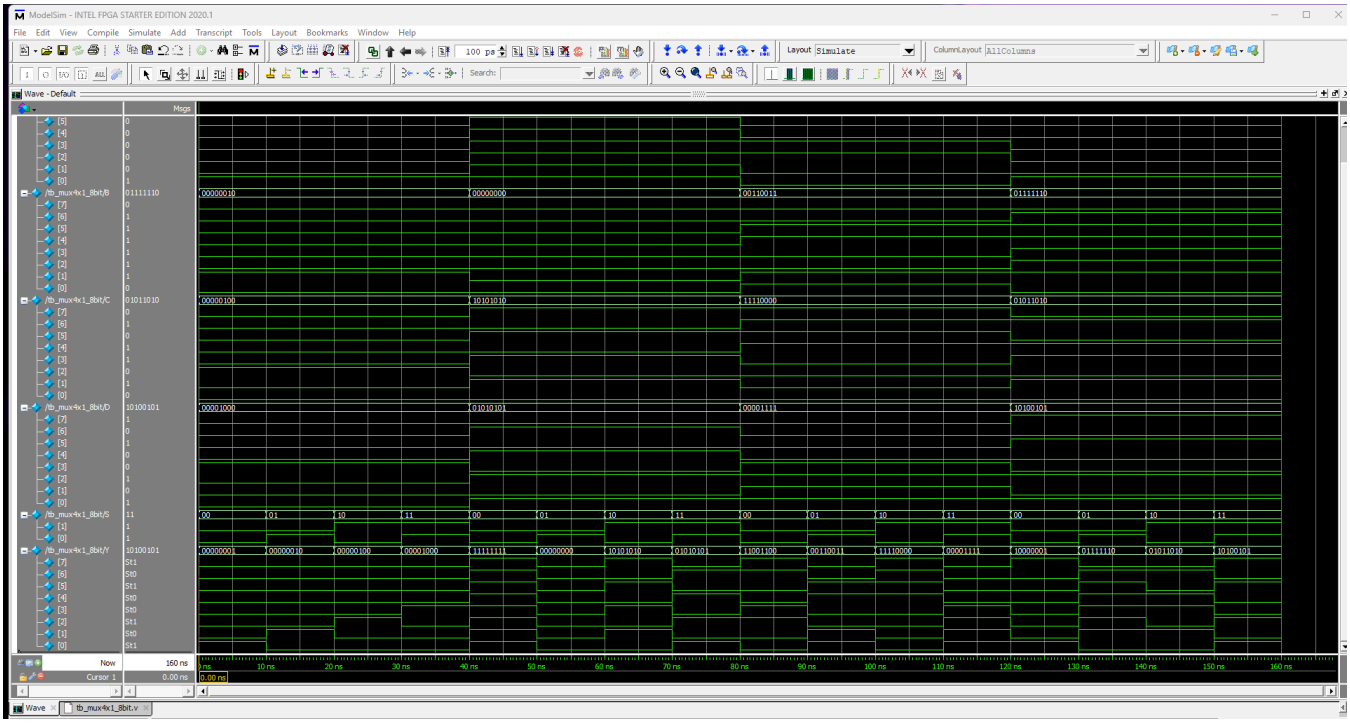

Figure 7. Simulation Results of 8-bit 4x1 Multiplexer

```
# Time  S       A               B               C               D               | Y
# 0     00      00000001 00000010 00000100 00001000 | 00000001
# 10000 01      00000001 00000010 00000100 00001000 | 00000010
# 20000 10      00000001 00000010 00000100 00001000 | 00000100
# 30000 11      00000001 00000010 00000100 00001000 | 00001000
# 40000 00      11111111 00000000 10101010 01010101 | 11111111
# 50000 01      11111111 00000000 10101010 01010101 | 00000000
# 60000 10      11111111 00000000 10101010 01010101 | 10101010
# 70000 11      11111111 00000000 10101010 01010101 | 01010101
# 80000 00      11001100 00110011 11110000 00001111 | 11001100
# 90000 01      11001100 00110011 11110000 00001111 | 00110011
# 100000 10     11001100 00110011 11110000 00001111 | 11110000
# 110000 11     11001100 00110011 11110000 00001111 | 00001111
# 120000 00     10000001 01111110 01011010 10100101 | 10000001
# 130000 01     10000001 01111110 01011010 10100101 | 01111110
# 140000 10     10000001 01111110 01011010 10100101 | 01011010
# 150000 11     10000001 01111110 01011010 10100101 | 10100101
# ** Note: $stop    : D:/BS CpE 3rd Year (1st Sem)/CPE 3101L/LE4/4B/tb_mux4x1_8bit.v(53)
#    Time: 160 ns  Iteration: 0  Instance: /tb_mux4x1_8bit
# Break in Module tb_mux4x1_8bit at D:/BS CpE 3rd Year (1st Sem)/CPE 3101L/LE4/4B/tb_mux4x1_8bit.v line 53

VSIM 2>
```

Figure 8. Simulation output of the 8-bit 4x1 multiplexer