University of San Carlos
DEPARTMENT OF COMPUTER ENGINEERING

Laboratory Report # 5

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Laboratory Exercise Title: Behavioral Modeling of Combinational Circuits

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

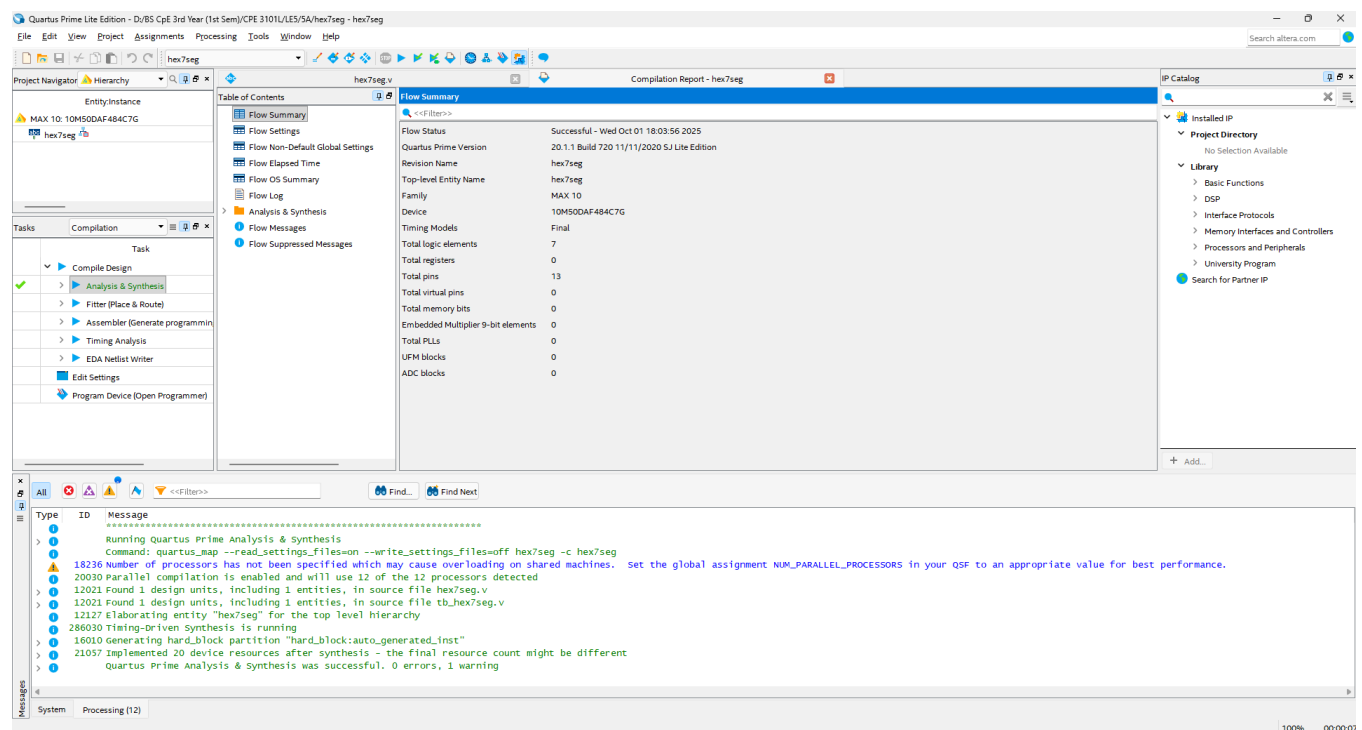## Exercise 5A: Hexadecimal Digit to 7-Segment Decoder

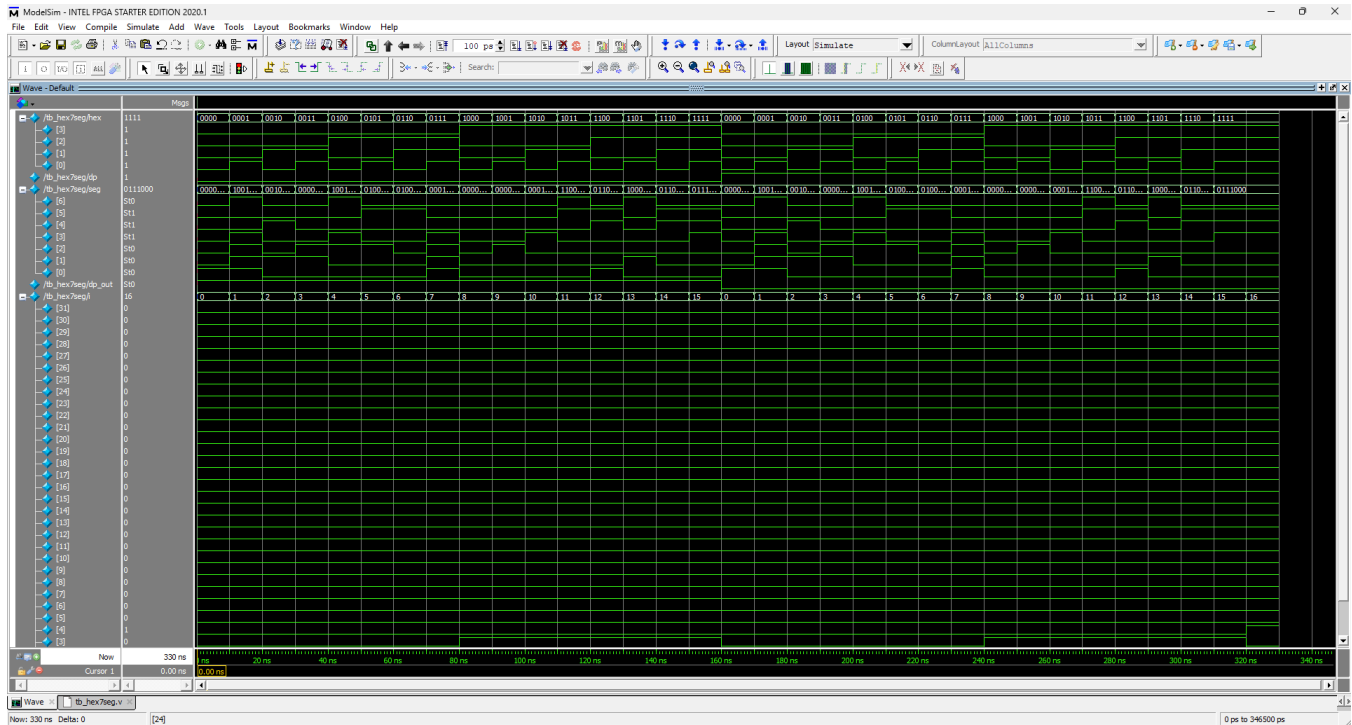*Figure 1. Design Synthesis Result of Hexadecimal Digit to 7-Segment Decoder*

Figure 2. Simulation Results of Hexadecimal Digit to 7-Segment Decoder

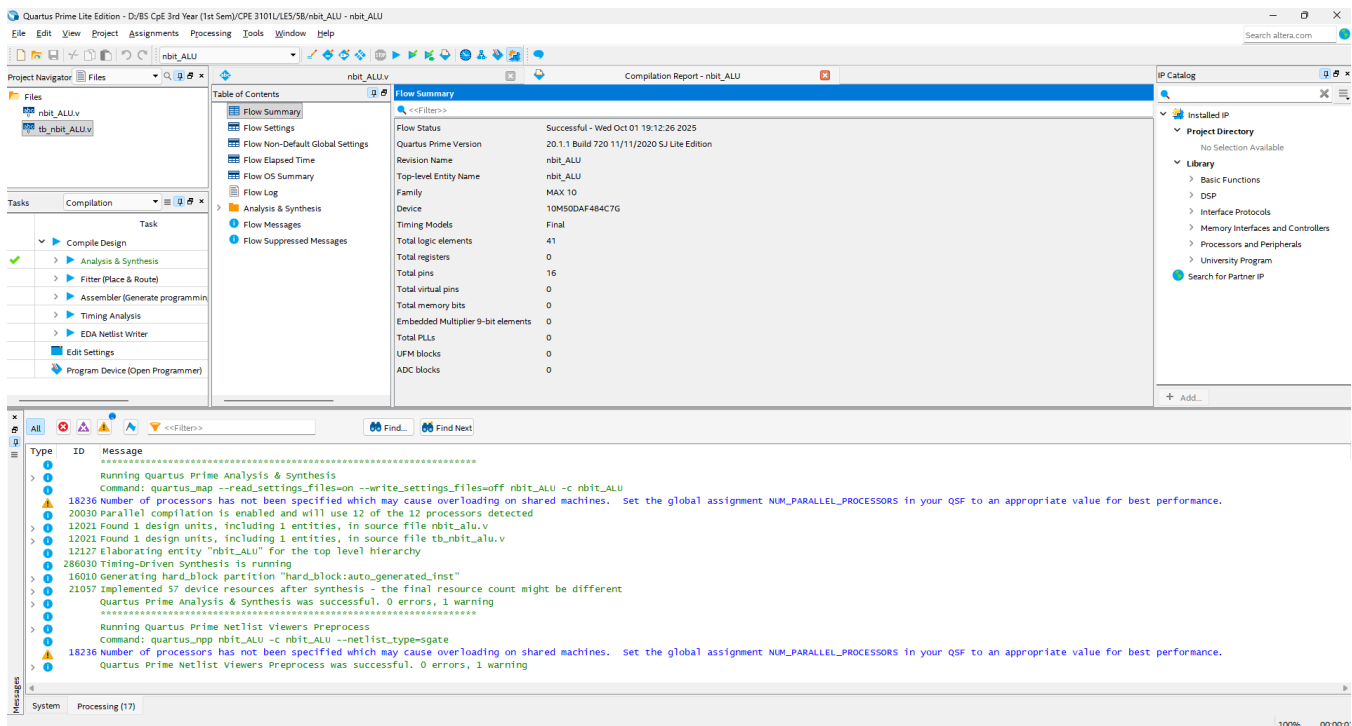## Exercise 5B: *n*-Bit Arithmetic and Logic Unit (ALU)

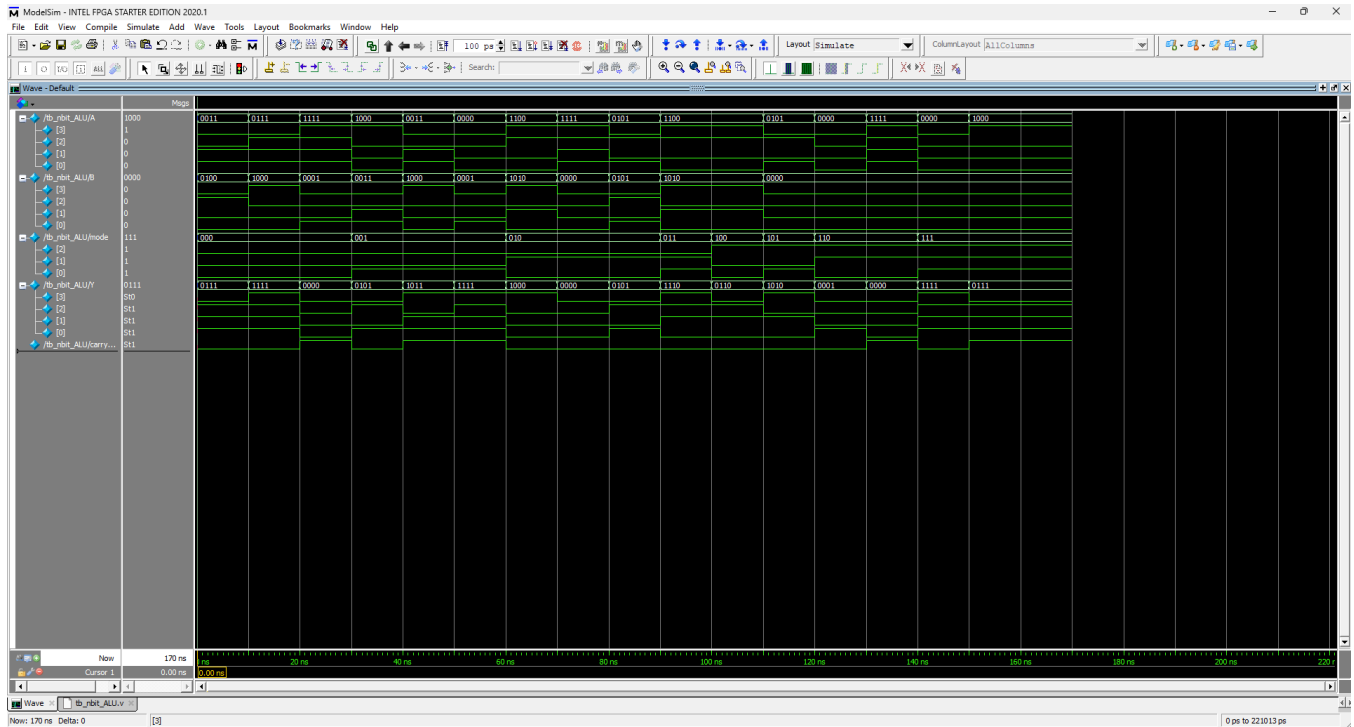*Figure 3. Design Synthesis Result of n-Bit Arithmetic and Logic Unit (ALU)*

Figure 4. Simulation Results of n-Bit Arithmetic and Logic Unit (ALU)