Laboratory Report # 6

Name: Lauron, John Enrico D. **Date Completed:** October 9, 2025

Laboratory Exercise Title: Behavioral Modeling of Sequential Circuits

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 6A: JK Flip-flop

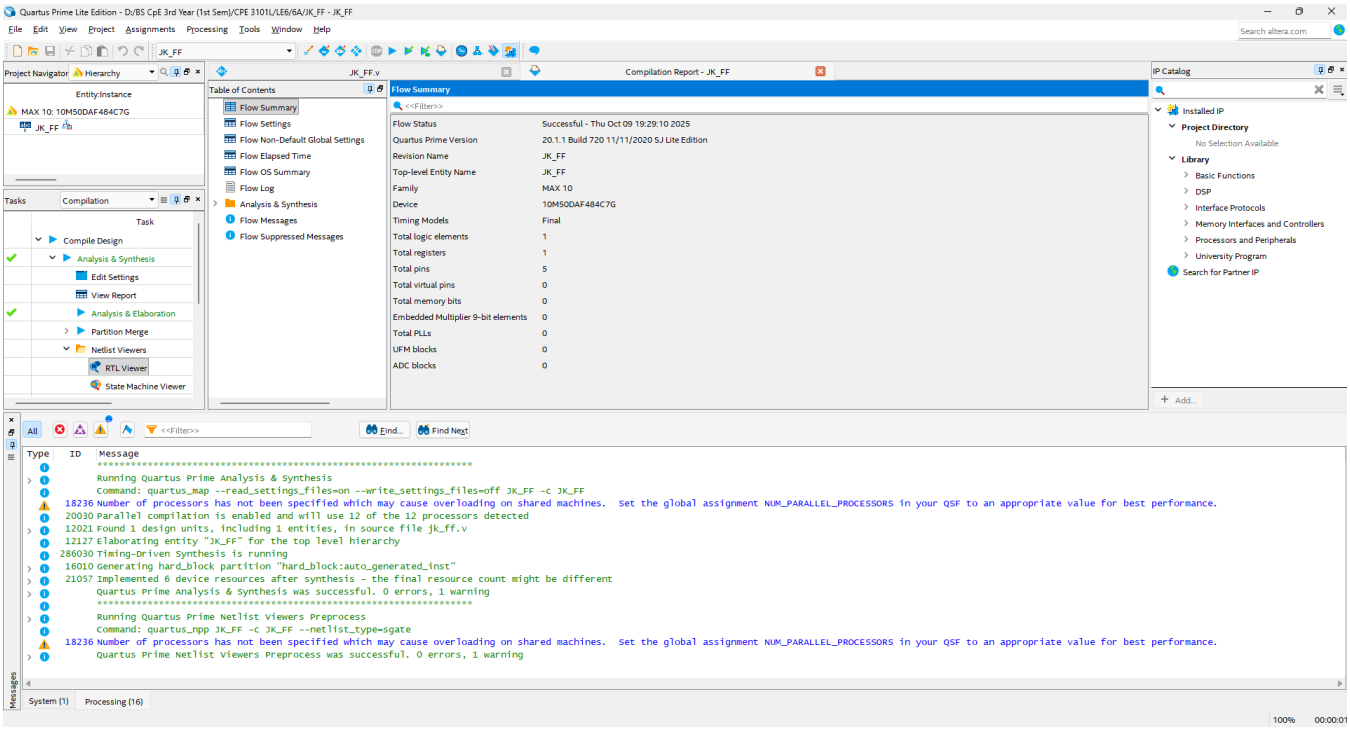

Figure 1. Design Synthesis Result of JK Flip-flop

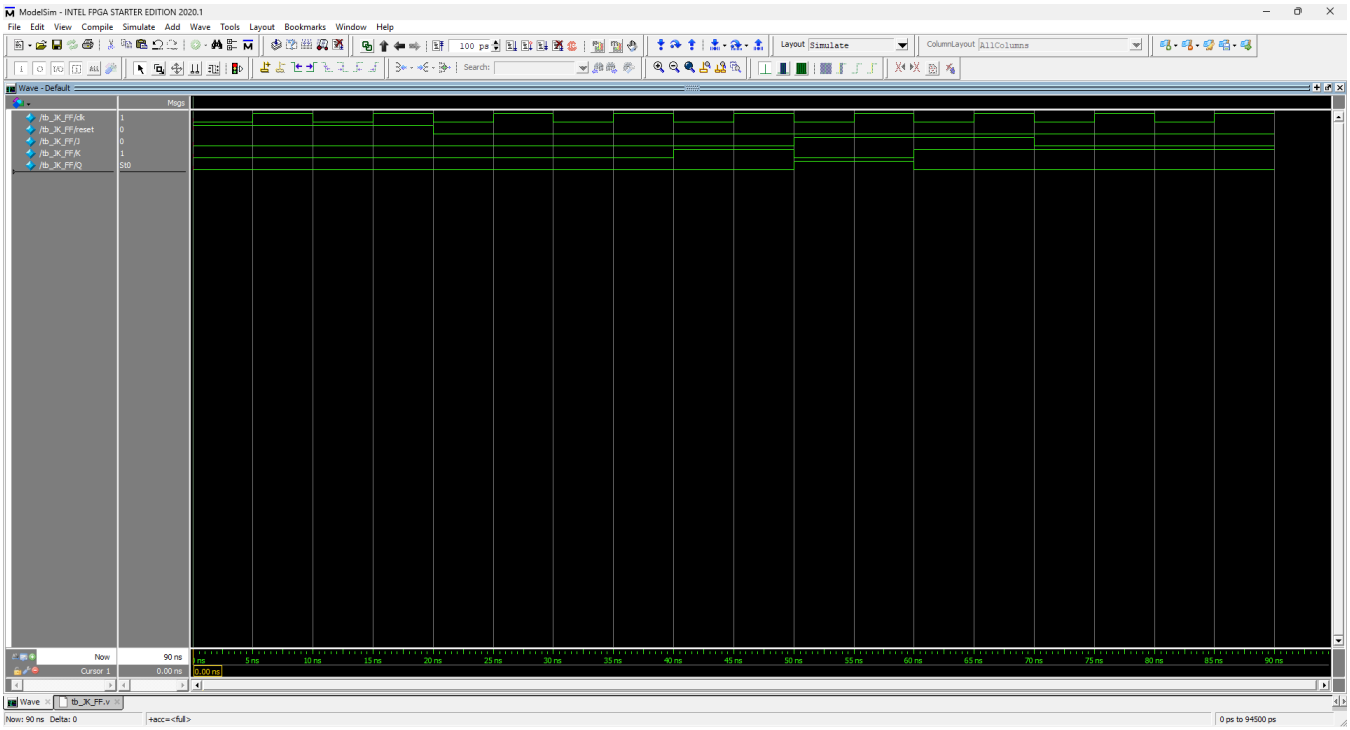

Figure 2. Simulation Results of JK Flip-flop

Exercise 6B: 4-Bit Binary Up/Down Counter

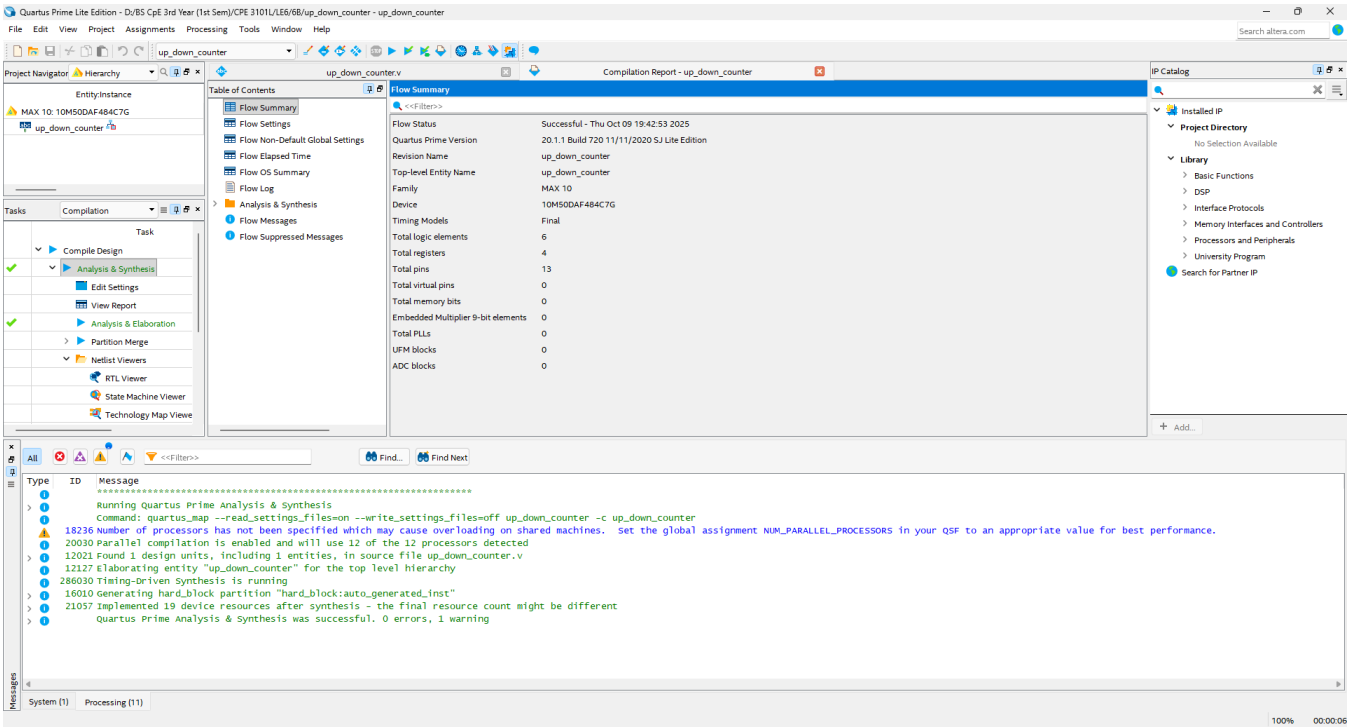

Figure 3. Design Synthesis Result of 4-Bit Binary Up/Down Counter

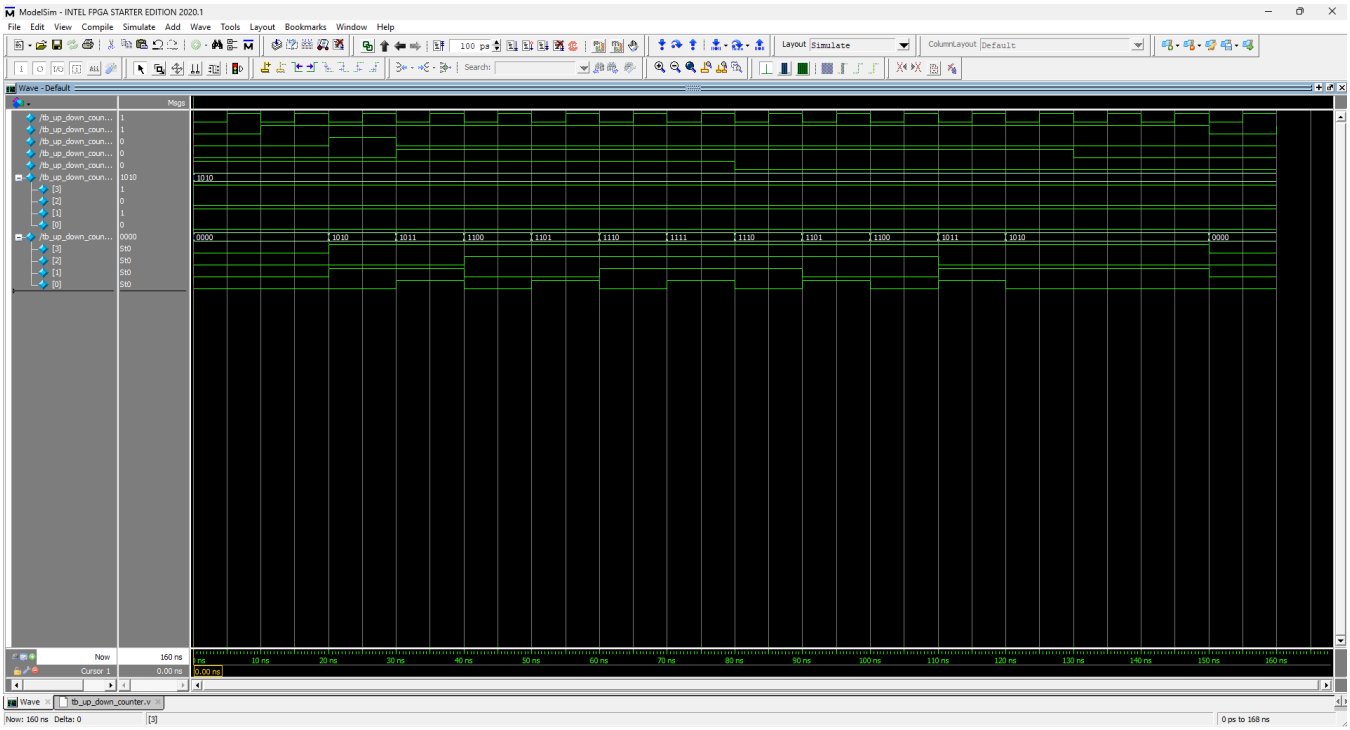

Figure 4. Simulation Results of 4-Bit Binary Up/Down Counter