



## Laboratory Report # 6

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Laboratory Exercise Title: Behavioral Modeling of Sequential Circuits

### Target Course Outcomes:

**CO1:** Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

**CO2:** Verify the functionality of HDL-based components through design verification tools.

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### Exercise 6A: JK Flip-flop

The screenshot shows the Quartus Prime Lite Edition interface with the following details:

- Project Navigator:** MAX 10: 10M50DAF484C7G, Entity Instance: JK\_FF.
- Tasks:** Compilation, Task: Compile Design, Analysis & Synthesis, View Report, Partition Merge, Netlist Viewers, RTL Viewer, State Machine Viewer.
- Flow Summary:** Successful - Thu Oct 09 19:29:10 2025. Quartus Prime Version: 20.1.1 Build 720 11/11/2020 SJ Lite Edition. Revision Name: JK\_FF. Top-level Entity Name: JK\_FF. Family: MAX 10. Device: 10M50DAF484C7G. Timing Models: Final. Total logic elements: 1. Total registers: 1. Total pins: 5. Total virtual pins: 0. Total memory bits: 0. Embedded Multiplier 9-bit elements: 0. Total PLLs: 0. UFM blocks: 0. ADC blocks: 0.
- Messages:** A list of synthesis messages including:
  - Running Quartus Prime Analysis & Synthesis
  - Command: quartus\_map --read\_settings\_files=on --write\_settings\_files=off JK\_FF -c JK\_FF
  - 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM\_PARALLEL\_PROCESSORS in your QSF to an appropriate value for best performance.
  - 18230 Parallel compilation is enabled and will use 12 of the 12 processors detected
  - 18230 12 parallel compilation tasks, including 1 entities, in source file JK\_FF.v
  - 12237 Elaborating entity "JK\_FF" for the top level hierarchy
  - 286030 Timing-driven synthesis is running
  - 16010 Generating hard\_block partition "hard\_block:auto\_generated\_inst"
  - 21057 Implemented 6 device resources after synthesis - the final resource count might be different
  - Quartus Prime Analysis & synthesis was successful. 0 errors, 0 warnings
  - \*\*\*\*\*
  - Running Quartus Prime Netlist Viewers Preprocess
  - Command: quartus\_npp JK\_FF -c JK\_FF --netlist\_type=sgate
  - 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM\_PARALLEL\_PROCESSORS in your QSF to an appropriate value for best performance.
  - Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning

Figure 1. Design Synthesis Result of JK Flip-flop

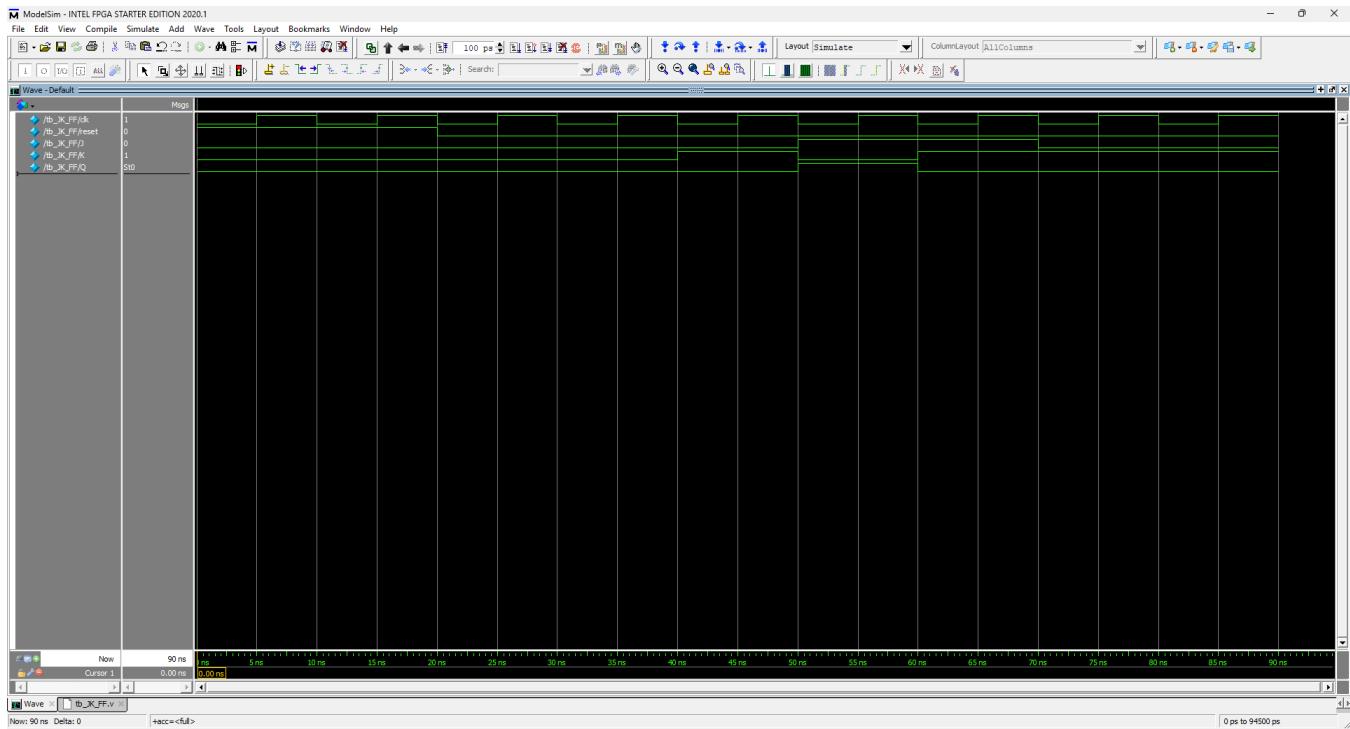


Figure 2. Simulation Results of JK Flip-flop

### Exercise 6B: 4-Bit Binary Up/Down Counter

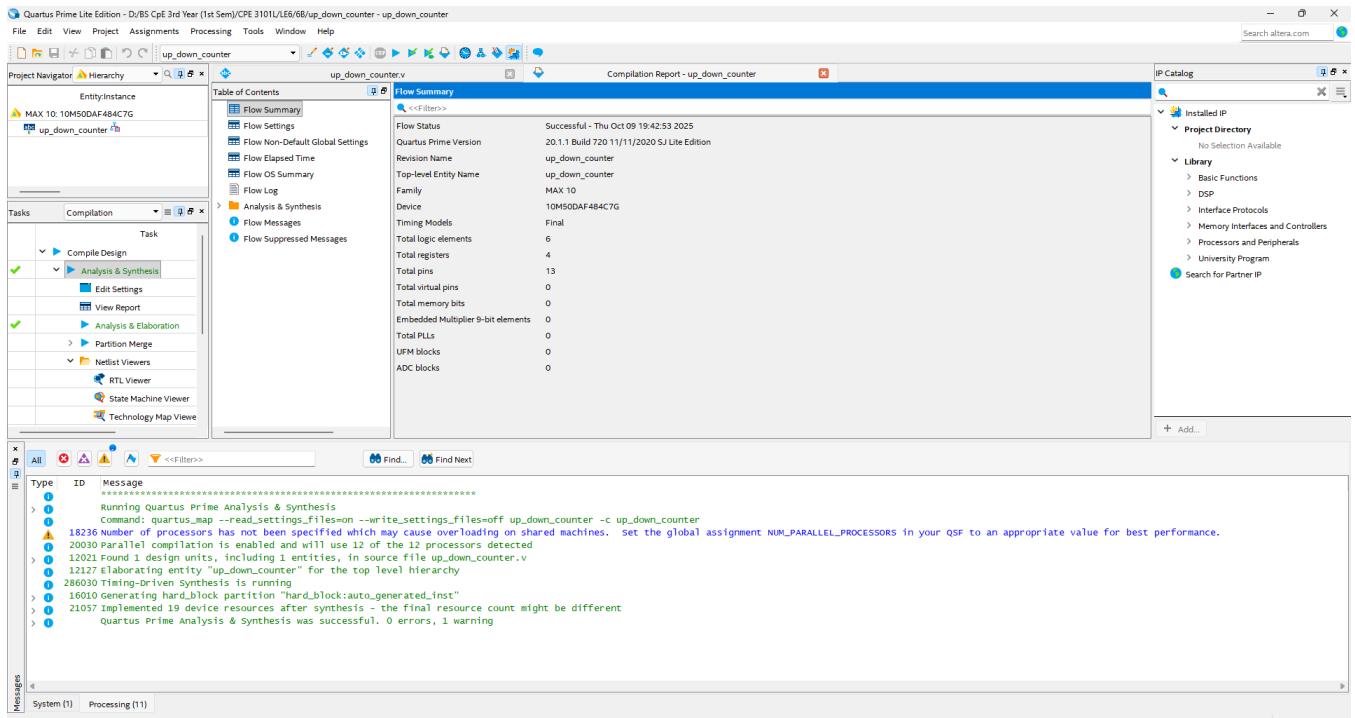


Figure 3. Design Synthesis Result of 4-Bit Binary Up/Down Counter

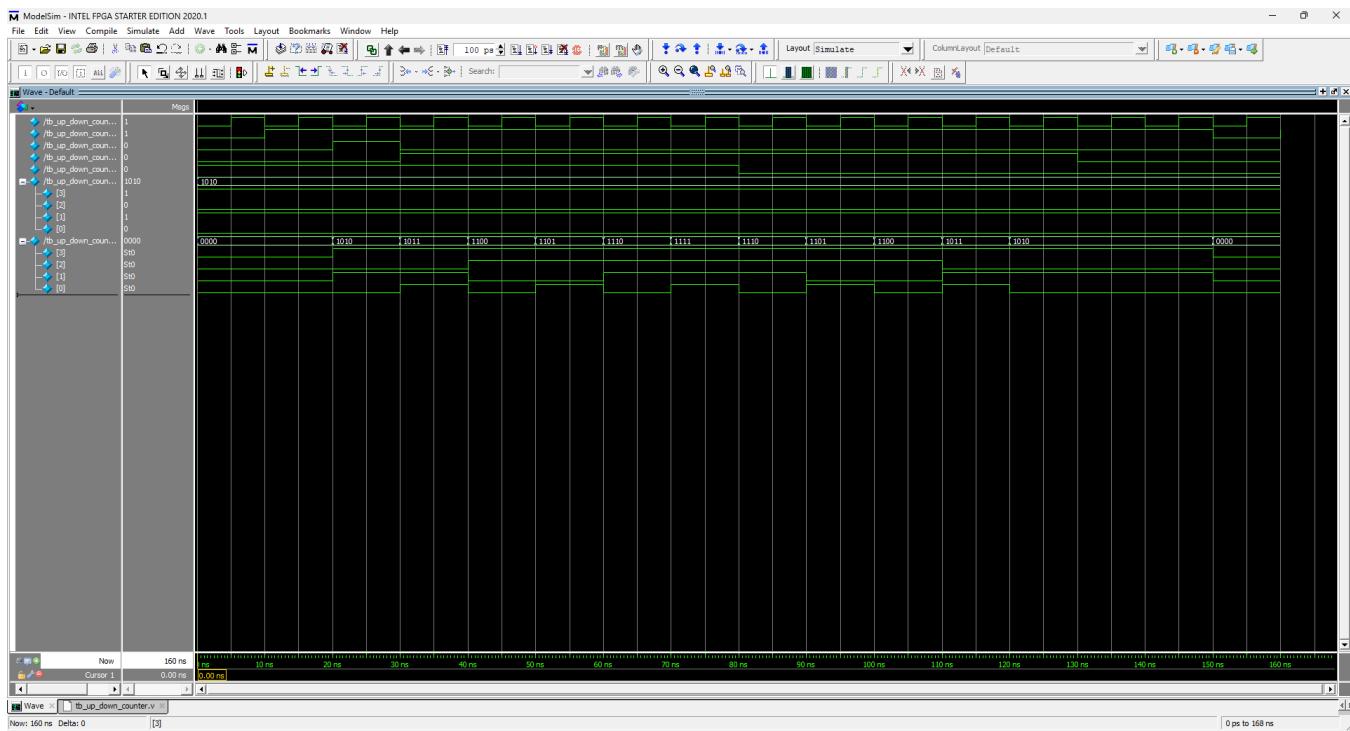


Figure 4. Simulation Results of 4-Bit Binary Up/Down Counter