

Unit 02 - 8086 Microprocessor Introduction

History of 80x86 Family

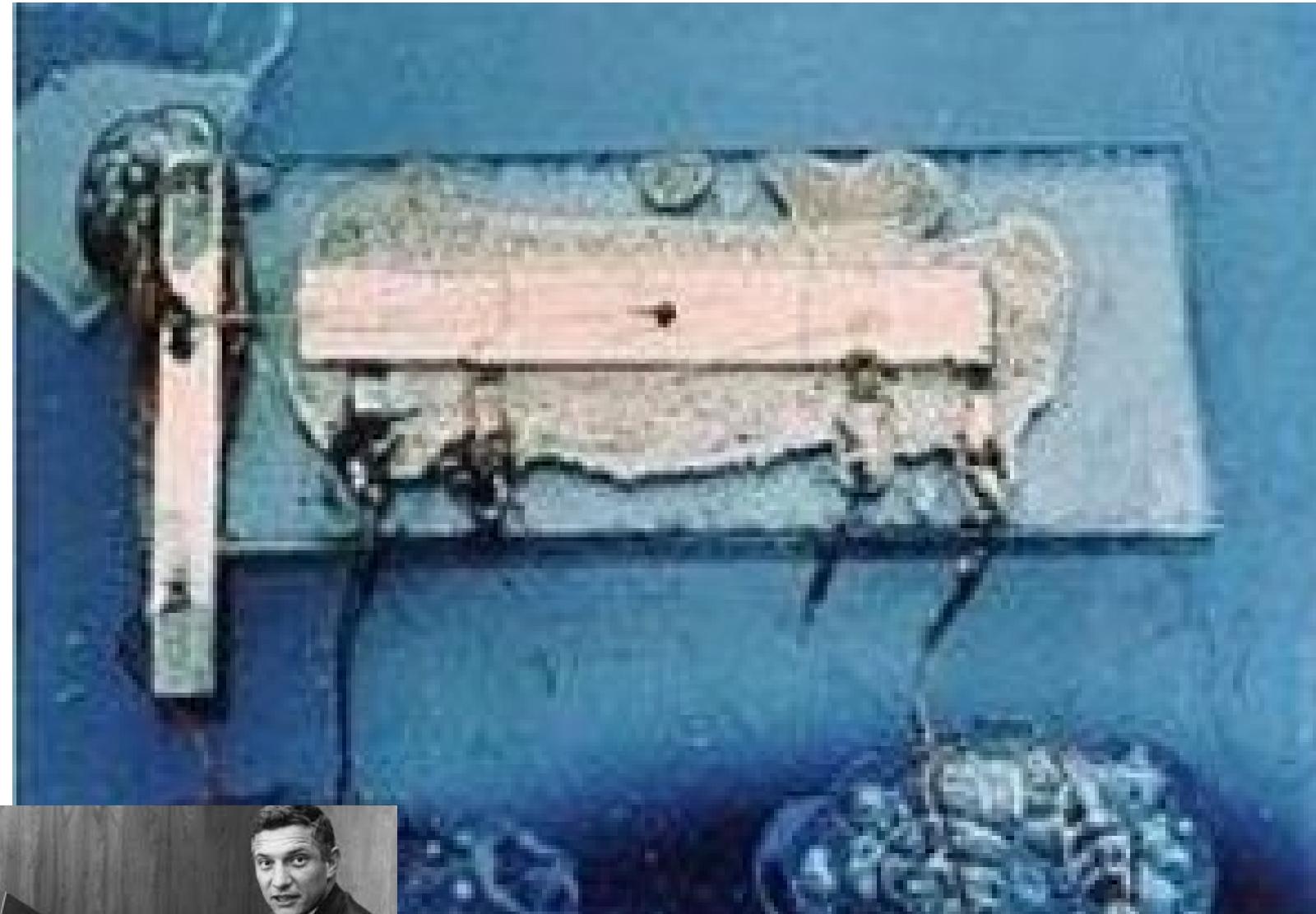
History of 8086 Family

- First IC (integrated circuit) invented in 1959 by Fairchild Semiconductor (founded 1957).
- **Gordon Moore**, Andrew Grove, Robert Noyce resigned from Fairchild Semiconductor and founded Integrated Electronics (Intel) in 1968.
- First Intel microprocessor was released in 1971
- Intel started with 4-bit uPs then evolved to 8, 16, 32, 64 – bit uPs

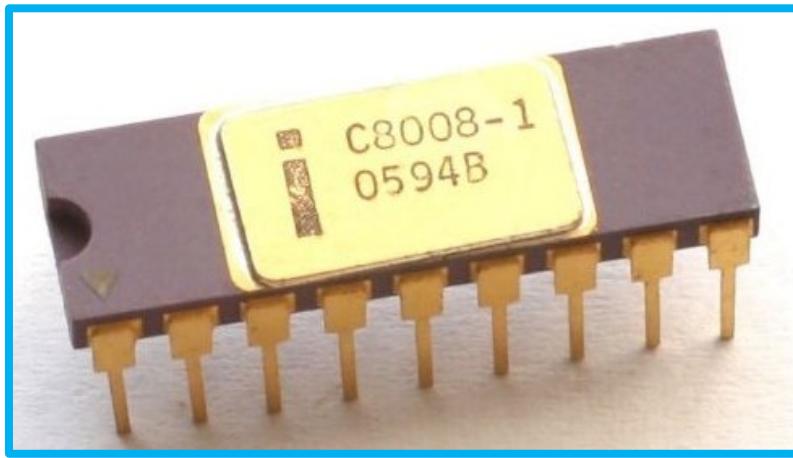
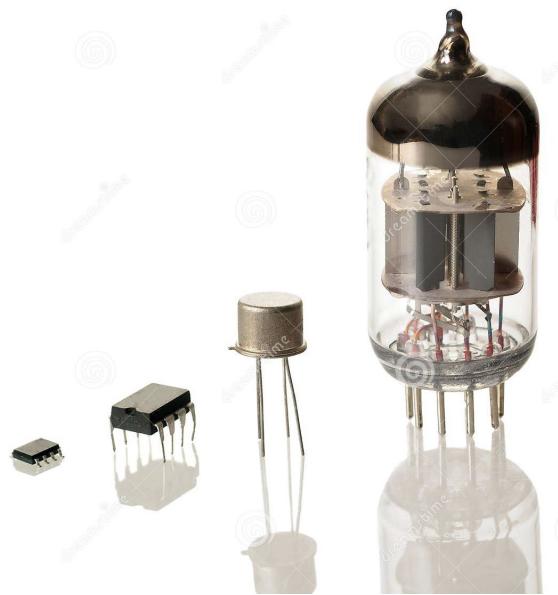
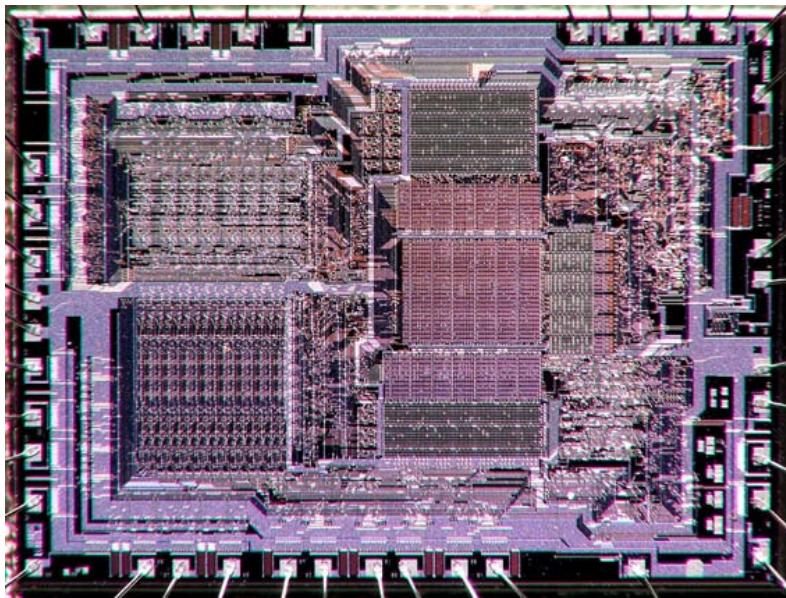
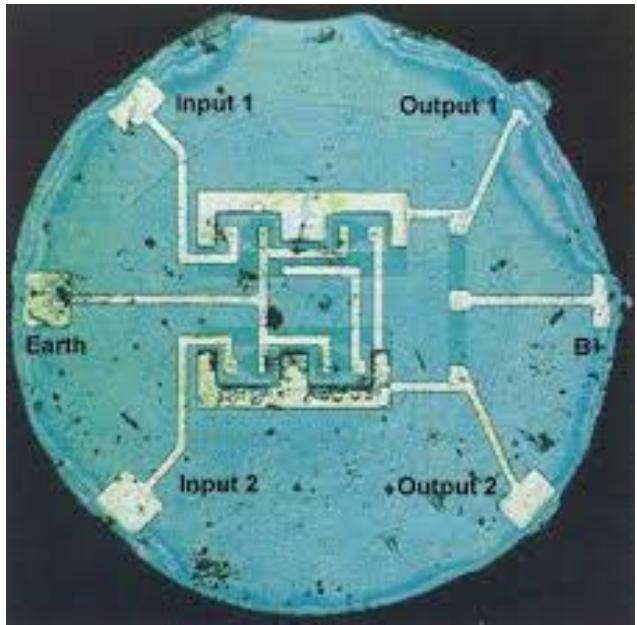


Robert Noyce (1927-1990)

American physicist, co-inventor of Integrated Circuit (IC), co-founder of Fairchild Semiconductor & Intel Corp., known as “Mayor of Silicon Valley”

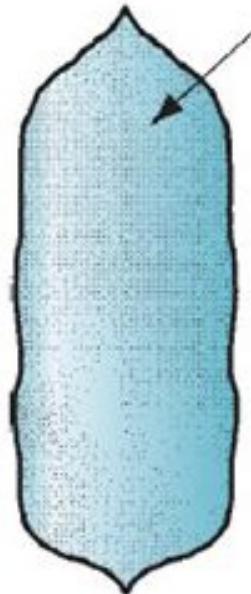


First Integrated Circuit (IC)



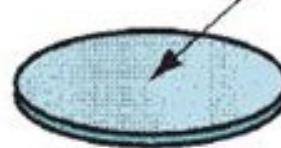
Microprocessors Fabrication

Silicon ingot

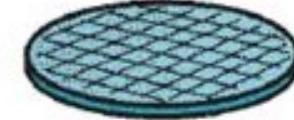


(1)

Silicon wafer



IC fabrication
on wafer surface

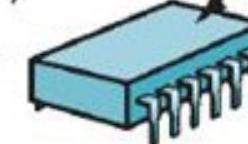


(2)

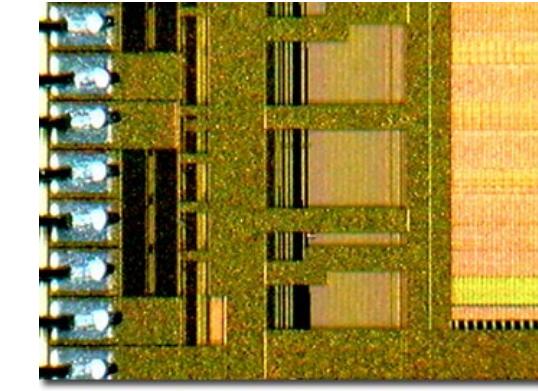
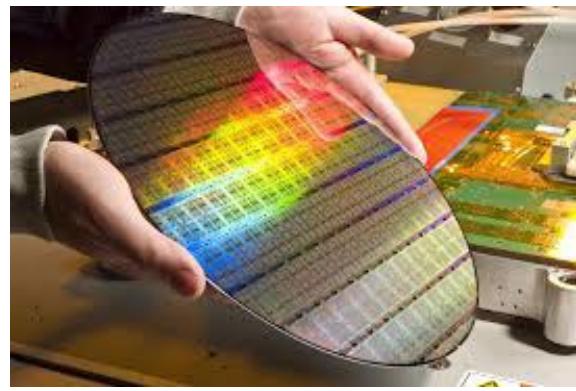
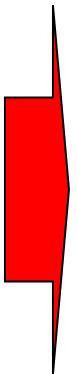
Chip (die)

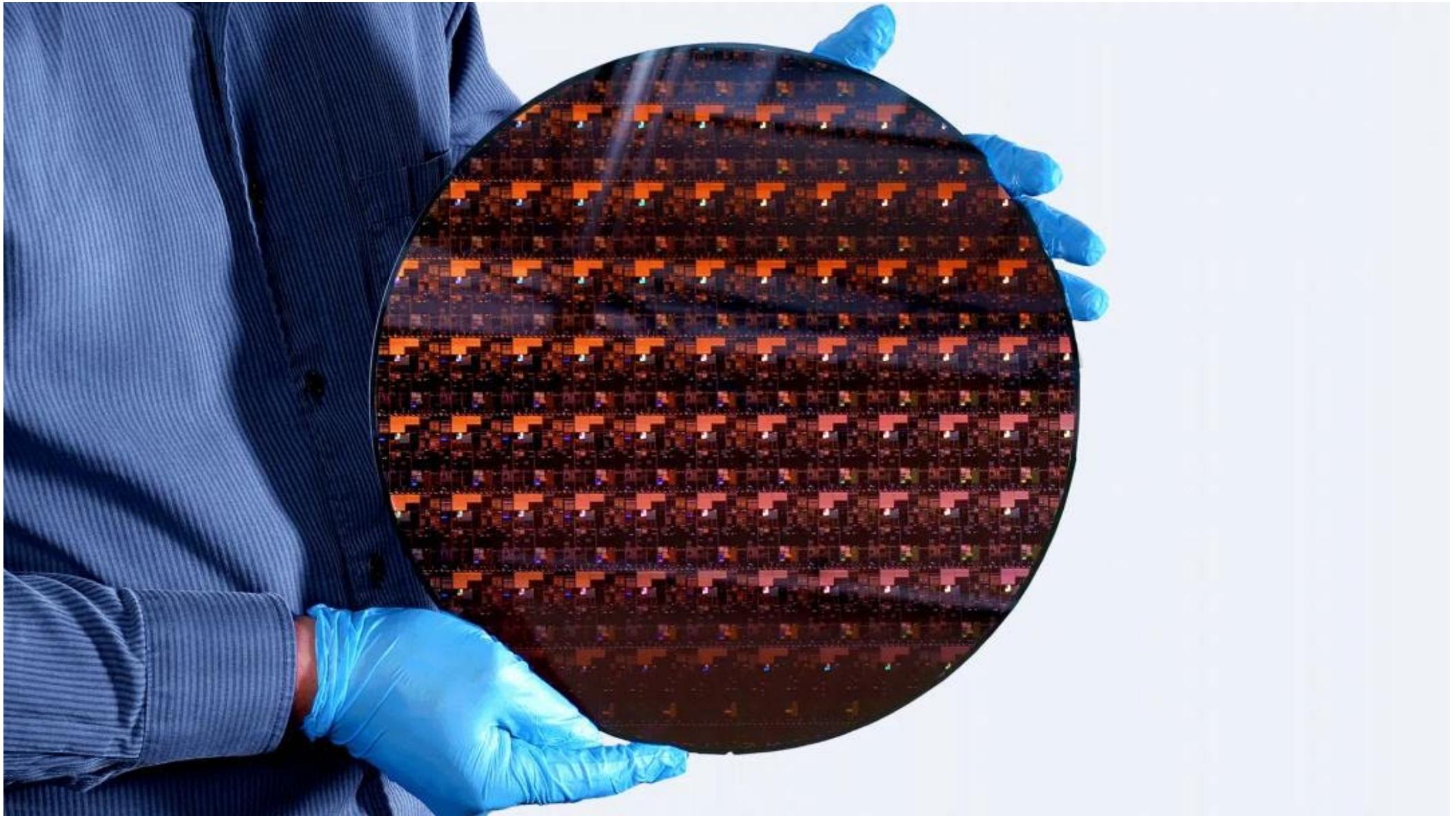


Packaged chip



(3)



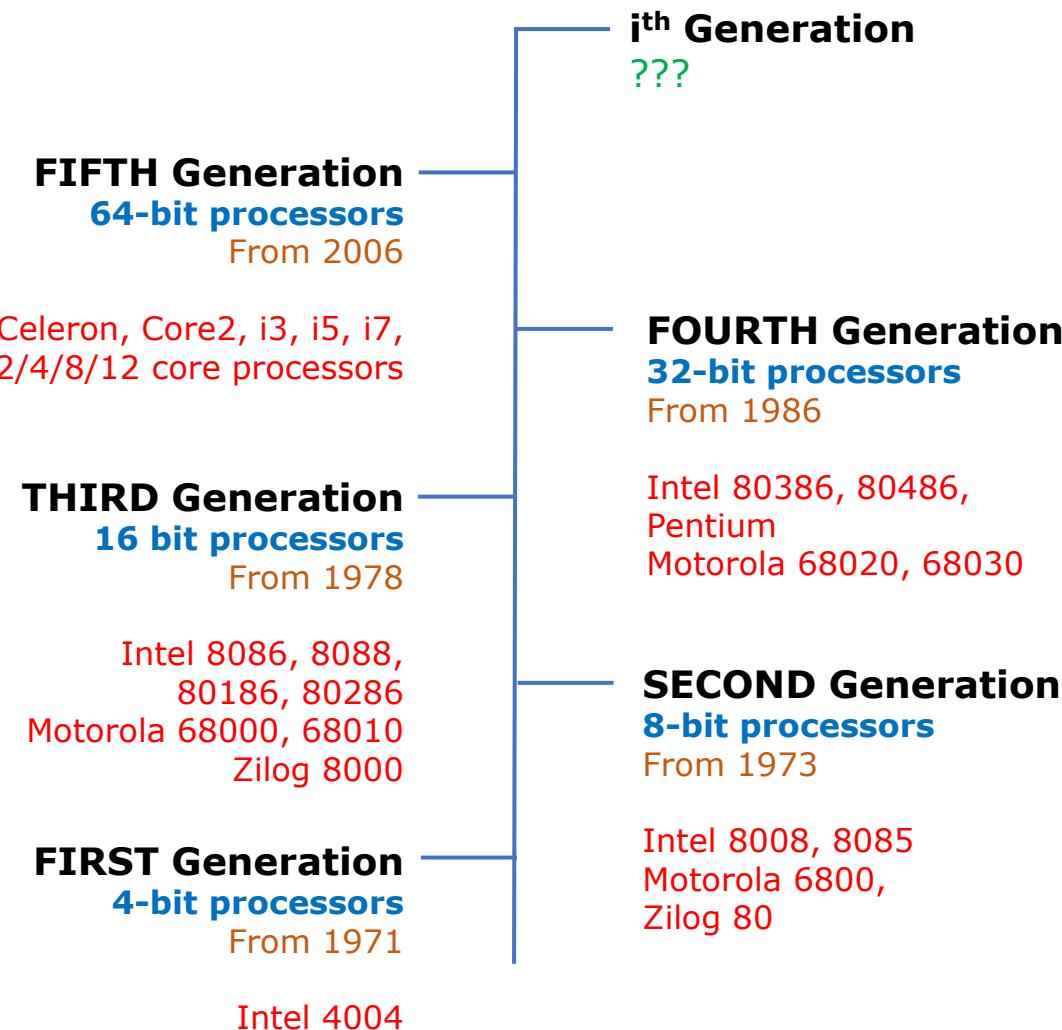


Evolution of Intel Microprocessors

Evolution of Microprocessors

Microprocessors are categorized by generations based on the size of the microprocessor:

- **First Generation (from 1971-1972): 4-bit Microprocessors**
- **Second Generation (from 1973-1977): 8-bit Microprocessors**
- **Third Generation (from 1978-1985): 16-bit Microprocessors**
- **Fourth Generation (from 1986-2005): 32-bit Microprocessors**
- **Fifth Generation (from 2006-present): 64-bit Microprocessors**



Date	Name	Developer	Clock	Process	Transistors (millions)	<u>Cores per die / Dies per module</u>	<u>Threads per core</u>
2020	Zen 3	AMD	3.4–4.9 GHz	7 nm, 12nm	6240-35290	4, 6, 8 / 1, 2, 4, 8	2
2020	M1 Series	Apple	3.2 GHz	5 nm	16000-144000	4-8P, 2-4E / 1, 2	1
2021	Alder Lake	Intel	0.7-5.3 GHz	7 nm	?	0-8P, 2-8E	1-2
2022	IBM Telum	IBM	>5 GHz	7 nm	22000	8	1
2022	M2 Series	Apple	3.49/2.42 GHz	5 nm (N5P)	20000-134000	4-8P, 4E / 1, 2	1
2022	Zen 4	AMD	2.0-5.7 GHz	5 nm, 7 nm	?	4, 6, 8 / 1, 2, 4, 8, 12	2
2023	Zen 4C	AMD	2.0 - 3.1 GHz	5 nm	?	4, 6, 8, 12, 14, 16 / 1, 2, 4, 8	1, 2
2023	M3 Series	Apple	4.05/2.75 GHz	3 nm	25000-92000	4-12P, 4-6E	1
2023	Meteor Lake	Intel	0.7-5.0 GHz	5 nm, 7 nm	?	2-6P, 4-8E, 2LP-E	1-2
2024	Oryon	Qualcomm	4.3 GHz	4 nm	?	12	1
2024	Zen 5	AMD	4.3 GHz	5 nm	?	6, 8, 16 / 2, 3	2

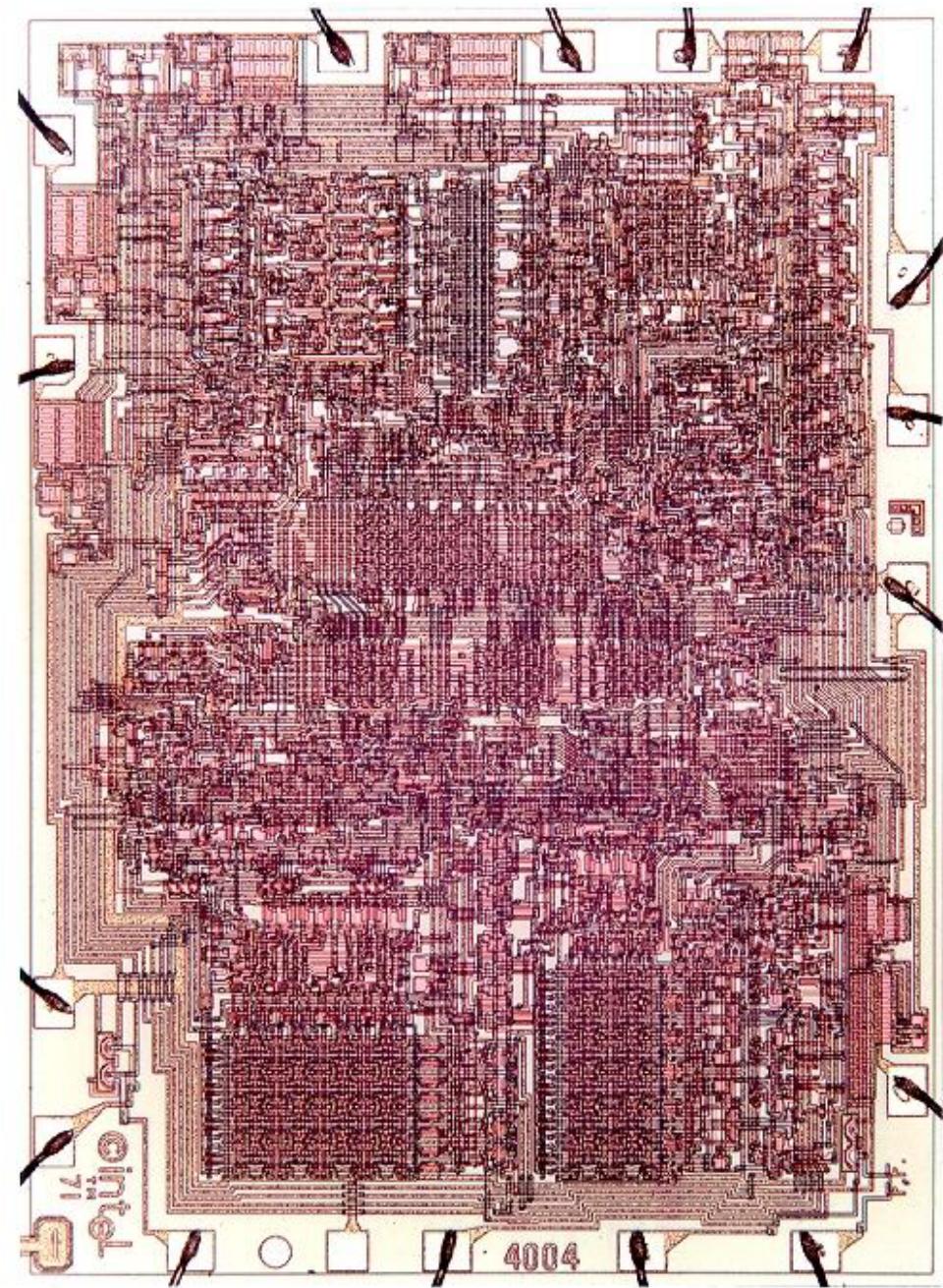
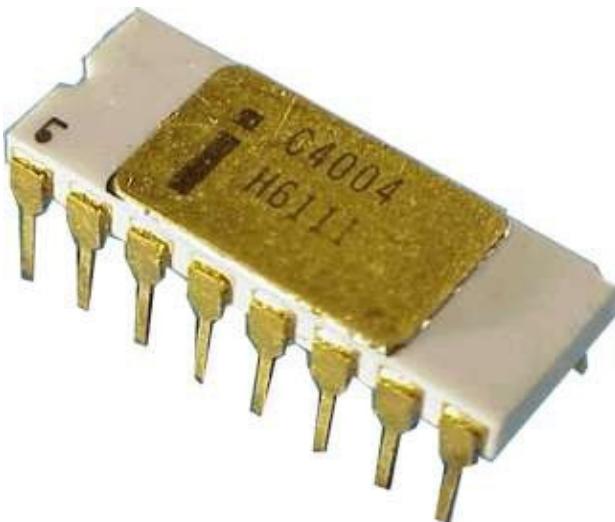
4-bit uP

Intel 4004

- Debuted in 1971
- 2,300 transistors
- 4-bit uP
- 740 KHz
- 640 bytes memory
- 60,000 instructions per second
- Costs \$200

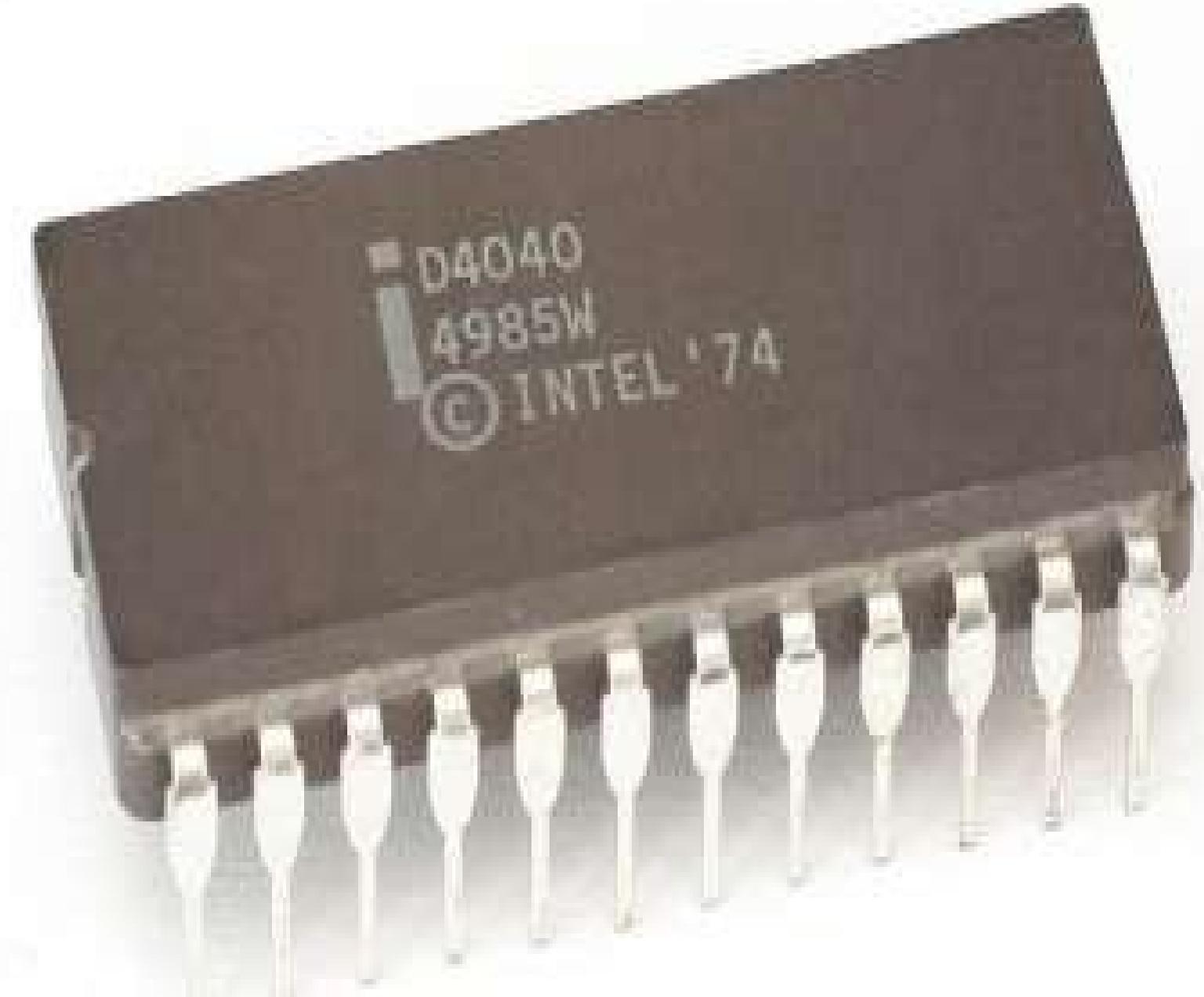
Smaller transistors allow

- More transistors per chip
- More processing per clock cycle
- Faster clock rates
- Smaller/cheaper chips



Intel 4040

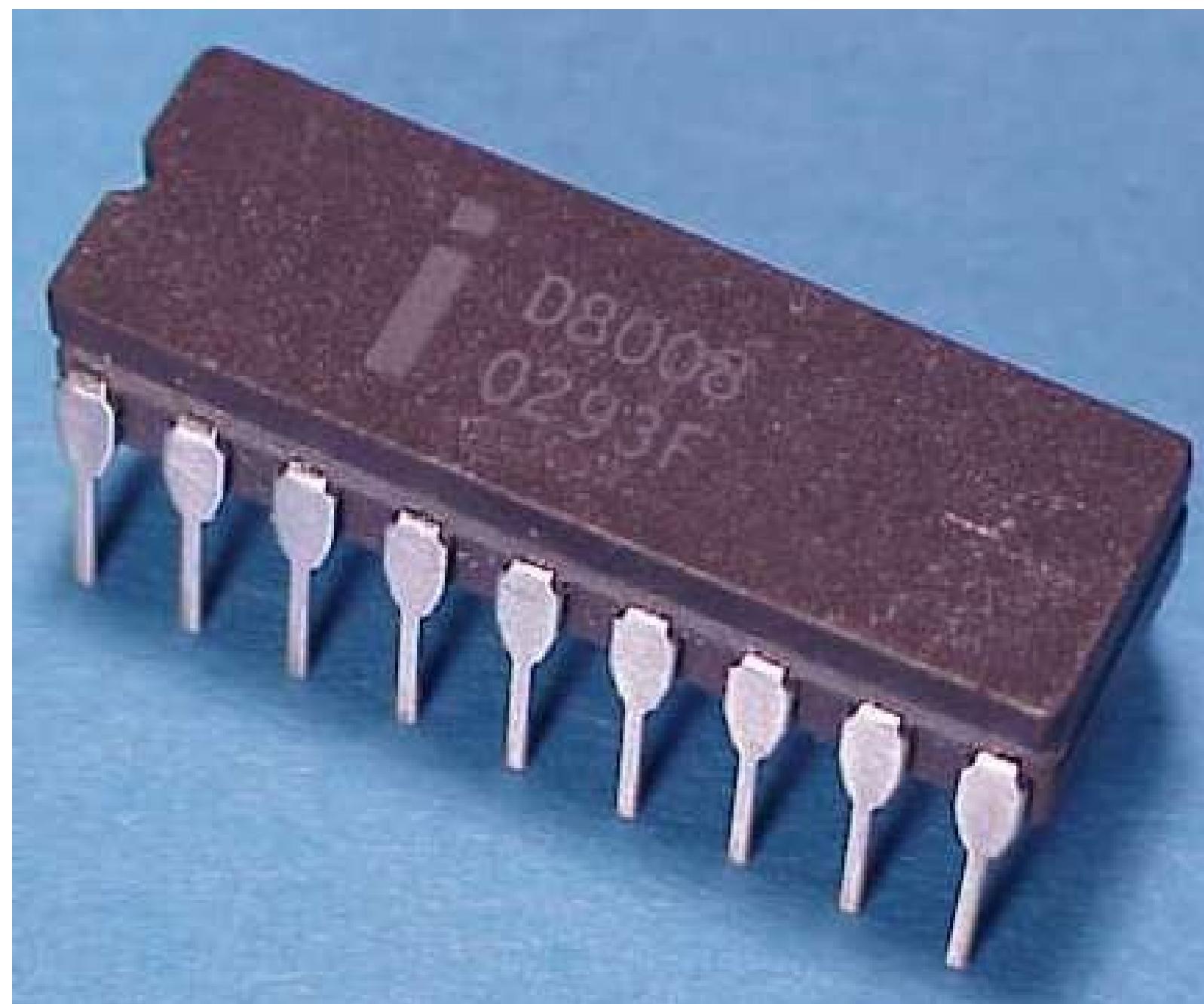
- Debuted in 1974
- Also a 4-bit uP



8-bit uP

Intel 8008

- Debuted in 1972
- First 8-bit uP
- 500 KHz clock speed
- 50,000 instructions per second



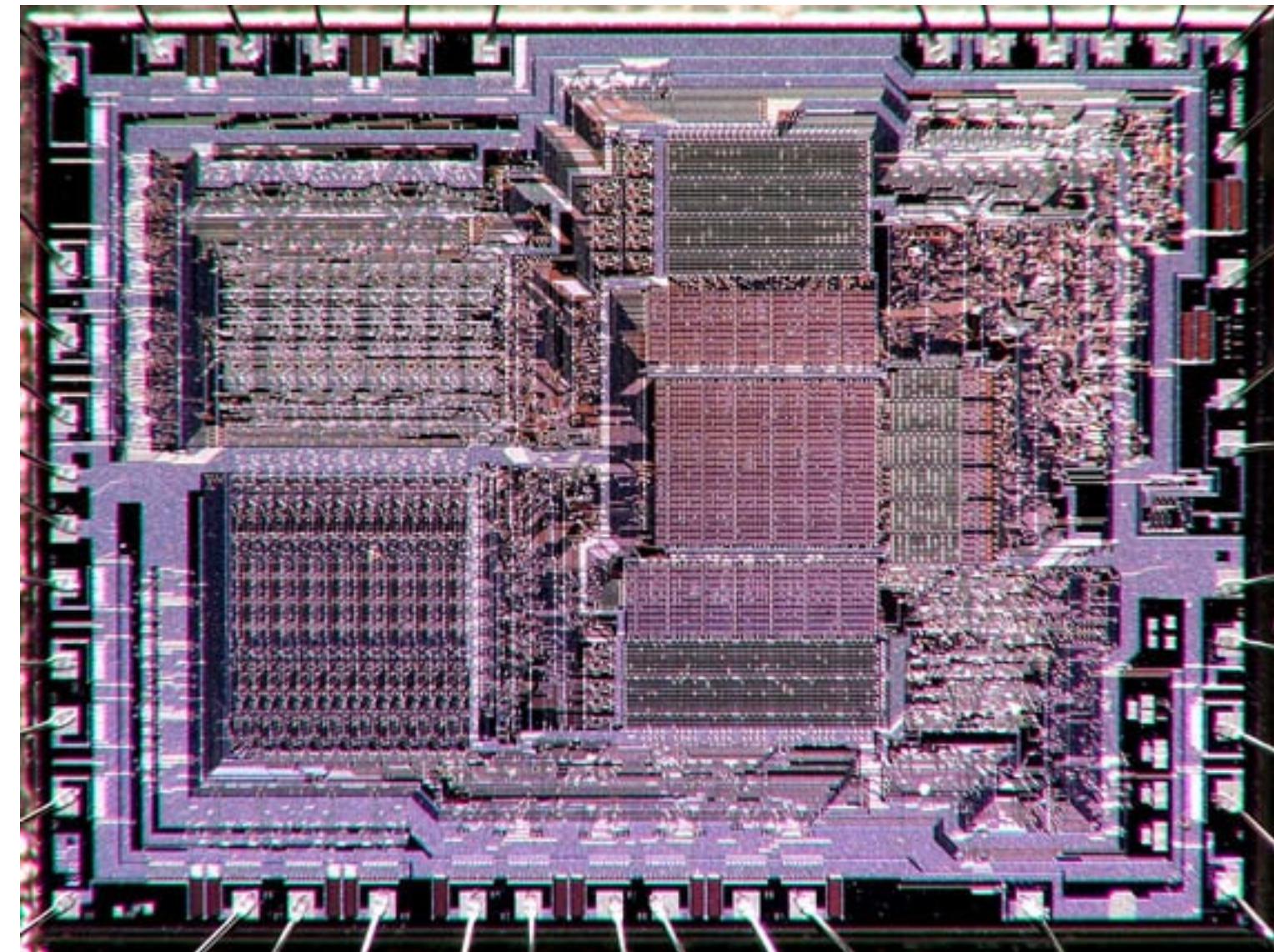
Intel 8080

- Debuted in 1974
- 6,000 transistors
- 8-bit uP
- 2 MHz clock speed
- 10x faster than 8008
- 500,000 instructions per second



Intel 8085

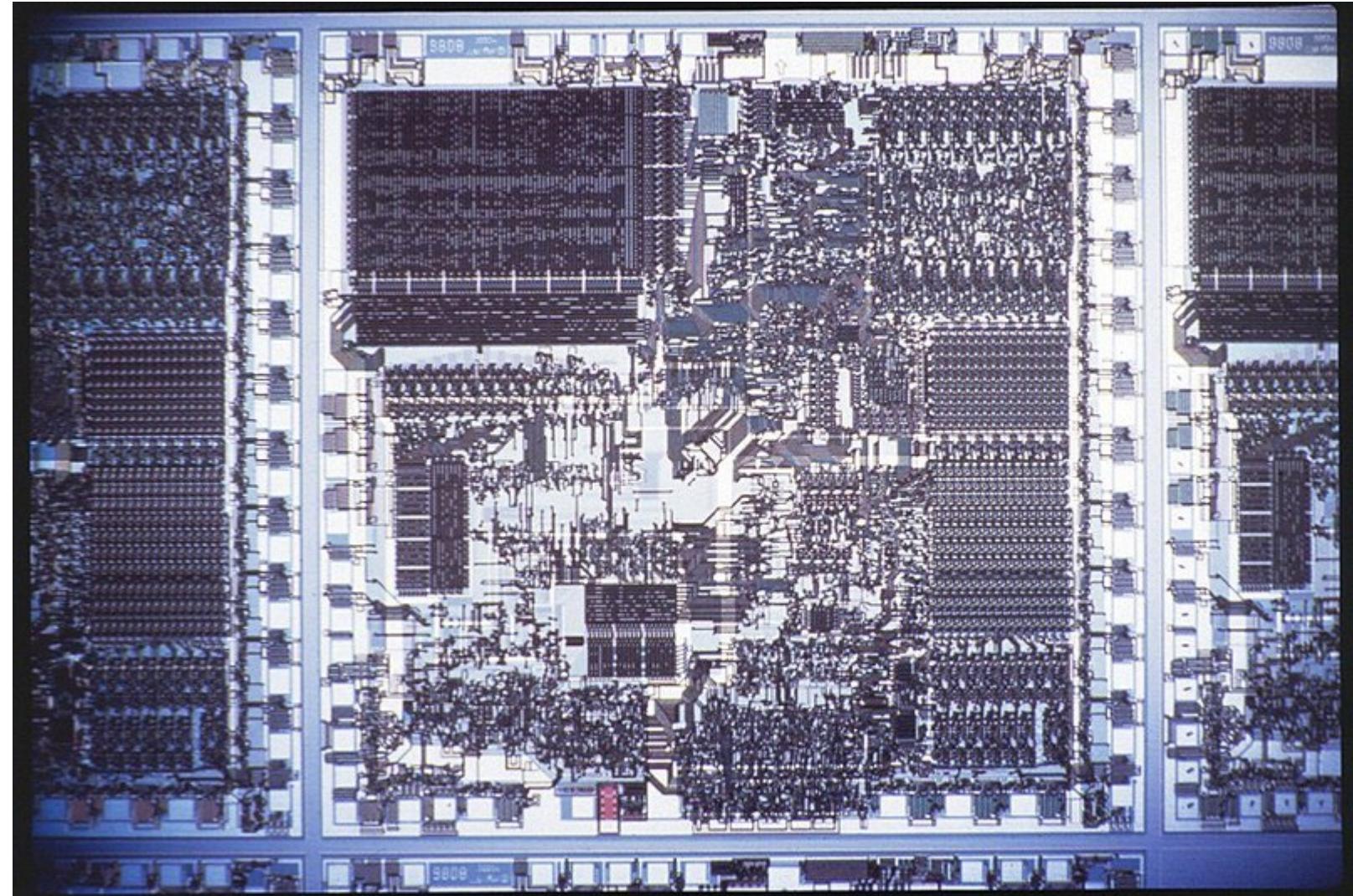
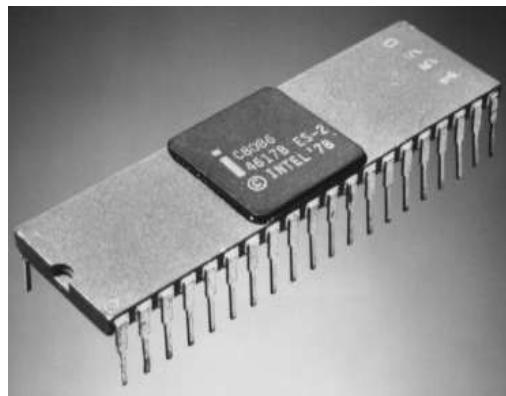
- Debuted in 1976
- 6,000 transistors
- 8-bit uP
- 3 MHz clock speed
- 8-bit data bus
- 16-bit address bus
- 64 KB memory
- 246 instructions
- 769,230 instructions per second



16-bit uP

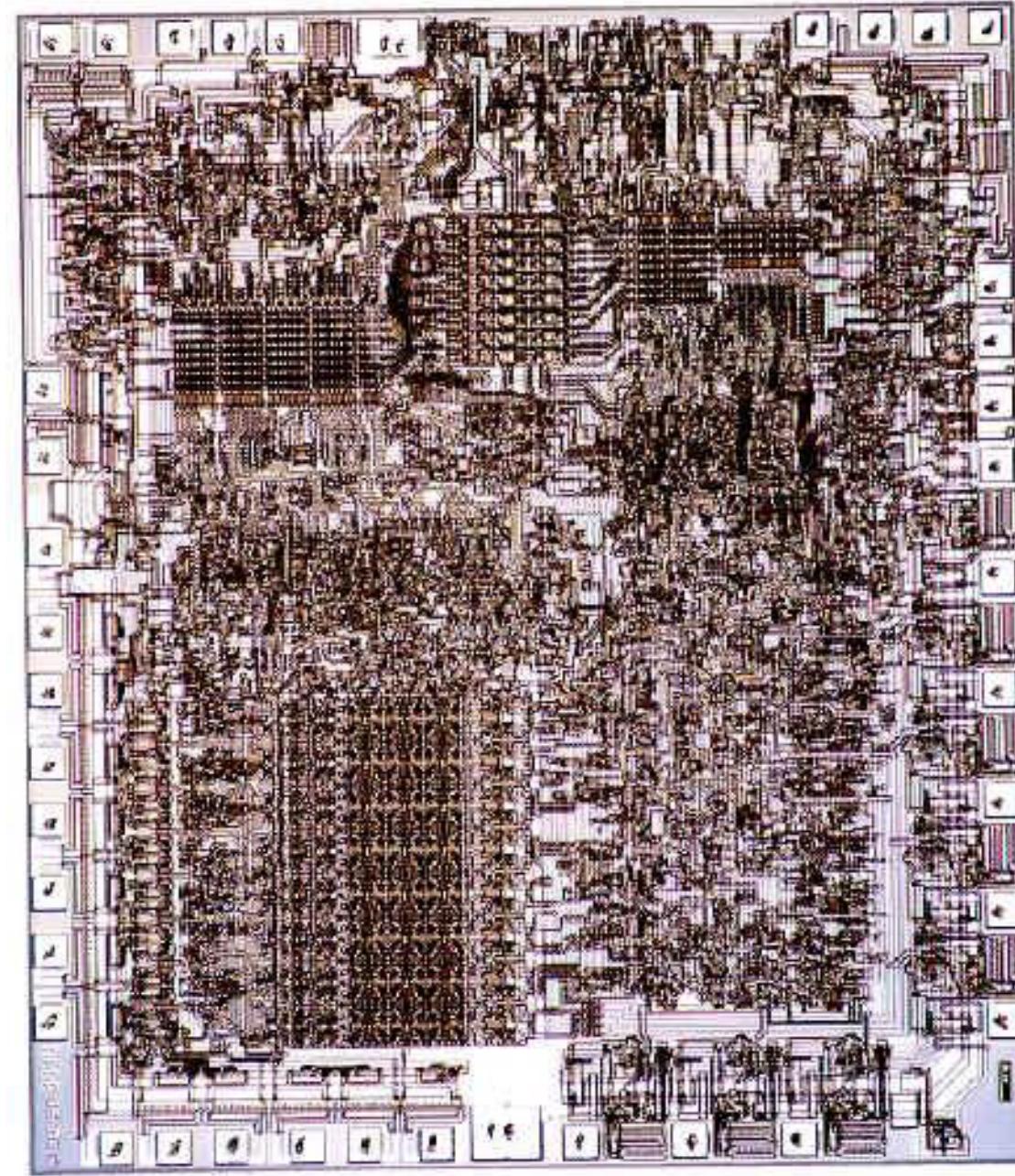
Intel 8086

- Debuted in 1978
- 29,000 transistors
- 16-bit uP
- 4.77, 8.00 and 10.00 MHz clock speeds
- 16-bit data bus
- 20-bit address bus
- 1 MB of memory
- 22,000 instructions
- 2.5 M instructions per second
- Had MUL and DIV instructions



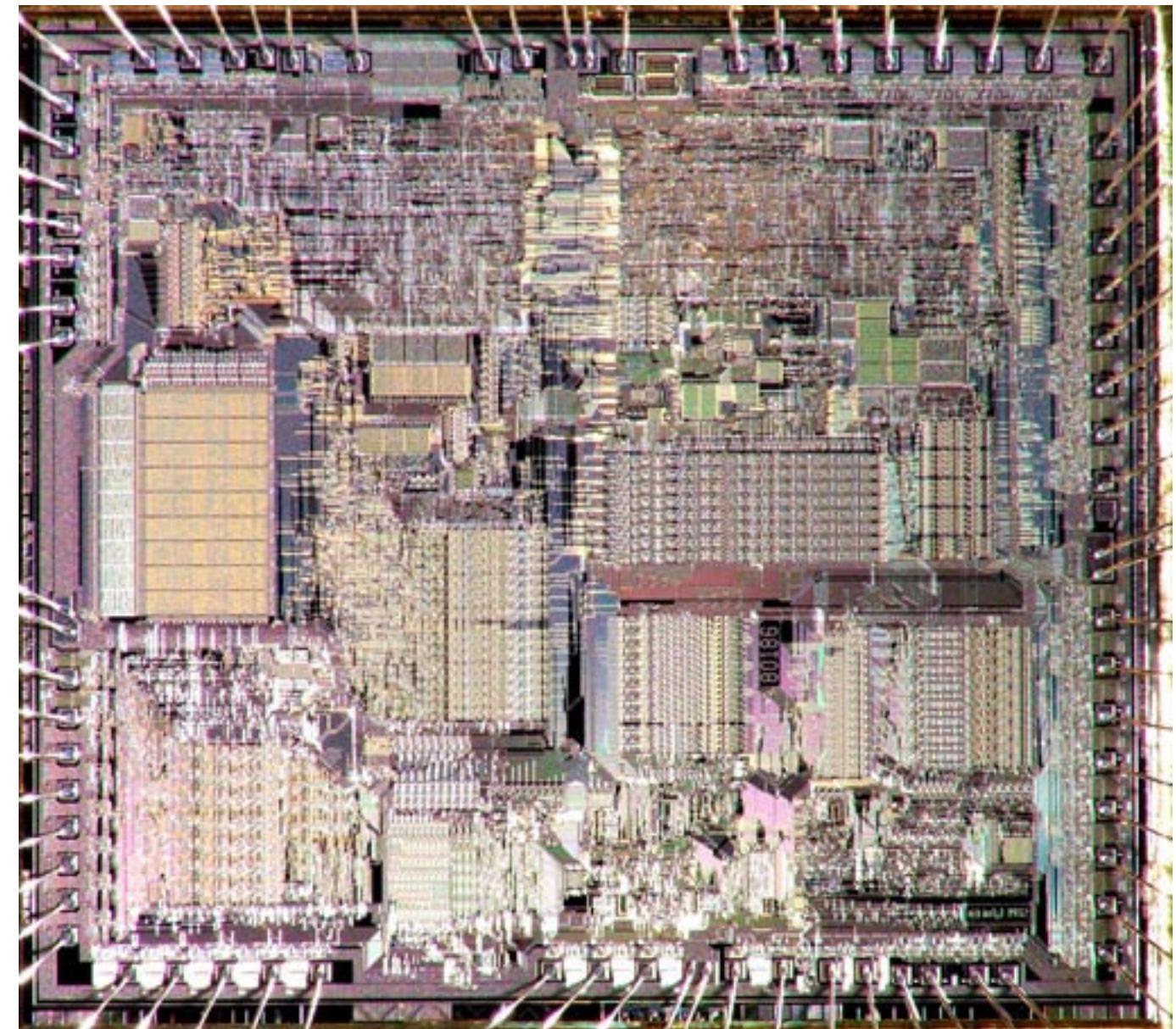
Intel 8088

- Debuted in 1979
- 16-bit uP
- 8-bit external bus
- Cheaper version of 8086



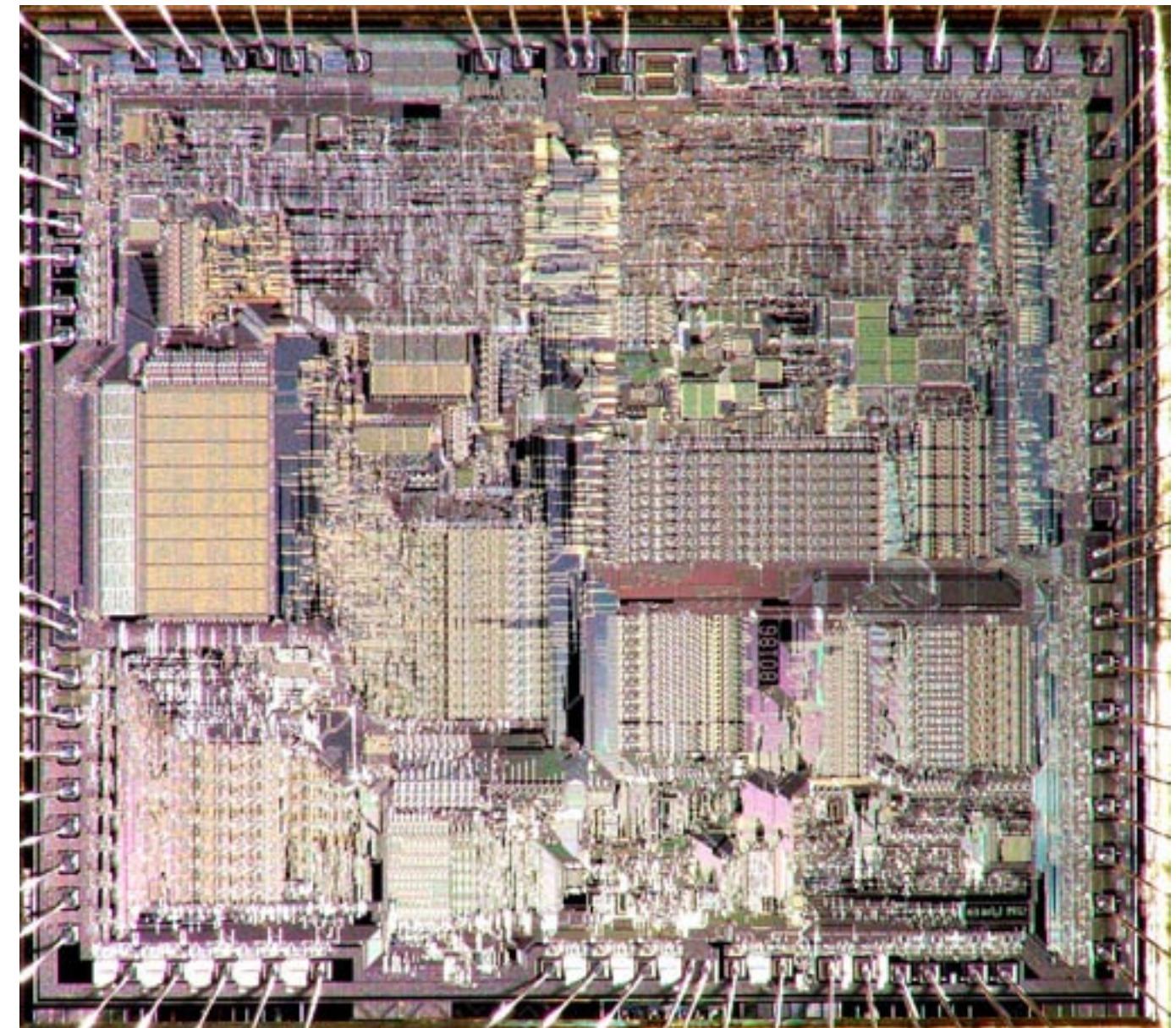
Intel 80186 and 80188

- Debuted in 1982
- 16-bit uPs
- 6 MHz clock speed



Intel 80286

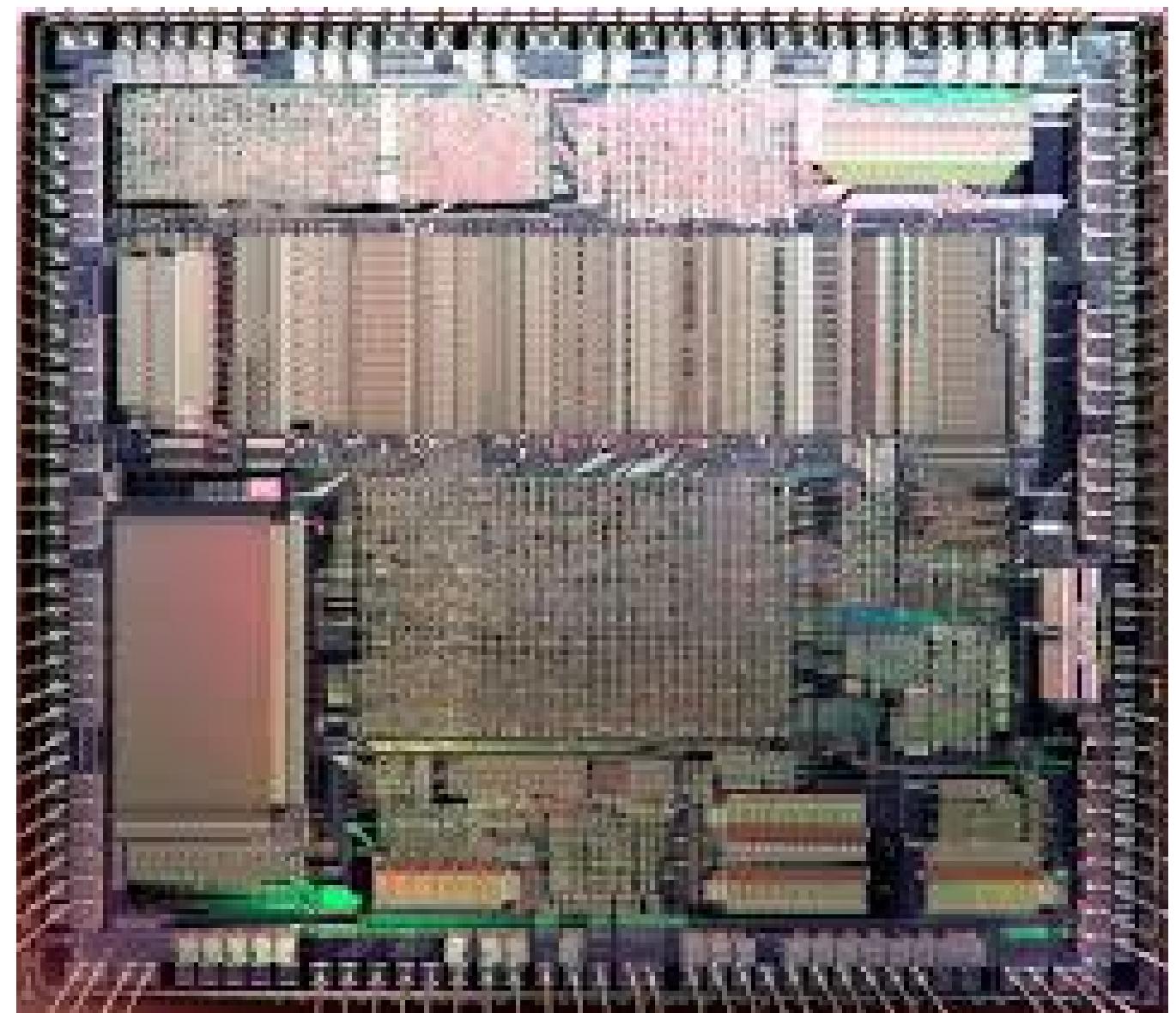
- Debuted in 1982
- 16-bit uP
- 8 MHz clock speed



32-bit uP

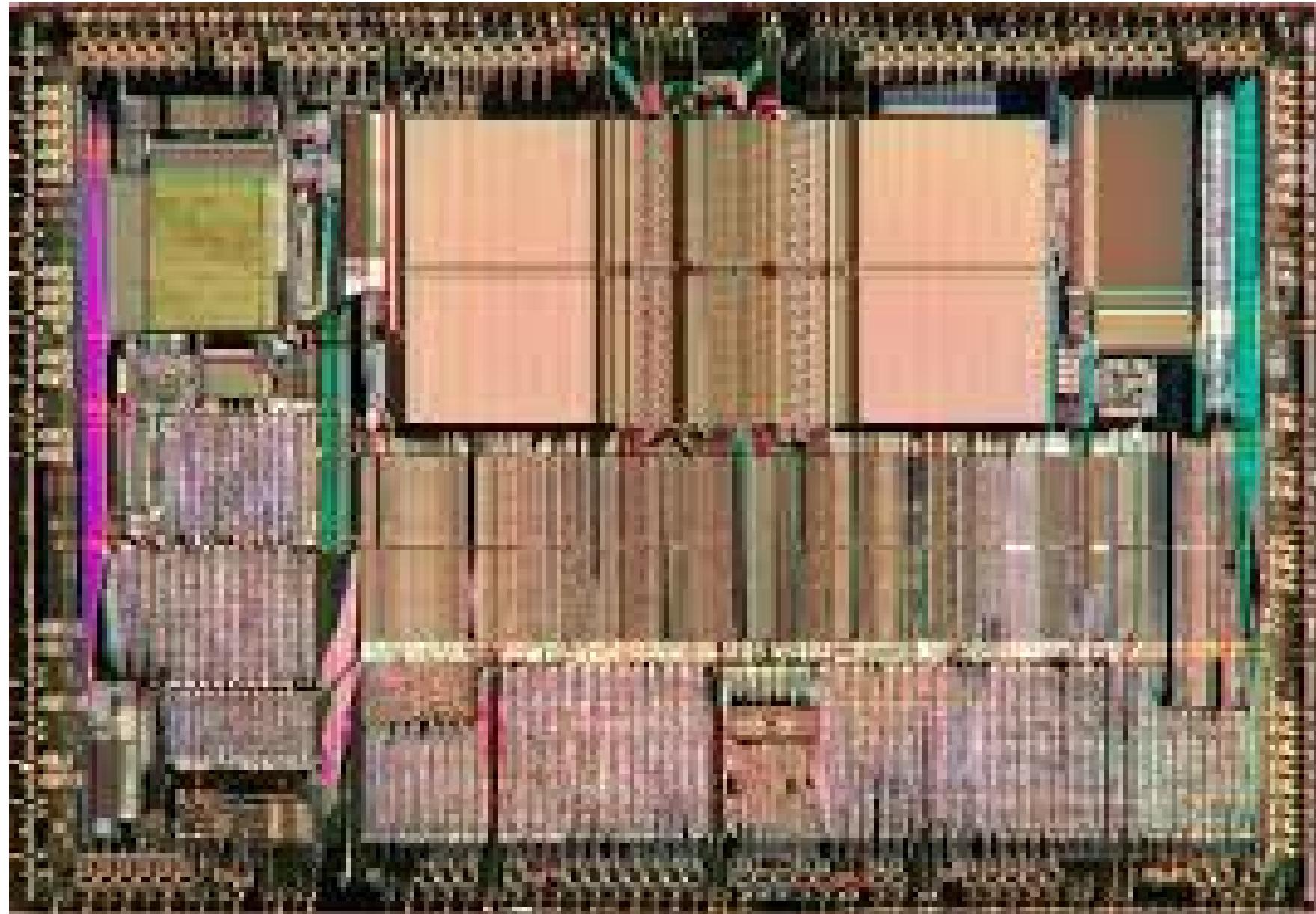
Intel 80386

- Debuted in 1986
- First 32-bit uP
- 32-bit data bus
- 32-bit address bus
- 4 GB memory



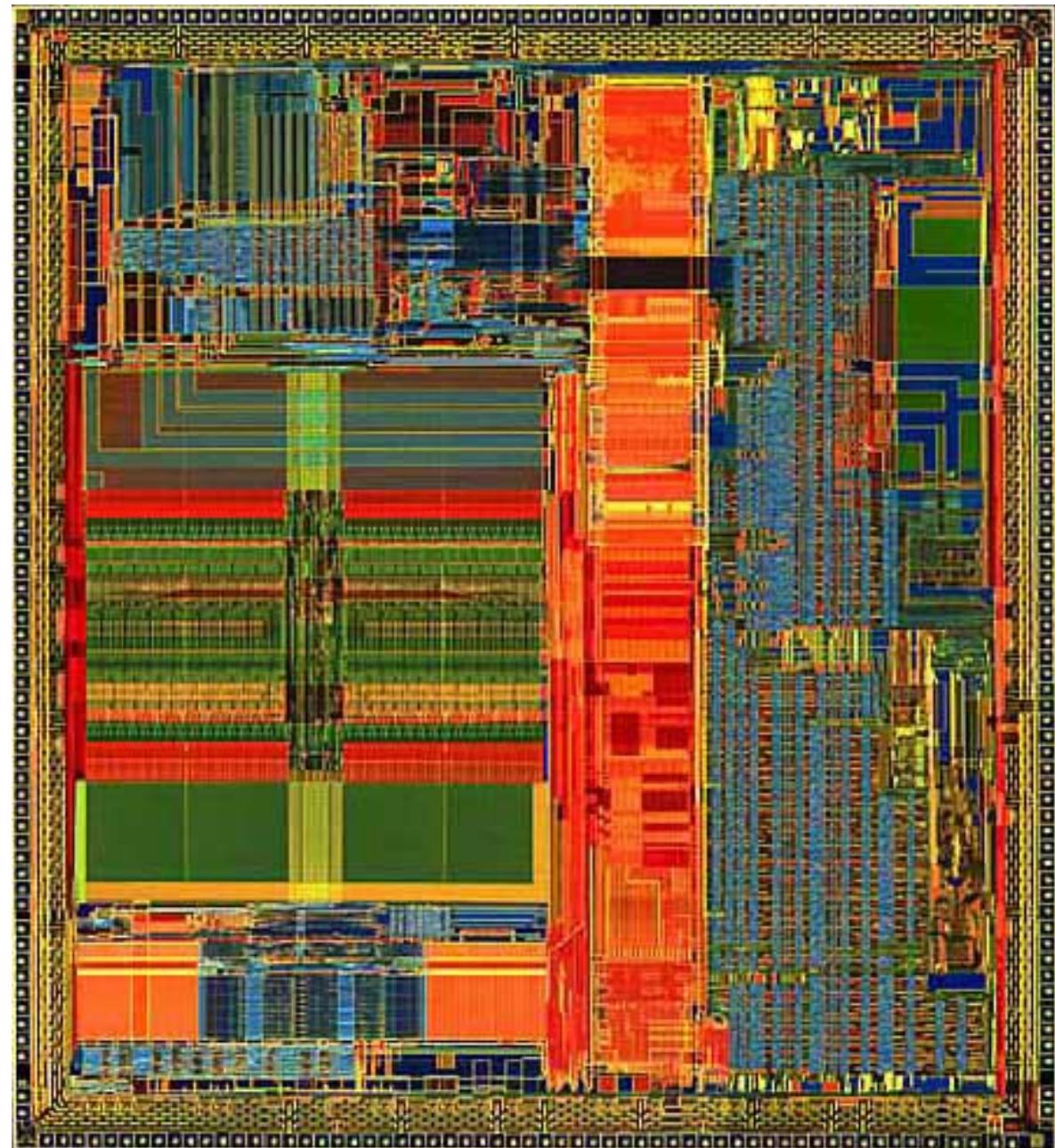
Intel 80486

- Debuted in 1989
- 32-bit uP
- 1.2 M transistors
- 16 to 100 MHz clock speed



Intel Pentium

- Debuted in 1993
- 32-bit uP
- Originally name 80586
- 66 MHz



Intel Pentium Pro

- Debuted 1995
- 32-bit uP
-



Intel Pentium II

- Debuted in 1997
- 32-bit uP



Intel Pentium II Xeon

- Debuted in 1998
- 32-bit uP



Intel Pentium III

- Debuted in 1999
- 32-bit uP



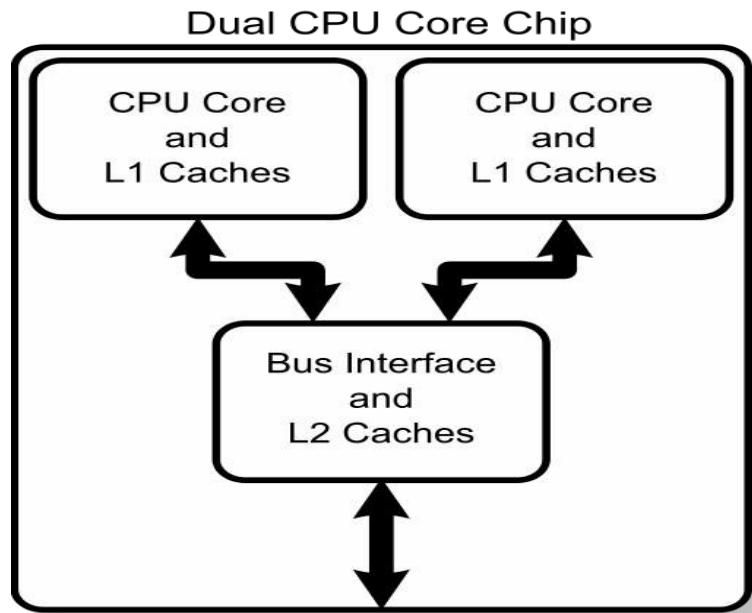
Intel Pentium IV

- Debuted in 2000
- 32-bit uP



Intel Dual Core

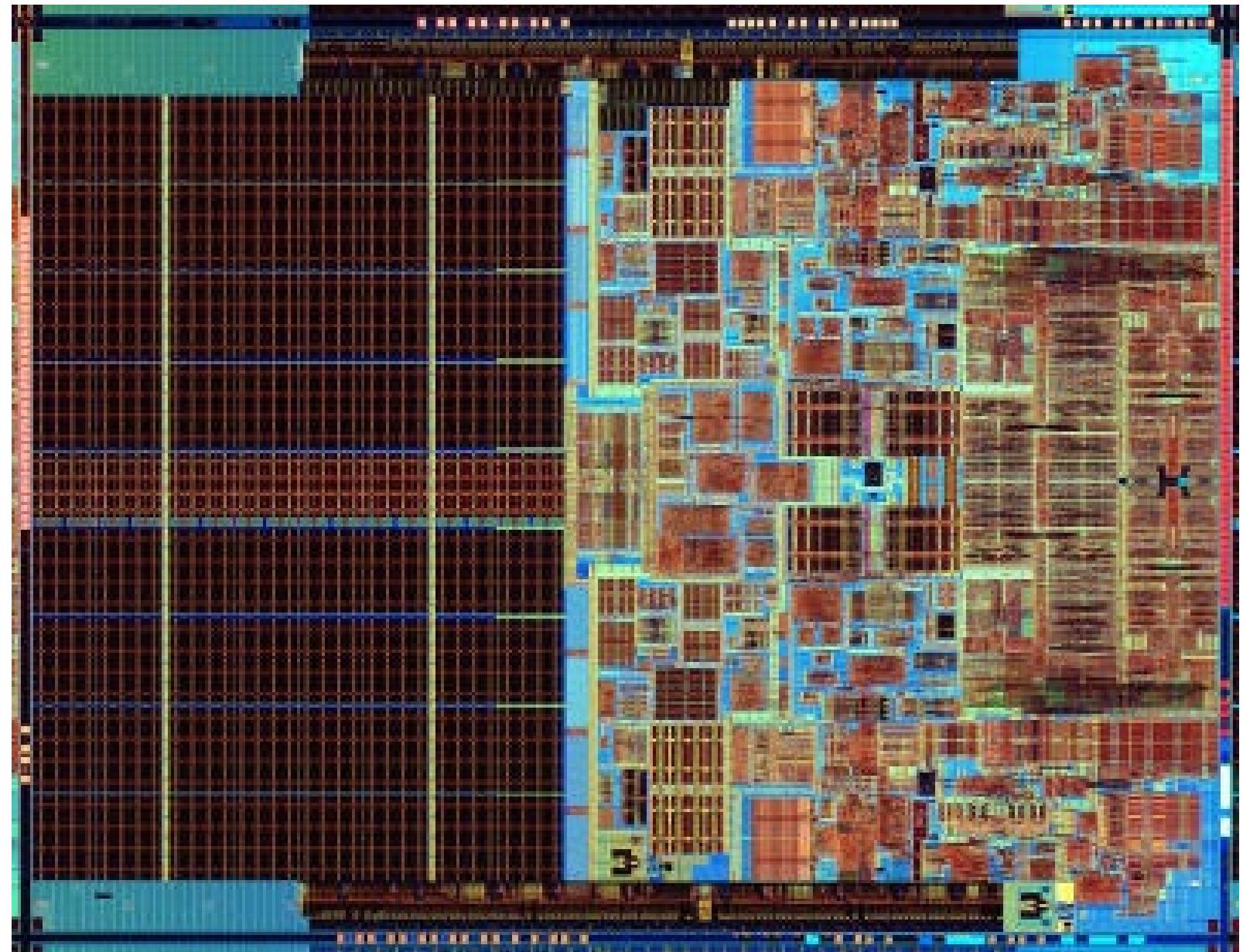
- Debuted in 2006
- 32-bit or 64-bit uP
- With two cores
- Each core with own internal bus and L1 cache
- Shares external bus and L2 cache



64-bit uP

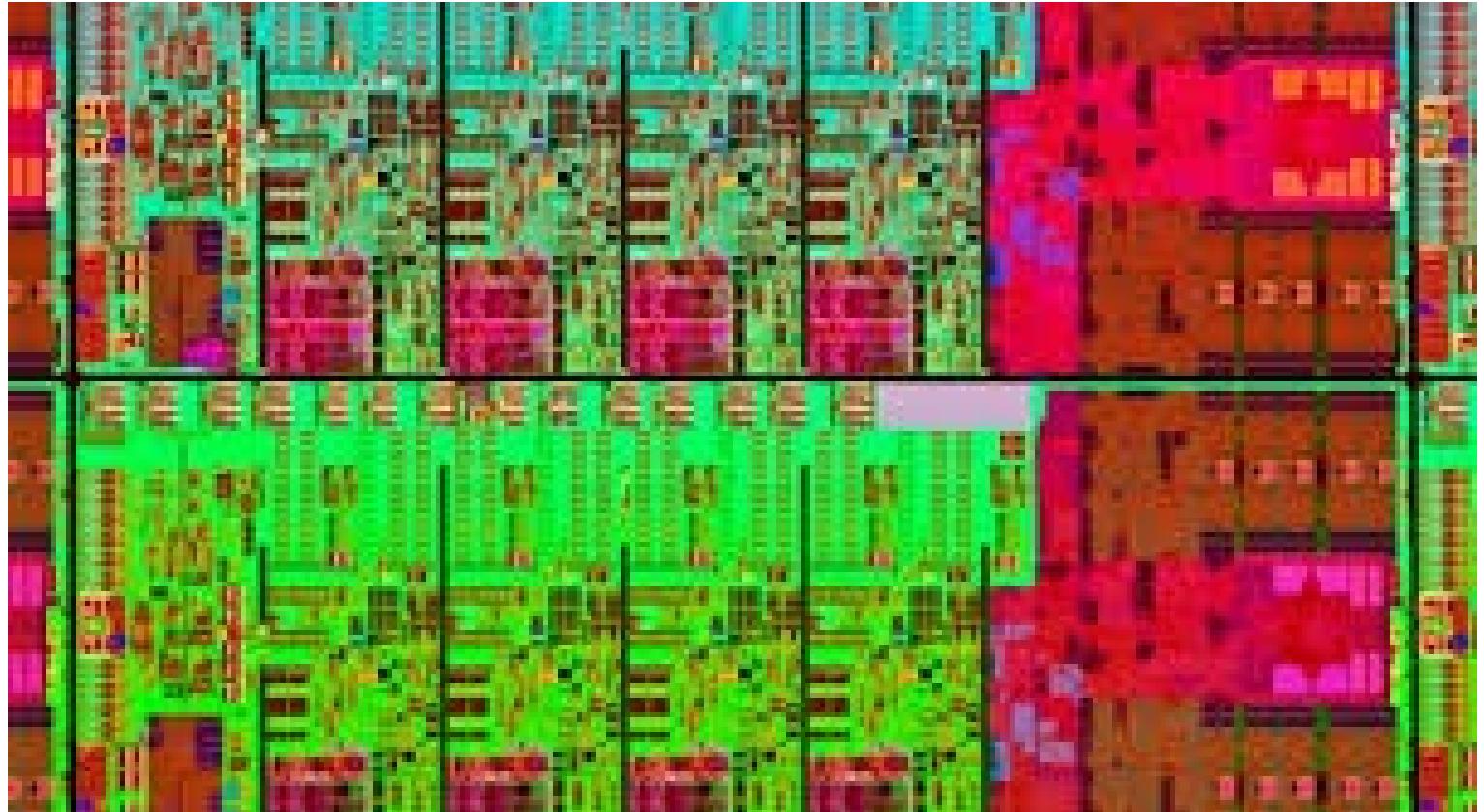
Intel Core 2 Duo

- Debuted in 2006
- 64-bit uP
- 4M cache
- 1.86 GHz



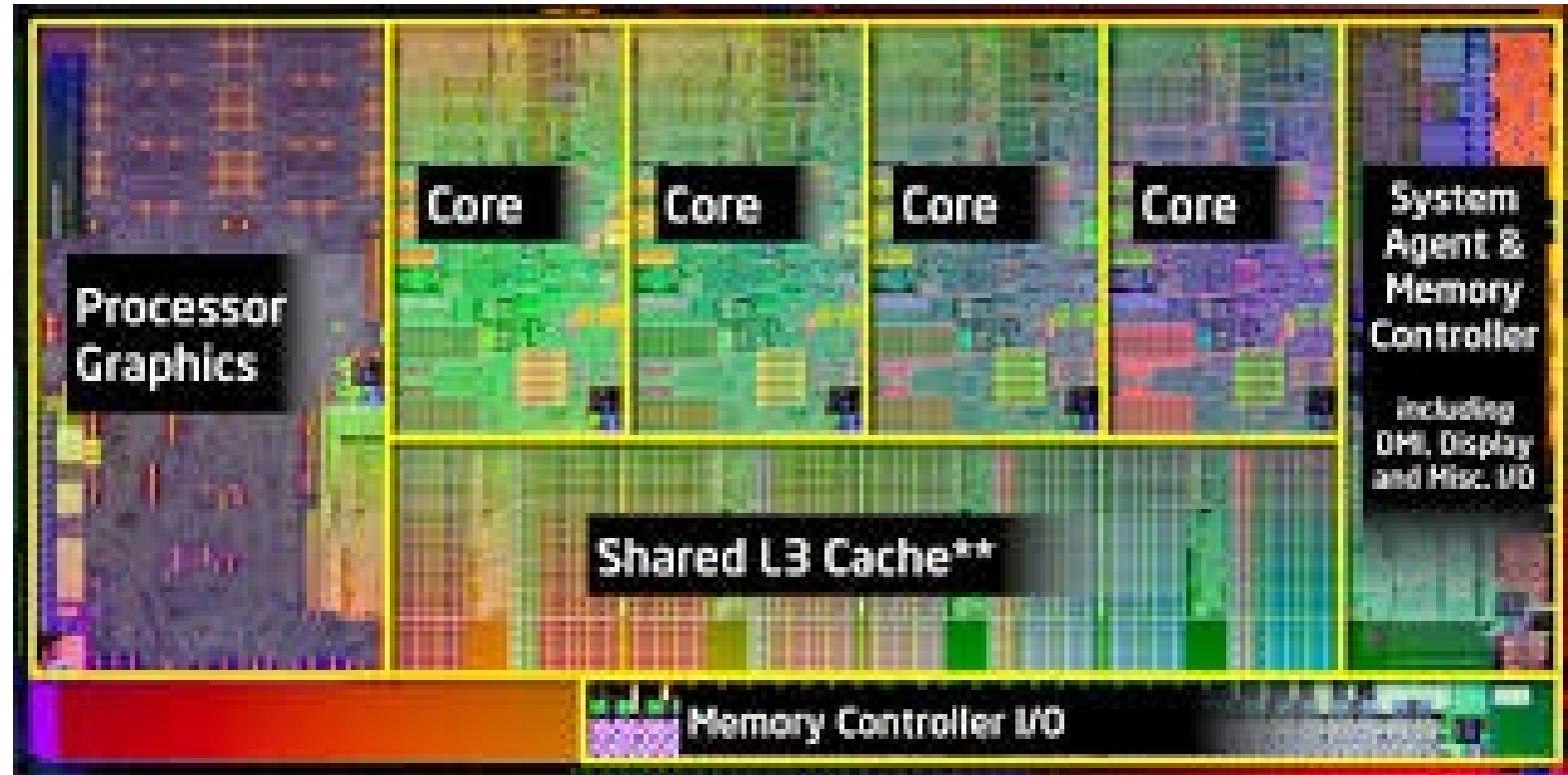
Intel Core i7

- Debuted in 2008
- 64-bit uP
- 6 original + 6 virtual cores
- For video editors, designers and gamers who crave power



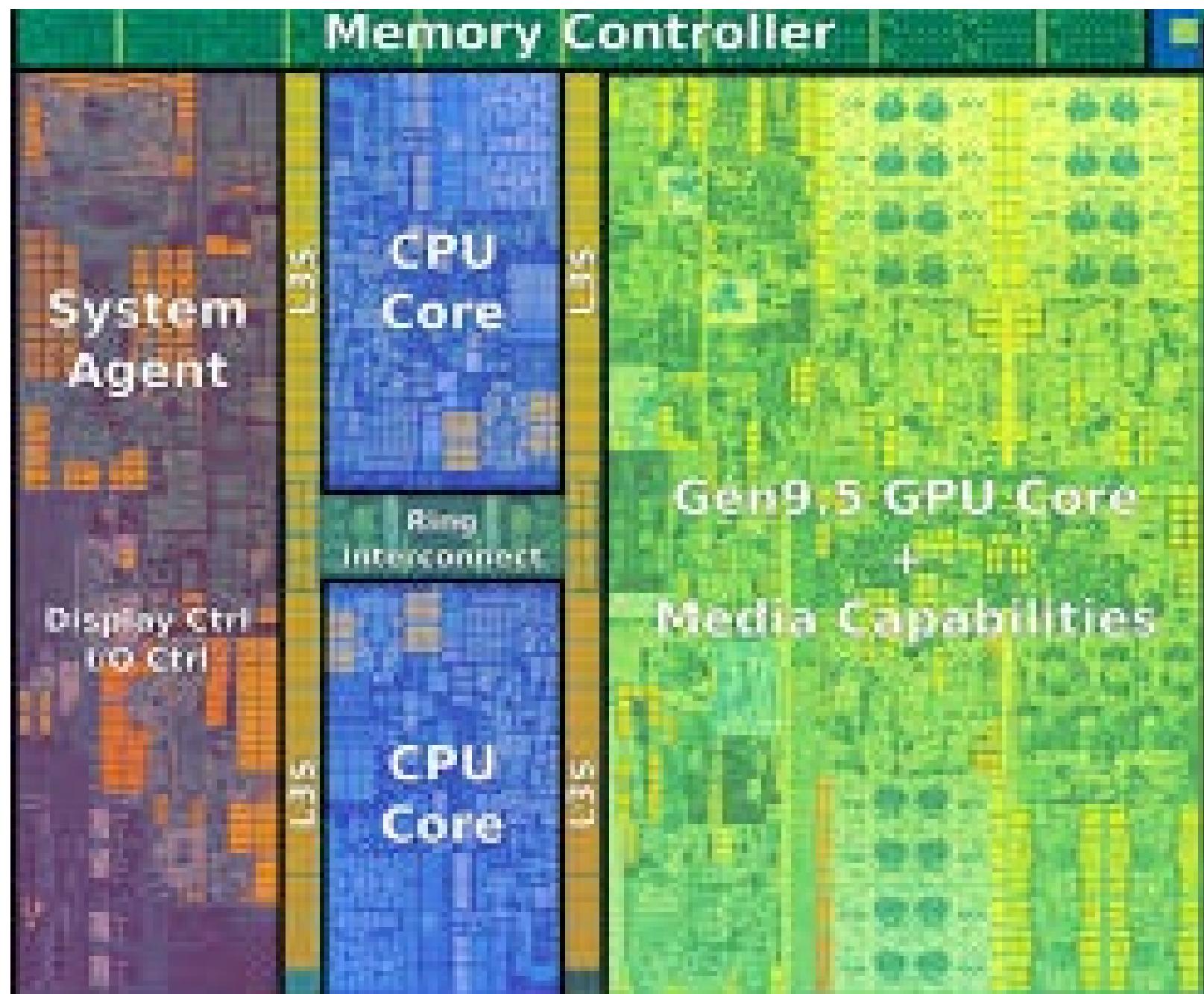
Intel Core i5

- Debuted in 2009
- 64-bit uP
- 6 cores
- Home and business use – busy multitaskers and Adobe-using creatives



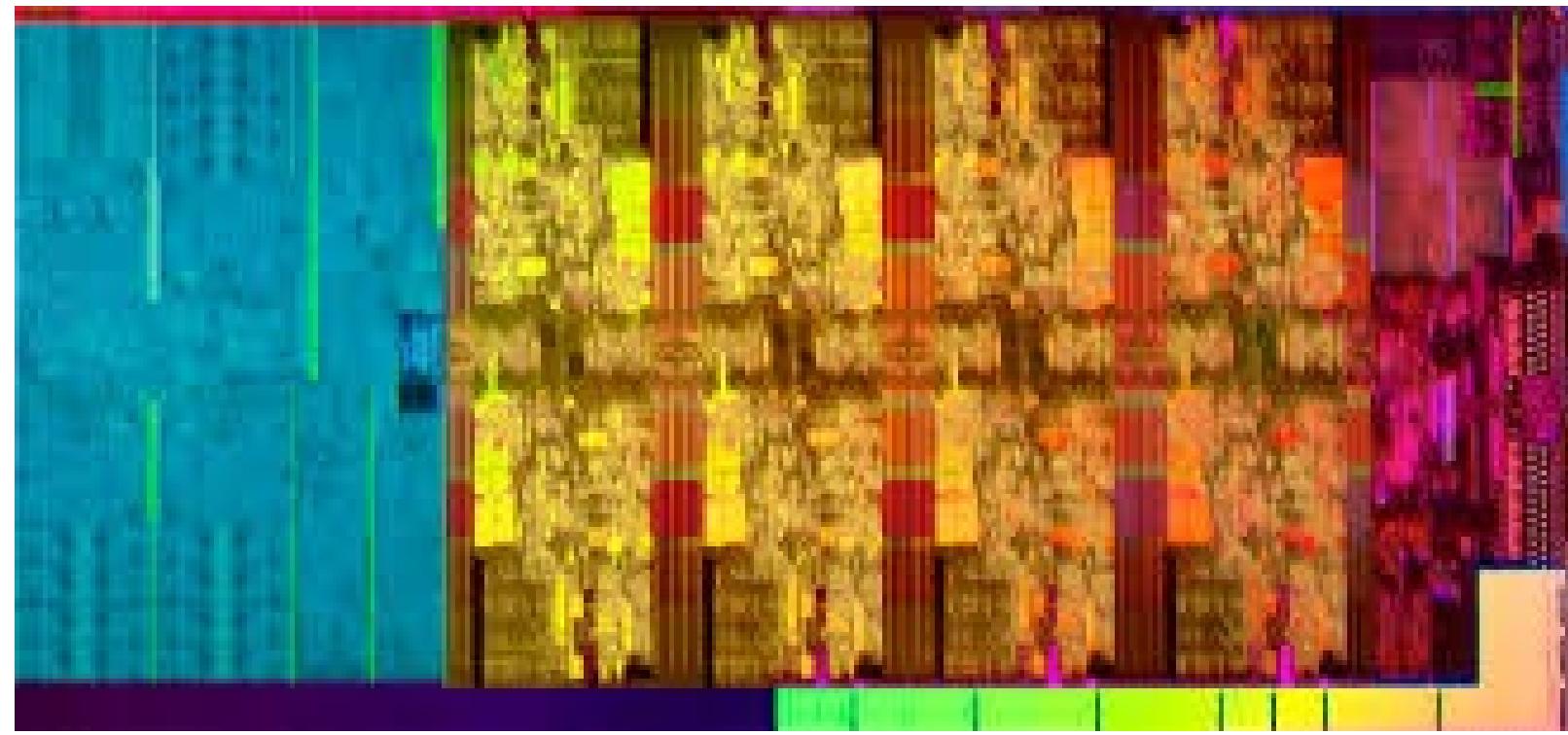
Intel Core i3

- Debuted in 2010
- 64-bit uP
- 3M cache
- 2.13 GHz
- Up to 4 cores
- For everyday users – web browsing, Word and media streaming

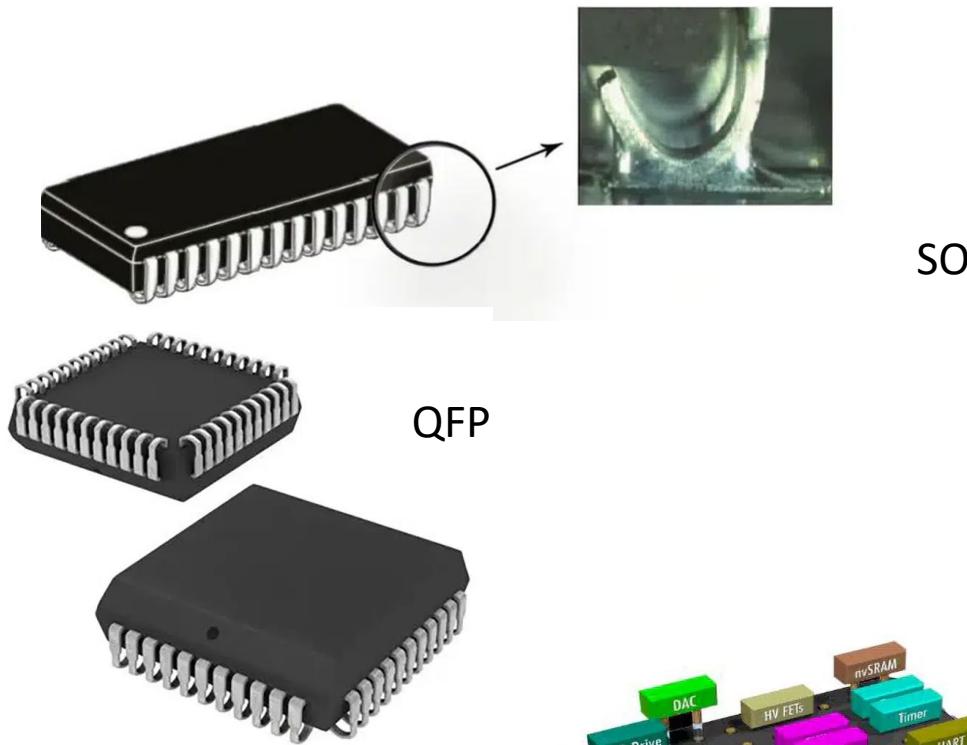


Intel Core i9

- Debuted 2017
- 64-bit uP
- 3.3 GHz
- 13.75 MB L3 cache
- 10 to 18 cores and 36 threads
- For extreme gaming, mega tasking and high end content creation

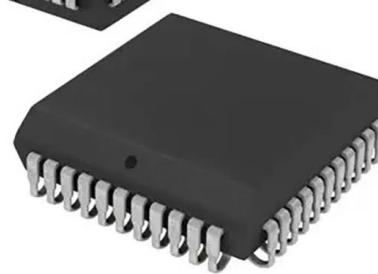


Package Type	Full Name	Time
DIP	Dual In-line Package	Before the 1980s
SOP	Small Out-line Package	1980s
QFP	Quad Flat Package	1995-1997
TAB	Tape Automated Bonding	1995-1997
COB	Chip on Board	1996-1998
CSP	Chip Scale Package	1998-2000
FC	Flip Chip	1999-2001
MCM/CSP/SIP	Multi-Chip Model	2000-present
WLCSP/TSV	Wafer Level Chip Scale Packaging	2000-present



SOJ

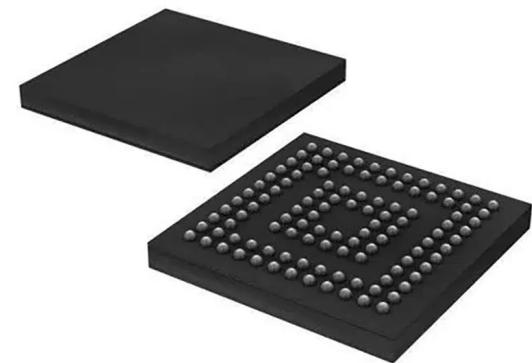
QFP



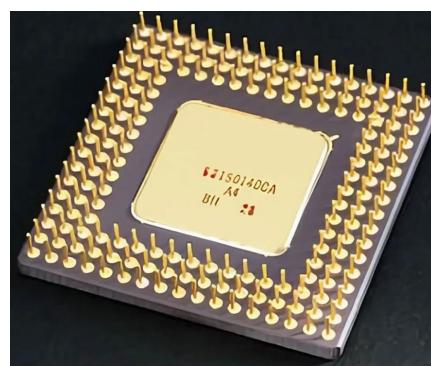
LGA



SOC

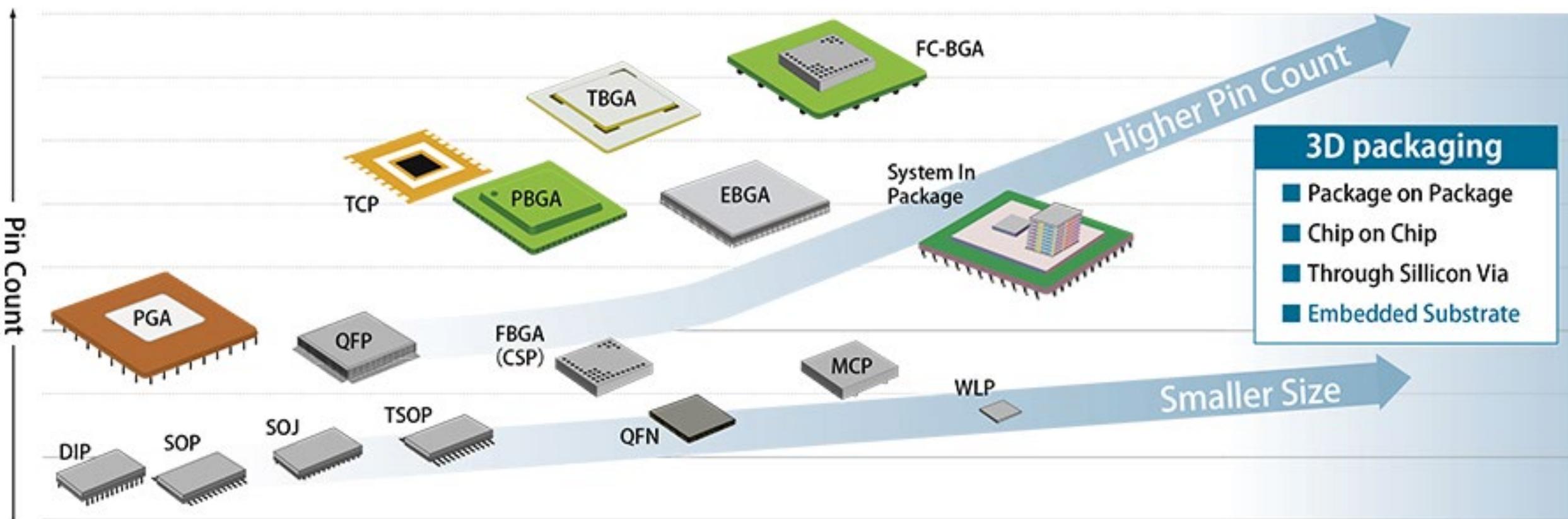


BGA



PGA

SEMICONDUCTOR PACKAGES



8086 Real and Virtual Modes of Operation

Real, Virtual Mode

- 8086 microprocessor represents the foundation upon which all the 80x86 family of processors have been built
- Intel has made a commitment that as new generations of microprocessors are developed, each will maintain software compatibility with its first generation part
- Hence, programs running on Intel 80386 microprocessor can run on a Pentium
- This is called **Upward Compatibility**
- To run older version programs in newer generation microprocessors, Intel employed the following modes of operation:
 - Real Mode
 - Virtual Mode
 - Protected Mode

Real Mode

- Only one program can be run at one time
- All of the protection and memory management functions are turned off
- Memory space is limited to 1 MB

Virtual 8086 Mode

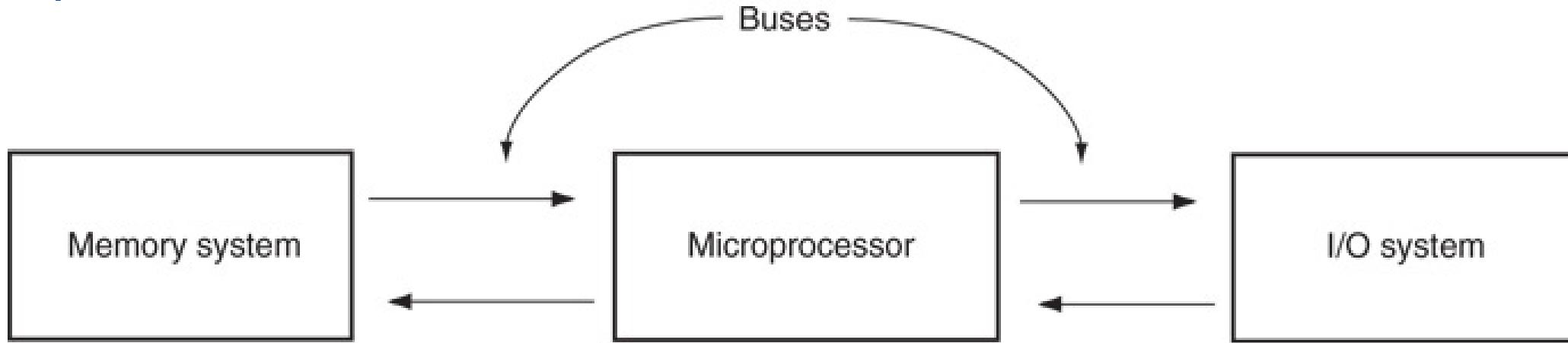
- 80386 had each real mode program its own 1MB chunk of memory
- Multiple 8086 programs to be run simultaneously but protected from each other, employs time sharing
- Due to time sharing, the response becomes much slower as each new program is launched
- 80386 can be operated in Protected and Virtual 8086 mode at the same time

Protected Mode

- Employs new addressing mechanism and protection levels
- Each memory segment ranges from a single byte to 4GB

Internal Microprocessor Architecture

Basic Bus System Architecture

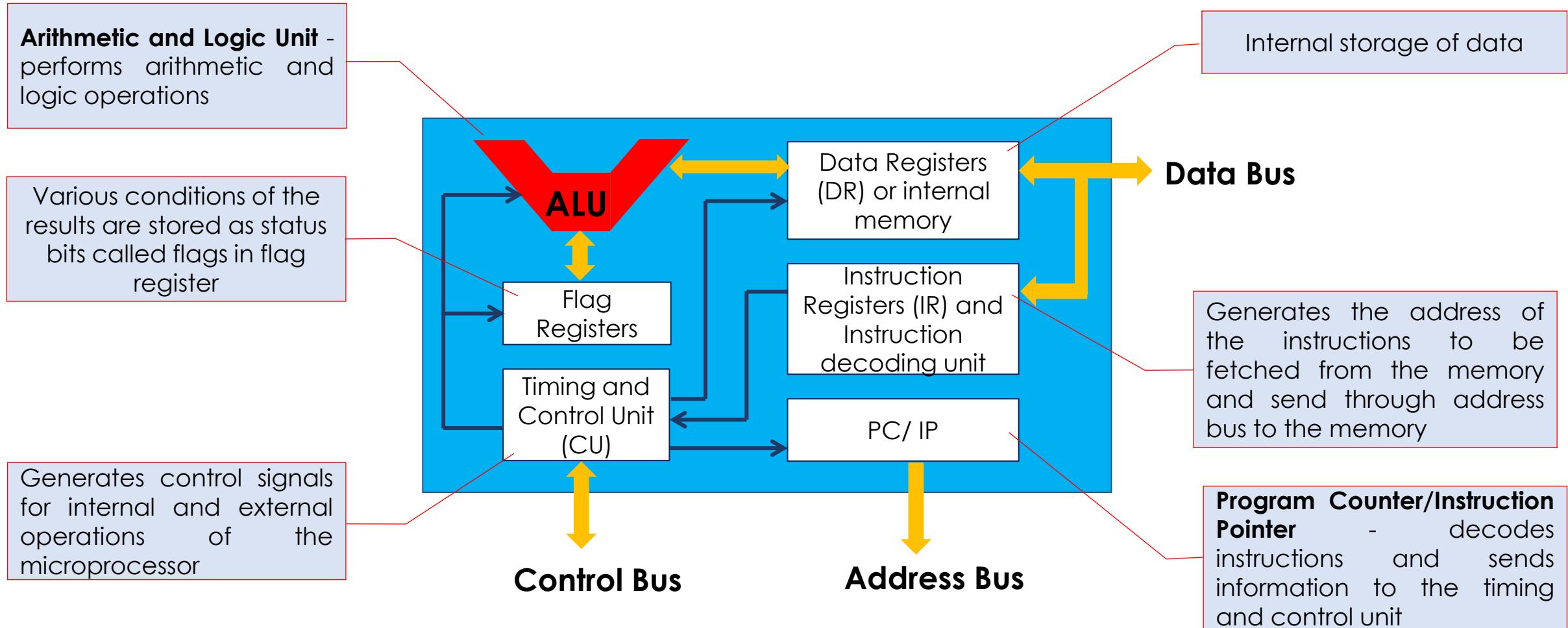


Dynamic RAM (DRAM)
Static RAM (SRAM)
Cache
Read-only (ROM)
Flash memory
EEPROM
SDRAM
RAMBUS
DDR DRAM

8086
8088
80186
80188
80286
80386
80486
Pentium
Pentium Pro
Pentium II
Pentium III
Pentium 4
Core2

Printer
Serial communications
Floppy disk drive
Hard disk drive
Mouse
CD-ROM drive
Plotter
Keyboard
Monitor
Tape backup
Scanner
DVD

Microprocessor Functional Bblocks



Fetch-Decode-Execute Cycle

Fetch-Decode-Execute (FDE) Cycle

Fetch the instruction (Fetch Cycle)

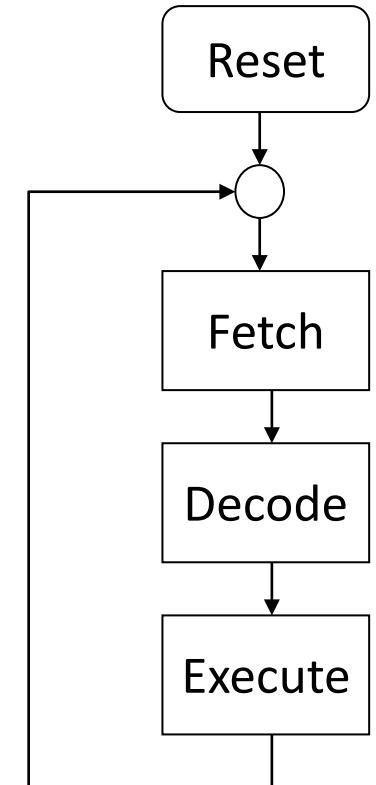
- In the beginning of the fetch cycle, the content of the program counter (PC), which is the address of the memory location where opcode is available, is sent to the memory.
- The memory puts the opcode on the data bus so as to transfer it to the CPU.
- The whole operation of fetching an opcode takes three clock cycles.
- A slow memory may take more time.

Decode the instruction (Decode Cycle)

- The opcode fetched from the memory goes to the **data register**, DR and then to **instruction register**, IR.
- From the IR it goes to the decoder circuitry which decodes the instruction.
- Decoder circuitry is within the microprocessor.

Execute the Instruction (Execute Cycle)

- After the instruction is decoded, execution begins.
- If the operand is reside the general purpose registers, execution is immediately performed.
- The time taken in decoding and execution of an instruction is one clock cycle.
- In some situations, an execute cycle may involve one or more **read** or **write cycles** or both.



Fetch-Decode-Execute (FDE) Cycle

Read Cycle:

- If an instruction contains data or operand address which are in the memory, the CPU has to perform some read operations to get the desired data.
- In case of a read cycle the instruction received from the memory are data or operand address instead of an opcode.

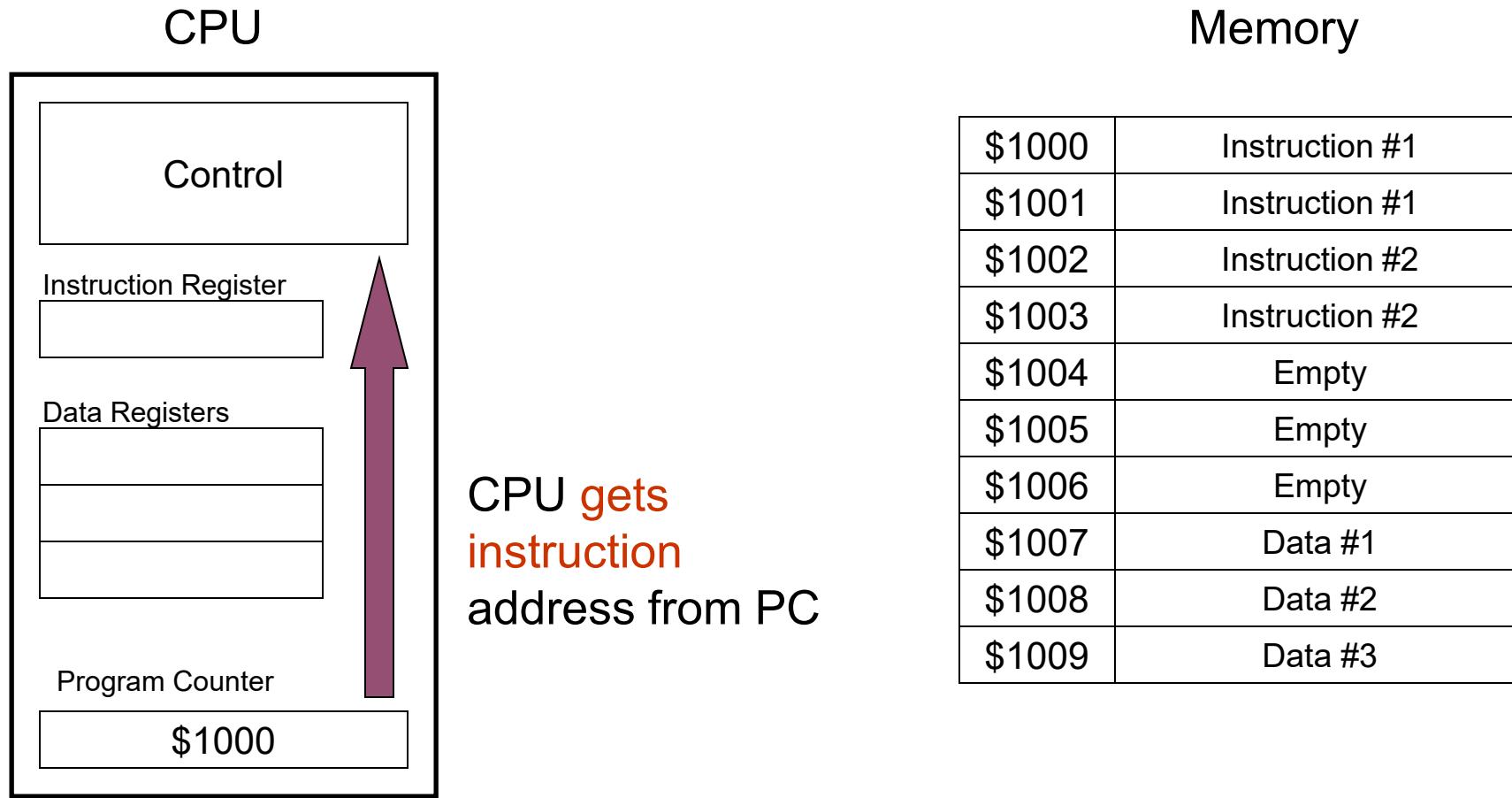
Write Cycle:

- In write cycle data are sent from the CPU to the memory or an output device.

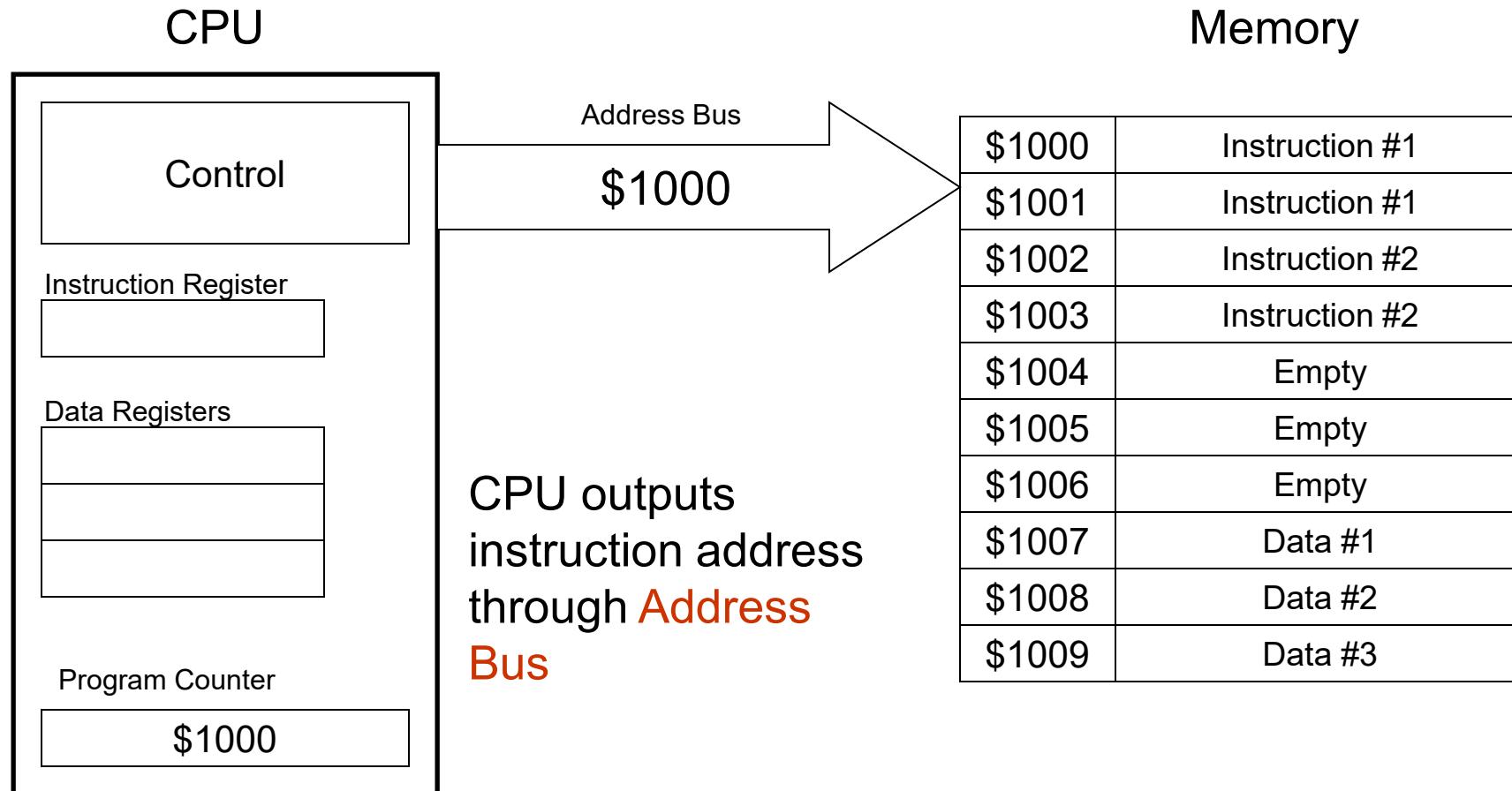
Machine Cycle and State

- The necessary steps carried out to perform the operation of accessing either memory or input output device, constitute a machine cycle.
- In other words, necessary steps carried out to perform a fetch, a read or a write operation constitutes a machine cycle.
- One sub-division of an operation performed in one clock cycle is called a state or T-state. In short, one clock cycle of the system clock is referred to as a state.

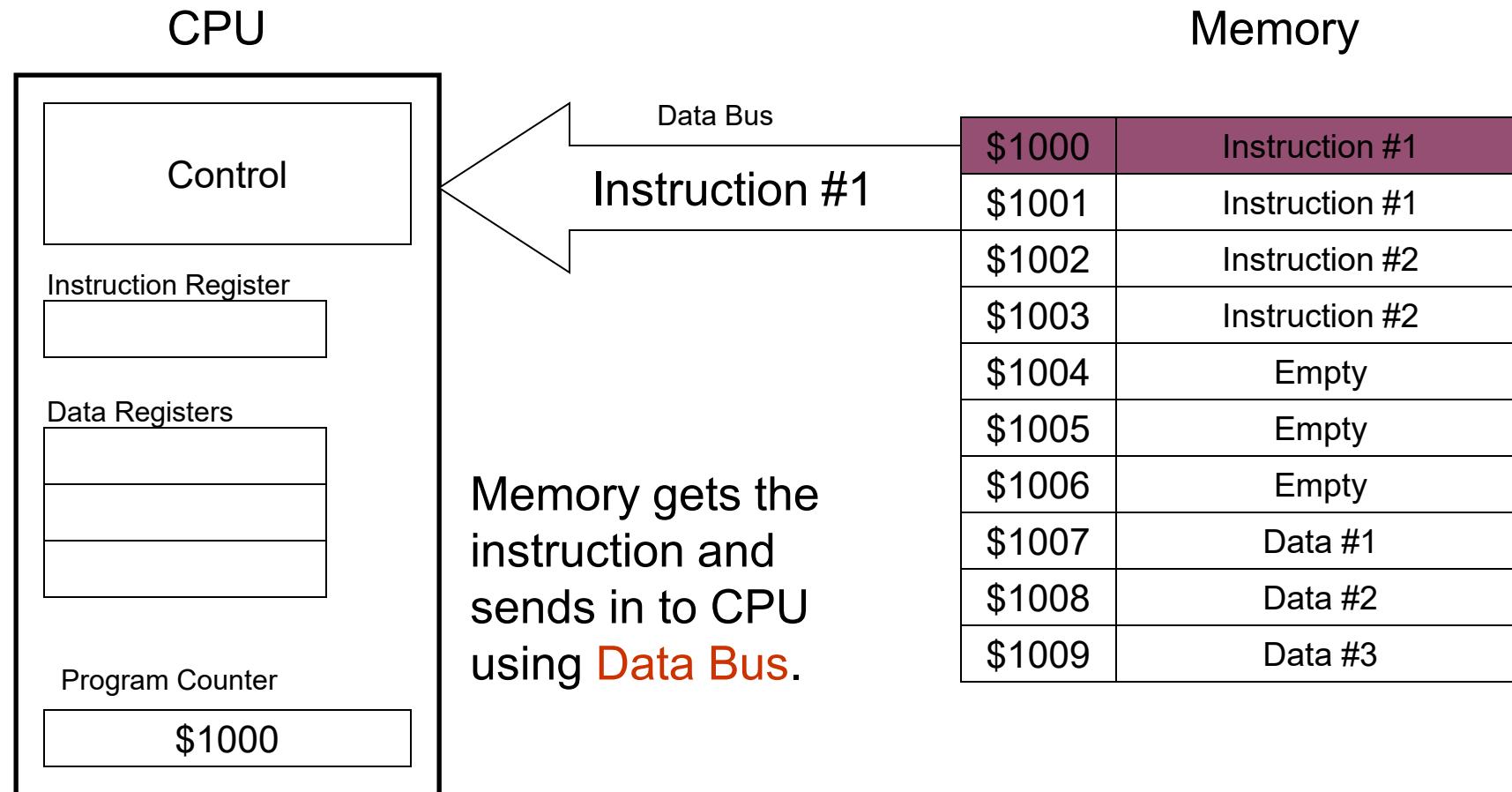
Fetch – Step 1

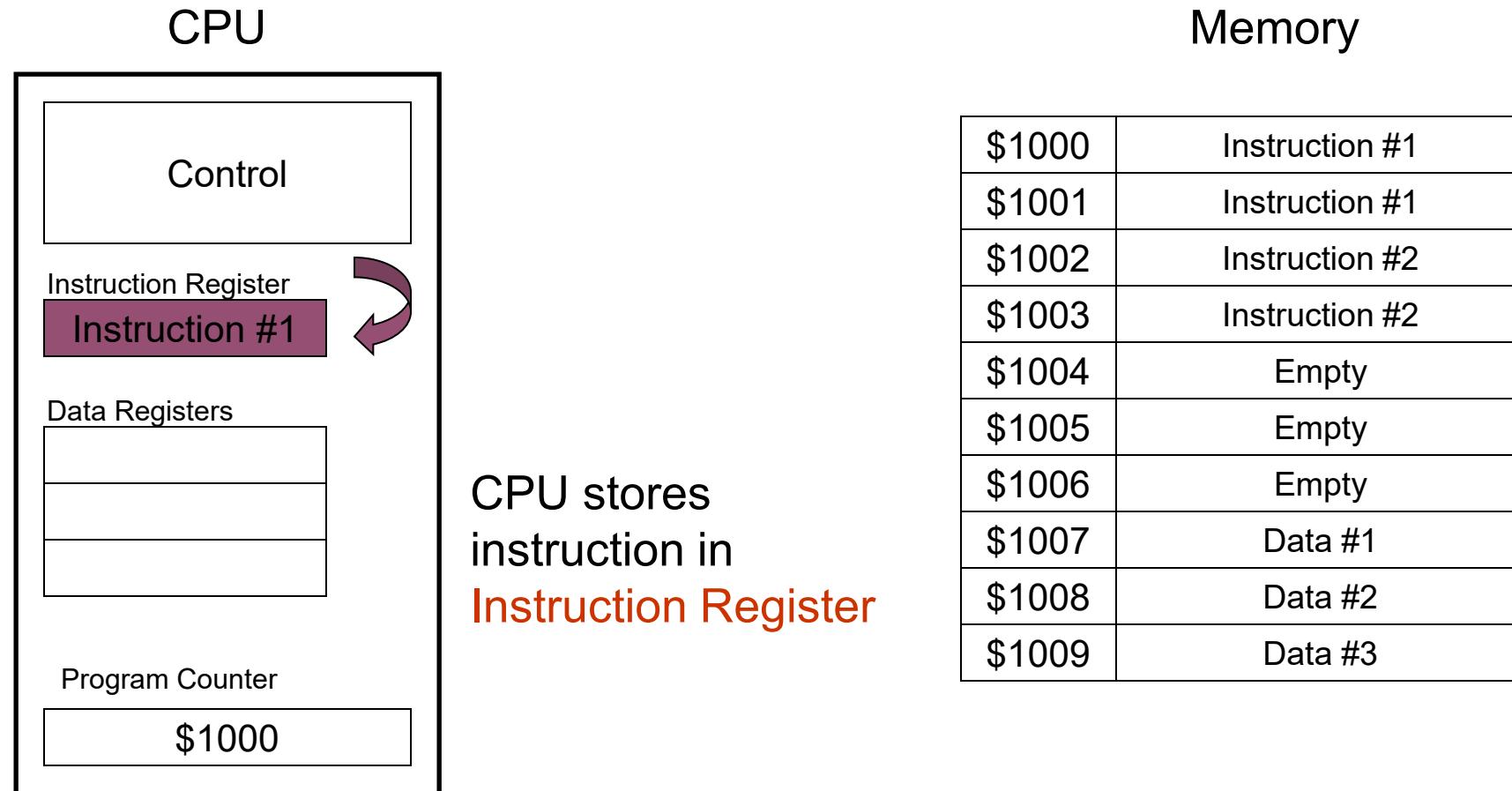


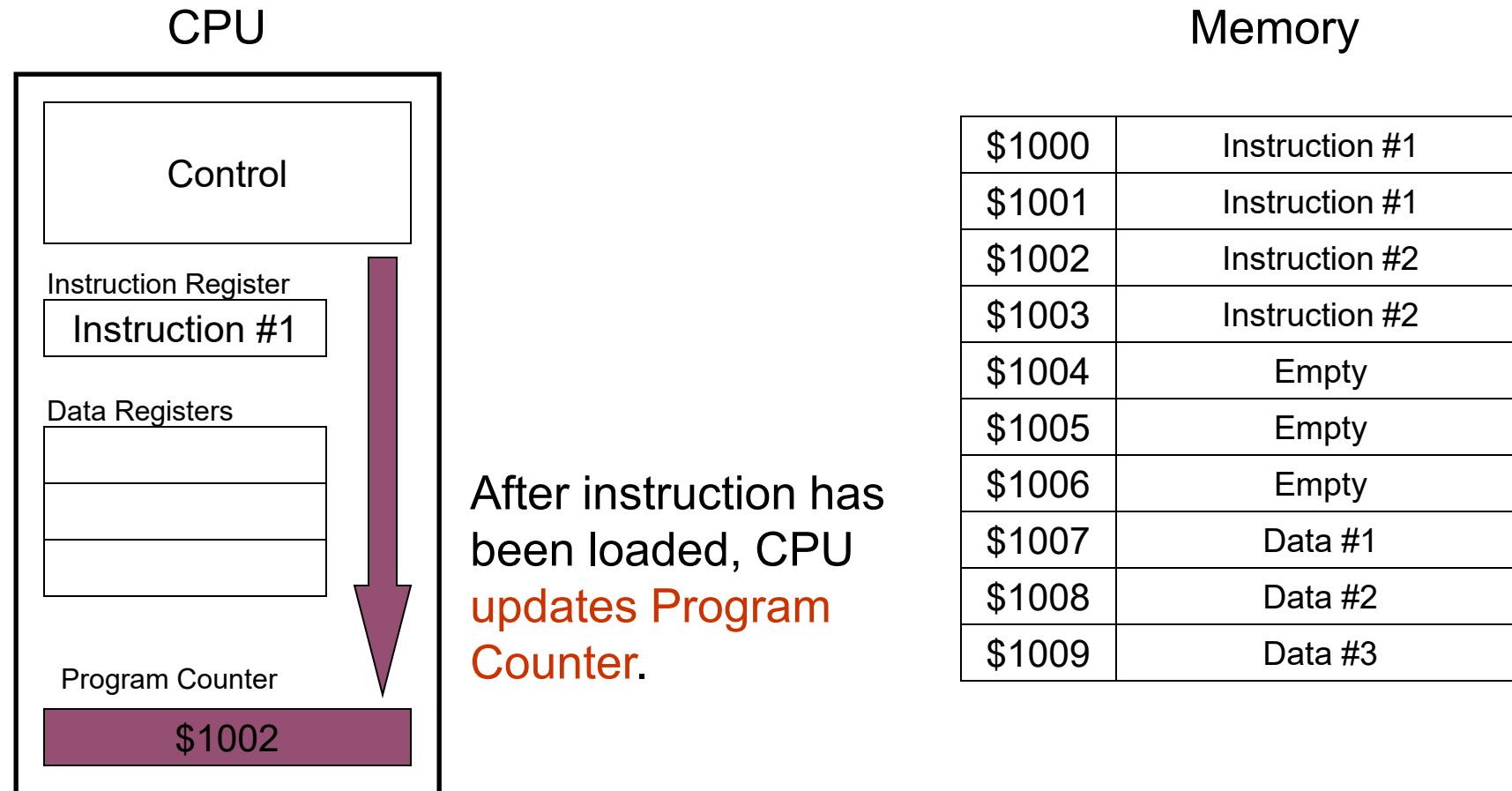
Fetch – Step 2

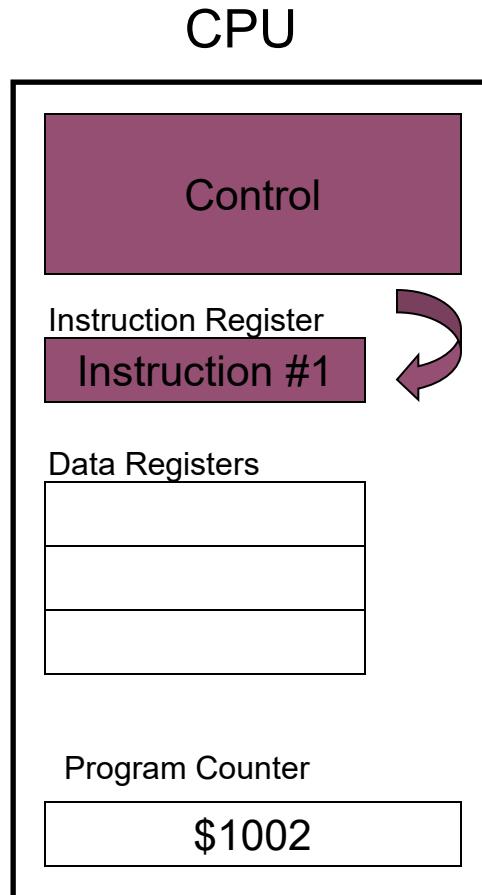


Fetch – Step 3









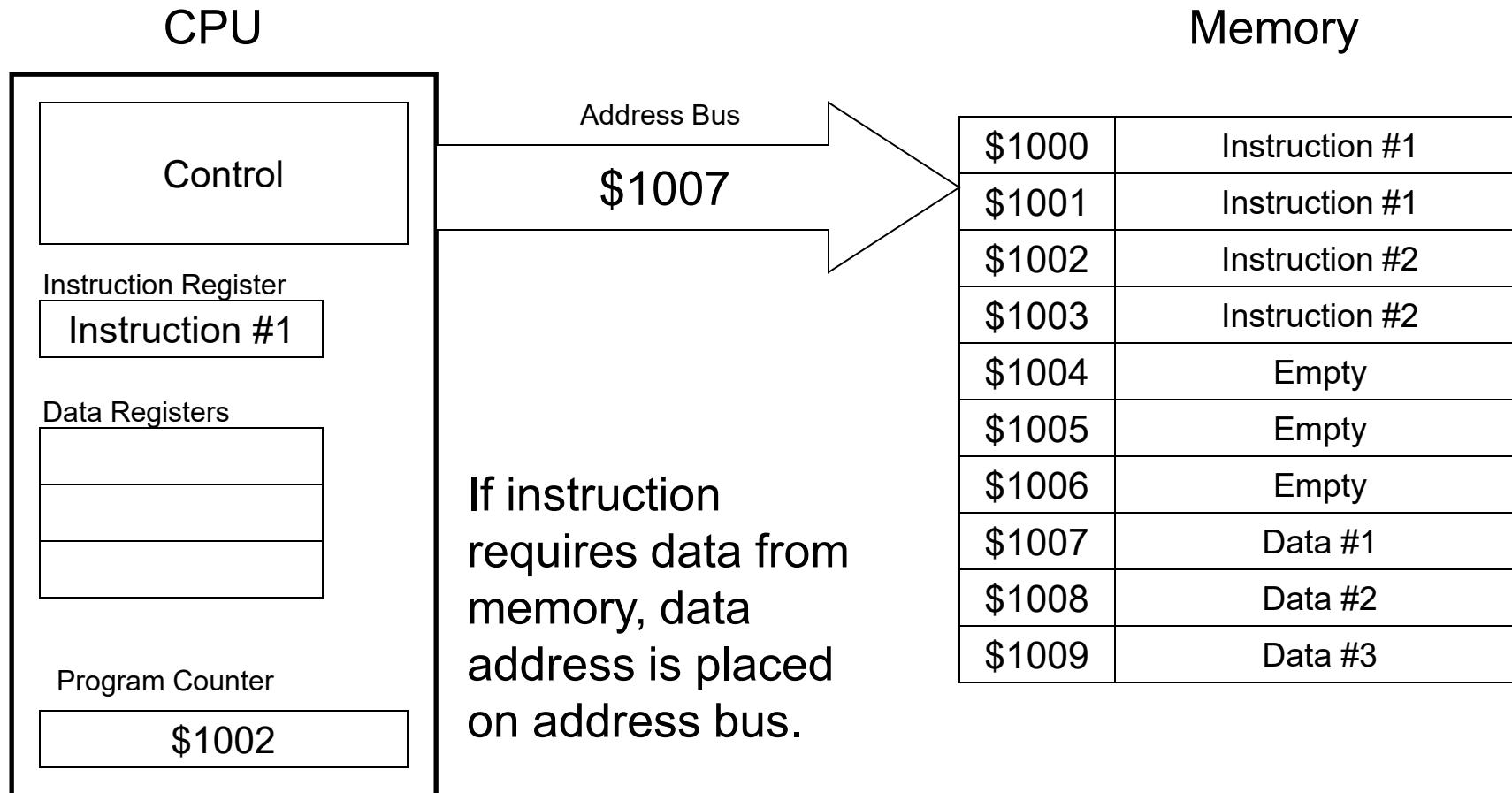
CPU analyzes
instructions before
executing it.

Memory

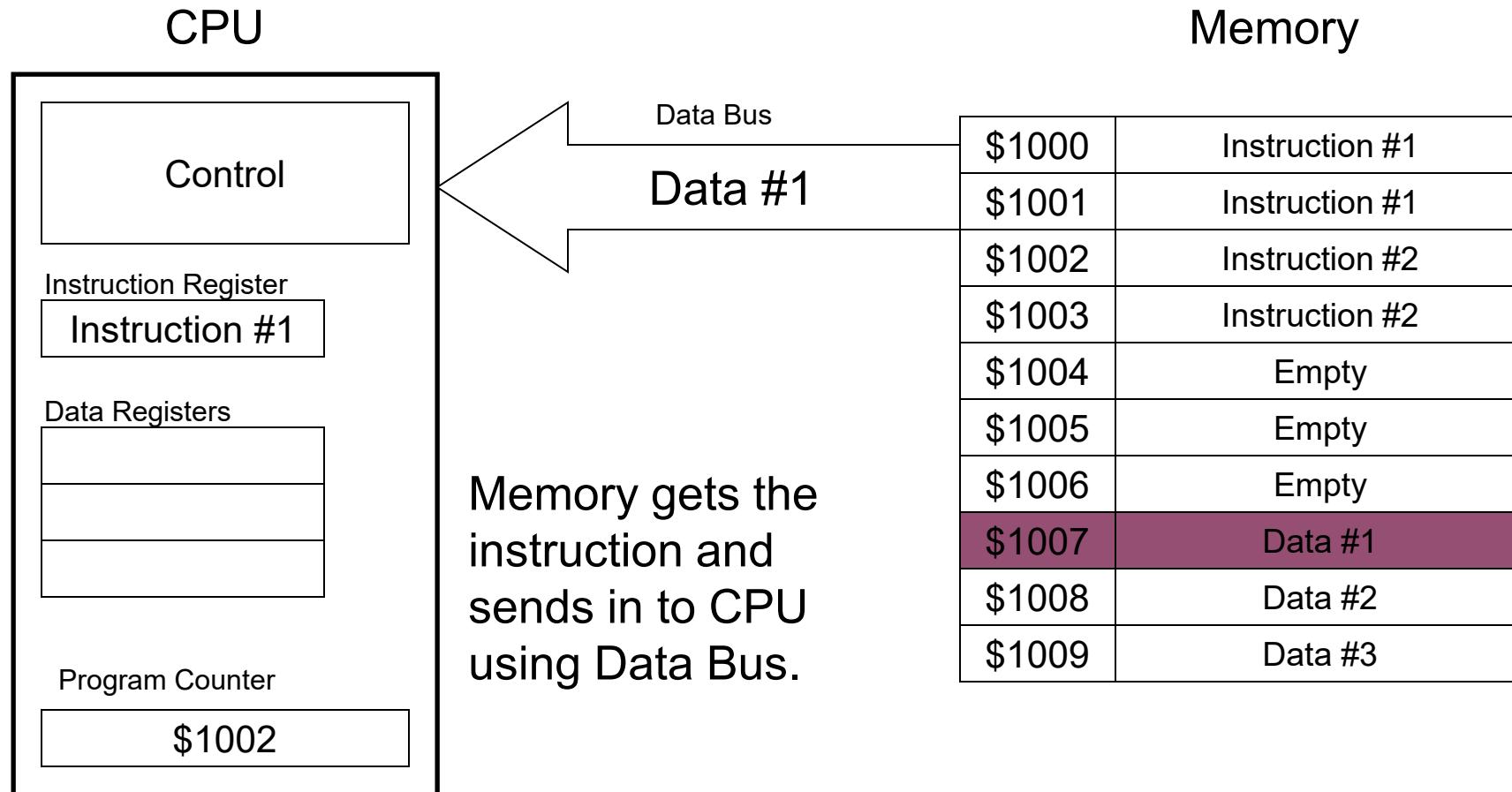
\$1000	Instruction #1
\$1001	Instruction #1
\$1002	Instruction #2
\$1003	Instruction #2
\$1004	Empty
\$1005	Empty
\$1006	Empty
\$1007	Data #1
\$1008	Data #2
\$1009	Data #3

Type of instruction.
Does the instruction require any data to perform calculations?
Where are the data located?

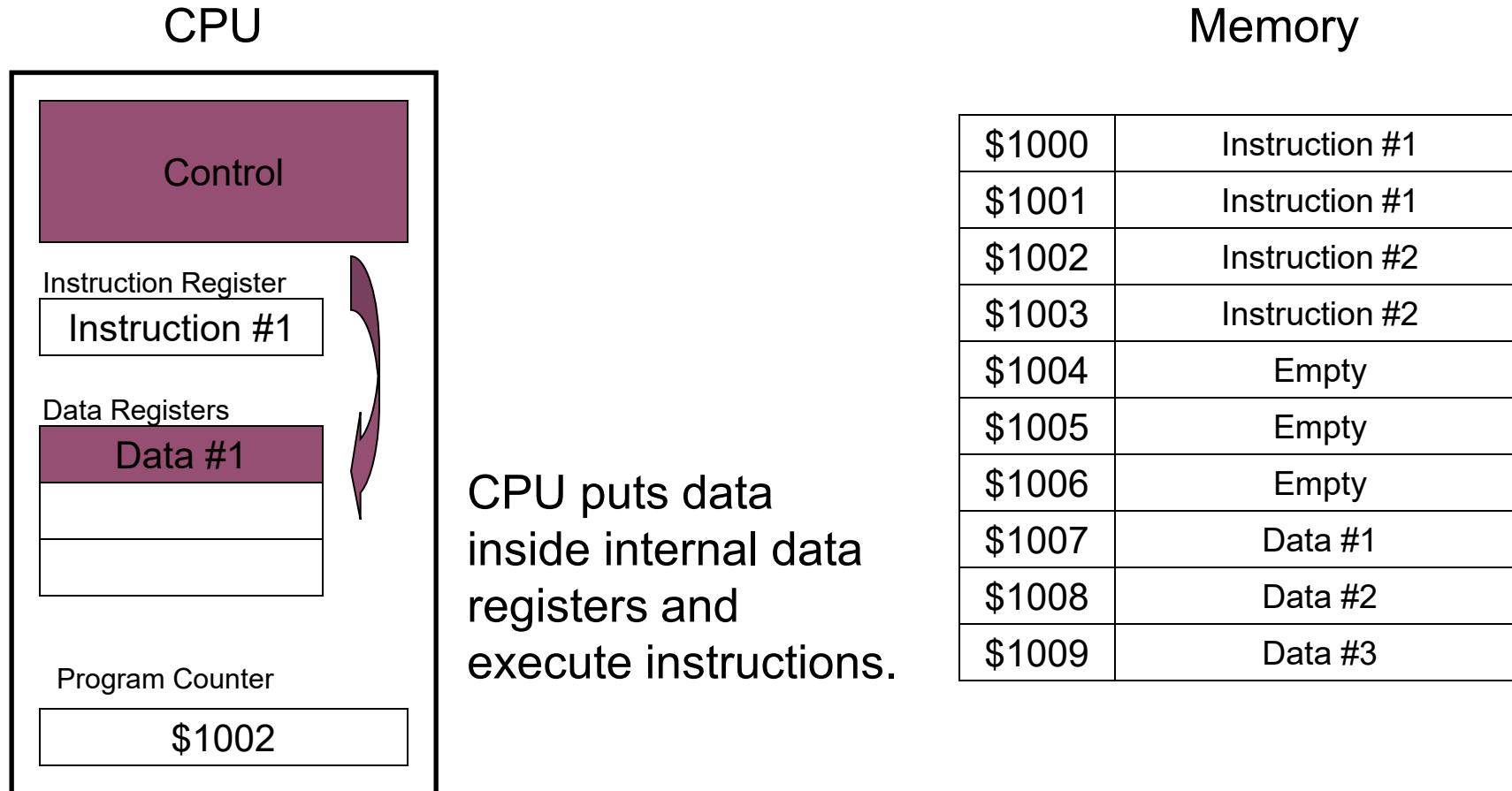
Execute – Step 1



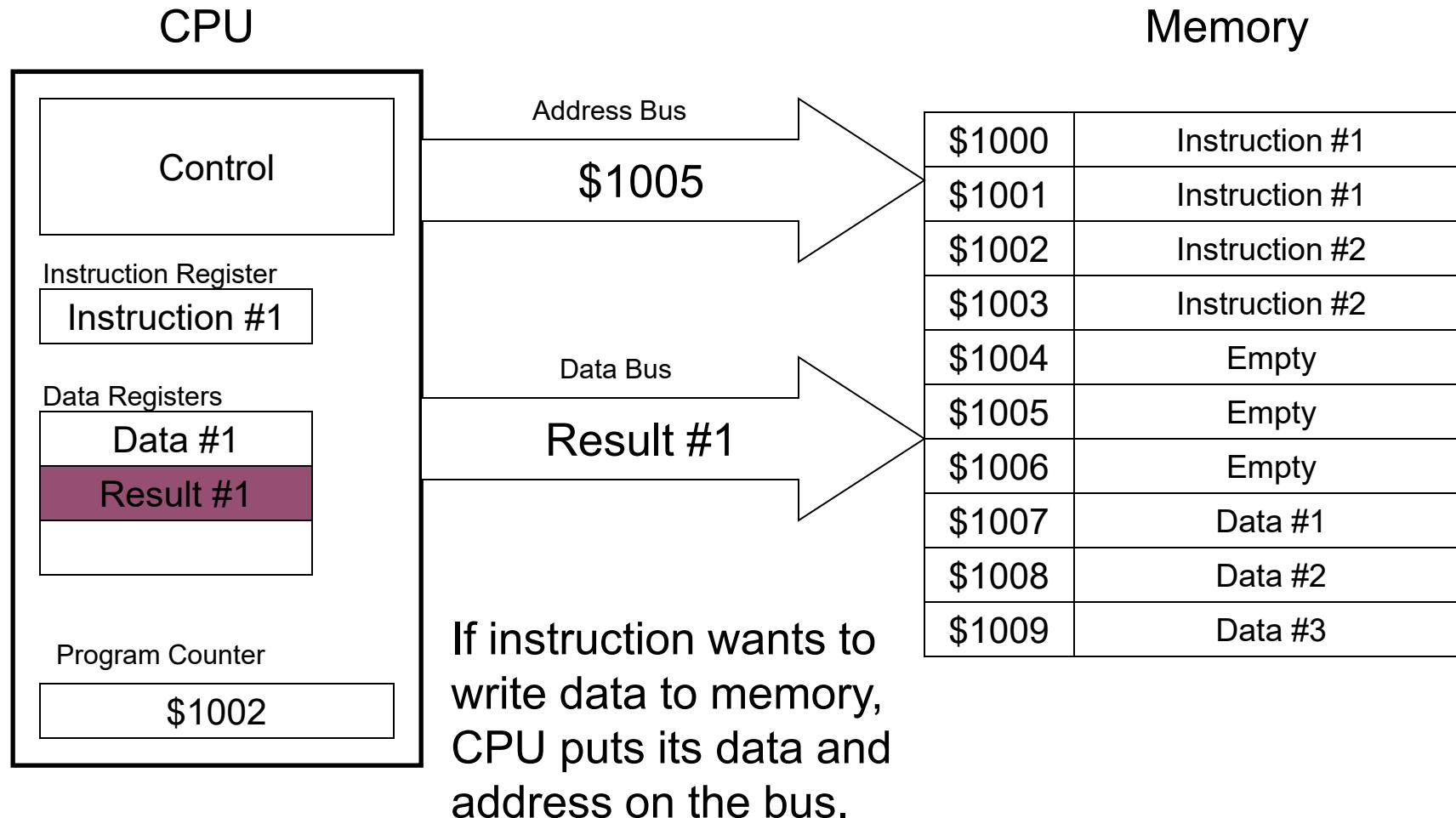
Execute – Step 2



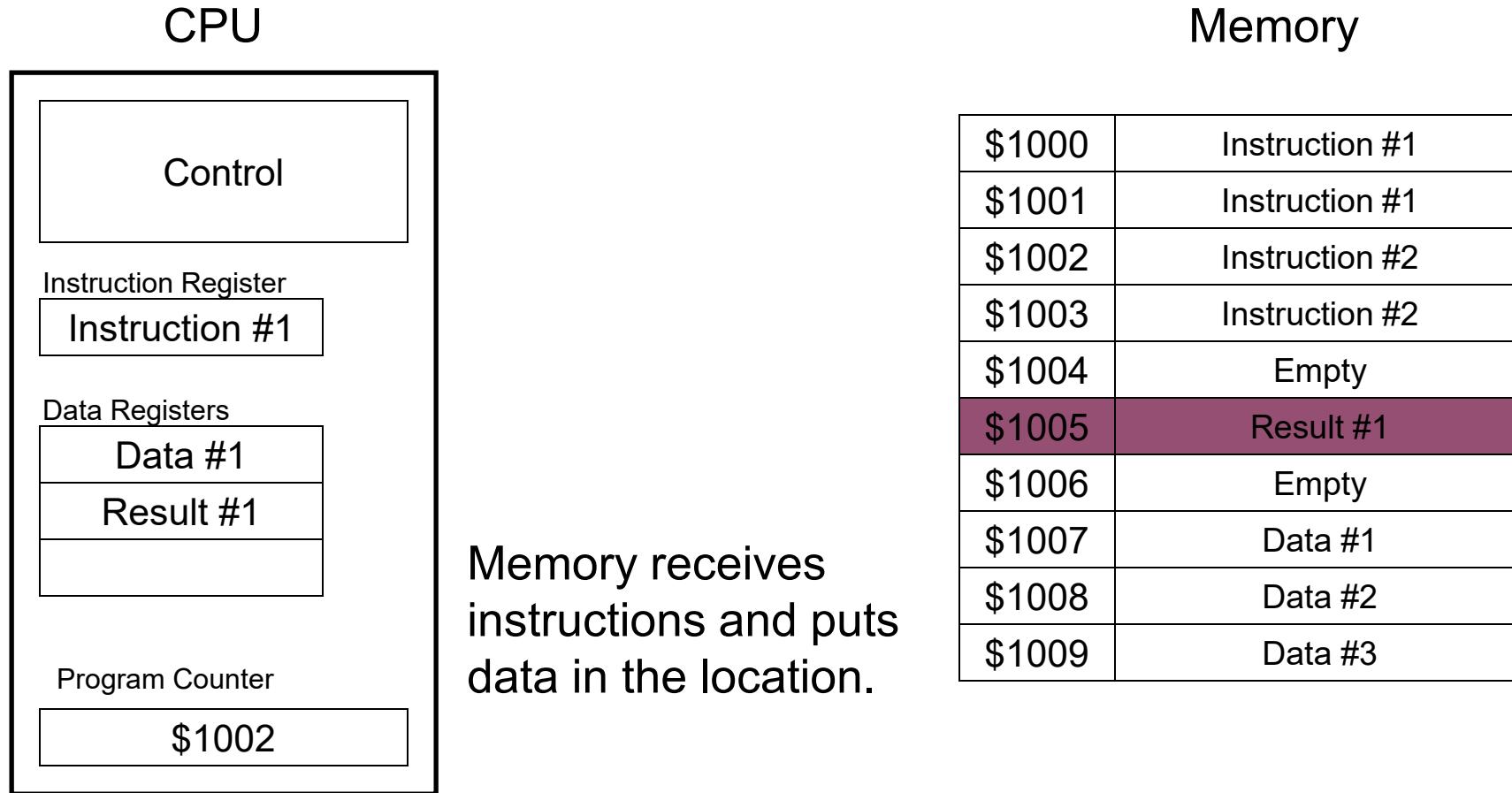
Execute – Step 3



Execute – Step 4



Execute – Step 5



Pipelined/Non-pipelined Architecture

Pipelined vs. Non-pipelined Execution

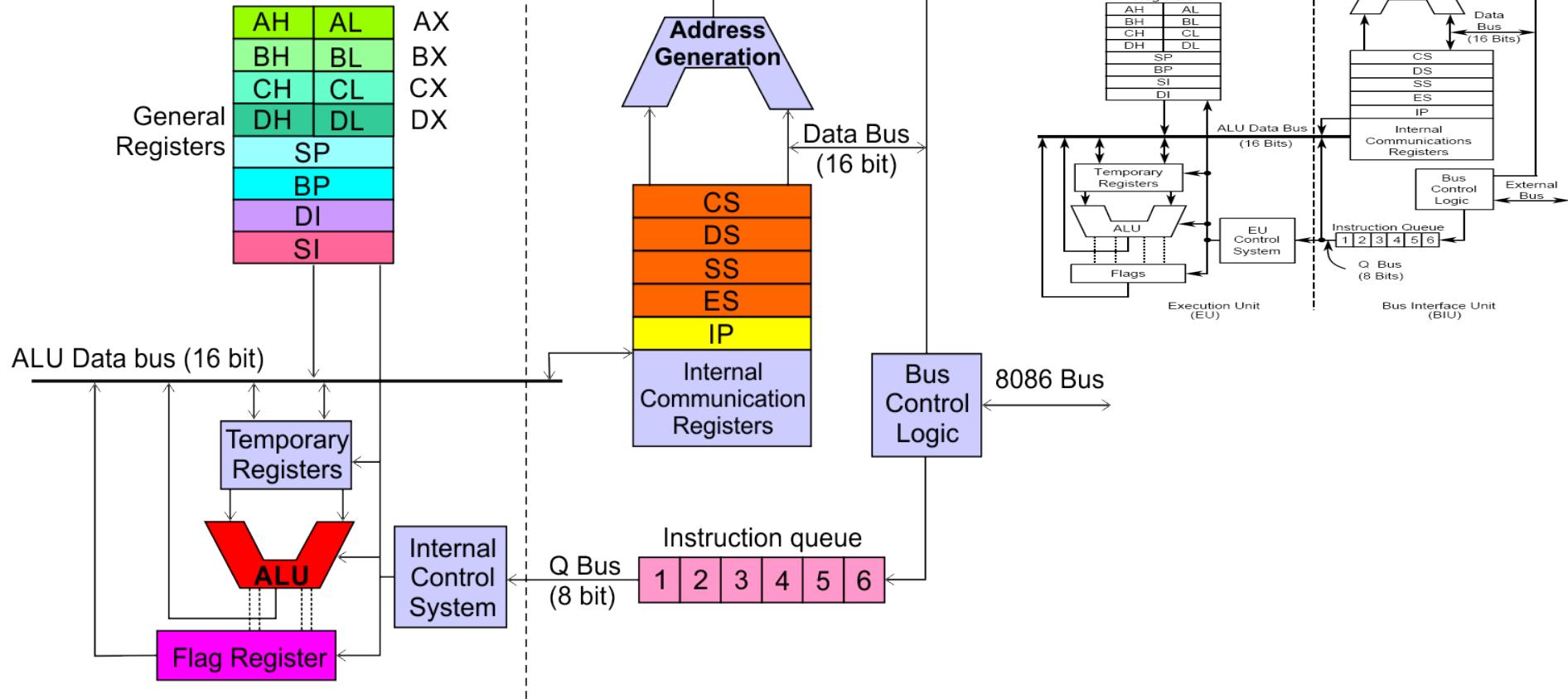
Pipelining of 8086

INSTRUCTION NO.	EXECUTION PHASES							
1	Fetch-1	Decode-1	Execute-1					
2		Fetch-2	Decode-2	Execute-2				
3			Fetch-3	Decode-3	Execute-3			
4				Fetch-4	Decode-4	Execute-4		
5					Fetch-5	Decode-5	Execute-5	
6						Fetch-6	Decode-6	Execute-6
Machine cycle	1	2	3	4	5	6	7	8

Non-Pipelining Process of 8085

	Instruction-1			Instruction-2			Instruction-3		
	Fetch-1	Decode-1	Execute-1	Fetch-2	Decode-2	Execute-2	Fetch-3	Decode-3	Execute-3
M. cycle	1	2	3	4	5	6	7	8	9

8086 Architecture and Processor Model



Execution Unit (EU)

EU executes instructions that have already been fetched by the BIU.

BIU and EU functions separately.

Bus Interface Unit (BIU)

BIU fetches instructions, reads data from memory and I/O ports, writes data to memory and I/O ports.

- The 8086 CPU logic has been partitioned into two functional units namely Bus Interface Unit (BIU) and Execution Unit (EU)
- The major reason for this separation is to increase the processing speed of the processor
- The BIU has to interact with memory and input and output devices in fetching the instructions and data required by the EU
- EU is responsible for executing the instructions of the programs and to carry out the required processing

Execution Unit

- The Execution Unit (EU) has
 - Control unit
 - Instruction decoder
 - Arithmetic and Logical Unit (ALU)
 - General registers
 - Flag register
 - Pointers
 - Index registers

Bus Interface Unit

- The BIU has
 - Instruction stream byte queue
 - A set of segment registers
 - Instruction pointer

BIU – Instruction Byte Queue

- 8086 instructions vary from 1 to 6 bytes
- Therefore fetch and execution are taking place concurrently in order to improve the performance of the microprocessor
- The BIU feeds the instruction stream to the execution unit through a 6 byte pre-fetch queue
- This pre-fetch queue can be considered as a form of loosely coupled **pipelining**

BIU – Instruction Byte Queue

- Execution and decoding of certain instructions do not require the use of buses
- While such instructions are executed, the BIU fetches up to six instruction bytes for the following instructions (the subsequent instructions)
- The BIU store these pre-fetched bytes in a first-in-first out register by name instruction byte queue
- When the EU is ready for its next instruction, it simply reads the instruction byte(s) for the instruction from the queue in BIU

Fetch and Execute Cycle Overlap

BIU outputs the contents of the IP onto the address bus

Register IP is incremented by one or more than one for the next instruction fetch

Once inside the BIU, the instruction is passed to the queue

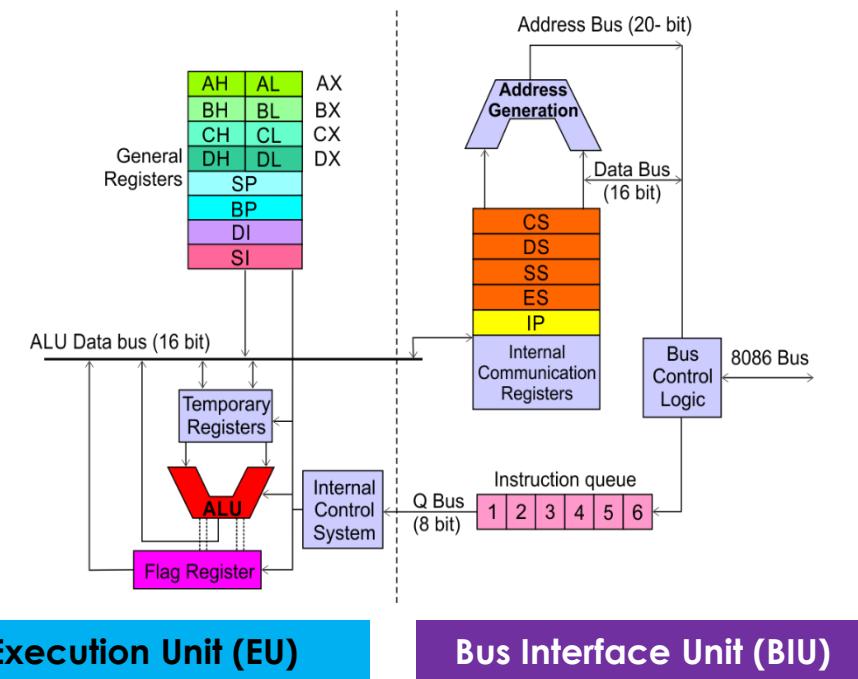
The queue is a First-In-First-Out (FIFO) register sometimes likened to a pipeline

Assuming that the queue is initially empty, the EU immediately draws this instruction from the queue and begins execution

While the EU is executing the instruction, the BIU proceeds to fetch a new instruction

BIU will fill the queue with several new instructions before the EU is ready to draw its next instruction

The cycle continues



Execution Unit (EU)

Bus Interface Unit (BIU)

INSTRUCTION NO.	EXECUTION PHASES							
	Fetch-1	Decode-1	Execute-1					
1								
2		Fetch-2	Decode-2	Execute-2				
3			Fetch-3	Decode-3	Execute-3			
4				Fetch-4	Decode-4	Execute-4		
5					Fetch-5	Decode-5	Execute-5	
6						Fetch-6	Decode-6	Execute-6
Machine cycle	1	2	3	4	5	6	7	8

8086 Registers

Flag Register

Execution Unit (EU)



OVERFLOW Flag (OF) – status flag

DIRECTION Flag (DF) – control flag

INTERRUPT Flag (IF) – control flag

TRAP Flag (TF) – control flag

SIGN Flag (SF) – status flag

ZERO Flag (ZF) – status flag

AUXILIARY Flag (AF) – status flag

PARITY Flag (PF) – status flag

CARRY Flag (CF)