EKT-423: OPERATING SYSTEM
TUTORIAL 01

1. A DMA module is transferring characters to main memory from an external device transmitting at <u>9600 bits per second</u> (bps). The processor can fetch instructions at the rate of <u>1 million instructions per second</u>. By how much will the processor be slowed down due to the DMA activity?

Answer

Let us ignore data read/write operations and assume the processor only fetches instructions. Then the processor needs access to main memory once every microsecond.

Transferring characters main memory from an external device transmitting at 9600 bits per second (bps);

Hence,   1 bit = 1/9600 s = 1.04 X 10^{-4} s= 104 us

Fetch instruction type, 1 million instructions per second

Assume that,
  1 Instruction = 1 bps
  1 mps = 1 us per Instruction
  9600 per second = 104 us per instruction
So, Processor Slowdown = (1/104) x 100% = 0.9615% (approx.) Ans…

2. A computer consists of a CPU and an I/O device D connected to main memory M via a shared bus with a data bus width of one word (16-bits). The CPU can execute a <u>maximum of 10^6 instructions per second</u>. An average instruction <u>requires five processor cycles, three of which use the memory bus</u>. A memory read or write operation uses one processor cycle. Suppose that the CPU is continuously executing <u>"background" programs that require 95%</u> of its instruction execution rate but not any I/O instructions. Assume that <u>one processor cycle equals one bus cycle</u>. Now suppose that very large blocks of data are to be transferred between M and D.

a. If programmed I/O is used and each one-word I/O transfer requires the CPU to execute two instructions, estimate the maximum I/O data transfer rate, in words per second, possible through D.

b. Estimate the same rate if DMA transfer is used.

Answer

a. The processor can only devote 5% (or, 5/100) of its time to I/O.

CPU can execute a maximum of 10^6 instructions per second

Thus the maximum I/O instruction execution rate is 10^6 x 0.05 = 50,000 instructions per second.

The I/O transfer rate is therefore = 50,000/2 = 25000 words/second.

b. The number of machine cycles available for DMA control is

$$10^6 \text{ x } (0.05 \text{ x } 5 + 0.95 \text{ x } 2) = 2.15 \text{ x } 10^6$$

If we assume that the DMA module can use all of these cycles, and ignore any setup or status-checking time, then this value is the maximum I/O transfer rate.

3. **Consider a memory system with the following parameters:**

$$T_c = 100 \text{ ns} \qquad C_c = 0.005 \text{ cents/bit}$$
$$T_m = 1200 \text{ ns} \qquad C_m = 0.0002 \text{ cents/bit}$$

a. What is the cost of 5 MByte of main memory?

b. What is the cost of 5 MByte of main memory using cache memory technology?

c. If the effective access time is 20% greater than the cache access time, what is the hit ratio H?

1 Kbit = 1000 bit
1MBytes=8000000 = 8×10^6 bit
1GBytes=8000000000 = 8×10^9 bit

Answer

a. **Cost of 5 MB of main memory**

$$\text{Cost} = C_m \times 5 \text{ MB} = 0.0002 \times 5 \times 8 \times 10^6 \text{ ¢} = 8000 \text{ ¢} = \$80$$

b. **Cost of 5 MB of main memory** using cache

$$\text{Cost} = C_c \times 5\text{MB} = 0.005 \times 5 \times 8 \times 10^6 \text{ ¢} = 200000 \text{ ¢} = \$2000$$

c. From the Equation $\quad T_s = H T_1 + (1 - H)(T_1 + T_2) = T_1 + T_2 - HT_2$

$$H = (T_1 + T_2 - T_s)/ T_2$$

where

T_s = average (system) access time = 20% T1 = (20/100) 100 = 20 ns
T_1 = access time of M1 (e. g., cache, disk cache) = 100 ns
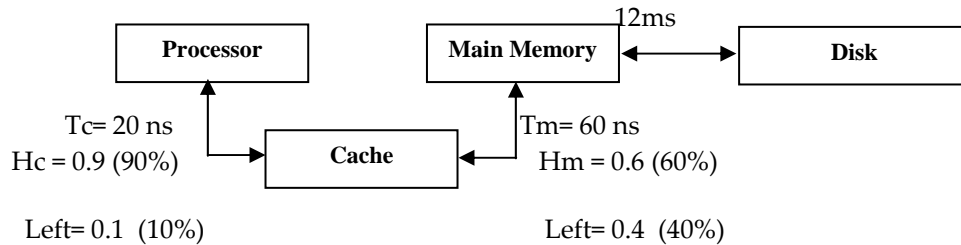T_2 = access time of M2 (e. g., main memory, disk) = 1000ns
H = hit ratio (fraction of time reference is found in M1) =?

$$H = (100 + 1000 - 20) / 1000 = 1080/1000 = 1.08$$

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4. A computer has a cache, main memory, and a disk used for virtual memory. If a referenced word is <u>in the cache, 20 ns</u> are required to access it. If it is <u>in main memory but not in the cache, 60 ns</u> are needed to load it into the cache (this includes the time to originally check the cache), and then the reference is started again. If the word <u>is not in main memory, 12 ms</u> are required to fetch the word from disk, followed by 60 ns to copy it to the cache, and then the reference is started again. The <u>cache hit ratio is 0.9(90%)</u> and the <u>main-memory hit ratio is 0.6 (60%)</u>. What is the average time in ns required to access a referenced word on this system?

Answer:

Processor		Main Memory		Disk

12ms (between Main Memory and Disk)

Tc= 20 ns
Hc = 0.9 (90%) → Cache ← Tm= 60 ns
Hm = 0.6 (60%)

Left= 0.1 (10%)   Left= 0.4 (40%)

There are three cases to consider:

Location of referenced word	Probability	Total time for access in ns
In cache	0.9	20
Not in cache, but in main memory	(0.1)(0.6) = 0.06	60 + 20 = 80
Not in cache or main memory	(0.1)(0.4) = 0.04	12ms + 60 + 20 = 12,000,080

So the average access time would be:

Avg = (0.9)(20) + (0.06)(80) + (0.04)(12000080) = 480026 ns