Home work sheet -3

Cs 207 D

Q1:

M,A two-way set-associative cache has lines of 16 bytes and a total size of 8 kbytes.The64-Mbyte main memory is byte addressable. Show the format of main memory Addresses?

Answer:

number of Blocks at the cache = 8000 byte/16byte=512 blocks (lines in the cache)
Set line=512/2=256 sets of 2 line each
256= 2 ^ 8 (8- bit for set slot)

Main memory 64 M byte= 2^ 26 (26-bit address memory)
number of Blocks at the Memory= 64 M byte/16 byte=4 M blocks=2^22
means : set slot bit + Tag bits=22 bits = s
Tage field =22 - 8=14 bits

The remains will be the Word length or
Block size=16 byte= 2^4 (Word length = 4)

	S		
	Tag	Sets slot	W
Memory address=26 bits	14	8	4

Extra:
set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.
Answer:
The cache is divided into 16 sets of 4 lines each. Therefore, 4 bits are needed to identify the set number. Main memory consists of 4K = 2 ^12 blocks. Therefore, the set plus tag lengths must be 12

bits and therefore the tag length is 8 bits. Each block contains 128 words. Therefore, 7 bits are needed to specify the word.

	S		
	Tag	Sets slot	W
Memory address	8	4	7

Q2:

For the hexadecimal main memory addresses 111111, 666666,BBBBBB, show the following information, in hexadecimal format:

a. Tag, Line, and Word values for a direct-mapped cache, using the format of Figure 4.10

b. Tag and Word values for an associative cache, using the format of Figure 4.12

c. Tag, Set, and Word values for a two-way set-associative cache, using the format of Figure 4.15

Address	111111	666666	BBBBBB
a.Tag/Line/Word	11 / 444 / 1	66 / 1999 / 2	BB / 2EEE / 3
b.Tag /Word	44444 / 1	199999 / 2	2EEEEE / 3
c.Tag/Set/Word	22 / 444 / 1	CC / 1999 / 2	177 / EEE / 3

Q3:

Consider a machine with a byte addressable main memory of 2^16 bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.

a. How is a 16-bit memory address divided into tag, line number, and byte number?

b. Into what line would bytes with each of the following addresses be stored?

0001 0001 0001 1011

1100 0011 0011 0100

1101 0000 0001 1101

1010 1010 1010 1010

c. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?

d. How many total bytes of memory can be stored in the cache?

e. Why is the tag also stored in the cache?.

a. 8 leftmost bits = tag; 5 middle bits = line number; 3 rightmost bits = byte number.

	S		
	Tag	**Sets slot**	**W**
Memory address=16 bits	**8**	**5**	**3**

b.
Line 3.
Line 6.
Line 3.
Line 21.

c. Bytes with addresses 0001 1010 0001 1000 through 0001 1010 0001 1111 are stored in the cache.

d. 256 bytes.=2^8 or
32 blocks * 8 byte = 256 byte

e. Because two items with two different memory addresses can be stored in the same place in the cache**.** The tag is used to distinguish between them

Q3:

Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size.

a. Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

a. Address Address format: Tag = 20 bits; Line = 6 bits; Word = 6 bits.
Number of addressable units = 2s+w = 232 bytes; number of blocks in main memory = 2s = 226; Number of lines in cache 2r = 26 = 64; size of tag = 20 bits.

b. Assume an associative cache. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.

b. Address format: Tag = 26 bits; Word = 6 bits.
Number of addressable units = 2s+w = 232 bytes; number of blocks in main memory = 2s = 226; Number of lines in cache = undetermined; size of tag = 26 bits.

c. Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in set, number of sets in cache, number of lines in cache, size of tag.
Answer:

c. Address format: Tag = 9 bits; Set = 17 bits; Word = 6 bits.
Number of addressable units = 2s+w = 232 bytes; Number of blocks in main memory = 2s = 226; Number of lines in set = k = 4; Number of sets in cache = 2d = 217; Number of lines in cache = k × 2d =219; Size of tag = 9 bits.