

16.41 The 8251A Programmable Communication Interface

The 8251A is a programmable chip designed for synchronous and asynchronous serial data communication, packaged in a 28-pin DIP. The 8251A is the enhanced version of its predecessor, the 8251, and is compatible with the 8251. Figure 16.12 shows the block diagram of the 8251A. It includes five sections: Read/Write Control Logic, Transmitter, Receiver, Data Bus Buffer, and Modem Control.

The control logic interfaces the chip with the MPU, determines the functions of the chip according to the control word in its register (to be explained below), and monitors the data flow. The transmitter section converts a parallel word received from the MPU into serial bits and transmits them over the TxD line to a peripheral. The receiver section receives serial bits from a peripheral, converts them into a parallel word, and transfers the word to the MPU. The modem control is used to establish data communication through modems over telephone lines. The 8251A is a complex device, capable of performing various functions. For the sake of clarity, this chapter focuses only on the asynchronous mode of serial I/O and excludes any discussion of the synchronous mode and the modem control. The asynchronous mode is often used for data communication between the MPU and serial peripherals such as terminals and floppy disks.

Figure 16.13 shows an expanded version of the 8251A block diagram. The block diagram shows all the elements of a programmable chip; it includes the interfacing signals, the control register, and the status register. The functions of various blocks are described below.

READ/WRITE CONTROL LOGIC AND REGISTERS

This section includes R/W control logic, six input signals, control logic, and three buffer registers: data register, control register, and status register. The input signals to the control logic are as follows.

Input Signals

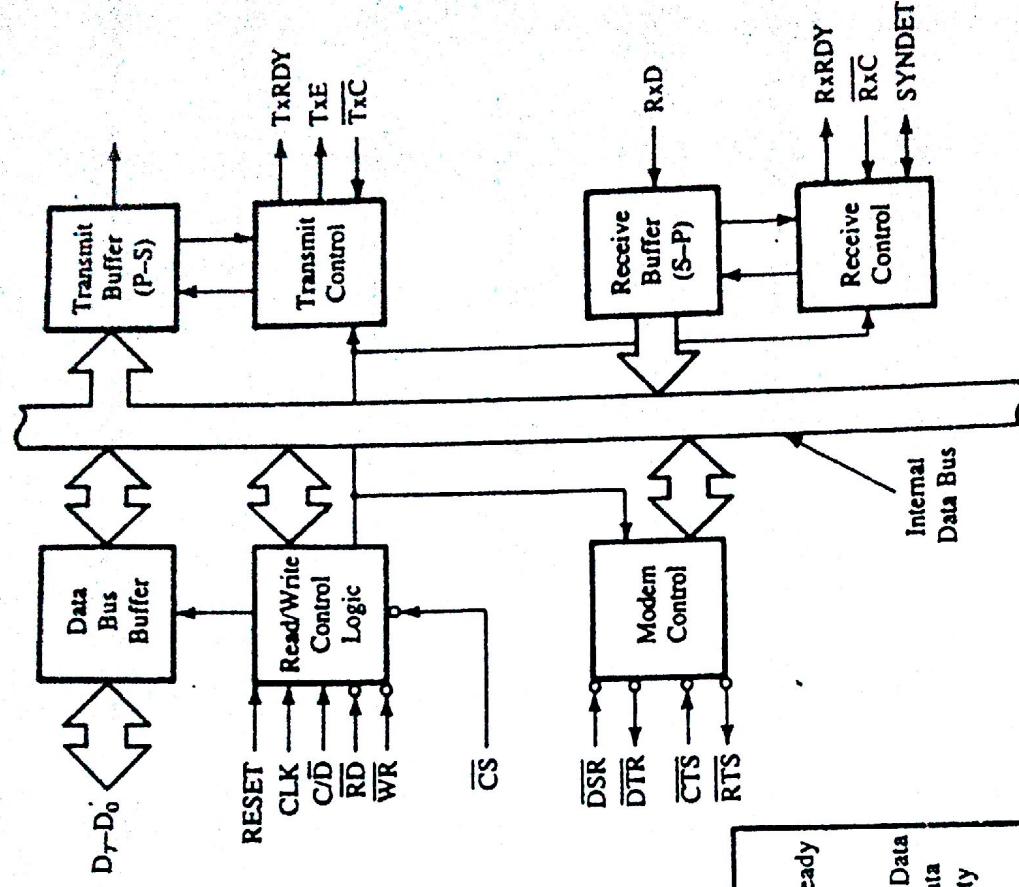
- CS—Chip Select:** When this signal goes low, the 8251A is selected by the MPU for communication. This is usually connected to a decoded address bus.
- C/D—Control/Data:** When this signal is high, the control register or the status register is addressed; when it is low, the data buffer is addressed. The control register and the status register are differentiated by WR and RD signals, respectively.
- WR—Write:** When this signal goes low, the MPU either writes in the control register or sends output to the data buffer. This is connected to IOW or MEMW.
- RD—Read:** When this signal goes low, the MPU either reads a status from the status register or accepts (inputs) data from the data buffer. This is connected to either IOR or MEMR.
- RESET—Reset:** A high on this input resets the 8251A and forces it into the idle mode.
- CLK—Clock:** This is the clock input, usually connected to the system clock. This clock does not control either the transmission or the reception rate. The clock is necessary for communication with the microprocessor.

Pin Configuration

D ₁	28	D ₁
D ₃	2	D ₀
RxD	27	
GND	3	26 V _{CC}
D ₄	4	25 Rx _C
D ₅	5	24 DTR
D ₆	6	23 RTS
D ₇	7	22 DSR
TxC	9	21 RESET
WR	10	20 CLK
CS	11	19 TxD
C/D	12	18 TxEMPTY
RD	13	17 CTS
RxD	14	16 SYNDET/BD
RxD	15	15 TxRDY

8251A

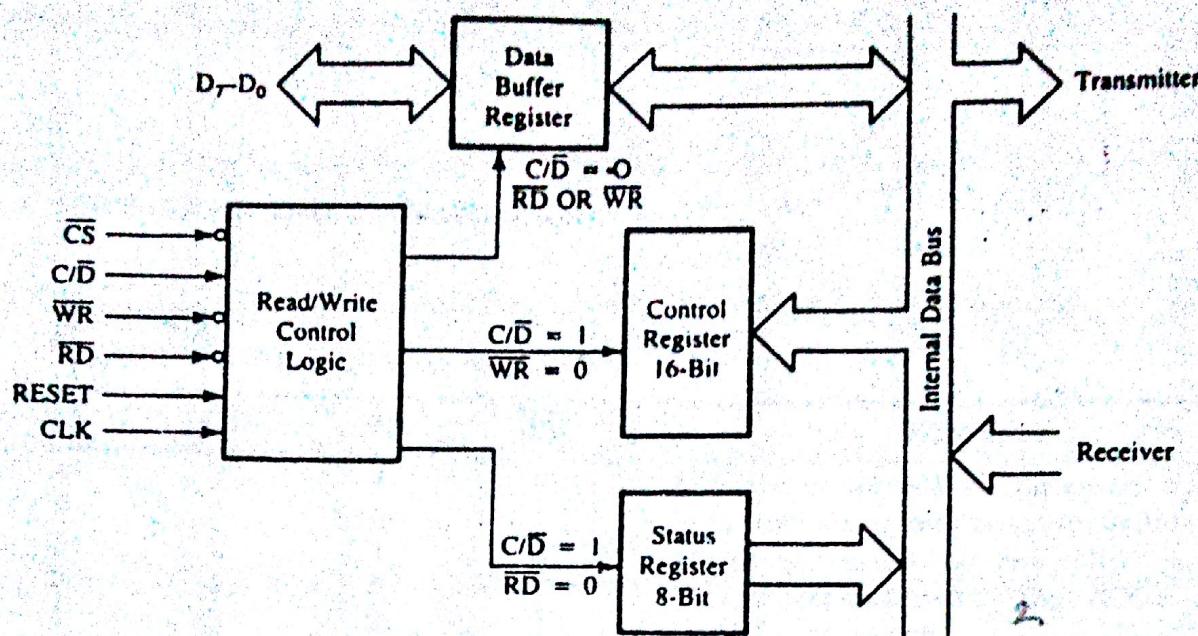
Block Diagram



Pin Names	Pin Descriptions
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET/BD	Sync Detect/ Break Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V _{CC}	+ 5 Volt Supply
GND	Ground

D ₇ -D ₀	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxD	Receiver Ready
TxRDY	Transmitter Ready

FIGURE 16.12
The 8251A: Block Diagram, Pin Configuration, and Description
SOURCE: Intel Corporation, Connectivity (Santa Clara, Calif.: Author, 1993), p. 2-2.

**FIGURE 16.13**

The 8251A: Expanded Block Diagram of Control Logic and Registers

Control Register This 16-bit register for a control word consists of two independent bytes: the first byte is called the **mode instruction** (word) and the second byte is called the **command instruction** (word). This register can be accessed as an output port when the C/D pin is high.

Status Register This input register checks the ready status of a peripheral. This register is addressed as an input port when the C/D pin is high; it has the same port address as the control register.

Data Buffer This bidirectional register can be addressed as an input port and an output port when the C/D pin is low. Table 16.4 summarizes all the interfacing and control signals.

TRANSMITTER SECTION

The transmitter accepts parallel data from the MPU and converts them into serial data. It has two registers: a buffer register to hold eight bits and an output register to convert eight bits into a stream of serial bits (Figure 16.14). The MPU writes a byte in the buffer register; whenever the output register is empty, the contents of the buffer register are transferred to the output register. This section transmits data on the TxD pin with the appropriate framing bits (Start and Stop). Three output signals and one input signal are associated with the transmitter section.

- **TxD—Transmit Data:** Serial bits are transmitted on this line.
- **TxC—Transmitter Clock:** This input signal controls the rate at which bits are transmitted by the USART. The clock frequency can be 1, 16, or 64 times the baud.

SERIAL I/O AND DATA COMMUNICATION

TABLE 16.4
Summary of Control Signals for the 8251A

CS	C/D	RD	WR	Function
0	1	1	0	MPU writes instructions in the control register
0	1	0	1	MPU reads status from the status register
0	0	1	0	MPU outputs data to the Data Buffer
0	0	0	1	MPU accepts data from the Data Buffer
1	X	X	X	USART is not selected

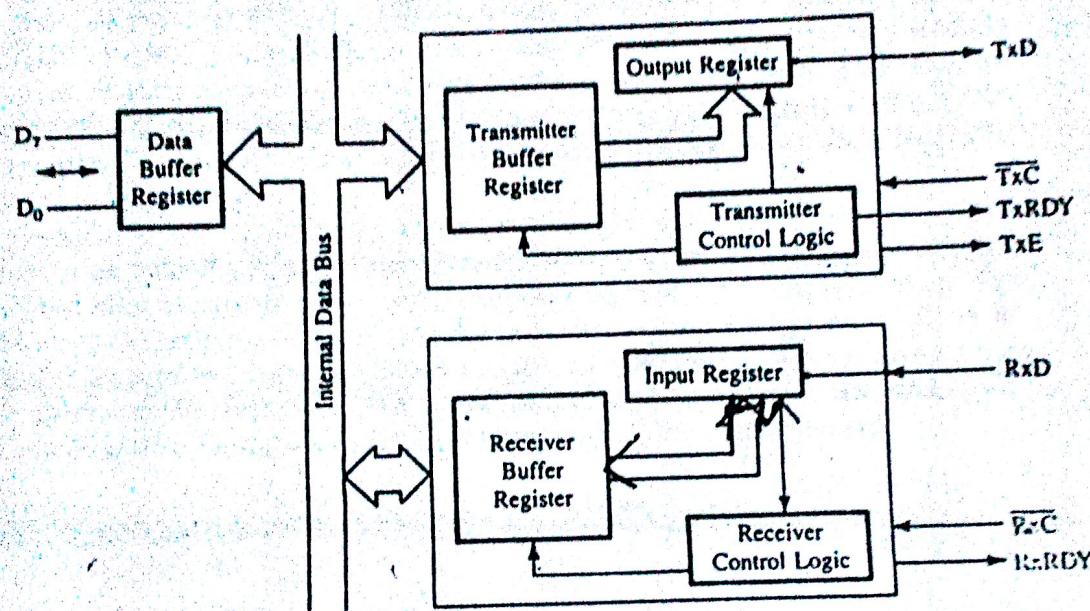


FIGURE 16.14
The 8251A: Expanded Block Diagram of Transmitter and Receiver Sections

- **TxRDY—Transmitter Ready:** This is an output signal. When it is high, it indicates that the buffer register is empty and the USART is ready to accept a byte. It can be used either to interrupt the MPU or to indicate the status. This signal is reset when a data byte is loaded into the buffer.
- **TxE—Transmitter Empty:** This is an output signal. Logic 1 on this line indicates that the output register is empty. This signal is reset when a byte is transferred from the buffer to the output registers.

RECEIVER SECTION

The receiver accepts serial data on the RxD line from a peripheral and converts them into parallel data. The section has two registers: the receiver input register and the buffer register (Figure 16.14).

When the RxD line goes low, the control logic assumes it is a Start bit, waits for half a bit time, and samples the line again. If the line is still low, the input register accepts

the following bits, forms a character, and loads it into the buffer register. Subsequently, the parallel byte is transferred to the MPU when requested. In the asynchronous mode, two input signals and one output signal are necessary, as described below.

- RxD—Receive Data:** Bits are received serially on this line and converted into a parallel byte in the receiver input register.
- RxC—Receiver Clock:** This is a clock signal that controls the rate at which bits are received by the USART. In the asynchronous mode, the clock can be set to 1, 16, or 64 times the baud.
- RxRDY—Receiver Ready:** This is an output signal. It goes high when the USART has a character in the buffer register and is ready to transfer it to the MPU. This line can be used either to indicate the status or to interrupt the MPU.

INITIALIZING THE 8251A

To implement serial communication, the MPU must inform the 8251A of all details, such as mode, baud, Stop bits, parity, etc. Therefore, prior to data transfer, a set of control words must be loaded into the 16-bit control register of the 8251A. In addition, the MPU must check the readiness of a peripheral by reading the status register. The control words are divided into two formats: mode words and command words. The mode word specifies the general characteristics of operation (such as baud, parity, number of Stop bits), the command word enables data transmission and/or reception, and the status word provides the information concerning register status and transmission errors. Figure 16.15 shows the definitions of these words.

To initialize the 8251A in the asynchronous mode, a certain sequence of control words must be followed. After a Reset operation (system Reset or through instruction), a mode word must be written in the control register followed by a command word. Any control word written into the control register immediately after a mode word will be interpreted as a command word; that means a command word can be changed anytime during the operation. However, the 8251A should be reset prior to writing a new mode word, and it can be reset by using the Internal Reset bit (D_6) in the command word.

16.42 Illustration: Interfacing an RS-232 Terminal Using the 8251A

PROBLEM STATEMENT

1. Identify the port addresses of the control register, the status register, and the data register in Figure 16.16.
2. Explain the RS-232 signals and the operations of the line driver (MC 1488) and the line receiver (MC 1489) shown in Figure 16.16.
3. Specify the initialization instructions and the status word to transmit characters with the following parameters if the transmitter clock frequency (TxC) is 153.6 kHz.
 - Asynchronous mode with 9600 baud
 - Character length = seven bits and two Stop bits
 - No parity check