solve dma (../12549/solve-dma)

+3 votes

664 views

Consider a system in which cycle takes 500 ns. Transfer of bus control in either direction, from processor to I/O device or vice versa, takes 250 ns. One of the I/O device has a data transfer rate of 50 kB/s and employees DMA. Data are transferred one byte at a time. For how long (in ms) would the device tieup the bus when transferring block of 128 bytes.??

(../user/focus+_GATE)

asked (../12549/solve-dma) **Jul 2, 2015** in **CO & Architecture (../co-and-architecture)** by **focus _GATE (../user/focus+_GATE) Boss** (22.1k points) | 664 views

Answer | Comment

0

Do you have an answer key for this question ?

commented (../12549/solve-dma?show=12623#c12623) Jul 2, 2015 by **Pranay Datta 1 (../user/Pranay+Datta+1) Boss**

(../user/Pranay+Datta+1)

Reply

0

Below answer is correct

commented (../12549/solve-dma?show=12649#c12649) Jul 3, 2015 by **focus _GATE (../user/focus+_GATE) Boss**

(../user/focus+_GATE)

Reply

0

Generally they is give you the DMA transfer time IO to MM . in this case they said nothing and this is done by this way DMA controls the bus until the whole block is transferred . If that`s the case then its correct (but should have mentioned it) .

commented (../12549/solve-dma?show=12652#c12652) Jul 3, 2015 by **Pranay Datta 1 (../user/Pranay+Datta+1) Boss**

(../user/Pranay+Datta+1)

Reply

0

why is transfer time included in the time the bus is tied up by IO?? sometimes they include only the bus transfer time in the bus tie up time and sometimes the transfer time also?? can someone clear this??

commented (../12549/solve-dma?show=77678#c77678) Oct 30, 2016 by **sushmita (../user/sushmita) Boss**
edited Oct 30, 2016 by **sushmita (../user/sushmita)**

(../user/sushmita)

Reply

2 Answers

+4 votes

Best answer

Steps :

1) 1 Byte data is read into the DMA Controller's buffer (During this time, the CPU has the control of the bus, so we don't take this time into consideration).

2) Take the bus from CPU = 250ns

3) Transfer the Byte = 500ns

4) Give the control back to the processor = 250ns

Total time of bus tie up for 1 Byte = (250 + 250 + 500) ns = ***1000ns***

Time for 128 Bytes is 128000ns or 0.128ms

See 11th solution part b : http://www.krchowdhary.com/co/ttut5-sol.pdf (http://www.krchowdhary.com/co/ttut5-sol.pdf)

(../user/Uzumaki+Naruto)
answered (../12549/solve-dma?show=96899#a96899) **Dec 26, 2016** by **Uzumaki Naruto (../user/Uzumaki+Naruto) Active** (2.5k points)
selected **Dec 29, 2016** by **vijaycs (../user/vijaycs)**

Comment

+2 votes

Device set up time 500ns..

Time to transfer 128 byte = 128/50*1024 s = 1/400 s = 2.5 Milli second

Transfer time (in milli second) >>> Setup time (in nano second) // ignore setup time

Total time = 2.5 Milli second

(../user/Digvijay+Pandey)
answered (../12549/solve-dma?show=12553#a12553) **Jul 2, 2015** by **Digvijay Pandey (../user/Digvijay+Pandey) Veteran** (54.4k points)

Comment

0

in this type how we can think that they are asking about TRANSFER TIME.?? :(

commented (../12549/solve-dma?show=12555#c12555) Jul 2, 2015 by **focus _GATE (../user/focus+_GATE) Boss** (../user/focus+_GATE)

Reply

0

Device transfer will be done in 2.56 ms ,but at 2.56 time ,device has just finished preparing last byte.Now we need one extra memory cycle to transfer that byte?Why aer we not adding that?

commented (../12549/solve-dma?show=130712#c130712) May 24, 2017 by **rahul sharma 5 (../user/rahul+sharma+5) Boss** (../user/rahul+sharma+5)

Reply

← Prev. Qn. in Sub. (../12286/explain)

Next Qn. in Sub. → (../12746/total-size-of-cache)

← Prev. (../12548/comment)

Next → (../12556/solve)

Related questions

DMA Cycle Stealing Mode

In the last step shouldn't it be (Y/X) and not (Y/X+Y) since its Cycle Stealing mode? (../199315/dma-cycle-stealing-mode)

+3 votes | 0 answers

asked Jan 24 in **CO & Architecture (../co-and-architecture)** by **vishal chugh (../user/vishal+chugh)** Active (../user/vishal+chugh)

(1.6k points) | 98 views

dma (../tag/dma) co-and-architecture (../tag/co-and-architecture)

1

DMA Controller

(../195320/dma-controller)

+2 votes | 0 answers

asked Jan 15 in **CO & Architecture (../co-and-architecture)** by **vishal chugh (../user/vishal+chugh)** Active (../user/vishal+chugh)

(1.6k points) | 47 views

dma (../tag/dma) computer-architecture (../tag/computer-architecture)

2

DMA Self Doubt

A device has been used in DMA. A word of 4 bytes can be transferred when it is available. The memory cycle time is 40 ms and CPU is idle for 10% of its time. What is the data transfer rate of the device for Burst mode and Cycle stealing mode. I'm getting Burst mode - 11.11 B/s Cycle stealing - 10 B/s Is it correct?? (../192065/dma-self-doubt)

+2 votes | 0 answers

asked Jan 9 in **CO & Architecture (../co-and-architecture)** by **Ashwin Kulkarni** (../user/Ashwin+Kulkarni)

(../user/Ashwin+Kulkarni) Boss (17.4k points) | 194 views

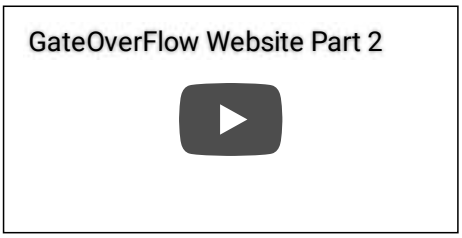
dma (../tag/dma) cycle-stealing (../tag/cycle-stealing) burst-mode (../tag/burst-mode) co-and-architecture (../tag/co-and-architecture)

3

Tag Search

Recent Posts

- COAP 2018 is now open for Registration (https://gateoverflow.in/blog/4126/coap-2018-is-now-open-for-registration)
- ISRO and IIIT-H hall tickets are out! (https://gateoverflow.in/blog/4124/isro-and-iiit-h-hall-tickets-are-out)
- Applying through previous year (https://gateoverflow.in/blog/4111/applying-through-previous-year)
- Power Transmission of Uttarakhand Corporation Limited(PTCUL) (https://gateoverflow.in/blog/4109/power-transmission-uttarakhand-corporation-limited-ptcul)
- barc 2018 paper analysis (https://gateoverflow.in/blog/4082/barc-2018-paper-analysis)



G GATE Overflow YouTube 973

All categories (../)

General Aptitude (../general-aptitude)	1.2k
Engineering Mathematics (../mathematics)	4.9k
Digital Logic (../digital-logic)	2k
Programming & DS (../programming-in-c)	3.6k
Algorithms (../algorithms)	3k
Theory of Computation (../theory-of-computation)	3.8k
Compiler Design (../compilers)	1.5k
Operating System (../operating-system)	2.7k
Databases (../databases)	2.9k
CO & Architecture (../co-and-architecture)	2.5k
Computer Networks (../computer-networks)	2.9k
Non GATE (../out-of-syllabus-now)	947
Others (../others)	1.2k
Admissions (../admissions)	374
Exam Queries (../exam-queries)	418
Tier 1 Placement Questions (../tier-1-placement-questions)	17
Job Queries (../job-queries)	54
Projects (../projects)	9

(//plus.google.com/u/0/118015014826045574666?prsrc=3) Follow @csegate (https://twitter.com/csegate)

Gatecse (https://www.facebook.com/gateoverflow)

Recent Blog Comments

Congrats and all the best for all your future ... (https://gateoverflow.in/blog/4109/?show=4128#c4128)

Thank you Satyajeet, Rahul and chalam. Do I need ... (https://gateoverflow.in/blog/4111/?show=4127#c4127)

Thanku For Sharing (https://gateoverflow.in/blog/4124/?show=4125#c4125)

no (https://gateoverflow.in/blog/4109/?show=4123#c4123)

nups.... (https://gateoverflow.in/blog/4109/?show=4122#c4122)

34,545 Questions 41,442 Answers 117,733 Comments 40,304 Users