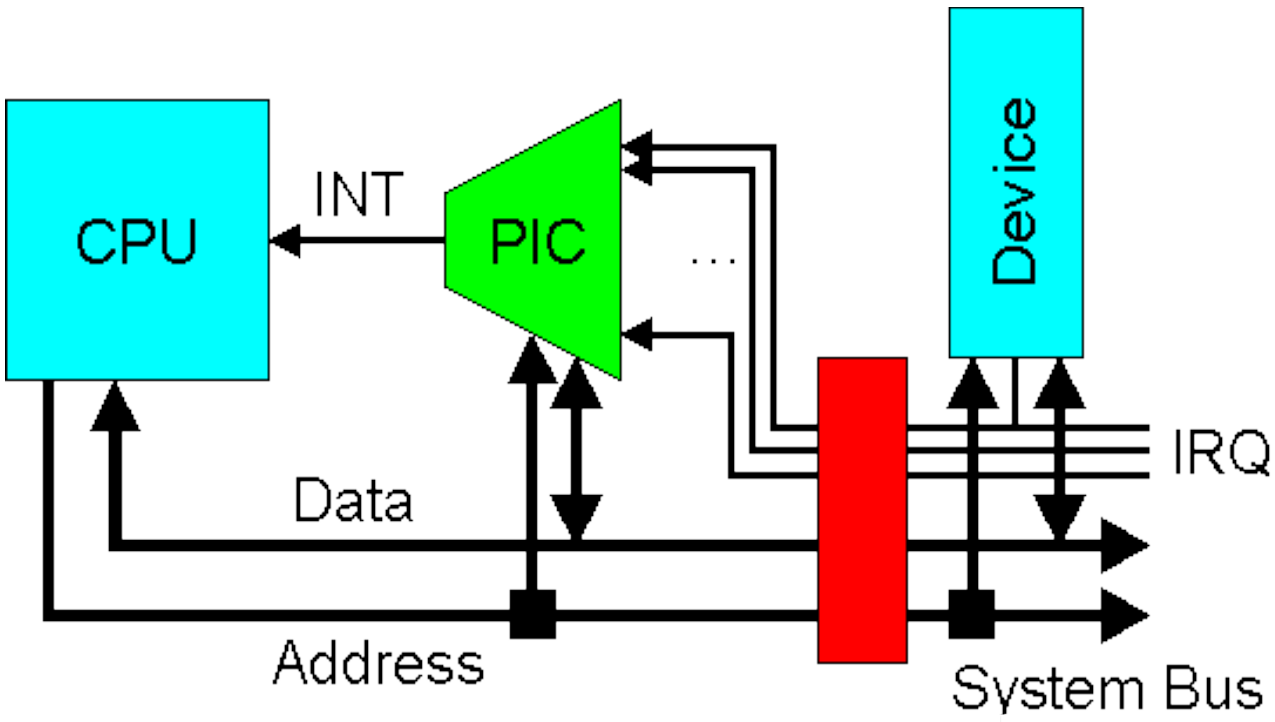
COMPUTER ORGANIZATION AND ARCHITECTURE

Sheet chapter 4

بنات هذا حلي مو حل الاستاذه اللي حابه تذاكر منه تذاكر بس مو اذا صار فيه شي خطا تقولون افراح نزلته بالموقع

انا كنت اكتب معاها الحل تقريبا كله صح بس يمكن طريقة الحل تختلف فنزلته لكم من باب المساعده واتمنى ماتحملوني مسؤلية الحل اول استاذه ايمان ماترسل الحل برفعه لكم بس هذا الحل خذوه مبدئيا لان مافيه وقت تذاكرون

تحياتي افراح



4.1 A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.

Number of set=16 → 4 lines

Number of block in main memory=size of memory/size of block

Size of memory = Number of block in main memory× size of block

Size of memory=$2^2 \times 2^{10} \times 2^7$

Size of memory=2^{19}

Tag	Set	Size of block

Size of block = 128=2^7 -> so size of block=7

Tag= size of memory – set – size of block

Tag=19-4-7

Tag=8

Tag	Set	Size of block
8	4	7

4.2 A two-way set-associative cache has lines of 16 bytes and a total size of 8 kbytes.The 64-Mbyte main memory is byte addressable. Show the format of main memory addresses.

Set 1	Block 1	Block 2
Set 2	Block 3	Block 4
Set 3	Block 5	Block6
Set 4	Block7	Block8
Set 5	Block9	Block10
Set 6	Block11	Block12
Set 7	Block13	Block14
Set 8	Block 15	Block16

Total block in the cache= 8kbytes/16 bytes=$2^3 \times 2^{10}/2^4=2^9$= 512

Number of set =number of block in cache/2

Number of set=512/2

Number of set in cache=256

Number of set in cache =2^8

Number of set=8

Size block=16=2^4

Size of memory=$2^6 \times 2^{20}=2^{26}$

Tag= size of memory – set-size of block

Tag=26-8-4

Tag=14

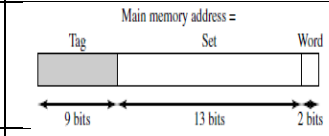
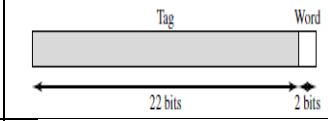
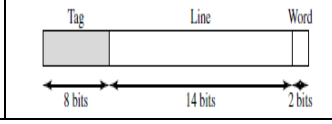
tag	set	Size of block
14	8	4

4.3 For the hexadecimal main memory addresses 111111, 666666,BBBBBB, show the following information, in hexadecimal format:

a. Tag, Line, and Word values for a direct-mapped cache, using the format of Figure 4.10

b. Tag and Word values for an associative cache, using the format of Figure 4.12

c. Tag, Set, and Word values for a two-way set-associative cache, using the format of Figure 4.15

	Figure	111111	666666	BBBBBB
a		11-444-1	66-1999-2	BB-2EEE-3
b		44444-1	199999-2	2EEEEE-3
c		22-444-1	CC-1999-2	177-EEE-3

4.5 Consider a 32-bit microprocessor that has an on-chip 16-KByte four-way set-associative cache. Assume that the cache has a line size of four 32-bit words. Draw a block diagram of this cache showing its organization and how the different address fields are used to determine a cache hit/miss.Where in the cache is the word from memory location ABCDE8F8 mapped?

Size of address CPU=32 bit

Total Block in cach=16k/16

Total Block in cache=$2^4 \times 2^{10}/2^4=2^{10}$= 1024

Number of set in cache=total block/4

Number of set in cache=1024/4

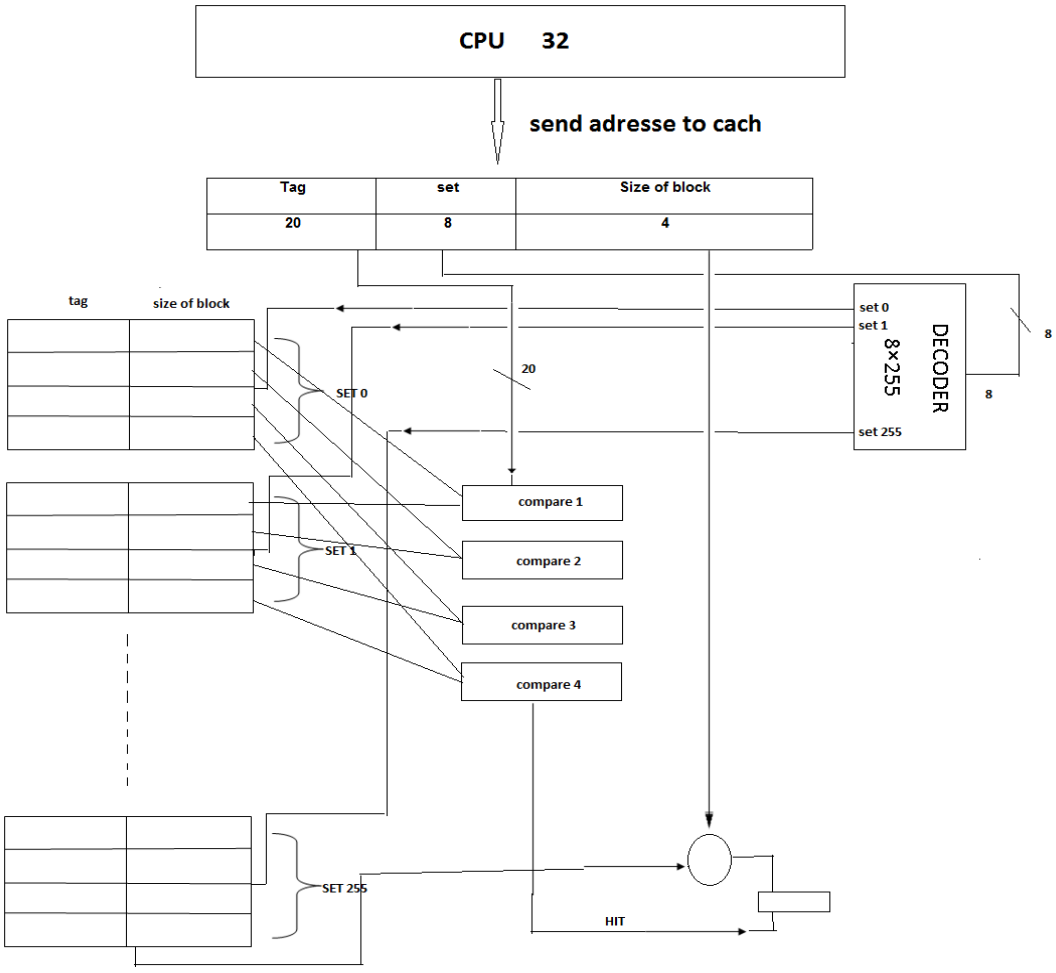
Number of set in cache=256=2^8

Size of block =16=2^4

Tag= Size of address CPU-set-size of block

Tag=32-8-4=20

Tag	set	Size of block
20	8	4



Where in the cache is the word from memory location ABCDE8F8 mapped?

Tag 20	Set 8	Size 4
1010 1011 1100 1101 1110	1000 1111	1000

So we select set 143 because the input to decoder is 10001111 and the output from decoder is set 143

4.8 Consider a machine with a byte addressable main memory of 216 bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.

a. How is a 16-bit memory address divided into tag, line number, and byte number?

Tag	line	Size
8	5	3

b. Into what line would bytes with each of the following addresses be stored?

0001 0001 0001 1011
1100 0011 0011 0100
1101 0000 0001 1101
1010 1010 1010 1010

0001 0001 0001 1011	Line 3
1100 0011 0011 0100	Line 6
1101 0000 0001 1101	Line 3
1010 1010 1010 1010	Line 21

c. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache.What are the addresses of the other bytes stored along with it?

0001 1010 0001 1111 stored in the cach

d. How many total bytes of memory can be stored in the cache?

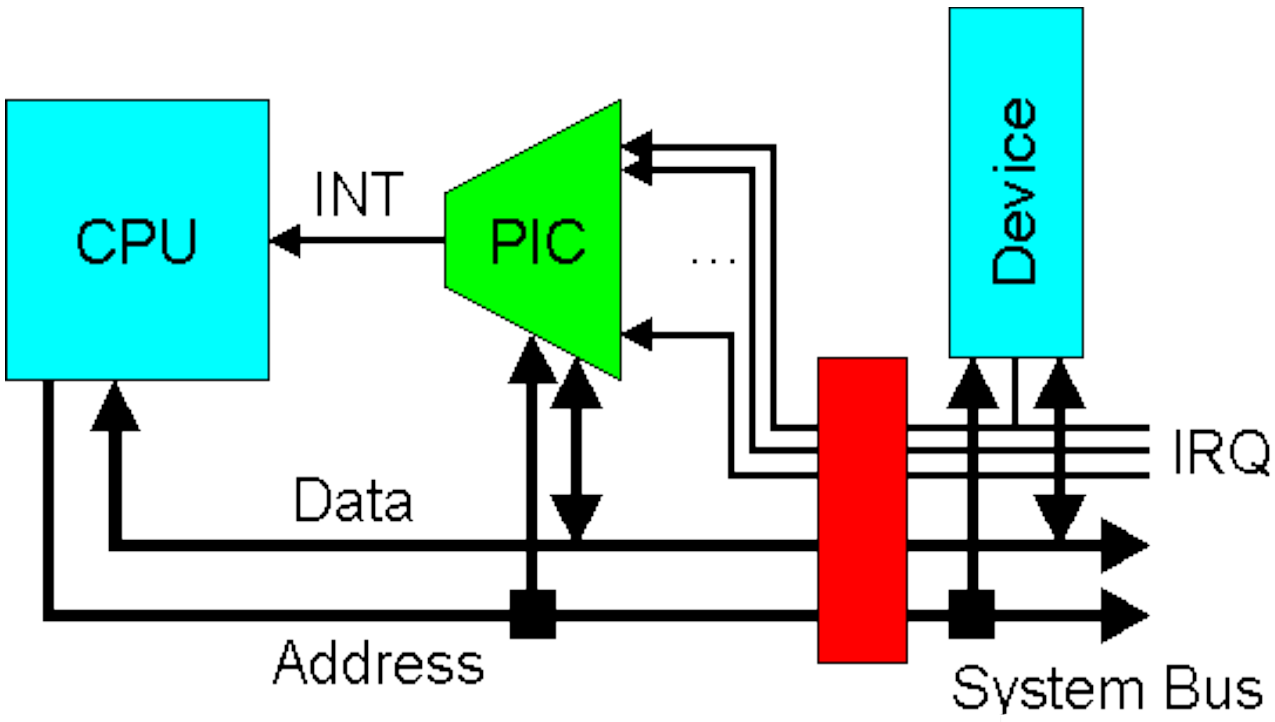
2^8=255 byte

e. Why is the tag also stored in the cache?

The tag is used to distinguish between two items with two different memory addresses Because it can stored in the same place in the cache

COMPUTER ORGANIZATION AND ARCHITECTURE

Sheet chapter 5



5.2 Consider a dynamic RAM that must be given a refresh cycle 64 times per ms. Each refresh operation requires 150 ns; a memory cycle requires 250 ns.What percentage of the memory's total operating time must be given to refreshes?

1ms→ refrech=64×150×10^{-6} =0.0096 Almost 1%

5.11 Suppose an 8-bit data word stored in memory 11000010. Using the Hamming algorithm, determine what check bits would be stored in memory with the data word.

M=8

2^k-1>=k+m

2^4-1>=4+8

15>=12

1	2	3	4	5	6	7	8	9	10	11	12
1	0	1	1	1	0	0	1	0	0	1	0

The check bits are in bit numbers 1, 2,4, and 8.
Check bit 8 calculated by values in bit numbers: 9,10,11, and 12
Check bit 4 calculated by values in bit numbers: 5,6,7 and 12
Check bit 2 calculated by values in bit numbers: 3,6,7,10 and 11
Check bit 1 calculated by values in bit numbers: 3,5,7,9,10 and 11
Thus, the check bits are:1011

5.12 For the 8-bit word 00111001, the check bits stored with it would be 0111. Suppose when the word is read fro memory, the check bits are calculated to be 1101.What is the data word that was read from memory?

0111

XOR

1101

1010=5 IN DICIMAL

SO the date read is 00110011 from 00111011