Computer Science Portfolio

Review questions chapter 3

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Review questions

1. What general categories of functions are specified by computer instructions? The categories are processor-memory, processor-I/O, data processing, and c ontrol.

2. List and briefly define the possible states that define an instruction execution.

Instruction address calculation(iac): Determine the address of the next instruction to be executed.

Instruction fetch (if): Read instruction from its memory location into the processor.

Instruction operation decoding: Analyze instruction to determine type of operation to be performed and operands to be used.

Operand address calculation (oac): If the operation involves reference to an operand in memory or available via I/O, then determine the address of the operand.

Operand fetch (of): Fetch the operand from memory or read it in from I/O.

Data operation: Perform the operation indicated in the instruction.

Operand store (os): Write the result into memory or out to I/O.

3. List and briefly define two approaches to dealing with multiple interrupts.

Disabling interrupts- processor has the ability to and will ignore the specific interrupts. Those interrupts remain pending and will be checked after the processor has enabled interrupts.

Interrupt service routine(ISR) - priorities assigned to the different types of interrupts. Interrupt service routines with higher priorities can interrupt ones with lower priority, in which case the ISR with the lower priority is put on the stack until that ISR is completed.

4. What types of transfers must a computer's interconnection structure (e.g. bus) support? Memory to processor, processor to memory, I/O to processor, processor to I/O, and I/O to or from memory.

5. What is the benefit of using a multiple-bus architecture compared to a single-bus architecture? It is efficient, since if only one bus is for everything, only one device can then communicate at a time, since if more than one device were to try and send data on the single bus, transmission would be garbled.

6. List and briefly define the QPI protocol layers.

Physical: Consists of the actual wires carrying the signals, as well as circuitry and logic to support ancillary features required in the transmission and receipt of the 1s and 0s.

Link: Responsible for reliable transmission and flow control.

Routing: Provides the framework for directing packets through the fabric.

Protocol: The high-level set of rules for exchanging packets of data between devices.

7. List and briefly define the PCIe protocol layers.

Physical: Consists of the actual wires carrying the signals, as well as circuitry and logic to support ancillary features required in the transmission and receipt of the 1s and 0s.

Data link: responsible for reliable transmission and flow control.

Transmission: Generates and consumes data packets sued to implement load/store data transfer mechanisms and also manages the flow control of those packets between the two components on a link.

Problems Chapter 3

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3. Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

a. What is the maximum directly addressable memory capacity (in bytes)? 16,777,216 bytes (16 Mbytes)

b. Discuss the impact on the system speed if the microprocessor bus has

1. a 32-bit local address bus and a 16-bit local data bus, or

2. a 16-bit local address bus and a 16-bit local data bus.

With a 32-bit local address bus and a 16-bit local data bus, it would take 2 cycles to fetch the 32 bit instruction. A 16-bit local address bus would slow down operation due to only being able to pass half the instruction a cycle.

c. How many bits are needed for the program counter and the instruction register? 24 bits.

5. Consider a 32-bit microprocessor, with a 16-bit external data bus, driven by an 8-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the maximum data transfer rate across the bus that this microprocessor can sustain in bytes/s? To increase its performance, would it be better to make its external data bus 32 bits or to double the external clock frequency supplied to the microprocessor? State any other assumptions you make, and explain. *Hint:* Determine the number of bytes that can be transferred per bus cycle.

Input clock cycle = 8 /4 = 2MHz.

width = 16, bus cycle=2. 16 * 2Mhz = 32,000,000 bits/sec = 4,000,000 bytes per sec. (1byte = 8 bits)

To increase performance, it would be better to make the external bus 32 bits. This would double the bit rate across the external bus.

9. The VAX SBI bus uses a distributed, synchronous arbitration scheme. Each SBI device (i.e., processor, memory, I/O module) has a unique priority and is assigned a unique transfer request (TR) line. The SBI has 16 such lines (TR0, TR1, …, TR15) with TR0 having the highest priority. When a device wants to use the bus, it places a reservation for a future time slot by asserting its TR line during the current time slot. At the end of the current time slot, each device with a pending reservation examines the TR lines; the highest-priority device with a reservation uses the next time slot.

A maximum of 17 devices can be attached to the bus. The device with priority 16 has no TR line. Why not?

The device with priority 16 has the lowest priority, so it doesn't need a TR line. It can run when there is nothing else with a reservation, it can use a time slot.

14. A microprocessor has an increment memory direct instruction, which adds 1 to the value in a memory location. The instruction has five stages: fetch opcode (four bus clock cycles), fetch operand address (three cycles), fetch operand (three cycles), add 1 to operand (three cycles), and store operand (three cycles).

a. By what amount (in percent) will the duration of the instruction increase if we have to insert two bus wait states in each memory read and memory write operation?

8 wait states added, since there are 4 memory operations dealing with read and write. 16 cycles per instruction.
(8/16) * 100 = 50%

b. Repeat assuming that the increment operation takes 13 cycles instead of 3 cycles.

Now 26 cycles per instruction (10 more cycles added to increment). (8/26) * 100 =30.8%

15. The Intel 8088 microprocessor has a read bus timing similar to that of Figure 3.18, but requires four processor clock cycles. The valid data is on the bus for an amount of time that extends into the fourth processor clock cycle. Assume a processor clock rate of 8 MHz.

a. What is the maximum data transfer rate?

b. Repeat but assume the need to insert one wait state per byte transferred.

a. 8 MHz with a requirement for 4 processor clock cycles.
8MHz / 4 = 2Mhz

   2Mhz * 8bits = 16,000,000 bits/sec = 2,000,000 bytes / 1024 bytes = 1953.125 Kbytes / 1024 Kbytes = 1.907 MB/sec.

b. 8,000,000 / 5 = 1,600,000 * 8 = 12,800,000 / 8 = 1,600,000 / 1024 = 1562.5 Kbytes / 1024 Kbytes = 1.5 Mbytes / sec.

17. Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 20% of the operands and instructions are 32 bits long, 40% are 16 bits long, and 40% are only 8 bits long. Calculate the improvement achieved when fetching instructions and operands with the 32-bit microprocessor.

20% 32 bit long

40% 16 bit long

40% 8 bit long

16 bit machine

20*2 = 40 (two cycles per 32-bit instruction)

40 = 40

40 = 40

120

32 bit machine

20 = 20

40 = 40

40 = 40

100

improvement of 20 over the 16 bit machine

20 / 120 = 2 / 12 = 1 / 6 = 16.7%

18. The microprocessor of Problem 3.14 initiates the fetch operand stage of the increment memory direct instruction at the same time that a keyboard actives an interrupt request line. After how long does the processor enter the interrupt processing cycle? Assume a bus clocking rate of 10MHz.

1 / 10,000,000 = .0000001 = 100 nanoseconds.

Fetch opcode = 4 cycles

Fetch operand address = 3 cycles

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activated interrupt at fetch operand.

Fetch operand = 3 cycles

add 1 to operand = 3 cycles

store operand = 3 cycles

9 cycles til it enters the interrupt processing cycle.

9 * 100 nanoseconds = 900 nanoseconds til it enters interrupt processing cycle.

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