TAO1221 Computer Architecture and Organization

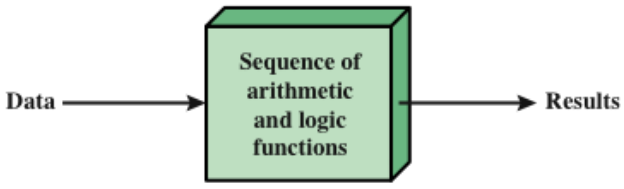
Lab03

Part 1: Discussion

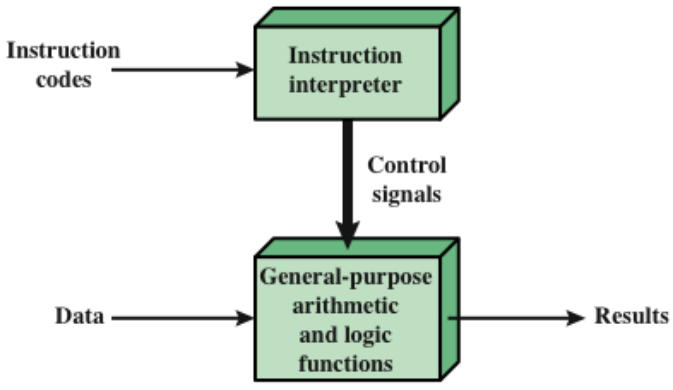
1. What general categories of functions are specified by computer instructions?

   - **Processor-memory**: Data may be transferred from processor to memory or from memory to processor.
   - **Processor-I/O**: Data may be transferred to or from a peripheral device by transferring between the processor and an I/O module.
   - **Data processing**: The processor may perform some arithmetic or logic operation on data.
   - **Control**: An instruction may specify that the sequence of execution be altered.

2. Differentiate between *programming in hardware* and *programming in software*.
   a) Programming in hardware means configuring a small set of basic logic components specifically for aparticularcomputation.
   b) Programming in software means supplying a specific set of control signals to a general-purpose hardware.



(a) Programming in hardware



(b) Programming in software

3. List and briefly define two approaches to dealing with multiple interrupts.

   - Disable all interrupts while an interrupt is being processed.
   - Define priorities for interrupts and to allow an interrupt of higher priority to cause a lower-priority interrupt handler to be interrupted.

4. Briefly explain the transfers that must be supported by interconnection structure (e.g. bus).

   - **Memory to processor**: The processor reads an instruction or a unit of data from memory.
   - **Processor to memory**: The processor writes a unit of data to memory.
   - I/**O to processor**: The processor reads data from an I/O device via an I/O module.
   - **Processor to I/O**: The processor sends data to the I/O device.
   - **I/O to or from memory**: For these two cases, an I/O module is allowed to exchange data directly with memory, without going through the processor, using direct memory access (DMA).

5. What is the benefit of using multiple-bus architecture compared to single-bus architecture?

   With multiple buses, there are fewer devices per bus. This:
   (1) reduces propagation delay, because each bus can be shorter, and
   (2) reduces bottleneck effects.

6. Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.
   a) What is the maximum directly addressable memory capacity (in bytes)?
   b) Discuss the impact on the system speed if the microprocessor bus has:
      i. a 32-bit local address bus and a 16-bit local data bus, or
      ii. a 16-bit local address bus and a 16-bit local data bus.
   c) How many bits are needed for the program counter and the instruction register?

   Answers:
   a) 2^{24} = 16 Mbytes
   b) The impact:
      i. If the local address bus is 32 bits, the whole address can be transferred at once and decoded in memory. However, because the data bus is only 16 bits, it will require 2 cycles to fetch a 32-bit instruction or operand.
      ii. The 16 bits of the address placed on the address bus can't access the whole memory. Thus a more complex memory interface control is needed to latch the first part of the address and then the second part (because the microprocessor will end in two steps). For a 32-bit address, one may assume the first half will decode to access a "row" in memory, while the second half is sent later to access a "column" in memory. In addition to the two-step address operation, the microprocessor will need 2 cycles to fetch the 32-bit instruction/operand.
   c) The program counter must be at least 24 bits. Typically, a 32-bit microprocessor will have a 32-bit external address bus and a 32-bit program counter, unless on-chip segment registers are used that may work with a smaller program counter. If the instruction register is to contain the whole instruction, it will have to be 32-bits long; if it will contain only the op code (called the op code register) then it will have to be 8 bits long.