Independent University, Bangladesh
Department of Computer Science and Engineering

Course Outline

Course Title: Computer Organization and Architecture
Course Code: CSE214, CSC 311
Spring 2018, STs at 8:0 a.m. (section-1) Room: 6009, Level 4,
Duration: 1:30 mnts

Instructor's details:

Mohammad Noor Nabi
Senior Lecturer
Office: Room-6005B, Visiting Hours: STs at 09:40 a.m. to 11:20 p.m. (or by appointment)
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Course Description

This is one of the core courses of Computer Science and Engineering with particular emphasis on computer organization and architecture; concept of computer as hierarchical system; and problems and methods of designing computers. The main objective of this course is to learn how certain operating system functions are supported by computer hardware organization. Understanding how various performance enhancements to computers are achieved and to be able to make an informed comparison among competing architectures for a given purpose.

Course Policy:

1. It is the student's responsibility to gather information about the assignments and covered topics during the lectures missed. Regular class attendance is mandatory. Points will be taken off for missing classes. Without 70% of attendance, sitting for final exam is NOT allowed. According to IUB system students must enter the classroom within the first 20 minutes to get the attendance submitted.
2. The date and syllabus of quiz, midterm and final exam is already given here, however, announcements will be given ahead of time. There is **NO** provision for make-up quizzes.
3. The reading materials for each class will be given prior to that class so that student may have a cursory look into the materials.
4. Class participation is vital for better understanding of sociological issues. Students are invited to raise questions.
5. Students should take tutorials with the instructor during the office hours. Prior appointment is required.
6. Students must maintain the IUB code of conduct and ethical guidelines offered by the school of engineering and computer sciences.

Assessment and Marks Distribution:

Students will be assessed on the basis of their overall performance in all the exams, quizzes, and class participation. Final numeric reward will be the compilation of:

- Three quizzes due in different times of the semester (30%)
- Two assignment (field based) (15%)
- One **mid-term** test (fourth week of June) (25%)
- A cumulative **final** exam (30%)

[Class attendance is mandatory; failure to do so may deduct the final marks]

Grade Conversion Scheme plan:
The following chart will be followed for grading. This has been customized from the guideline provided by the School of Engineering and Computer Science.

A	A-	B+	B	B-	C+	C	C-	D+	D	F
90-100	85-89	80-84	75-79	70-74	65-69	60-64	55-59	50-54	45-49	0-44

* Numbers are inclusive

Required Text:
The course will be based mostly on the following books [some other books and journals may be referred time to time]:

- William Stallings – Computer Organization and Architecture – Design for Performance – **[8th or later International Editions], Prentice Hall**
- John P. Hays – Computer Architecture and Organization – **[3rd or later International Editions] WCB/McGraw-Hill.**

Link to Virtual Learning System:
https://piazza.com/independent_university_bangladesh/spring2018/csc413cse315/home

Audit:
Students who are willing to audit the course are welcome during the first two classes and are advised to contact the instructor after that.

Note:
Plagiarism – that is, the presentation of another person's thoughts or words as though they were the student's own – must be strictly avoided. Cheating and plagiarism on exam and assignments are unacceptable.

University Regulation and Code of Conduct:
Please see the Green Book for further information about academic regulation and policies, including withdrawal and grading, appeals and penalties for plagiarism and academic misconduct.

Students with Disabilities:
Students with disabilities are required to inform the Department of Law of any specific requirement for classes or examination as soon as possible.

More Readings:

- John D. Carpinelli – Computer Systems Organization and Architecture – **[1st or later International Editions] Pearson**
- Hennessy and Peterson – Computer Architecture, A Quantitative Approach – **[4th or later International Editions] Elsevier**

Class & Exam Schedule plan, Topics and Readings:

Sessions	Topics	Learning Outcome	Readings
Session – 1	Introduction	1. Students will be able to know each other 2. Students will learn about the course policy 3. Students will be able to plan for the exams	
Session – 2	Key Concepts in Computer organization and architecture	1. Students will learn the background of organization and architecture 2. They will be able to categorize structure and function of computer 3. They will be able to focus on CPU and control unit,	Handout (available on Virtual Learning System) Stallings, Ch-1
Session – 3	Key Concepts in Computer Evolution and Performance	1. They will be able to learn computer evolution. 2. . They will be able to categorize design and performance 3. Students will be able to know The Von Neumann Machine and structure of IAS computer.	Handout (available on Virtual Learning System) Stallings, Ch-2
Session – 4	Key concepts and top level view of computer function and interconnection	1. Students will learn about computer components and instruction cycle states 2. Students will learn about interrupts systems use in efficient use of computing resources. 3. They will learn interconnection structures	Handout (available on Virtual Learning System) Stallings, Ch-3
Session – 5	Key concepts and top level view of computer function and interconnection **Quiz 1 due** [**Assignment]**	1. The will be able know issues regarding multiple bus hierarchies and bus arbitration. 2. Students will be able to know different bus operations 3. They will be able to know PCI and other bus architectures.	Handout (available on Virtual Learning System) Stallings, Ch-3
Session – 6	Internal Memory: Cache Memory	1. Students learn about characteristics of memory systems and the memory hierarchy 2. They will know about cache memory principles and elements of cache memory design 3. They will learn about cache memory mapping	Handout (available on Virtual Learning System) Stallings, Ch-4
Session – 7	Internal Memory: Cache Memory	1. Students will learn about direct , associative and set associative cache memory design 2. They will learn about replacement algorithms 3. They will learn about writing policies and cache coherence issues in multiprocessor cache design	Handout (available on Virtual Learning System) Stallings, Ch-4
Session – 8	Internal Memory: Main Memory	1. Students will learn about DRAM versus SRAM and use of different type of ROM.	Handout (available on Virtual Learning System)

		2. They will learn chip logics and packaging of RAM and ROM 3. They will learn about memory module organization	Stallings, Ch-5
Session – 9	Internal Memory: Main Memory	1. Students will learn error correction technique: parity method. 2. They will learn about hamming code for single bit error correction and double bit error detection. 3. They will know Advance DRAM organization: SDRAM, DDR1, DDR2, DDR3 DDR4 and cached DRAM	Handout (available on Virtual Learning System) Stallings, Ch-5
Session – 10	External Memory	1. Students will learn magnetic disk: Read and Write mechanisms. 2. They will learn about data organization and formatting. 3. They will learn about physical characteristics and disk performance parameters.	Handout (available on Virtual Learning System) Stallings, Ch-6
Session – 11	External Memory	1. Students learn about RAID technologies. 2. They will learn about optical memory devices: CD, DVD, Blue ray etc. 3. They learn about Magnetic tape memory organization.	Handout (available on Virtual Learning System) Stallings, Ch-6
Session – 12	Input / Output	1. They will learn about generic models of I/O module and external devices. 2. Students will learn major functions and structure of I/O module. 3. They will learn about different I/O techniques including programmed I/O, Interrupt I/O and DMA	Handout (available on Virtual Learning System) Stallings, Ch-7
Session – 13	Input / Output	1. Students will learn about I/O module design issues. 2. They will learn about programmable interrupt controller (8259) and programmable peripheral interface(8255) 3. They will learn about DMA configuration, DMA module (8237) and I/O channels and I/) channels and processors.	Handout (available on Virtual Learning System) Stallings, Ch-7
Session – 14	**Mid-term test (Class Time)**	1. Internal Memory: Cache Memory 2. External Memory 3 Input / Output	Stallings, Chapter-4, 5 and 6
Session – 15	Computer Arithmetic	1. Students will learn about arithmetic logic unit. 2. They will learn about signed and unsigned	Handout (available on Virtual Learning System)

		integer representation issues. 3. They will learn about hardware algorithms for addition, subtraction multiplication and division.	Stallings, Ch-9
Session – 16	Computer Arithmetic **Quiz 2 due**	1. Students will learn about fixed and floating point representation. 2. They will learn about IEEE standard for binary floating point representation. 3. They will learn floating point arithmetic.	Handout (available on Virtual Learning System) Stallings, Ch-9
Session – 17	Computer Arithmetic [**Assignment]**	1. Students will learn about hardware algorithms for floating point addition and subtraction. 2. They will learn about hardware algorithms for floating point multiplication and division 3. They will learn about rounding and IEEE standard for binary floating point arithmetic.	Handout (available on Virtual Learning System) Stallings, Ch-9
Session – 18	Processor Structure and Function	1. Students will learn about processor organization and data flow during fetch cycle, indirect cycle and execute cycles. 2. They will learn about instruction pipelining strategies. 3. They will learn about speed up using pipeline.	Handout (available on Virtual Learning System) Stallings, Ch-12
Session – 19	Processor Structure and Function **Quiz 3 due**	1. Students will learn about pipeline hazards. 2. They will learn branch prediction strategies.	Handout (available on Virtual Learning System) Stallings, Ch-12
Session – 20	Reduced Instruction Set Computers	1. Students will learn about RISC instruction execution characteristics. 2. They will learn about use larger register file issues and compiler-based register optimization 3. They will learn RISC versus CISC characteristics.	Handout (available on Virtual Learning System) Stallings, Ch-13
Session – 21	Control Unit design	1. Students will learn about Micro-operations. 2. They will learn about micro-operations timing states during fetch, indirect, interrupt and execute sub cycles. 3. They will learn about flow chart of instruction cycle micro operations.	Handout (available on Virtual Learning System) Stallings, Ch-15
Session – 22	Control Unit design	1. Students will learn about functional requirement of control unit design. 2. They will learn about generation control unit signals. 3. They will learn about sequencing of control signals.	Handout (available on Virtual Learning System) Stallings, Ch-15
Session – 23	Micro programmed control unit	1. Students will learn about basic concepts micro	Handout (available on

		instruction and its format in micro-programmed control unit. 2. They will learn about organization of control memory and functioning of micro-programmed control unit including wilkies micro-programmed control unit. 3. They will learn about micro-instruction sequencing and micro-instruction execution.	Virtual Learning System) Stallings, Ch-16
Session – 24	Multi core computers	1. Students will learn about hardware performance issues: pipelining, superscalar, and symmetric multithreading. 2. They will learn about Software performance issues on multi-core. 3. They will learn about multi-core organization includes Intel X86 multi-core organizations: core duo, core i3 and core i7.	Handout (available on Virtual Learning System) Stallings, Ch-18
Session – 25	Self Study and Revision		
Session – 26	**Final Exam**	1. Computer Arithmetic 2. Processor Structure and Function 3. Reduced Instruction set computers 4. Control Unit design 5. Micro programmed control unit 6. Multi core computers	Stallings, Chapter-9, 12, 13, 15, 16 and 18