co_williams (../158967/co_williams)

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A system is based on an 8-bit microprocessor and has two I/O devices. The I/O controllers for this system use separate control and status registers. Both devices handle data on a 1-byte-at-a-time basis.The first device has two status lines and three control lines.The second device has three status lines and four control lines.
a. How many 8-bit I/O control module registers do we need for status reading and control of each device?
b. What is the total number of needed control module registers given that the first device is an output-only device?
c. How many distinct addresses are needed to control the two devices?

asked (../158967/co_williams) **Oct 10, 2017** in **CO & Architecture (../co-and-architecture)** by **arch (../user/arch) Active** (3.9k points) | 👁 137 views
(../user/arch)

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1 Answer

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c)8 bit microprocessor . Each 4 bit can generate 1 memory addresses

by 4 bit we can generate 2^4 addresses.

then by 8 bit we can generate 2^8 addresses

a)Now

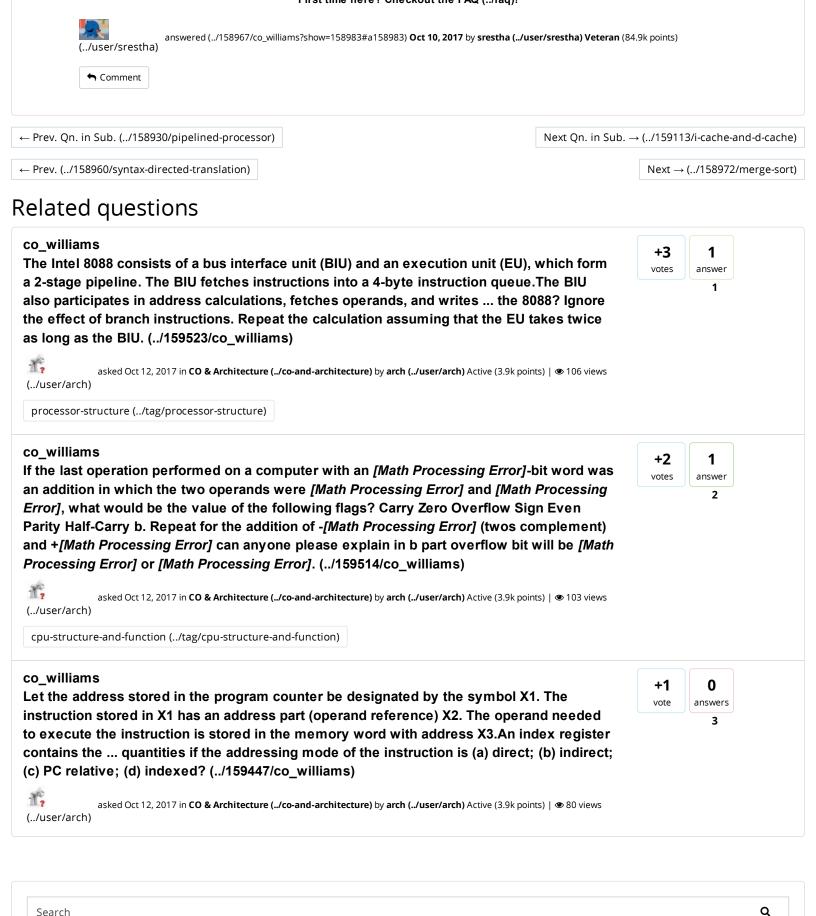The first device has 2 status lines and 3 control lines.

3 control line can generate 8 control signals.

So, **1 eight bit register** is enough to control 1st device

The second device has 3 status lines and 4 control lines.

4 control lines can generate 16 control signals

and for that we need **2 eight bit registers**

First time here? Checkout the FAQ (../faq)!   X

(../user/srestha)

answered (../158967/co_williams?show=158983#a158983) **Oct 10, 2017** by **srestha (../user/srestha) Veteran** (84.9k points)

↩ Comment

Related questions

co_williams

The Intel 8088 consists of a bus interface unit (BIU) and an execution unit (EU), which form a 2-stage pipeline. The BIU fetches instructions into a 4-byte instruction queue.The BIU also participates in address calculations, fetches operands, and writes ... the 8088? Ignore the effect of branch instructions. Repeat the calculation assuming that the EU takes twice as long as the BIU. (../159523/co_williams)

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asked Oct 12, 2017 in **CO & Architecture (../co-and-architecture)** by **arch (../user/arch)** Active (3.9k points) | 👁 106 views
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processor-structure (../tag/processor-structure)

co_williams

If the last operation performed on a computer with an *[Math Processing Error]*-bit word was an addition in which the two operands were *[Math Processing Error]* and *[Math Processing Error]*, what would be the value of the following flags? Carry Zero Overflow Sign Even Parity Half-Carry b. Repeat for the addition of -*[Math Processing Error]* (twos complement) and +*[Math Processing Error]* can anyone please explain in b part overflow bit will be *[Math Processing Error]* or *[Math Processing Error]*. (../159514/co_williams)

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cpu-structure-and-function (../tag/cpu-structure-and-function)

co_williams

Let the address stored in the program counter be designated by the symbol X1. The instruction stored in X1 has an address part (operand reference) X2. The operand needed to execute the instruction is stored in the memory word with address X3.An index register contains the ... quantities if the addressing mode of the instruction is (a) direct; (b) indirect; (c) PC relative; (d) indexed? (../159447/co_williams)

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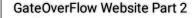Quick search syntax

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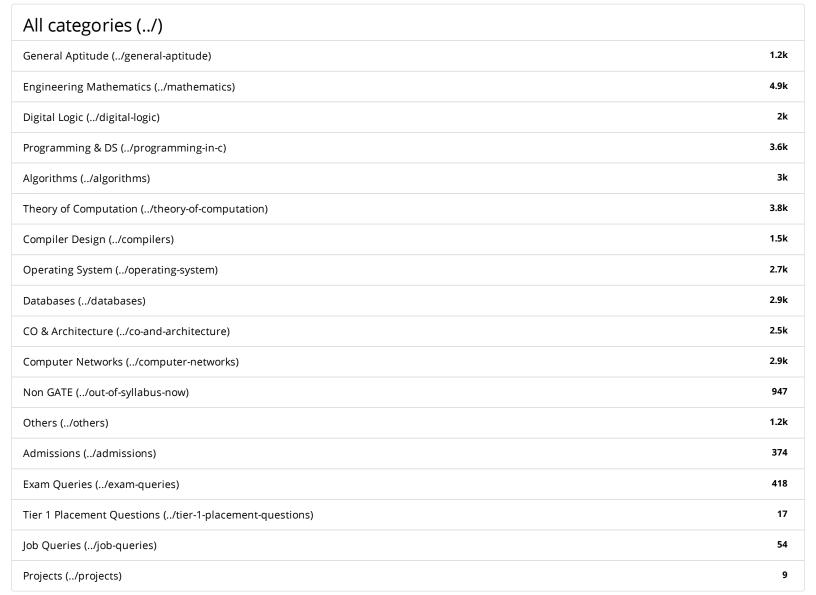barc 2018 paper analysis (https://gateoverflow.in/blog/4082/barc-2018-paper-analysis)

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