Ultra-Low Power Logic for Energy Harvesting Systems

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***Abstract*—In many logic systems the primary concern is not one of speed, but of power consumption. In these systems calculations may be required at a very low frequency, the calculations are likely to be fairly simple in nature, and the available power is minimal.**

In this paper, three different main types of low power logic are discussed; sub-threshold logic, adiabatic logic, and ultra-low-leakage logic. Their various advantages and disadvantages discussed, and variations upon each are looked at.

I. Introduction

There are many systems where processing ability comes second to power usage. Sensor systems, and energy harvesting systems fall well inside this category. In the majority of lower power systems in use, such as mobile devices, power availability is large, however energy availability is limited - the system can draw a large amount of current from the battery at any time, however when the battery runs out of power the system fails. In the systems focussed on in this report, energy availability is essentially infinite, however available current draw at any one time is minimal. Due to these restrictions various technologies have to be utilised to maximise power usage and still provide reasonable processing capabilities.

There are a variety of different energy harvesting mechanisms available and in use in modern systems. These suffer from many issues of energy availability, for instance any sensing or control electronics should not significantly cut down the supplied power. In sensing applications the energy harvesting does not want to affect the values under test, and as such supplied power can be incredibly low [1, 2]. [1] discuss a system whereby as little as 57.2µJ are generated over a 30 second period, this equates to less than 2µW of power. This is enough to power a single CMOS inverter using ultra-low-leakage technology, as Flandre et al. [3] states that the inverters require 1.1µW.

In standard CMOS designs energy is lost through switching and leakage currents. Leakage current is the current that passes from the channel in the transistors through to the gate, "leaking" across the junction. Energy lost through switching happens when the gate changes state. Due to the fast switching nature of the logic, there are time when the entire power supply voltage is across the channel of the transistor. This results in a large current flow through the transistor, and a large heat dissipation. This heat dissipation uses up a lot of energy.

In this report three main forms of energy saving techniques are described and compared, and variations on each type are also looked at. Section II looks at the use of sub-threshold logic, section III looks at adiabatic logic and energy recovery, and section IV looks at ultra-low-leakage logic.

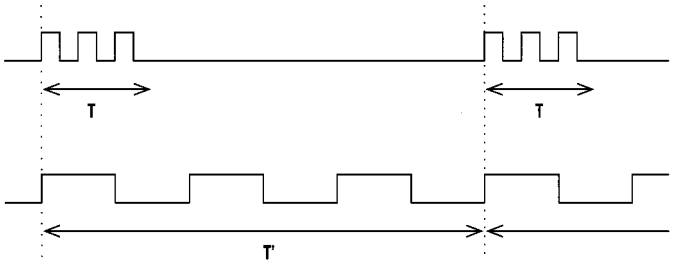

Fig. 1. Bursty computation and its relevance to subthreshold operation [5]

II. Sub-Threshold Logic

A. Design

Sub-threshold logic works by reducing the supply voltage to below the threshold voltage of the transistors. This uses the leakage current from gate to source as the switching current in the device [4]. The main form of current flow in the transistor is the current flowing between the drain and the source. In subthreshold systems the transistor is in very weak inversion, which means that the channel between the drain and source which is normally open in standard CMOS logic is closed off. This results in a fraction of the normal current flow than would normally be experienced, this is the 'leakage' current. As the leakage current is exponentially related to the gate voltage, reducing the voltage to below the devices threshold voltage results in the leakage current being greatly reduced. The knock-on effect of this is an exponential increase in delay can be expected.

The increase in the delay makes subthreshold logic very good for applications which require bursts of computation, spread out over a long period of time. An example of this can be seen in figure 1. The upper waveform shows the activity status of a standard CMOS logic gate operating in bursts, when the waveform is at the high level the transistor is active and when the waveform shows low the transistor is inactive. The lower waveform relates to the activity of a subthreshold circuit. Under these conditions the standard CMOS logic operates over a time T, in this way it rapidly completes the computation and then sits idle, until time T' has passed at which point the computation begins again. The subthreshold logic, needing longer to complete the calculation, is slowed to take the entirety of T' to complete. As such it achieves a large power reduction while providing the same throughput as its standard CMOS equivalent [5, 4].

In addition to the power saving there are a number of other advantages that subthreshold logic gives. One of these is an increase in the transconductance gain gm of the device. Under subthreshold operation the relationship between

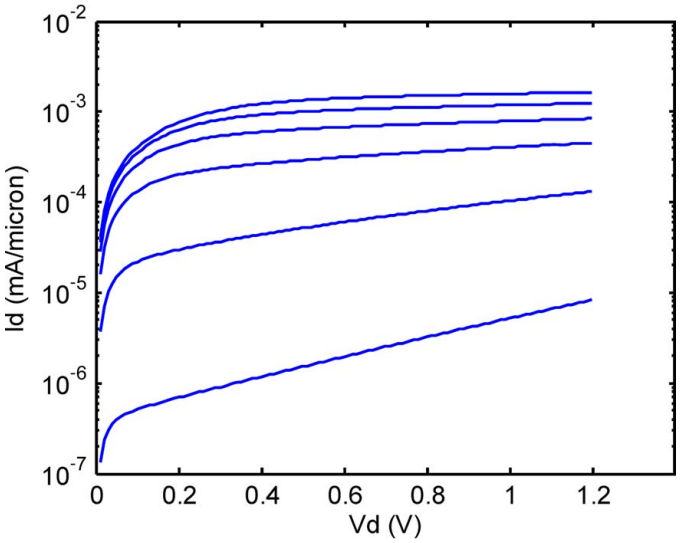

Fig. 2. V_{ds} vs. I_{ds} [6]

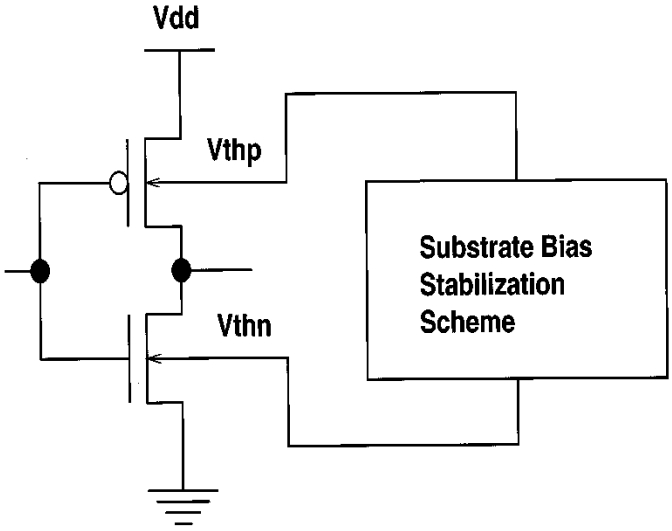

Fig. 3. The stabilisation scheme used in VT-Sub-CMOS [5]

V_{gs}, the voltage across the gate and source, and I_{ds}, the current between drain and source, becomes exponential [4]. As transconductance gain is defined as $gm = \frac{I_{ds}}{V_{gs}}$, the exponential relationship results in the transconductance gain becoming very large. Additionally the static noise margin of the device is improved to almost ideal levels.

Furthermore, there are some additional costs in order to achieve the desired power savings. The devices sensitivity to the temperature, process variations, and power supply noise increases. As shown in figure 2 as V_{gs} increases so does the current I_{ds}, however the device then enters saturation region at which point I_{ds} levels out. In this mode of operation, when there is variation on the power supply V_{gs} also varies, however there is minimal change in I_{ds}. With subthreshold logic, the device is operating in the triode region where a change in V_{gs} results in a large change in I_{ds}, as such the transconductance gain with respect to the power supply has increased.

B. Variations

1) Variable Voltage: In [5] Soeleman et al. attempt to improve subthreshold designs so that they are less susceptible to a number of the side effects experienced in standard subthreshold operation. Variable Voltage Subthreshold CMOS (VT-Sub-CMOS) logic is an attempt to reduce the effect of temperature and process variations.

VT-Sub-CMOS works by having a stabilisation circuit involved which adjusts the bias applied to the substrate of the transistors, as shown in figure 3. This stabilisation circuit consists of two key parts, the leakage current monitor, and the self-substrate bias. The leakage current monitor acts like a current sensor, and monitors the amount of leakage current flowing through the transistor. An output voltage is produced which is then passed into the self-substrate bias. The self-substrate bias then determines an appropriate bias voltage to apply to the substrates. As this bias voltage then corrects the leakage current a closed loop is formed and the circuit is held stable.

The stabilisation circuitry relies on the basis that the temperature and process variations will be fairly constant across the device, or at least across a small area. To form the leakage current monitor a transistor is placed in series with a resistance, and the two are then connected between the two power rails, with the gate of the transistor connected to the appropriate power rail to bring it into saturation. An output voltage is then taken from the centre point of the potential divider that is formed, which is then fed into the self-substrate bias block. The NMOS and PMOS transistors require separate leakage current mirrors, and hence separate stabilisation circuitry, as production of the two transistor types vary and hence they may experience different process variations. The self-substrate bias then contains a ring oscillator with an enable controlled by the leakage current monitor's output. The output of this ring oscillator operates a charge pump which builds a charge on the substrates. As such this stabilisation circuitry acts to rebuild the charge whenever it falls below a defined value.

SPICE simulations show that this VT-Sub-CMOS logic stays stable as the temperature changes [5], effectively bringing the threshold voltage down to just below the supply voltage. This removes the exponential relationship between V_{gs} and I_{ds}, reducing the sensitivity to temperature variations. The delay required between switching is also greatly reduced, meaning that the system can operate at a higher frequency. While this approach introduces stability into the subthreshold logic, it increases the circuit complexity, and hence also increases the area.

2) Dynamic Voltage: Dynamic threshold voltage CMOS, or Sub-DTMOS, is an attempt to achieve the same stability as provided by VT-Sub-CMOS but without the expense of complex circuitry. In order to achieve this the substrate of each transistor is directly connected to its gate. This causes the threshold voltage to change to suit the state of the transistor. At zero bias the threshold voltage is high, and when V_{gs} is equal to the high voltage level the threshold voltage is low. This is caused by the body effect of the transistor [7]. In standard CMOS the threshold voltage is high, as it tracks the

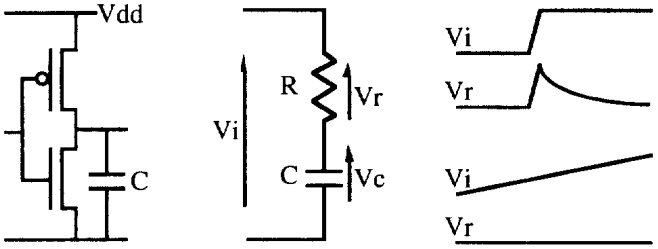

Fig. 4. Conventional CMOS vs. Adiabatic CMOS in terms of power consumption, shown through the use of the equivalent circuit [8]

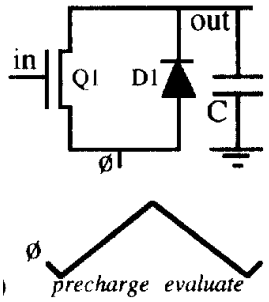

Fig. 5. Circuit diagram of Adiabatic Dynamic Logic [8]

body-source bias. In a Sub-DTMOS configuration the body-source junction is forward biased, this draws the threshold voltage down. When the threshold voltage is at its minimum the charge on the body is at its minimum, the lower charge results in a higher electron mobility. This higher mobility comes about because the lower charge reduces the normal field in the substrate, allowing the carriers to move less impeded. The effect of this is to give the device a higher on current, resulting in greater gain but at the cost of a greater power consumption.

Increased power consumption is not the only cost of the Sub-DTMOS design, it also results in a higher gate capacitance than would be experienced in normal CMOS logic. However, this effect is countered as the higher on current causes the capacitance to gain and lose charge quicker. This increase in on current far outweighs the increase in capacitance, and as such the Sub-DTMOS logic is able to operate faster than even standard CMOS [5].

The Sub-DTMOS logic was simulated under SPICE and showed a higher resilience to temperature with respect to the delay, requiring less delay than VT-Sub-CMOS. This, in addition to the area saved due to the lower complexity of the design. However this comes at the expense of a higher power draw.

III. Adiabatic Logic

A. Design

As discussed in section I, energy is lost as the transistors in a circuit change state. Adiabatic logic attempts to counter this by slowly charging up the components, preventing there ever being a continuous channel from the supply rail to ground. As such the heat dissipation lost during switching is drastically minimised. Clearly this has the effect of heavily restricting the maximum speed at which the circuit can operate.

The effect of this can be seen in figure 4. When the conventional CMOS logic input voltage rises suddenly there is an observable peak in the voltage across the resistance. This high voltage causes a large current flow and hence a large heat dissipation in the resistance. The current through the resistance causes the capacitor to charge, reducing the voltage across the resistor and preventing further power loss. In the adiabatic setup, the slower change in the input results in the capacitor being able to keep up with the increase in potential with a minimal current through the resistor, hence significantly less power is dissipated.

In order to achieve the energy saving, adiabatic logic uses a number of stages to set itself up. Firstly the circuit passes through a *precharge* stage. In this stage the nodes in the circuit are preloaded with a charge. Secondly comes the *evaluation* stage, during which the logical expression is evaluated, and the various nodes either remain charged or discharge as required. Then the output can be read from the gate. This requirement dictates that adiabatic circuits have a complex clocking circuitry, able to provide two different phases. Creating this complex clock results in a further loss of power, as such the design of this clock must have careful attention paid to it to ensure that it does not restrict the power savings. Given all of this, adiabatic circuits are able to produce power savings of the order of 10-20 while maintaining speeds in the hundreds of megahertz [9, 10, 8, 11, 12]

A by product of the slower switching involved with adiabatic circuits is that switching noise is reduced. This is a much more critical effect in mixed signal circuits, as opposed to digital only systems, as the analogue circuitry is much more sensitive to noise. Another advantage of adiabatic logic is its simplicity in production, as in general it requires nothing more than standard CMOS logic gates, with the exception of the clocking circuitry.

In the switching process, a small lump of charge is moved from the power rail to the ground rail during each switching process. While power is saved from the spike prevention in each switch, this small packet of charge being essentially thrown away is rather wasteful. As such the use of charge recovery circuitry is advised with adiabatic circuits. Some adiabatic circuits, such as those discussed in sections III-B2 and III-B3 include the recovery mechanism as part of the logic.

B. Variations

1) Adiabatic Dynamic Logic: Adiabatic Dynamic Logic as defined by Dickinson and Denker in [8] adds two additional stages to the cycle, an *input* stage and a *latch* stage. Adiabaticity requires that there is never a large potential across the transistor channel while it is conducting, otherwise the same high switching current would be experienced as in conventional CMOS. The input and latch stages help to achieve this by providing a time during which the input can change without causing non-adiabatic effects, and by ensuring the output is stable for a measurable amount of time in the latch phase.

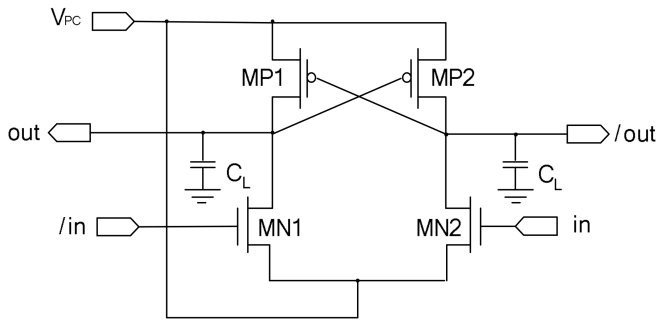

Fig. 6. Circuit diagram of a PAL inverter [13]

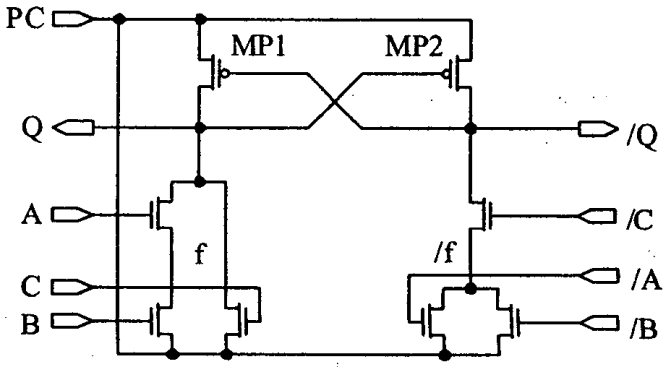

Fig. 7. A PAL AND-OR gate ($Q = A.B + C$) showing how to increase the complexity of the circuit [9]

2) PAL: Pass-transistor Adiabatic Logic uses a sinusoidal power clock, connected to the nodes through an evaluating NMOS circuit, and also through a single PMOS transistor. An example of a PAL inverter is shown in figure 6. This inverter circuitry is fairly simple, however more complex functions can be achieved by adding to the NMOS circuitry connecting to the OUT node, and creating a complimentary NMOS function on the /OUT node, as shown in figure 7.

Focussing on the inverter, as the power clock rises from low to high one of the NMOS transistors conducts, allowing the charge to rise on the output node. The complementary output node will remain low as its respective NMOS does not conduct. As the charge rises it causes the PMOS transistor to also conduct, allowing the output to reach the peak voltage of the power clock. When this peak is reached, the output is valid. As the voltage on the power clock begins to fall away the charge on the output node is discharged to the power clock, resulting in the energy being recovered.

A key advantage of PAL over many other adiabatic systems is that it only requires a single clock source [14, 9]. Given this fact it generates savings in the order of 10-20 [9] while losing very little power in clock generation.

3) LPAL: Latched Pass-transistor Adiabatic Logic is a variation on PAL which adds transistors to disconnect the gate from the power clock. These transistors can be seen in figure 8, labelled as *MN3* and *MP3*.

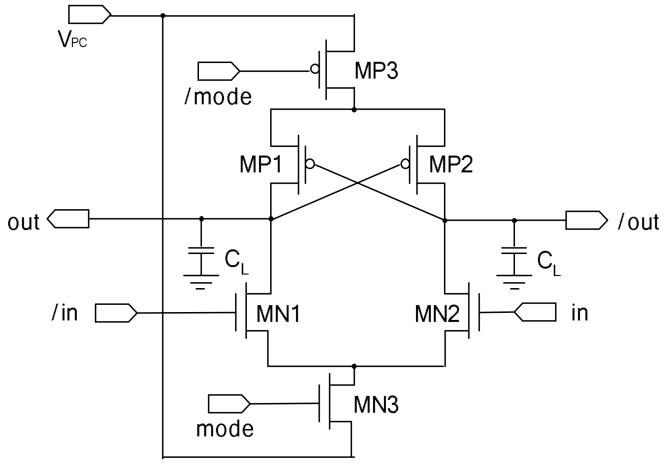

Fig. 8. Circuit diagram of a LPAL inverter [13]

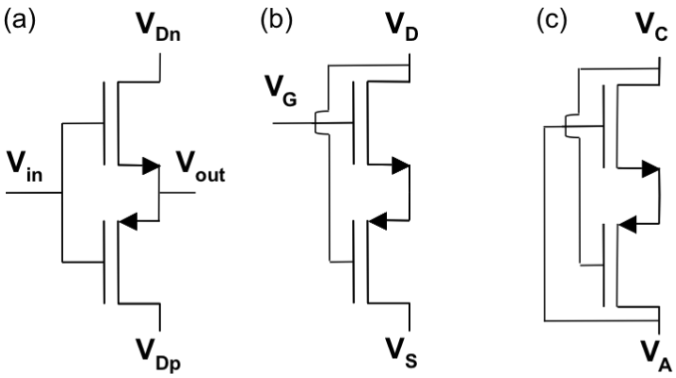

Fig. 9. A selection of devices exploiting ultra-low leakage. (a) Voltage Follower, (b) Transistor, (c) Diode [15]

IV. ULTRA-LOW-LEAKAGE (ULL)

A. Design

Of the two main forms of loss in CMOS logic, switching and leakage currents, ULL works to reduce the leakage currents down to the physical limits of the device.

It is often forgotten in CMOS design that there is not only digital circuitry, but also analogue components as well, as these are required to interface with the physical world. Flandre et al. help address this by producing a number of analogue components, as well as digital ones. Among their designs are voltage followers, transistors, and diodes, as seen in figure 9.

Initially a pair of N and P channel MOSFETs are selected with appropriate V_{Th} values such that their $I_D - V_{GS}$ curves intersect at a low current. These transistors are then connected up in such a way that the P-channel and N-channel transistors are connected by their sources. This is contradictory to the standard arrangement of transistors, where the transistors would connect via their drains. The effect of connecting the transistors up this way is that the circuit biases itself automatically, such that the sum of the V_{gs}'s of the two transistors is equal to the voltage across the devices, and that the current through the two devices is equal. This also produces the effect that as the device characteristics vary with temperature, the two transistors act to counter each other

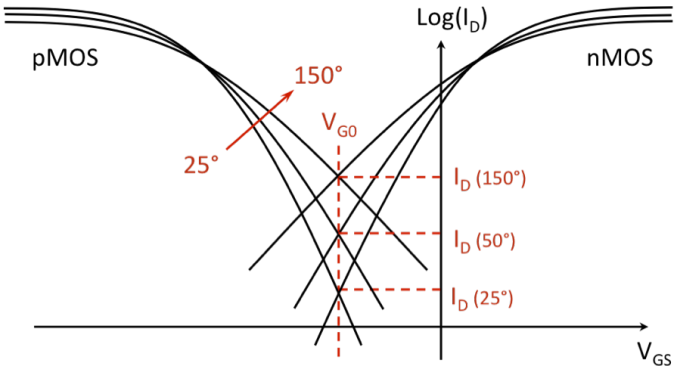

Fig. 10. A graph showing the autobiasing of V_{gs} as temperature changes [15]

keeping the gate bias constant. This is shown in figure 10.

As a reverse voltage is placed across the terminals of a ULL structure, the self biasing effect brings in another aspect by which it decreases the NMOS V_{gs} while increasing the PMOS V_{gs}. This causes the reverse current for the transistor to be reduced below its off current right down towards its leakage current. A similar effect is seen when the power rail voltage is increased, initially the off current through the devices increases, however the gates then bias themselves causing the off current to drastically reduce. This can result in reductions of the off current of a factor from 100 to 10000+ when compared to standard CMOS [3, 15]. The value of this factor depends on the physical leakage limit of the device.

The simplistic design of these circuits means that only standard CMOS processes are required in production, however it results in each transistor in a standard logic circuit effectively becoming two. This obviously has a significant effect on the area required for the design. Additionally, the nature of the low leakage current at high reverse voltage makes the designs highly efficient, especially so in the diode configuration. Flandre et al. suggest a efficiency increase from 10.47% to 79.92% against standard CMOS, at a speed of over 13MHz [15]. This also shows a further advantage involved in ULL designs, the simplistic design leads rise to the systems being largely unaffected with regards to speed of processing.

V. Conclusion

In this report a number of different low power technologies have been discussed, with particular emphasis on those that provided ultra low power usage at the expense of processing speed and ability. It has been discussed that there are two main forms of loss in CMOS logic transistors, namely switching and leakage currents. All the technologies discussed worked to reduce one of these two losses as significantly as possible.

Subthreshold logic works to reduce the leakage current by operating at a low supply voltage, and hence using the leakage current as the switching current in the device. This results in a very low power usage, however at the expensive of requiring a long delay in order to build up the appropriate charge for the next stage to be operated. Given the circumstances that this report was focussing on, technologies that provide the power savings given that low processing ability is required, this is not necessarily a hugely significant issue, however would ultimately depend on application. A couple of variations were considered, one which improves the robustness of the technology to temperature and process variations at the expense of circuit complexity, another which provides small improvements in robustness and design simplicity at the expense of power consumption. In contrast ultra-low leakage technologies work to reduce the same current, however do not require such a long delay. This works by creating an automatically self-biasing circuit which biasses itself to force the drain-source current to reduce down to the physical limits. However the price paid was for an increase in area. This price is similar to that involved with VT-Sub-CMOS designs, whereby a complex circuit is required in order to ensure the logic stayed stable.

Adiabatic logic works to reduce the current lost when the transistors switch and create a short between the power rails. This has the advantage of large savings in the power lost, with factors of 10-20, while having a slowing effect on the system. Further to this it requires a complex clocking circuitry in order to achieve the savings.

A comparison of the three technologies can be seen in table I.

For all the technologies, there are still losses involved, some of which can be remedied through the use of additional circuitry. One possible form of circuit to achieve these additional savings is a charge recovery circuit, which returns charge back to the power rails.

As can be seen a variety of technologies are available for power reduction, with their various advantages and disadvantages. Which one will be ideal will depend heavily of the application to which it is to be put, with some deciding factors being the area available, the rate of throughput required, and the processing speed. This decision must be left to the designer, however a number of options are presented here.

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	Sub-Threshold	Adiabatic	ULL
Variable reduced	Leakage current	Switching current	Leakage current
Form of change	Reduced operating voltage	Slowed switching	Create self-biasing reverse diodes
Saving factor	$1000\times$	$10-20\times$	$100-10000\times$
Operating frequency	$175KHz$	$<1GHz$	$13.56MHz$
Area increase (direct)	0	0	$2\times$
Additional circuitry	None	Clocking circuitry Energy recovery	None

TABLE I
A COMPARISON OF THE VARIOUS TECHNOLOGIES

employing only physical parameters," *IEEE Transactions on Electron Devices*, vol. 56, no. 8, August 2009.

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