Kaixin Yang

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Education

Viterbi School of Electrical and Computer Engineering, University of Southern California
Los Angeles, CA 90007, U.S. **Sept. 2019 – Present**

Ph.D. student in Computer Engineering

Viterbi School of Electrical and Computer Engineering, University of Southern California
Los Angeles, CA 90007, U.S. **Sept. 2019 – May. 2021**

M.S. in Electrical Engineering

School of Electronics Engineering and Computer Science, Peking University
Beijing, China **Sept. 2015 – Jul. 2019**

B.S. in Electronic and Information Science and Technology

Research Experience

Research on Hardware Security and Sequential Logic Encryption **Aug. 2019 – Present**

Advisor: Prof. Pierluigi Nuzzo *Affiliation: Cyber-Physical System Design Group*

- Systematically summarized the assumptions and metrics of current sequential logic attack methods.
- Evaluated several sequential logic encryption methods, proposed potential strategies to attack on sequential logic encryption methods, developed an unrolling-based SAT attack and compared with existing methods in literature.
- Developed a graph neural network-based approach to retrieve correct key values from encrypted netlists.
- Explored unrolling-based approach to attack latch-based logic locking technique.

Teaching Experience

Teaching Assistant for EE477L: MOS VLSI Circuit Design **Aug. 2021 – Dec. 2021**

Instructor: Prof. Massoud Pedram

Publication

Book Chapter

- Hu, Y., Yang, K., Nazarian, S., Nuzzo, P., 2021. SANSCrypt: Sporadic-Authentication-Based Sequential Logic Encryption, VLSI-SoC: Design Trends, Springer. *(published)*

Conference Papers

- Chowdhury, S., Yang, K., Nuzzo, P., 2021. ReIGNN: State Register Identification Using Graph Neural Networks for Circuit Reverse Engineering. ICCAD 2021. *(published)*
- Hu, Y., Zhang, Y., Yang, K., Chen, D., Beerel, P., Nuzzo, P., 2021. Fun-SAT: Functional Corruptibility-Guided SAT-Based Attack on Sequential Logic Encryption. IEEE International Symposium on Hardware Oriented Security and Trust (HOST). *(published)*
- Hu, Y., Yang, K., Chowdhury, S. and Nuzzo, P., 2020. Risk-Aware Cost-Effective Design Methodology for Integrated Circuit Locking. DATE 2021. *(published)*
- Hu, Y., Yang, K., Nazarian, S. and Nuzzo, P., 2020. SANSCrypt: A Sporadic-Authentication-Based Sequential Logic Encryption Scheme. VLSI-SoC 2020. *(published)*

Honor and Award

2019 Annenberg Fellowship
2018 Excellent Presentation in The Sixth Peking University Young Scientists Symposium on Informatics
2018 Third Prize in 2018 Intel Cup Undergraduate Electronic Design Contest
2017 Award for Academic Excellence of Peking University in academic year
2017 Level 3 in National Computer Rank Examination
2016 First Prize in College Physics Contest awarded by Beijing Physics Society in year 2016

Skill

Programming Languages: Verilog, Python, C++, C
Softwares & platforms: Synopsys, Cadence, MATLAB, LaTeX, Linux
Languages: Chinese(Native), English(Proficient)
Standard English Test: TOEFL 102 (R27, L27, S20, W28); GRE 323 (V153, Q170, W3.5)