Experiment No: 10

Name: parity bit Generator Circuit - Even parity.

Aim: to design, construct and test circuit that generally parity bit from 4 message bit.

Objectives: To study the construction and design of the combitional circuit

components: Bread board / kit, 7486

Theory:

A parity bit is an extra bit included with a binary message to make the number either odd or even. The message including the checked at the reciving end for errors. An error is detcted if the checked parity does not correspond with the transmitted. the circuit that generates the parity bit in the transmitted is called parity generator

Procedure:

1 connection use made as per the circuit diagram

2. Switch on the power supply

3. Apply different combinational at input and observe the output. Compare the output with the truth table

Result

Different logic circuit are constructed and their truth tables are verified

Circuit diagram & truth table

A	B	C	D	P
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

AB \ CD	00	01	11	10
00	m_0	m_1	m_3	m_2
01	m_4	m_5	m_7	m_6
11	m_{12}	m_{13}	m_{15}	m_{14}
10	m_8	m_9	m_{11}	m_{10}

C (11, 10) · B (01, 11) · A (11, 10) · D (01, 11, 10, 00)

$$F = A \oplus B \oplus C \oplus D$$