Experiment No: 7

Name: SOP & POS

Aim: plot the following Bolean function in a map as well as implinent in the logic diagram

$f = A'D + BD + B'C + AB'D$

Objectives: To study the simplification of Boolean function SOP & POS forms.
(Demonstrate the relationship between a boolean function and the corresponding logic diagram using map reduction method)

Components: Bread Board / kit, 7408, 7404, 7032

Theory:

a) Convert the given function in standerd SOP form. Enter in to K-map and seduce it.

b) Convert the given function in standerd POS form. Enter in to K-map and reduce it

c) verify that (a & b) is equal.
convert the given function into Standerd SOP form.

$f = A'D + BD + B'C + AB'D$

Since it is in the SOP convert into Standerd SOP.

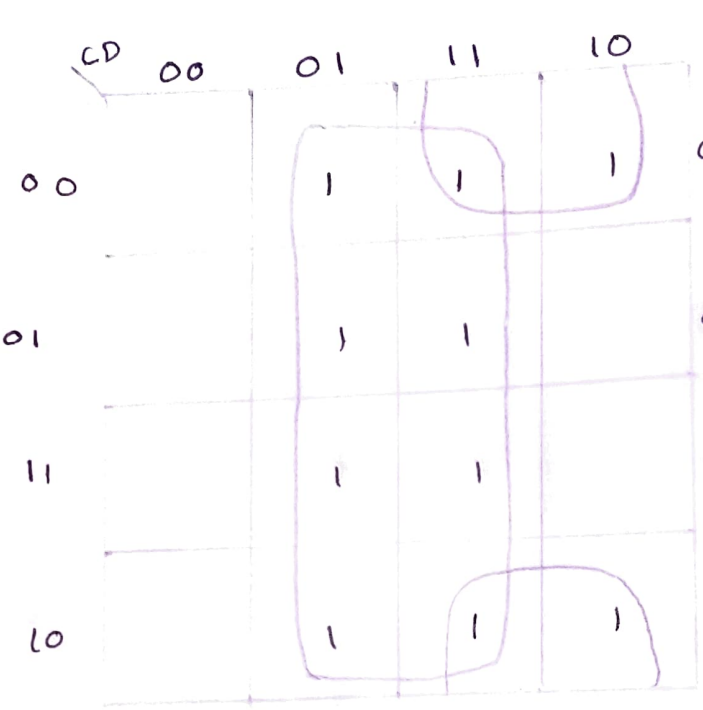
* Add the variable B for the missing terms.

$A'D = A'D(B + B') = A'DB + A'DB'$

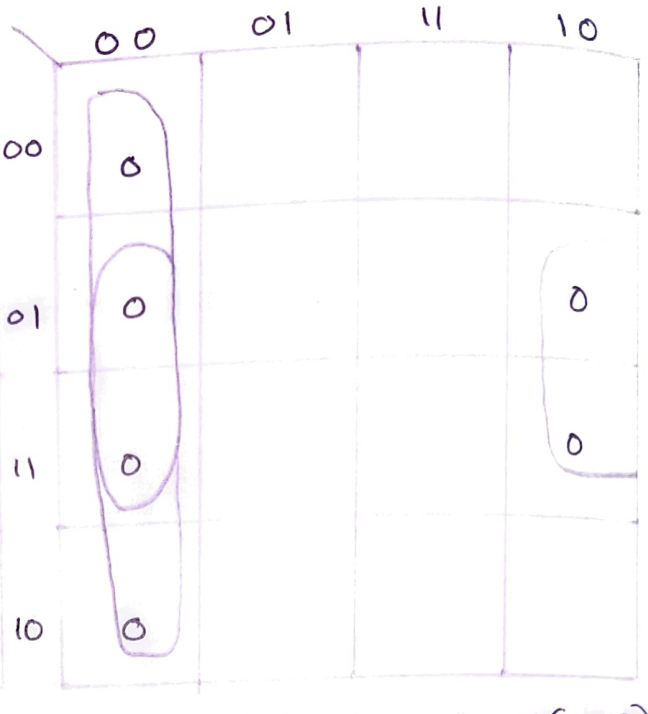
* Add the variable A for missing terms.

$BD = BD(A' + A) = A'BD + ABD$

$B'C = B'C(A' + A) = AB'C + A'B'C$



SOP F = min = D + B'C



POS F max = (C + D)(B + D)

Truth table of SOP F Min = D + B'C

C	B	D	B'C	D + B'C
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	1
1	1	0	0	0
1	1	1	0	1

* Add the variable C for the missing terms.

$A'DB = A'DB(C'+C) = A'BC' + A'DBC$

$A'DB' = ADB'(C'+C) = ABB'C' + ADB'C$ (AD)

$A'BD = A'BD(C'+C) = A'BDC' + A'BCD$

$ABD' = ABD(C'+C) = ABDC' + ABDC$

$AB'D = AB'D(C'+C) = AB'DC' + AB'DC$

* Add the variable D for the missing terms

$A'B'C = A'B'C(D'+D) = A'B'CD' + A'B'CD$

$AB'C = AB'C(D'+D) = AB'CD' + AB'CD$

* combine the above four variable terms all together.

$F = A'BC'D + A'BCD + A'B'C'D + A'B'CD + A'BC'D + A'BCD + AB'CD + ABCD + AB'C'D + AB'C'D + AB'CD + A'B'CD' + A'B'CD + AB'CD' + AB'CD$

ie $F = m(1, 2, 3, 5, 7, 9, 10, 11, 13, 15)$

ie $F = m(0, 4, 6, 8, 12, 14)$

Procedure

1. Connect all made as per the circuit diagram
2. Switch on power supply.
3. Apply different combinations of inputs and observe the output. Compare the output with the truth table

Result

Different logic circuits all constructed and their truth tables are verified.

POS Fmax = (C+D)(B'+D)

C	B	D	C+D	B+D	(C+D)(B'+D)
0	0	0	0	1	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	1	1	1	1
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	1	0	0
1	1	1	1	1	1

The above truth table shows both are equal but in SOP minimized equation needs 3 gates pos minimized equation needs 4 gates.
So here SOP minimized equation is more economical.