EXP NO – 4 DCP·LAB·ASSIGNMENT – 4

Realisation of Gates using NOR

Name: Demonstration of universal gates.

Aim: Implement logic gates using universal gate NOR

Objective: To study the design and implementation of logic gates (OR, AND, NOT, NOR, NAND, XOR) using universal gates (NAND, NOR) & verify their truth table.

components: Bread board / kit, 7400, 7402.

Theory:

a) An OR gate is a logic circuit with 2 or more inputs and one output. The output of an OR is low when all of it's inputs are low for all other possible input combinations the output is high.

b) The output of an AND gate is high only when all of it's inputs are in the high state. In all other situations the output is low.

c) A NOT gate is a one-input / one-output logic circuit whose output is always the compliment of the input; that is a low input produces high output and vice versa

d) The output of a NOR gate is a logic '1' when all its inputs are logic '0' for all other input combinations the output is logic '0'

e) The output of a NAND gate is a logic '0' when all its inputs are logic '1' for all other inputs combinations the output is a logic '1'

Procedure

a) test all the IC's manually / using IC tester

b) connect VCC and GND

c) connect the appropriate pins of the input & output LED's and switches

d) verify the truth table with respect to the clock

Result

Different logic gates are constructed and their truth tables are verified.

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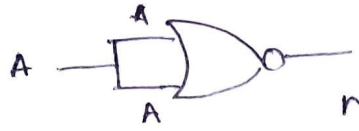
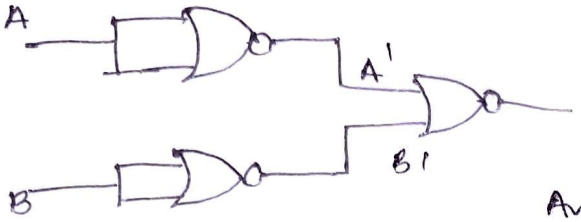
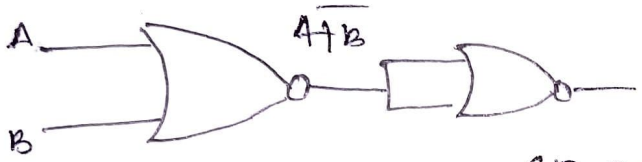
* 

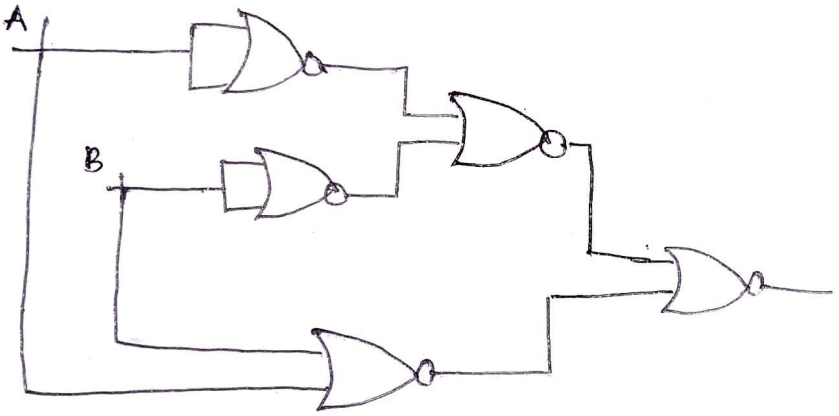
NOR gate

* 

AND gate

* 

OR gate

* 

XOR gate