Experiment NO: 11

Name: S-R Latch using NAND

Aim: Construct, test and investigate the operation of S-R latch using NAND

Objectives: To study the construction and the working of SR latch using NAND.

Components: Bread board/ kit, 7400

Theory:

SR-latch: The SR latch is a circuit with two cross-coupled NOR gates or two cross-coupled NAND gates, and two inputs labelled S for SET and R for RESET. The SR latch has 2 useful states: $Q = 1$ and $Q' = 0$ the latch is said to be in SET state.

when $Q = 0$ and $Q' = 1$ the latch is said to be in RESET state.

Outputs Q and Q' are normally to complemented of each other. However, when both inputs are equal to 1 at the same time, a condition in which both outputs are equal to '0' occurs

If both inputs are then switched to 0 simultaniously the device will enter an unpredictable or undefined state or a mestastable state.

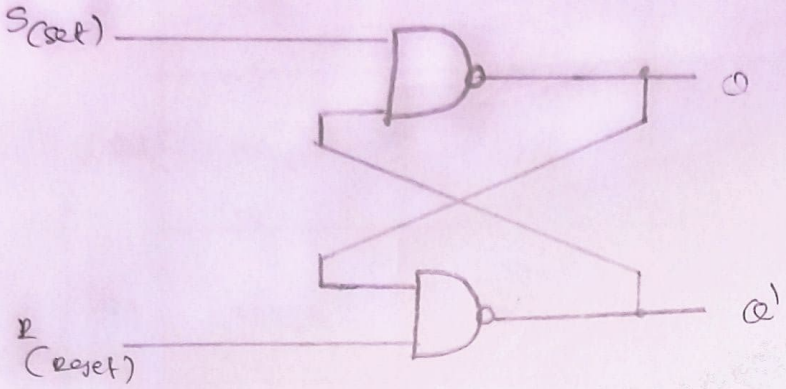
Procedure

1 Connections are made as per the circuit diagram
2 Switch on the power supply
3 Apply different combinations of inputs and observe the output, compare the output with the truth tables

Result

Different logic circuits are constructed & truth tables verifi

Circuit diagram



Truth table

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after S=1, R=0)
0	1	1	0	
1	1	1	0	(after S=0, R=1)
0	0	1	1	(forbidden)