



SIRIUS®
Technical Reference Manual
Version: 1.5.3



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5.13 STG / STG+

5.13.1 STGv3: Specifications

Inputs	Voltage, full bridge strain, ½ bridge strain, ¼ bridge strain, potentiometer, RTD, Resistance			
ADC Type	24bit delta-sigma dual core with 100/5 kHz analogue anti-aliasing filter (5.2.1 SIRIUS® Dual Core series: High Dynamic (up to 160 dB) page 65)			
Sampling Rate	Simultaneous 200kS/sec			
Dual Core Ranges (Low)	±50V (2.5 V)	±10V (500 mV)	±1V (50 mV)	±100mV (5 mV)
Gain Accuracy	±0.05% of reading			
Offset Accuracy (Dual Core)	±20(10)mV	±2(1)mV	±0.2(0.2)mV	±0.1(0.1)mV
Offset Accuracy after Balance Amplifier	±1mV	±0.1mV	±0.02mV	±0.01mV
Typ. Dynamic Range@10kS (Dual core)	137 dB (147 dB)	137 dB (152dB)	137 dB (147dB)	135dB (137 dB)
Typ. SNR@10kS (Dual Core)	108 dB (118 dB)	107 dB (125 dB)	107 dB (113 dB)	100 dB (100 dB)
Typ. CMR @ DC..50 Hz/400 Hz/1 kHz	56 / 56 / 56 dB	88 / 86 / 84 dB	97 / 96 / 95 dB	115 / 112 / 102 dB
Gain Drift	Typical 10 ppm/K, max. 30 ppm/K			
Offset Drift	Typical 0.3 µV/K + 2 ppm of range/K, max 0.8µV/K + 10 ppm of range/K			
Gain Linearity	<0.02%			
Inter Channel Phase-mismatch	0.02° * f _m [kHz] + 0.1° (@ 200 kS/sec and 10V range)			
Channel Cross talk	120 dB @ 10kHz (Range ≤ 10V); 95 dB @ 10kHz (Range = 50V)			
Input Coupling¹	DC, AC 1 Hz (3 Hz, 10 Hz per SW)			
Input Impedance	1 MΩ between IN+ and IN- for 50 V Range; all other Ranges > 1GΩ			
Max. common mode voltage	Isolated version: ±500 V Differential version: 50V Range: ±60 V; all other Ranges: ±12 V			
Input over-voltage protection	50 V Range: 300 V; all other Ranges: 50V (200 V peak for 10msec)			
Excitation Voltage	Free programmable (16 Bit DAC)			
Predefined levels	0, 1, 2.5, 5, 10, 15 and 20 V _{CD}			
Accuracy	±0.05 % ±2 mV			
Drift	±10 ppm/K ±100 µV/K			
Load stability: 0% to 100% load	< 0.01%			
Line regulation over 20 Ω of change	< 0.005% @ 120 Ω load			
Noise @ 10 Volt / 350 Ω	< 150 µVrms@10 kS			
Sense Impedance to Exc / to GND	100 kΩ / > 100 MΩ			
Current limit	100mA (max. 800mW)			
Protection	Continuous short to ground			
Excitation Current	Free programmable (16 Bit DAC)			
Predefined levels	0.1, 1, 2, 5, 10, 20 and 60 mA _{DC}			
Accuracy (> 10mA)	0.1% ±2µA [0.5% ±50 µA]			
Drift (> 10mA)	15 ppm/K [100 ppm/K]			
Compliance voltage	20 Volt, max. 500 mW			
Output Impedance	>1 MΩ			
Bridge connection types	full bridge, ½ bridge and ¼ bridge (3- or 4-wire)			
Ranges	2mV/V...1000mV/V free programmable with Dual Core			
Internal bridge completion	½ bridge and ¼ bridge 120Ω and 350Ω			
Bridge completion accuracy	0.05 %; TCR: 5 ppm/K (others on request)			
Internal Shunt resistor	59.88 kΩ and 175 kΩ, bipolar to Exc+ or Exc- (others on request)			
Shunt resistor accuracy	0.05 %; TCR: 10 ppm/K (others on request)			
Input short, Sensor offset adjust	Software selectable			
Counters (only on STGv3+ type)	1counter / 3 digital input, fully synchronised and alarm output			
Counter Modes	counting, waveform timing, encoder, tacho, gear-tooth sensor			
General Counter Specifications	See 5.6.1 General Counter Specifications on page 72			
Additional Specifications				
Misc. function	Excitation level monitoring, self check function			
Input Connector	DSUB-9, LEMO2B 7pin LEMO2B 10pin (others on request)			
TEDS support	Standard + DSI® adapters			

¹ In- must be within ±10V referred to GND(iso); for Ranges 100 V the DC value of In- is not rejected

Table 27: SIRIUS-STG specifications

5.13.2 STG+ (Counter) L1B7f



1: IN0/A
2: IN1/B
3: IN2/Z
4: DO
5: +5V
6: +12V
7: GND

Illustration 134: CNT: counter pin-out (LEMO 7pin)



Illustration 135: SIRIUS 8xSTG+

Connector type	L1B7f
Connector on the module:	EGG.1B.307.CLL
Mating cable connector:	FGG.1B.307.CLAD52

Table 28: STG+ counter connector type

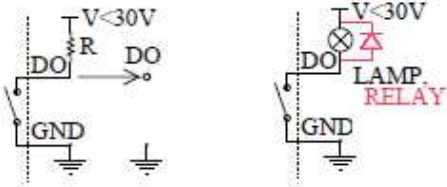
WARNING



GND of the counter input is connected to the GND of the analogue channel.

Digital Output Configuration

The “switch” of the open collector output is closed when active.



5.13.3 STG-L2B7f



Illustration 136: STG8 with 7-pin Lemo connectors