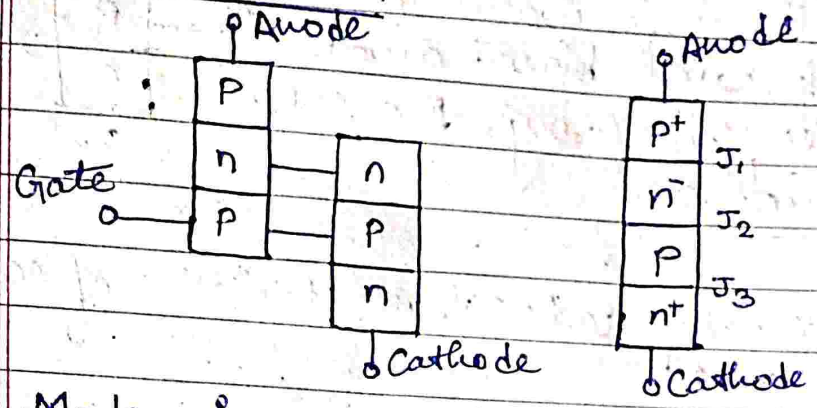
PDE

Assignment No. 1

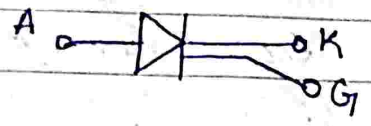
Q1. Draw construction diagram, symbol of SCR? Explain mode-wise operations of SCR.

Ans

Construction



Symbol

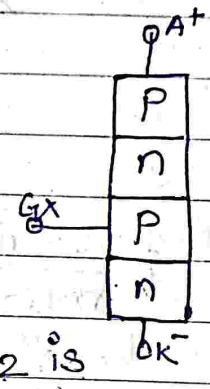


Mode-wise operations

There are 4 modes of operations

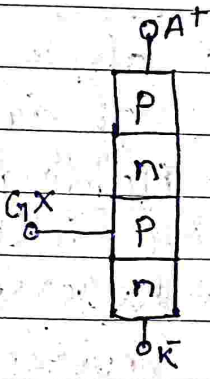
(1) Forward blocking modes

- Because no signal applied to it, thats why unbiased.
- Anode is +ve, Cathode is -ve & no gate signal.
- Junction J_1 & J_3 are forward biased but J_2 is reversed biased.



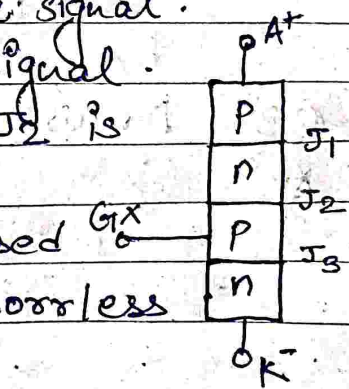
(2) Reversed biased mode

- Anode is -ve, Cathode is +ve & no gate signal.
- Junction J_1 & J_3 are reversed biased but J_2 is forward biased.
- Hence current through SCR is zero.



(3) Forward conduction mode without gate signal.

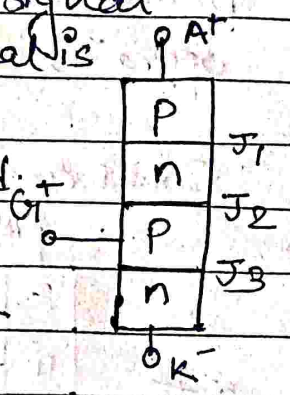
- Anode is +ve, Cathode is -ve & no gate signal.
- Junction J_1 & J_3 are forward biased but J_2 is Reversed biased.
- When forward voltage continously increased till forward break voltage, velocity of corrless



becomes very high so kinetic energy becomes very high junction J_2 breaks forcibly.

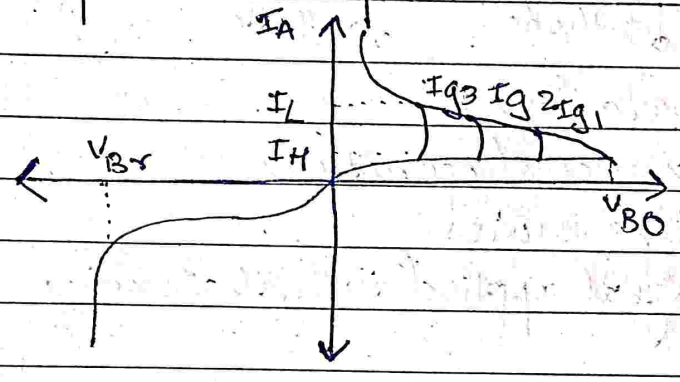
(4) Forward Conduction mode with gate signal

- Anode is +ve, cathode is -ve & Gate signal is +ve.
- Junction J_1, J_2 & J_3 is forward biased.
- Due to junction forward biased anode current start to flow through the SCR hence SCR becomes ON.



Q2. Draw & Explain steady state characteristics of SCR.

Ans



forward breakover voltage (V_{BO}): It is a max^m forward voltage i.e V_{AK} at which SCR conducts without any gate signal & finally get damaged.

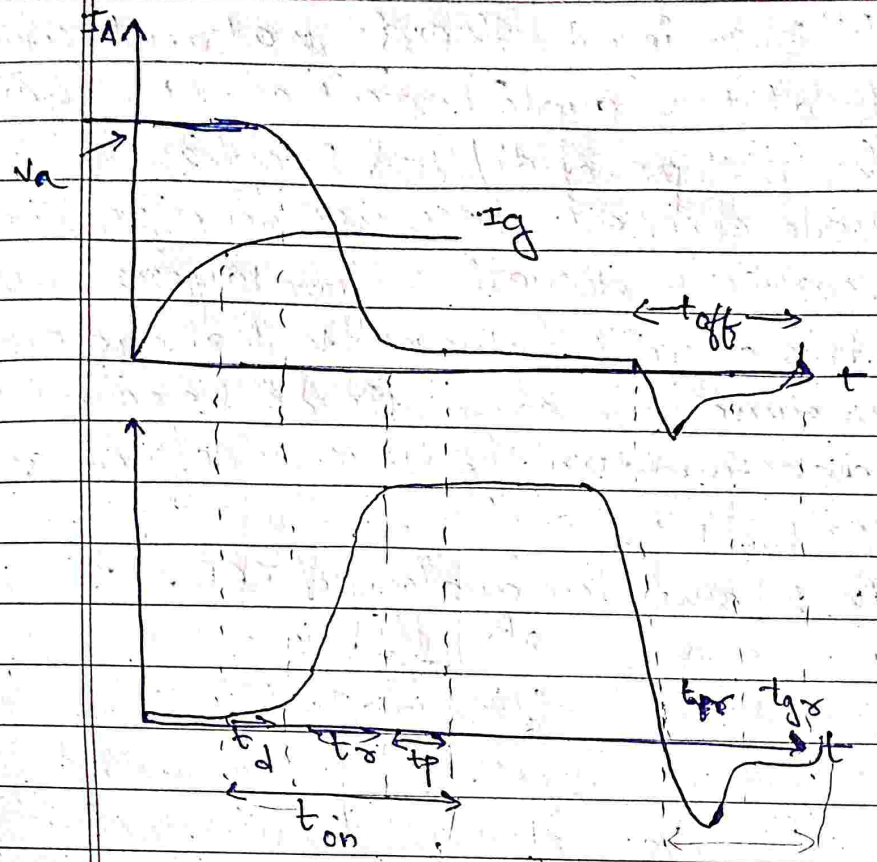
Latching Current (I_L): Minimum anode current above which SCR conducts continously in absence of gate signal.

Holding Current (I_H): Minimum anode current below which SCR becomes off in presence of gate signal.

Reverse breakdown voltage (V_{Br}): It is a max^m reverse voltage at which large $-I_A$ will flow through SCR without any gate signal & finally gets damaged.

Q3. Draw & explain switching characteristics of SCR?

Ans



Turn on: A SCR is turned on by applying a +ve gate pulse under forward biased condition. During turn on there ~~are~~ are 3 time interval.

i) Delay time (t_d): It is time required to change junction capacitances during which anode current rises from zero to 10% of I_a.

ii) Rise time (t_r): It is the time during which anode current rises from 10% to 90% of I_a. During this turn on losses in the thyristor are max.

iii) Spread time (t_p): It is time during which anode current rises from 90% of I_a to max anode current. During spread time conduction spreads over the entire cross section of the cathode of SCR.

It is defined as,

$$t_{on} = t_d + t_r + t_p$$

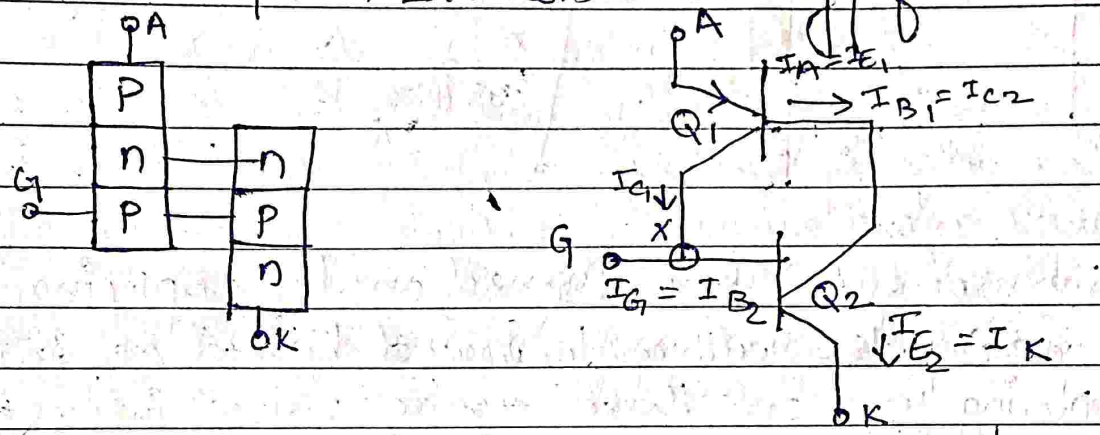
turn off: When SCR is turned on gate loses the control. The SCR can be turned off by reducing anode current below the holding

current which is achieved through natural commutation. During turn off at $t=t_1$ anode current crosses zero, becomes reverse with a slope of di/dt & Reaches to $-I_{rr}$ at $t=t_2$. The anode current becomes reverse due to presence of carriers stored in four layers. During time t_2-t_3, this current reduces to leakage current level, remains same for some time & becomes zero at $t=t_4$. Hence ~~time~~ turnoff time is defined as,

$$t_{off} = t_{rr} + t_{gr}$$

Q4. Draw & Explain 2 transistor analogy of SCR.

Ans



In the absence of gat signal, at V_{BO} the factor $(\alpha_1+\alpha_2)$ almost becomes unity & denominator of $I_A = \frac{I_{CBO}+I_{CBO2}}{1-(\alpha_1+\alpha_2)}$ becomes zero & hence becomes infinite resulting in damage of SCR.

When +ve gate signal is present, denominator $1-(\alpha_1+\alpha_2)$ becomes very small causing more anode current through SCR.

In two transistor ~~to~~ circuit of SCR, when a +ve gate signal is applied to gate as a base to Q_2 & Q_2 conducts. Conduction of Q_2 provides zero base signal to Q_1 which is p-n-p & Q_1 start conducting. It will acts as a base current of Q_2 & keeps Q_2 in one condition. In this way due to conduction of Q_2, Q_1 conducts & due to conduction of Q_1, Q_2 conducts. This is known as 'latching' of SCR. ~~or reg~~

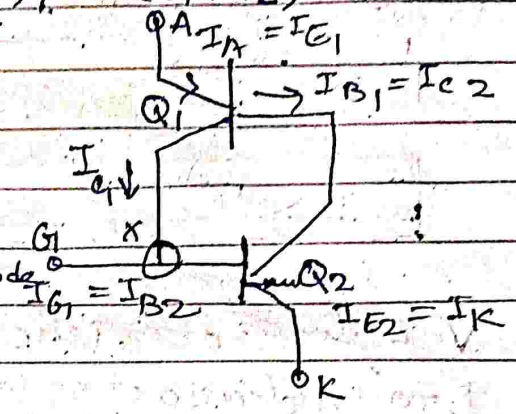
PAGE No.
DATE / /

Q5. For two transistor analogy of SCR show that:

$$I_A = (I_{CBO_1} + I_{CBO_2}) / 1-(\alpha_1+\alpha_2)$$

Ans Collector current of BJT is

$$I_C = \alpha I_E + I_{CBO}$$



Where,

α = current amplification factor.

I_{CBO} = leakage current in C-B mode

For BJT Q_1,

$$I_{C_1} = \alpha_1 I_{E_1} + I_{CBO_1} \quad \text{--- (1)}$$

For BJT Q_2,

$$I_{C_2} = \alpha_2 I_{E_2} + I_{CBO_2} \quad \text{--- (2)}$$

Total current to SCR

$$I_A = I_{C_1} + I_{C_2} \quad \text{--- (3)}$$

$$I_A = (\alpha_1 I_{E_1} + I_{CBO_1}) + (\alpha_2 I_{E_2} + I_{CBO_2}) \quad \text{--- (4)}$$

but from the given circuit;

$I_A = I_{E_1}$, $I_K = I_{E_2}$

$$I_A = \alpha_1 I_A + I_{CBO_1} + \alpha_2 I_K + I_{CBO_2} \quad \text{--- (5)}$$

Apply KCL at Junction X,

$$I_{C_1} = I_{E_1}$$

$$I_A = I_G = I_K \quad \text{--- (6)}$$

$$I_A = \alpha_1 I_A + I_{CBO_1} + \alpha_2 (I_A + I_G) + I_{CBO_2}$$

$$I_A(1-\alpha_1-\alpha_2) = I_{CBO_1} + \alpha_2 I_G + I_{CBO_2}$$

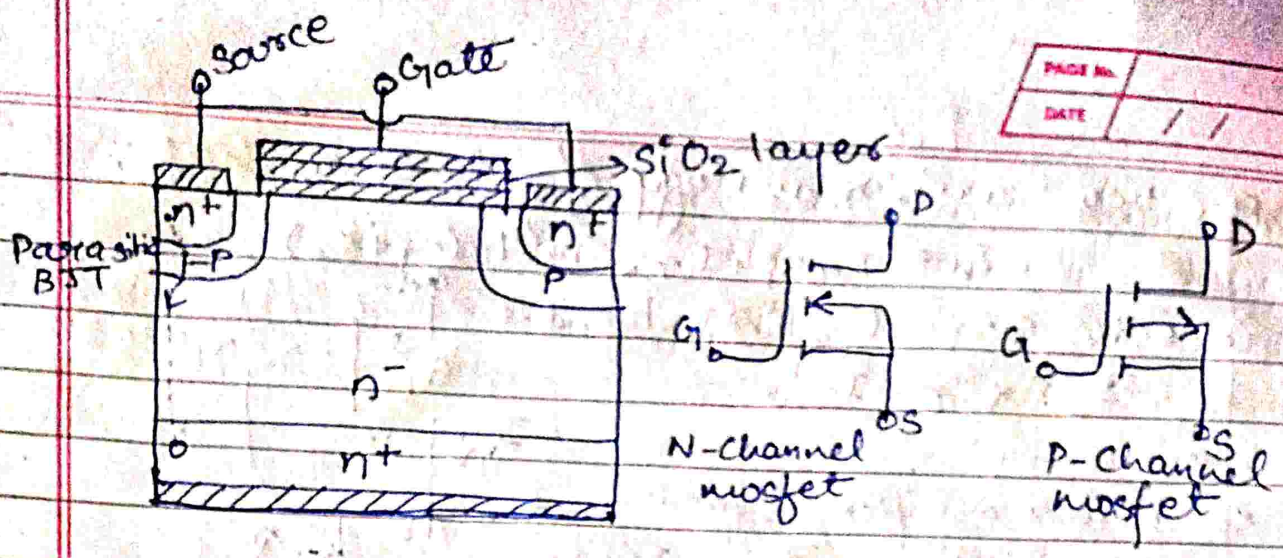
$$I_A = \frac{\alpha_2 I_G + I_{CBO_1} + I_{CBO_2}}{1-\alpha_1-\alpha_2} \quad \text{--- (7)}$$

When there is no gate signal

$$\boxed{I_A = \frac{I_{CBO_1} + I_{CBO_2}}{1-(\alpha_1+\alpha_2)}} \quad \text{--- (8)}$$

Q6. Draw construction diagram, symbol of MOSFET? Explain V-I characteristics of n-channel enhancement power MOSFET.

Ans

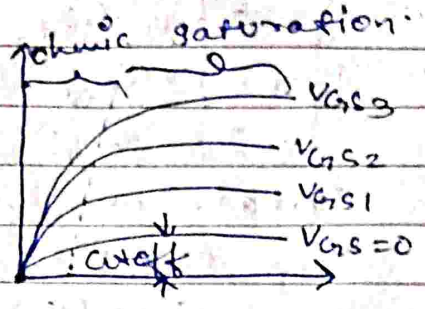


V-I Characteristics

(1) Drain Characteristics

i) Cutoff region.

- In this region $V_{GS} = 0$ so very neglide current will flow to the mosfet & it remains off.



ii) Ohmic region

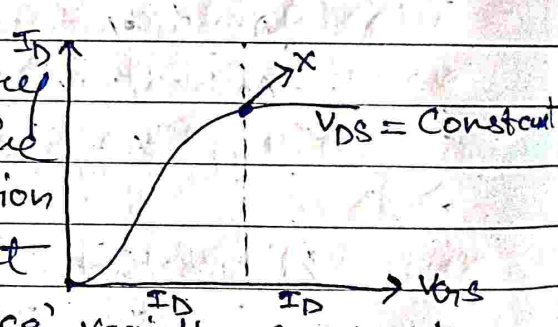
- In this region drain current start flowing to the mosfet. Hence mosfet becomes on & acts as closed switch.

iii) Saturation region.

- This is constant current region with respect to V_{GS}. & acts as an amplifier.

(2) Transfer characteristics

As i/p impendence of mosfet is very high, current gain (I_D/I_G) is in the order of 10^9. For mosfet operation current gain is not an important parameter but 'transconductance' is very important parameter which is ratio of drain current I_D to gate voltage V_{GS}, defines the transfer characteristics.



Q7.) Explain various turning ON methods of SCR.

Ans. There are 5 turning on methods of a SCR.

PAGE No.
DATE / /

i) Forward voltage triggerring / Anode triggering : When forward voltage i.e V_{AK} of a SCR is increased to V_{BO} with gate terminal open, junctions J_1 & J_3 become forward biased & J_2 becomes reverse bias. At V_{BO} J_2 breaks due to avalanche breakdown, a huge current will flow through SCR & finally it gets damaged.

ii) Thermal / temperature triggerring : During forward blocking mode, when temperature of junction J_2 increases, leakage current through J_2 increases & causes the turn on SCR.

iii) dv/dt triggerring : The charging current of junction capacitance is given as $I_c = C_j(dv/dt)$. If dv/dt rating of SCR is increased, charging current of capacitance junctions will become sufficient enough to turn on SCR. But a high value charging current may damage the SCR.

iv) Light triggerring : If a light is focused on gate junction (J_2), electron-hole pairs increase & SCR turn on. Light activated silicon controlled rectifier (LASCR) is the best example of the radiation triggerring.

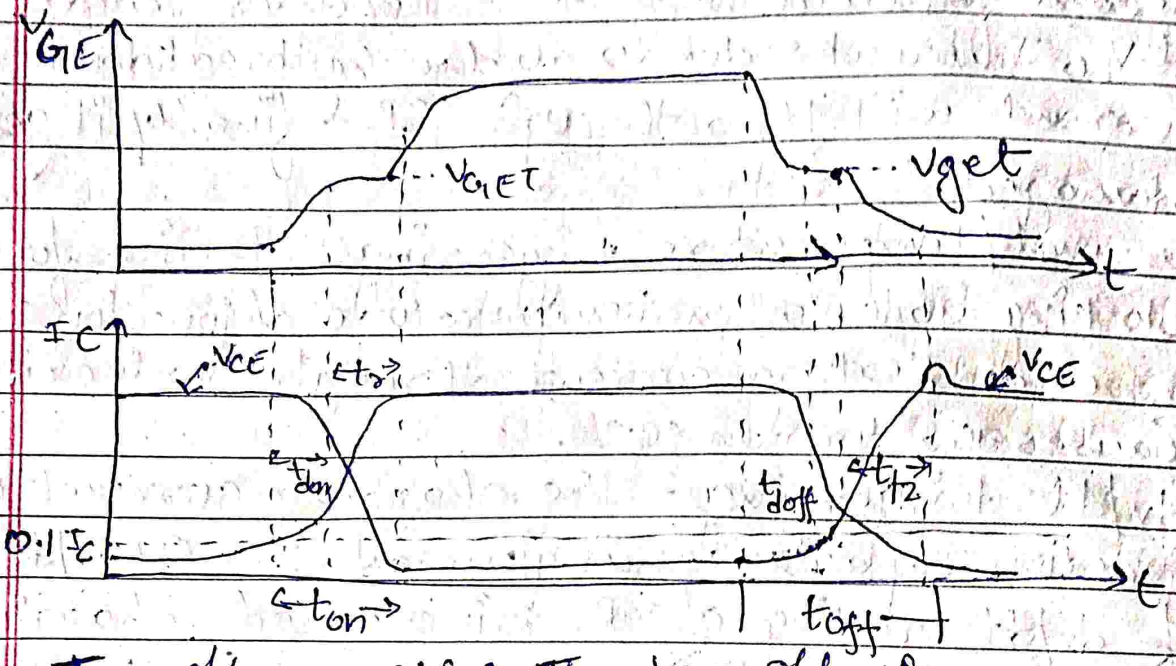
v) Gate triggerring : It is the most commonly used method of turning on of a SCR. When a +ve gate signal is applied to forward biased SCR, it turn on. If gate current increases, forward blocking voltage will be reduced as seen in SCR characteristics.

Q8. Draw & explain switching characteristics of ~~MOSFET~~ IGBT.
Ans

Turn on process : Turn on time t_{on} is composed of two components as usual, delay time (t_{dn}), & rise time (t_r). Delay is defined as the time

in which collector current rises from leakage current I_{CE} to $0.1 I_C$. Hence turn on time is:

$$t_{on} = t_{don} + t_r$$

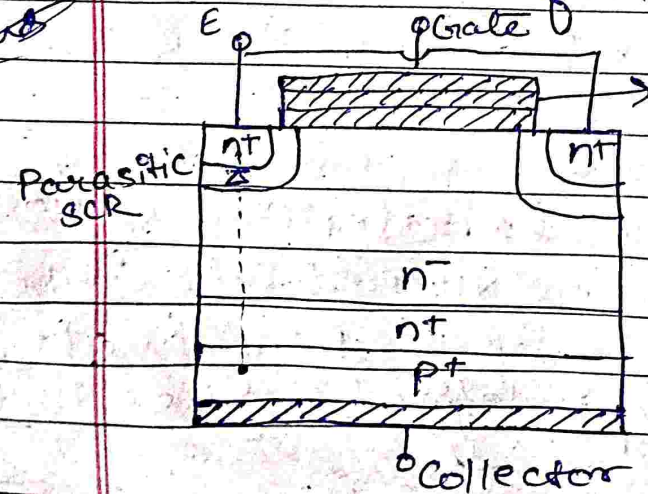


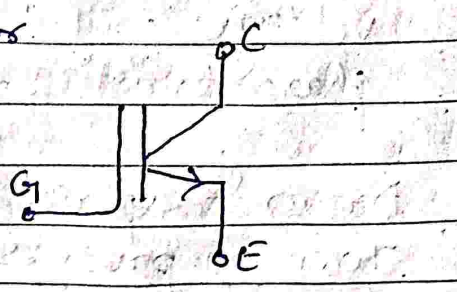
Turn off process: The turn off time t_{off} consists of three components, delay time (t_{df}), initial fall time (t_{f1}) & final fall time (t_{f2}). Delay time is defined as time when collector fall from max I_c to $0.9 I_c$.

Initial fall time is the time during which collector falls from $0.9 I_c$ to $0.2 I_c$. The final fall time time (t_{f2}) is the time during which collector current falls from $0.2 I_c$ to $0.1 I_c$. Hence turn off time is : $t_{off} = t_{doff} + t_{f1} + t_{f2}$

Q9. Draw construction diagram, symbol of IGBT? Explain V-I characteristics of IGBT.

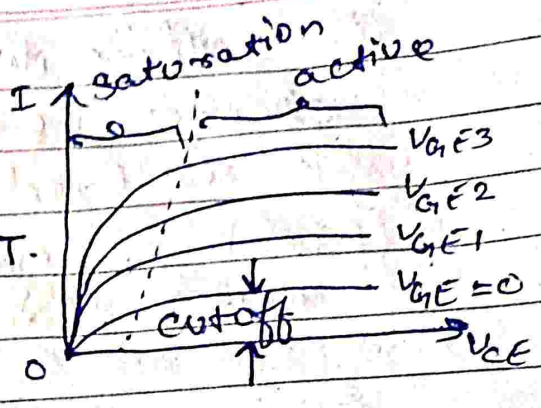
Ans





PAGE No.
DATE / /

V-I Characteristics of IGBT:

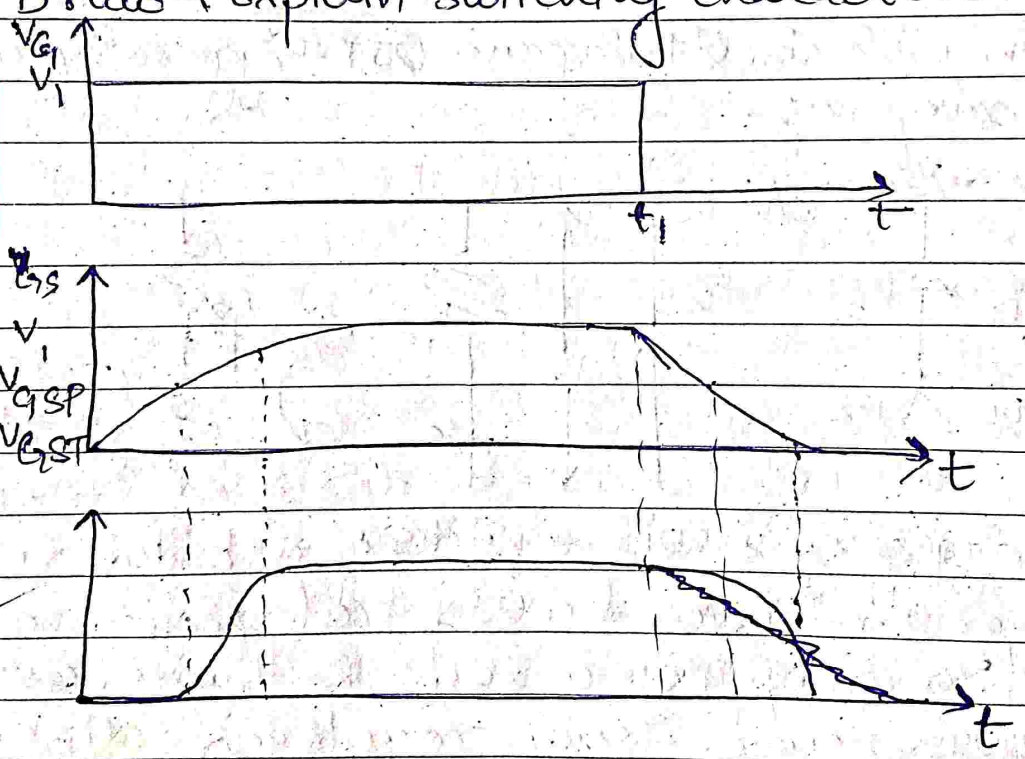


(1) Cutoff region
- Due to this collector current will not flow through the IGBT. Hence IGBT remains off & acts as open switch.

(2) Saturation region.
Due to this collector start flowing through IGBT. Hence IGBT becomes ON & acts as closed switch.

(3) Active region
Due to this collector current is flowing through IGBT which is independent on V_{CE} but dependent on V_{GE}. Hence IGBT conducts with some forward resistance. It acts as an amplifier.

Q8. Draw & Explain switching characteristics of ~~IGBT~~ MOSFET.
Ans



~~Turnoff~~ Turn on: When a +ve gate voltage is applied, source capacitance C_{GS} starts charging and gate voltage reaches to its threshold level called "gate threshold voltage (V_{GST}) so that drain current I_D begins to increase.

This time during which source capacitance C_{GS} changes, is called 'turn on delay time' t_{don}. When threshold gate voltage (V_{GST}) reaches to its peak gate voltage (V_{GSP}) is called rise time t_r. Hence turn on time is:

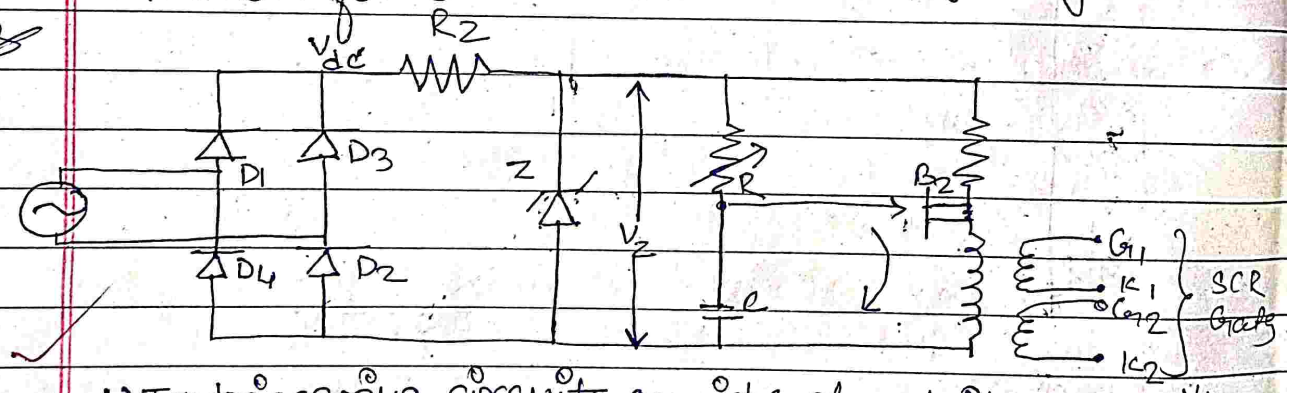
$$t_{on} = t_{don} + t_r.$$

Turn off: When gate voltage decreases from V_1 level to V_{GSP}, source capacitance C_{GS} starts discharging & drain current just start decrease. The time during which gate voltage decreases from V_1 level to V_{GSP} is called 'turn off delay time' t_{doff}. The time during which drain current becomes zero is called fall time t_f.

$$t_{off} = t_{doff} + t_f.$$

Q11. Explain with circuit diagram UJT Triggering circuit with waveforms.

Ans



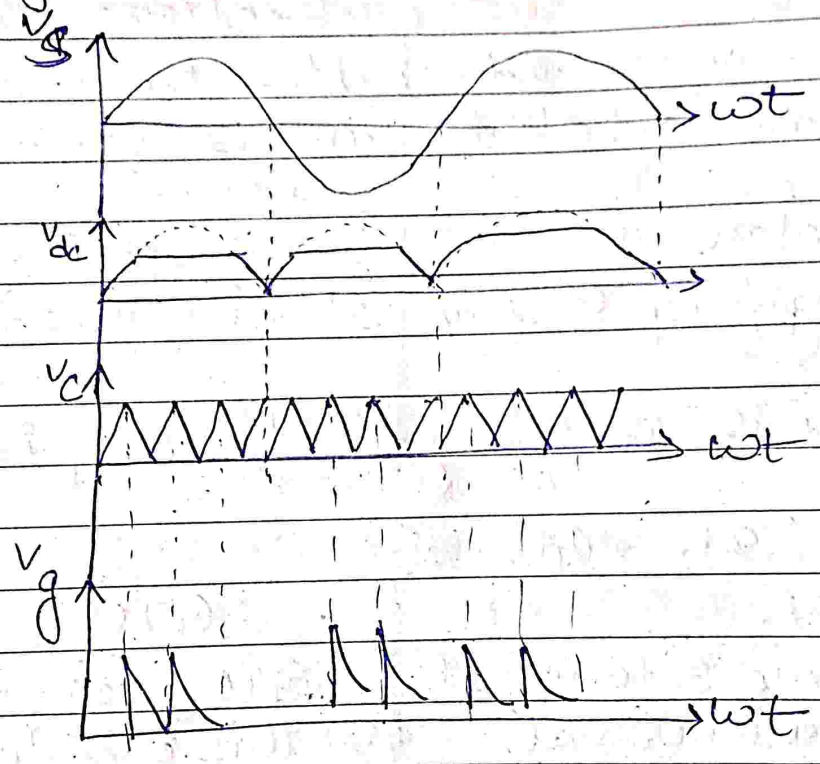
UJT triggering circuit consists of a bridge rectifier, a zener regulator & a UJT relaxation oscillator. Rectifier rectifies ac to dc, R_2 limits current through zener. Zener regulator clips rectified voltage to a constant level V_z. The voltage V_z acts as a V_{BB} for UJT ~~relaxation~~ relaxation oscillator.

When switched on, capacitor C start charging through R. When capacitor voltage V_c

PAGE No.
DATE / /

becomes equal to peak voltage of UJT V_p, junction E-B1 breaks & UJT conducts when UJT conducts, C discharges through UJT & primary winding of pulse transformer resulting a gate pulse across secondary of pulse transformer.

When charging resistance R is larger, capacitor C charges slowly & a single gate pulse will be obtained. When R is smaller, C charges rapidly to V_p, UJT conducts & C discharges. After discharging of C again it charges rapidly to V_p, again, UJT conducts & C discharges.



Q12. Compare power mosfet & IGBT

Ans

Power mosfet	IGBT
① Construction is done by injecting layer p^+ is absent.	① Injecting layer p^+ is pres to increase the conducti
② Input impendance is high.	② Input impedence is lower than MOSFET
③ t_{on} & t_{off} ~~very~~ small	③ t_{on} & t_{off} are large

(4) State resistance larger due to drift layer.	(4) State resistance smaller due to injection p^+ layer
(5) It is unipolar	(5) It is bipolar.
(6) Switching freq. is high.	(6) Switching freq are smaller.

Q13. Compare Power mosfet & SCR.

Ans

Power mosfet	SCR.
(1) SiO_2 layer is present to isolate the gate.	(1) SiO_2 layer is ~~present~~ absent in the construction.
(2) State resistance is larger	(2) State resistance is smaller.
(3) t_{on} & t_{off} is very small	(3) t_{on} & t_{off} is ~~very~~ large
(4) It is voltage controlled device.	(4) It is current controlled device.
(5) It is unipolar	(5) It is bipolar.
(6) Switching freq is very high.	(6) Switching freq is low
(7) Efficiency is less	(7) Efficiency is more.

Q14. Compare SCR & GTO.

Ans

SCR	GTO
(1) ~~They~~ SCR have 3 terminal	(1) GTO has 3 terminal
(2) It is unidirectional	(2) It is unidirectional.
(3) Commutation circuit is required.	(3) Commutation circuit is not required.
(4) Shorted anode structure is not used.	(4) Shorted anode structure is used.
(5) Turn off time is 5 to 30 μs.	(5) Turn off time is 1 μs.
(6) Efficiency is low.	(6) Efficiency is high.
(7) Switching freq. is low	(7) Switching freq is higher than SCR.

PAGE No.
DATE / /

Numericals.

Q1. For an SCR, the gate-cathode characteristics have a straight line slope of 130 for trigger source voltage of 15V and allowable gate power dissipation of 0.5 watts compute.

i) Triggering voltage (V_g)

ii) Triggering Current (I_c)

iii) the gate source resistance (R_g)

Ans. Given

line slope = 130

$V_s = 15V$

$P = 0.5W$

$$\text{Slope} = \frac{V_g}{I_g}$$

$$\frac{V_g}{I_g} = 130 \quad \text{--- (1)}$$

$P = 0.5W$

$P = V_g \cdot I_g$

$V_g \cdot I_g = 0.5W$ --- (2)

from (1) & (2)

$130\, I_g^2 = 0.5$

$I_g = 0.062A$

$\boxed{I_g = 62mA}$

$V_g = 130 \times 0.062$

$\boxed{V_g = 8.06V}$

$V_s = R_g I_g + V_g$

$15 = R_g\, 62\times10^{-3} + 8.06$

$R_g(62\times10^{-3}) = 6.94$

$$R_g = \frac{6.94}{62\times10^{-3}}$$

$$\boxed{R_g = 111.935\,\Omega}$$

Q2. The trigger circuit of a thyristor has a source voltage of 15 V & the load line has a slope of −120 V per ampere. The minimum gate current to turn on the SCR is 25 mA. Compute
i) Source resistance required in gate circuit.
ii) The trigger voltage & trigger current for an average gate power dissipation of 0.4 W.

Ans Given

$V_s = 15\,V$

load line slope $\left(\frac{V_g}{I_g}\right) = -120\ V/A = R_g$

$I_{gmin} = 25\,mA$.

ii)

$V_s = R_g I_g + V_g$

$15 = 120\,I_g + \frac{0.4}{I_g}$

$15 I_g = 120 I_g^2 + 0.4$

$120 I_g^2 - 15 I_g + 0.4 = 0$

$I_g = 0.086\,A$ & $0.038\,A$

$= 86\,mA$ & $38\,mA$.

we know,

$I_g \geq 2 I_{min}$.

$I_{min} = 25\,mA$

$\boxed{I_g = 86\,mA.}$

$V_g . I_g = 0.4$

$V_g = \frac{0.4}{86} \times 10^3$

$\boxed{V_g = 4.65\,V}$

13/3/23