



Dr. Vishwanath Karad

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TECHNOLOGY, RESEARCH, SOCIAL INNOVATION & PARTNERSHIPS

Basics of Electrical and Electronics Engineering

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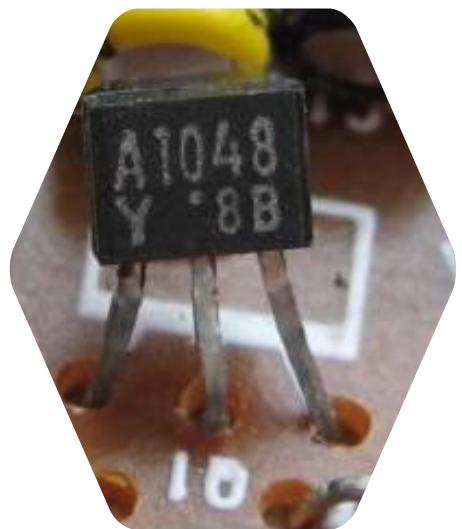
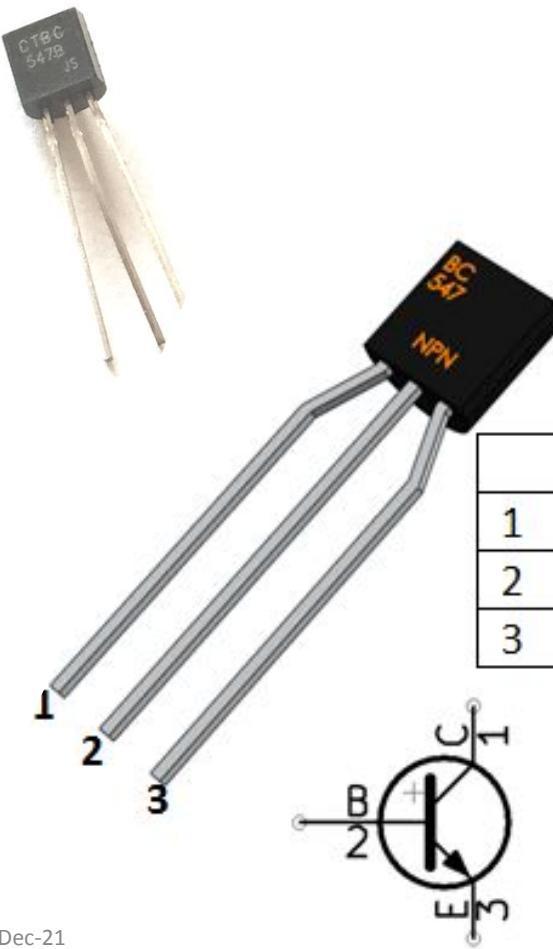


Contents of Unit 2 - Bipolar Junction Transistor (Duration:8L)

- BJT-Working principle
- Operation of Common Emitter (CE), Common Base (CB), Common Collector (CC) Configurations
- V-I characteristics
- Biasing circuits
- CE amplifier and its DC and AC Analysis with h parameter model

Unit-2

Bipolar Junction Transistor- BJT



First – BJT (History)

The transistor was probably the most important invention of the 20th Century,

Shockley, Bardeen and Brattain three shared a Nobel Prize in 1955 for invention of transistor.



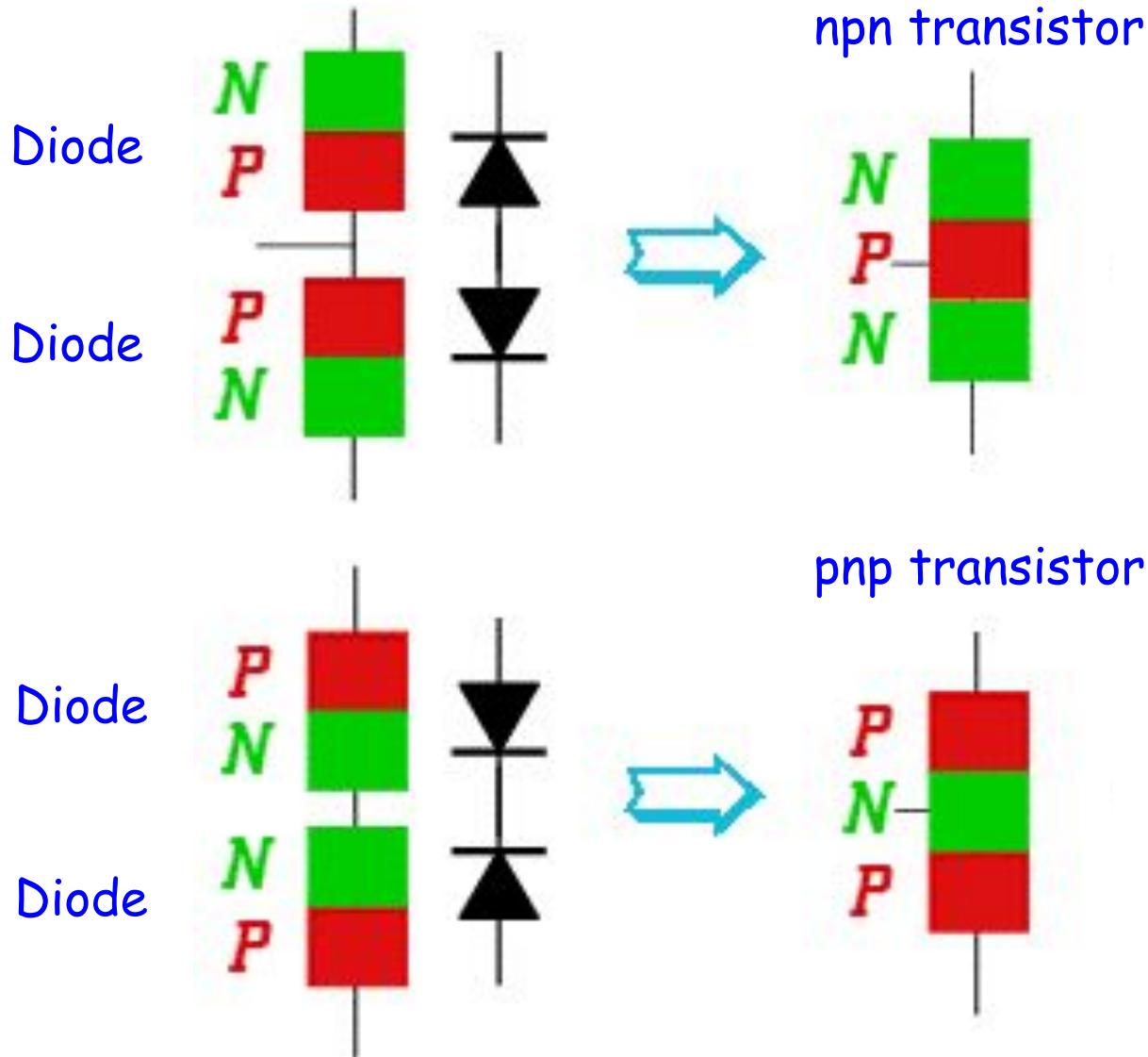
Introduction

- Bipolar transistors are one of the main ‘building-blocks’ in electronic systems
- They are used in both analog and digital circuits
- The transistor is a three-layer semiconductor device consisting of two n-type and one p-type layers of material or two p-type and one n-type layers of material.

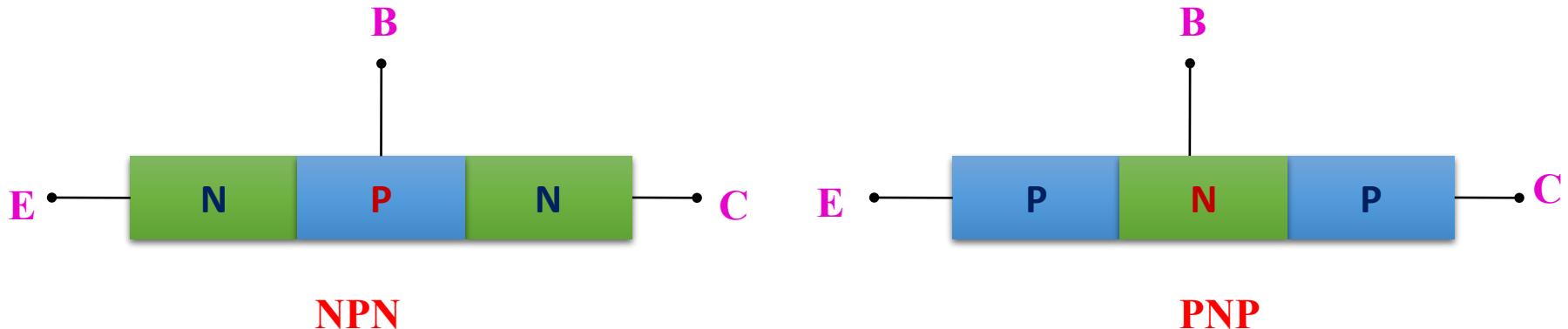
Bipolar junction transistors (BJT)

- **Bipolar junction transistors** or **BJTs** includes two PN junctions
- The term bipolar reflects the fact that holes and electrons involve in the current flow.
- The BJT is analogous to a vacuum triode and is comparatively smaller in size.
- It is used in amplifier and oscillator circuits, and as a switch in digital circuit.
- It has wide applications in computers, satellites and other modern communication system.

Basic models of BJT



NPN and PNP



- The three sections of the transistor are **Emitter, Base and Collector**, shown as E, B, and C, respectively.
- **Emitter is heavily doped** so that it can inject a large number of charge carriers into the base.
- **Base is lightly doped** and very thin. It passes most of the injected charge carriers from the emitter into the collector.
- **Collector is moderately doped**.

Datasheet of transistor



2N3903, 2N3904 (Silicon) NPN Transistors



NPN silicon annular transistors, designed for general purpose switching and amplifier applications.

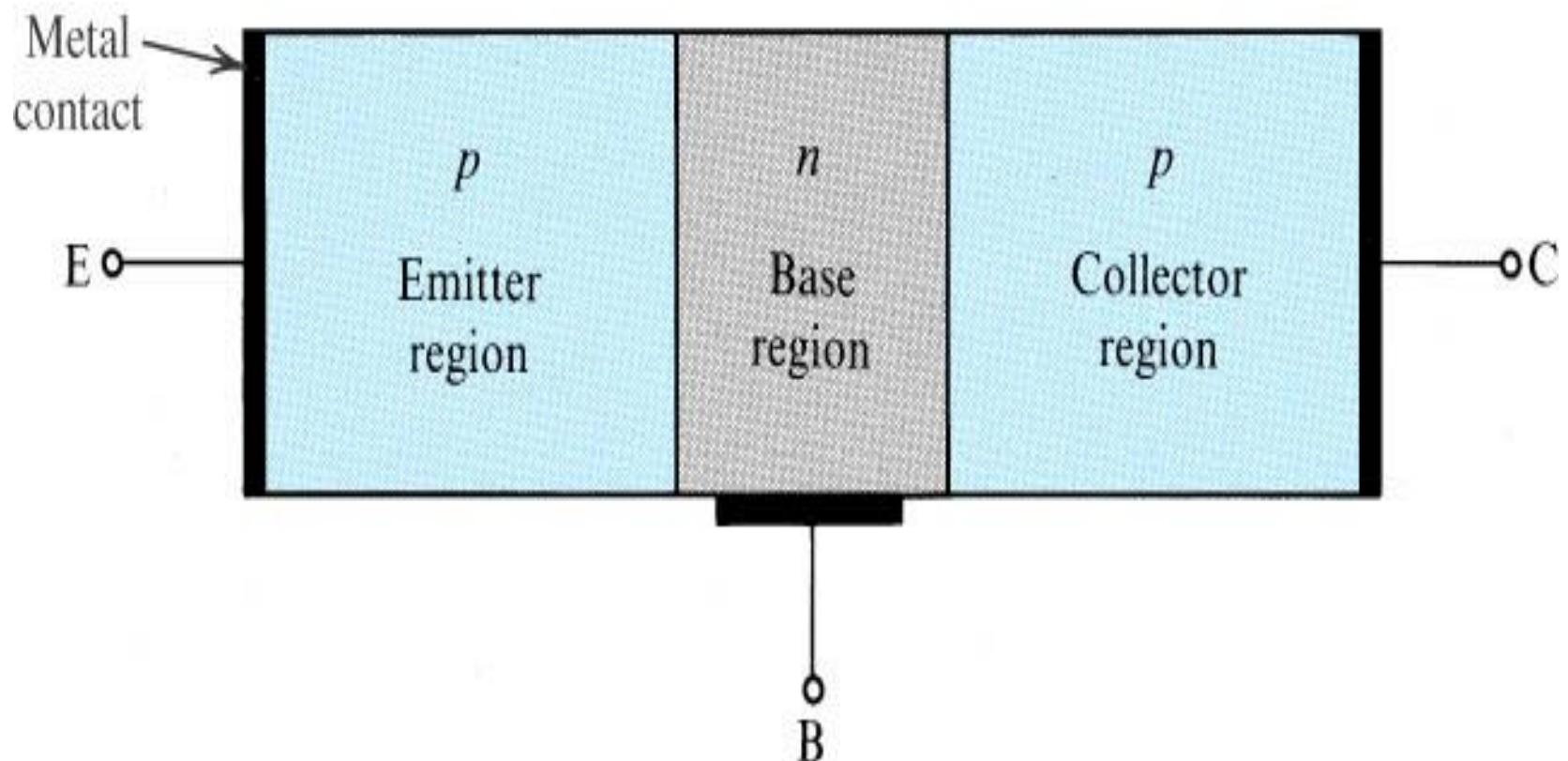
EBC

Maximum ratings at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Characteristic	Symbol	Rating	Unit
Collector-emitter voltage	V_{CEO}	40	V_{dc}
Emitter-base voltage	V_{EB}	6	V_{dc}
Collector Current	I_C	200	mA

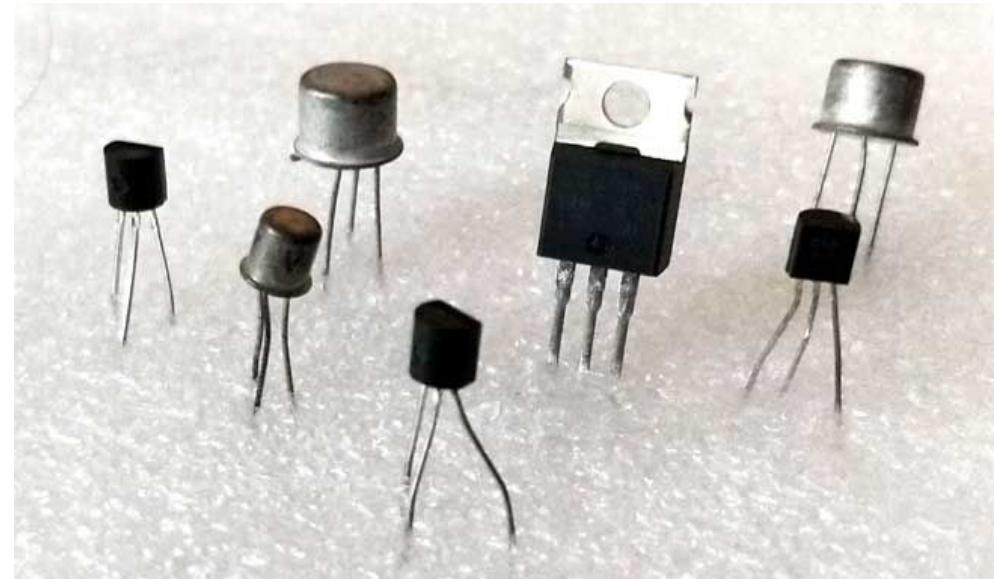
Figure 8-1
Portion of 2N3903-2N3904
transistor data sheet listing
maximum terminal voltages and
collector current.

Physical Structure PNP transistor



NPN vs PNP Transistors

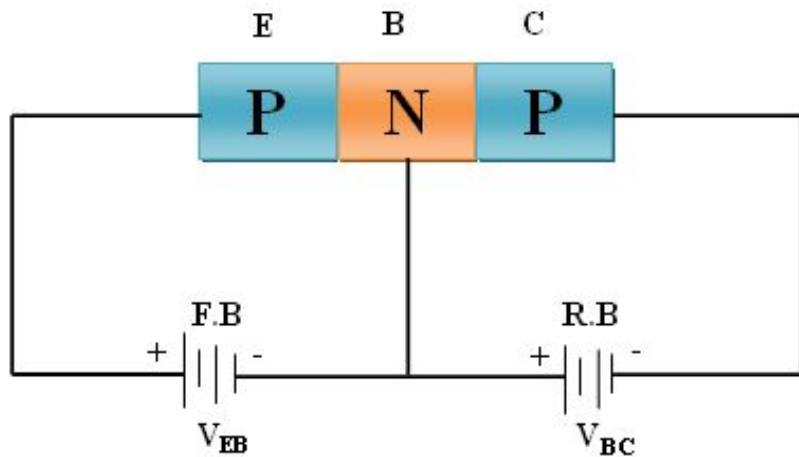
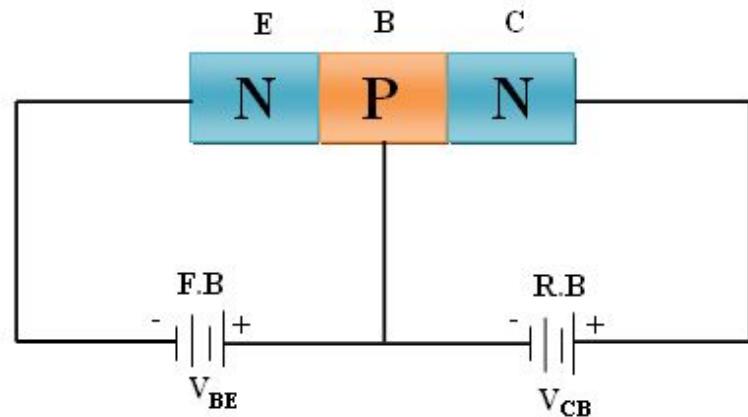
- NPN and PNP BJTs function the same way
- Power supply polarities are reversed for biasing
- Current direction is reversed in a cct
- NPN is more widely used in ccts



Transistor biasing

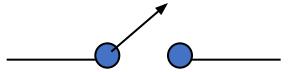
- The figure shows, usually the emitter-base junction is forward biased and collector-base junction is reverse biased.
- Due to the forward bias on the emitter-base junction, an emitter current flows through the base into the collector.
- Though the collector-base junction is reverse biased, almost the entire emitter current flows through the collector circuit.

NPN Transistor biasing

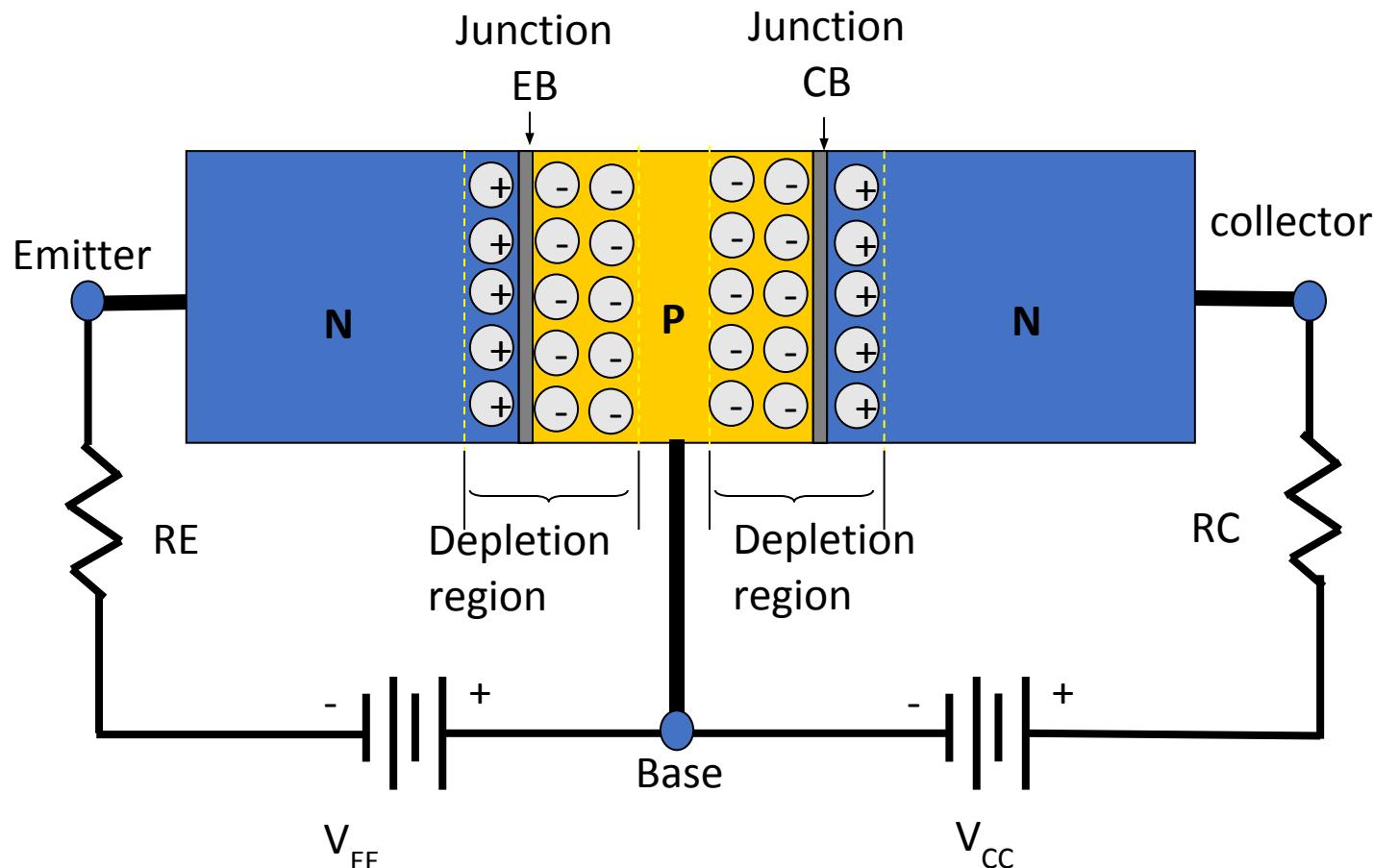


PNP Transistor biasing

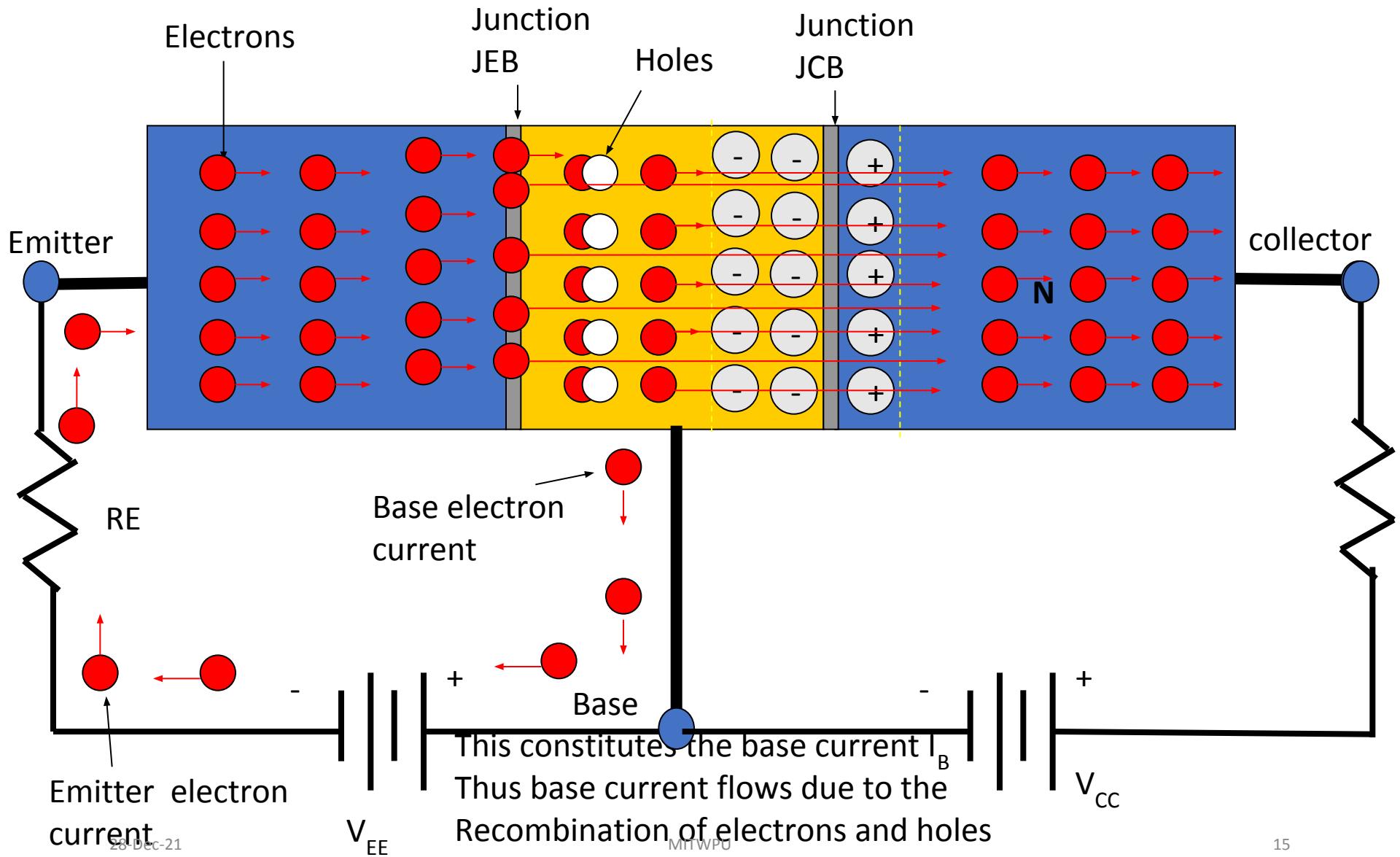
Transistor biasing in different region of operation:

Sr. No.	Region of operation	Base emitter junction	Collector base junction	application
1	Cutoff region	Reverse biased	Reverse biased	
2	Saturation region	Forward biased	Forward biased	
3	Active region	Forward biased	Reverse biased	Amplifier

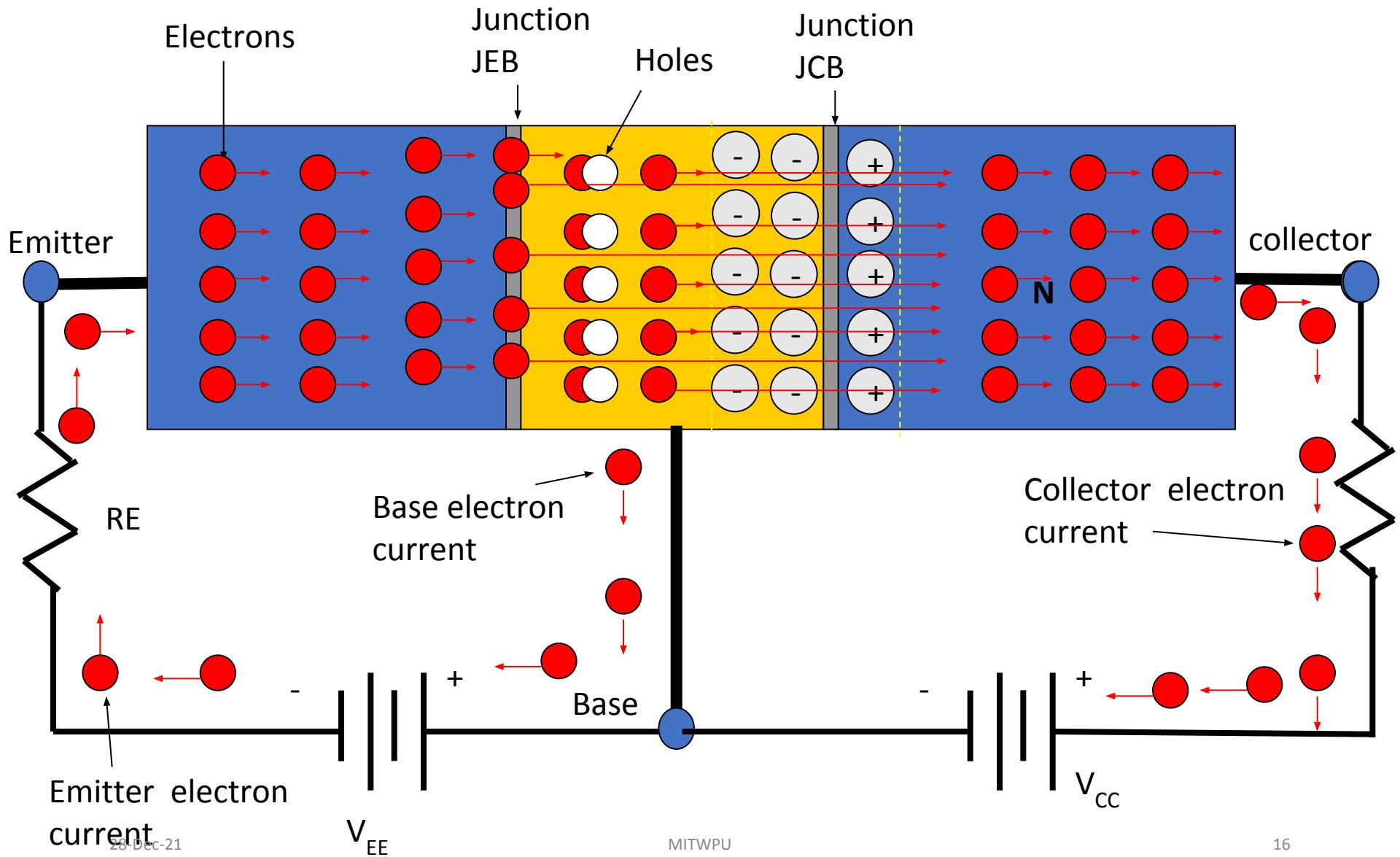
Transistor operation in the active region (NPN)



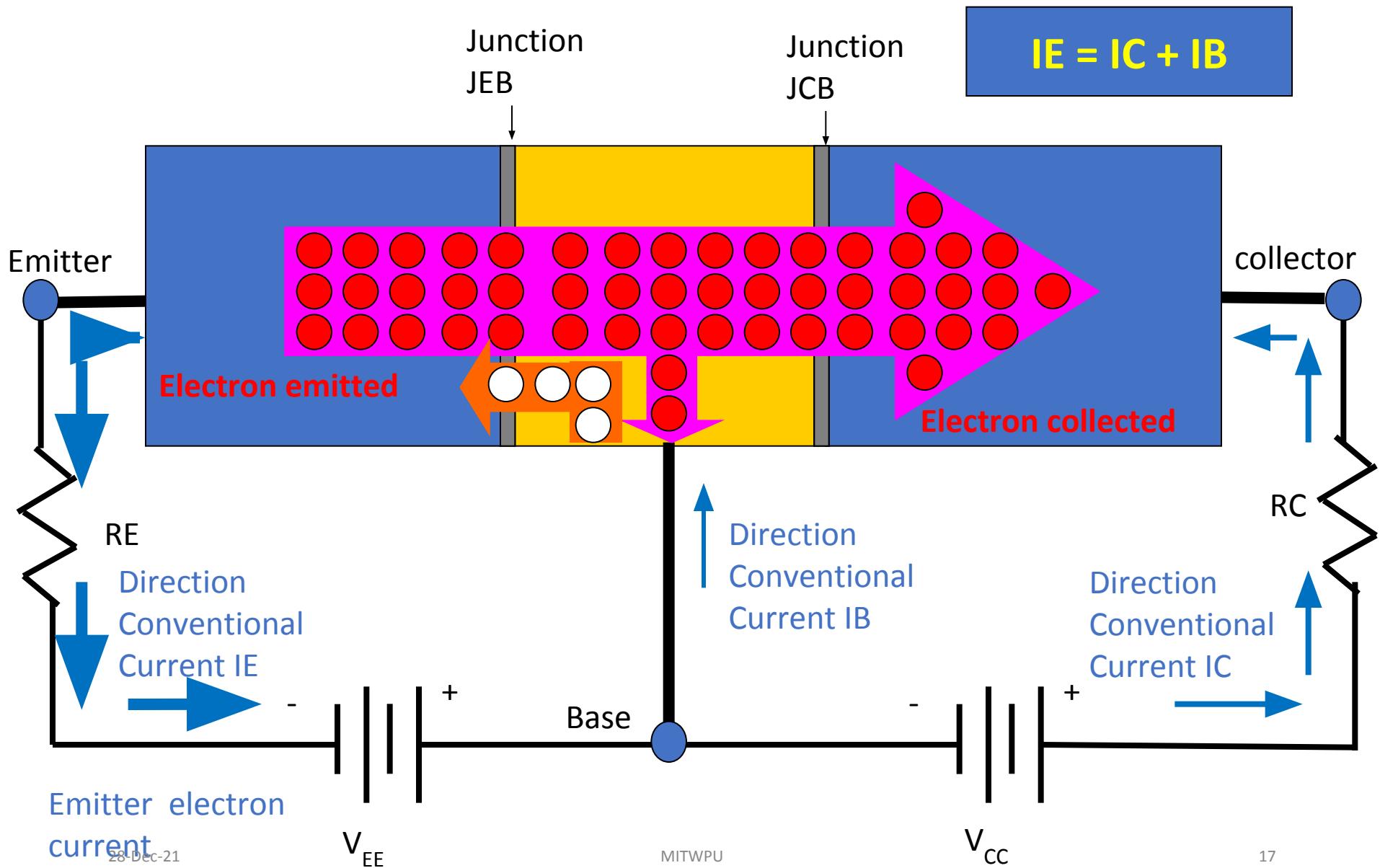
Transistor operation in the active region (NPN)



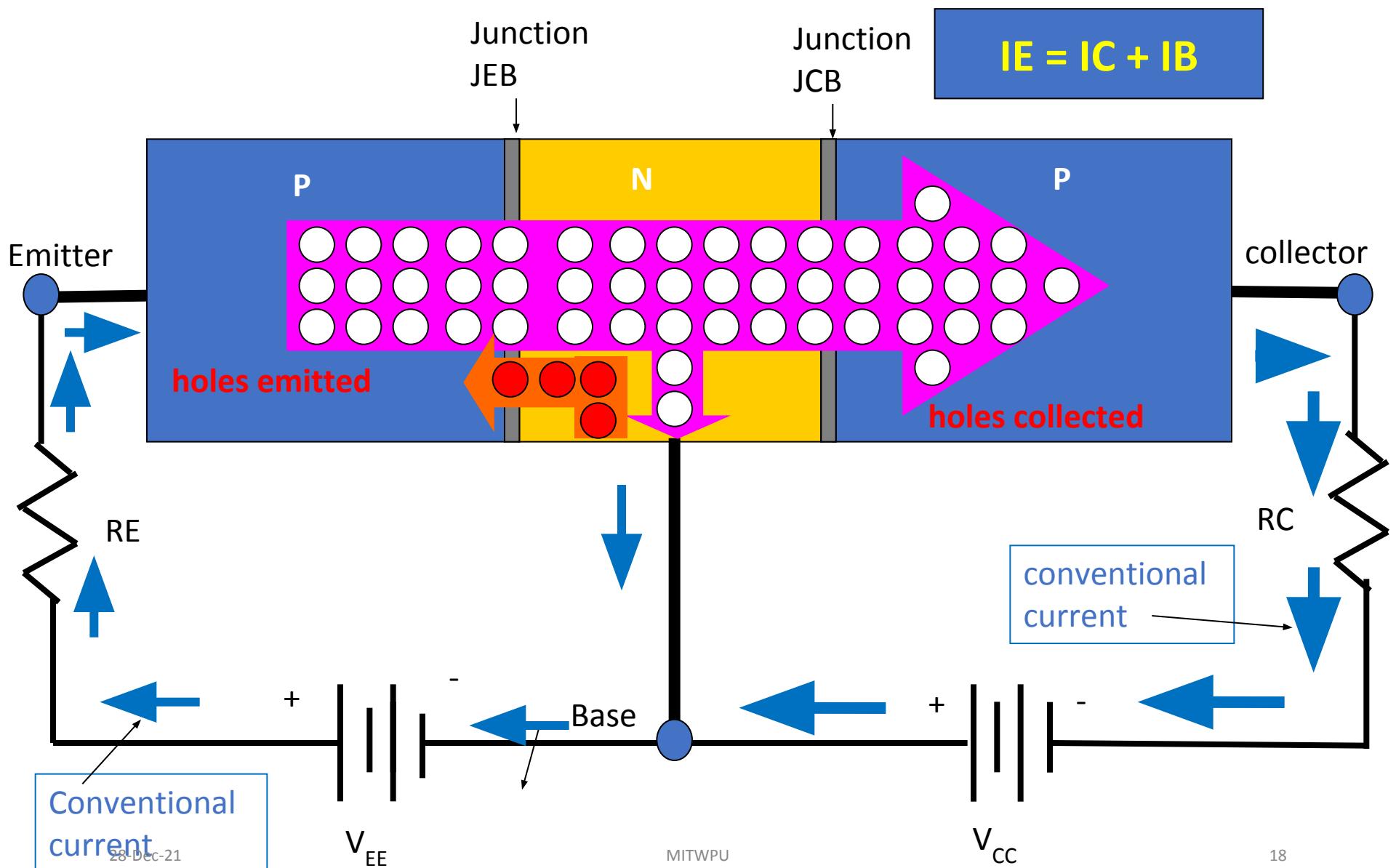
Transistor operation in the active region (NPN)



Transistor operation in the active region (NPN)



Transistor operation in the active region (PNP)



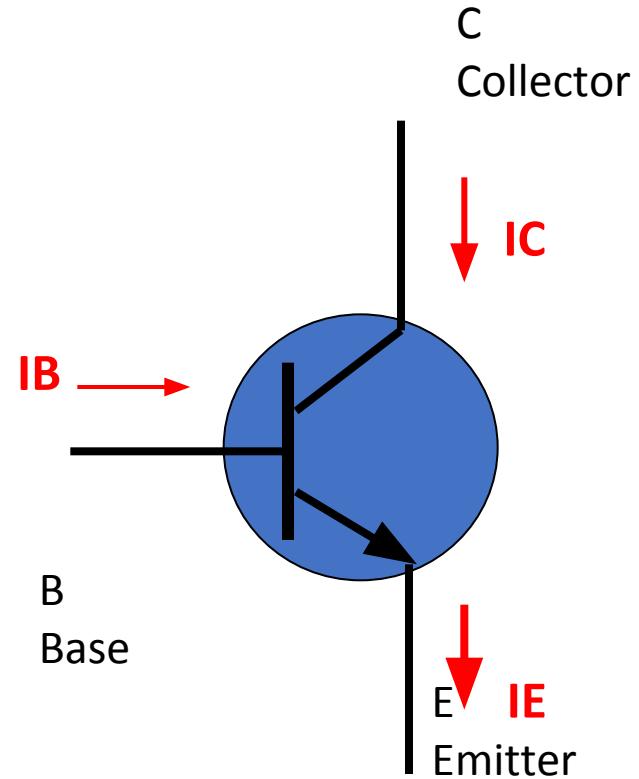
Transistor currents:

- As discussed earlier, the electrons injected from emitter into base constitute the emitter current (I_E).
- Out of these electrons very few will combine with the holes in the thin base region to constitute the base current (I_B).
- The remaining electrons pass through to the collector region and then to the positive end of V_{cc} to constitute the collector current (I_C).

Transistor currents:

- Therefore we can write that

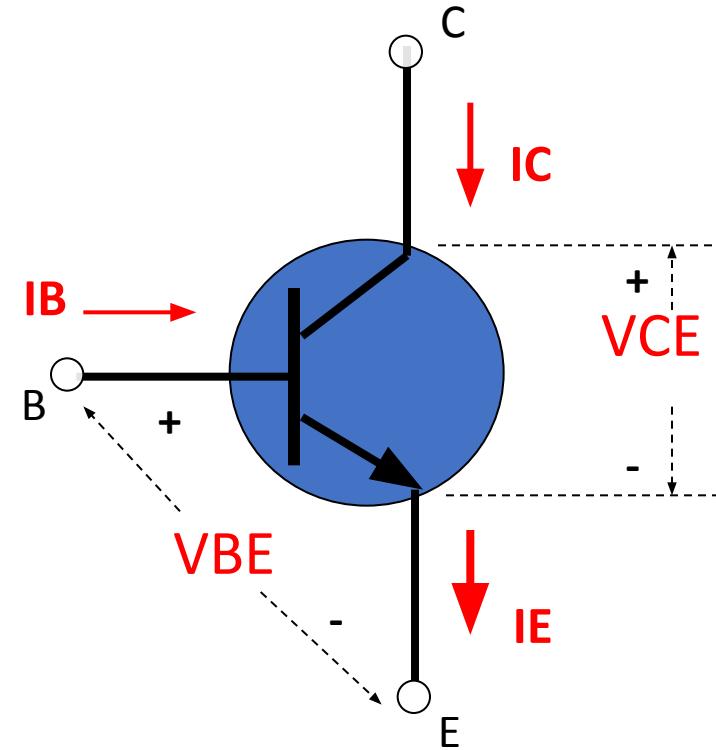
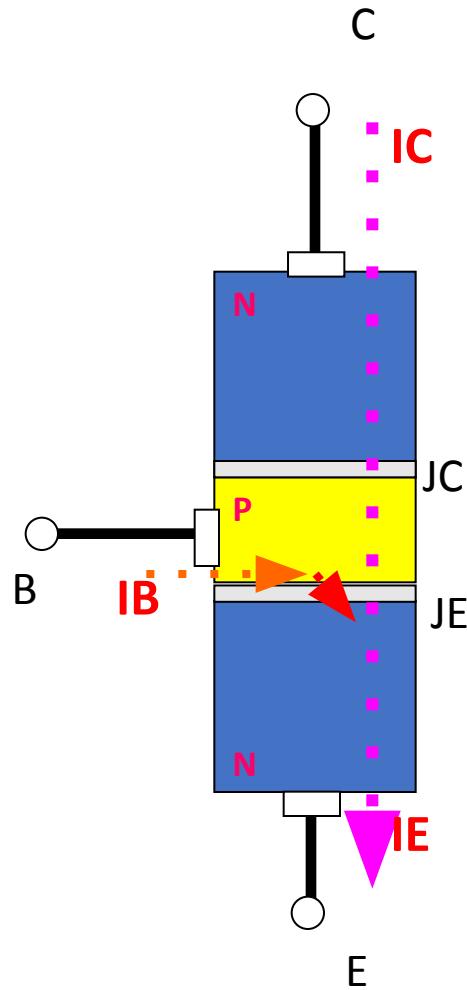
$$I_E = I_C + I_B$$



- Emitter current is always equal to the sum of collector current and base current.
- As I_B is very small as compared to I_E we can assume the collector current to be nearly equal to the emitter current

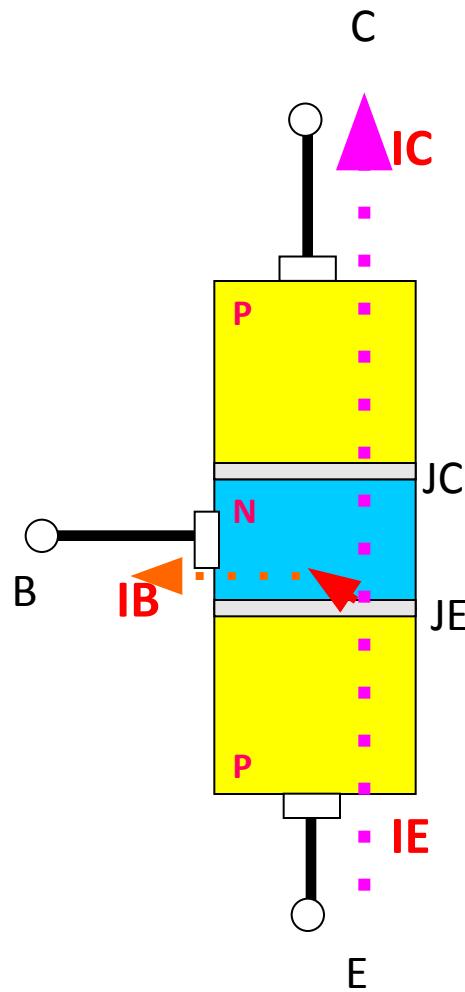
$$I_E \approx I_C$$

Circuit symbols and Transistor Terminal Voltages

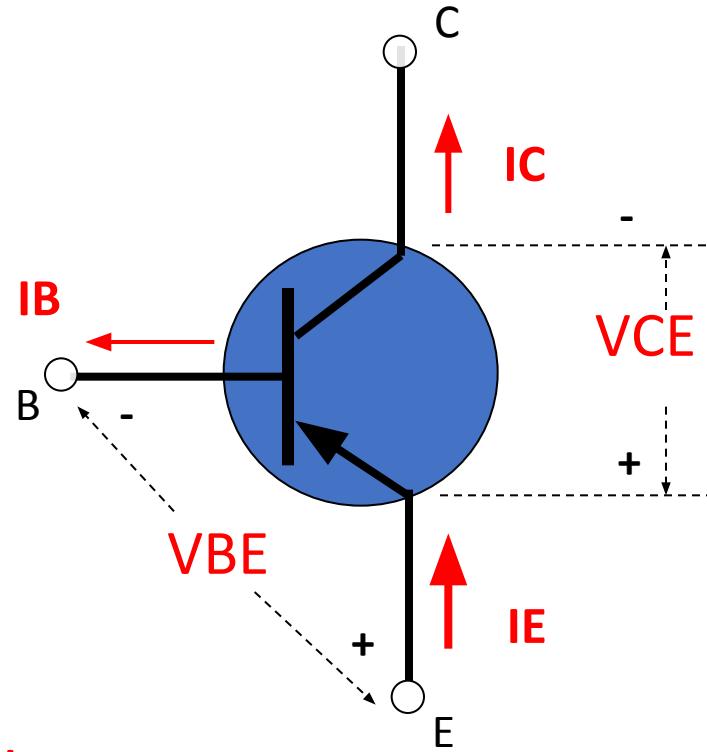


N-P-N Transistor

Circuit symbols and conventions of Transistor



P-N-P Transistor

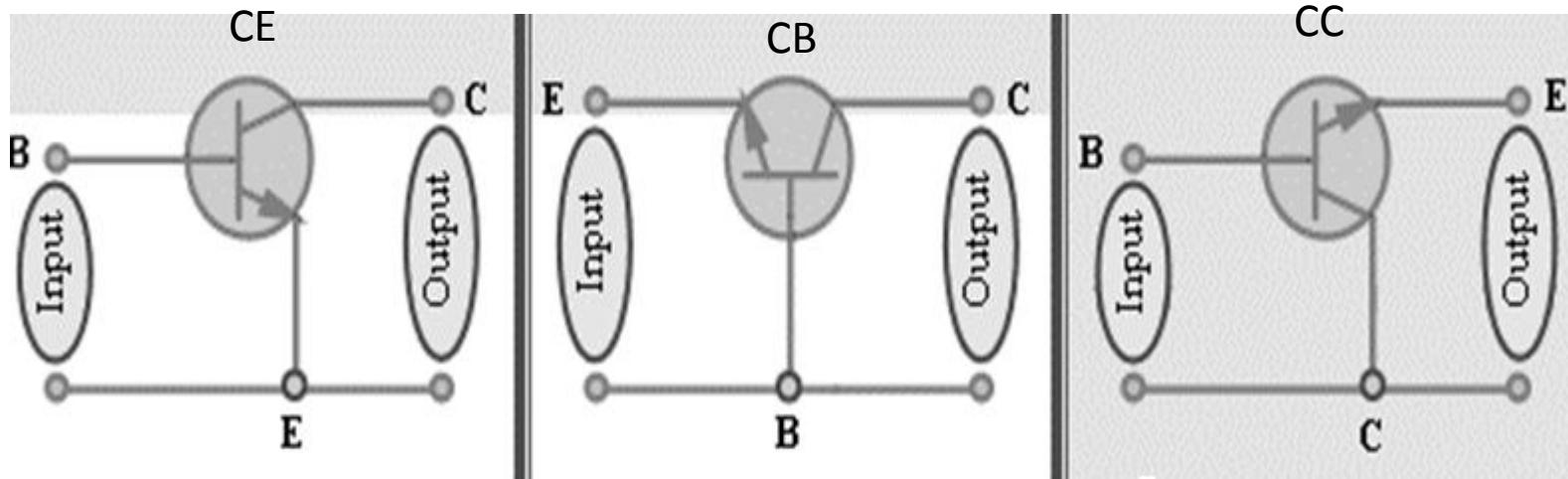


Transistor Working

- <https://youtu.be/7ukDKVHnac4>
- <https://www.youtube.com/watch?v=jKVPEIMybUg>

Transistor configurations:

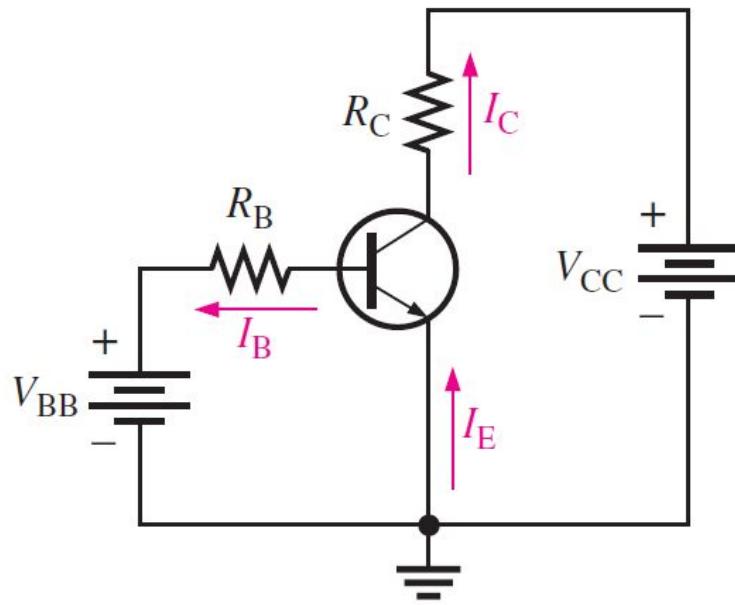
- Transistor is 3 terminal device, hence one of the three terminals “common” to input and output port.
- Depending on which terminal is made common to input and output port, there are three possible configurations of transistor, they are as follows:
 1. Common Base(CB) configuration
 2. Common Emitter(CE) configuration
 3. Common Collector(CC) configuration



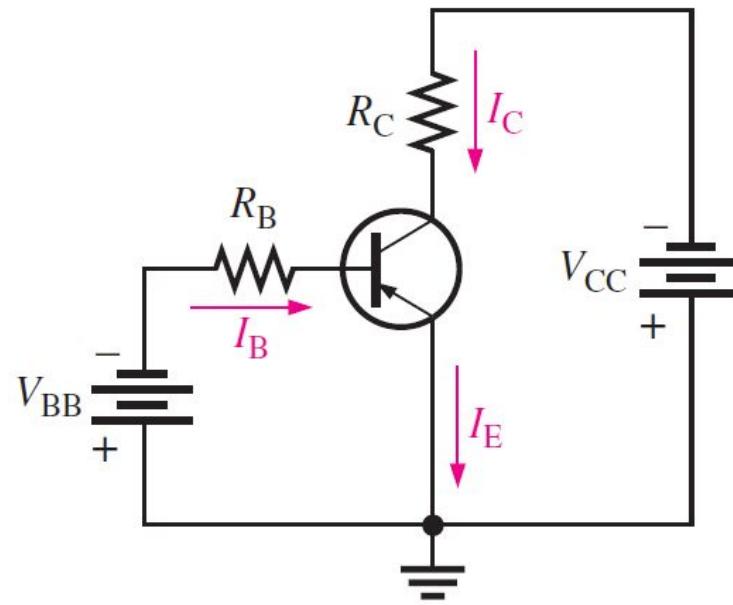
Common-Emitter Configuration

- It is called common-emitter configuration since :
 - emitter is common or reference to both input and output terminals.
 - emitter is usually the terminal closest to or at ground potential.
- CE configuration is used in amplifier circuits it provides the high gain for current and voltage.
- Two sets of characteristics are necessary to describe the behavior for CE; input (base terminal) and output (collector terminal) parameters.

Common Emitter (CE) Configuration



(a) *npn*



(b) *pnp*

Current gain (β_{dc}): $\beta_{dc} = I_C / I_B$

- In CE configuration, emitter acts as common terminal between input and output ports.
- The bias voltage V_{BB} is applied between base and emitter while bias voltage V_{CC} is applied between collector and emitter.

- **Current relations:**

For CE configuration, Collector current is given by

$$I_C = \beta_{dc} I_B + I_{CEO}$$

- **Current amplification factor or current gain (β_{dc}):**

The current amplification factor is the ratio of collector current to the base current

$$\beta = \frac{I_C}{I_B}$$

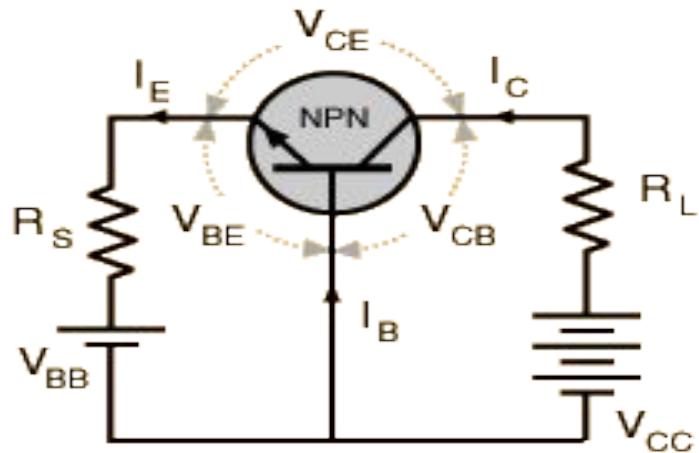
- **Two set of characteristics are necessary to describe the behavior for CE :**

1. Input characteristics (base terminal)
2. Output characteristics (collector terminal).

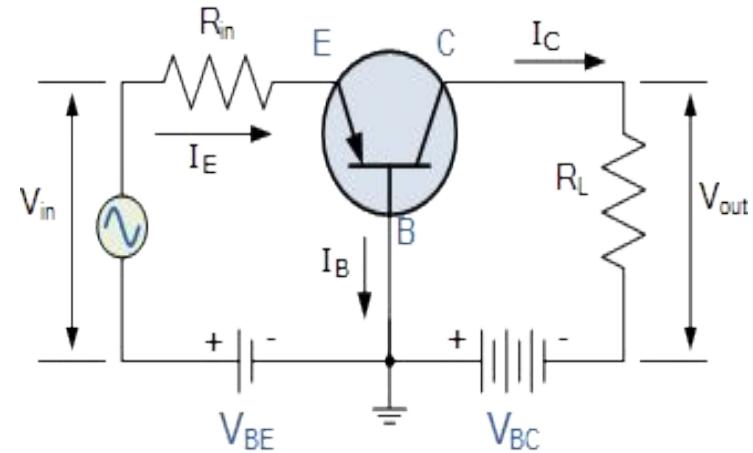
Common Base Configuration

- In this configuration, emitter is the input terminal, collector is the output terminal and base is the common terminal.
- The input is applied between the emitter and base terminals.
- The output is taken between the collector and base terminals.
- Used as current buffer as current gain is approximately one.

Common-Base (CB) Configuration



a) NPN transistor



b) PNP transistor

Current amplification factor (α_{dc}): $\alpha_{dc} = I_C / I_E$

- In CB configuration, base acts as common terminal between the input and output ports.
- The input voltage V_{EB} is applied between emitter and base while output voltage V_{CB} is taken between collector and base.

Current relations:

The output current I_C is given by

$$I_C = I_{C(INJ)} + I_{CBO}$$

where $I_{C(INJ)}$ = injected collector current

and I_{CBO} = reverse saturation current of CB junction

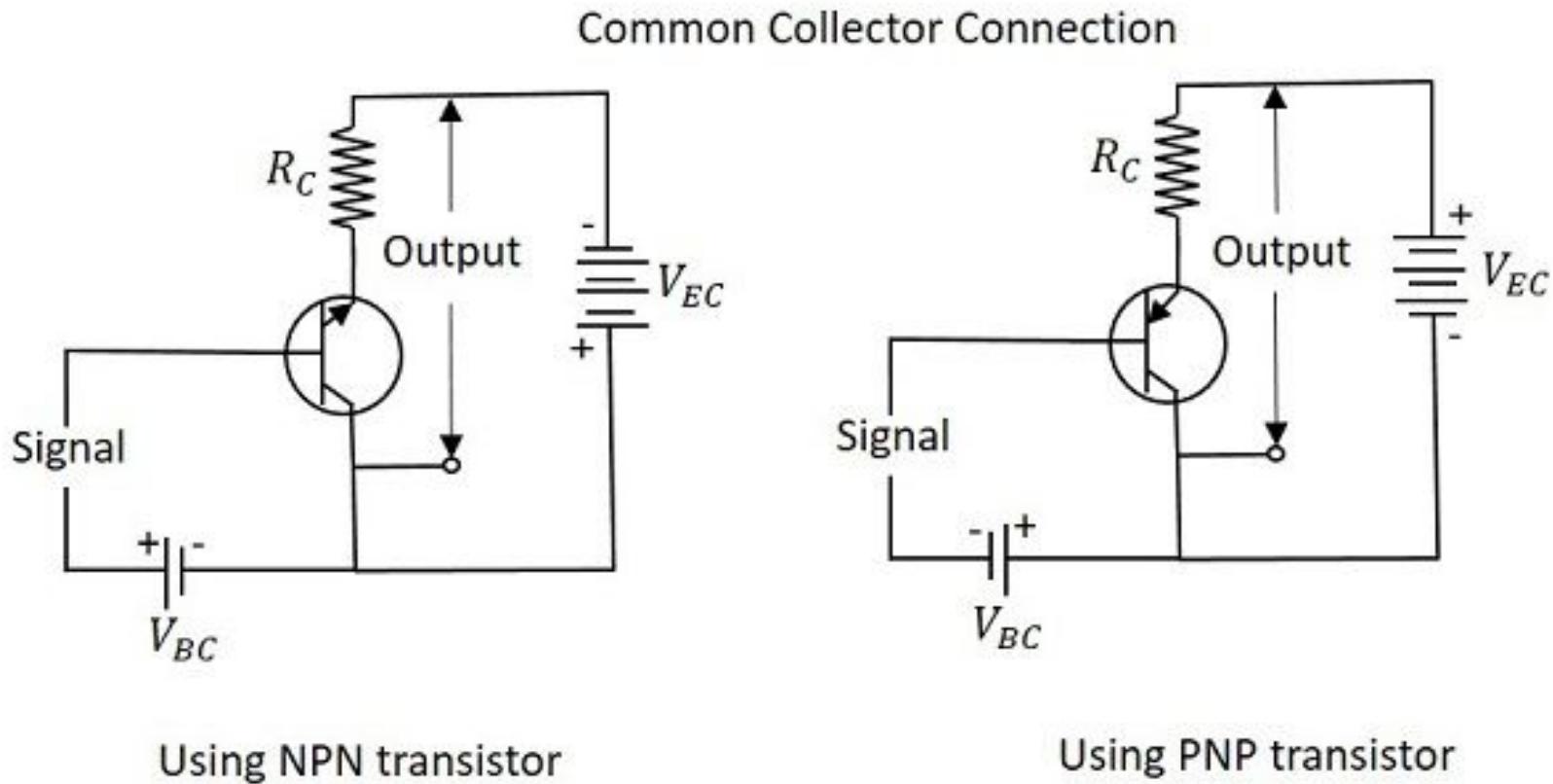
As I_{CBO} flows due to minority carriers, it is negligible as compared to $I_{C(INJ)}$,

$$\therefore I_C \approx I_{C(INJ)}$$

Common – Collector Configuration

- Also called emitter-follower (EF)
- It is called common-collector configuration since both the signal source and the load share the collector terminal as a common connection point.
- The input is applied between the base and collector terminals.
- The output voltage is obtained at emitter terminal.
- It is used primarily for impedance-matching purpose since it has high input impedance and low output impedance.

Common – Collector Configuration



Current amplification factor (γ_{dc}): $\gamma_{dc} = I_E / I_B$

Comparison of BJT circuit configurations

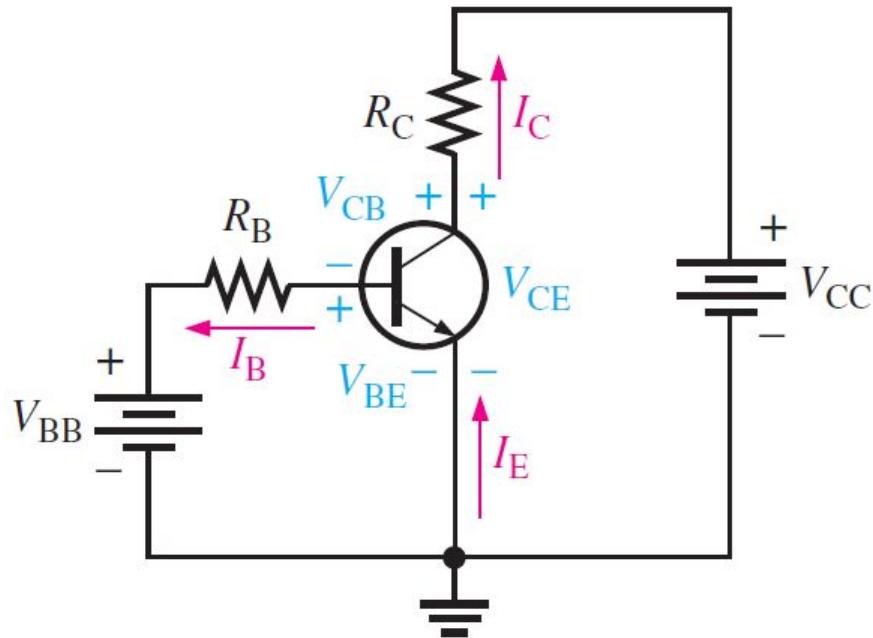
Sr. No.	Parameter	CB	CE	CC
1.	Input current	I_E	I_B	I_B
2.	Output current	I_C	I_C	I_E
3.	Current gain	Less than 1 $\alpha_{dc} = I_C / I_E$	Medium $\beta_{dc} = I_C / I_B$	Medium $\gamma_{dc} = I_E / I_B$
4.	Input voltage	V_{EB}	V_{BE}	V_{BC}
5.	Output voltage	V_{CB}	V_{CE}	V_{BC}
6.	Voltage gain	Medium	Medium	Less than 1
7.	Input resistance	Very low (20Ω)	Moderate ($1k\Omega$)	High ($500 k\Omega$)
8.	Output resistance	Very high ($1M\Omega$)	High ($40 K\Omega$)	Low (50Ω)
9.	Phase shift between input and output	0°	180°	0°
10.	Applications	As preamplifier	Audio amplifier	For impedance matching

BJT Circuit Analysis

I_B : dc base current

I_E : dc emitter current

I_C : dc collector current

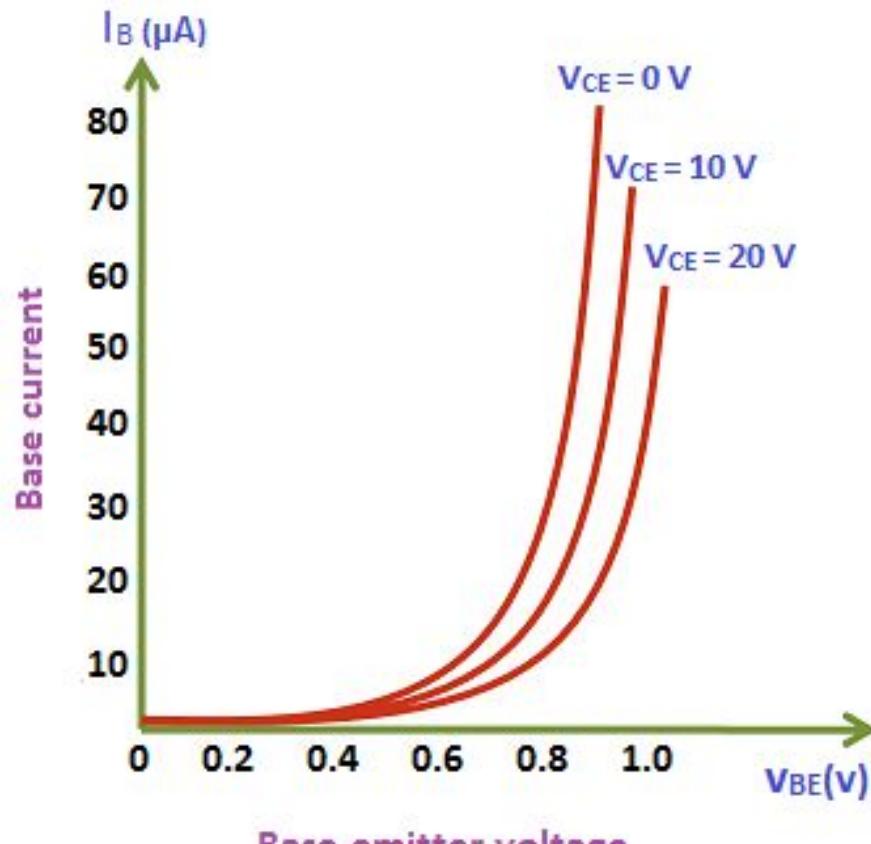


V_{BE} : dc voltage at base with respect to emitter

V_{CB} : dc voltage at collector with respect to base

V_{CE} : dc voltage at collector with respect to emitter

Input Characteristics



I/P characteristics CE configuration

- $V_{BE} = 0.7 \text{ V}$

voltage across R_B –

$$V_{R_B} = V_{BB} - V_{BE}$$

Also, by Ohm's law,

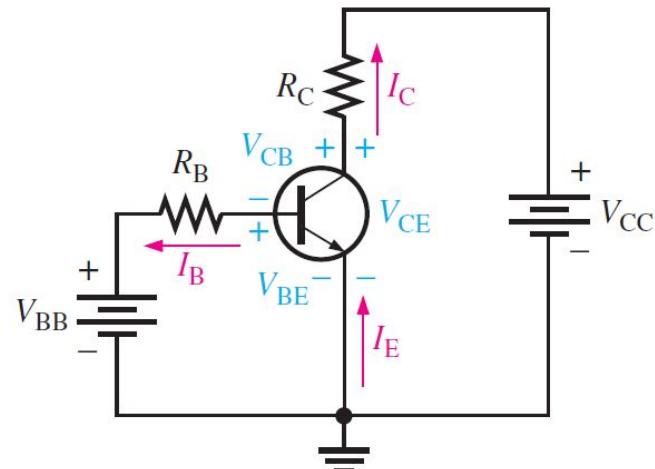
$$V_{R_B} = I_B R_B$$

Substituting for V_{R_B} yields

$$I_B R_B = V_{BB} - V_{BE}$$

Solving for I_B ,

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$



The voltage at the collector with respect to the grounded emitter is

$$V_{CE} = V_{CC} - V_{R_C}$$

Since the drop across R_C is

$$V_{R_C} = I_C R_C$$

the voltage at the collector with respect to the emitter can be written as

$$V_{CE} = V_{CC} - I_C R_C$$

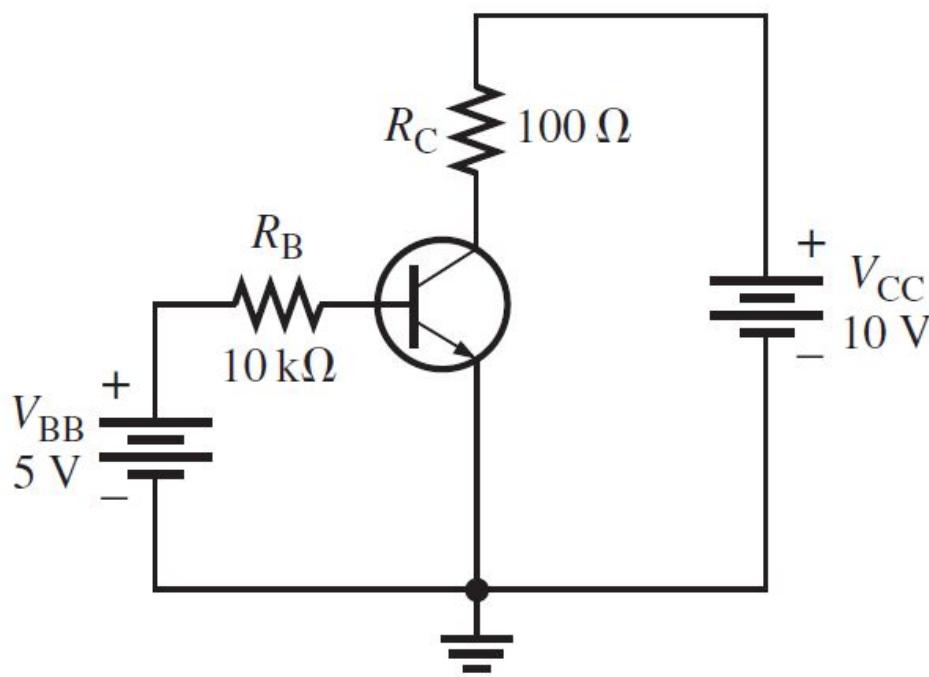
where $I_C = \beta_{DC} I_B$.

The voltage across the reverse-biased collector-base junction is

$$V_{CB} = V_{CE} - V_{BE}$$

Numerical 1: DC biasing of CE configuration

Determine I_B , I_C , I_E , V_{BE} , V_{CE} , and V_{CB} in the circuit shown below. The transistor has a $\beta_{DC} = 150$.



Numerical 1 Solution

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5 \text{ V} - 0.7 \text{ V}}{10 \text{ k}\Omega} = 430 \mu\text{A}$$

$$I_C = \beta_{DC} I_B = (150)(430 \mu\text{A}) = 64.5 \text{ mA}$$

$$I_E = I_C + I_B = 64.5 \text{ mA} + 430 \mu\text{A} = 64.9 \text{ mA}$$

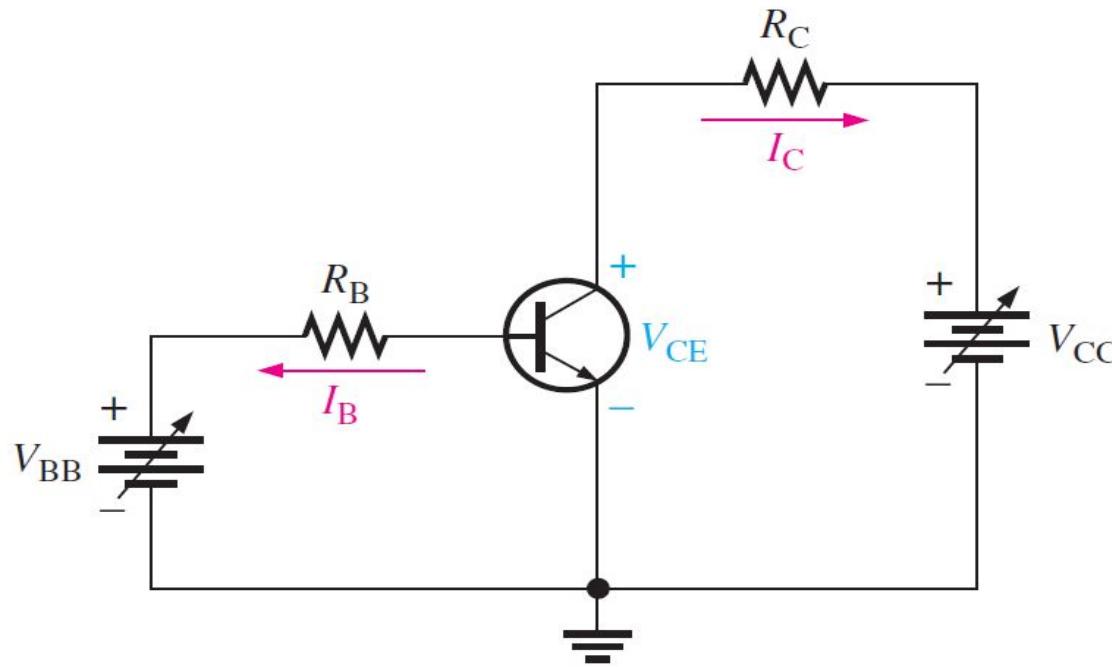
Solve for V_{CE} and V_{CB} .

$$V_{CE} = V_{CC} - I_C R_C = 10 \text{ V} - (64.5 \text{ mA})(100 \Omega) = 10 \text{ V} - 6.45 \text{ V} = 3.55 \text{ V}$$

$$V_{CB} = V_{CE} - V_{BE} = 3.55 \text{ V} - 0.7 \text{ V} = 2.85 \text{ V}$$

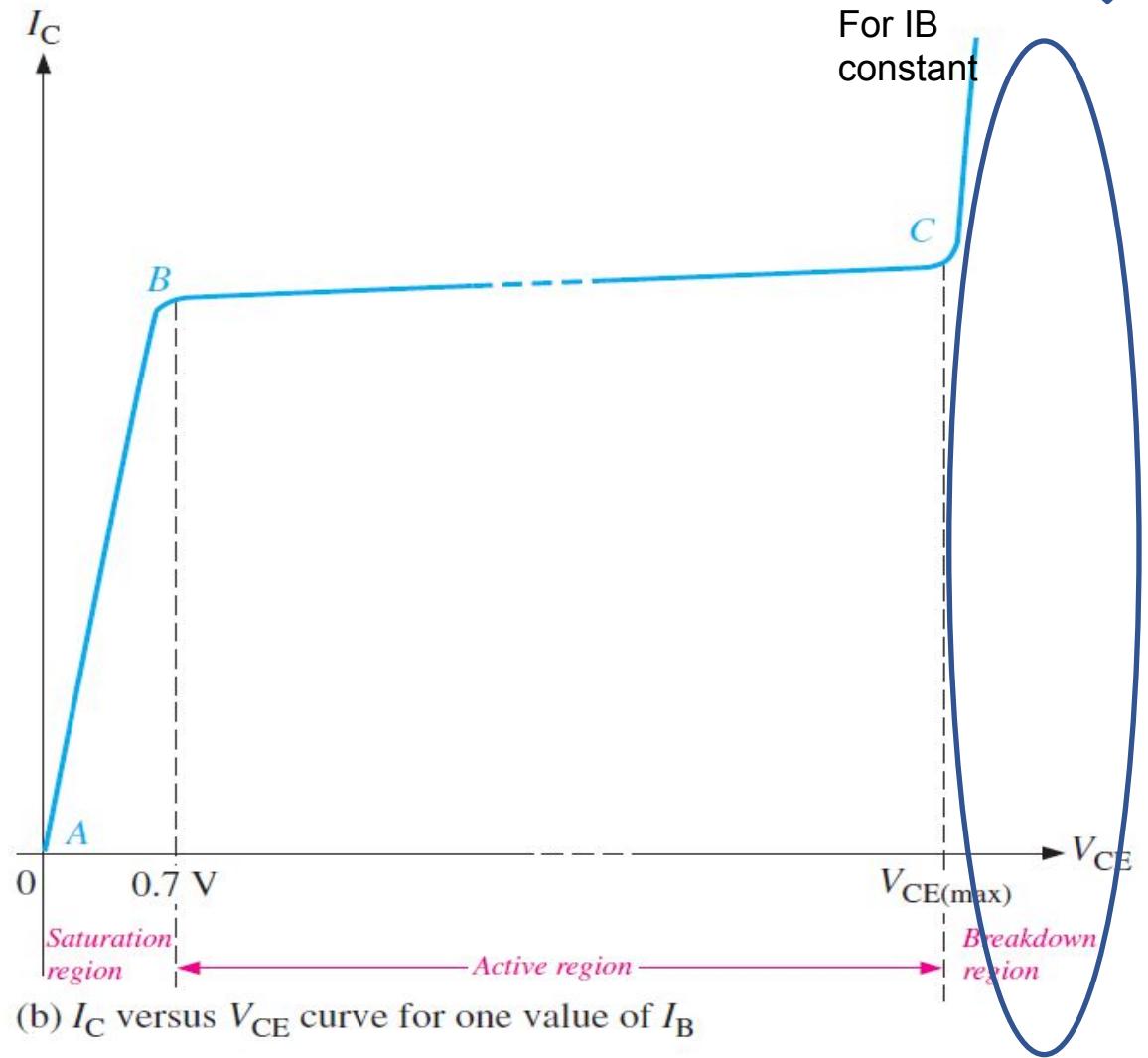
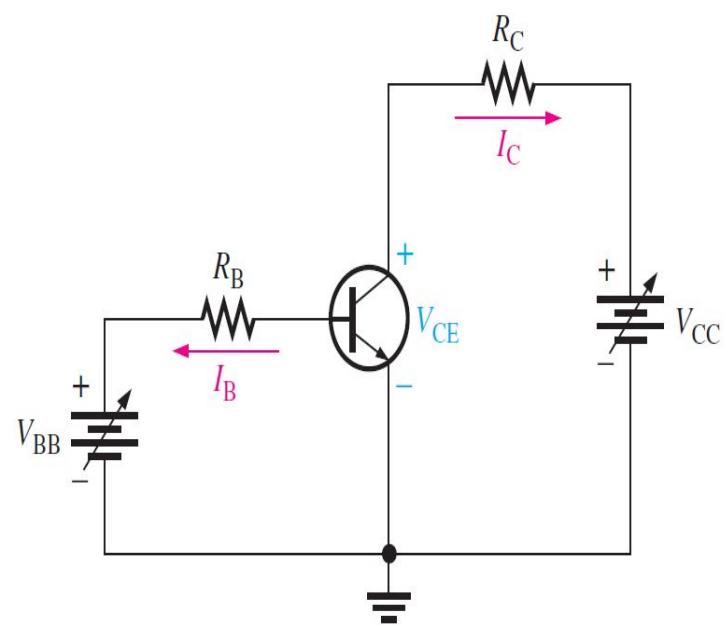
Since the collector is at a higher voltage than the base, the collector-base junction is reverse-biased.

Collector Characteristic – Output Characteristics

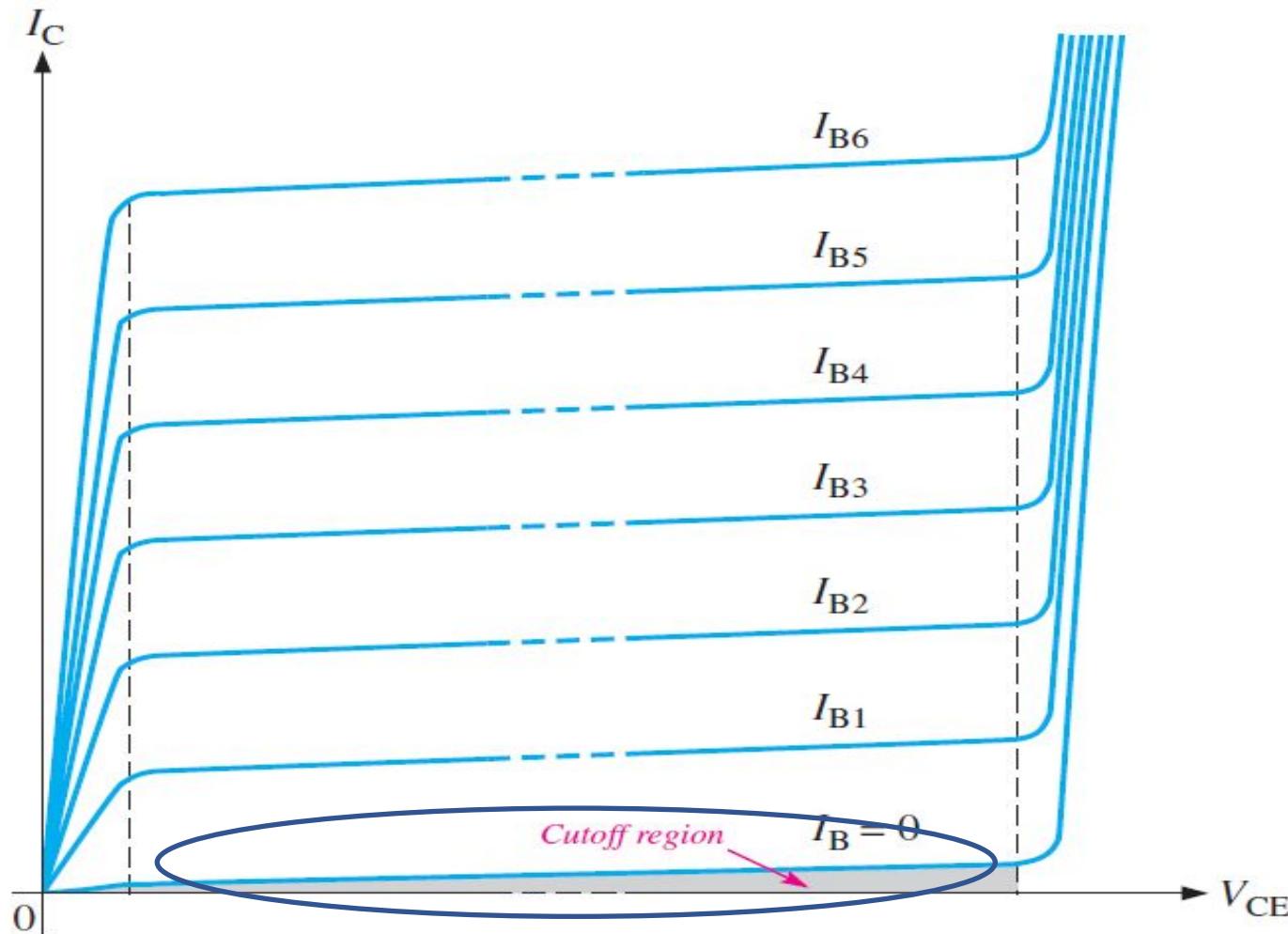


A set of collector characteristic curves can be generated that show how the collector current, I_C , varies with the collector-to-emitter voltage, V_{CE} , for specified values of base current, I_B .

Collector Characteristic Curve

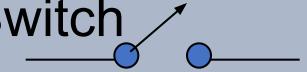
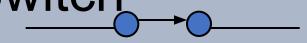


Family of Collector Characteristic Curves

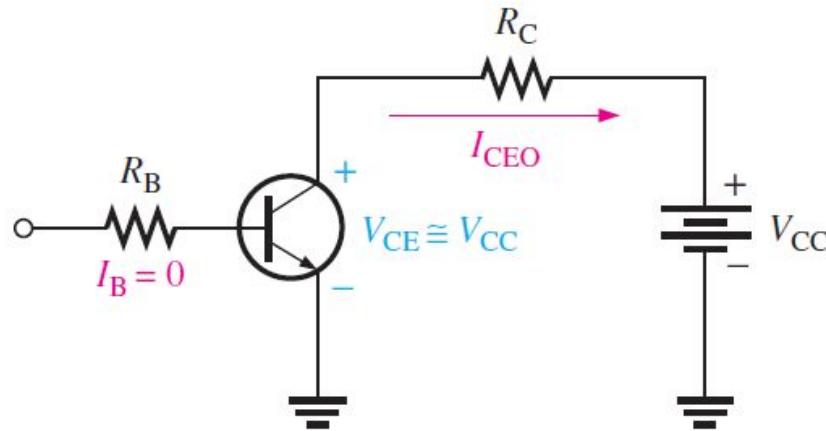


(c) Family of I_C versus V_{CE} curves for several values of I_B
($I_{B1} < I_{B2} < I_{B3}$, etc.)

Transistor biasing in different region of operation:

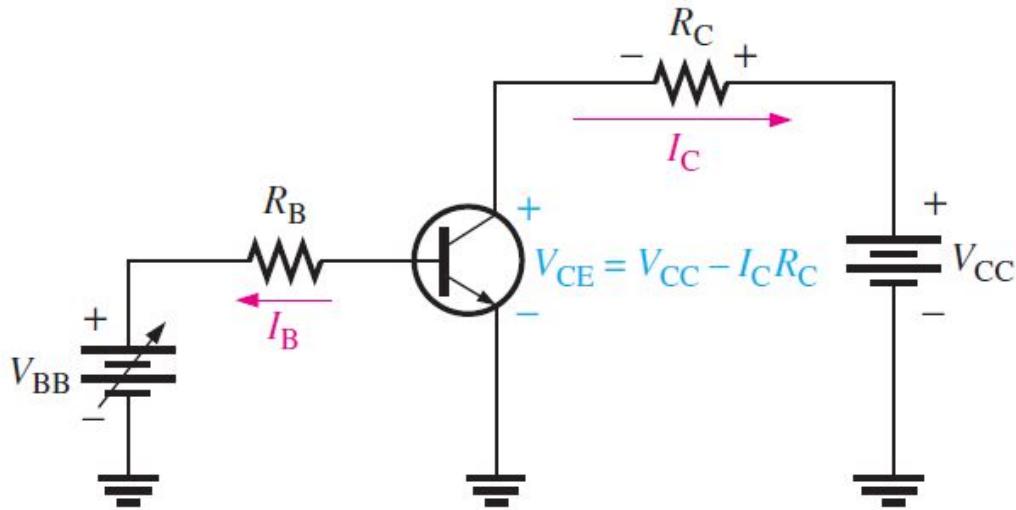
Sr. No.	Region of operation	Base emitter junction	Collector base junction	Application
1	Cutoff region	Reverse biased	Reverse biased	Switch 
2	Saturation region	Forward biased	Forward biased	Switch 
3	Active region	Forward biased	Reverse biased	Amplifier

Cutoff region



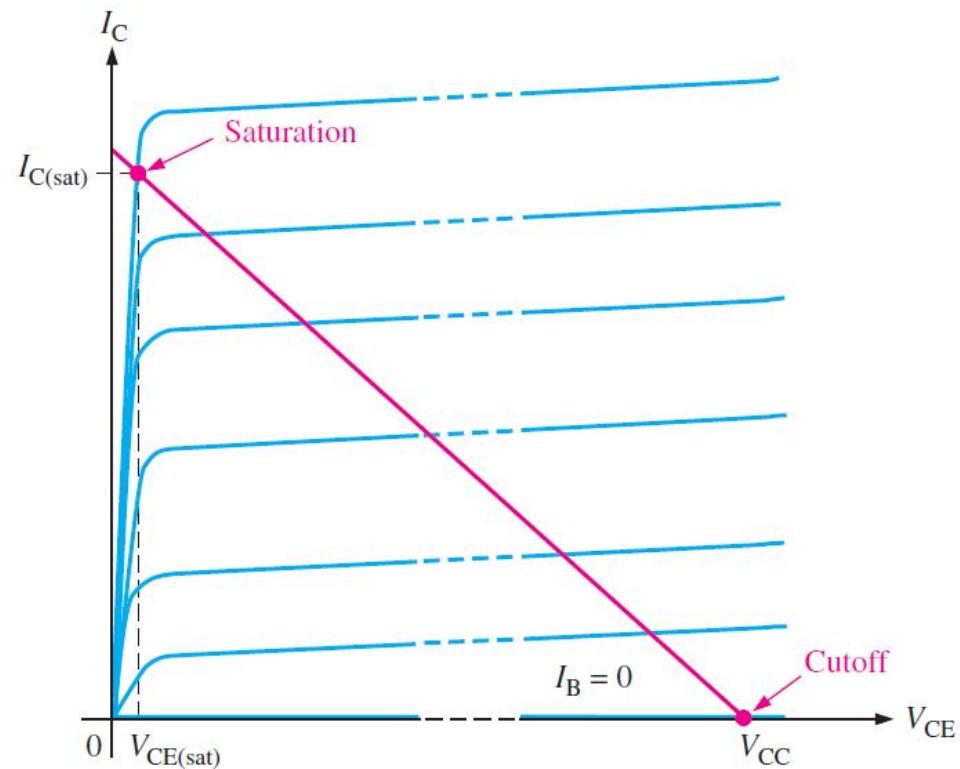
- When $I_B = 0$, the transistor is in the cutoff region of its operation.
- This is shown in Figure with the base lead open, resulting in a base current of zero.
- Under this condition, there is a very small amount of collector leakage current, I_{CEO} , due mainly to thermally produced carriers.
- Because I_{CEO} is extremely small, it will usually be neglected in circuit analysis so that
$$V_{CE} \approx V_{CC}$$
- In cutoff, neither the base-emitter nor the base-collector junctions are forward-biased.

Saturation region



- As I_B increases due to increasing V_{BB} , I_C also increases and V_{CE} decreases due to the increased voltage drop across R_C .
$$V_{CE(sat)} = 0.2V$$
- When the transistor reaches saturation, I_C can increase no further regardless of further increase in I_B .
- Base-emitter and base-collector junctions are forward-biased.

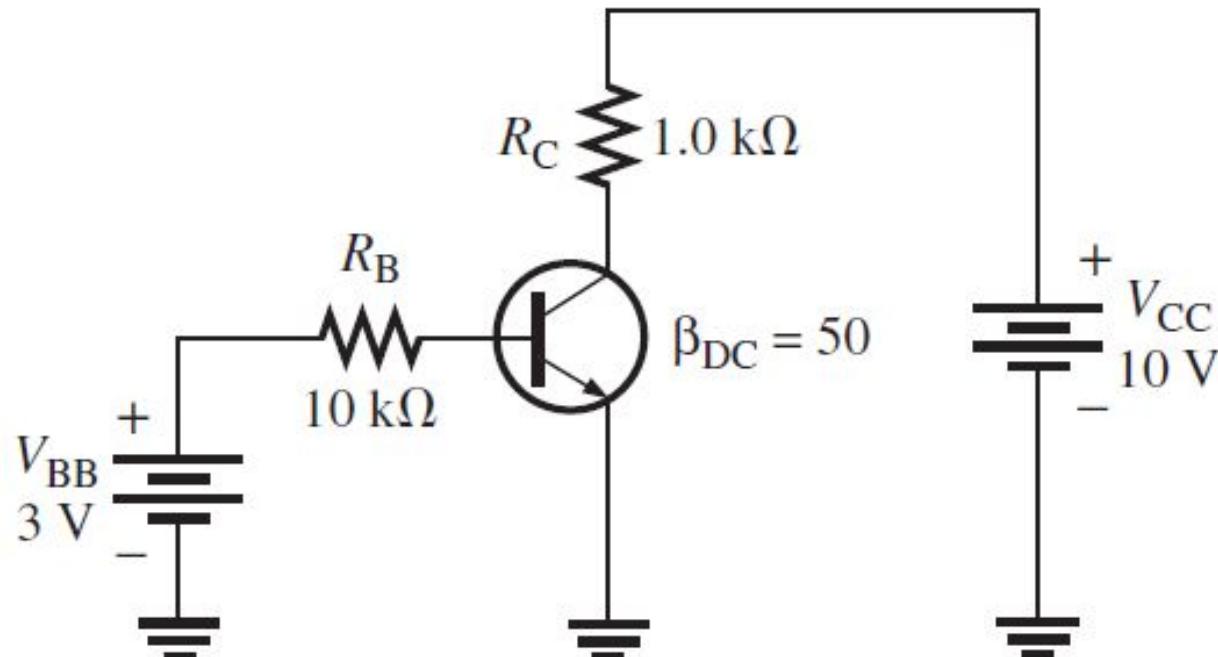
DC Load Line



- Cutoff and saturation can be illustrated in relation to the collector characteristic curves by the use of a load line.
- Figure shows a dc load line drawn on a family of curves connecting the cutoff point and the saturation point.
- The bottom of the load line is at ideal cutoff where $I_C = 0$ and $V_{CE} = V_{CC}$
- The top of the load line is at saturation where $I_C = I_{C(sat)}$ and $V_{CE} = V_{CE(sat)}$
- In between cutoff and saturation along the load line is the *active region* of the transistor's operation.

Numerical 2

Determine whether or not the transistor in Figure is in saturation.
Assume $V_{CE(sat)} = 0.2$ V.



Numerical 2 Solution

First, determine $I_{C(\text{sat})}$.

$$I_{C(\text{sat})} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_C} = \frac{10 \text{ V} - 0.2 \text{ V}}{1.0 \text{ k}\Omega} = \frac{9.8 \text{ V}}{1.0 \text{ k}\Omega} = 9.8 \text{ mA}$$

Now, see if I_B is large enough to produce $I_{C(\text{sat})}$.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{3 \text{ V} - 0.7 \text{ V}}{10 \text{ k}\Omega} = \frac{2.3 \text{ V}}{10 \text{ k}\Omega} = 0.23 \text{ mA}$$

$$I_C = \beta_{DC} I_B = (50)(0.23 \text{ mA}) = 11.5 \text{ mA}$$

This shows that with the specified β_{DC} , this base current is capable of producing an I_C greater than $I_{C(\text{sat})}$. Therefore, the **transistor is saturated**, and the collector current value of 11.5 mA is never reached. If you further increase I_B , the collector current remains at its saturation value of 9.8 mA.

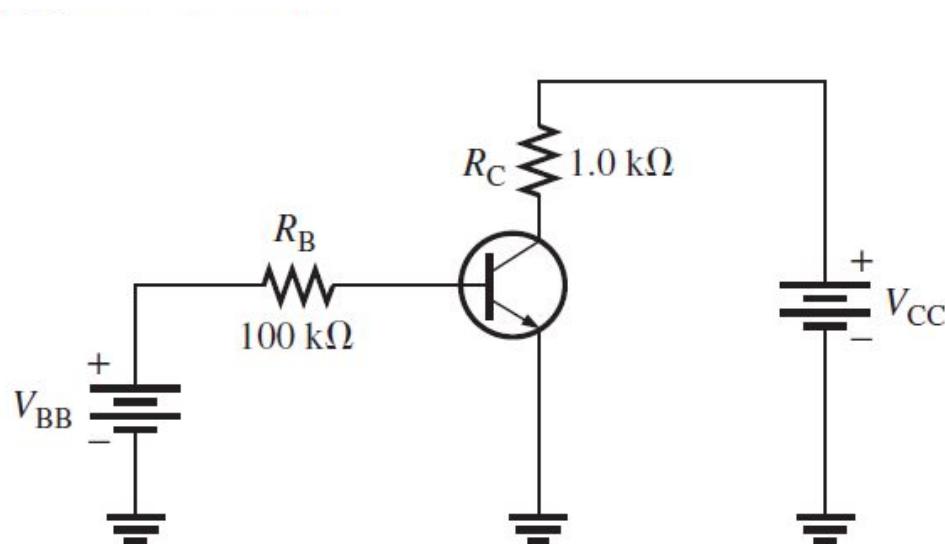
Homework problem

- Determine whether or not the transistor in Figure 4–16 is saturated for the following values:
 $\beta_{DC} = 125$, $V_{BB} = 1.5 \text{ V}$, $R_B = 6.8 \text{ kohms}$,
 $R_C = 180\text{ohms}$, and $V_{CC} = 12 \text{ V}$.

Answer: Transistor is not in saturation

Numerical 3

- A base current of $50 \mu\text{A}$ is applied to the transistor in Figure, and a voltage of 5 V is dropped across R_C . Determine the β_{DC} of the transistor.



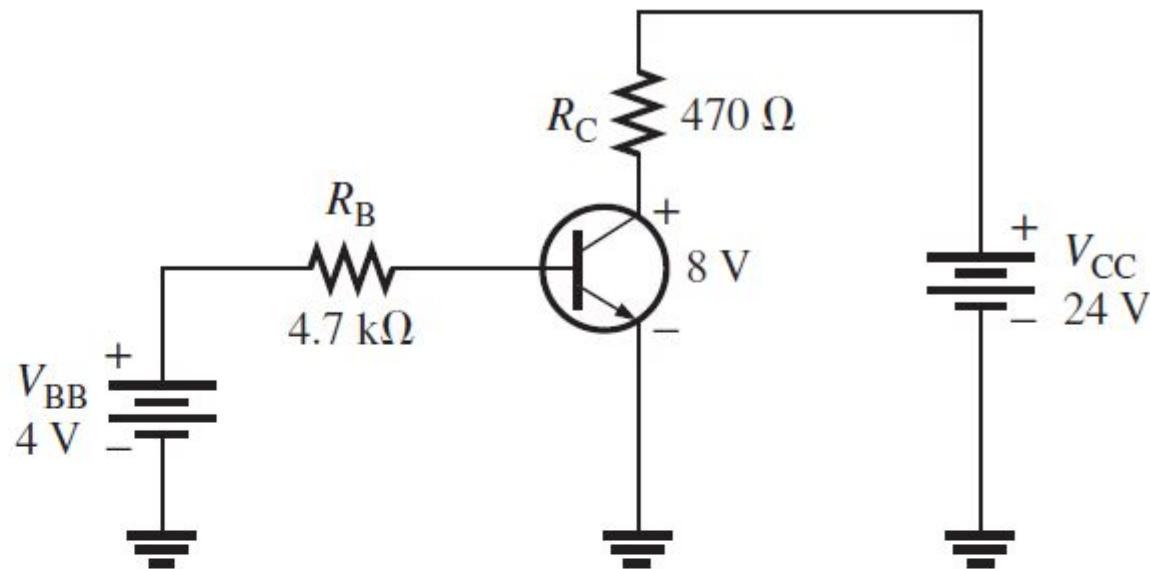
Numerical 3 Solution

$$\begin{aligned}I_c &= V_c / R_c \\&= 5V / 1 \text{ k}\Omega \\&= 5 \text{ mA}\end{aligned}$$

$$\begin{aligned}\beta_{DC} &= I_c / I_B \\&= 5 \text{ mA} / 50 \mu\text{A} \\&= 100\end{aligned}$$

Numerical 4

- Determine each current in Figure below. What is the β_{DC} ?



Numerical 4 Solution

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{4 - 0.7}{4.7 K\Omega} = 702 \mu A$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{24 - 8}{470 \Omega} = 34 mA$$

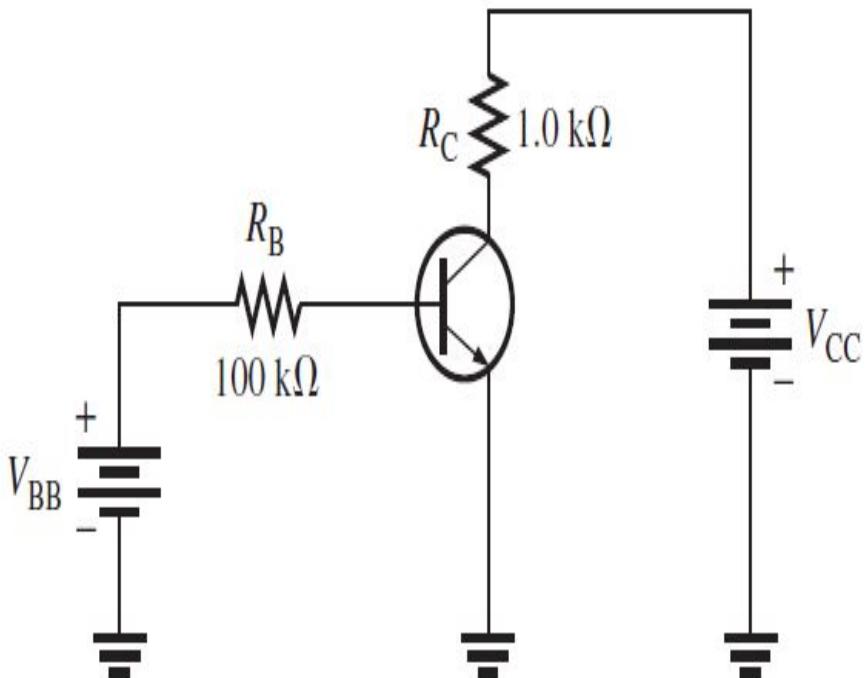
$$I_E = I_B + I_C = 702 \mu A + 34 mA = 34.7 mA$$

$$\beta_{DC} = \frac{I_C}{I_B} = 48.4$$

Numerical 5

- Assume that the transistor in the circuit below is having a β_{DC} of 200. Determine I_B , I_C , I_E , and V_{CE} given that $V_{CC} = 10$ V and $V_{BB} = 3$ V.

QUESTION



$$14. I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{3\text{ V} - 0.7\text{ V}}{100\text{ k}\Omega} = 23\text{ }\mu\text{A}$$

$$I_C = \beta_{DC} I_B = 200(23\text{ }\mu\text{A}) = 4.6\text{ mA}$$

$$I_E = I_C + I_B = 4.6\text{ mA} + 23\text{ }\mu\text{A} = 4.62\text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 10\text{ V} - (4.6\text{ mA})(1.0\text{ k}\Omega) = 5.4\text{ V}$$

Quiz 1

1. Name the two types of BJTs according to their structure.
2. The BJT is a three-terminal device. Name the three terminals.
3. What separates the three regions in a BJT?

Quiz 1

- The power gain of ----- configuration is the highest.

Ans - CE

- Voltage gain of -----configuration is unity.

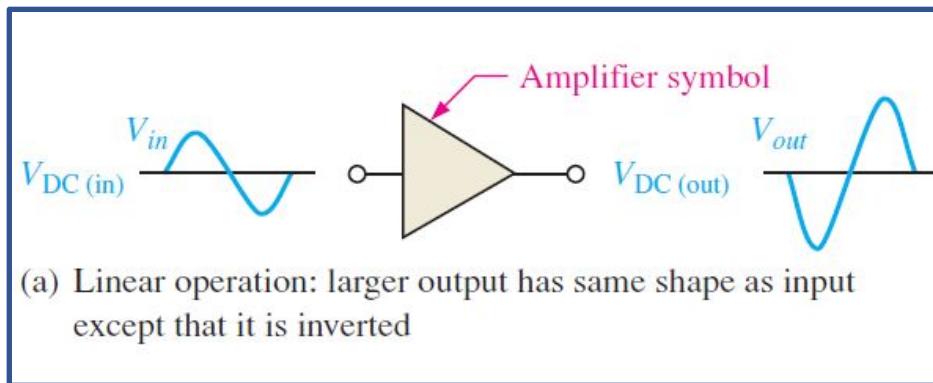
Ans - CC

- Current gain of -----configuration is low;

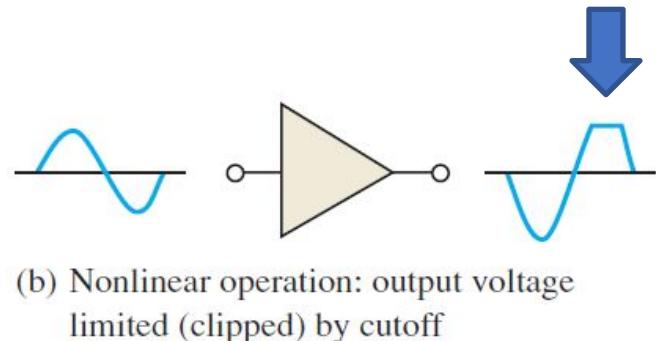
Ans - CB

DC Bias

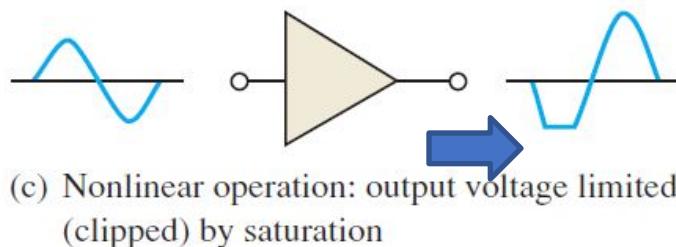
Bias establishes the dc operating point or **Q-point (Quiescent point)** for proper linear operation of an amplifier.



(a) Linear operation: larger output has same shape as input except that it is inverted



(b) Nonlinear operation: output voltage limited (clipped) by cutoff



(c) Nonlinear operation: output voltage limited (clipped) by saturation

FIGURE : Examples of linear and nonlinear operation of an inverting amplifier (the triangle symbol).

Quiescent point (Q point) or bias point or operating point of CE amplifier:

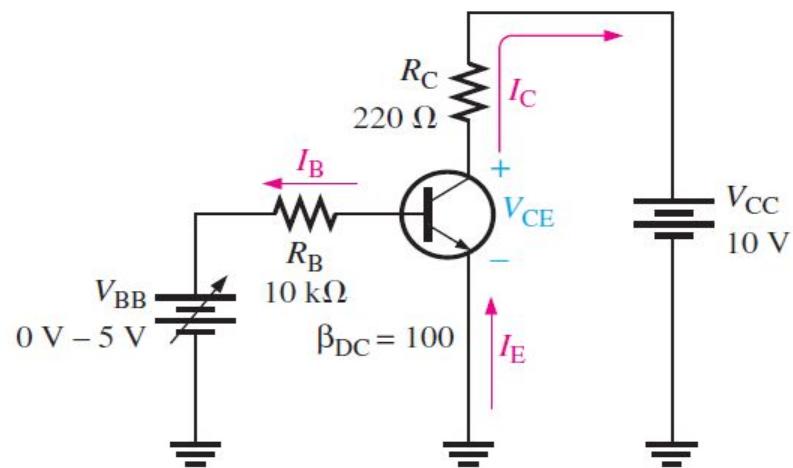
- It is the point on the load line which represents the dc current through a transistor (I_{CQ}) and the voltage across it (V_{CEQ}), when no ac signal is applied.
- The dc load line is a set of infinite number of such operating points.
- If the transistor is being used for “amplification” purpose, then Q point should be exactly at the center of load line.

Instability of Quiescent point

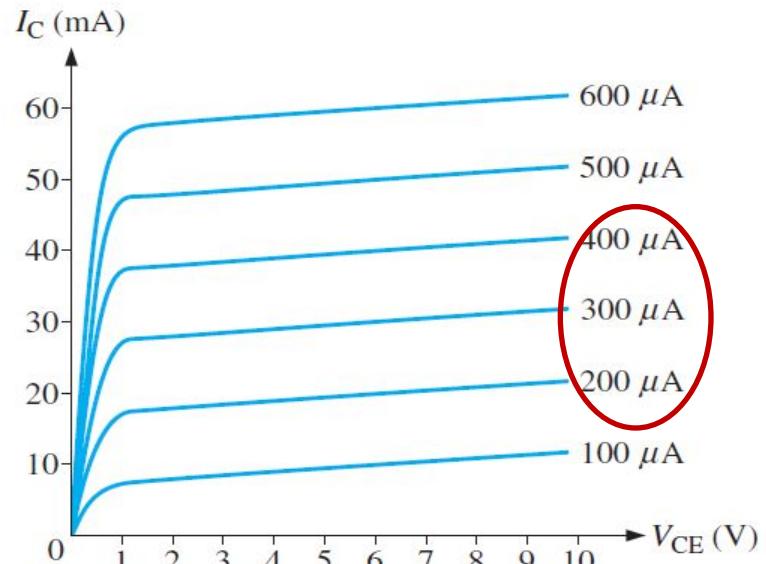
- Due to Temperature
- Due to gain β_{dc}
- Device to device variation
- The operating point of a transistor amplifier shifts mainly with changes in temperature, since the transistor parameters — β , I_{CO} and V_{BE} (*where the symbols carry their usual meaning*)—are functions of temperature.

DC Bias: Graphical Analysis

We assign three values to I_B and observe what happens to I_C and V_{CE} .



(a) DC biased circuit



(b) Collector characteristic curves

FIGURE : A dc-biased transistor circuit with variable bias voltage (V_{BB}) for generating the collector characteristic curves shown in part (b).

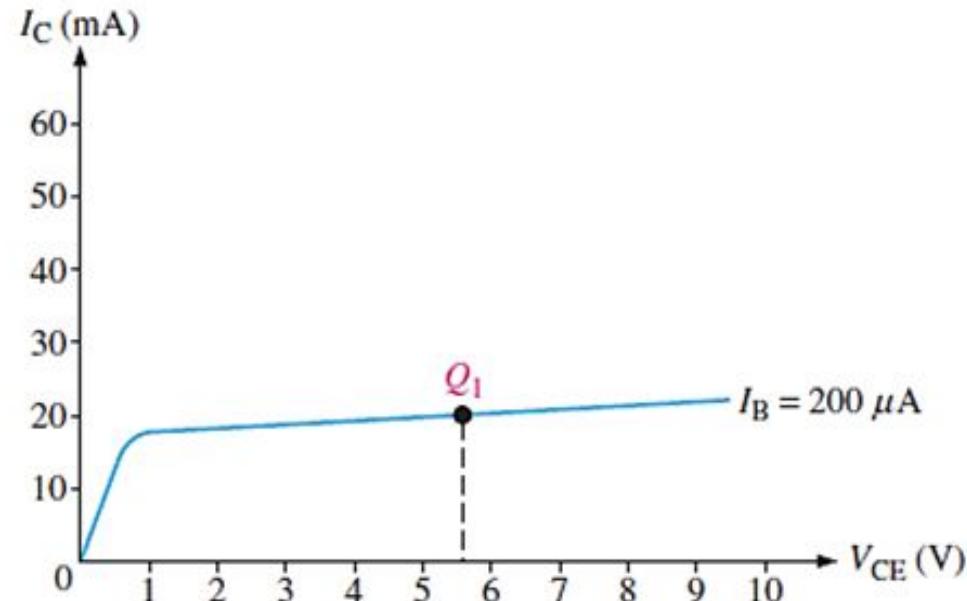
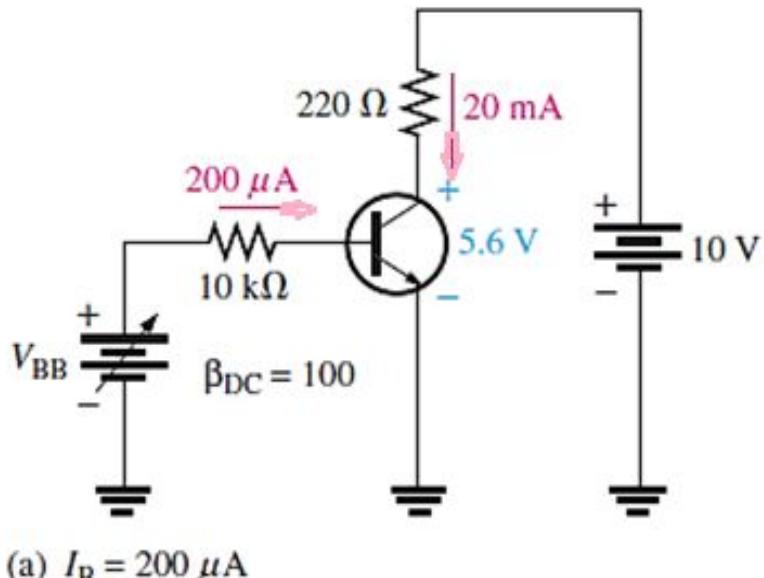
DC Bias: Graphical Analysis

First, V_{BB} is adjusted to produce an I_B of $200\mu A$.

Since $I_C = \beta_{DC} I_B$ the collector current is 20 mA, as indicated, and

$$V_{CE} = V_{CC} - I_C R_C = 10\text{ V} - (20\text{ mA})(220\Omega) = 10\text{ V} - 4.4\text{ V} = 5.6\text{ V}$$

This Q-point is shown on the graph as $Q1$.

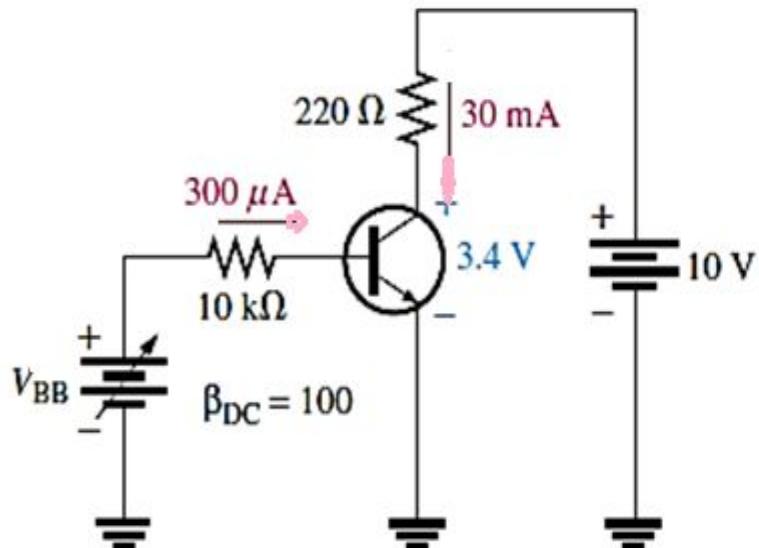


DC Bias: Graphical Analysis

Next, V_{BB} is increased to produce an I_B of $300\mu\text{A}$ and an I_C of 30 mA .

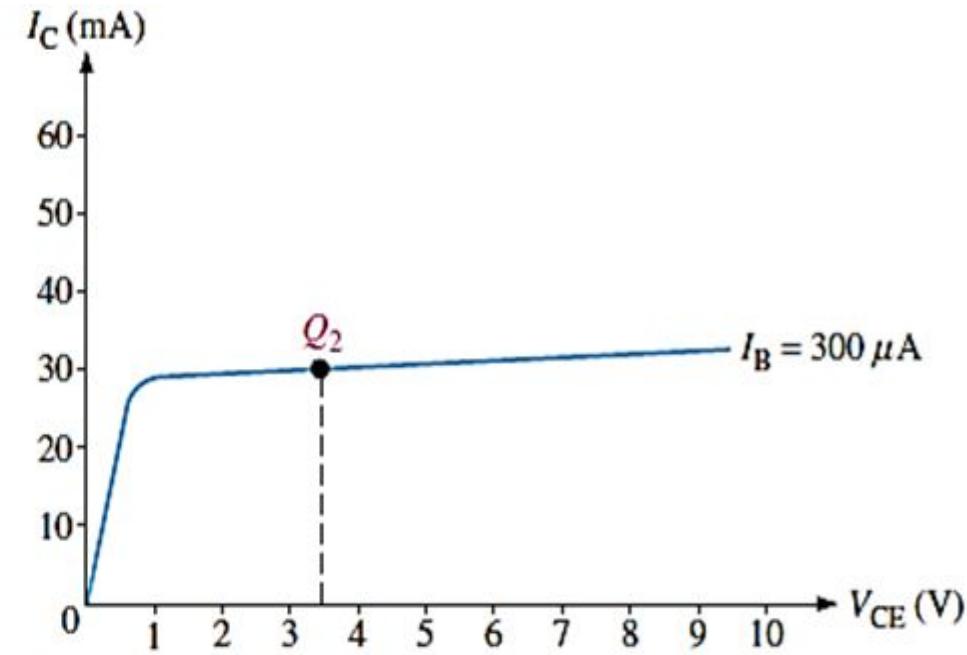
$$V_{CE} = 10\text{ V} - (30\text{ mA})(220\ \Omega) = 10\text{ V} - 6.6\text{ V} = 3.4\text{ V}$$

The Q-point for this condition is indicated by Q_2 on the graph.



(b) Increase I_B to $300\ \mu\text{A}$ by increasing V_{BB}

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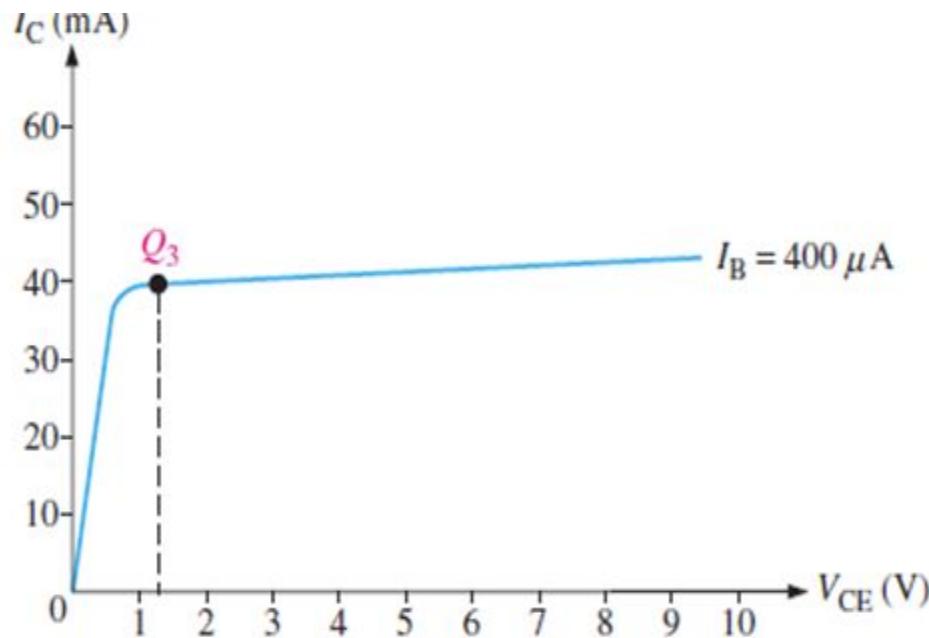
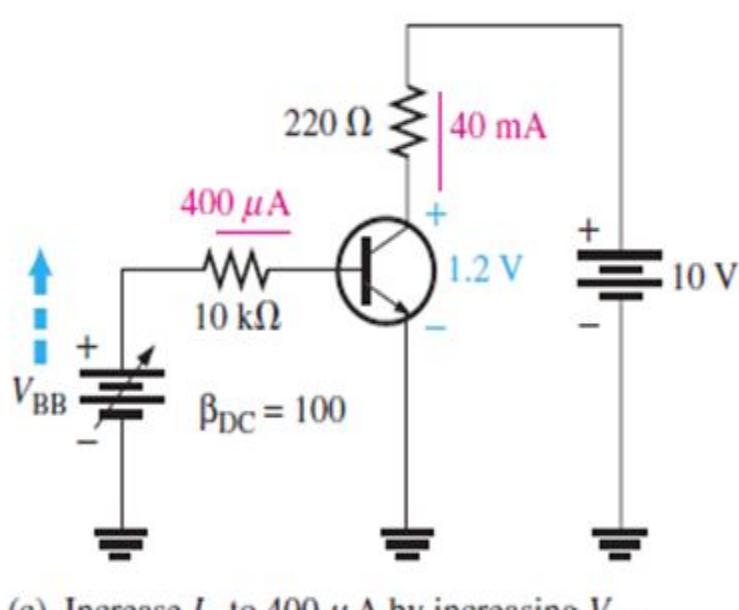
MITWPU

DC Bias: Graphical Analysis

Finally, V_{BB} is increased to give an I_B of $400\mu A$ and an I_C of 40 mA.

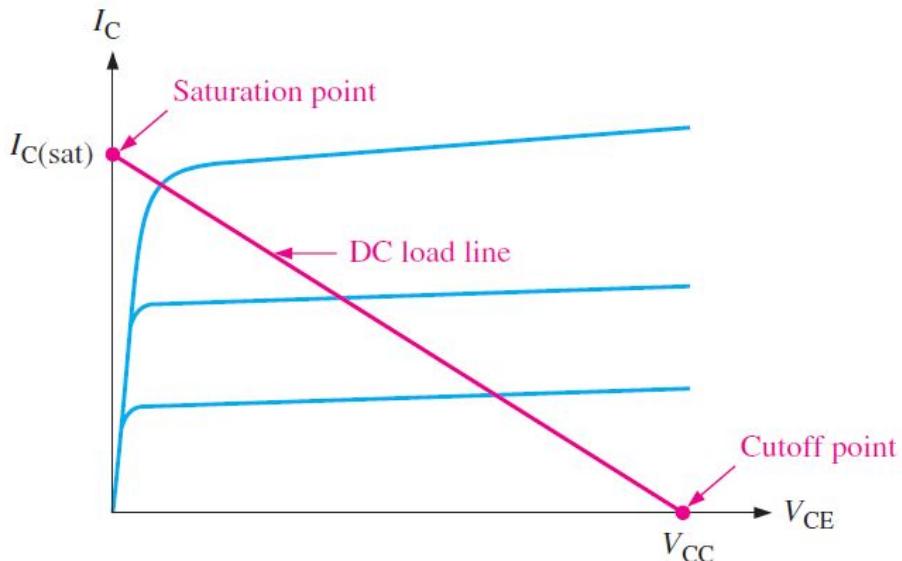
$$V_{CE} = 10 \text{ V} - (40 \text{ mA})(220 \Omega) = 10 \text{ V} - 8.8 \text{ V} = 1.2 \text{ V}$$

Q_3 is the corresponding Q-point on the graph.

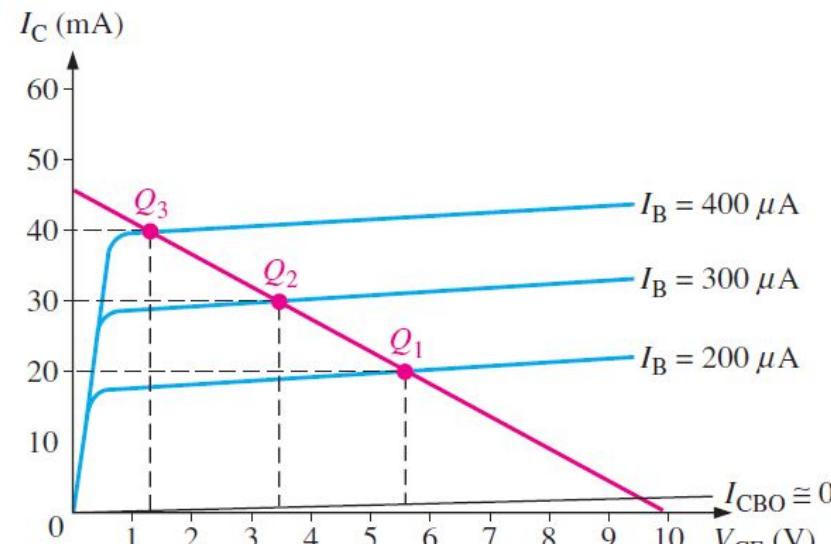


DC Bias: DC Load Line

- The dc operation of a transistor circuit can be described graphically using a **dc load line**.
- This is a straight line drawn on the characteristic curves from the saturation value where $I_C = I_{C(sat)}$ on the y -axis to the cutoff value where $V_{CE} = V_{CE(sat)}$ on the x -axis, as shown in Figure



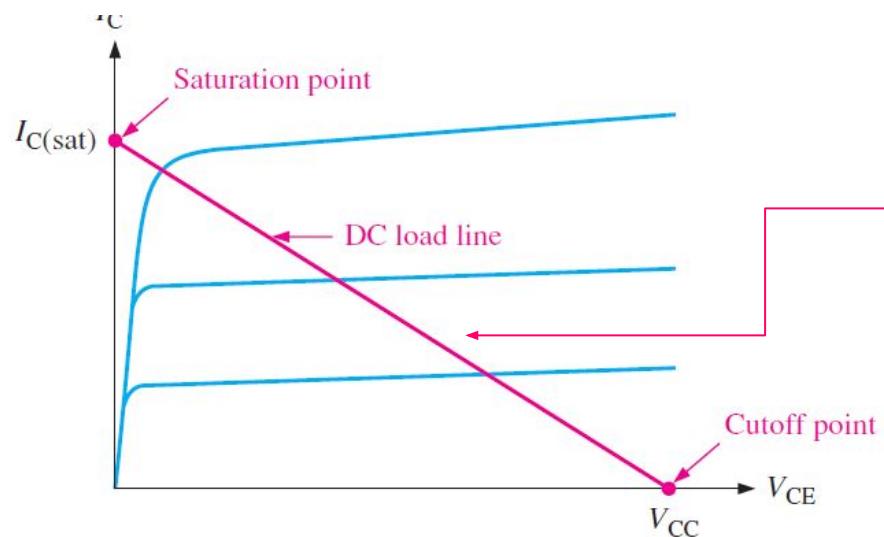
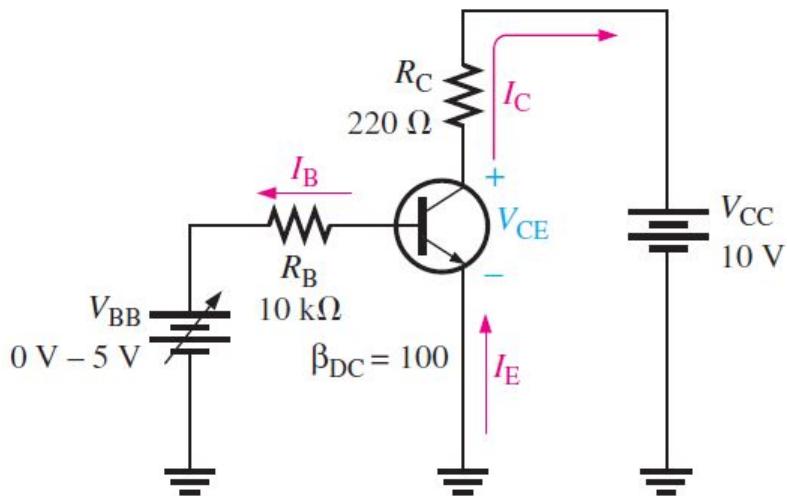
(a)



(b)

The point at which the load line intersects a characteristic curve represents the Q-point for that particular value of I_B .

DC Bias: DC Load Line



Apply KVL to collector circuit to write,

$$V_{CC} - V_{CE} - I_C R_C = 0$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} = -\frac{V_{CE}}{R_C} + \frac{V_{CC}}{R_C}$$

Rearranging this equation we get,

$$I_C = [-1 / R_C] V_{CE} + V_{CC} / R_C$$

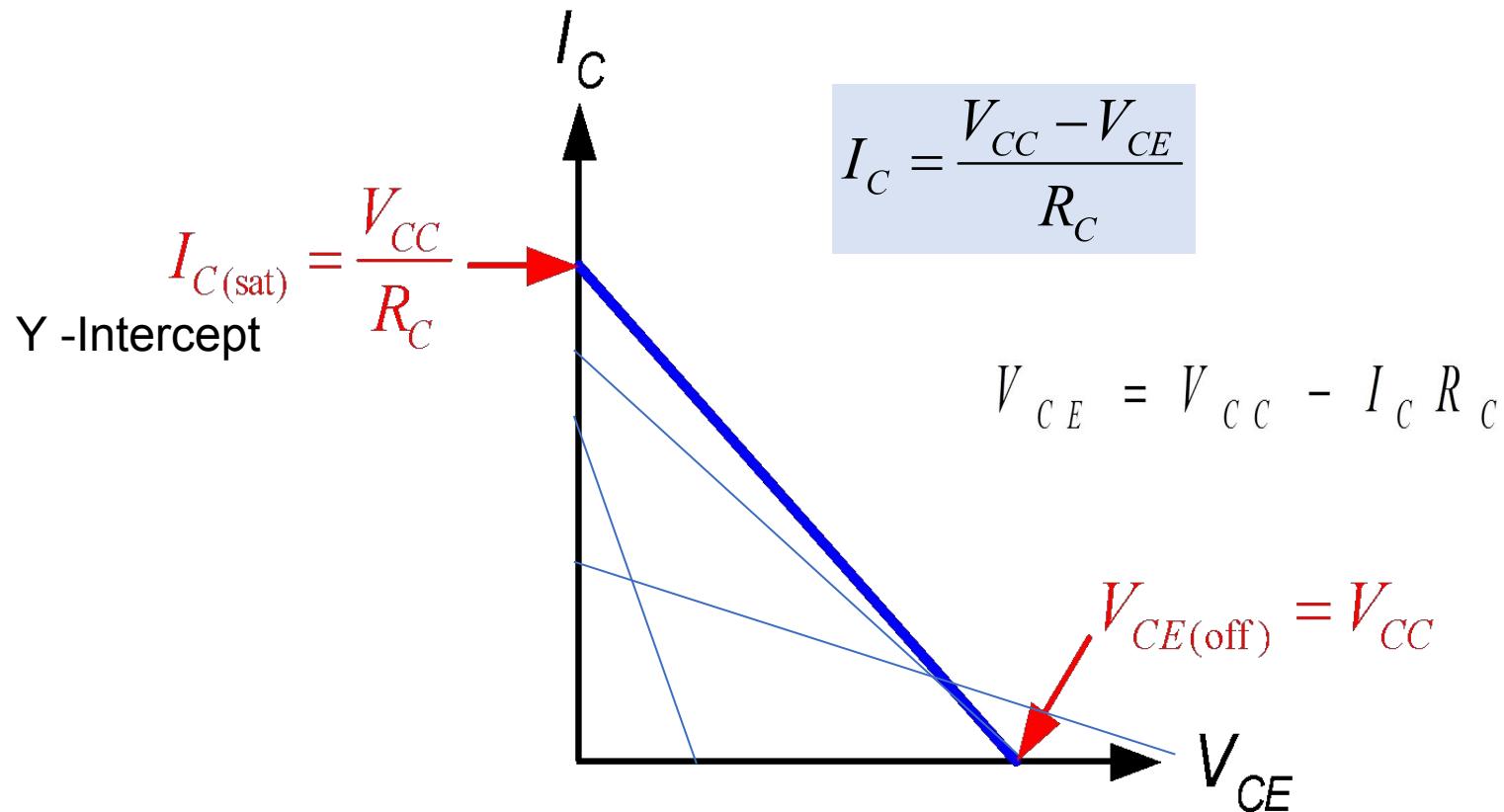
Compare this equation with the general equation of a straight line,

$$y = mx + C$$

From above equations

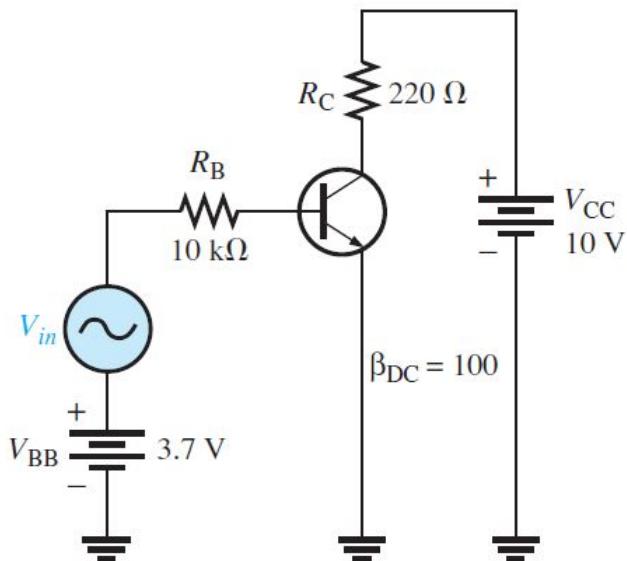
$$\begin{aligned} y &= I_C \\ x &= V_{CE} \\ \text{slope, } m &= -1 / R_C \\ C &= V_{CC} / R_C \end{aligned}$$

A generic dc load line



Linear Operation

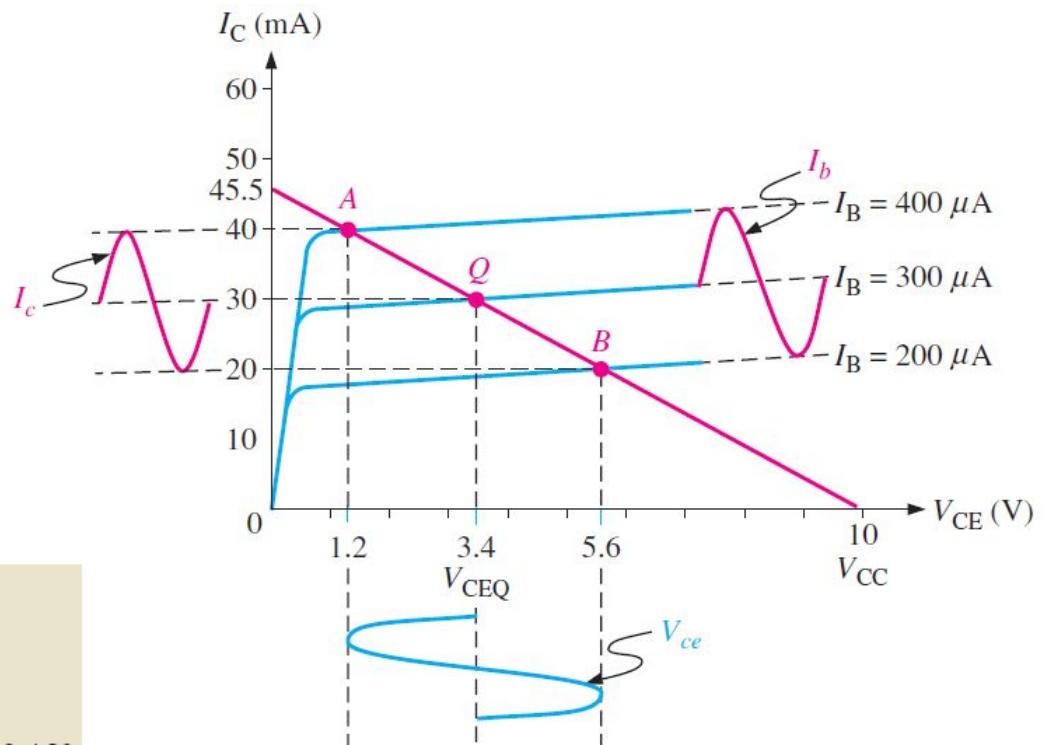
The region along the load line including all points between saturation and cutoff is generally known as the **linear region** of the transistor's operation.



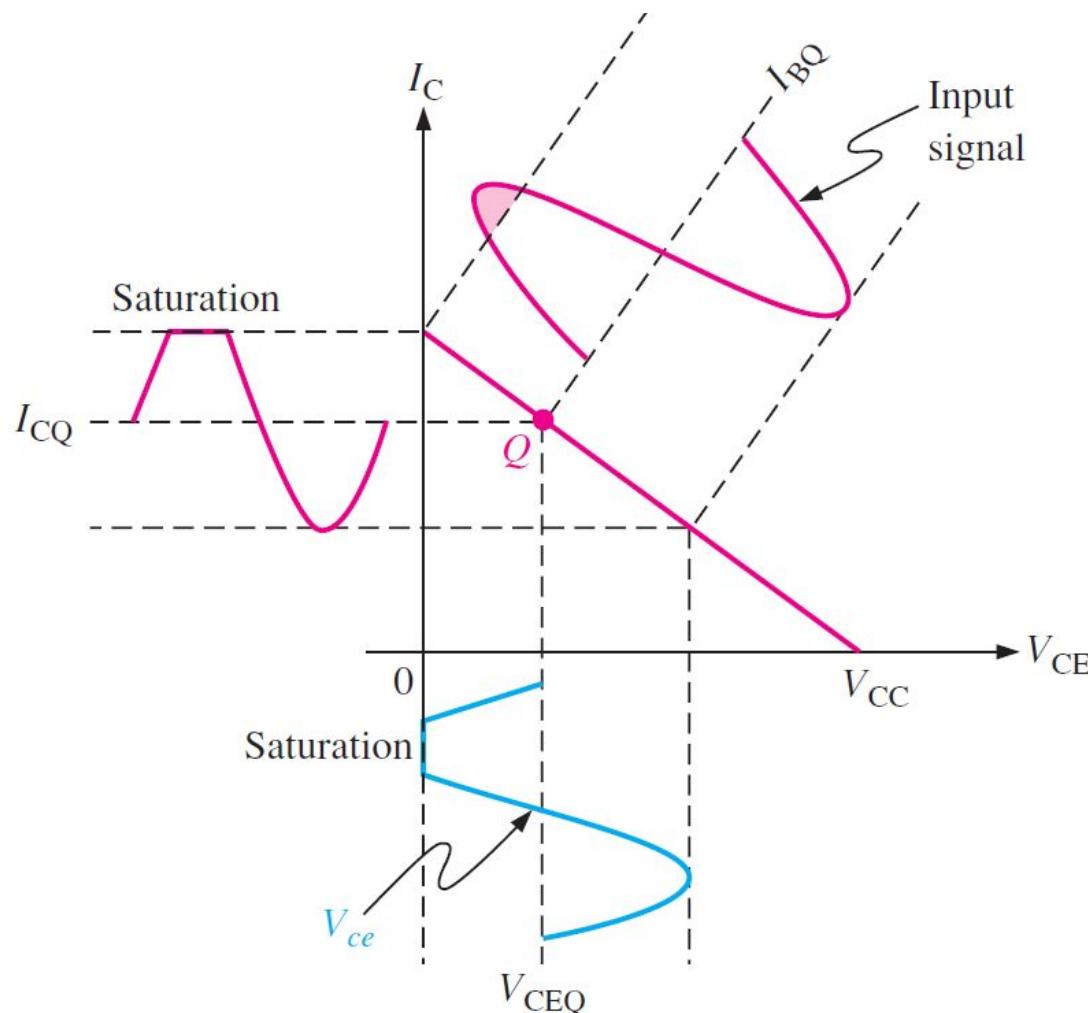
$$I_{BQ} = \frac{V_{BB} - 0.7 \text{ V}}{R_B} = \frac{3.7 \text{ V} - 0.7 \text{ V}}{10 \text{ k}\Omega} = 300 \mu\text{A}$$

$$I_{CQ} = \beta_{DC} I_{BQ} = (100)(300 \mu\text{A}) = 30 \text{ mA}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10 \text{ V} - (30 \text{ mA})(220 \Omega) = 3.4 \text{ V}$$

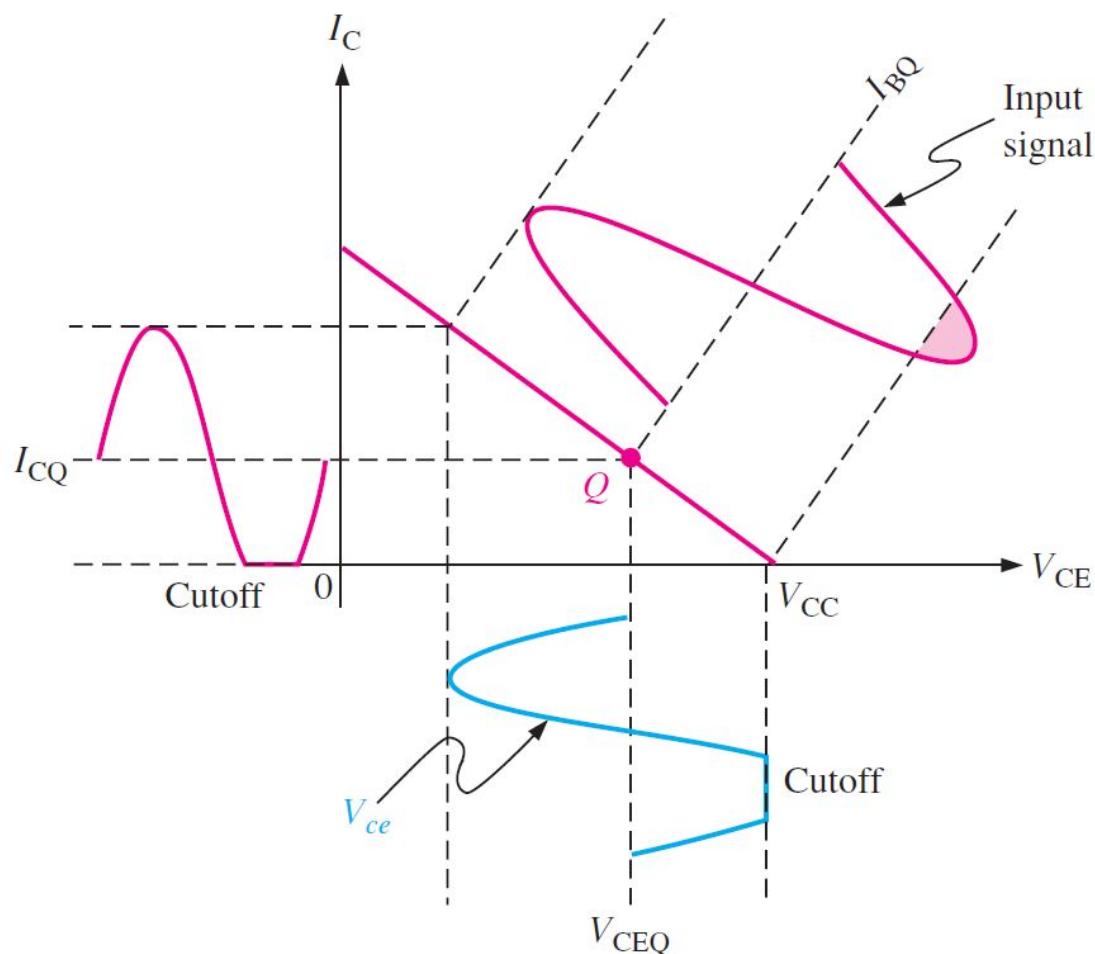


Waveform Distortion due to improper biasing



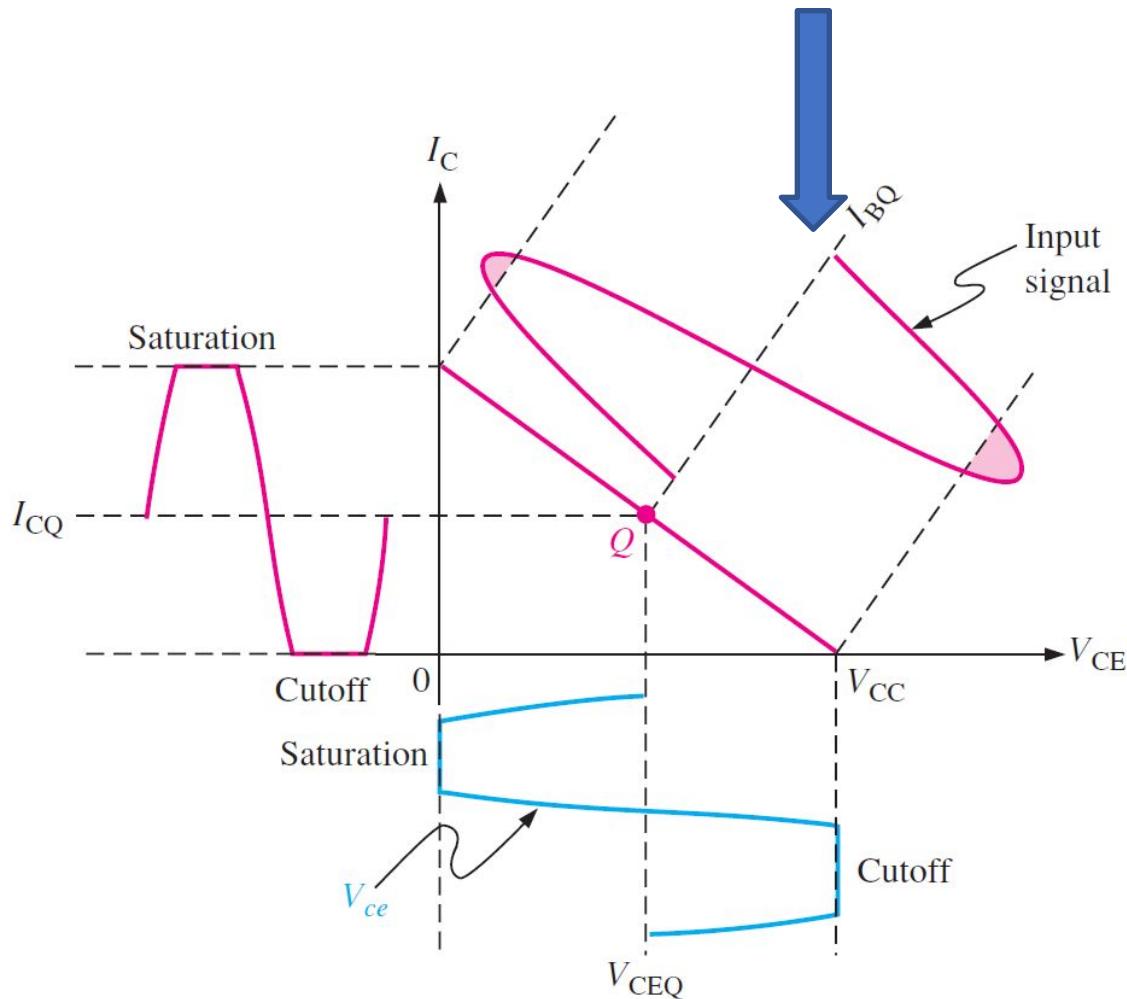
- (a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.

Waveform Distortion due to improper biasing



- (b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.

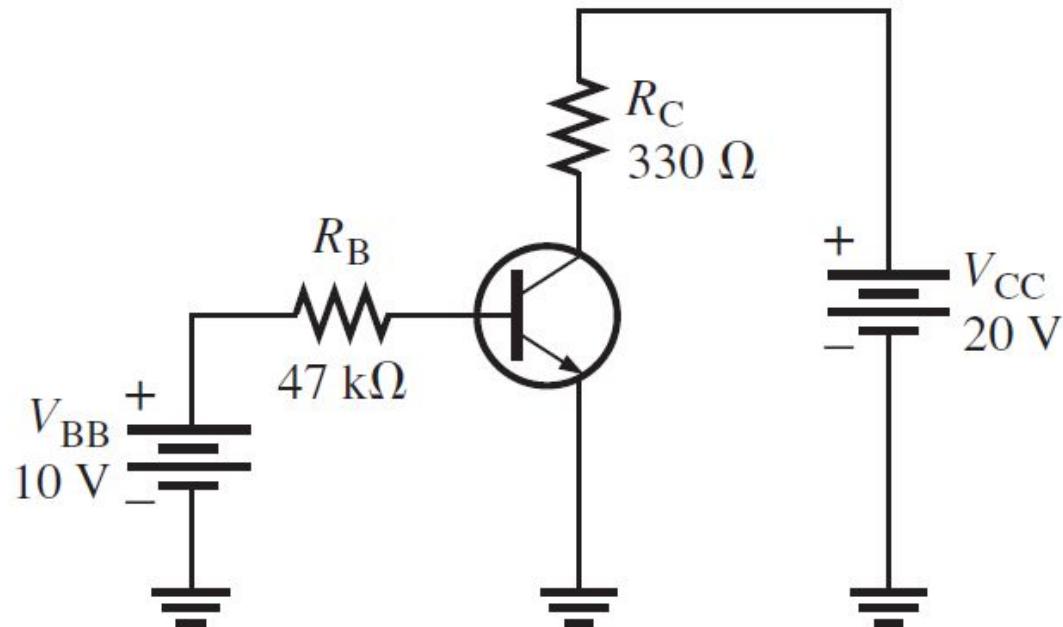
Waveform Distortion- Input signal too large



- (c) Transistor is driven into both saturation and cutoff because the input signal is too large.

Numerical 6

Determine the Q-point for the circuit in Figure below and draw the dc load line. Find the maximum peak value of base current for linear operation. Assume $\beta_{DC} = 100$.



Solution

The Q-point is defined by the values of I_C and V_{CE} .

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{47\text{ k}\Omega} = 198\text{ }\mu\text{A}$$

$$I_C = \beta_{DC} I_B = (200)(198\text{ }\mu\text{A}) = \mathbf{39.6\text{ mA}}$$

$$V_{CE} = V_{CC} - I_C R_C = 20\text{ V} - 13.07\text{ V} = \mathbf{6.93\text{ V}}$$

The Q-point is at $I_C = 39.6\text{ mA}$ and at $V_{CE} = 6.93\text{ V}$.

Since $I_{C(\text{cutoff})} = 0$, you need to know $I_{C(\text{sat})}$ to determine how much variation in collector current can occur and still maintain linear operation of the transistor.

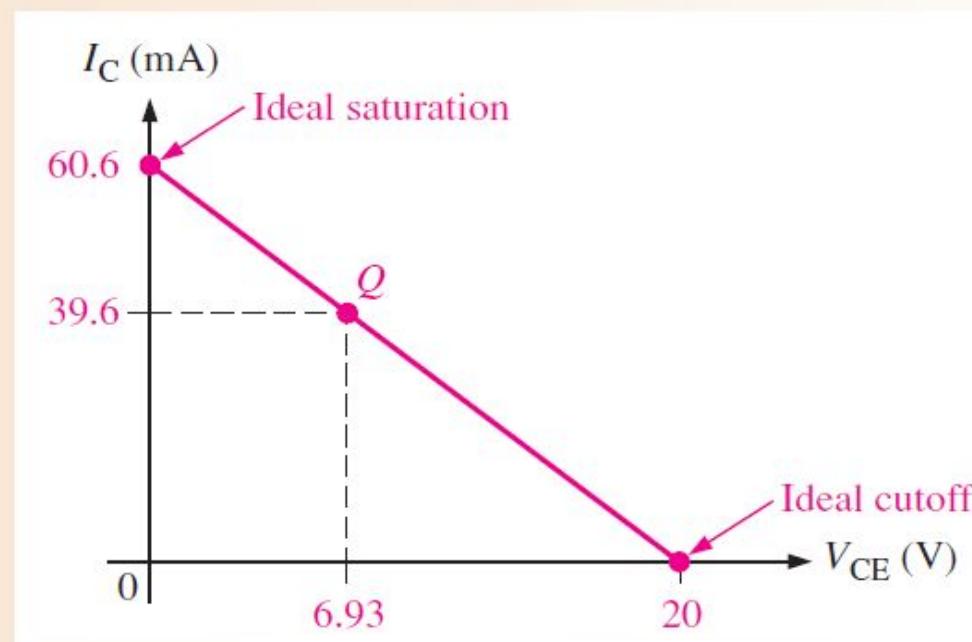
$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C} = \frac{20\text{ V}}{330\text{ }\Omega} = 60.6\text{ mA}$$

The dc load line is graphically illustrated in Figure 5–8, showing that before saturation is reached, I_C can increase an amount ideally equal to

$$I_{C(\text{sat})} - I_{CQ} = 60.6\text{ mA} - 39.6\text{ mA} = 21.0\text{ mA}$$

However, I_C can decrease by 39.6 mA before cutoff ($I_C = 0$) is reached. Therefore, the limiting excursion is 21 mA because the *Q-point is closer to saturation than to cutoff*. The 21 mA is the maximum peak variation of the collector current. Actually, it would be slightly less in practice because $V_{CE(sat)}$ is not quite zero.

► FIGURE 5–8



Determine the maximum peak variation of the base current as follows:

$$I_{b(peak)} = \frac{I_{c(peak)}}{\beta_{DC}} = \frac{21 \text{ mA}}{200} = \mathbf{105 \mu A}$$

Quiz 2

Question:

If a transistor operates at the middle of the dc load line, a decrease in the base current will move the Q point _____

- A. off the load line
- B. nowhere
- C. Up
- D. Down

Answer:D

Quiz 2

Question:

The end points of a DC load line drawn on a family of output curves determine _____

- A. saturation and cutoff
- B. the operating point
- C. the power curve
- D. the amplification factor

Answer: A

Quiz 2

Question 3

What are the upper and lower limits on a dc load line in terms of VCE and IC?

- 1 IC=0, VCE=0
- 2 IC=IC sat, VCE=0 and IC=0, VCE=VCC
- 3 IC=0, VCE=VCC and IC=IC sat, VCE=0
- 4 IC=0, VCE=VCC

DC Biasing and Q point

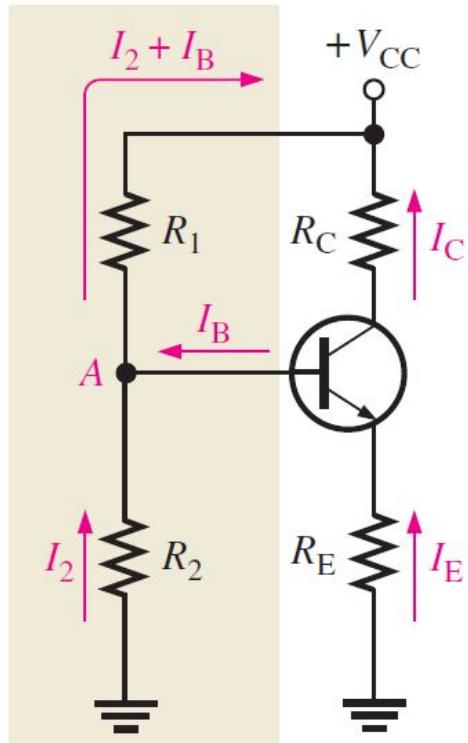
- Voltage-divider bias circuits

Voltage-divider bias is widely used because reasonably good bias stability is achieved with a single supply voltage.

- Base-bias circuits
- Emitter-bias circuits
- Collector-feedback bias circuits
- Emitter-feedback bias circuits

Voltage Divider Bias

- The resistor R_1 and R_2 form a potential divider to apply a fixed voltage V_B to the base.
- The resistor R_E is connected to the emitter.
- Voltage divider network biasing makes the transistor circuit independent of changes in beta (β).

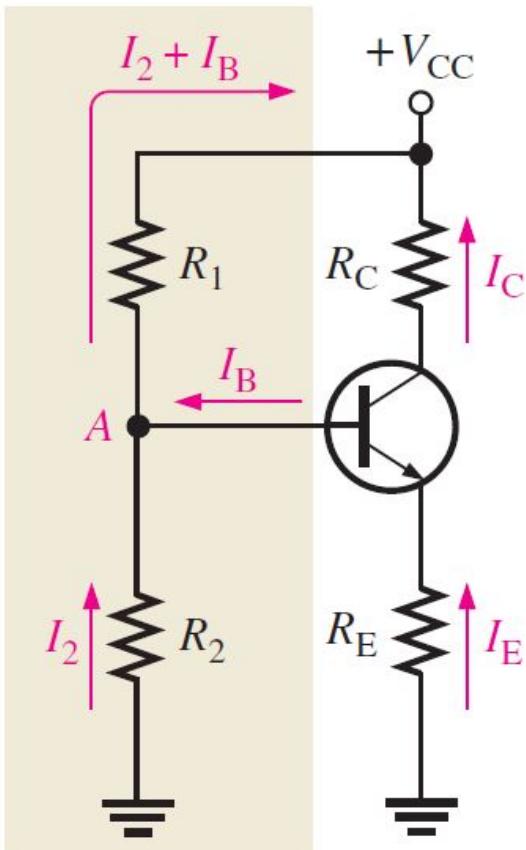


$$V_B \cong \left(\frac{R_2}{R_1 + R_2} \right) V_{CC}$$

Voltage Divider Bias

Once we know the base voltage, we can find the voltages and currents in the circuit, as follows:

$$V_E = V_B - V_{BE}$$



$$I_C \cong I_E = \frac{V_E}{R_E}$$

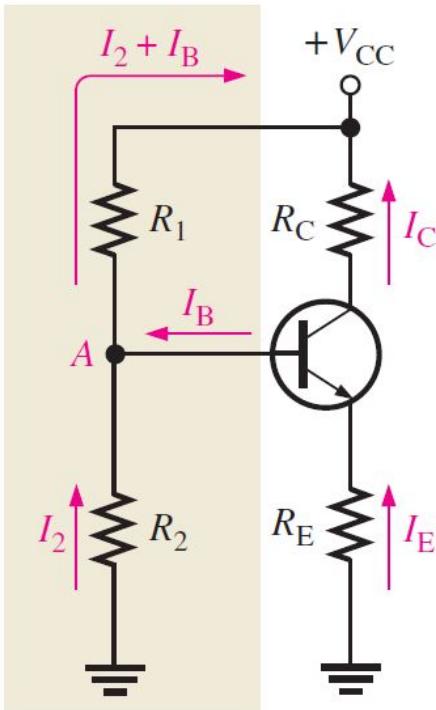
$$V_C = V_{CC} - I_C R_C$$

Once you know V_C and V_E , you can determine V_{CE} .

$$V_{CE} = V_C - V_E$$

Stabilization of Q point by voltage divider bias circuit:

If I_C increases due to change in temperature or β_{dc}



Then I_E increases

Hence drop across R_E increases ($V_E = I_E R_E$)

But V_B is constant. Hence V_{BE} decreases.

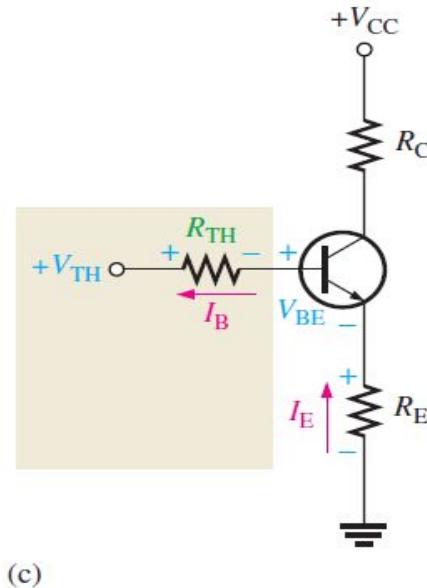
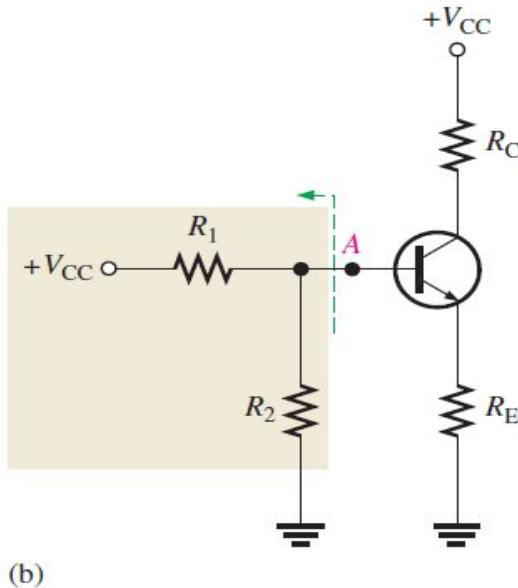
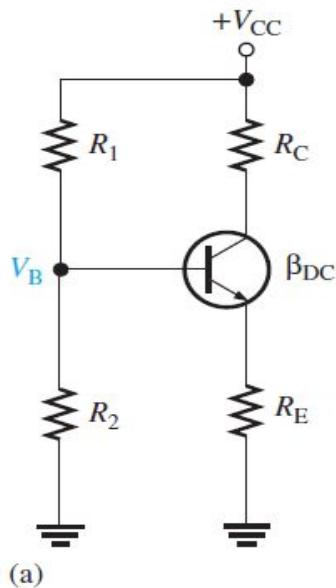
Hence I_B decreases.

Hence I_C also decreases. Thus compensation for increase in I_C is achieved.

Stabilization of Q point by voltage divider bias circuit

- This is the most commonly used arrangement for biasing as it provides good bias stability.
- The stability of the base bias network and therefore the Q-point is generally assessed by considering the collector current as a function of both Beta (β) and temperature.
- In this arrangement the emitter resistance ' R_E ' provides stabilization.
- The net forward bias across the emitter base junction is equal to V_B - dc voltage drop across ' R_E '.
- The base voltage is set by V_{cc} and R_1 and R_2 . The dc bias circuit is independent of transistor current gain.

Thevenin's Theorem Applied to Voltage-Divider Bias



$$V_{TH} = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

Thevenin's Theorem Applied to Voltage-Divider Bias

- Applying Kirchhoff's voltage law around the equivalent base-emitter loop gives

$$V_{TH} - V_{R_{TH}} - V_{BE} - V_{R_E} = 0$$

Substituting, using Ohm's law, and solving for V_{TH} ,

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

Substituting I_E/β_{DC} for I_B ,

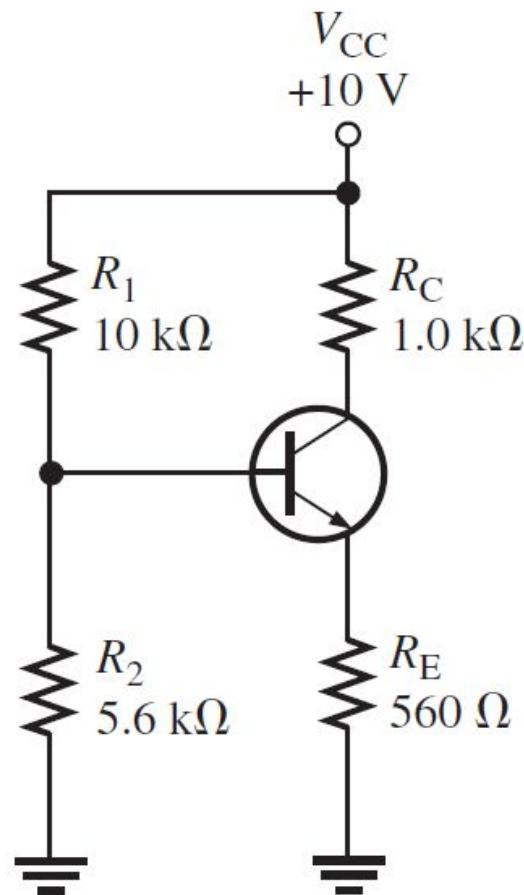
$$V_{TH} = I_E(R_E + R_{TH}/\beta_{DC}) + V_{BE}$$

Then solving for I_E ,

$$I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}$$

Numerical 1

Determine V_{CE} and I_C in the voltage-divider biased transistor circuit of Figure if $\beta_{DC} = 100$.



Solution The base voltage is

$$V_B \cong \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} = \left(\frac{5.6 \text{ k}\Omega}{15.6 \text{ k}\Omega} \right) 10 \text{ V} = 3.59 \text{ V}$$

So,

$$V_E = V_B - V_{BE} = 3.59 \text{ V} - 0.7 \text{ V} = 2.89 \text{ V}$$

and

$$I_E = \frac{V_E}{R_E} = \frac{2.89 \text{ V}}{560 \text{ }\Omega} = 5.16 \text{ mA}$$

Therefore,

$$I_C \cong I_E = \mathbf{5.16 \text{ mA}}$$

and

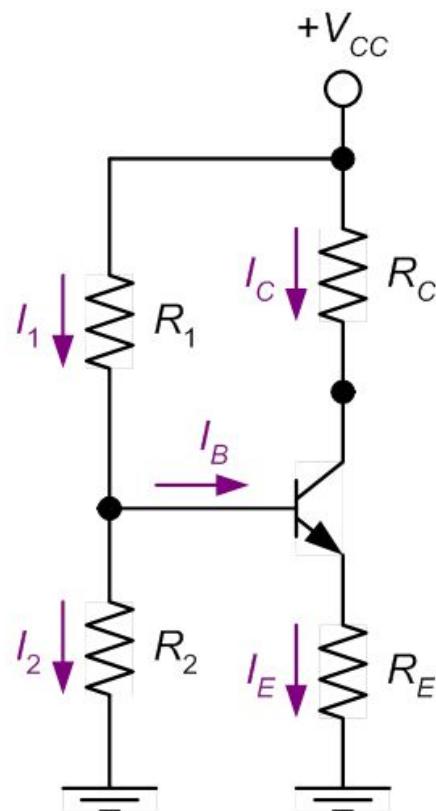
$$V_C = V_{CC} - I_C R_C = 10 \text{ V} - (5.16 \text{ mA})(1.0 \text{ k}\Omega) = 4.84 \text{ V}$$

$$V_{CE} = V_C - V_E = 4.84 \text{ V} - 2.89 \text{ V} = \mathbf{1.95 \text{ V}}$$

Numerical 2

A silicon transistor connected in common emitter configuration with voltage divider bias is shown in figure.

If $V_{CC}=22.5V$, $R_C= 5.6K\Omega$, $R_1=90 K\Omega$, $R_2= 10 K\Omega$, $R_E= 1 K\Omega$ and $\beta=55$.
Find Q point.



$$V_B = 22.5 \times (10/100) = 2.25V$$

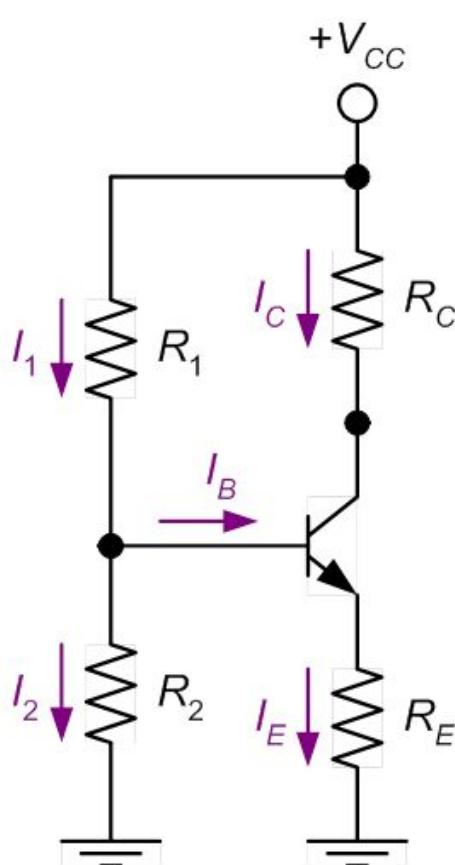
$$V_E = 2.25 - 0.7 = 1.55V$$

$$I_{CQ} = I_E = 1.55/1000 = 1.55 \text{ mA}$$

$$V_C = 22.5 - 5.6 \times 10^3 \times 1.55 \times 10^{-3} \\ = 13.82 \text{ V}$$

$$V_{CEQ} = V_C - V_E = 12.27 \text{ V}$$

Therefore Q point is:

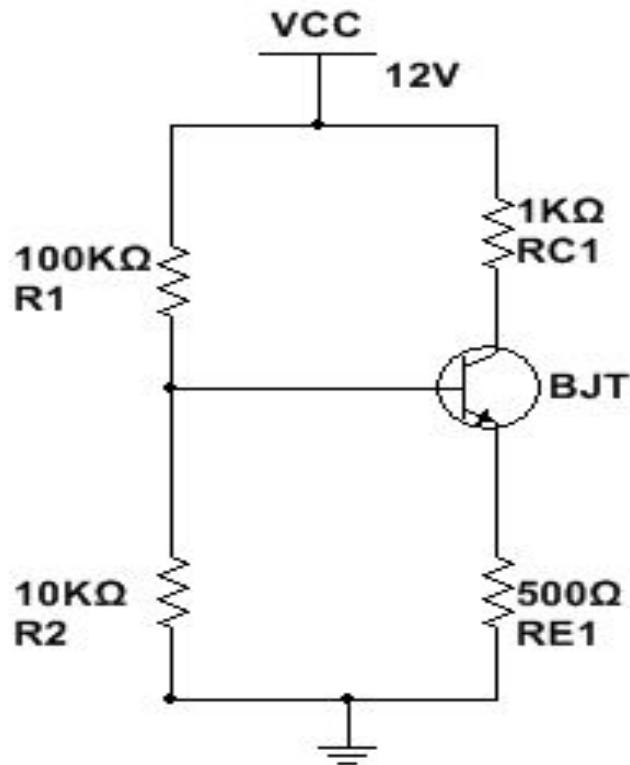


$$I_{CQ} = I_E = 1.55 \text{ mA}$$

$$V_{CEQ} = 12.27 \text{ V}$$

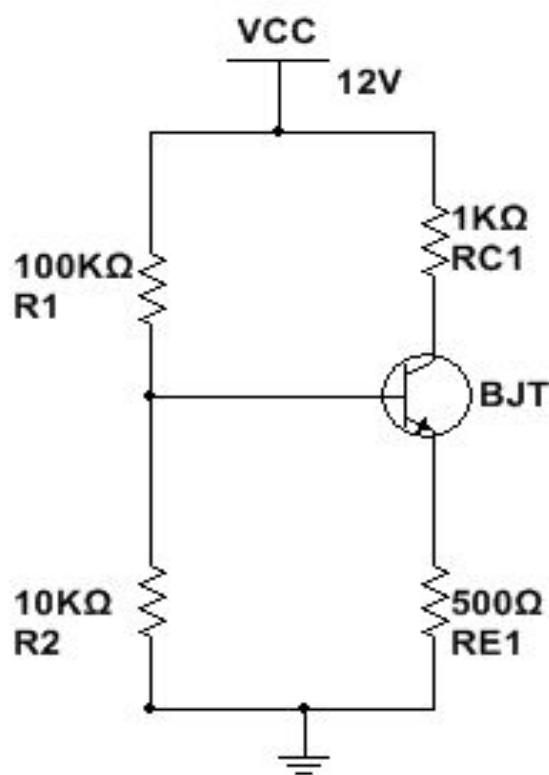
Numerical 3

Analyze the following circuit to find out D.C. parameters I_{CQ} , V_{CEQ} ,
Assume $V_{BE} = 0.6V$.



$$V_B = 12 \times (10/110) = 1.09 \text{ V}$$

$$V_E = 1.09 - 0.6 = 0.49 \text{ V}$$



$$I_{CQ} = I_E = 0.49 / 500 = 0.98 \text{ mA}$$

$$\begin{aligned} V_C &= 12 - 1 \times 10^3 \times 0.98 \times 10^{-3} \\ &= 11.02 \text{ V} \end{aligned}$$

$$V_{CEQ} = V_C - V_E = 10.53 \text{ V}$$

Therefore Q point is:

$$I_{CQ} = I_E = 0.98 \text{ mA}$$

$$V_{CEQ} = 10.53 \text{ V}$$

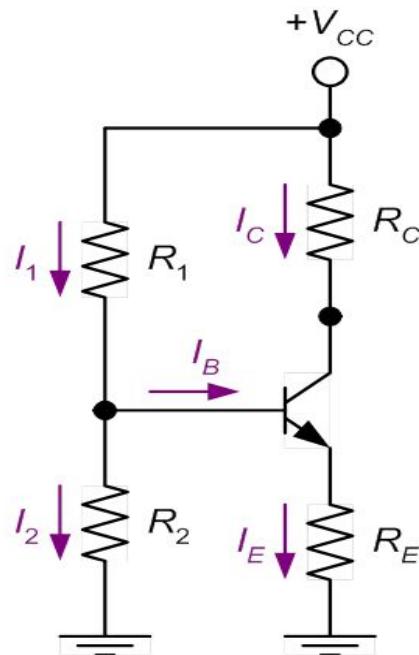
Numerical 4

A silicon transistor connected in common emitter configuration with self bias is shown in figure.

$$V_{CC} = 16V, R_C = 1.5K\Omega, \beta = 55$$

The quiescent point is chosen to be $V_{CE} = 8V, I_C = 4mA$.

Find R_1, R_2, R_E .



$$8 = 16 - 4\text{mA} \times (1.5\text{K} + R_E)$$

Use $V_{CE} = V_{CC} - I_C(R_E + R_C)$

$$R_E = 0.5\text{K} = 500\Omega$$

$$V_E = 0.5\text{K} \times 4\text{mA} = 2\text{V}$$

$$V_B = V_E + V_{BE} = 2.7\text{V}$$

$$V_B = (R_2 / (R_1 + R_2)) \times V_{CC}$$



Let $R_2 = 1\text{K}$

Assumed value

So $R_1 = 4.92\text{K}$

Nearest standard value for $R_1: 5.1\text{K}$

Transistor as an Amplifier

- One of the primary uses of a transistor is to amplify ac signals.
- DC load line -Active region operation
- This could be an audio signal (upto 20 KHz) or perhaps some high frequency radio (MHz-GHz) signal.
- No distortion in the amplified output

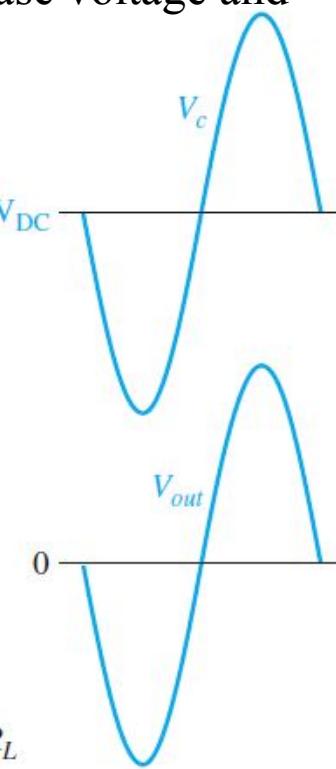
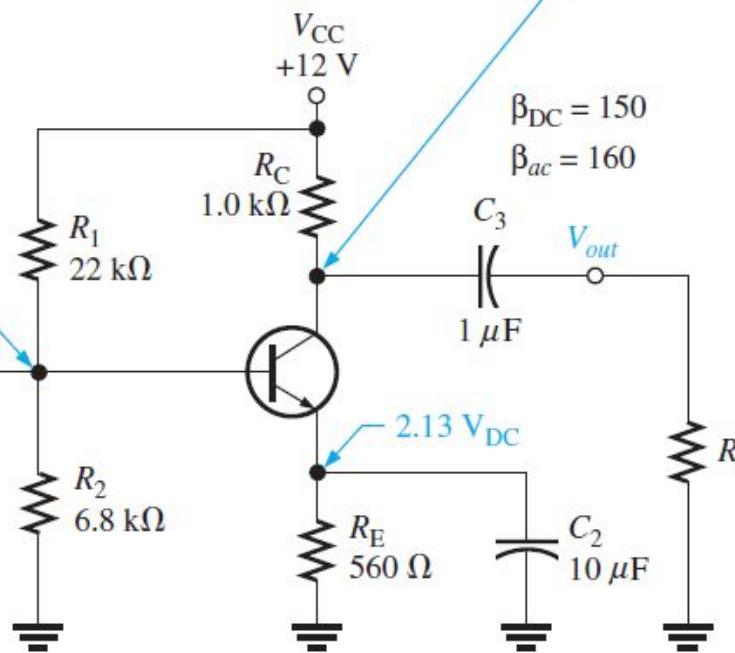
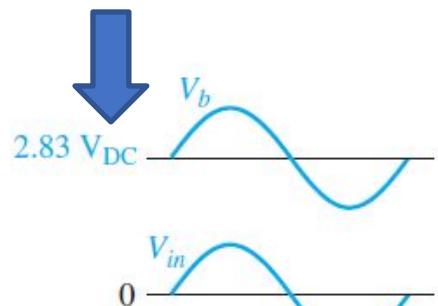
The Common-Emitter Amplifier

- The region between cutoff and saturation is called the **linear region**.
- A transistor which operates in the linear region is called a linear amplifier.
- Only the ac component reaches the load because of the capacitive coupling and that the output is 180° out of phase with input.
- CE amplifiers exhibit high voltage gain and high current gain and hence power gain.

The Common-Emitter Amplifier

- A linear amplifier provides amplification of a signal without any distortion so that the output signal is an exact amplified replica of the input signal.
- A transistor always produces a **phase inversion** between the base voltage and the collector voltage

$$(6.8/22+6.8)12=2.83V$$



CE amplifier Circuit Components and their Functions:

1. Resistors:

- Resistors R_1 , R_2 and R_E are used to bias the transistor in active region by using voltage divider bias circuit.
- R_C is collector resistor used to control collector current.

2. Input coupling capacitor C_I :

- The input coupling capacitor C_1 is used to couple the ac input voltage V_S to the base of the transistor.
- As capacitor block dc voltage , C_1 couples only the ac component of the input signal.
- This capacitor also ensures that the dc biasing conditions of transistor remain unchanged even after applications of the input signal.

3. *Bypass capacitor C_E :*

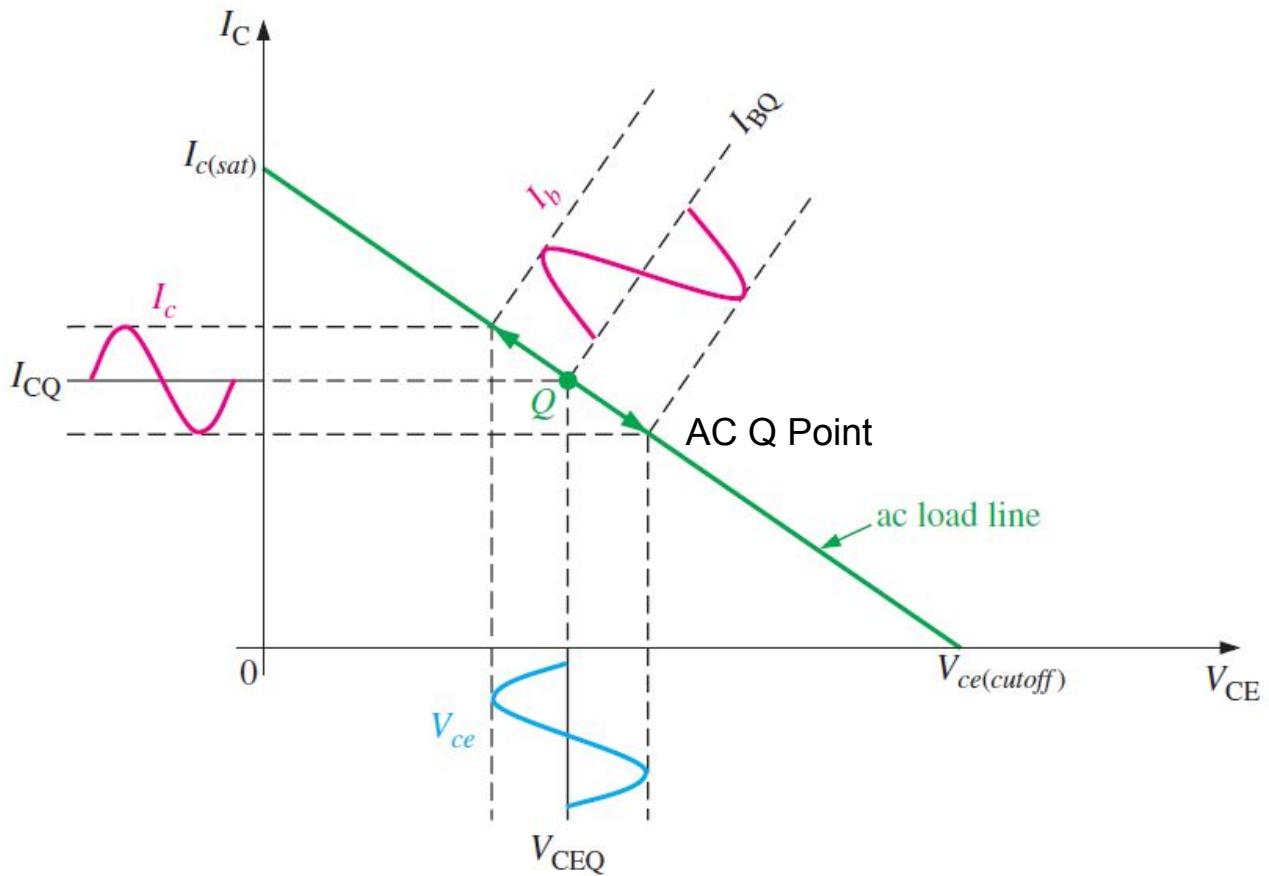
- As C_E is connected in parallel with R_E is called emitter bypass capacitor C_E .
- This capacitor offer a low reactance to the amplified ac signal, therefore R_E gets bypassed through C_E for only the ac signals.
- This will increase the voltage gain of the amplifier.

4. *Output coupling capacitor C_2 :*

- This capacitor couples the amplifier output to the load or to the next stage amplifier.
- It is used for blocking the dc part and passing only the ac part of the amplified signal to the load.

Phase Inversion in CE amplifier

Phase Inversion The output signal is 180° out of phase with the input signal. As the input signal voltage changes, it causes the ac base current to change, resulting in a change in the collector current from its Q-point value. If the base current increases, the collector current increases above its Q-point value, causing an increase in the voltage drop across R_C . This increase in the voltage across R_C means that the voltage at the collector decreases from its Q-point. So, any change in input signal voltage results in an opposite change in collector signal voltage, which is a phase inversion.



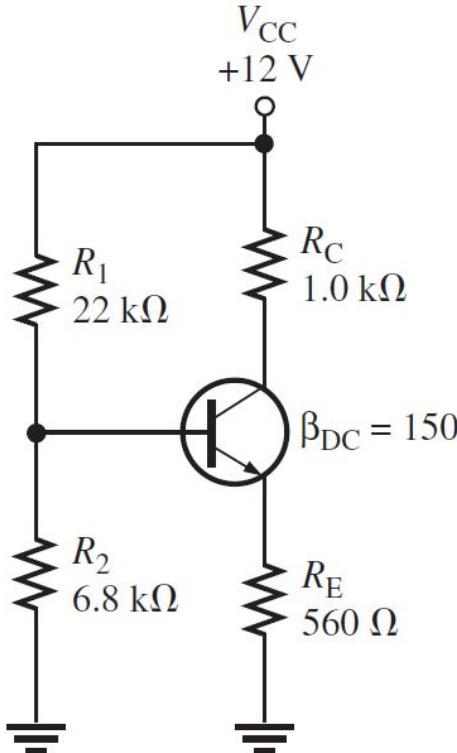
Graphical ac load line operation of the amplifier showing the variation of the base current, collector current, and collector-to-emitter voltage about their dc Q-point values. I_b and I_c are on different scales.

The Common-Emitter Amplifier

- Common-emitter amplifier with voltage-divider bias and coupling capacitors C_1 and C_3 on the input and output and a bypass capacitor, C_2 , from emitter to ground.
- The input signal, V_{in} , is capacitively coupled to the base terminal, the output signal, V_{out} , is capacitively coupled from the collector to the load.
- The amplified output is 180° out of phase with the input.
- Because the ac signal is applied to the base terminal as the input and taken from the collector terminal as the output, the emitter is common to both the input and output signals.
- There is no AC signal at the emitter because the bypass capacitor effectively shorts the emitter to ground at the signal frequency.
- All amplifiers have a combination of both ac and dc operation, which must be considered, but the common-emitter amplifier designation refers to the ac operation.

DC Analysis

- To analyze the amplifier, the dc bias values must first be determined.
- To do this, a dc equivalent circuit is developed by removing the coupling and bypass capacitors because they appear open as far as the dc bias is concerned.
- This also removes the load resistor and signal source. The dc equivalent circuit is shown in Figure below



$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = \frac{(6.8 \text{ k}\Omega)(22 \text{ k}\Omega)}{6.8 \text{ k}\Omega + 22 \text{ k}\Omega} = 5.19 \text{ k}\Omega$$

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} = \left(\frac{6.8 \text{ k}\Omega}{6.8 \text{ k}\Omega + 22 \text{ k}\Omega} \right) 12 \text{ V} = 2.83 \text{ V}$$

$$I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}} = \frac{2.83 \text{ V} - 0.7 \text{ V}}{560 \Omega + 34.6 \Omega} = 3.58 \text{ mA}$$

$$I_C \approx I_E = 3.58 \text{ mA}$$

$$V_E = I_E R_E = (3.58 \text{ mA})(560 \Omega) = 2 \text{ V}$$

$$V_B = V_E + 0.7 \text{ V} = 2.7 \text{ V}$$

$$V_C = V_{CC} - I_C R_C = 12 \text{ V} - (3.58 \text{ mA})(1.0 \text{ k}\Omega) = 8.42 \text{ V}$$

$$V_{CE} = V_C - V_E = 8.42 \text{ V} - 2 \text{ V} = 6.42 \text{ V}$$

AC Analysis of CE amplifier

To analyze the ac signal operation of an amplifier, an ac equivalent circuit is developed as follows:

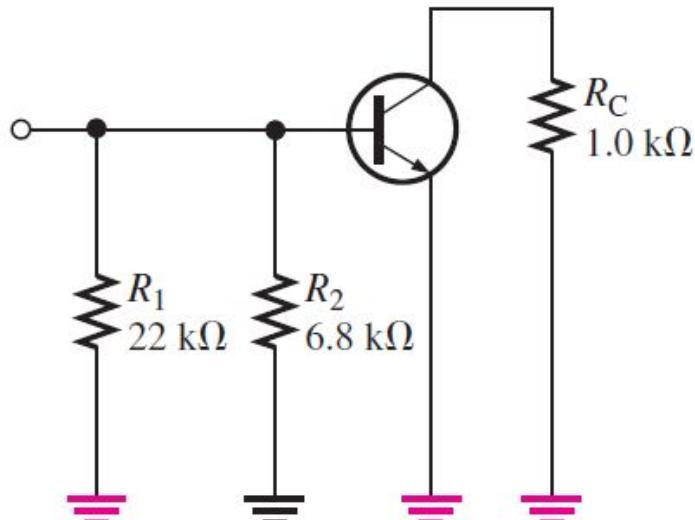
1. The capacitors C_1 , C_2 , and C_3 are replaced by effective shorts because their values are selected so that X_C is negligible at the signal frequency and can be considered to be 0Ω

$$X_C = \text{Capacitive Reactance} = 1/2\pi f C$$

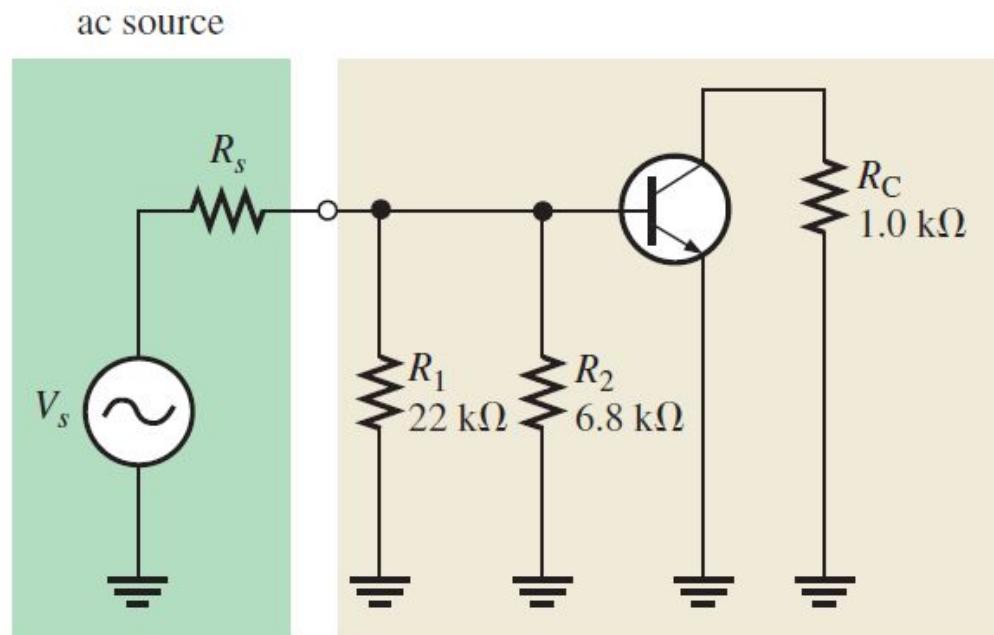
2. The dc source is replaced by ground.

AC Analysis of CE amplifier

- The ac equivalent circuit for the common-emitter amplifier is shown in Figure
- Notice that both R_C and R_1 have one end connected to ac ground (red) because, in the actual circuit, they are connected to V_{CC} which is, in effect, ac ground.



(a) Without an input signal voltage
(AC ground is shown in red.)



(b) With an input signal voltage

Input Resistance at the Base

- A high value of input resistance is desirable so that the amplifier will not excessively load the signal source.
- The input resistance looking in at the base of the transistor is

$$R_{in(base)} = \frac{V_{in}}{I_{in}} = \frac{V_b}{I_b}$$

Output Resistance

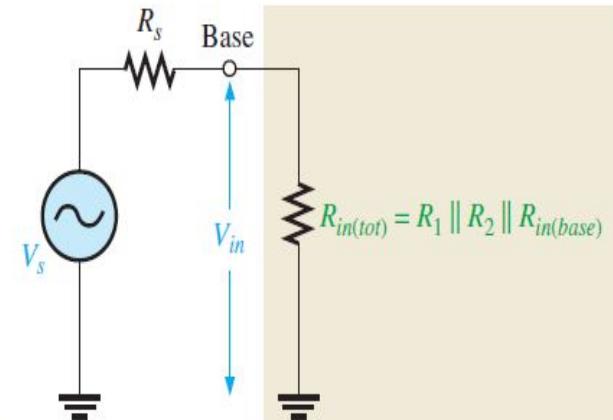
- The output resistance of the common-emitter amplifier is the resistance looking in at the collector and is approximately equal to the collector resistor

$$R_{out} \cong R_c$$

Signal (AC) Voltage at the Base

- The source voltage, V_s , is divided down by R_s (source resistance) and $R_{in(tot)}$ so that the signal voltage at the base of the transistor is found by the voltage-divider formula
- The *bias resistance* and the *ac input resistance* at the base of the transistor and is simplified by combining R_1 , R_2 , and $R_{in(base)}$ in parallel to get the total *input resistance*, $R_{in(tot)}$

$$R_{in(tot)} = R_1 \parallel R_2 \parallel R_{in(base)}$$



$$V_b = \left(\frac{R_{in(tot)}}{R_s + R_{in(tot)}} \right) V_s$$

If $R_s \ll R_{in(tot)}$, then $V_b \approx V_s$ where V_b is the input voltage, V_{in} , to the amplifier.

Voltage Gain

- The gain is the ratio of ac output voltage at the collector (V_c) to ac input voltage at the base (V_s).

$$A_V = \frac{V_{out}}{V_{in}} = \frac{V_c}{V_s}$$

Current Gain

- The current gain from base to collector is However, the overall current gain of the common-emitter amplifier is

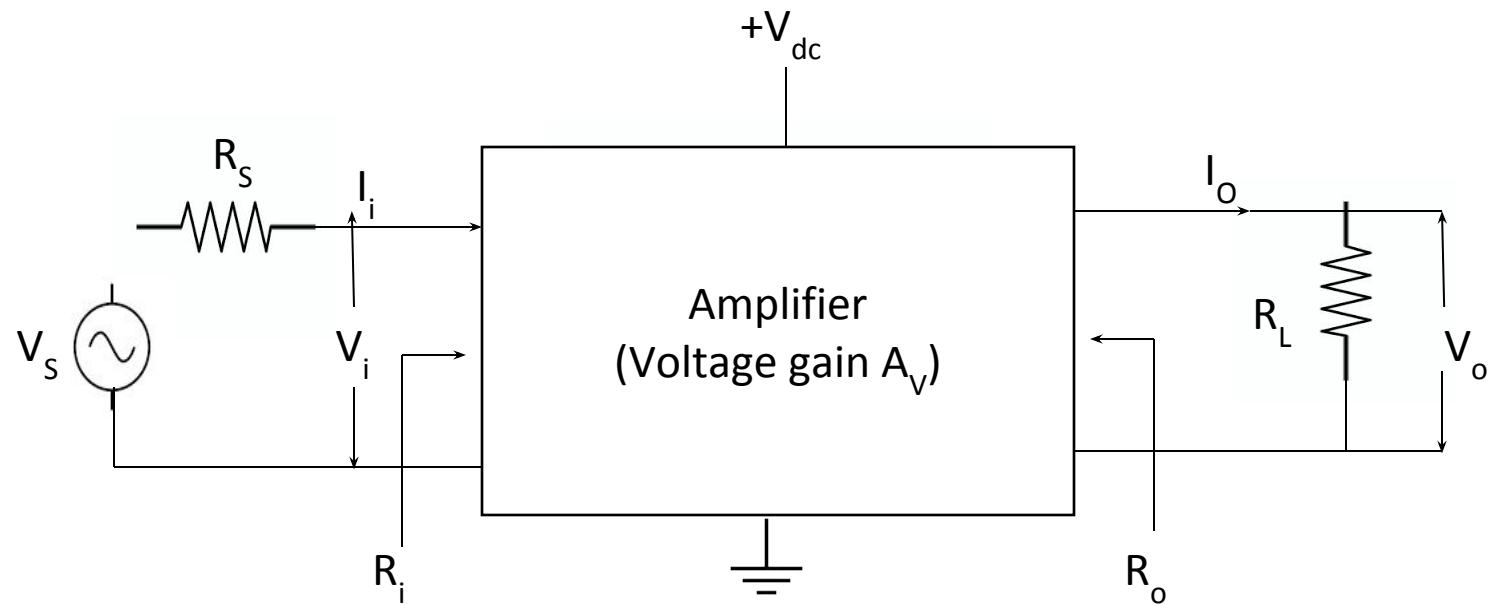
$$A_i = \frac{I_c}{I_s}$$

Power Gain

- The overall power gain is the product of the overall voltage gain (A_V) and the overall current gain (A_i).

$$A_p = A_V \times A_i$$

Amplifier – As a two port Network



h-parameters

- Hybrid parameters (also known as h parameters) are known as ‘hybrid’ parameters to represent the relationship between voltage and current in a two port network
- They use Z parameters, Y parameters, voltage ratio, and current ratio
- H parameters encapsulate all the important linear characteristics of the circuit, so they are very useful for transistor circuit analysis
- H parameters are useful in describing the input-output characteristics of circuits where it is hard to measure Z or Y parameters (such as a transistor)
- The term hybrid : the combination of variables V and I

ac h parameters of a transistor

A manufacturer's datasheet typically specifies h (hybrid) parameters (h_i , h_r , h_f , and h_o) because they are relatively easy to measure.

h PARAMETER	DESCRIPTION	CONDITION
h_i	Input impedance (resistance)	Output shorted
h_r	Voltage feedback ratio	Input open
h_f	Forward current gain	Output shorted
h_o	Output admittance (conductance)	Input open

◀ TABLE 6-2

Basic ac h parameters.

CONFIGURATION	h PARAMETERS
Common-Emitter	h_{ie} , h_{re} , h_{fe} , h_{oe}
Common-Base	h_{ib} , h_{rb} , h_{fb} , h_{ob}
Common-Collector	h_{ic} , h_{rc} , h_{fc} , h_{oc}

◀ TABLE 6-3

Subscripts of h parameters for each of the three amplifier configurations.

Hybrid Parameters

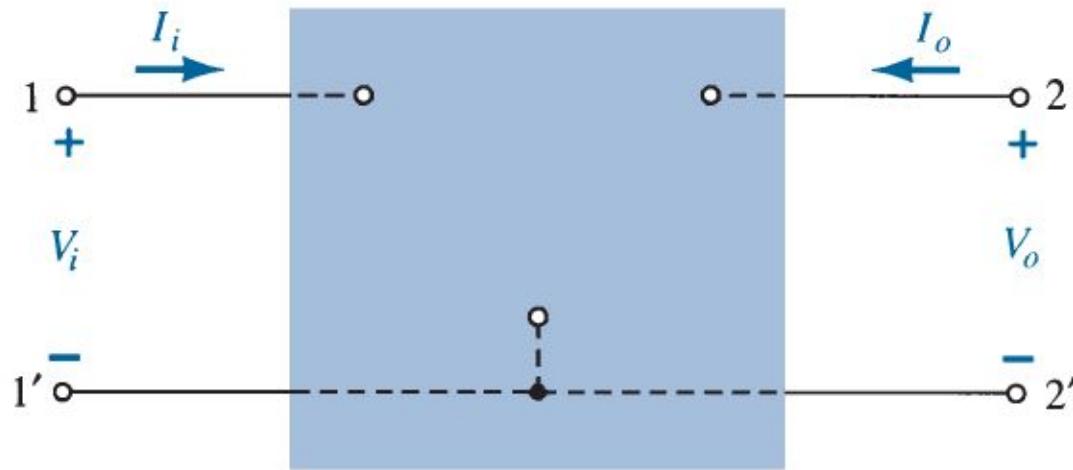


FIG. 93
Two-port system.

$$V_i = h_{11}I_i + h_{12}V_o$$

$$I_o = h_{21}I_i + h_{22}V_o$$

Hybrid Parameters

$$V_i = h_{11}I_i + h_{12}V_o$$

$$I_o = h_{21}I_i + h_{22}V_o$$

$$h_{11} = \left. \frac{V_i}{I_i} \right|_{V_o=0}$$

ohms -> short-circuit input-impedance parameter

$$h_{12} = \left. \frac{V_i}{V_o} \right|_{I_i=0}$$

unitless -> *Open-circuit reverse transfer voltage ratio parameter*

$$h_{21} = \left. \frac{I_o}{I_i} \right|_{V_o=0}$$

unitless -> *Short-circuit forward transfer current ratio parameter*

$$h_{22} = \left. \frac{I_o}{V_o} \right|_{I_i=0}$$

siemens Or Ω (mho)
 -> *Open-circuit output admittance parameter*

The Hybrid Equivalent Model

h_{11} -> input resistance -> h_i

h_{12} -> reverse transfer voltage ratio -> h_r

h_{21} -> forward transfer current ratio -> h_f

h_{22} -> output conductance -> h_o

$$V_i = h_{11}I_i + h_{12}V_o$$

$$I_o = h_{21}I_i + h_{22}V_o$$

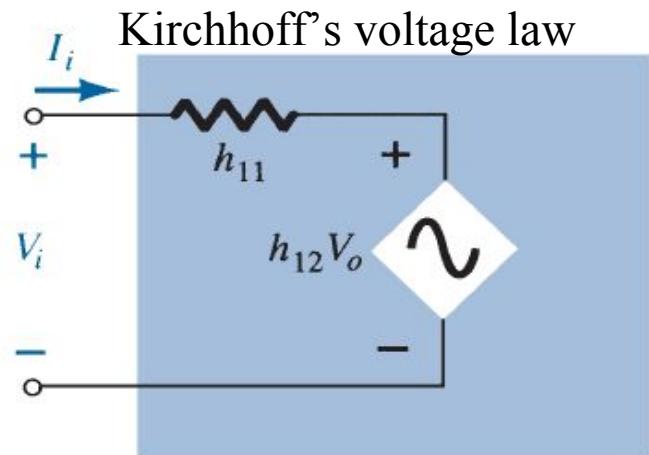


FIG. 94

Hybrid input equivalent circuit.

Kirchhoff's current law

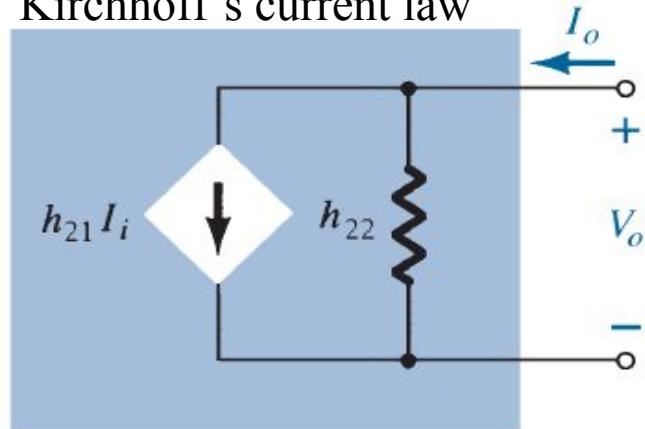


FIG. 95

Hybrid output equivalent circuit.

The Hybrid Equivalent Model

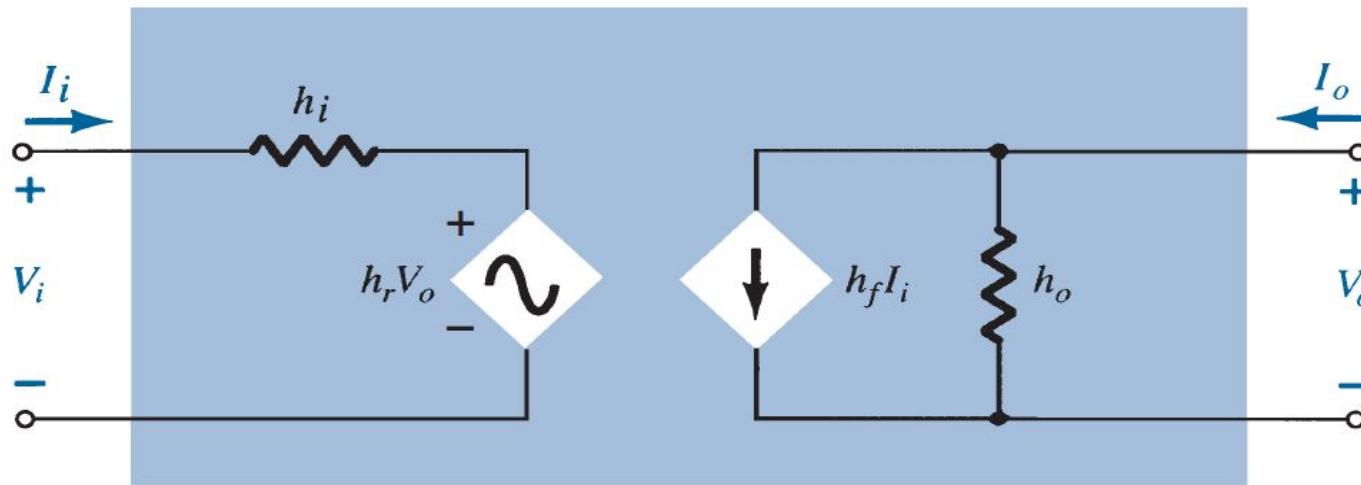


FIG. 96

Complete hybrid equivalent circuit.

- The complete “ac” equivalent circuit for the basic three-terminal linear device is indicated in Fig. 96 with a new set of subscripts for the h -parameters.
- For the transistor, therefore, even though it has three basic configurations, *they are all three-terminal configurations*, so that the resulting equivalent circuit will have the same format

The Hybrid Equivalent Model

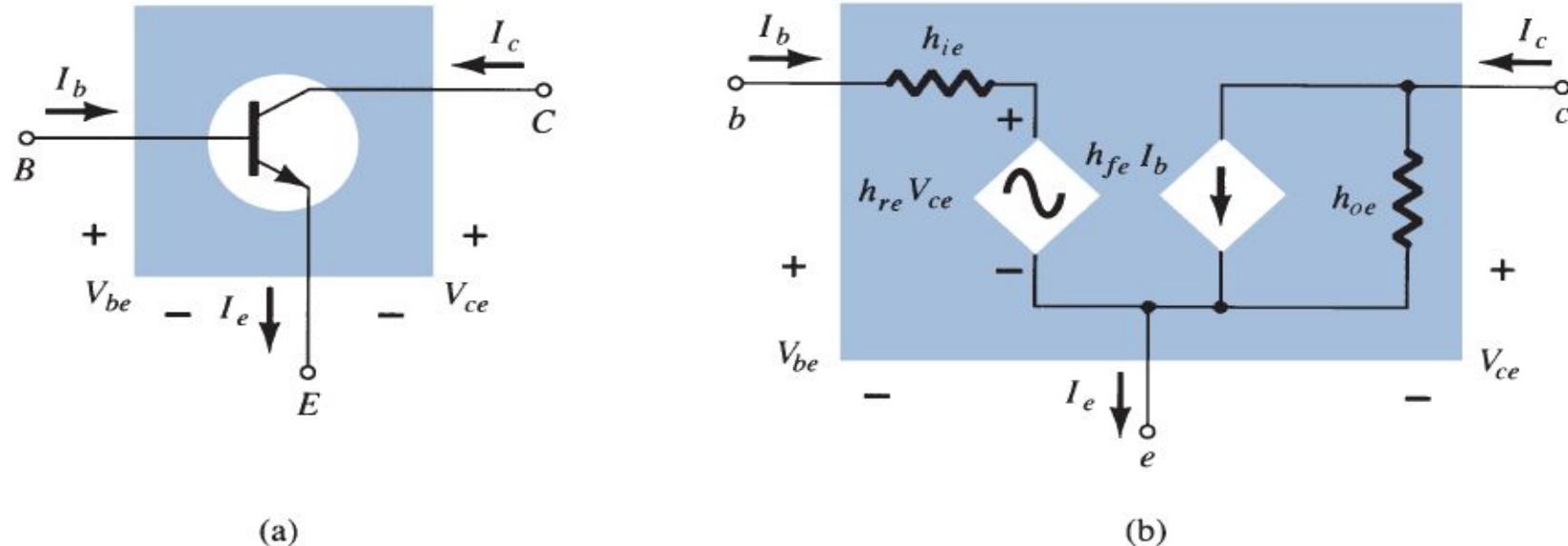


FIG. 97

Common-emitter configuration: (a) graphical symbol; (b) hybrid equivalent circuit.

- The transistor model is a three-terminal two-port system.
- The h -parameters, however, will change with each configuration.
- To distinguish which parameter has been used subscript has been added to the h -parameter notation

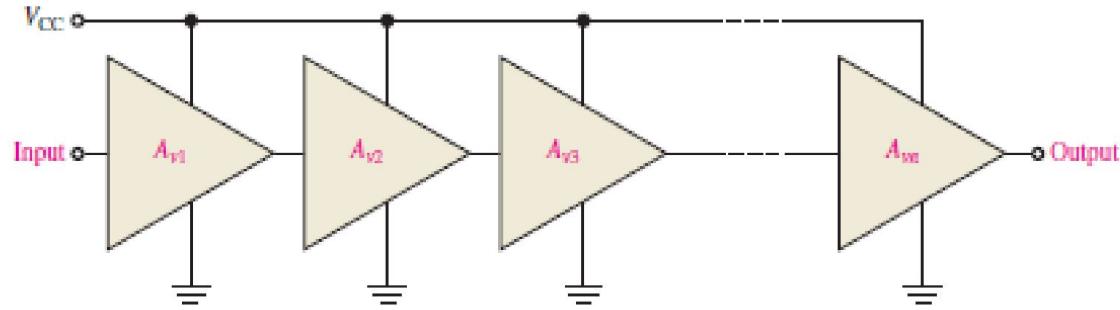
h-parameters for CE

- The quantities h_{ie} , h_{re} , h_{fe} , and h_{oe} of Fig. 7.28 are called the hybrid parameters
- These are components of a small-signal equivalent circuit of the transistor
- h_{oe} parameter of the hybrid equivalent model provide some measure for the output impedance.

		Min.	Max.	
Input impedance ($I_C = 1 \text{ mA dc}, V_{CE} = 10 \text{ V dc}, f = 1 \text{ kHz}$)	h_{ie}	0.5	7.5	$\text{k}\Omega$
Voltage feedback ratio ($I_C = 1 \text{ mA dc}, V_{CE} = 10 \text{ V dc}, f = 1 \text{ kHz}$)	h_{re}	0.1	8.0	$\times 10^{-4}$
Small-signal current gain ($I_C = 1 \text{ mA dc}, V_{CE} = 10 \text{ V dc}, f = 1 \text{ kHz}$)	h_{fe}	20	250	—
Output admittance ($I_C = 1 \text{ mA dc}, V_{CE} = 10 \text{ V dc}, f = 1 \text{ kHz}$)	h_{oe}	1.0	30	$1\mu\text{S}$

Figure 7.28 Hybrid parameters for the 2N4400 transistor.

Multistage amplifier to get higher gain



▲ FIGURE 6–33

Cascaded amplifiers. Each triangular symbol represents a separate amplifier.

Quiz

- 1) The dimension of the four hybrid (h) parameters h_{11} , h_{12} , h_{21} and h_{22} of a two port network are-----
- a) ohm b) mho c) volts d) none

Ans- a, d, d , b

- 2) The current gain of an amplifier _____
as the load resistance is increased
- a)increases b) decreases c) unchanged d)increases and then
decreases

Ans : b

Quiz

- 3) The overall voltage gain of a common emitter amplifier with non ideal voltage source ----- as the internal resistance of the input voltage source increases
a)increases b) decreases c) unchanged d)increases and then decreases

Ans : b

- 4) The common emitter is the most common amplifier configuration as it has
a) a very high input resistance and low output resistance
b)a low volage gain and low current gain
c)a low input resistance and high output resistance
d) a high voltage gain and high current gain

Ans : d

Quiz

- 5) Current gain for common emitter amplifier with transistor parameters $h_{fe} = 220$, $h_{ie} = 2.7K$, $h_{oe} = 18\mu s$, $h_{re} = 1.5 \times 10^{-4}$ and $R_L = 1.5K\Omega$ is.....
- 6) In hybrid model of bipolar junction transistor h_{12} represents.....

Transistor Used in Laboratory



BC547 is a NPN transistor

- BC547 has a gain value of 110 to 800, this value determines the amplification capacity of the transistor.
- The maximum amount of current that could flow through the Collector pin is 100mA, hence we cannot connect loads that consume more than 100mA using this transistor.
- To bias a transistor we have to supply current to base pin, this current (I_B) should be limited to 5mA.

Datasheet of BJT

BC546, B BC547, A, B, C BC548, A, B, C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS					
DC Current Gain ($I_C = 10 \mu\text{A}, V_{CE} = 5.0 \text{ V}$)	h_{FE}	—	90	—	—
	BC547A/548A	—	150	—	—
	BC546B/547B/548B	—	270	—	—
	BC548C	—	—	—	—
($I_C = 2.0 \text{ mA}, V_{CE} = 5.0 \text{ V}$)	BC546	110	—	450	—
	BC547	110	—	800	—
	BC548	110	—	800	—
	BC547A/548A	110	180	220	—
	BC546B/547B/548B	200	290	450	—
	BC547C/BC548C	420	520	800	—
($I_C = 100 \text{ mA}, V_{CE} = 5.0 \text{ V}$)	BC547A/548A	—	120	—	—
	BC546B/547B/548B	—	180	—	—
	BC548C	—	300	—	—
Collector-Emitter Saturation Voltage ($I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$) ($I_C = 100 \text{ mA}, I_B = 5.0 \text{ mA}$) ($I_C = 10 \text{ mA}, I_B = \text{See Note 1}$)	$V_{CE(\text{sat})}$	—	0.09	0.25	V
	—	—	0.2	0.6	—
	—	—	0.3	0.6	—
Base-Emitter Saturation Voltage ($I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$)	$V_{BE(\text{sat})}$	—	0.7	—	V
Base-Emitter On Voltage ($I_C = 2.0 \text{ mA}, V_{CE} = 5.0 \text{ V}$) ($I_C = 10 \text{ mA}, V_{CE} = 5.0 \text{ V}$)	$V_{BE(\text{on})}$	0.55	—	0.7	V
	—	—	—	0.77	—

SMALL-SIGNAL CHARACTERISTICS

Current-Gain — Bandwidth Product ($I_C = 10 \text{ mA}$, $V_{CE} = 5.0 \text{ V}$, $f = 100 \text{ MHz}$)	BC546 BC547 BC548	f_T	150 150 150	300 300 300	— — —	MHz
Output Capacitance ($V_{CB} = 10 \text{ V}$, $I_C = 0$, $f = 1.0 \text{ MHz}$)		C_{obo}	—	1.7	4.5	pF
Input Capacitance ($V_{EB} = 0.5 \text{ V}$, $I_C = 0$, $f = 1.0 \text{ MHz}$)		C_{ibo}	—	10	—	pF
Small-Signal Current Gain ($I_C = 2.0 \text{ mA}$, $V_{CE} = 5.0 \text{ V}$, $f = 1.0 \text{ kHz}$)	BC546 BC547/548 BC547A/548A BC546B/547B/548B BC547C/548C	h_{fe}	125 125 125 240 450	— — 220 330 600	500 900 260 500 900	—
Noise Figure ($I_C = 0.2 \text{ mA}$, $V_{CE} = 5.0 \text{ V}$, $R_S = 2 \text{ k}\Omega$, $f = 1.0 \text{ kHz}$, $\Delta f = 200 \text{ Hz}$)	BC546 BC547 BC548	NF	— — —	2.0 2.0 2.0	10 10 10	dB

Resource Material for the topic

- Reference Books:

Floyd Thomas, *Electronic Devices*, Prentice Hall, 9th Edition 2012

- Links to Useful Videos:

1. Transistors

<https://www.youtube.com/watch?v=0C4uxtS-tIQ>

2. Fabrication of BJT

<https://www.youtube.com/watch?v=j-YEdsVV74>

- Links to Useful Resource material: