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MIT WORLD PEACE UNIVERSITY | PUNE
TECHNOLOGY, RESEARCH, SOCIAL INNOVATION & PARTNERSHIPS

MIT-WPU
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School of Computer science and Engineering

Department of Computer Engineering and Technology
Final Year BTech (CSE/CSF) (Academic Year 2024-25)
Mid Term Exam - Semester VIII

Course Name:- System Software and Compiler Design
Course Code:-CET3011B
Maximum Marks: 30 **Time: 1 Hr ... Minutes** **Date:**

Instructions:-

1. *Attempt any 3 questions from Q. 1 to Q. 4 AND Attempt any 3 questions from Q. 5 to Q. 8*
2. *Figure to the right indicates full marks.*
3. *Use of cell phone is prohibited in the examination hall.*
4. *Neat diagrams must be drawn wherever necessary.*
5. *Assume suitable data, if necessary and clearly state.*
6. *Use of scientific calculator is allowed*

Attempt any 3 questions from Q. 1 to Q. 4

Q1		START 200
		BACK MOVER AREG, LOOP
		ADD AREG, ='2'
		SUB BREG, ='3'
		LTORG
		MULT DREG, B2
		B1 EQU BACK
		ADD BREG, ='2'
		LOOP DS 5
		B2 DS 4
		END
		
		Build the contents at the end of Pass 1 of a 2 pass assembler, by considering the assembly language program above.
			[5 Marks]

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Q2		List the Statement Classes for an ALP of a hypothetical machine. Give examples of 2 statements belonging to each class.	[5 Marks]

Q3		Build intermediate code and literal table for the following source program:
		
		START 200
		MOVER DREG, ='8'
		MOVEM AREG, X
		B1 MOVER BREG, Y
		MOVER CREG, Z
		MOVER DREG, ='3'
		LTORG
		SUB BREG, = '6'
		ORIGIN B1 + 10
		MULT BREG ='3'
		X DS 5
		Y EQU B1
		Z DC 10
		END
			[5 Marks]

Q4		List the tasks of Analysis and synthesis phase of a 2-pass assembler.	[5 Marks]
		Attempt any 3 questions from Q. 5 to Q. 8	

Q.5		MACRO
		MULTIPLY &A1,&A2
		MOVER AREG, &A1
		MULT AREG,&A2
		MEND
		MACRO
		DIVIDE &A3,&A4
		MOVER BREG, &A3
		DIV BREG,&A4
		MEND
		START 100
			[5 Marks]

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		MULTIPLY S1,S2 DIVIDE S1,S2 END Build the contents at the end of Pass 1 of a 2 pass macroprocessor, by considering the assembly language program above.	
Q.6		Discuss transfer vector and relocation bits in Relocating loaders with an example.	[5 Marks]
Q.7		Define Linker. Derive the equation to find the linking time address of a particular symbol in an assembly language program.	[5 Marks]
Q.8		Explain Direct linking Loader.Generate ESD and RLD card for following code	[5 Marks]

```
0     0     MAIN      START
1           ENTRY     S1, S2
2           EXTRN     ARG1, MAIN1
3     40    S1
4     50    S2
5     60          DC    A(S1)
6     64          DC    A(S2+15)
7     68          DC    A(S2-S1-3)
8     72          DC    A (MAIN1)
9     76          DC    A(ARG1+MAIN1+S2-4)
10          END
```

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