Silicon Photo-Receivers

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Abstract. The properties of photodiodes being exploitable in standard bipolar, CMOS, and BiCMOS technologies are summarized. In addition examples of advanced photodiodes will be introduced in order to show how the properties of integrated photodiodes can be improved significantly by minor process modifications. Furthermore, examples of optoelectronic integrated circuits (OEICs) for such important applications like optical storage systems and optical fiber receivers are described. New trends for the circuit topology of digital-video-disk (DVD) and digital-video-recording (DVR) read-OEICs are covered. Progress of OEIC receivers for optical data transmission and communication as well as optical interconnects is also summarized.

1 Photodetectors in Standard Silicon Technologies

Nowadays, there are three types of silicon process technologies for the fabrication of integrated circuits: bipolar, complementary metal oxide semiconductor (CMOS), and a combination of both in BiCMOS processes. These technologies are very mature and there is a trend towards integrated sensors. The integration of optical sensors especially is very interesting. In the following, properties of photodiodes being available without process modifications are described.

1.1 Photodetectors in Bipolar Technology

Modern bipolar integrated circuits are manufactured in standard-buried-collector (SBC) technology [1]. Without any technological modifications, the buried N^+ collector can serve as the cathode (see Fig. 1), the N collector epitaxial layer can serve as the 'intrinsic' layer of a PIN photodiode, and the base implant can serve as the anode in order to integrate PIN photodiodes with a thin 'intrinsic' region in bipolar technologies [2,3]. The process of [2] was described in [4]. The only difference in Fig. 1 compared to the cross section of an NPN transistor is that the N^+ emitter (lying within the P-base) is omitted, which is a pure layout matter and does not need any technological modification.

The small thickness of the epitaxial layer of high-speed bipolar processes in the range of about 1 µm causes a low quantum efficiency in the yellow to the infrared spectral region (580 nm to 1100 nm). The rise and fall times of

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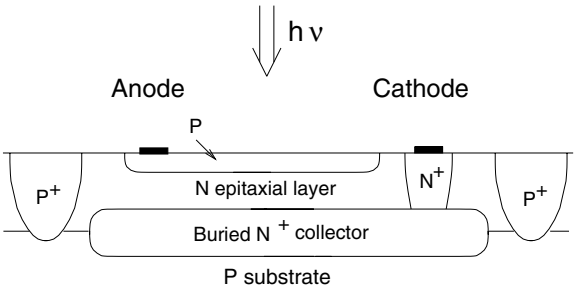

Fig. 1. Schematic cross section of a base-collector photodiode

the photocurrent for light pulses are very short due to the small epitaxial layer thickness. In [2] a bit rate of 10 Gb/s for the base-collector diode and a responsivity R of merely 48 mA/W for 840 nm were reported. This low responsivity at wavelengths from 780 nm to 850 nm, which are widely used for optical data transmission on short fiber lengths of up to several kilometers, is a major disadvantage of standard bipolar OEICs.

The base-collector diode with a sensitive area of 100 μm^2 fabricated in a 0.8 µm silicon bipolar technology worked up to 3 Gb/s for a wavelength of 850 nm [3]. A sensitivity of 0.045 A/W was reported. A phototransistor with a very small sensitive area of 10 μm^2 reached a data rate of 5 Gb/s.

1.2 Photodetectors in CMOS Technology

The simplest way to build CMOS OEICs is to use the PN junctions available in CMOS processes: source/drain-substrate, source/drain-well, and well-substrate diodes. These PN photodiodes, however, possess regions which are free of electric fields. In these regions, the slow diffusion of photogenerated carriers determines the transient behavior of such PN photodiodes. Published PN CMOS OEICs are characterized by bandwidths of less than 15 MHz [5, 6, 7]. Another example is described in [8], where the OEIC was optimized for a dynamic range of six decades in illumination.

The source/drain-substrate and source/drain-well photodiodes are more appropriate for the detection of wavelengths shorter than about 600 nm, whereas the well-substrate photodiode is more appropriate for long wavelengths like 780 nm or 850 nm. Figure 2, for instance, shows an N^+/P-substrate photodiode.

In addition to carrier diffusion, the series resistance of the photodiodes due to lateral anode contacts at the silicon surface together with the relatively large junction capacitance of the photodiode may limit the dynamical PN photodiode behavior. In an N-well process, the anode of the N^+/P-substrate photodiode has to be at V_{SS} potential, which may be a restriction for circuit design.

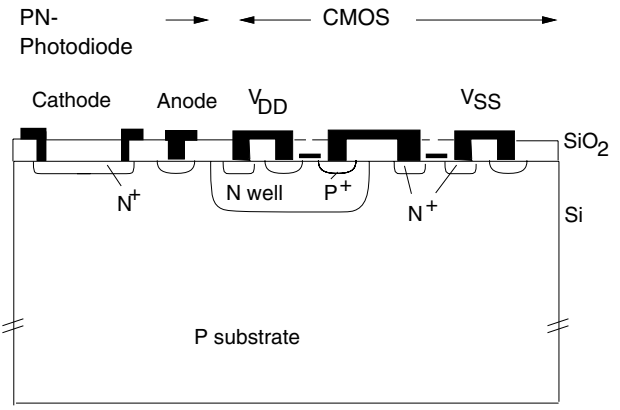

Fig. 2. Schematic cross section of a PN photodiode integrated in a one-well CMOS chip

A lateral N^+/P-substrate/P^+ photodiode was used as an optical detector, into which light was coupled by an integrated waveguide [5]. This detector was realized in a 0.8 µm N-well CMOS process. A maximum bandwidth of 10 MHz was achieved with a transimpedance amplifier for a photocurrent of 1 µA with $\lambda = 675$ nm. The speed of the detector was limited by carrier diffusion due to photogeneration outside the diode [6].

The N-well/P-substrate diode in a 2 µm N-well CMOS process was used as a photodiode in [7]. A bandwidth of 1.6 MHz with a wavelength $\lambda = 780$ nm was reported for an unoptimized system. The leakage current density of the photodiode was 15 pA/mm^2 at 5 V. The responsivity for $\lambda = 780$ nm was 0.5 A/W (quantum efficiency $\eta = 70\%$). The light was coupled into the photodiode via an integrated waveguide.

1.3 Photodetectors in BiCMOS Technology

In order to demonstrate the speed limitation caused by the rather high doping concentrations in modern standard technologies, we consider an N^+/P-substrate photodiode in a CMOS-based BiCMOS technology. The problem, however, is exactly the same in modern CMOS processes. Figure 3 shows the cross section of this photodiode.

Modern CMOS and BiCMOS process are optimized with respect to a minimum number of masks and, therefore, implement a self-aligned well processing scheme. Such a process scheme has the effect, that only N wells can be defined in the layout (for a process using P-type substrate) and everywhere outside of the N wells P wells are present. Therefore, there is a P well with a doping concentration exceeding 10^{16} cm^{-3} incorporated in the N^+/P-substrate photodiode. This leads to a thin N^+/P-substrate space-charge region and the effect of slow carrier diffusion is very pronounced (see Fig. 4). Rise

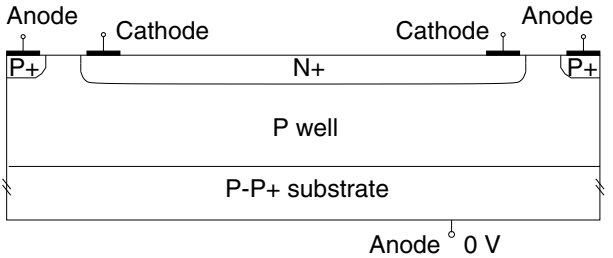

Fig. 3. Cross section of a N^+/P-substrate photodiode in self-adjusting well BiCMOS technology

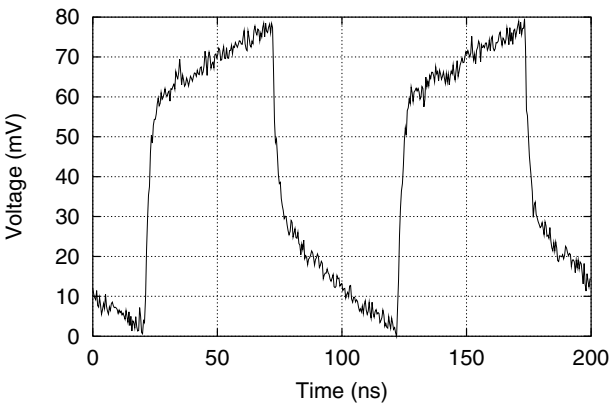

Fig. 4. Transient response of a N^+/P-substrate photodiode in a self-adjusting well BiCMOS technology

and fall times of 26 ns and 28 ns, respectively, are determined due to the pronounced diffusion tail. The measured −3 dB bandwidth is 6.7 MHz [9].

A standard BiCMOS technology with a minimum effective channel length of 0.45 µm (corresponding to a drawn or nominal channel length of about 0.6 µm) without any modifications was used [10, 11] to exploit a fast photodiode. The buried N^+-collector in Fig. 5 was used for the cathode of the PIN photodiode. The P^+-source/drain island served for the anode. The intrinsic zone of the PIN photodiode was formed by the N well and, therefore, had only a thickness of 0.7 µm. Consequently, the responsivity of the photodiode was only 0.07 A/W for a wavelength of 850 nm [10]. For a bias of 2.5 V across the $75 \times 75\ \mu m^2$ PIN photodiode with a capacitance of 1.8 pF, a −3 dB bandwidth of 700 MHz was reported. The OEIC reached a bit rate of 531 Mb/s with a bit error rate of 10^{-9} and a sensitivity of $-14.8\,dB \cdot m$. This bit rate was limited by the capacitance of the photodiode and the feedback resistor of 1.4 kΩ in the amplifier transimpedance input stage. The dark current of the photodiode was 10 nA for a reverse voltage of 2.5 V at room temperature.

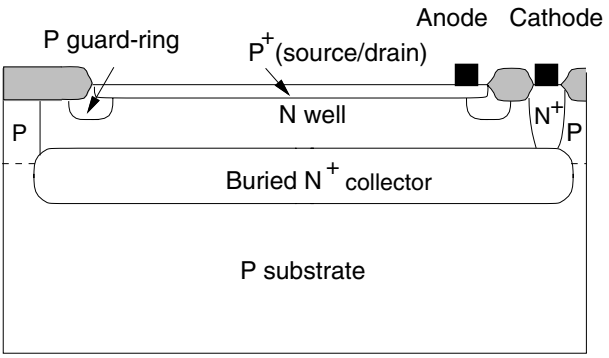

Fig. 5. PIN photodiode in a SBC-based BiCMOS technology [10]

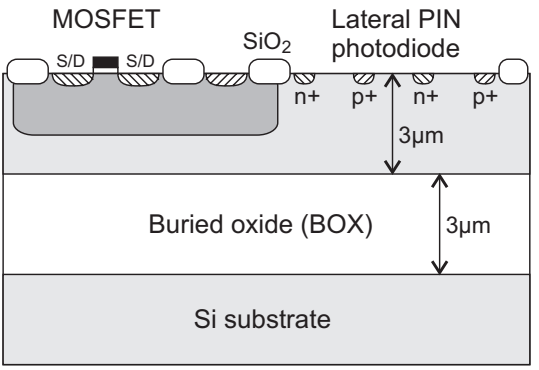

Fig. 6. Cross section of lateral SOI PIN photodiode

In [11] a laser with a wavelength of 670 nm was used for the characterization of the same OEIC as in [10]. The data rate was increased to 622 Mb/s for this wavelength. No measured result for the responsivity was given in [11]. Instead, a three times larger responsivity value of approximately 0.2 A/W for $\lambda = 670$ nm was estimated due to the lower penetration depth than for $\lambda = 850$ nm. This estimation, however, may be doubtful, because possible destructive interference in the isolation and passivation stack is neglected. The main drawback for the photodiode used in [10, 11] was its low responsivity due to the thin epitaxial layer in the SBC-bipolar based BiCMOS process.

1.4 Lateral PIN Photodiodes on SOI

Silicon-on-Insulator (SOI) was suggested to be the technology of future CMOS [12]. SOI uses a thin crystalline silicon film for the integration of devices. A cross section of the integration scheme used for SOI receivers [13] is shown in Fig. 6. The starting material was bonded and etched-back silicon-on-insulator (BESOI), and the active Si layer was N-type (100) with a resistivity of

$50\,\Omega \cdot \mathrm{cm}$–$80\,\Omega \cdot \mathrm{cm}$ and a thickness of 3 µm. The buried oxide layer (BOX) was also 3 µm thick. The fabrication steps have been described in detail elsewhere [14]. All processing steps were fully compatible with standard CMOS processes. Indeed, this structure could easily be implemented in a standard process with no modifications other than the starting substrate.

The P- and N-fingers of the lateral, interdigitated PIN photodiode were formed during the P-well contact and source/drain implants, respectively. The finger width was 2 µm and the spacing between the fingers was 5 µm. The total photodiode area was 51 µm by 46 µm.

The dark current of the SOI device was 2.1 nA at 5 V and 2.2 nA at 20 V. The onset of breakdown occured at 40 V. The external quantum efficiency was measured as a function of wavelength using a white light source, spectrometer, chopper, and lock-in amplifier using a calibrated Si photodiode as a reference. At 850 nm, the efficiency of the SOI photodiode was 29% corresponding to a responsivity of 0.20 A/W. The −3 dB bandwidth of the SOI photodiode with a bias $|\ V_{\mathrm{PD}}\ | = 20\,\mathrm{V}$ was 2.8 GHz [13].

2 Advanced Photodetectors

2.1 Double Photodiode

In a standard CMOS or a CMOS-based triple-diffused (3-D) BiCMOS technology [9], the so-called double photodiode can be applied in order to eliminate slow carrier diffusion. In a CMOS based (3-D) BiCMOS process, an N well can be used as the collector of a bipolar NPN transistor. This N well can also be used in order to form the cathode of the double photodiode (DPD). Figure 7 shows the cross section of such a DPD. The two anodes are connected to ground. The cathode is connected to the amplifier in the OEIC. Two PN junctions are vertically arranged.

In addition to the two space-charge regions at the two vertically arranged PN junctions, an electric field is also present between the two space-charge regions due to the doping gradient of the N well. Therefore, there is no contribution of slow carrier diffusion from the region between the two space-charge regions. With an integrated polysilicon resistor of 1 kΩ, rise and fall times of

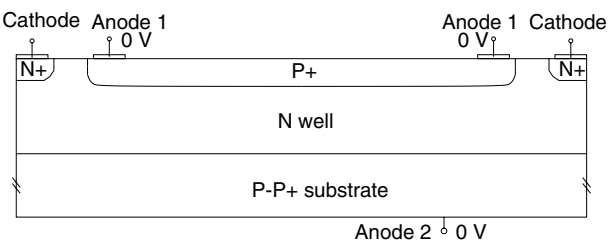

Fig. 7. Cross section of a double photodiode in BiCMOS technology [15]

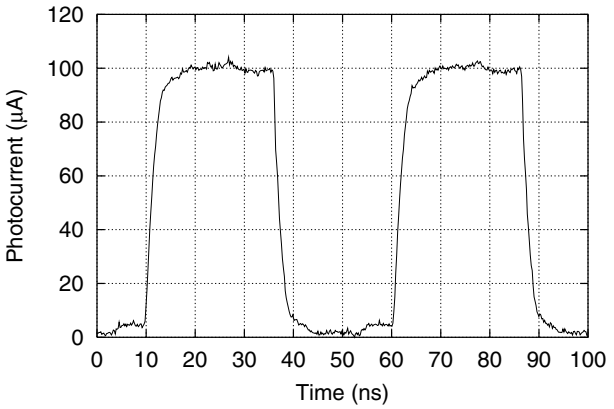

Fig. 8. Transient response of the double photodiode in BiCMOS technology shown in Fig. 7 [16]

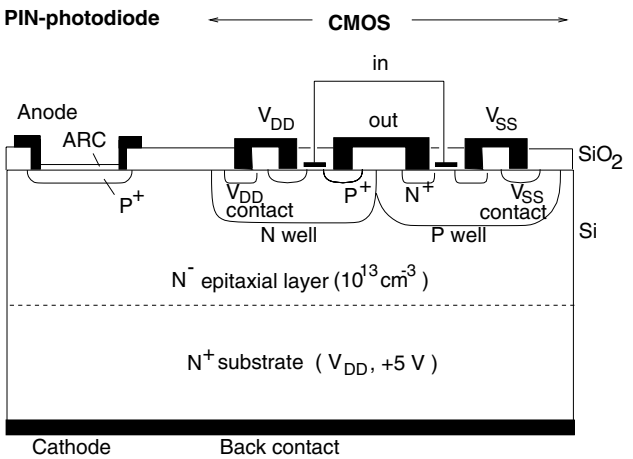

Fig. 9. Cross section of a N^-N^+ PIN-CMOS-OEIC [33]

3.2 nm and 2.8 ns, respectively, were measured for the DPD with $\lambda = 638\,\text{nm}$ and $U_\text{r} = 2.5\,\text{V}$ [16]. With an integrated $500\,\Omega$ resistor, rise and fall times of 1.8 ns and 1.9 ns, respectively, were found [15]. There is no indication of a so-called diffusion tail in the photocurrent (Fig. 8).

2.2 Vertical PIN Photodiode

Figure 9 shows the structure of an N^-N^+ CMOS-OEIC in the twin-well CMOS approach [9]. Here the N^+ substrate serves as the cathode and the P^+ source/drain region forms the anode of the integrated PIN photodiode.

PIN-CMOS photodiodes with an area of $2700\,\mu\text{m}^2$, with a standard doping concentration of $1 \times 10^{15}\,\text{cm}^{-3}$ and with reduced doping concentrations in

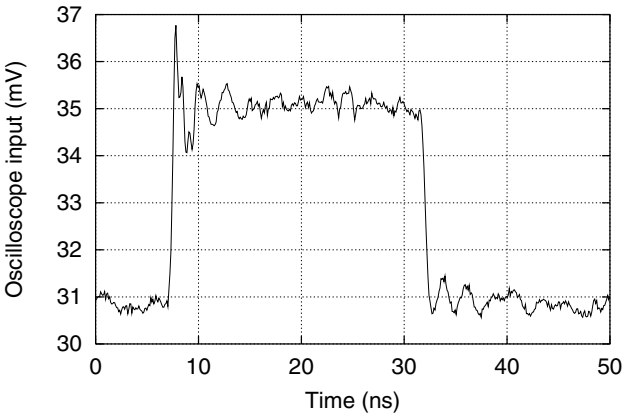

Fig. 10. Measured transient response of a CMOS-integrated PIN photodiode with an I-layer doping concentration of $2 \times 10^{13}\,\mathrm{cm}^{-3}$ for $\lambda = 638\,\mathrm{nm}$ and $|V_{\mathrm{PD}}| = 3.0\,\mathrm{V}$. The overshoot in the signal is due to the direct modulation of the laser [18]

the epitaxial layer down to $2 \times 10^{13}\,\mathrm{cm}^{-3}$, and with an integrated polysilicon resistor of $500\,\Omega$, were fabricated in an industrial $1.0\,\mu\mathrm{m}$ CMOS process [17]. For the measurements, a laser with $\lambda = 638.3\,\mathrm{nm}$ was modulated with a commercial ECL generator. The light pulses were coupled into the photodiodes on a wafer prober via a single-mode optical fiber. The rise (t_r) and fall (t_f) times of the photocurrent of the photodiodes were measured with a picoprobe (pp), which possesses a $-3\,\mathrm{dB}$ bandwidth of $3\,\mathrm{GHz}$ and an input capacitance of $0.1\,\mathrm{pF}$, and with a $20\,\mathrm{GHz}$ digital sampling oscilloscope HP54750/51.

For the PIN photodiode with a doping concentration in the epitaxial layer of $2 \times 10^{13}\,\mathrm{cm}^{-3}$, the oscilloscope extracted $t_\mathrm{r}^{\mathrm{osc,disp}} = 0.37\,\mathrm{ns}$ and $t_\mathrm{f}^{\mathrm{osc,disp}} = 0.57\,\mathrm{ns}$ from the waveform shown in Fig. 10. The evaluation according $(t_\mathrm{r}^{\mathrm{PIN}})^2 = (t_\mathrm{r}^{\mathrm{osc,disp}})^2 - (t_\mathrm{r}^{\mathrm{laser}})^2 - (t_\mathrm{r}^{\mathrm{pp}})^2 - (t_\mathrm{r}^{\mathrm{osc}})^2$ with $t_\mathrm{r}^{\mathrm{laser}} = 0.30\,\mathrm{ns}$, $t_\mathrm{f}^{\mathrm{laser}} = 0.51\,\mathrm{ns}$, $t_{\mathrm{r/f}}^{\mathrm{pp}} = 0.1\,\mathrm{ns}$ and $t_{\mathrm{r/f}}^{\mathrm{osc}} \approx 0.02\,\mathrm{ns}$ results in $t_\mathrm{r}^{\mathrm{PIN}} = 0.19\,\mathrm{ns}$ and $t_\mathrm{f}^{\mathrm{PIN}} = 0.24\,\mathrm{ns}$ [33]. With $f_{3\,\mathrm{dB}} = 2.4/(\pi(t_\mathrm{r} + t_\mathrm{f}))$, the $-3\,\mathrm{dB}$ bandwidth can be estimated to be $1.7\,\mathrm{GHz}$ for $|V_{\mathrm{PD}}| = 3.0\,\mathrm{V}$. With the conservative estimate $\mathrm{BR} = 1/(1.5(t_\mathrm{r} + t_\mathrm{f}))$, a bit rate, BR, of $1.5\,\mathrm{Gb/s}$ results for $|V_{\mathrm{PD}}| = 3.0\,\mathrm{V}$. With an antireflection coating (ARC), the quantum efficiency η could be increased from 49% to 94%. To our knowledge this is the first time that such a high speed and such a high quantum efficiency have been achieved with an integrated silicon photodiode for a reverse voltage of only $3\,\mathrm{V}$, whereby an only slightly modified standard CMOS process has been used.

In contrast to transistors in bipolar OEICs, the electrical performance of the N- and P-channel MOSFETs is not degraded when the epitaxial layer is modified. This statement was verified by measurements (Table 1). The threshold voltages of the NMOS and PMOS transistors are practically independent of the doping concentration in the epitaxial layer, because these transistors are placed inside wells which possess a much higher doping level of several

Table 1. Measured threshold voltages U_{Th} and drain leakage currents $I_{\mathrm{D}}^{\mathrm{r}}$ for different doping levels in the epitaxial layer

I-Doping (cm^{-3})	$U_{\mathrm{Th}}^{\mathrm{NMOS}}$ (V)	$I_{\mathrm{D}}^{\mathrm{r,NMOS}}$ (pA)	$U_{\mathrm{Th}}^{\mathrm{PMOS}}$ (V)	$I_{\mathrm{D}}^{\mathrm{r,PMOS}}$ (pA)
Standard	0.79	2.19	−0.62	63.1
1×10^{14}	0.79	0.83	−0.60	66.1
5×10^{13}	0.79	0.81	−0.60	66.1
2×10^{13}	0.78	1.02	−0.60	67.6

times $10^{16}\,\mathrm{cm}^{-3}$ than the standard epitaxial layer with about $1 \times 10^{15}\,\mathrm{cm}^{-3}$ and because the threshold implants produce an even higher doping level ($\approx 10^{17}\,\mathrm{cm}^{-3}$) than the wells [19].

The reverse, i.e. the leakage current of the drain to well diodes is also listed in Table 1 for the NMOS and PMOS transistors [19]. The leakage current for the NMOS transistor in an epitaxial layer with reduced doping concentrations actually seems to be smaller than for the standard concentration.

These results confirm the superiority of the PIN-CMOS integration [20] compared to the PIN-bipolar integration [21]. In contrast to the PIN-bipolar integration, the electrical transistor parameters of the standard twin-well CMOS process are completely unaffected for the PIN-CMOS integration and can be used for circuit simulations within the design of OEICs.

2.3 Finger Photodiode

A new photodiode for the UV/blue spectral range down to wavelengths of 400 nm, which can be integrated monolithically with CMOS circuits was presented [22]. Such optoelectronic integrated circuits (OEICs) with a high sensitivity in the UV/blue spectral range are needed in near-future optical storage systems like DVR (Digital Video Recording) with a storage capacity of more than 30 GB compared to todays CD-ROMs with 650/700 MB, which are read with 780 nm light.

At 400 nm, where laser diodes are available [23], the so-called finger photodiode achieved a responsivity of 0.23 A/W corresponding to a quantum efficiency η of 70% (with an anti-reflection coating (ARC)) and rise and fall times of 1.0 ns and 1.1 ns, respectively. The finger photodiode can be used in the red spectral range, too, for which todays DVD optical pickups use red laser diodes with a wavelength of 630/650 nm. At 638 nm, the responsivity is 0.49 A/W ($\eta = 95\%$) and rise and fall times of less than 2.3 ns were achieved. For the integration of the finger photodiode in an industrial 1 µm twin-well CMOS process only one additional mask (beside the ARC mask) was needed in order to block out the threshold voltage implantation in the photoactive region.

The absorption depth of light with a wavelength of 400 nm in silicon is approximately 0.1 µm. The absorbed optical power is given by the Lambert–

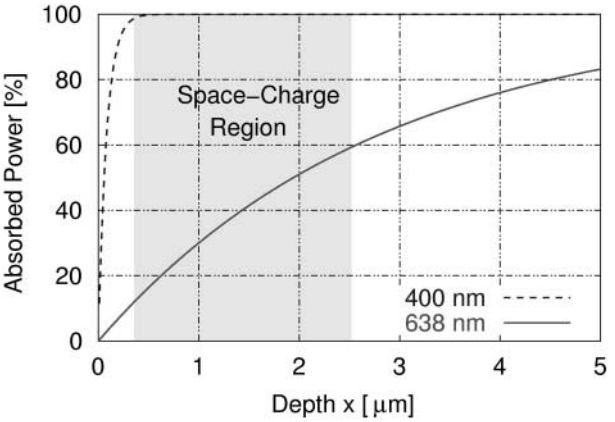

Fig. 11. Absorption of light in silicon for $\lambda = 400\,\text{nm}$ and $\lambda = 638\,\text{nm}$ (higly doped P^+-anode on n-substrate with a doping concentration of $1 \times 10^{15}\,\text{cm}^{-3}$, $V_{PD} = 3\,\text{V}$)

Beer-Law:

$$P = (1 - R)\, P_0\, e^{-\alpha x}\,. \tag{1}$$

P is the absorbed optical power at the depth x in the photodiode (whereby the origin is located at the surface of the photodiode), R is the reflectivity, P_0 is the incident optical power, and α is the absorption coefficient. Considering a conventional PN photodiode with a noninterdigitated P^+-surface anode we can conclude that almost all of the incident photons are absorbed in the quasi neutral region (at the left of the space-charge region in Fig. 11) of the P^+-anode, which normally has a depth of 0.2 µm–0.4 µm.

The majority of the photogenerated carriers recombine in the P^+-anode, because of the small diffusion coefficient due to the low electron and hole mobilities (keeping the Einstein relation in mind). As a consequence of this strong recombination, the responsivity for $\lambda = 400\,\text{nm}$ with a noninterdigitated anode (or cathode for a P-substrate) is low. Furthermore, the slow diffusion processes outside the space-charge region are responsible for a limited response speed.

To avoid both, recombination and diffusion, space-charge regions at the surface have to be implemented. This can be achieved with an interdigitated structure as it is shown in Fig. 12. The N^+-substrate is used as the cathode and the P^+-fingers which are located in the N-epitaxial layer are used as the anode of the photodiode. The P^+-fingers are connected by metal outside of the photosensitive region. Photogenerated carriers can be separated in the space-charge region, electrons drift to the N^+-substrate and holes drift to the P^+-fingers. In order to find the optimum concerning response speed and responsivity, several finger photodiodes on wafers with different doping concentrations in the epitaxial layer and with different numbers of fingers

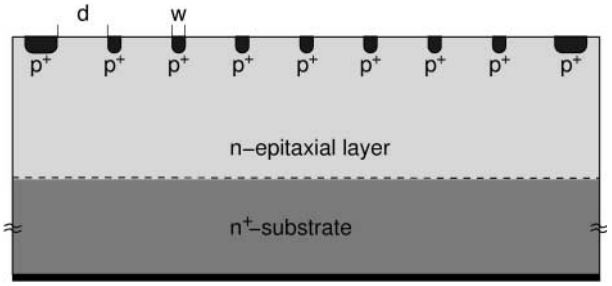

Fig. 12. Cross section of the 9-finger photodiode on n-substrate

have been processed. An industrial 1 µm twin-well CMOS process with one additional mask to block out the threshold voltage implantation in the photo-active region was used. The antireflection coating (ARC) was realized by a stack consisting of SiO_2 and Si_3N_4 (see [19]).

For measurements, an integrated polysilicon resistor with a resistance of $R_L = 0.5\,k\Omega$ for $\lambda = 630\,nm$ and $R_L = 1\,k\Omega$ for $\lambda = 400\,nm$ (because of different optical signal power) was connected in series with the photodiode. The cathode (substrate) was connected to V_{PD} and the anode was connected to the resistor. The second pin of the resistor was connected to ground.

The laser light was coupled into the photodiode with an photo-active area of $50 \times 50\,\mu m^2$) via an optical fiber. The photocurrent resulted in a voltage V_{out} across R_L, which was measured with a picoprobe (with an input capacitance of 0.1 pF and a high input resistance of 10 MΩ). For the transient measurements a sampling oscilloscope (HP 54750A) was used. The dark currents were measured with a parameter analyzer (HP 4156A). A calibrated photodiode was used to determine the incident optical power for responsivity measurements at the finger photodiodes.

In order to find the optimized interdigitated structure, the finger photodiodes were processed with different numbers of fingers. The distance d between the fingers and the finger width w (see Fig. 12) were varied. Table 2 summarizes the results for the 3-, 4-, 6-, and 9-finger photodiodes ($\lambda = 400\,nm$).

Table 2. Dimensions of the finger photodiodes with different numbers of fingers [22]

Fingers	d (µm)	w (µm)	t_r (ns)	t_f (ns)
3	18.6	4.2	6.9	7.9
4	12.8	2.8	5.2	6.3
6	8.0	1.6	3.8	4.5
9	4.8	1.2	1.0	1.1

The fastest photodiode was the one with 9 fingers. Drift of photogenerated carriers leads to the fast response for the 9-finger photodiode with an epitaxial doping concentration $C_e = 1 \times 10^{15}\,cm^{-3}$. For the 3-, 4- and 6-finger photodiode the distance of the anode fingers was too wide and carrier diffusion slows down the response speed.

A responsivity of 0.23 A/W at 400 nm was measured for the 9-finger photodiode compared to 0.08 A/W for a reference photodiode having a noninterdigitated anode both with the same antireflection coating. For the reference photodiode without ARC a responsivity of only 0.045 A/W was found.

For 400 nm, an SOI photodiode suggested in [24] would be a good choice. An SOI photodiode, however, shows a low responsivity for red light due to the thin SOI layer. Therefore, the finger photodiode was optimized at the same time for the UV/blue and red spectral ranges by varying the doping concentration of the epitaxial layer C_e. Four different wafers with $C_e = 2 \times 10^{13}\,cm^{-3}$, $C_e = 5 \times 10^{13}\,cm^{-3}$, $C_e = 1 \times 10^{14}\,cm^{-3}$, and $C_e = 1 \times 10^{15}\,cm^{-3}$ were used. For $\lambda = 638$ nm, the 9-finger photodiode had a responsivity of 0.49 A/W (with ARC, independent of C_e). Table 3 summarizes the rise and fall times of the 9-finger photodiode on these wafers. Figure 13 shows a transient response for $\lambda = 638$ nm ($C_e = 2 \times 10^{13}\,cm^{-3}$). Figure 14 shows the transient response for $\lambda = 400$ nm on wafers with $C_e = 2 \times 10^{13}\,cm^{-3}$.

Table 3. Rise and fall times of the 9-finger photodiode on wafers with different epitaxial doping concentrations ($R_L = 0.5\,k\Omega$ for $\lambda = 638$ nm, $R_L = 1\,k\Omega$ for $\lambda = 400$ nm, $V_{PD} = 3$ V) [22]

C_e (cm^{-3})	$t_r^{638\,nm}$ (ns)	$t_f^{638\,nm}$ (ns)	$t_r^{400\,nm}$ (ns)	$t_f^{400\,nm}$ (ns)
2×10^{13}	0.3	0.9	1.3	1.7
5×10^{13}	0.4	1.0	1.2	1.6
1×10^{14}	0.5	2.3	1.1	1.4
1×10^{15}	15.2	16.9	1.0	1.1

It can be seen that the photodiode on standard epitaxial wafers ($C_e = 1 \times 10^{15}\,cm^{-3}$) gives the best results for 400 nm. The reason is, that the space-charge regions of adjacent fingers still meet each other for the 9-finger photodiode for $C_e = 1 \times 10^{15}\,cm^{-3}$. For lower C_e, the space-charge region extends deeper resulting in a lower drift speed and a longer drift distance increasing the rise and fall times.

At 638 nm the 9-finger photodiode with $C_e = 1 \times 10^{15}\,cm^{-3}$ shows a slow response due to the thin space-charge region letting room for slow diffusion. With lower doping concentration the space-charge region extends deeper into the epitaxial layer resulting in a faster response. The difference between the rise and the fall time is more pronounced in the case of red light (see Table 3). This is due to the longer drift distance of the holes generated deep in the

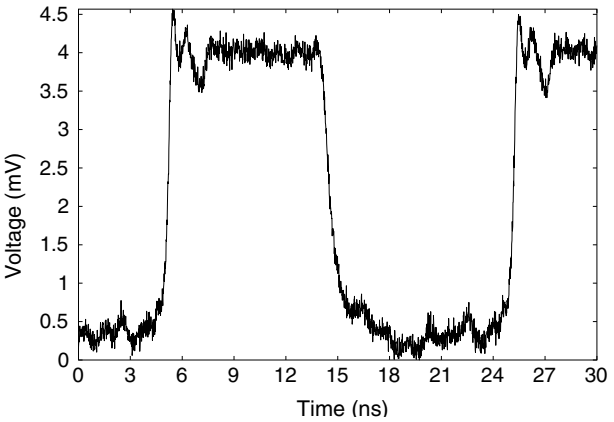

Fig. 13. Transient response of the 9-finger photodiode ($C_e = 2 \times 10^{13}\,cm^{-3}$, $\lambda = 638\,nm$, $R_L = 0.5\,k\Omega$ and $V_{PD} = 3\,V$) [22]

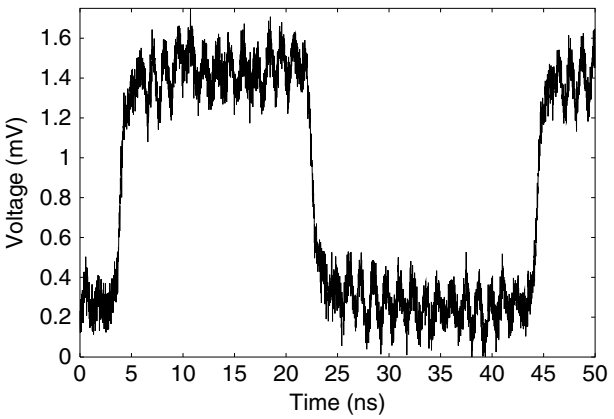

Fig. 14. Transient response of the 9-finger photodiode ($C_e = 2 \times 10^{13}\,cm^{-3}$, $\lambda = 400\,nm$, $R_L = 1\,k\Omega$ and $V_{PD} = 3\,V$) [22]

epitaxial layer to the P^+-anode compared to the lateral drift distance of the holes generated close to the Si surface for $\lambda = 400\,nm$.

The finger photdiodes processed on wafers with a doping concentration of $C_e = 1 \times 10^{14}\,cm^{-3}$ in the epitaxial layer are sensitive and fast enough for todays red and for near-future UV/blue OEICs.

In OEICs for optical storage systems a low offset voltage is required [25]. Therefore the dark current of the photodiode which is connected to the input of the amplifier has to be small. Even for reverse voltages up to 5 V the dark current remains below 1 pA at room temperature for finger photodiodes with an area of $2500\,\mu m^2$ [22]. Therefore, there is no problem with offset voltages.

Let us conclude: with the finger photodiodes the responsivity for a wavelength $\lambda = 400\,nm$ was increased by a factor of 2.8 compared to a conventional

photodiode and rise and fall times of less than 1.1 ns were obtained for the standard epitaxial doping concentration. The finger photodiodes have a responsivity of 0.49 A/W (with ARC) for $\lambda = 638$ nm and rise and fall times of less than 2.3 ns for $C_e \leq 1 \times 10^{14}\,\mathrm{cm}^{-3}$. The finger photodiodes can be integrated in twin-well CMOS-processes with only one additional mask (besides the ARC mask) and are therefore well suited for UV/blue-sensitive OEICs for optical storage systems of the next generation, which are compatible with todays optical storage systems using red light.

3 Examples of Photo-Receiver Circuits

The design of microelectronic integrated circuits is a highly developed area. Circuits for advanced OEICs, however, are not yet investigated thoroughly. In the following, progress in this field will be summarized especially at the examples of OEICs for optical storage systems (OS-OEICs) like DVD and DVR as well as OEICs for receiver applications in optical interconnects, optical data transmission and optical communication.

3.1 OS-OEICS for DVD Applications

The first presented approach requires no process modification to implement a double photodiode (DPD) as shown in Fig. 7. An OEIC with the DPD with a light-sensitive area of about $50 \times 50\,\mu\mathrm{m}^2$ was fabricated in a 0.8 µm BiCMOS process [26].

The circuit diagram of a fast channel (A–D) of the OEIC for optical storage systems (OS-OEIC) is shown in Fig. 15. An integrated DPD is connected to a transimpedance amplifier using an operational amplifier to obtain a low output offset voltage compared to a 2.5 V reference voltage as is required for applications in optical storage systems.

For a universal applicability, the gain is switchable by MOS elements between high (H, R3), medium (M, R4||R3) and low (L, R5||R4||R3) with

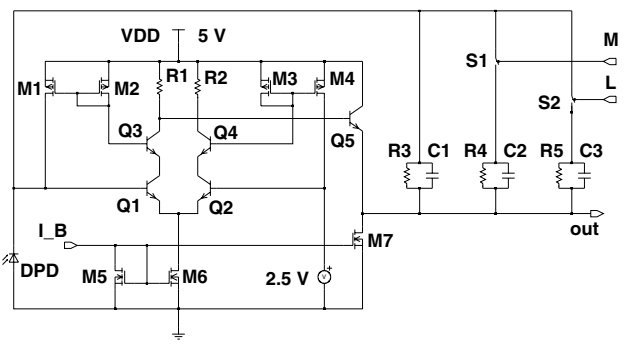

Fig. 15. Schematic of a fast channel amplifier (A–D) in a BiCMOS OS-OEIC [26]

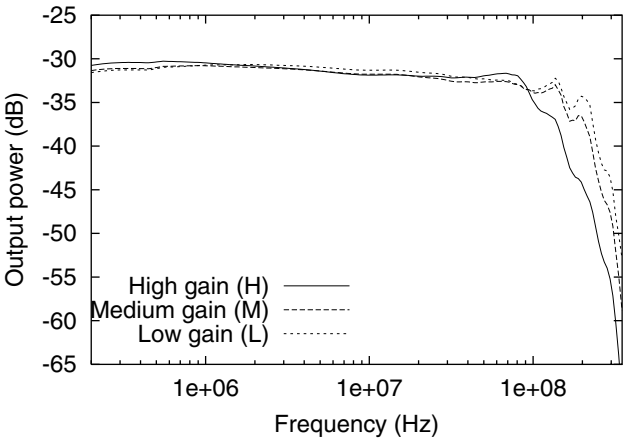

Fig. 16. Frequency response of a fast channel amplifier (A–D) in a BiCMOS OS-OEIC [26]

a ratio of approximately 1/3 each (Fig. 15). Polysilicon-polysilicon-capacitors can be produced in the 0.8 µm BiCMOS process and are used for frequency compensation with C1, C2 and C3. Only NPN transistors were applied in the signal path of operational amplifier to achieve high −3 dB bandwidths. The NPN transistors Q3 and Q4 are used to sense the base current of Q1 and Q2, respectively. These currents are mirrored by the current mirrors M1/M2 and M3/M4 back to the bases of the input transistors Q1 and Q2, respectively. This method is called bias-current cancellation. This biasing of the input transistors Q1 and Q2 reduces the systematic output offset of approximately 110 mV, which would result from the base current of Q1 across the largest resistor R3 = 20 kΩ, by more than one order of magnitude. The low-frequency open-loop gain of the operational amplifier was 27 dB and its transit frequency was 870 MHz with a 1 kΩ and 10 pF load. An OEIC was packaged, mounted on a printed circuit board together with these load elements, and a probe head with an input capacitance of 1.7 pF is used to measure the frequency response shown in Fig. 16.

The measured bandwidths exceeded 92 MHz, which was much larger than the bandwidth value 7.3 MHz of the circuit for 8× speed CD-ROMs fabricated in 0.8 µm CMOS technology with off-chip photodiodes [27].

The four sensitive channels E–H have a ten times larger sensitivity for tracking control in the optical storage system. A double photodiode with approximately twice the size of the DPDs in the channels A–D was implemented here. 90 mV/µW sensitivity in combination with a low offset voltage was realized. Each amplifier of channels A–H covered an active area of approximately 0.079 mm^2. The total OEIC die area was 3.25 mm^2. The power consumption of the OS-OEIC was less than 75 mW at 5.0 V. Table 4 summarizes the properties of the OS-OEIC channels A–H.

Table 4. Measured results of the high-bandwidth OS-BiCMOS-OEIC

	H	M	L
$f_{-3\,\mathrm{dB}}$ (MHz) A–D	92.0	94.9	95.1
$f_{-3\,\mathrm{dB}}$ (MHz) E–H	5.2	8.5	14.6
Sensitivity (mV/μW) A–D	8.8	2.9	0.9
Sensitivity (mV/μW) E–H	88.1	29.3	9.1
U_{Offset} (mV) A–D	< 10.8	< 9.5	< 9.0
U_{Offset} (mV) E–H	< 7.4	< 6.4	< 6.4
Noise (dBm) at 10 MHz with 30 kHz RBW A–D	−81.5	−85.0	−85.2
Noise (dBm) E–H	−66.0	−67.5	−73.5

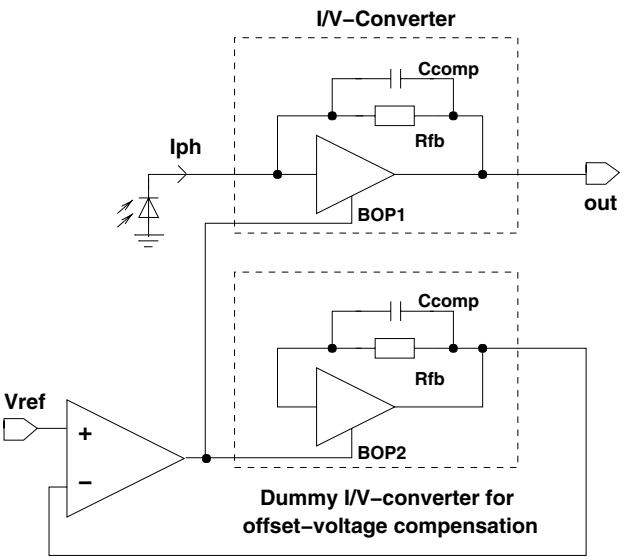

Fig. 17. Basic topology for output offset voltage reduction [28]

The next shown circuit topology implements transistor transimpedance amplifiers instead of operational amplifiers in transimpedance configuration. The innovative topology of this OEIC for optical storage systems is shown in Fig. 17. A current-to-voltage converter is connected to the integrated photodiode. The BOP1 (bias operating point) input allows to correct the operating point of this transimpedance amplifier in order to cancel the output offset voltage.

For this purpose an identical dummy current-to-voltage converter with an open input and a low-offset operational amplifier are integrated together with the transimpedance amplifier connected to the photodiode. The operational amplifier measures the output offset voltage of the dummy current-to-voltage (I/V) converter compared to $V_{\mathrm{ref}} = 2.1\,\mathrm{V}$ and changes its operation

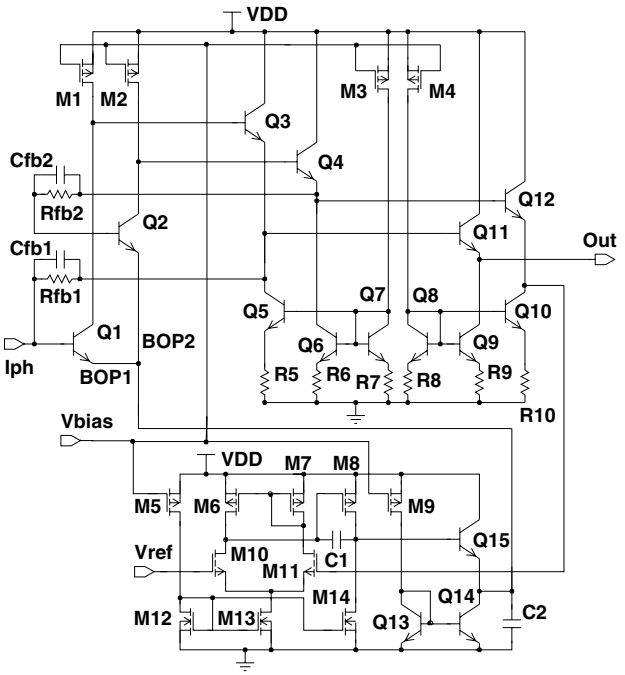

Fig. 18. Schematic diagram of one BiCMOS OS-OEIC channel

point via the BOP2 input in order to minimize the output offset voltage. The BOP1 input of the actual transimpedance amplifier is also connected to the output of the operational amplifier. In such a way, the output offset voltage of the transimpedance amplifier can be reduced provided that a good matching between the two I/V converters and a low offset voltage of the operational amplifier can be guaranteed. The first requirement can be dealt with a careful layout reducing the distance between corresponding devices in the two I/V converters. The second requirement can be fulfilled, because the operational amplifier can be designed to have a very slow response, i.e. transistors with a large emitter area or large gate lengths and widths for a good matching can be used.

An OEIC containing four fast channels (for data extraction) and four sensitive channels (for tracking control in the optical storage system) with Rfb $\approx 60\,\mathrm{k}\Omega$ values was fabricated in a $0.8\,\mu\mathrm{m}$ BiCMOS technology. The N-well/P-substrate photodiode was implemented with a light sensitive area of $2500\,\mu\mathrm{m}^2$ in the fast channels and $9100\,\mu\mathrm{m}^2$ in the sensitive channels.

The schematic diagram of the fast and sensitive channels of the BiCMOS OEIC is shown in Fig. 18. The transistor transimpedance amplifier is formed by Q1 in common-emitter configuration, the PMOS load element M1, the emitter follower Q3, and the feedback resistor Rfb1. Q3 provides a low output impedance of this input stage. The capacitor Cfb1 is used for com-

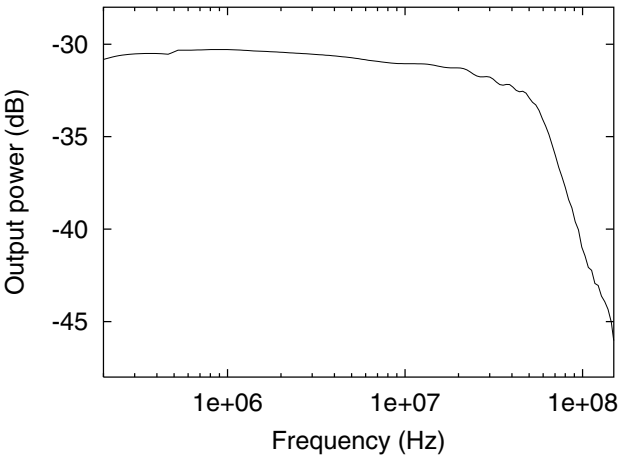

Fig. 19. Frequency response of fast channel of BiCMOS OS-OEIC [26]

pensation. The emitter follower Q11 decouples the feedback path from the output and provides a low overall output impedance. The dummy I/V converter is formed by Q2, M2, Q4, Rfb2, Cfb2 and Q12. Q5–Q10, R5–R10 and M3/M4 are used for biasing. The circuit diagram in Fig. 18 corresponds to the interlaced layout for good matching of the two I/V converters.

The BiCMOS operational amplifier is based on a CMOS Miller type topology with the NPN emitter follower Q15 at the output in order to supply a voltage source with a low output resistance for the emitter inputs BOP of the two I/V converters. The simulated open-loop gain of the operational amplifier was 77 dB and its transit frequency was 7.3 MHz.

A sensitivity for the fast channel of 25 mV/μW and of 51 mV/μW for the sensitive channels at 638 nm was found by determining the incident light power with a calibrated photodiode. A −3 dB frequency of 58.5 MHz was measured for a fast channel with a load of 10 kΩ and 10 pF (Fig. 19). The sensitive channels showed a −3 dB frequency of 26.7 MHz with the same load. All measured output offset voltages for photodiodes and OEICs in the dark were lower than 7.5 mV. This value is considerably lower than in the maximum simulated offset voltage of a reference amplifier without offset compensation of more than 72 mV for worst case transistor parameters at room temperature.

It should be mentioned that the BiCMOS operational amplifier and the emitter BOP inputs reduce the bandwidth of the I/V converters. The output resistance of the BiCMOS operational amplifier, however, is obviously rather low, since the bandwidth of 58 MHz is not considerably lower than that of a reference I/V converter of 82 MHz where the emitter of Q1 was connected to V_{ref} directly.

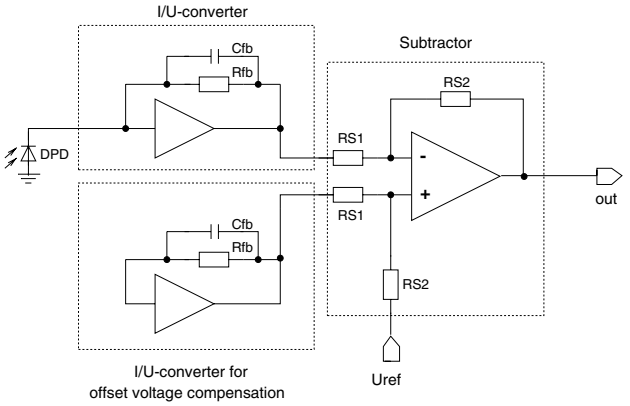

Fig. 20. Block diagram of a two-stage optical receiver for a fast channel of a high-speed OS-BiCMOS-OEIC

The bandwidth of the N-well/P-substrate photodiode may seem to be rather high compared to [7] where a bandwidth of 1.6 MHz was reported for a similar photodiode for $\lambda = 780\,\text{nm}$. The high bandwidth determined here, however, can be explained by the shorter wavelength and by an electric field, i.e. by a drift zone for photogenerated carriers, due to the doping gradient of the N-well similarly to that in the N-well of a double photodiode [29].

Noise measurements at 10 MHz with a resolution bandwidth of 30 kHz revealed values of $-76\,\text{dB}\cdot\text{m}$and $-65\,\text{dB}\cdot\text{m}$for the fast and sensitive channels, respectively. The power consumption determined by simulation was 36 mW for a fast channel at a supply voltage of 5.0 V. The active die area of each channel was approximately $0.042\,\mu\text{m}^2$ and the total chip area was $3.1\,\text{mm}^2$.

When a high speed and a higher sensitivity are required in addition to a lower output offset voltage for the OS-OEICs, a two-stage optical receiver may be necessary. The circuit principle of such a two-stage amplifier [30, 31] is shown in Fig. 20.

The circuit consists of a transimpedance amplifier for the photocurrent and a reference I/V converter for offset compensation plus an operational amplifier in subtractor configuration. The subtractor can also be used as a voltage amplifier with the amplification factor RS2/RS1 enabling a high overall sensitivity of the OEIC. It has be mentioned, however, that offset voltages due to mismatch of the two transimpedance preamplifiers are also amplified. The circuit diagram of the complete circuit is shown in Fig. 21.

In order to achieve a high bandwidth, only NPN transistors are used in the signal paths of the preamplifiers. Q1 is used in common-emitter configuration, Q3 is used as emitter follower, and the feedback resistor Rfb1 together with Q1 and Q3 represents a low input impedance for the photocurrent of the double photodiode (DPD).

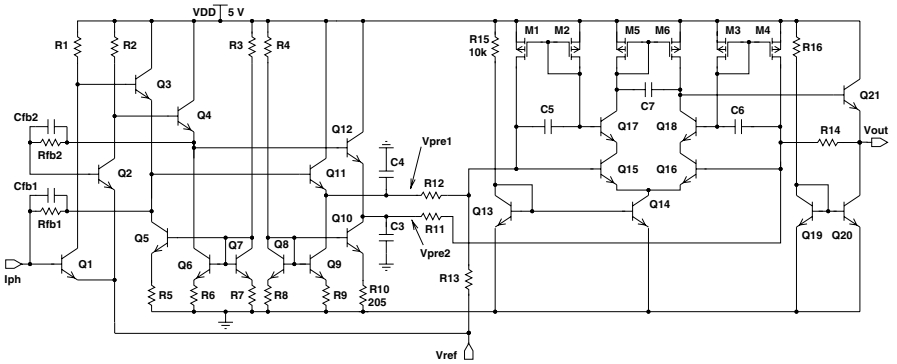

Fig. 21. Schematic of high-speed BiCMOS-OEIC for the fast channels A–D in an OS-BiCMOS-OEIC

Thereby, the effect of the DPD capacitance is minimized. The reference voltage V_{ref} is chosen as the emitter potential of Q1 in order to increase the reverse voltage of the DPD to $V_{\mathrm{BE,Q1}} + V_{\mathrm{ref}}$. The values for R1, Rfb1 and Cfb1 were 3 kΩ, 27 kΩ and 25 fF, respectively. A second emitter follower (Q11) is implemented for level shifting and decoupling of output and feedback path. The second preamplifier consists of transistors Q2, Q4 and Q7 and the feedback resistor Rfb2 plus the compensation capacitor Cfb2. At the outputs of the preamplifier, C3 and C4 are added as further compensation capacitors.

Perfect matching of the two preamplifiers is necessary in order to obtain $V_{\mathrm{pre1}} = V_{\mathrm{pre2}}$ for a dark photodiode (Fig. 21). This perfect matching of the two preamplifiers requires a careful layout to achieve a low output offset voltage.

The preamplifiers are connected to the operational amplifier in subtractor configuration via R_{11} and R_{12}. The bias current cancellation introduced in Fig. 15 is applied to reduce the input currents of the operational amplifier enabling a low output offset voltage. A PMOS current mirror load with M5 and M6 is used here in order to obtain a higher open loop gain of the operational amplifier. For $\mathrm{R}_{11} = \mathrm{R}_{12}$ and $\mathrm{R}_{13} = \mathrm{R}_{14}$, an analysis of the subtractor amplifier yields the transfer function

$$V_{\mathrm{out}} \approx V_{\mathrm{ref}} + \frac{R13}{R12} I\mathrm{ph} R\mathrm{fb1}$$

when we assume a large open-loop voltage gain of the operational amplifier. A −3 dB frequency of 189 MHz was determined by numerical prelayout simulation for the complete amplifier with a load of $\mathrm{R_L} = 1\,\mathrm{k\Omega}$ and $\mathrm{C_L} = 10\,\mathrm{pF}$. The complete two-stage amplifier was designed for a sensitivity of 10 mV/μW and an offset voltage less than 10 mV for R11 = R12 = R13 = R14.

The OEIC with the DPD and the two-stage amplifier was fabricated in a 0.8 μm BiCMOS technology. The measured frequency response of this two-stage optical receiver is shown in Fig. 22. A −3 dB frequency of 147.7 MHz

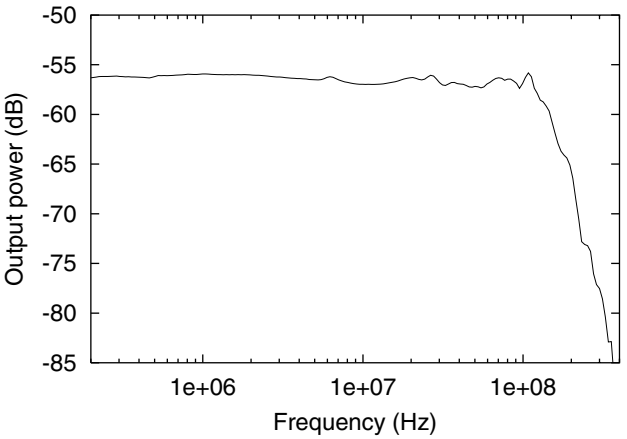

Fig. 22. Frequency response of a two-stage optical BiCMOS receiver for the fast channels A–D of a high-speed BiCMOS-OEIC for optical storage systems [28]

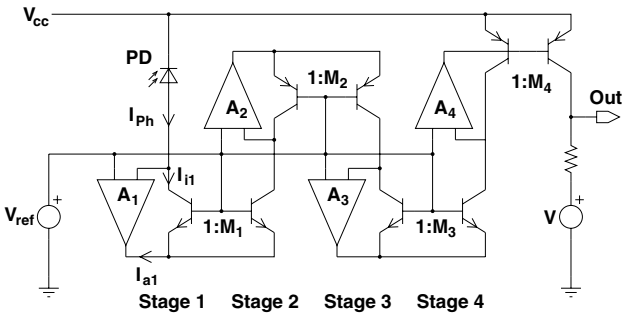

Fig. 23. Circuit topology of one segment in the fast OEIC for optical storage systems [32]

is determined from this frequency response. The power consumption of the two-stage optical receiver was 35 mW at a supply voltage of 5 V. The active die area of the two-stage optical receiver was 340 µm × 140 µm.

An even faster OEIC for optical storage systems has been presented recently. A bandwidth of 250 MHz has been achieved with a four-stage current amplifier in a standard 0.6 µm BiCMOS technology [32]. This OEIC can be used for channel data rates up to 600 Mb/s corresponding to 22× DVD speed with 12 000 rpm. The photodiode of this OEIC was optimized to a low capacitance of 0.25 pF. Nevertheless, the high bandwidth is an astonishing result when we consider that no bias currents were superimposed to the photocurrents to reduce the offset of the amplifiers. Lowest power consumption, therefore, also could be achieved. Figure 23 shows the topology of the current preamplifier used in the 8-channel OEIC.

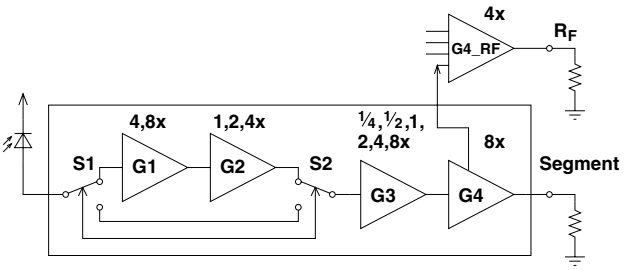

Fig. 24. Gain partitioning of one segment in the fast OEIC for optical storage systems [32]

Since the gain-bandwidth product of the BiCMOS process used was 400 GHz and a gain over 1000 was needed, a four-stage amplifier with a bandwith of at least 400 MHz for each stage was necessary. The transistors in Fig. 23 form current dividers for the output currents of the transconductance (V/I) amplifiers A1–A4. The loops are closed over one arm of the current dividers.

The gain was switchable implementing MOS switchees between and in the stages from 2 to 2048 for different laser powers during read and write as well as for different media according to the scheme illustrated in Fig. 24.

A summation amplifier (RF amplifier) for the channels A–D was implemented. The bandwidth of this RF amplifier only weakly depended on the gain. The gain of the satellite amplifiers in channels E–H was always four times higher than shown in Fig. 24.

It has to be mentioned that a trick was necessary to achieve the high bandwidth for low photocurrents, since photocurrents of 100 nA to 1 µA caused the transit frequencies of the NPN transistors T1 and T2 to drop to tens of kHz to 1 MHz [32]. The large attenuation resulting at 400 MHz hat to be eliminated. This was done by bypass capacitors, which were not shown in the circuit diagram however. The V/I amplifiers A1 to A4 used NMOS input transistors to avoid base input currents, their DC-current offset, and their base current shot noise. Gain peaking around 200 MHz was caused by crosstalk between the output drivers and the first two stages. It was stated that this problem can be solved in a redesign by separated front-end and back-end supplies.

The output stage delivered a current of 8 mA into a 150 Ω load with a one-sigma offset value of 117 µV.

3.2 Fiber Receivers

First, we demonstrate an innovative monolithic integration of vertical PIN photodiodes in a twin-well CMOS process (Fig. 9), which uses epitaxial wafers, in order to combine the high speed and the large quantum efficiency of the photodiode [33]. In contrast to the OEICs of [34,35], here, only a single

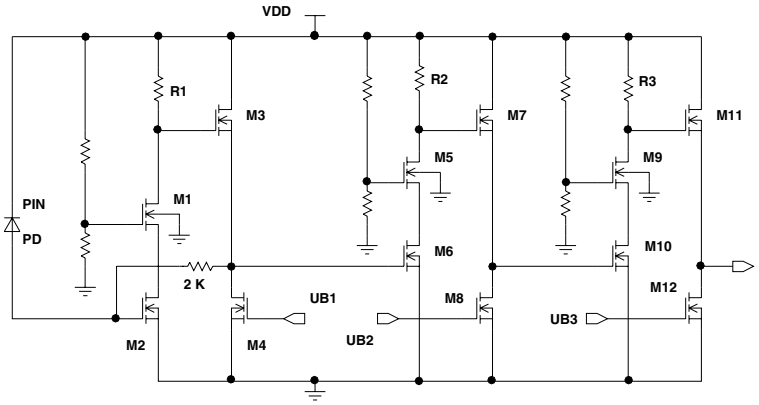

Fig. 25. Circuit of a fiber receiver OEIC [33]

power supply of 2.5 V, 3.3 V, of 5 V is needed. The integration of PIN photodiodes in a twin-well CMOS technology requires much less additional process complexity than the published approaches to standard-buried-collector (SBC) based bipolar OEICs [21, 36]. Three additional masks were necessary for the PIN-bipolar integration and for the avoidance of the Kirk effect. Only one photodiode protection mask is added for the PIN-CMOS integration in order to block out an originally unmasked threshold implantation from the photodiode area. This additional mask seems to be justified due to the expected high volumes of OEICs and OPTO-ASICs.

The PIN-CMOS photodiodes with an area of 2700 µm^2, a doping concentration C_e in the epitaxial layer of 2×10^{13} cm^{-3}, and an integration polysilicon resistor of 500 Ω, as well as complete OEICs, were fabricated in an industrial 1.0 µm CMOS process. Reference samples both for the photodiodes and OEICs with the standard doping concentration $C_e = 10^{15}$ cm^{-3} were also fabricated. The measurements on the PIN photodiodes and their results were described in the Chapter by *Paniccia* et al.

The circuit of a high-speed preamplifier with an integrated PIN photodiode is shown in Fig. 25. The cascode transistors M1, M5, and M9 reduce the Miller effect and increase the bandwidth correspondingly. The input stage with transistors M1–M4 is a transimpedance configuration, which converts the photocurrent change in the integrated PIN photodiode to a voltage change. The source followers M3, M7 and M11 as well as the current sources M4, M8 and M12 are used for level shifting. The threshold voltage of transistors M3, M7 and M11 was reduced intentionally to about 0.4 V by the photodiode protection mask in order to obtain lower V_{GS} values. Due to the feedback across the 2 kΩ resistor and to the identical dimensions of the transistors in the different stages, a good independence from process deviations within the relatively large specified process tolerances of the used digital CMOS process was obtained. Three identical biasing circuits (UB1 = UB2 = UB3)

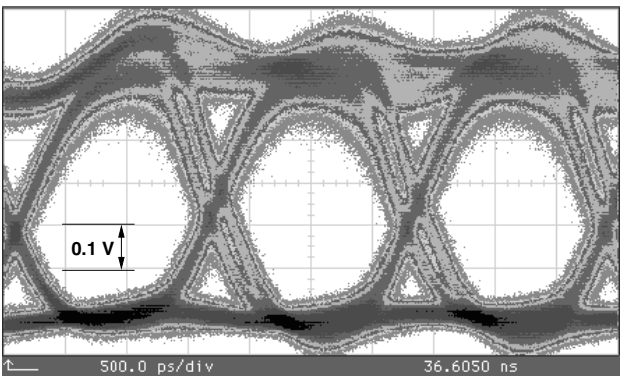

Fig. 26. Eye diagram of the CMOS preamplifier OEIC for a data rate of 622 Mb/s (500 ps/div; 0.1 V/div)

were used instead of one in order to avoid parasitic coupling between the stages. The sensitivity of the PIN amplifier OEIC was 4.7 mV/μW increasing to 9.0 mV/μW with ARC, which corresponds to an overall transimpedance of 18.4 kΩ. Its power consumption was 44 mW at 5.0 V reducing to 17 mW at 3.3 V and to 9 mW at 2.5 V. The photodiode together with its metal shield around covered an area of approximately 150 μm × 150 μm. The preamplifier occupied an active area of less than 190 μm × 200 μm.

The rise and fall times for the OEIC with the epitaxial doping concentration $C_e = 10^{15}\,\mathrm{cm}^{-3}$ were $t_r = 15.5$ ns and $t_f = 17.6$ ns. These large values for t_r and t_f were due to the slow carrier diffusion in the standard epitaxial layer of the photodiode. The corresponding values for the doping concentration $2 \times 10^{13}\,\mathrm{cm}^{-3}$ in the epitaxial layer, where the depletion region spread through the whole epitaxial layer and carrier diffusion in the photodiode was eliminated, were 0.53 ns and 0.69 ns, respectively. These values indicate that CMOS OEICs with a reduced doping concentration in the epitaxial layer having an appropriate output buffer can be used as receivers for optical data transmission via fibers or for optical interconnects on a board level up to a bit rate (BR) of 622 Mb/s in the non-return-to-zero (NRZ) mode, verified by a measured eye diagram with pseudo random bit sequences (PRBS) of $2^{23} - 1$ (Fig. 26).

The next fiber receiver described used PIN photodiodes in the same 1.0 μm CMOS process also with a reduced doping concentration in the epitaxial layer. The high-speed preamplifier circuit is shown in Fig. 27. Only N-channel MOSFETs with a minimum channel lengths were used in order to achieve a high bandwidth. The transistors M1–M5 operate in common-source configuration. The input stage with M1 in transimpedance configuration converts changes in the photocurrent of the photodiode to voltage changes. The feedback resistor in the input stage is formed by gate polysilicon. Two further stages with two transistors each are used as voltage amplifiers. The polysil-

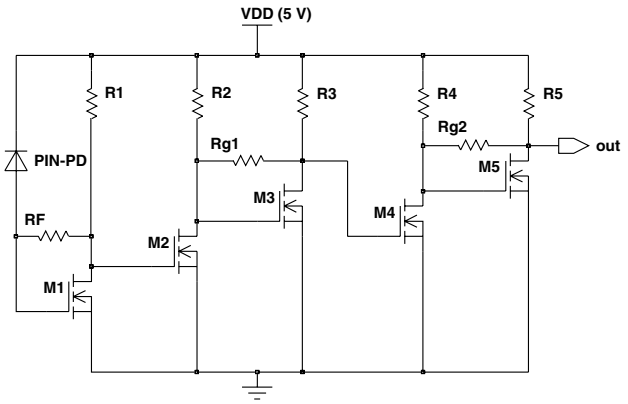

Fig. 27. Circuit of a fiber receiver OEIC [37]

icon feedback resistor in each of the two stages (Rg1, Rg2) limits the gain and therefore boosts the bandwidth. Due to the feedback resistors, a good independence from process deviations within the relatively large specified process tolerances of the used digital CMOS process is obtained. The sensitivity of the PIN preamplifier OEIC was 13.8 mV/μW without ARC, which corresponds to an overall transimpedance of 45.9 kΩ. Compared to the above-mentioned receiver, the sensitivity of the new OEIC has been increased by a factor of more than 2.5. Its power consumption is 2.5 mW at 5.0 V. The photodiode has an area of 2700 μm^2. The preamplifier occupies an active area of 245 μm × 140 μm due to the large area necessary for the resistors formed by low-resistivity (gate) polysilicon.

The rise and fall times measured at the OEIC output with the picoprobe were 0.72 ns and 0.57 ns, respectively, with a supply voltage of 5.0 V. With these values a bandwidth of $f_{-3\,\mathrm{dB}} = 2.2/(\pi(t_\mathrm{r} + t_\mathrm{f})) = 550\,\mathrm{MHz}$ can be estimated for the OEIC. The higher data rate of this OEIC is due to less transistors in the preamplifier than in the typical high-frequency circuit with cascode transistors and source followers described before. In the above-mentioned receiver, 12 NMOS transistors were used in the preamplifier, which therefore contained more parasitic capacitanes. Here, the number of parasitic capacitances is considerably lower. In addition, the gain per amplifying transistor is lower here, allowing for a higher data rate of the new preamplifier.

The so-called Q-factor is defined as $(B_1 - B_0)/(\sigma_1 + \sigma_0)$ [38], where B_1 and B_0 are the mean values and σ_1 and σ_0 are the standard deviations of the output signal for a "1" and "0". B_1, B_0, σ_1 and σ_0 can be determined from eye diagram measurements.

The bit error rate (BER) then is available from [38]: $\mathrm{BER} \approx e^{-\frac{Q^2}{2}}/Q\sqrt{2\pi}$. The BER of the OEIC has been determined with an HP 54570/51 digital sampling oscilloscope for the NRZ data rates of 622 Mb/s and 1 Gb/s in dependence on the optical input power. The results for the bit error rate

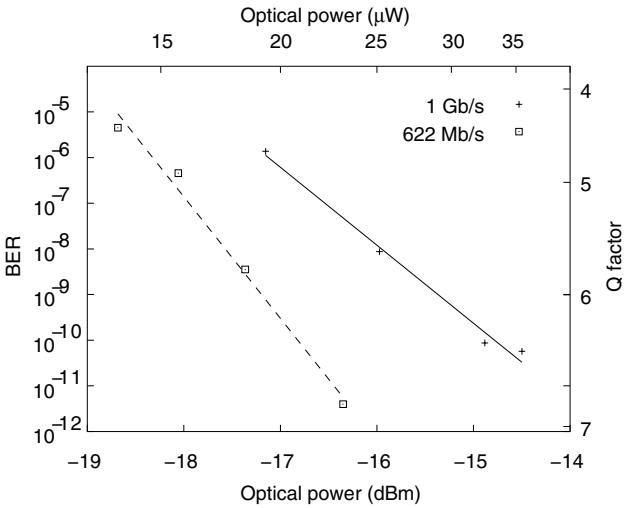

Fig. 28. BER of PIN OEIC without ARC in dependence on the optical input power at 638 nm

are shown in Fig. 28. From this diagram for $\lambda = 638\,\text{nm}$ being especially interesting for data transmission via plastic optical fibers and for optical interconnects, it can be seen that an optical input power of $-15.4\,\text{dB}\cdot\text{m}$ is necessary for a BER of 10^{-9} at a data rate of 1 Gb/s. At 622 Mb/s the sensitivity of the OEIC for the same BER is $-17.2\,\text{dB}\cdot\text{m}$. The sensitivity for a BER of 10^{-10} at a data rate of 1 Gb/s is $-14.8\,\text{dB}\cdot\text{m}$. The sensitivity for a BER of 10^{-11} at a data rate of 622 Mb/s is $-16.5\,\text{dB}\cdot\text{m}$. For $\lambda = 850\,\text{nm}$, a sensitivity of $-15.3\,\text{dB}\cdot\text{m}$ for a BER of 10^{-9} at a data rate of 622 Mb/s has been verified.

These values are very good results for an OEIC in a 1.0 μm CMOS technology. The overall transimpedance of 46 kΩ and the data rate of 1 Gb/s result in a $46\,\text{Tb}\cdot\Omega/\text{s}$ transimpedance data rate product. With the bandwidth of 550 MHz, a $25\,\text{THz}\cdot\Omega$ effective transimpedance product results, which exceeds the value of $18\,\text{THz}\cdot\Omega$ reported in [39]. The sensitivity of the PIN CMOS OEIC for a data rate of 1 Gb/s and a BER of 10^{-9} with a value of $-15.4\,\text{dB}\cdot\text{m}$ for 638 nm exceeds the sensitivity of $-6.3\,\text{dB}\cdot\text{m}$ of a 0.35 μm OEIC for 850 nm [35] by a factor of 8. It shall be mentioned that the implementation of an antireflection coating will improve the sensitivity of the OEICs by a value of 2 dB–3 dB. The minimum sensitivity of $-17\,\text{dB}\cdot\text{m}$ specified in the Gigabit Ethernet networking standard, therefore, may be achievable with PIN CMOS OEICs. The data rate of the OEIC is limited by the amplifier in a 1.0 μm technology. With submicrometer PIN-CMOS-OEICs data rates in excess of 1 Gb/s are possible.

The circuit diagram for a receiver with a SOI PIN photodiode (Fig. 6) is shown in Fig. 29. Optimum results were obtained for input transistors

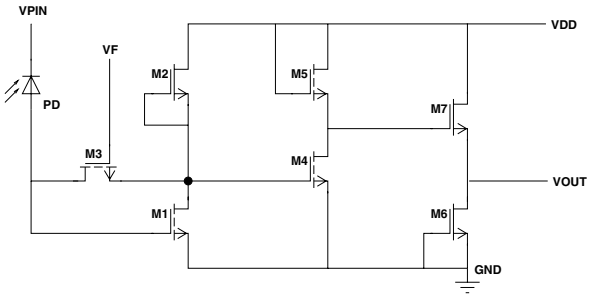

Fig. 29. Circuit diagram of the SOI receiver [13]

(M1–M2) with 50 µm widths for the SOI receiver. The functionality of the three-stage amplifier has been described in [14]. The small-signal transfer function of this design is discussed in [13].

At $V_{DD} = 5\,V$ and $V_{PD} = 20\,V$, for 850 nm and a BER $= 10^{-9}$, the sensitivity of the SOI receiver was $-26.1\,dB \cdot m$ at 622 Mb/s, $-20.2\,dB \cdot m$ at 1.0 Gb/s as well as $-12.2\,dB \cdot m$ at 2.0 Gb/s. The dependence of the sensitivity on the photodiode voltage was also investigated. The SOI receiver demonstrated a penalty that was typically less than 1 dB as the photodiode supply was reduced to 10 V. For single-supply 5 V operation, the sensitivity degraded by 2.8 dB to 3.9 dB and the maximum data rate was 1.5 Gb/s with a sensitivity of $-12\,dB \cdot m$.

The dynamic range of the receivers was measured with both a constant voltage supply and with a variable feedback voltage (V_F) as a simple form of automatic gain control (AGC). The photodiode bias has a large impact on the dynamic range, although the feedback voltage can be used very effectively to compensate for this degradation. At the optimum bias point and a constant V_F, the SOI receiver exhibited dynamic ranges of $> 23.5\,dB \cdot m$, $> 17.7\,dB \cdot m$, and $12.0\,dB \cdot m$ at 622 Mb/s, 1.0 Gb/s and 2.0 Gb/s.

This receiver was not optimized for the best sensitivity at the higher data rates. The dominant noise term was thermal noise of the feedback resistor (M_F) and not the channel noise of the input transistor. Better performance is possible with an optimized circuit design in a more advanced technology.

4 Conclusion

Double photodiode, vertical PIN photodiode, and lateral SOI photodiode avoid slow carrier diffusion effects. The performance of integrated photodiodes can be improved significantly when minor process changes are made to obtain these advanced integrated photodiodes. Finger photodiodes, another advanced approach, are very good appropriate for application together with blue light in near future DVR systems.

Advanced OEICs for optical storage systems have been realized. These low-offset solutions have bandwidths ranging from 58 MHz to 250 MHz. Furthermore, high-speed fiber receiver OEICs have been presented. PIN CMOS OEICs reach sensitivities of $-17.2\,\mathrm{dB\cdot m}$ at 622 Mb/s and $-15.4\,\mathrm{dB\cdot m}$ at 1 Gb/s (BER = 10^{-9}) with a single 5 V supply voltage. Using higher photodiode bias voltages, the SOI receiver reaches sensitivities of $-20.2\,\mathrm{dB\cdot m}$ at 1 Gb/s and $-12.2\,\mathrm{dB\cdot m}$ at 2 Gb/s. The speed of integrated photodiodes and of amplifiers can be increased with sub-μm technologies. Then receivers for Gigabit Ethernet and the Fiber Channel working with 850 nm light, for instance, can be realized with Si OEICs.

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