Monolithic Silicon Microphotonics

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Abstract. The technology evolution of optical interconnection is driven by the distance × bandwidth product required for a given link. As such optical fiber deployment in telecommunications has become the dominant paradigm since the early 1980s. Today, with excess telecommunications capacity, optical interconnection is driven by data communications needs throughout the interconnection hierarchy, from the network to the chip. Silicon Microphotonics is the only current approach that offers a scalable solution to the anticipated barriers of I/O density, interconnection bandwidth and latency, and electronic/photonic partitioning through monolithic integration. This chapter reviews the drivers, barriers and current solutions for the development and deployment of a monolithic silicon microphotonic technology. Light sources, photodetectors, waveguides, photonic filters, optical amplifiers and photonic crystals are discussed in the contexts of materials design and systems applications.

1 Introduction

1.1 The Silicon Paradigm

The legacy of Silicon Microelectronics has made silicon the most studied material in the history of civilization. As one of the most abundant elements on the earth's crust, and as the basis of a $250B semiconductor industry, silicon (Si) has become more pervasive than steel in its affect on quality of life. Silicon integrated circuits have provided the computation capacity that created the Information Age. The keys to the success of silicon in Microelectronics have been 1. compatible, multifunctional materials: Si, SiO_2, Al; 2. scalable, planar device interconnection; and 3. integrated vs. single component process yield management. With these tools in place, the variable of technology shrink has produced faster, lower cost components with each new generation. This technology shrink has progressed with the help of a Roadmap [1] that coordinates materials, processing and design for successive generations. The Roadmap (ITRS) projects that the benefits of continued scaling will be limited by the performance and complexity of interconnects when the device density is $> 10^7$ devices/chip.

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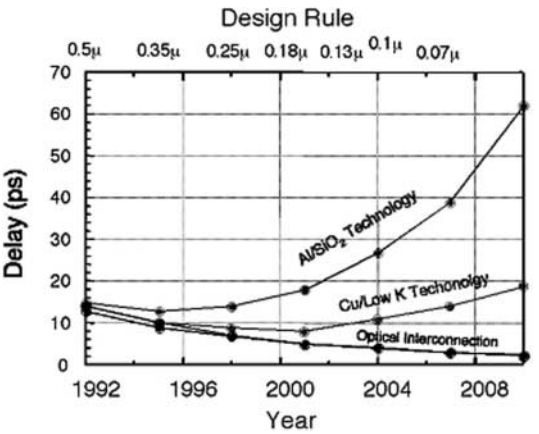

Fig. 1. Trend in interconnect propagation delay (1 cm length) with technology linewidth and time for traditional aluminium metal and SiO2 insulator; projected copper and low-k dielectric; and projected optical waveguide technologies [2]

1.2 The Interconnect Bottleneck

The 'interconnect bottleneck', is an RC circuit delay occurring due to the smaller cross-section and closer spacing of conducting metal lines above the integrated circuit chip. In addition, these metal interconnects account for the majority of chip power dissipation,information latency and cross talk noise. Figure 1 shows that while aluminum-based interconnect technology reached a performance limit at the 0.55 μm lithographic technology node, the introduction of copper conductors to reduce resistance and low-k dielectrics to reduce capacitance has sustained a performance improvement limit up to 0.18 μm [2].

Silicon microphotonics represents a potential solution to the resistance and capacitance limitations of traditional metal interconnects. Using photons as bits of information instead of electrons, enormous transfer rates due to the high frequencies of optical carrier waves can be achieved. In addition, since photons are electrically neutral massless particles, they propagate in transparent media with negligible heat dissipation and no cross talk. A silicon based optical interconnection technology has the appeal of a well understood materials and process technology with the performance advantage of optics.

1.3 A Roadmap for Communication Technology

The distance × data rate product is the performance metric for point-to-point communications. Twisted pair electronic conductors has provided the bandwidth for interpersonal voice communication with enhanced distance. As the number of users increased it became necessary to compress bandwidth/user and multiplex multiple users on a single twisted pair line.

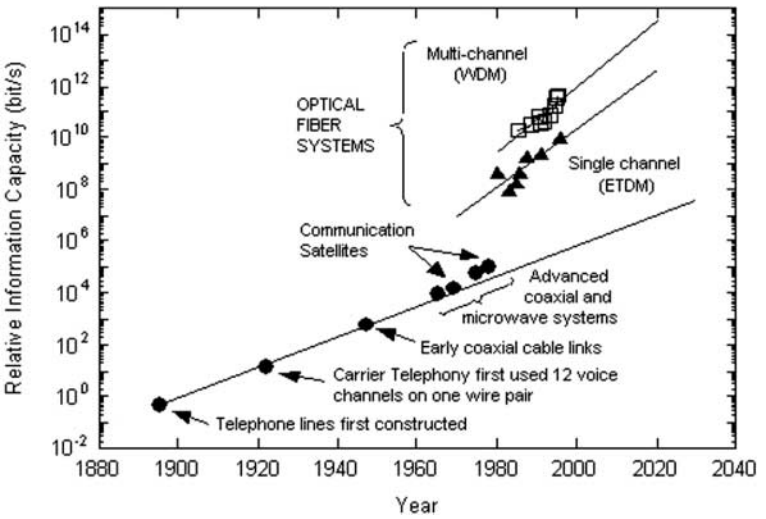

Fig. 2. Growth in information carrying capacity of a single communications line [3]

This capacity growth increased at a remarkable semi-logarithmic rate as coaxial cable, microwave and satellite platforms were adopted. The fiber platform for ligthwave communications represented the first deviation from this trend. The crossover from electronic to optical communication (see Fig. 2) occurred at the distance × bandwidth product of $\sim$ 10 Mb/s × km. This performance metric scales to 1 Tb/s × cm for local interconnection. The characteristics of this cross-over are both a discontinuous increase in performance and change of slope to a sustainable increase in performance/cost of 100 × /10 years [3].

1.4 Photonic Interconnection

The use of photonic interconnection has revolutionized telecommunication systems with the deployment of low-loss, single mode silica fibers, efficient photodetectors and double heterostructure, single mode injection lasers. Long haul fiber optic systems were ultimately enabled with the development of erbium-doped fiber amplifiers (EDFAs), operating around the 1.55 μm fiber transparency window, dubbed the C-band.

Present optical networks contain several optoelectronic components such as lasers, modulators, detectors, beam splitters and multiplexers all connected by glass fibers. This long haul component paradigm does not translate well to higher complexity and functionality at shorter distances.

A significant reduction in costs and system size can be reached by the development of Microphotonics, in which all the optical components are arranged on a single silicon substrate, resulting in an optoelectronic integrated circuit (OEIC). On an integrated optical chip, light is directed through optical

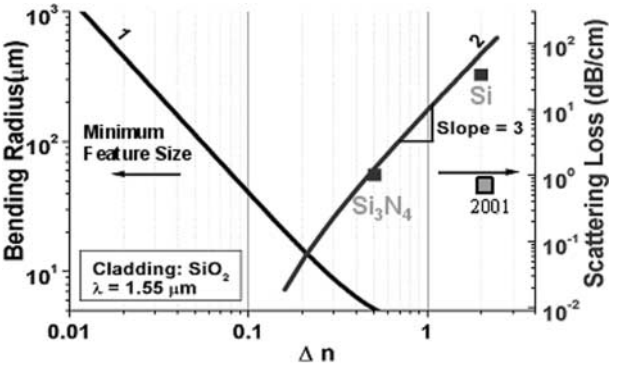

Fig. 3. Dimensional scaling for microphotonic component with index difference Δn and the consequent increase in scattering loss with with current pattern transfer technology [5]

circuits by means of planar waveguides, fabricated on silicon with standard lithographic techniques.

These micron-scale structures present a convergence of solutions for both the interconnect bottleneck problem, and the MAN requirement of low-cost high volume components. At present there are two main approaches to achieve silicon OEICs: hybrid and monolithic integration. Since silicon is a poor light emitter, the hybrid approach tends to combine efficient light emitting III–V semiconductor materials or device components by expensive bonding technologies to Si substrates. In the monolithic approach, III–V and Si based light emitting materials are integrated by sequential deposition, growth and pattern transfer onto Si substrates, producing a complete set of optoelecrtronic functionalities [4].

1.5 Microphotonic Integrated Circuits

It is generally accepted that optical devices will scale to larger dimensions than electrical devices due to the size of the photon relative to that of the electron in a medium. However, this ultimate limitation should not hinder the integration of microphotonic components with current ULSI electronic circuits, and it will likely not affect the ultimate architecture and applications of optoelectronic integrated circuits (OEICs). Current Planar ligthwave Circuits (PLCs) are constructed of lightly doped SiO_2 waveguides with index contrast ($\Delta n = 0.005$) closely matching that of the long haul, optical fiber that feed signals to them. The core dimension is about 10 μm and the cladding is about 20 μm on either side, resulting in a total film thickness approaching 50 μm.

While this design serves the constraint of low loss, it does not meet the critical microphotonics requirement of small bend radius and silicon CMOS compatibility. High Index Contrast (HIC) design is consistent with 1 μm turn

radii and total film thicknesses of $< 5\,\mu m$. These results meet both the performance and fabrication targets for a low cost, high functionality platform. Figure 3 gives a representation of the scaling law for silicon compatible HIC design. As Δn approaches 1 the minimum device dimension falls below 10 μm, and scattering loss from edge roughness becomes a dominant concern. The data for silicon nitride and silicon waveguides are taken post-lithography and match the theoretical (solid line) expectation. The data point labelled 2001 represents the measured result achieved by post-lithography processing (oxidation smoothing) [6]. The challenge is to bring the scattering loss line down by process innovation to realize radiation limited (bending loss) performance. The propagation loss target of optical fiber $\sim 0.1\,dB/km$ scales to a value of $\sim 0.1\,dB/cm$ for microphotonic integrated circuits.

1.6 Optical Interconnects in Computing

Within a computing system, optics can afford superior performance for a variety of communication needs ranging from the board-to-board to the intra-chip level. This section introduces two applications of optical interconnects in computing systems: optical clocking and the optical data bus. The figure of merit for electronic/photonic convergence is bandwidth × power dissipation/footprint.

1.6.1 Optical Clock Signal Distribution

Distributing clock signals throughout the electronic computing system is one of the important functions that must be fulfilled by interconnection. In current prevalent synchronous design of computing architecture, periodic pulse signals travel along the interconnects and deliver to each register a timing reference for the movement of data within a system. As a result, the synchronized computing system will be able to operate by sampling data in the registers at precise time intervals, controlled by a central clock. This clocking synchronization applies to elements within an individual microprocessor, or at a higher hierarchy level, between chips and boards. In conventional clocking, where an oscillator clock generates an electrical signal and transports it through a conducting line, increasing technical difficulties arise at the higher frequencies required for faster operation.

Since clock signal interconnects are often loaded with the greatest fanout, travel the largest distances, and operate at the highest speeds within the system, clocking is the application where electrical interconnect problems arise first: prohibitive power consumption, crosstalk and RC delay make it an increasingly difficult task to lower the skew and jitter of signals at higher clock frequencies [7, 8, 9].

Optical clocking, which transports the clock signal by optical interconnects, is an alternative solution overcoming this barrier. Its fast transfer of signal and relative independence of power consumption on clocking speed and

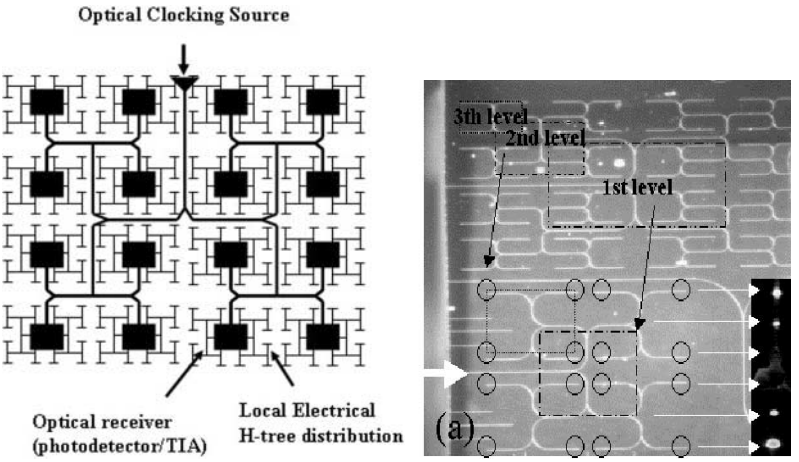

Fig. 4. *Left*: Monolithically integrated optical clocking structure for the Si microprocessor. *Right*: Photographic image of an H-tree optical clock signal distribution network circuitries

propagation length will make optical clocking attractive for new technology platforms.

Figure 4 shows the architectures for a reliable intra-chip optical clocking [10]. A single light source that generates a periodic pulse clock signal can be externally attached to the waveguide and monolithically integrated onto the chip. Light signals propagate along the waveguide in a H-tree network [see Fig. 4 (left)] ensuring that equal path length and fast propagation of photons will minimize skew of the clocking signal. At the end of the optical interconnect, photon signals are converted back to electrical signals by receiver units comprised of a photodetector and transimpedance amplifier. The electric clock signal continues to travel locally via electrical interconnects to the end register. The crossover level from optical interconnect to electrical interconnect is determined by the relative technical advantage between the two technologies at each H-tree hierarchy level.

Key technology elements are monolithically-integrable with Si waveguides, photodetectors and their coupling between components. These components and technologies are discussed in the following sections. optical clocking, unlike an optical data communication bus, provides a simplified technical challenge because there is no need for arrays of on-chip light sources and data modulators.

Since clocking applications see the electrical technology platform quickly approaching its technical limit and offer a relatively simple transition into optical technology, optical clocking posits itself as a significant milestone to the demonstration of the feasibility and applicability of microphotonics.

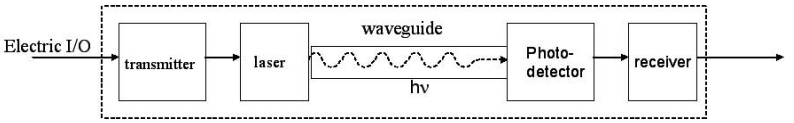

Fig. 5. Schematic block diagram of point-to-point optical data bus

1.6.2 Optical Data Bus

The optical data bus is a device for transporting data in an optical interconnect from one electronic device to another, enabling data transmission at faster rates and with less heat dissipation. The optical data bus is comprised of five basic components: a transmitter, laser, waveguide, photodetector, and receiver, as shown in Fig. 5. The transmitter translates electrical data into drive currents for the laser. The modulated laser light is then injected into the waveguide (optical interconnect) and transmitted to the photodetector. The photodetector converts the photons into an electrical signal, which is then reconditioned by the receiver and outputted to another electrical device.

Implementation of the optical data bus into higher hierarchy level applications (i.e. board to board), where fast data buses are needed is a rapidly developing area of research. One major issue in implementing the optical data bus is the material compatibility of the laser. Most lasers in the telecom window are made up of III–V semiconductors, requiring difficult hybrid integration onto a Si substrate [11,12], increasing fabrication complexity and cost.

2 Photonic Components

Section 2 presents the results of our work in developing passive Photonic device building blocks for the PLC. These waveguide structures guide light by the phenomena of total internal reflection (*Index Guiding*), and are based on Si, silicon nitride (Si_3N_4) and silicon oxynitride (SiON) waveguide cores surrounded by a silicon oxide (SiO_2) cladding, resulting in index guided structures with a core-cladding index difference $\Delta n = 0.1 \div 2.0$. These microphotonic device elements are realized by Si-on-Insulator technologies or deposition on thermal oxidized Si substrates, where the thermal oxide is a $0.5 \div 10\,\mu$m layer optically isolating waveguide modes from the Si substrate.

2.1 Optical Waveguides

As with most technologies, PLC design comes with tradeoffs, specifically a tradeoff between the photonic device size and sensitivity to surface roughness. Both properties are dictated by the refractive index difference Δn between waveguide core and cladding. A high Δn allows for smaller turning

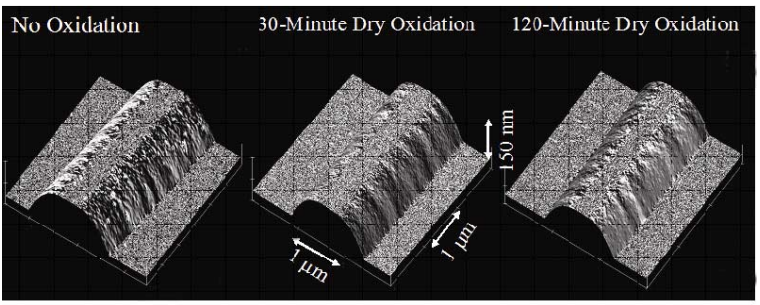

Fig. 6. AFM images of silicon waveguides, the *left image* is as fabricated whereas the *center* and *right* waveguides have undergone 30 and 120 minutes of dry oxidation and subsequent oxide etch respectively

radii, due to increased light confinement, which leads to smaller, densely integrated PLC components. However, as Δn is increased, index guided modes become increasingly sensitive to the roughness of device surfaces and results in appreciable transmission loss. Waveguide roughness running parallel to the direction of the waveguide yields an effective dielectric stack, in terms of varying effective index, resulting in destructive interference and scattering of the optical signal. This effect is augmented in high Δn systems since the strength of a dielectric stack is proportional to Δn^3.

An acceptable scattering loss for PLCs is less than 0.1 dB/cm. This loss value is mainly affected by fabrication related scattering loss. Therefore, there is a strong need to reduce scattering loss through the introduction of additional processing steps. Surface roughness in microphotonics is analogous to the role of impurities in microelectronics, with respect to processing difficulties affecting device performance. There are several ways to reduce surface roughness: oxidation [5], wet etching, and laser annealing [13]. Recently the focus has been on oxidation smoothing, a technique that can be used in any microphotonics system that uses a core material that forms a stable native oxide. Silicon is one such material with the added benefit of having SiO_2 as a compatible, high index contrast, cladding material ($\Delta n = 2$). The reduction of surface roughness is apparent from the AFM images shown in Fig. 6. As oxidation time increases the waveguide surface roughness decreases. From our initial work, we believe the transmission loss in silicon waveguides can be reduced to less than 0.2 dB/cm [14], matching the demands of future PLCs.

2.2 Bends

Current spliced-fiber photonic circuits are limited in complexity by their footprint. Each fiber 'pigtail' must be about 15 cm in length, because prohibitive radiative losses are introduced at fiber bend radii of < 1 cm. The platform elements must, therefore, provide open space for the fiber bends. While this

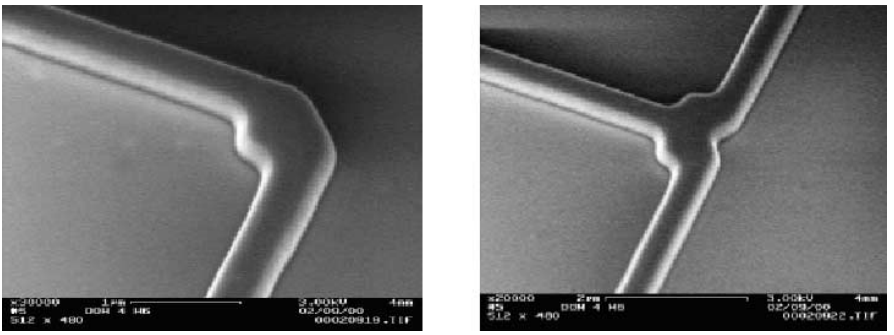

Fig. 7. *Left*: HTC bend device: the device area is $0.5\,\mu m^2$ and the loss are $< 0.3\,dB/turn$ for $1\,\mu m$ bend. *Right*: HTC junction device: optical loss are $< 1\,dB$

architecture has been adequate for long haul telecommunications applications where the interconnection density is limited, it clearly does not scale to server buses and chip-to-chip interconnects. This section reviews the principles of design for small bend radii. They are predicated on both higher optical confinement through 1. high index contrast (HIC) materials systems and 2. resonant structures that confine light.

2.2.1 High Transmission Cavity (HTC) Bends

Using High Index Contrast (HIC) material systems such as Si/SiO_2 or $SiON/SiO_2$, the bending radii can be minimized on the order of $1 \div 10\,\mu m$ at the cost of $0.1\,dB/point$ of bending loss [16]. Due to its strong light confinement, the HIC platform provides excellent dense optical integration [17]. To reduce the footprint further, High Transmission Cavity (HTC) bends were devised and fabricated [18].

Motivated by the optical clock H-tree structure, right angle bends have been prototyped using Si and SiON HIC platforms (Fig. 7). The bending loss was minimized up to $0.3\,dB/turn$ for $1\,\mu m$ bend and $1\,dB$ loss was achieved for T-splitter junctions [18]. The issue for HIC platforms is high propagation loss when sharp bends are realized.

2.2.2 Air Trench Bends for Sharp Bends

The low index contrast (LIC) silica-based platform has been produced using silica optical fiber technology where Δn is less than 0.01. In this LIC platform, propagation loss is not an issue, and several products such as arrayed waveguide gratings (AWGs) are commercially available. The challenge for the LIC platform is to minimize its large footprint applicability to optical clocking. To miniaturize the footprint, the bending radii should be minimized. However, sharp bends of LIC waveguides lead to substantial loss of light power due to poor light confinement.

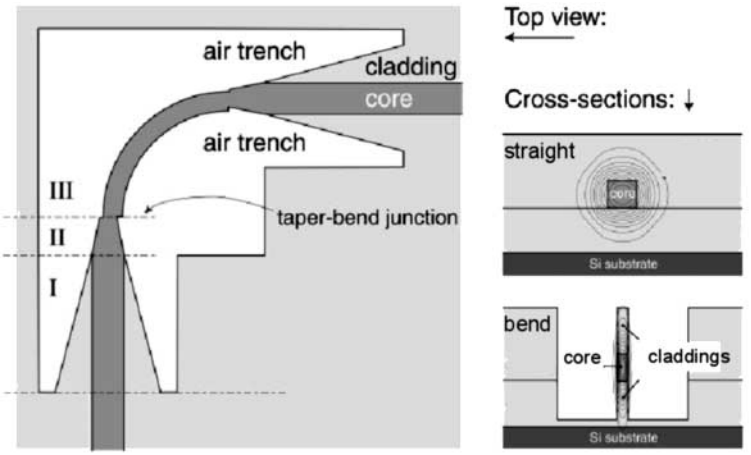

Fig. 8. Schematic diagram of air trench bend

The bending radius is typically 10 mm for $\Delta n = 0.01$, and thus on-chip integration of Si-LSICs (Large Scale Integrated Circuits) is almost impossible using the LIC platform. To minimize bending loss in LIC systems, we introduce air cladding at the bends (in the form of etched air trenches) to locally increase the index difference [19]. The index difference at the bends increases by approximately 0.5, enabling the minimum bending radii to 5–10 μm. The LIC platform with air trench bends becomes a potential candidate for on-chip integration. Figure 8 shows a schematic diagram of the air trench bends, consisting of two tapered parts and a bending part with offset junctions between the taper and the bend. The adiabatic tapering is to avoid abrupt junction-induced mode mismatch and Fresnel reflection. This results in drastic reduction of bending radii while preserving the low-loss performance of the LIC platform. Two-dimensional finite difference time-domain (FDTD) simulation shows how the inclusion of air trenches strongly reduces the bending radius (10–1000 ×) enabling smaller footprints (4–60 ×) for index guided systems with $\Delta n = 0.003$–0.1.

Table 1. Experimentally measured Bend transmission (%) per right turn (TM mode data, ±3% error bars) and FDTD calculation for the structure with $\Delta n = 0.1$

Radius (μm)	2	3	4.5	7	9
Theoretical (%)	92.82	98.12	98.85	99.57	99.67
Experimental (%)	86.87	93.92	96.31	96.54	97.17

For $\Delta n = 0.007$ the bending loss of 0.1 dB/turn at 1.55 μm is obtained with an air trench bend size of 96 μm (trench region bend radius of 9 μm), as

compared to a regular bend of 2.5 mm. The fabrication was done based on $\Delta n = 0.1$ and showed good agreement with FDTD simulations (Table 1).

2.3 WDM Functions and Add/Drop Micro-rings

The fundamental element required for bringing WDM communications onto a PLC chip is a compact, high-speed add/drop multiplexerdemultiplexer ("mux/demux"). Coupling of individual channels is the dominant design and cost factor in WDM optical signal distribution. For Microphotonic PLCs utilizing High Index Contrast (HIC) components, resonant coupling provides effective coupling with minimum footprint. A passive device that is resonant with the optical carrier frequency (wavelength) acts similar to an inductive tank circuit in electronics as power is coupled into the device with great efficiency. microcavity resonant structures, designed with free spectral ranges (FSR) larger than the WDM communications window, comfortably satisfy the mux/demux requirement within a compact area, for individual wavelength channels pulse encoded at 1–100 Gb/s.

Micro-ring resonators are travelling wave resonant structures which couple to an incident WDM waveguide bus by evanescent field overlap. Figure 9 shows an SEM of a micro-ring resonator coupled to input and output waveguides for channel drop functionality [20]. The ring becomes a sink for signal power when an integral number of wavelengths match its circumference, producing resonant whispering gallery modes. In Fig. 9 four Si_3N_4 rings, each with a 10% difference in circumference, couple to the same input waveguide. The power loss in each channel is shown in the through-port data (upper plot in Fig. 9 on the left). The power distributed to each channel drop port is shown in the drop-port data (lower plot in Fig. 9 on the left). Each micro-ring resonator acts as a filter with Lorentzian line shape. The quality factor, Q, of these filters is ~ 500, and the drop efficiency is nearly 100%.

The value of Q decreases with increased waveguide coupling, increased propagation loss in the micro-ring and radiative loss due to decreasing ring circumference. The micro-rings's FSR, determining add/drop channel selectivity, increases with decreasing circumference, thus correlating optimizing WDM add/drop performance with minimizing device footprint.

In contrast, increasing the Q of a linear resonator however requires increasing the number of Bragg reflector pairs, and this increases the amount of device scattering loss, due to the addition of interface roughness with each additional Bragg reflector pair. Increasing the Q of a micro-ring resonator requires increases the gap spacing between micro-ring and input WDM bus, and this does not increase the device scattering loss. The evanescent coupling strategy of a micro-ring resonator enables the design of ultra-high Q structures: we have demonstrated passive ring resonator structures with $Q = 5000$. The micro-ring architecture is thus ideally suited for long-term dense-WDM (DWDM) PLC designs.

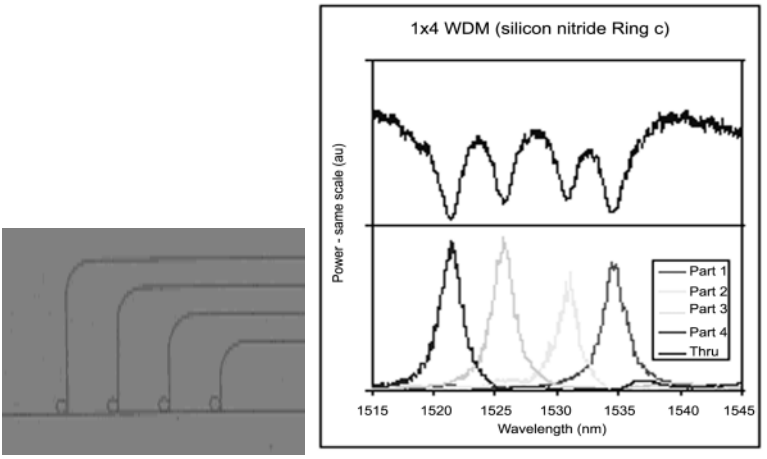

Fig. 9. Four channel add/drop configuration utilizing silicon nitride waveguides and micro-ring resonators with the performance data in [20]

2.4 Polarization Splitters and Rotators

Fiber coupling to a HIC integrated optic circuit is substantially more difficult than coupling to an integrated optic circuit with an index contrast similar to that of the fiber system for the following reasons: 1. The HIC waveguides used on the chip tightly confine the optical field thereby preventing a solid mode match between the chip and fiber modes, 2. The impedance mismatch between the low index fiber and high index chip results in substantial reflections and 3. HIC structures tend to be wavelength sensitive. The mode mismatch may readily be corrected by choosing an appropriate waveguide height and tapering the waveguide to a fine point thereby forcing the waveguide mode into a loosely confined state at the input of the chip. Reflection at the interface may then be mitigated by introducing a quarter-wave antireflection coating on the edge of the chip. However, because the HIC devices on the chip tend to be wavelength sensitive, connecting the input waveguide directly to these components would result in a polarization sensitive component in an otherwise polarization insensitive fiber optic communications link. Rather than attempt to correct the problem at the device level, a polarization diversity scheme may be applied whereby the input polarization is split into orthogonal TE-like and TM-like states, TM-like state is then rotated by 90 ° and the two identical TE-like chip states are then processed in parallel with identical polarization dependent structures. After passage through the devices on the chip, a second polarization conversion is applied to one of the paths (preferably, the path which it had not been previously applied to) and the two polarizations are recombined [21].

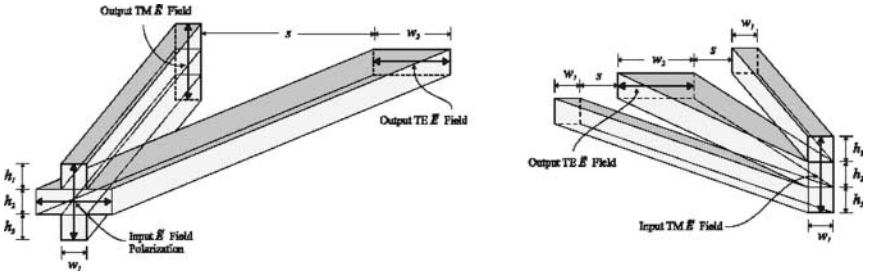

Fig. 10. A polarization splitter (*left*) and a polarization rotator (*right*) based on adiabatic following are shown. Three dimensional FDTD simulations were performed on each structure with core and cladding indices of 2.2 and 1.445 (SiN to SiO_2), layer thicknesses of $h_1 = h_2 = h_3 = 0.25\,\mu m$, and widths $w_1 = 0.25\,\mu m$ and $w_2 = 0.75\,\mu m$. The separations s for the beam splitter and the rotator are $2\,\mu m$ and $0.125\,\mu m$ respectively

In order for this approach to be successful, broadband and low loss polarization splitters and rotators must be integrated on the chip. Several proposals for integrated optic polarization splitters and rotators have been previously published [22,23,24]. However, with the exception of the polarization splitter offered by [25], all such proposals rely on mode coupling to achieve the desired result. As a result of modal dispersion, approaches based on mode coupling tend to be wavelength sensitive. Moreover, in order for the modes to couple efficiently, the modes must be phase-matched and precisely spaced leading to strict fabrication tolerances.

However structures that rely only on adiabatic following [26] do not suffer from these limitations. Essentially, a mode will follow and evolve along a perturbed structure so long as the coupling to other modes introduced by the perturbation is sufficiently small to allow the modes to de-phase before substantial power exchange occurs. The polarization splitter and rotator presented in Fig. 10 (left) and Fig. 10 (right), respectively, are based on this principle. The polarization splitter begins from a cross-shaped waveguide with degenerate polarization states and gradually shifts the two arms of the cross apart. Although the TE-like and TM-like modes of this structure are phase-matched, coupling between them is prevented by mode symmetry and the TE-like and TM-like modes follow the horizontal and vertical waveguides, respectively. The polarization rotator mates up to either of the output arms of the polarization splitter depending on whether a TE or TM on-chip polarization is desired, and is essentially an approximation of a twisted waveguide.

The upper and lower layers are progressively moved into the evanescent field of the mode while core material is added to the middle layer. The results of three dimensional FDTD simulations shown in Fig. 11 (left) and Fig. 11 (right) indicate that near perfect splitting and rotating of polarizations is achieved across the entire 1.45 μm to 1.65 μm band in structures only

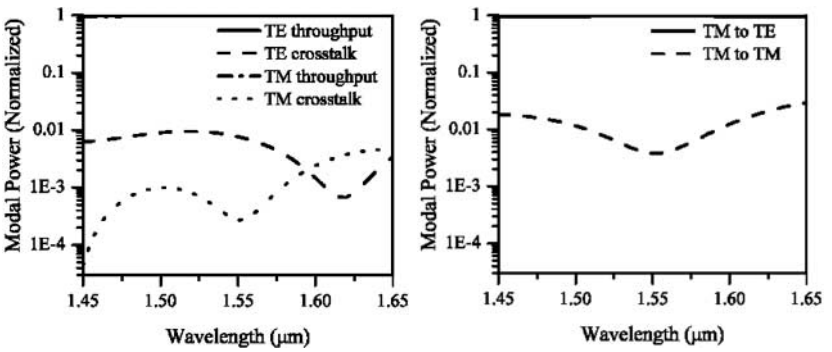

Fig. 11. *Left*: Three-dimensional FDTD simulations results for the polarization splitter with a device length of 50 μm (and separation $s = 2\,\mu\text{m}$). *Right*: Results for the polarization rotator with a device length of 50 μm

50 μm long. a simple taper as described in the beginning of this section may be used to couple into the polarization splitter.

2.5 Silicon Light Sources

The scientific and technological breakthrough in the current stage of silicon microphotonics would be the demonstration of an efficient Si light emitter in order to combine Si light emission with all the different functionalities of passive devices described in the preceding sections.

Light emission from silicon is an indirect phonon mediated processes with low probability. In addition, fast nonradiative transitions such as Auger or free carrier absorption [27] severely prevent population inversion at the high pumping rates needed to achieve optical amplification and lasing. Despite of these fundamental limitations, during the 1990s several different strategies have been deeply investigated to increase light emission from different silicon structures [28]. Among the different approaches developed so far, quantum confinement and rare earth doping of silicon have dominated scientific efforts towards the goal of achieving active Si microphotonics. Due to the favorable modification of their optical properties, numerous silicon nanostructures, such as porous silicon [29], silicon nanocrystals embedded in an SiO_2 matrix [30,31,32], and Si/SiO_2 superlattices [33,34] have been widely studied. In particular, silicon nanocrystal research has recently led to exciting results, related to the possibility of fast optical gain in closely-packed silicon nanocrystals, stimulating a rich debate around the feasibility of a future silicon laser device [35,36,37]. In addition, external quantum efficiencies in excess of 1% have been very recently reported in high purity bulk silicon LEDs with surface texturing [38], and the occurrence of optical gain in indirect band-gap materials has been theoretically reassessed [39].

After the discovery of room temperature light emission in Erbium (Er) doped Si [40], Erbium doping has been considered as an ideal candidate to realize the goal of integrated silicon optoelectronics satisfying VLSI requirements. Despite a strong temperature quenching of the luminescence, room temperature eletroluminescence from an Er-doped silicon LED structure with an emission linewidth of 130 Å, was demonstrated for the first time at MIT in 1994 [41]. Despite this breakthrough, it became clear that light emission from Er in silicon is limited by the presence of efficient nonradiative channels like energy back transfer (occurring from the internal first excited state of Er to the external Si lattice) and non-radiative Auger recombination involving Si excitons and Er complexes. A detailed study of the recombination kinetics of Er in silicon is reported in [42]. Using Er as an optical dopant in a Si host material results in a room temperature light emitting device with 10^4 lower quantum efficiency than III–V materials. In addition, parasitic gain limiting effects like free carrier absorption in bulk Si and Er-related up-conversion prevents population inversion of Er in Si, making such a materials system unsuitable for a laser light source or an optical amplifier. Er-doping of glass structures continues to be an ideal approach for the low loss third Telecom window, producing an almost temperature independent emission line at 1.55 μm. Even though Er-doped SiO_2 is already used commercially in optical fiber amplifiers, the application of Er-based structures in Si microphotonics is limited thus far by the small optical cross section of the Er^{3+} transition, and represents a major challenge towards silicon-based microphotonics.

Si CMOS compatible dielectrics, specifically SiO_2, Si_3N_4, and SiON mixtures of the two, form an amorphous insulator host material system for the Er (or other ms-lifetime rare-earth) optical dopant, resulting in 1. efficient room temperature light emission, and 2. negligible Auger, free carrier absorption and energy back-transfer contributions.

Recently, Er doping of Si nanocrystals has been recognized as a hybrid approach combining the promising features of both quantum confinement and impurity doping. It has been demonstrated that Si nanocrystals in the presence of Er act as efficient sensitizers for Er light emission [43], enhancing the Er excitation cross section by more than two orders of magnitude due to a quasi-resonant energy transfer process.

Recent observations of net optical gain at 1.54 μm with enhanced Er emission cross section in Er-doped Si nanocluster sensitized waveguides [44], and the demonstration of efficient room temperature electro-luminescence from Er-silicon nanocrystal devices [45] has opened the route towards the future fabrication of CMOS compatible Er-based devices with efficient electron injection.

2.6 Microphotonic Amplifiers and Lasers

From the perspective of an optical amplifier, the choice of working with ms-lifetime light emitting rare earth atoms, within an amorphous host material,

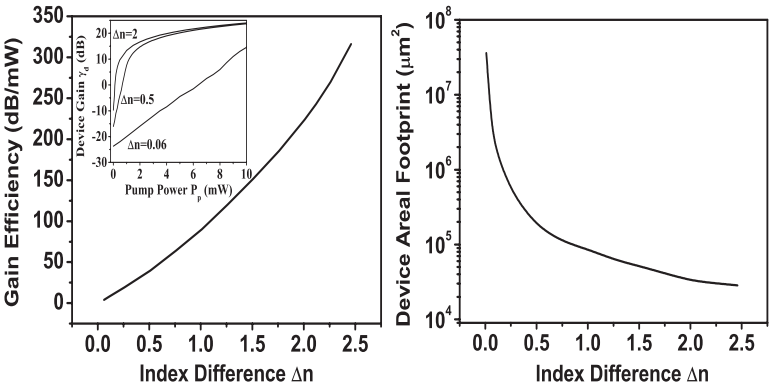

Fig. 12. *Left*: Performance Scaling Advantage [46]: gain efficiency versus Δn for an Er-doped, 1 m long HIC-WOA. *Inset*: plot of Device Gain γ_{eff} vs Pump Power P_{p} shows increasing slope with higher Δn. This data does not include the simulation of scattering transmission loss. *Right*: Size Scaling Advantage: plot of a coiled structure (with a 1 cm device length) areal footprint versus Δn

enables an optimal design by ensuring 1. negligible WDM crosstalk at 1 Gb/s, 2. noise figure values approaching the theoretical limit, and 3. a broad gain bandwidth for full WDM spectrum amplification. From the perspective of a laser light source, the choice of working with light emitting atoms, which are diffused/implanted into waveguide structures, enables the design of in-plane laser structures with zero coupling loss to other passive PLC devices. Using the SiO_2/Si_3N_4 system as a host material, we envision Si microphotonic laser light sources and optical amplifiers as optically pumped waveguide structures with $\Delta n = 0.1$–0.75.

2.6.1 Index Scaling and the Design of Efficient Microphotonic Optical Amplifiers

As microphotonic PLCs scale to higher complexity, the circuit fanout (number of splits) becomes a major source of signal attenuation. WDM long haul transport architecture was enabled by $\sim$ 20 dB gain full spectrum optical amplifiers, utilizing high power III–V pump lasers and $>$ 20 m of Er-doped fiber.

For PLCs a 3 dB signal gain at each Y-split would be sufficient to compensate for fanout. To be practical as a planar device, such 3 dB optical amplifiers must occupy a negligible footprint relative to the circuit size. A reasonable design benchmark for compact amplifier device is a footprint of $< 2\,\text{mm}^2$, 3 dB optical gain, 1.75 dB noise figure, 1 mW pump power source and compatibility with 1 Gb/s data transmission. We have recently derived scaling laws for the design of HIC waveguide optical amplifiers (HIC-WOAs) [46],

observing that higher Δn waveguide structures result in 1. performance and 2. size scaling advantage for HIC-WOAs.

The increase in optical confinement with higher Δn results in an increase of signal and pump flux within the waveguide core, creating an increase in amplifier gain efficiency (dB/mW). In a co-propagating pump design, this performance scaling advantage occurs for a constant output signal-to-noise ratio, implying constant noise figure performance, as a function of Δn. We observe (see Fig. 12 (left) a gain efficiency increase of $25\times$ for a microphotonic scale $\Delta n = 1.0$ system, compared to an EDFA scale $\Delta n = 0.06$ system. This means $25\times$ less pump power is required to achieve the same small signal gain coefficient in a HIC-WOA, compared to an EDFA.

The waveguide wound into a two-dimensional coil structure [46] scales dimensionally to a smaller areal footprint with higher Δn due to the smaller turn radii enabled by HIC design. A constant device length [$L = 1$ cm, see Fig. 12 (right)] amplifier shows the impact Δn has on its footprint size scaling: a microphotonic scale $\Delta n = 1.0$ system can deliver the same amount of device gain from an area that is $500\times$ smaller than the EDFA scale $\Delta n = 0.06$ system. Gain per unit area on a PLC has thus increased 500 times.

We define a cumulative Figure Of Merit (FOM) for HIC-WOA performance as the device's Areal Gain Efficiency: device gain/(pumppower $\times$ area). This FOM scales dramatically as $(\Delta n)^{2.6}$, summarizing the major benefits due to performance and size scaling for microphotonic HIC-WOA design [46].

2.6.2 Compact Lasers

Micro-ring resonator amplifiers merge both light amplification and WDM filter functions, resulting in flexible devices with high wavelength selectivity and low inversion threshold (very high quality factor Q). In addition, such devices realize the conditions for strong light-matter coupling, yielding a variety of interesting applications for all-optical signal processing related to the enhancement in single channel intensity and nonlinear materials interactions.

In addition, it has been recently demonstrated [47] that Micro-ring laser light sources may potentially realize compact optically pumped lasers for future Si microphotonic platforms.

We show that laser oscillations are possible within these microring structures if fabrication techniques can considerably reduce optical losses. Figure 13 shows the theoretically computed minimum resonator quality factor, Q_{th}, for lasing to occur at a given pump power density, considering an Er-doped Si_3N_4/SiO_2 system.

Several loss coefficients (representing the overall device losses) are shown as horizontal lines related to an equivalent loss quality factor Q_{loss}. For a given value of the total device losses α (yielding a power independent Q_{loss} factor), pump power density must be high enough to ensure the gain clamping relation: $Q_{\text{th}} \leq Q_{\text{loss}}$. Under this condition the total device quality factor given by

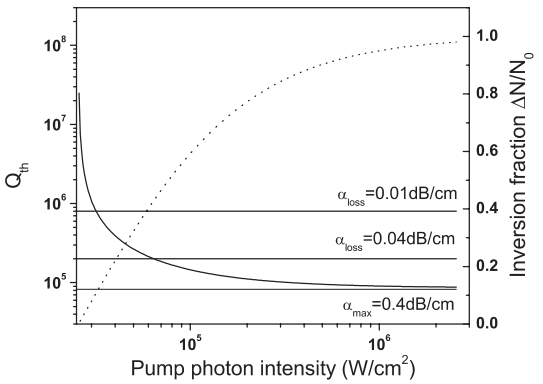

Fig. 13. Threshold quality factor versus pump power density for an Er-doped Si_3N_4/SiO_2 micro-ring resonator. The *dotted curve* shows the fractional population inversion in the device. The *horizontal lines* correspond to the overall device loss reported in the figure

$Q = (Q_{\text{th}}^{-1} + Q_{\text{loss}}^{-1})^{-1} \approx Q_{\text{th}}$, and laser oscillation can be sustained. This analysis makes manifest the critical device processing challenge for realization of optically pumped laser light: the reduction of optical loss (mainly scattering losses) to below 0.4 dB/cm for $\Delta n = 0.1$–0.75 waveguide structures.

3 Photodetectors

3.1 Heteroepitaxial Growth of On-Chip Detectors

Microphotonics is inherently a materials diverse technology. Compound semiconductor sources, dielectric waveguides and ceramic isolators and modulators offer a much greater integration challenge than silicon, silicon dioxide and aluminium did for electronic circuits. The Large Scale Integration (LSI) of microphotonic components to device densities greater than 10^4 devices per chip, encounters two primary barriers: cost and complexity. At device densities of less than 10 devices per chip, hybrid integration by pick-and-place flip-chip, solder-bumps or wafer bonding have the lowest barrier to technology implementation. The advantages of the hybrid approach are 1. best in class optoelectronic devices, and 2. separation of yield issues to device fabrication and packaging [48]. The fact that the packaging of single components dominates cost today is the dominant driver for monolithic integration at even moderate levels of integration. LSI is predicated on the establishment of high yield process technologies and process integration strategies. There is a clear need to develop heteroepitaxial growth and fabrication technologies and concepts for process integration to create a credible vision for LSI microphotonics. The most likely first step for the technology evolution is

heteroepitaxy on CMOS or BiCMOS circuits. a particularly important application is the integration of Ge photodetectors with polycrystalline Si waveguides and Si based electronic devices for the distribution and detection of optical signals at wavelengths of 1.3 μm and 1.55 μm on Si. High-quality Ge on Si can also be used for the integration of Ge-based transistors on Si.

The primary difficulty in Ge on Si epitaxy is the 4% lattice mismatch between Si and Ge. This lattice mismatch must be accommodated either through strain or dislocations. In particular, threading dislocations degrade device performance by reducing carrier collection efficiency and increasing leakage current strain may also lead to surface roughness or islanding of films.

One successful approach to reducing the dislocation density is through the use of buffer layers. The first effective linearly graded buffers were grown by *Fitzgerald* et al. [49,50] by MBE at AT & T Bell Labs. In one attempt, pure Ge epilayers were obtained by deposition of amorphous Ge on Si, followed recrystallization by annealing [51]. Despite encouraging results, the problem with direct epitaxy of Ge or SiGe alloys is the high dislocation density.

Due to the lattice mismatch, SiGe alloys with Ge concentrations greater than 30% generally have dislocation densities of 10^{11}–$10^{12}\,\mathrm{cm}^{-2}$ [52]. Post-growth cyclic annealing can reduce the dislocation density to $10^{7}\,\mathrm{cm}^{-2}$ [53]. This method can produce Ge films suitable for high quality photodetectors.

3.2 Ge Detectors Integrated on Si

Ge is an ideal candidate for low cost, high performance photodetectors because of its compatibility with existing silicon processing, its high carrier mobility, and its high optical absorption at telecommunication wavelengths [54]. CMOS compatible photodiodes were fabricated from films described in the previous section, resulting in the diode structure shown in the inset of Fig. 14. With low temperature oxide (LTO) as an insulation and passivation layer, p–i–n diode structure can be realized in a way that is fully compatible with CMOS technology. At a reverse bias of −2 V and a Ge epitaxial film thickness of 1.3 μm, the responsivity at 1.3 μm and 1.55 μm are 0.64 A/W and 0.40 A/W, respectively.

The experimentally measured responsivity data are shown in Fig. 14 (black curve). As will be explained in the following section, the stress-induced bandgap shrinkage increases the device responsivity with respect to the one calculated for a Ge film without strain, making this approach appealing for achieving broadband detection.

3.3 Broadband High Speed Detectors

The development of Dense Wavelength Division Multiplexing (DWDM) technology and Fiber to the Home (FTTH) technology require broad band, high speed Ge detectors integrated on Si microchips to convert optical signals

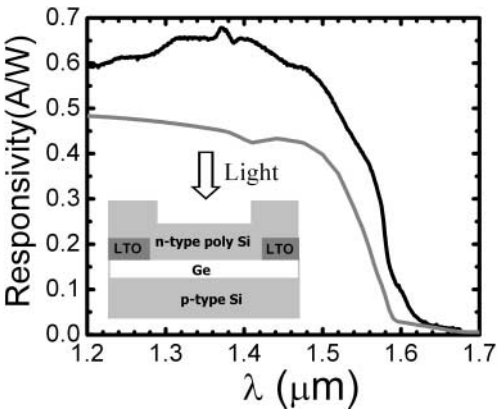

Fig. 14. *Black curve*: Experimentally measured responsivity of the Ge detector device shown in the *inset*. The measured in-plain strain in the Ge film is 0.13%. *Grey curve*: Calculated device responsivity assuming no strain in the Ge film

to electronic signals after demultiplexing by ring resonators. Currently the wavelength range used in telecommunications is expanding from the C-band (1528–1561 nm) to the L-band (1561–1620 nm) [55]. However, the absorption of bulk Ge falls rapidly for energies below the direct band-gap at Γ point (Eg^{Γ}) of 0.8 eV, corresponding to 1550 nm, limiting the application of Ge photodetectors to wavelengths of 1550 nm or shorter. Tensile strained Ge has been found to be a promising candidate for achieving photodetection up to the L-band [56,57,58]. When a thin Ge film of a few atomic layers is pseudomorphically grown on Si, a compressive stress in the film will be induced. As the Ge film grows thicker, misfit dislocations generate at the Ge/Si interface to relax the elastic strain and minimize the free energy of the system [59]. When the sample is cooled down to room temperature, tensile strain dominates the Ge film due to thermal expansion coefficient of Ge being greater than that of Si.

Under tensile biaxial stress the direct band-gap of Ge film shrinks and the valence band becomes non-degenerate, as schematically shown in Fig. 15. The direct band-gap of the tensile stressed Ge film is determined by the gap between the light hole band and the conduction band [$E_g^{\Gamma} = E_g^{\Gamma}(\mathrm{lh})$]. The grey shadow areas in Fig. 15 (left) shows $E_g^{\Gamma}(\mathrm{lh})$ and $E_g^{\Gamma}(\mathrm{hh})$ as a function of tensile strain. To take into account the error ranges of the deformation potential reported in [60], we have plotted the upper and lower limits of theoretical predictions. Epitaxial Ge films were grown at temperatures from 600 °C to 800 °C to study the direct band-gap versus strain relationship experimentally, and the results are shown by the solid circles in the Fig. 15.

Backside silicidation can be employed to further increase the tensile strain and decrease the direct band-gap of Ge film [58]. The highly conductive silicide layer also forms a good back contact for the devices. With this method, a tensile strain of 0.24% and a direct band-gap of 0.7656 ± 0.0004 eV was achieved, as shown by the hollow circle in Fig. 15. This result indicates

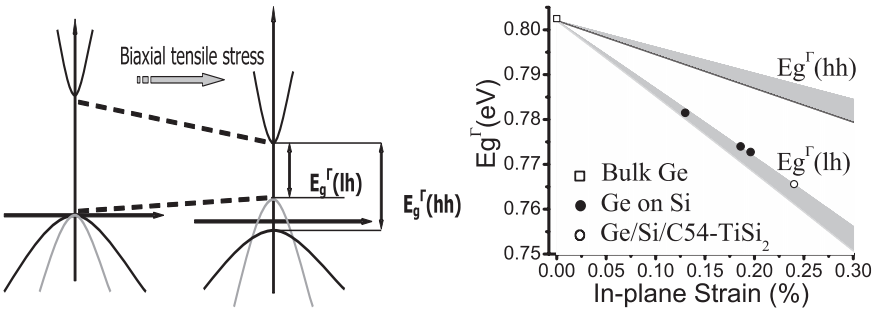

Fig. 15. *Left*: Schematic diagram showing the effect of biaxial stress on the band structure of Ge. *Right*: Theoretical calculation and experimental data of Ge direct band-gap as a function of in-plane strain. The *grey shadow* shows the range of theoretical prediction calculated by the deformation potential theory, using the deformation potential values reported in [60] and taking into account the error bars of these data. The *open square* is the datum of unstrained bulk Ge(100) single crystal. The *solid circles* show the band-gap shrinkage of Ge on Si samples grown at different temperatures, while the *open circle* shows further band-gap shrinkage induced by the backside silicidation

that with backside silicidation efficient light detection up to 1620 nm can be achieved, covering the entire L-band.

The speed of a photodetector is mainly determined by two factors: RC delay and carrier transit time. The RC delay of Ge p–i–n photodiodes can be effectively reduced by decreasing the area so that the capacitance is reduced. For a well designed photodetector, the response time is mainly determined by the carrier transit time. With an electron mobility of 3900 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ and a hole mobility of 1900 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ for bulk Ge material [61], assuming an intrinsic Ge layer thickness of 1 μm and an applied reverse bias of 1 V, the maximum working frequency is calculated to be 25 GHz. High-speed Ge p–i–n detectors with a response time < 200 ps have already been demonstrated, corresponding to a frequency of 2 GHz, and the responsivity was as high as 0.89 A/W and 0.75 A/W at 1.3 μm and 1.55 μm, respectively [62]. p–i–n diodes made of tensile strained Ge grown on Si substrates are expected to achieve a high speed of > 25 GHz with high responsivity over a broad band up to 1620 nm after device optimization (see Fig. 14).

3.4 Lightwave Circuit Integation with Photodetector

Efficient photodetector/waveguide coupling represents an issue of primary importance for the achievement of dense optical integration. Typical schemes for the integration of photodetectors with planar ligthwave circuits can be grouped into two main categories (see Fig. 16): Butt coupling [63, 64, 65] (or End-Fire coupling) and evanescent coupling. In the case of the Butt coupling scheme the photodetector is aligned in series with the waveguide to increase

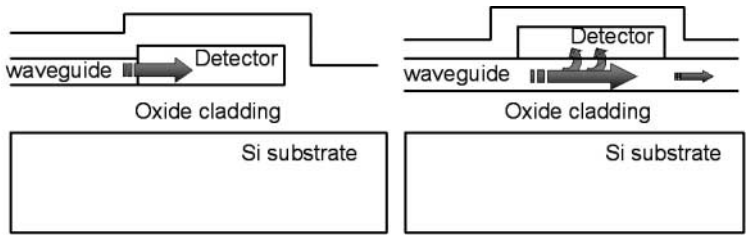

Fig. 16. Coupling structure of waveguide and photodetector integration. *Left*: Butt-coupling structure. *Right*: Evanescent-wave coupling structure

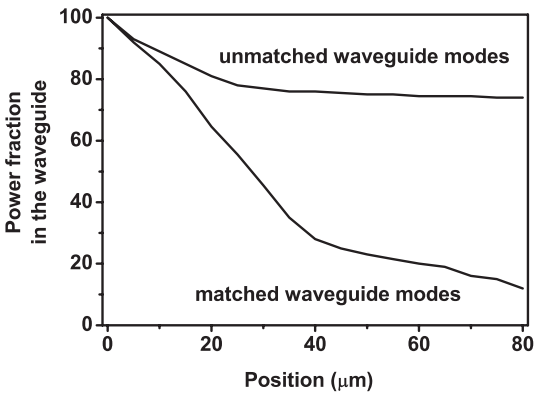

Fig. 17. Two dimensional beam propagation method (BPM) simulation of integrated structure showing power coupling for an out of phase matching condition and for a phase-matched condition

photon absorption rate. However, precise Butt coupling alignment demands complex fabrication capabilities with high geometrical accuracy. In addition, back reflection at the detector/waveguide interface (especially in the case of high Δn materials) has to be suppressed through an anti reflection (AR) coating.

In the case of evanescent coupling structures [66, 67, 68], the detector is positioned on top of the waveguide and light coupling occurs through the evanescent tails of the waveguide modes. When waveguides and detectors are grown by epitaxial methods (Si/Ge, Si/SiGe, or III–V semiconductor materials system), the evanescent coupling approach provides monolithic process control of the waveguide/photodetector interface and eliminates the requirement of precise lateral alignment, yielding more robust coupling structures for reliable integration.

A particularly powerful geometry for weakly absorbing (indirect gap, Ge or Si) detector materials is the 'waveguide configuration': for high index contrast between the waveguide and detector materials, a phase matched design is required for efficient evanescent coupling.

Figure 17 shows the critical dependence of coupling behavior on Si layer thickness for an SiON ($n = 1.5$) waveguide. When calculated index guided mode propagation constants are not matched, photons are not coupled into the absorbing Si layer and almost no coupling occurs. For a calculated Si thickness that matches the Si layer propagation constants to the SiON waveguide, the coupling is strongly enhanced.

4 Photonic Crystal Structures

Photonic crystals provide the ultimate in photon control and device shrink. A photonic crystal is a periodic composite of high and low index materials that, as a medium, influence the propagation of light in a way similar to atomic potentials with the flow of electrons in a semiconductor. The fabrication of photonic crystals is difficult, and HIC index guided structures (see Sect. 2) can achieve similar performance/area for many applications. Nevertheless, photonic crystals provide a dominant design paradigm for microphotonics, including HIC components. Four specialized applications are discussed below: small modal volume for in-line filters and low threshold sources; multichannel tuneable devices for ubiquitous placement in microphotonic circuits; photonic band-gap waveguide amplifiers and complex photonic structures for future active and multi-resonant devices.

4.1 Ultrasmall Devices

An in-line add/drop device can be constructed as a microcavity inserted in a waveguide [69]. One dimensional photonic crystals are inserted as dielectric stack mirrors. As the index contrast in the mirror increases, a larger spectrum of high reflectivity (photonic band-gap) results. In the example of Fig. 18, air sections ($n = 1$) are separated by silicon sections ($n = 3.5$) with the spacings chosen to give a photonic band-gap overlapping the WDM gain spectrum of an Erbium Doped Fiber amplifier (EDFA).

The missing air section in the middle of the device defines the pass band (wavelength of the channel to be dropped). The simulated and measured performance on the right indicates the strong theoretical foundation behind photonic crystal design. The Q of this device is 265 at the resonant wavelength of 1564 nm. Most impressive is the modal volume of $V = 0.055\,\mu m^3$. Low threshold Er-based light sources require high values of Q/V. High Q can be designed with large numbers of sections, but low V has been the challenge until the advent of photonic crystals.

4.2 Multichannel Design

The design paradigm of photonic crystals creates an analogy between channel drop frequencies of an optical filter and bound defect states in the gap of

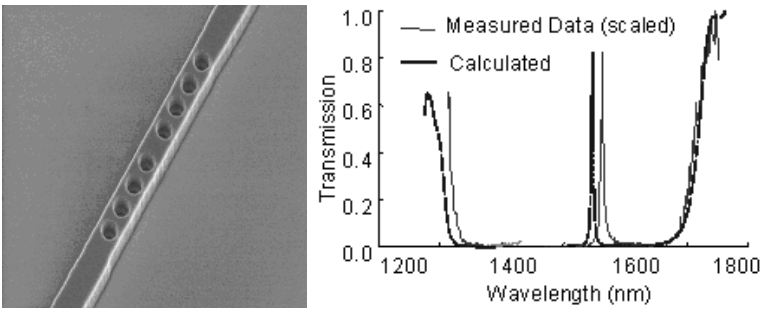

Fig. 18. An inline photonic crystal add/drop filter in a silicon waveguide with measured and calculated performance

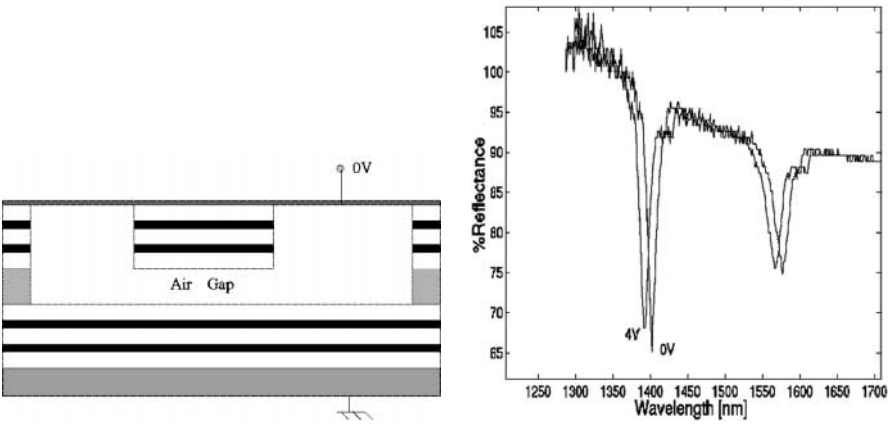

Fig. 19. Device cross-section and performance for a multichannel, tuneable add/drop filter [70]

a semiconductor. As some defects can present more than one state in the gap of a semiconductor, a photonic crystal filter can be designed as a multichannel device. For microphotonic circuits to grow in complexity beyond 10 devices/chip, a ubiquitous device, akin to a transistor, must perform switching and amplification functions. Since photons possess no charge, their interaction is mediated by wavelength or frequency.

A variable frequency (wavelength) filter can act as a switch, add/drop path and multiplexer/demultiplexer for telecommunication channels. If the same device can yield all functions, it can be replicated in a simplified design/process integration scheme. The photonic crystal device in Fig. 19 is such a device with operation in the 1310–1600 nm regime [70]. For this microelectromechanical actuated device a 12 V bias results in 100 nm tuning for each channel.

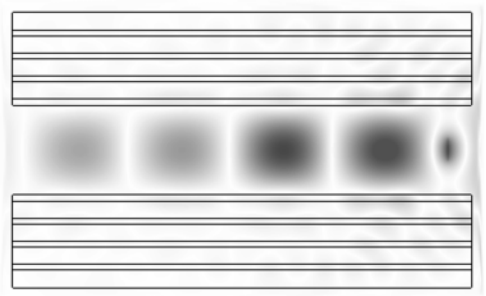

Fig. 20. FDTD simulation of the PBG waveguide, showing light propagation in the low index core material (SiO_2)

4.3 Photonic Band-Gap Waveguide Amplifier

Total internal reflection (TIR) has been traditionally the only mechanism to confine light within the core of optical waveguides whose core refractive index is higher than the index of the cladding. Optical fiber and silica-bench optical waveguides are entirely based on TIR. An interesting departure from this traditional index guiding scheme is based on the realization of photonic band Gaps (PBG), forbidden frequency ranges in periodic dielectric structures capable of full light confinement also in low-index materials or hollow waveguide cores. A new type of silicon waveguide-PBG cladding waveguide can be developed based on the PBG principles. The light in the core of the waveguide is confined by destructive Bragg scattering as opposed to TIR mechanism.

The low refractive index in a PBG cladding waveguide core allows for a large device flexibility, realizing sharp bends with negligible radiation losses due to the PBG confining mechanism. The PBG waveguide can be designed as a slab waveguide, ridge waveguide, and channel waveguide with low index core (SiO_2 or air) surrounded by high index contrast dielectric cladding stacks (Si/SiO_2 or Si/Si_3N_4). The resulting waveguides are fully compatible with CMOS process.

Potential applications include optical amplifiers where these structures are doped with optically active materials (e.g. Er atoms, quantum dots, etc.) in the SiO_2 core. Scattering losses out of the active guiding region can be suppressed in these waveguide devices, allowing for low threshold operation.

The PBG waveguide amplifier can be optically pumped from the top or in a co-propagating geometry. The stop band of the PBG cladding layers can be designed so that the propagation modes are around the 1.54 μm range, while the pumping wavelength can have full transmission. The FDTD simulation of the modes confined in the low index core are shown in Fig. 20.

Near 100% absolute reflectivity of 6 pair Si/SiO_2 PBG cladding layers has been achieved using novel thermal oxidation process.

While photonic crystals and the formation of light defect states can afford unique properties like strong dispersion at the bulk localized band edge

states, strong field enhancement effects in a small defect volume, etc., the strict requirement of periodicity gives rise to some fabrication constraints. Recently, new types of photonic structures – random or quasi periodic photonic structures, have been found to be more flexible in terms of engineering of the dispersion properties, affording more freedom in terms of design parameters and defect engineering.

4.4 Complex Photonic Structures

The interest in random dielectrics and complex photonic structures, materials where the refractive index fluctuates over length scales comparable with the wavelength of light, has increased in the last few years. The phenomena related to coherent backscattering of light [71,72] and Anderson photon localisation [73,74] have been demonstrated experimentally [75,76] and the study of disordered dielectrics with gain [77,78] has demonstrated the feasibility of random lasers [79] – mirrorless lasers where the required optical feedback is achieved through strong multiple scattering inside the inverted disordered medium. The class of photonic complex structures can be enlarged by considering fractal and quasiperiodic structures, characterized by refractive index profiles that fluctuate neither randomly nor periodically, though the structures are deterministically generated according to simple iterative prescriptions (such as the Fibonacci sequence $F_{j+1} = F_j + F_{j-1}$). Despite their attractive physical properties, little attention has been devoted so far to the experimental realization of this intermediate (between random and perfectly ordered structures) class complex dielectrics, namely photonic quasicrystals (PQs) [80].

Photonic quasicrystals, realized by the stacking together different dielectric materials, exhibit many novel phenomena such as a fractal transmission spectrum of zero Lebesgue measure, field quasi-localisation (field states decaying as a power law inside the structure) and sizeable field enhancement, fractal field states and several interesting anomalies both in the electron and photon transport (marginal diffusion, subdiffusive behaviour, etc.) related to the fractal characteristics [81,82,83,84] of the structures.

The rich transmission spectra of fractal photonic structures, the strong band-edge dispersion and the occurrence of quasilocalized modes with field enhancement are attractive characteristics from a device application point of view [85].

In particular, the band-edge zone of quasicrystalline photonic structures can considerably slow down light diffusion because of the combined presence of auto-similar (fractal) localized states and the finite size band-edge resonances with enhanced mode density [86,87] (see Fig. 22).

The strong light-matter interaction that occurs for high index contrast PQs both at the quasilocalized or at the strongly dispersive band-edge states can lead to gain enhancement [89] in the material with appealing implications for future multifrequency active devices, such as fractal band-edge lasers,

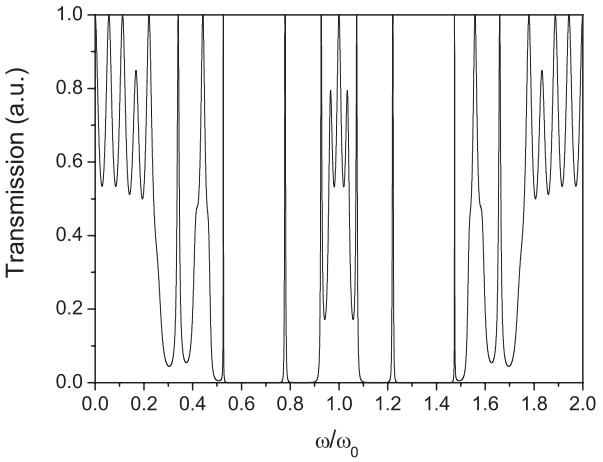

Fig. 21. Calculation of the transmission spectrum versus the normalized frequency for a 32 layers Thue-Morse nonperiodic structure realized with Si and SiO_2 layers. The multilayers structure satisfies the $\lambda/4$ condition around the operation wavelength $\lambda_0 = 1.54\,\mu m$

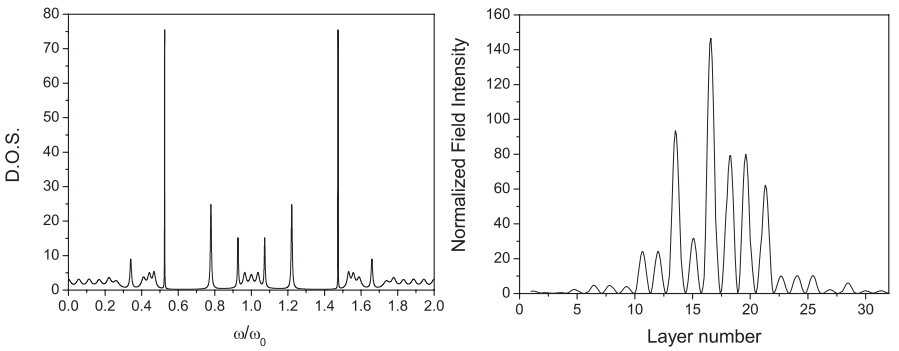

Fig. 22. *Left*: Calculation of the adimensional density of optical modes for the 32 layers Si/SiO_2 Thue-Morse structure [88]. *Right*: Calculation of the electric field intensity at the higher energy band-edge normalized to the input field

multiwavelength light sources and amplifiers, frequency selective filters for DWDM.

The occurrence of strong band edge group velocity reduction and enhanced band edge dispersion (with respect to periodic structures) in quasiperiodic 1D structures have been recently demonstrated experimentally [90, 91].

The possibility to fabricate PQs alternating Si and SiO_2 layers with standard CMOS compatible deposition techniques represents a promising route to demonstrate significant localization features (see Figs. 21 and 22) in a PQ structure with a limited number of dielectric layers, paving the way for the realization of a variety of optical devices based on localized or heavy photons.

5 Conclusion

Monolithic Silicon Microphotonics offers a scalable solution to interconnection density, bandwidth, latency and electronic/photonic partitioning. The use of standard silicon-compatible materials and process tools is highly leveraged with the $250B/year integrated circuit industry supply chain. It is both surprising and gratifying that Silicon Microphotonics can produce the entire range of photonic component functionalities with reasonable performance. One can project a vision for the technology as outlined below. As photonics emerges from its near term niche market character (< $20B/year) to universal deployment in all intelligent systems, silicon will become the dominant platform. With performance/cost as the driving metric, the high levels of parallelism made possible by photonic interconnection will assume control of systems design. The silicon platform will drive standards and cost reduction until photonic circuits are commoditized, and then photonic functionality through repartitioning of the electronic/photonic interface will drive the new value proposition.

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