# Silicon-Based Waveguide Technology for Wavelength Division Multiplexing

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**Abstract.** This chapter reviews the application of silicon-based planar waveguide components for wavelength division multiplexing (WDM) and demultiplexing. The polarization dependent properties and dominant waveguide loss mechanisms in both silica-on-silicon and silicon-on-insulator (SOI) waveguides are described, and the technologies developed to control loss and eliminate polarization dependence in both material platforms are presented and compared. Although less mature, the development of high index contrast devices in SOI closely parallels the evolution of silica glass waveguide technology. Many of the important design challenges have been resolved, and the performance of SOI-based integrated optic components is rapidly approaching that of the silica waveguide system.

## 1 Introduction

The multiplexing, demultiplexing, and measurement of wavelength are essential photonic functions, and the need for high performance dispersive elements continues to drive research in planar waveguide optics. Wavelength division multiplexing (WDM) in particular is a flexible technology that provides an elegant solution to the problem of transporting large quantities of data in parallel streams over a single conduit, the optical fibre or perhaps even free space. Therefore the applications of planar waveguide dispersive elements may likely expand to include board-to-board data bus applications, rack-to-rack connections, and finally merge with the telecommunications network at the local area network level. The same wavelength selective element that lies at the heart of any WDM demultiplexer can also be used for spectroscopy, replacing present day bulk optic spectrometers for sensing and chemical analysis wherever small size, stability and portability are essential. These new applications will all require continued improvements in planar waveguide spectrometer performance and reductions in size.

Of the many waveguide materials systems investigated to date, silica glass on silicon has come to dominate the commercial market for WDM planar waveguide devices. Extremely low loss and uniform silica glass waveguides can be deposited on silicon using chemical vapor deposition [1,2,3,4,5,6] and flame hydrolysis [7,8,9,10,11]. Silicon itself has become the most widely used platform for large-scale planar waveguide circuits. Silicon is an inexpensive,

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mechanically strong platform that is the natural substrate for both conventional and high index contrast waveguide systems including silica waveguides, silicon oxynitride/silica waveguides, polymers, and more recently the silicon-on-insulator (SOI) system. Single crystal silicon wafers can be obtained with diameters up to eight and twelve inches, as a a result of demand from the microelectronics industry. From another perspective, it is possible that the most viable solution to the integration of active and passive device may be based on hybrid integration schemes. Examples of hybrid systems combining passive glass or silicon waveguide components with III–V based semiconductor lasers and detectors [12, 13, 14] rely on the underlying Silicon optical bench. Here again silicon comes to fore because of its mechanical properties and the existing fabrication and micromachining knowledge that can be applied.

In the future silicon is expected to play an increasing role in photonics as emphasis shifts from conventional waveguide devices to devices where the feature size becomes comparable to or less than the wavelength of light. In this regime the use of sub-μm waveguides and photonic crystal structures may significantly alter the photonic landscape, not only in scale but also in the types of functions and applications that can be implemented. The creation of these new microphotonic devices relies on the use of high-index contrast waveguides, and the commonly used platforms are silicon oxynitride/silica on silicon, and silicon-on-insulator. Although the technology of microphotonics is just beginning to emerge, it is clear that silicon is again the material of choice because of its excellent optical qualities and the scope of the fabrication technologies that can be brought to bear on the technical challenges.

A discussion of the intricate details involved in waveguide spectrometer design is well beyond the scope of this chapter. The objective will be to provide an overview of the interplay between material science and optical engineering that occurs in the development of demultiplexers and spectrometers on the silicon platform. In Sect. 2 of this chapter, the basic design and layout of the AWG and echelle grating demultiplexer will be reviewed. Section 3 will give an overview of the material and fabrication challenges and solutions encountered when making well-established silica waveguide based WDM demultiplexers and spectrometers. A similar discussion of the implementation of planar waveguide demultiplexer technology in the SOI platform is presented in Sect. 4 of this chapter, to highlight the special challenges encountered when working with high index contrast systems. High index contrast silicon oxynitride waveguides are also a topic of much interest. Although a discussion of silicon oxynitride devices has been omitted, the parallel discussions of SOI and silica should have some relevance to this system as well.

## 2 Planar Waveguide WDM Components

Wavelength division multiplexing technology first attracted serious interest in the integrated optics community more than twenty years ago. It was then not

obvious how WDM would be eventually implemented, if ever, and the existing technology for time domain multiplexing (TDM) still had a considerable potential for improvement. Furthermore, prior to the advent of the erbium doped fibre amplifier (EDFA) there was still debate as to the wavelengths that would actually be used in fibre-optic links. The first demultiplexers were essentially miniature versions of grating devices found in bulk optic spectrometers. The basic principles of echelle grating spectrometers have been previously described for both free space and planar waveguide configurations [15,16,17]. One early device consisted of a three layer multimode glass waveguide with a diffraction grating mechanically ruled on one facet of the die, and multimode input and output fibres bonded to the other face of the die [18]. Other groups used similar designs but with holographic gratings written in glass [19], or wet etched silicon gratings [20] bonded onto one facet of the waveguide. A somewhat different approach to the same problem was demonstrated by *Chartier* et al. [21], who used ion-exchanged waveguides. The diffraction grating was produced by ion exchange through a mask to define the step grating structure. Because of the low index contrast between the ion-exchanged glass and normal glass, the grating efficiency of this device would be very small. These labor-intensive hybrid approaches illustrate that creating the grating facets was the biggest obstacle in making planar waveguide diffraction grating devices. This is still the key to implement the echelle design, but as will be discussed below, modern fabrication methods and tools can meet and overcome this challenge.

### 2.1 Arrayed Waveguide Grating Demultiplexer

The most significant development in planar waveguide demultiplexers came with the proposal by *Smit* [22] to replace the diffraction grating by an array of waveguides. The layout of such an arrayed waveguide grating demultiplexer (AWG) is shown in Fig. 1. The light is coupled into a single input waveguide leading to a slab waveguide splitter/combiner where it diffracts in the plane of the waveguide, illuminating an array of many waveguides. Each waveguide in the array section is longer than the adjacent waveguide by a constant length increment $\Delta L$. The array waveguide inputs are distributed evenly on the circular arc of radius $R$ that forms the boundary of the splitter section. In the simplest configuration the input waveguide is at the center of the circle so that the arc defines a line of constant phase for input light coupled to the splitter section. The array waveguides all converge at a second slab coupler which is often identical to the splitter. Because of the length increment between each array waveguide, the corresponding phase difference between light emerging from adjacent waveguides is $\Delta\phi(\lambda) = 2\pi\Delta Ln/\lambda$ where $n$ is the effective index of the fundamental waveguide mode. At the center wavelength $\lambda_0$ this phase shift is a multiple of $2\pi$, and the optical path in the output coupler simply mirrors the path through the input coupler, with the light being focused at the central output waveguide. As the wavelength is

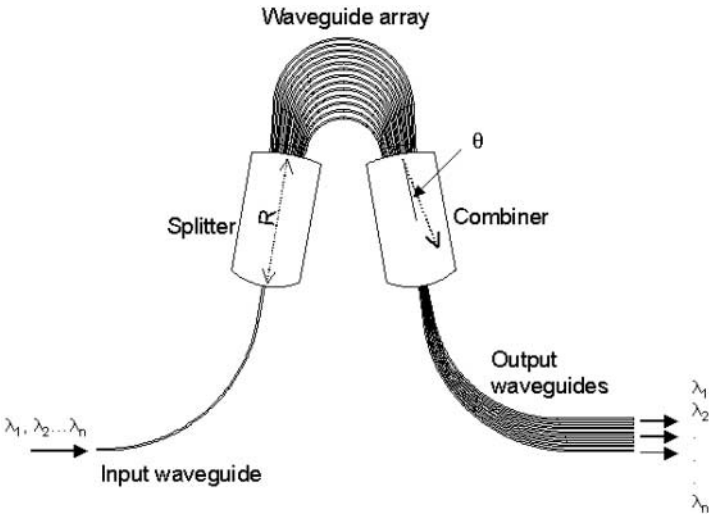


**Fig. 1.** Schematic layout of an arrayed waveguide grating demultiplexer

changed to $\lambda_0 + \Delta\lambda$ however, the phase increment is no longer an exact multiple of $2\pi$, and the beam is directed at an angle $\theta$ away from the center waveguide

$$\sin\theta = \frac{\lambda}{n_c d} \times \frac{\Delta\phi(\lambda) - \Delta\phi(\lambda_0)}{2\pi} . \tag{1}$$

Here $d$ is the separation of the array waveguide outputs, $n_c$ is the effective index of the combiner waveguide, and the order $M$ is defined in terms of the center wavelength $\lambda_0$ as $M = n_g \Delta L/\lambda_0$, where $n_g$ is the group effective index. Substituting $\Delta\phi(\lambda)$ into (1) gives the diffraction angle in terms of the wavelength shift $\Delta\lambda$

$$\sin\theta = -\frac{\Delta\lambda}{n_c d} \times M . \tag{2}$$

This has the same form as the grating equation that describes diffraction from a conventional ruled grating in Littrow configuration, when illuminated at normal incidence. Thus from a theoretical point of view the operation of a conventional grating and AWG are the same. The great advantage of the AWG is that fabrication requires only the ability to make single mode waveguides with low loss, and with sufficient reproducibility and uniformity that the relevant phase relationships between the optical paths through the array section are maintained. The phase relationships between the array waveguide outputs can be arbitrarily specified simply by assigning each array waveguide length. It is therefore possible to design very high order gratings, or gratings with unique phase distributions at the output of the array section – for example to modify the shape of the focused spot on the output waveguide. Since

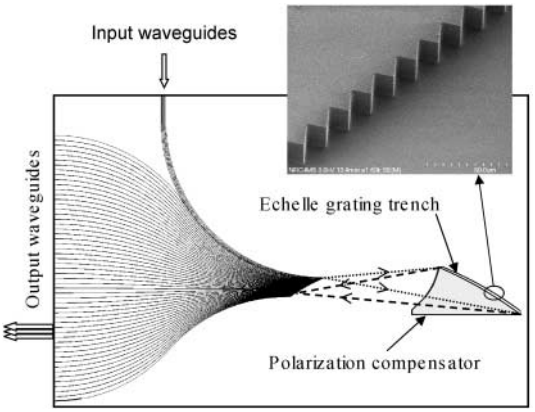


**Fig. 2.** Schematic layout of 48-channel echelle grating demultiplexer chip. *Inset* photograph shows magnified view of the grating trench

the first proposal by *Smit* [22], AWGs have evolved into a mature technology that is displacing the dielectric filter demultiplexer in the commercial telecommunications market. In the laboratory, AWG demultiplexers with more than 1000 channels have been demonstrated. There is already an extensive literature on the subject of AWG devices, and several recent reviews and articles on this subject can be found in [23].

### 2.2 Echelle Grating Demultiplexer

Since the development of the AWG demultiplexer, the telecommunications industry has neglected conventional diffraction grating for integrated WDM applications. This occurred because of a perceived difficulty in manufacturing planar waveguide diffraction grating devices. Although the operating principles basic of the diffraction gratings and AWGs are the same, three fundamental challenges in implementing planar waveguide diffraction gratings must be overcome. These are to fabricate vertical grating facets in a waveguide structure, to reduce the polarization dependence of the grating diffraction efficiency, and to eliminate or compensate the birefringence of the device.

Despite the difficulties faced in fabricating the device, the echelle grating (EG) does offer some compelling advantages. The EG configuration shown in Fig. 2 has a folded beam path and does not require the waveguide array, and so will be several times smaller than the equivalent AWG device. An EG device can also easily be scaled up to larger channel counts of more than 160 channels and smaller channel spacing. Similar scaling of AWG devices quickly leads to components of unmanageable size, because of the length increment conditions on the individual array waveguides. Some work has continued on echelle gratings based demultiplexers, but mainly in the III–V semiconductor systems [22, 25, 26, 27]. More recently, the feasibility of planar

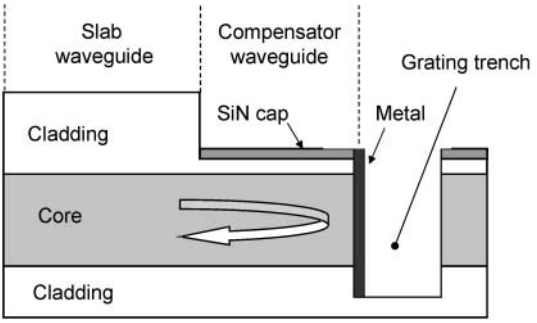


**Fig. 3.** Cross-sectional schematic view of the echelle grating device picture in Fig. 2, showing the layer structure of the slab waveguide, compensator waveguide, and the grating trench. The Si substrate is not shown

waveguide EG demultiplexers in glass has been demonstrated [28, 29]. The EG layout for a 48-channel glass device is shown in Fig. 2. The input waveguide terminates at the boundary of slab waveguide region where the light diverges and illuminates the echelle grating. Light is diffracted from the concave echelle grating and focused backwards towards the output waveguides. The angular dispersion of the diffracted light is again given by (2) in the case of illumination at normal incidence to the grating facets, where $M$ is the grating order. At any given wavelength, the grating will form an image of the input waveguide at the Rowland circle [16]. The output waveguides are positioned along this arc with spacing chosen to give the required wavelength channel separation. Figure 3 shows the corresponding cross-section view of the waveguide structure including the polarization compensator section and grating.

The prototype echelle waveguide structure consists of a 5 μm thick phosphorous doped silica glass (PSG) core surrounded by upper and lower cladding glass layers, with an index step of approximately 1% between the core and cladding. The layers are grown on a six inch silicon substrate using plasma enhanced chemical vapor deposition (PECVD). As shown in Fig. 3, the diffraction grating in Fig. 2 is formed by etching a 10 μm deep trench through the core layer, using a high density inductively coupled plasma system. The wall of the trench facing the input and output waveguides on the Rowland circle is stepped to form a $20^{\text{th}}$ order echelle grating. After etching the grating facet is metal coated to enhance the reflectivity. The ability to etch grating sidewalls that are flat and vertical to within $\pm 1^\circ$ is the key step to achieving acceptable insertion losses. A grating wall offset of only $1^\circ$ from the vertical will result in a coupling loss of more than 0.5 dB from the incident fundamental mode to the reflected fundamental mode. In addition to the insertion loss penalty, the lost light will be coupled to leaky modes of the slab waveguide that can eventually couple back into the input and output waveguides, and contribute to return loss, cross-talk and ghost peaks in the

channel spectra. Using an anisotropic etching process based on $C_4F_8$ and Ar gases, we have been able to consistently achieve grating walls with a sidewall angle between 89° and 90° as measured by scanning electron microscopy.

The diffraction efficiency of a metallized grating is polarization dependent due to the different electromagnetic boundary conditions for light polarized parallel and perpendicular to the metal–glass interface. By depositing metal only on the reflecting facet of each grating tooth in our planar waveguide grating, we were able to largely eliminate this effect and achieve planar waveguide diffraction gratings with a PDL of less than 0.2 dB across the entire C-band. As will be discussed in Sect. 3, the polarization birefringence effects intrinsic to glass waveguides were compensated using a polarization compensator section shown in Figs. 2 and 3. By adjusting the layer parameters of this compensator structure, TE-TM channel wavelength shifts of $\Delta\lambda = 10\,\text{pm}$ or less are routinely achieved.

Two versions of the final device were fabricated: a 48-channel echelle grating demultiplexer with 100 GHz channel spacing, and a 256-channel spectrometer chip with 25 GHz channel spacing. In both cases the basic fabrication processes were identical. The output channel spectra for the two devices are shown in Figs. 4 and 5. The fibre-to-fibre insertion loss for the 48-channel devices is approximately 4 dB, with a measured adjacent channel cross-talk better than −35 dB. The insertion loss for the 256-channel device is approximately 10 dB, while other performance parameters are similar to the 40-channel devices. In both devices the polarization dependent wavelength shift of the channel wavelengths was reduced to 10 pm or better. This similarity in performance for essentially identical fabrication procedures demonstrates the scalability of echelle gratings. The overall die size was $18 \times 17\,\text{mm}^2$ for the 48-channel device, and of $20 \times 40\,\text{mm}^2$ for the 256-channel device. A comparable 256-channel AWG device has dimensions of $75 \times 55\,\text{mm}^2$ [30], approximately five times the area of the EG chip. In competitive technologies such as AWGs, scaling up to 256 or more channels drastically increases device size, and accumulated phase errors in the array waveguides limit achievable cross-talk. That is not the case here, where the cross-talk is comparable for 40 and 256-channel devices.

We have presented two general approaches to planar waveguide demultiplexers in this section. The AWG is a mature technology that has been commercialized for a number of years, and is based on standard waveguide technology. The echelle grating approach has only been recently demonstrated on glass waveguides, and a number of unique challenges needed to be overcome to successfully fabricate this device. However, it has been established that EG devices with performance comparable to state of the art AWG demultiplexers can be fabricated in the silica-on-silicon system, using standard silicon fabrication tools. There are other approaches to planar waveguide demultiplexing which we cannot include here, such as the use of superprism effects in two-dimensional photonic crystals [31] and planar waveguide transmission

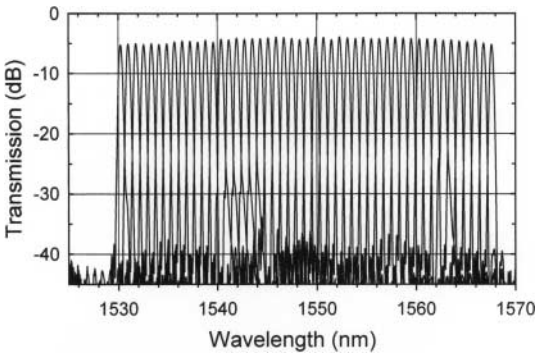


**Fig. 4.** Measured channel spectra for a 48-channel echelle grating demultiplexer

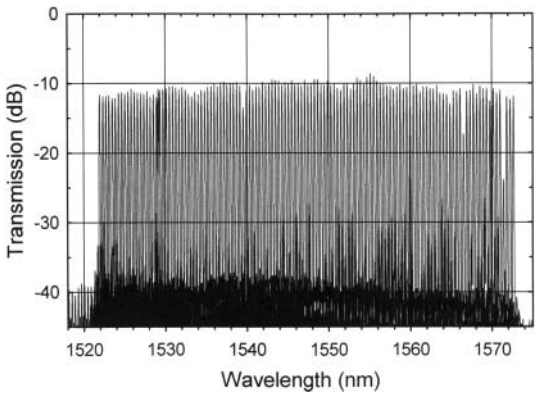


**Fig. 5.** Measured channel spectra for a 256-channel echelle grating demultiplexer

gratings [32]. These approaches have not yet been as extensively researched as the AWG and EG devices described, but many of the materials and fabrication issues will be similar. In the following sections this chapter will now focus on the specific materials and fabrication challenges in implementing AWG and EG demultiplexers on the silica-on-silicon and silicon-on-insulator platforms. The objective is to review how key issues such as polarization sensitivity and waveguide loss have been resolved in the more mature glass waveguide technology. Then approaches to the similar issues in silicon-on-insulator (SOI) will be explored, with the hope of shedding some light on the path to achieving extremely compact spectrometers and dispersive elements in high index contrast systems.

## 3 Silica Glass Waveguides on Silicon

Over the last decade, silica glass waveguides on silicon substrates have been the dominant platform for high performance passive waveguide components

such as WDM demultiplexers. Losses in glass are intrinsically lower than in most other materials at the wavelengths of interest for telecommunications. In glass optical fibre losses much less than 1 dB per kilometer are achieved. The techniques used to ensure compositional purity and uniformity in optical fibre manufacture cannot yet be reproduced in planar waveguide manufacturing, but waveguide losses of less than 0.1 dB/cm are routinely achieved in planar glass waveguides deposited on silicon [3, 33]. Glass waveguide core dimensions and cladding-core index steps can closely match those of optical fibre. The resulting good overlap between fibre and waveguide mode size eliminates the need for discrete coupling optics or mode matching structures. Although such coupling techniques are well known and used in the packaging of active III–V semiconductor devices, the added complexity and cost become prohibitive for waveguide multiplexers and demultiplexers with up to hundreds of input and output ports. In the case of glass waveguides well matched to optical fibre, coupling of fibre to numerous ports involves only alignment and attachment, and can be done in a single step using fibre ribbons mounted in silicon V-groove arrays.

### 3.1 Silica Glass Waveguide Growth

One must modify the refractive index of the glass in order to fabricate waveguides. In conventional glass waveguides where index steps of the order of $\Delta n = 0.01$ are used to define the waveguide core, small amount of dopants such as Ti, P, Ge, As, and B are incorporated during growth [7, 9, 11, 34]. In early work Ti was often used, but recently Ge doping has been more commonly employed. Ti doped glass has the disadvantage of having significantly higher losses for a given index step compared with Ge-doped glass. This may arise because Ti doping raises the melting temperature of glass making consolidation and homogenization of the glass by annealing less effective. Increasing the refractive index using P-doping has also been used, but P is a much more reactive element than Ge. As a result the growth chemistry may be more difficult to control, and unless the final glass structure is appropriately capped with an impermeable layer, P-doped silica glass (PSG) can degrade with time due to the absorption of water. Both P and B dopants are more commonly incorporated into glass as a means of lowering the melting temperature and modifying the thermal expansion coefficients, with the objective of reducing birefringence and planarizing the surface of the completed device.

Silica waveguides are commonly deposited using two techniques. Flame hydrolysis deposition (FHD) is capable of growing very thick glass layers [7, 8, 9, 10, 11]. In the case of silica waveguides optimized to match optical fibre waveguide mode sizes, the core is of the order of five to ten μm thick with upper and lower cladding layers up to several tens of μm thick. In FHD, a mixture of gases, including $SiCl_4$ are burned along with hydrogen and oxygen in a torch, depositing a fine soot of silica particles onto a silicon

substrate. Rotating the substrates wafer and/or scanning the torch position ensures uniform coverage. This layer of silica particles is then consolidated by heating the wafer to a temperatures of the order of 1200 °C or higher, so that the particles sinter together and a homogeneous silica layer is formed. Doping with Ti, Ge, P, N, B and As is accomplished by including appropriate compounds containing these elements in the burned mixture.

Recently silica deposition by plasma enhanced chemical vapor deposition (PECVD) has become accepted for waveguide manufacture [1, 2, 3, 4, 5, 6]. PECVD can also grow silica layers at rates of several hundred nanometers per minute, with excellent control over the uniformity of refractive index and layer thickness. In PECVD, a plasma is created between two parallel electrodes in the presence of a gas mixture consisting of $SiH_4$, $N_2O$ and a carrier gas such as He, Ar or $N_2$. The wafer itself is usually heated to a temperature of the order of 400 °C. These gases react on the surface of the wafer to form a layer of $SiO_2$. As in the case of FHD, the glass index and material properties are modified through incorporation of dopants during deposition by adding the appropriate precursor gases to the gas mixture. Simply varying the precursor gas ratios can be used to deposit layers of $SiO_xN_y$ with compositions and refractive index ranging from $SiO_2$ ($n = 1.46$) to $Si_3N_4$ ($n = 2.0$). Silicon oxynitride in particular has attracted considerable attention as a material for the fabrication of high index contrast waveguides [35]. PECVD is attractive because it is already a standard tool in the microelectronics industry, where PECVD silicon dioxide and silicon nitride are used as dielectrics for various applications. Commercial PECVD reactors intended for the semiconductor industry can easily be adapted to the manufacture of glass waveguides. PECVD deposition can also be carried out on a very large scale, for example some reactors can deposit oxide on tens or even hundreds of wafers at one time.

The quality of as-deposited PECVD glasses tends to be lower than those produced by FHD. The glass network often contains significant concentrations of hydrogen and nitrogen, which can contribute to waveguide absorption. In particular, strong absorption lines centered at $\lambda = 1480$ nm and $\lambda = 1510$ nm associated with overtones of the N-H and Si-H bonds often appear [1, 3, 36]. These lines can be particularly strong in silicon oxynitrides. Since the absorption features are very broad, they may contribute to demultiplexer insertion loss and channel nonuniformity in the C-band ($\lambda = 1525$ nm–1565 nm). The glass network also is not as complete as in a thermal or FHD grown oxide, with defects and voids that contribute to scattering losses and make the material susceptible to changes with time, for example as water is absorbed into the network. For this reason, PECVD grown glass for optical applications must be annealed at high temperatures of the order of $T = 1000$ °C [1, 3]. Annealing releases hydrogen trapped in the glass during growth, and plays a similar role to the high temperature anneal in FHD by consolidating and homogenizing the glass. After annealing,

waveguides grown by PECVD have excellent optical properties comparable to those achieved using FHD.

Waveguides fabricated in silica on silicon are usually buried channel waveguides, except where slab waveguides are required as in the combiner section of an AWG. Fabrication usually occurs in a series of steps in which first a lower cladding is deposited using FHD or PECVD, although a lower cladding layer of thermally grown oxide is often used. A doped silica layer with a slightly higher refractive index is then deposited to form the waveguide core. The planar waveguide circuit is then patterned on the core layer using conventional lithography tools, and defined using dry etching. The final step is to deposit an upper cladding layer over the structure.

### 3.2 Losses in Silica Waveguides

Compared with most optoelectronic materials the transparency of silica glass is excellent. However there are sources of waveguide loss that must eliminated, particularly when building to the specifications of the modern telecommunications industry, where total device insertion losses of less than a few dB are expected. These losses can arise from intrinsic material absorption as discussed previously, and light scattering. Rayleigh scattering is always present to some extent due to small index inhomogeneities and defects in the glass itself. Such intrinsic scattering can usually be minimized to acceptable levels through proper annealing of the glass to temperatures above which the glass becomes plastic. Scattering may also arise from roughness of the sidewall profiles of the ridge waveguides. This roughness is introduced by imperfections in lithography, or as an artifact of the etch process used to define the waveguides. This side-wall scattering is one of the critical issues in high index contrast waveguides systems such as silicon-on-insulator, and will be discussed in more detail in Sect. 4.2. In conventional glass waveguides the side-wall roughness is usually of the order of 10 nm to 50 nm in height, and the resulting loss has not been noted as a serious problem. Since the core-cladding index step is of the order of $\Delta n = 0.01$, scattering is very weak. Calculated losses for typical values of roughness are of the order of 0.1 dB/cm or less for buried glass channel waveguides, as shown in Fig. 6. However, as Fig. 6 illustrates, the induced loss for the same roughness can be much higher for high index contrast waveguides such as SOI.

Another source of scattering is the presence of cracks and defects. Such defects may arise during deposition of cladding layers over the high aspect ratio ridge waveguides, because the high stress occurring at the waveguide corners and variations in growth processes with the local substrate geometry (e.g. for deposition on vertical and horizontal surfaces and near sharp corners). If these defects are close enough to the waveguide core they can interact with the waveguide mode and contribute to the waveguide loss. Conformal overcladding coverage that avoids cracking can be achieved by building up the cladding using a series of depositions of thin layers, with appropriate

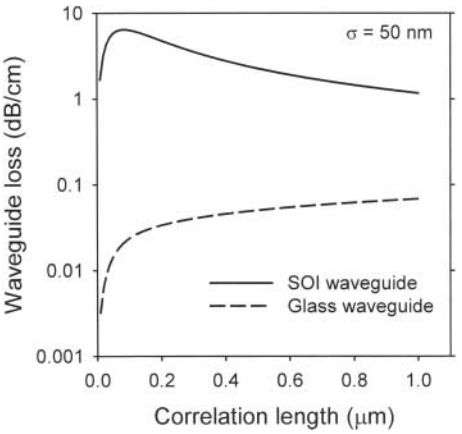


**Fig. 6.** Variation of the scattering induced loss with roughness correlation length in a buried glass waveguide and an SOI waveguide, both with dimensions $5\,\mu\text{m} \times 5\,\mu\text{m}$ and an assumed rms sidewall roughness of $\sigma = 50\,\text{nm}$. The *curves* are calculated using the model of Payne and Lacey [37]

anneals between each deposition. Dopants such as P and B are often used to lower the melting point of the cladding glass well below that of the core glass material, so that each layer in the sequence can be made to reflow and conform to the ridge waveguide profile, while the ridge itself retains its shape.

### 3.3 Polarization Dependent Properties of Silica Glass Waveguides

The polarization dependence of waveguides presents one of the most difficult challenges in the design of planar waveguide components using glass on silicon. Since optical fibers used in communications links are not polarization maintaining, any optical signal arriving at a waveguide chip will be in an arbitrary polarization state. Furthermore, this polarization can fluctuate randomly on time scales of minutes for buried fiber links or less than a second for above ground fibre links. Because of this random time variation, the polarization sensitivity in any component used to process the optical signal will be translated into signal noise.

The two fundamental polarization effects are polarization dependent loss (PDL) and birefringence. Intrinsic PDL is due to waveguide loss by scattering or absorption processes that are polarization dependent. Polarization dependent absorption is unlikely to occur in amorphous materials such as glass. However polarization dependent scattering can arise, for example, from residual roughness in the ridge waveguide side-walls. The boundary conditions for the electric fields normal and parallel to the interface between two dielectric media are different. The parallel component of the electric field $E$ must be continuous, while the normal component of the electric displacement $D = \varepsilon E$ must be continuous across the interface. Clearly this difference will result in polarization dependence of the scattering at a rough interface. Again, since the index contrast between cladding and core found in conventional glass

waveguides is small, this source of PDL has not been reported as a significant problem.

Waveguide birefringence refers to difference $\Delta n = n_{\mathrm{TE}} - n_{\mathrm{TM}}$ in effective indices $n_{\mathrm{TE}}$ and $n_{\mathrm{TM}}$ of the orthogonally polarized TE and TM waveguide modes. The transverse electric (TE) mode refers to the mode with electric field parallel to the plane of the waveguide. However, in the case of a channel waveguide, TE is often used to denote the mode with field parallel to the wafer plane. Similarly the transverse magnetic mode (TM) refers to the mode with the magnetic field parallel to the wafer plane (or electric field approximately normal to the wafer plane). Birefringence is present in any waveguide that is not perfectly symmetric in cross-section. As mentioned above, this geometric or modal birefringence is rooted in the different boundary conditions for electric field tangential and normal to the core-cladding interface. This difference means that the mode shape and effective index for TE and TM polarized modes differ in any waveguide that is not perfectly square or circular in cross-section. In high-index contrast waveguides such as SOI, the birefringence can be very large, unless stringent design rules are followed.

Birefringence changes the phase velocity of orthogonally polarized waveguide modes, so that the TE and TM polarized components of an optical signal become separated in time. This effect is known as polarization mode dispersion (PMD) and is a critical issue in optical fiber transmission. However, since planar waveguide components tend to be a few centimeters in length, the accumulated PMD is small, typically only of the order 100 femtoseconds. In cases where very high bit rates are used, or the signal must traverse many cascaded components, the on-chip PMD can become important. Birefringence also creates a shift in the effective wavelength of orthogonally polarized light, since wavelength inside the waveguide is $\lambda = \lambda_0/n$. Here the vacuum wavelength is $\lambda_0$ and waveguide mode effective index is $n$. For a given waveguide birefringence, $\Delta n$, the channel wavelengths in a demultiplexer will have a polarization dependent shift of $\Delta\lambda = \lambda_0 \Delta n/n_{\mathrm{g}}$ between TE and TM polarized light. This is the most important polarization effect in planar waveguide demultiplexers for WDM systems. If this shift is large it can result in significant inter-channel cross-talk and signal attenuation. Even if $\Delta\lambda$ is small relative to the channel pass-band, it can result in unacceptable PDL over much of the pass-band.

In low index contrast glass waveguides the geometrical birefringence can be quite small (e.g. $\Delta n \sim 10^{-5}$). The single most important source of birefringence is stress induced optical anisotropy. The thermal expansion coefficient of silica glass is $\alpha = 0.5\,\mathrm{ppm/^{\circ}C}$ while for silicon is ten times larger at approximately $\alpha = 5\,\mathrm{ppm/^{\circ}C}$. Since the glass is deposited at high temperatures, as the silicon substrate and glass system is cooled to room temperature the silicon tends to contract much more than the glass. If the glass layer remains bonded to the substrate and does not develop cracks, it will usually be under strong compressive stress at room temperature. On the other hand

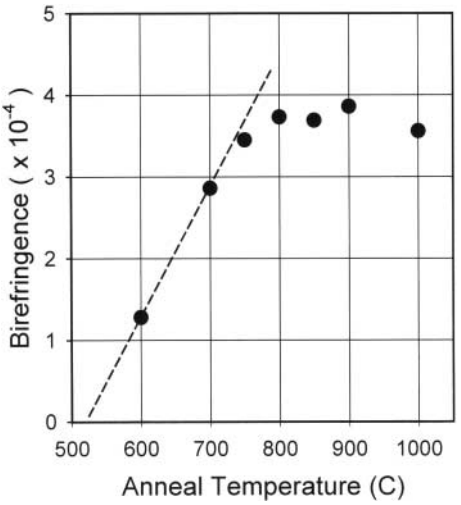


**Fig. 7.** Birefringence measured by Rayleigh scattering for PSG waveguides that have been annealed at temperatures from 600 °C to 1000 °C. The *dashed line* is the estimated extrapolation to zero birefringence [39]

stresses are also present even in the glass films at the deposition temperature. For example, PECVD glasses in some cases may even be under tensile stress, particularly if the as deposited material has microscopic voids and is non-stoichiometric. For this reason the stress of PECVD films can vary widely, and often displays complex behavior and hysteresis as the temperature is varied [38].

In the case of silica waveguide layers, some form of annealing at high temperatures is a critical step in producing material with acceptable optical properties. Annealing is usually done at temperatures near or above the temperature at which the glass deforms under plastic flow. At such temperatures the glass accommodates itself to the silicon substrate and stress will vanish. Stress is only frozen in when the temperature falls below the point where glass becomes rigid. Figure 7 illustrates that the final thermal stress at room temperature depends mainly on the difference between the plastic flow temperature and room temperature rather than initial deposition conditions. Figure 7 shows the stress induced birefringence measured in PSG glass waveguides for several different anneal temperatures. In this case the stress is frozen in only as the temperature falls below approximately 800 °C. After annealing the properties of the glass depend primarily on chemical composition rather than initial deposition conditions and growth chemistry. As a result, the stresses and corresponding optical birefringence built into glass waveguides of a similar chemical composition are remarkably similar whether FHD or PECVD deposition was employed. The stress in waveguide glass films is usually compressive and in the range of a few hundred MPa.

Stress and the resulting strain modify the optical properties and electronic structure of a material by changing the bond length and crystal symmetry at the microscopic level. Using the language of optically anisotropic crystals,

the strained silica behaves as a uniaxial crystal with the optic axis along the surface normal $z$-direction. The refractive index $n_{\mathrm{TE}}$ for TE light ($E$-field polarized in the $x$-$y$ or wafer plane) corresponds to the ordinary index while the index for TM polarized light ($E$-field along the $z$-direction) is the extraordinary index. The resulting refractive index changes can be cast in the formalism of the photoelastic effect, where the effect of strain $e_j$ on the index ellipsoid is expressed in terms of the photoelastic tensor $\mathrm{p}_{ij}$ as

$$\Delta \left(\frac{1}{n^2}\right)_i = p_{ij} e_j \,. \tag{3}$$

Contracted tensor notation is used here (i.e. $1 \to xx, 2 \to yy, 3 \to zz, 4 \to zy, 5 \to zx, 6 \to xy$). In isotropic materials this relation can be simplified to give the strain induced change in index $\Delta n_i$ for light polarized along the $i$-axis

$$\Delta n_i = -0.5 n^3 p_{ij} e_j \,. \tag{4}$$

In an alternate formulation in terms of the stress $\sigma_i$, (2) can be rewritten as

$$\Delta n_i = -C_{ij} \sigma_j \,, \tag{5}$$

where $\mathrm{C}_{ij}$ is the stress-optic tensor [40]. In the case of isotropic materials only tensor elements $p_{11}$ (or $C_{11}$) and $p_{12}$ (or $C_{12}$) and elements related by permutation of the coordinate axes are non-zero. The stress-optic and strain-optic tensor elements are related by the mechanical constants of the materials: Poisson's ratio $\mu$ and Young's modulus $E$,

$$\begin{aligned} C_{11} &= \frac{n^3}{2E} \left[ p_{11} - 2\mu p_{12} \right] \,, \\ C_{12} &= \frac{n^3}{2E} \left[ (1-\mu) p_{12} - \mu p_{11} \right] \,. \end{aligned} \tag{6}$$

A glass film grown on a silicon substrate will be under biaxial stress in the plane of wafer ($\sigma_1 = \sigma_2$), but is under no stress in the surface normal direction ($\sigma_3 = 0$) since the upper surface is free. The stress induced refractive index changes for light polarized in the wafer plane ($\Delta n_1 = \Delta n_2$) and normal to the plane ($\Delta n_3$) will then have the form

$$\begin{aligned} \Delta n_1 &= -\left(C_{11} + C_{12}\right) \sigma_1 \\ \Delta n_3 &= -2 C_{12} \sigma_1 \,, \end{aligned} \tag{7}$$

and the corresponding birefringence due to the in plane stress is $\Delta n = \Delta n_1 - \Delta n_3 = (C_{12} - C_{11}) \sigma_1$, where in the context of a planar waveguide film $n_1$ is the index for TE polarized light and $n_3$ is the index for TM polarized light. Taking the physical parameters for fused silica ($p_{11} = 0.121$, $p_{12} = 0.270$, $E = 70\,\mathrm{GPa}$, $\mu = 0.17$ [41]), and assuming a typical in-plane stress for a silica

on silicon layer of −300 MPa, (1) through (5) predict an optical birefringence of $\Delta n = -0.0013$ and a positive shift of 0.0025 in the overall refractive index (i.e. the average of the TE and TM indices). These shifts are small, but they are two orders of magnitude larger than the geometrical waveguide birefringence. The birefringence will produce an effective wavelength difference between TE and TM polarized light of $\Delta\lambda = 1.3\,\text{nm}$. In a standard WDM system based on the 100 GHz ($\sim 0.8\,\text{nm}$) channel spacing ITU grid, this is almost twice the channel spacing, rendering the device unusable for randomly polarized optical signals. The calculated $\Delta n$ in this example is somewhat high compared with that actually measured in commercially available planar glass waveguides. However, measurements in our laboratory on waveguides from several vendors yield birefringence values scattered throughout the range from $\Delta n = -0.0004$ to $\Delta n = -0.001$. Without correction, these values will produce polarization induced channel wavelength shifts comparable to a full channel spacing.

The discussion so far has considered the case of a planar slab waveguide only. In silica devices the waveguide is actually in the form of a ridge or buried channel. In cases where the cladding layers have similar thermal expansion coefficients as the core glass layers, the procedure outlined above can still provide a good estimate of the TE-TM waveguide birefringence in buried channel silica waveguides.

From the previous discussion, it is obvious that controlling stress birefringence is one of the fundamental challenges in implementing glass waveguides based components for WDM systems. As WDM technology has evolved over the last decade, a number of approaches have been proposed and demonstrated. The simplest and most conceptually elegant approach is to interchange the polarization states of orthogonally polarized optical signals inside the devices. It was shown by *Takahashi* and *Hibino* [30, 42] that placing a zero-order half-wave plate in the waveguide array such that it intersects each array waveguide at the midpoint, polarization insensitive operation can be achieved. An AWG demultiplexer shown in Fig. 1 is symmetric about this midline, with the optical path length before and after polarization interchange exactly equal. The overall phase accumulation of any optical signal passing through an array waveguide with a wave plate will therefore be independent of initial polarization. This method of polarization compensation does add a number of additional process steps to cut a groove and insert and bond the wave plate. The groove and wave plate should be as thin as possible since the light diverges as it propagates across the wave plate gap, resulting in coupling loss at the opposite facet of the groove. In the original demonstration, the additional losses incurred by introducing the wave plate into 100 µm wide groove are about 5 dB [42]. More recently, by using a thin polyimide wave plate the total groove width has been reduced to only 18 µm, with a corresponding excess insertion loss of only 0.4 dB [30]. Despite these extra losses, the wave plate technique effectively decouples the polarization

compensation problem from the material properties, and can be applied in any waveguide material system. The polarization interchange approach is effective in devices such as an AWG where there is a clear symmetry plane in the optical paths, and is now one of the accepted techniques in AWG manufacture. On the other hand, devices such as the echelle grating demultiplexer shown in Fig. 2 have no symmetry plane and other methods of polarization compensation must be used.

In devices based on buried channel waveguides, stress itself can be manipulated to correct for birefringence effects. By including the dopants B and P in silica glass (BPSG), the thermal expansion coefficient of the glass silica can be tailored to closely match that of silicon. One solution is then to use BPSG as the waveguide core material, so that the thermal stress in the core always remains close to zero [43,44]. Unfortunately in practice it has been found that BPSG of the appropriate composition has higher optical loss and may even degrade with time. BPSG can be equally effective though, when used as the waveguide cladding [11, 45] as shown in Fig. 8. In this case, as the wafer is cooled from the annealing temperature, the BPSG cladding applies a stress to the buried silica channel in the surface normal direction that is close to the stress induced by the silicon substrate. The net result is that while the isotropic compressive stress will still shift the index of refraction, the birefringence anisotropy can be largely eliminated. This technique has been referred to as stress balancing, and has been adopted as a manufacturable method for eliminating birefringence effects in glass AWG waveguides. The use of BPSG glass as the upper cladding is also useful because of the low melting point of BPSG glass. Since each cladding layer can be annealed and undergo reflow, good conformal coverage of the cladding is achieved and the final waveguide structure can be fully planarized. The stress balancing method can only be applied to buried channel waveguides, since the stress must be applied along the surface normal direction to balance the in-plane stress applied by the silicon substrate. Therefore, although it may be the most attractive approach for birefringence control in devices based on buried channel waveguide structures, it is not possible to apply stress balancing in devices involving a slab waveguide, such as the echelle grating demultiplexer.

Glass waveguides can be made birefringence free through the use of a birefringence compensating layer (BCL), as shown in Fig. 9 [46]. The BCL concept is an extension of the concept of form birefringence [15]. In an artificial material consisting of alternating layers of high and low index materials, the refractive index will be different for light polarized parallel and perpendicular to the layer plane. This anisotropy, known as form birefringence, has been used to artificially induce a strong birefringence in nonlinear waveguides to allow phase matching of wavelength conversion processes [47]. In the work of *Wörhoff* et al. [46], the form birefringence is used instead to eliminate waveguide birefringence. The BCL is a thin layer of silicon nitride with $n \sim 2$ placed in contact with the waveguide core. If the thickness and index of the

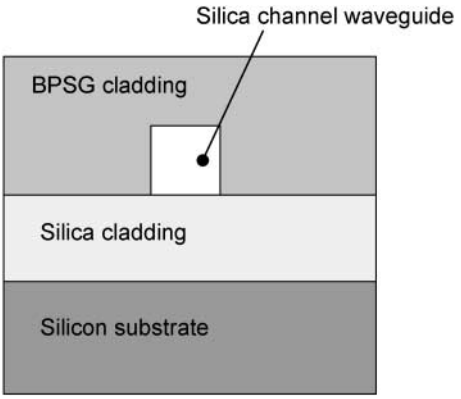


**Fig. 8.** Buried channel waveguide with a BPSG cladding for birefringence compensation by stress balancing

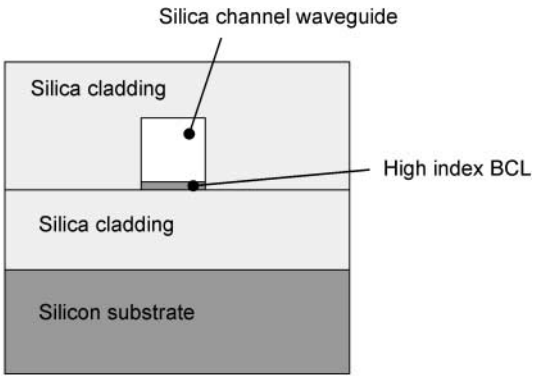


**Fig. 9.** Cross-section of a silica buried channel waveguide using a high index birefringence compensating layer [46]

BCL are correctly chosen, the resulting form birefringence can be used to cancel out the stress and geometrical components of the birefringence. The thickness of the BCL layer in [46] was approximately 26 nm to eliminate the birefringence of a 3 microm wide silica channel waveguide. An uncertainty of $\pm 10$ nm in the deposited BCL thickness can result in potential errors in demultiplexer channel wavelength shift of $\pm 0.2$ nm. However, the BCL method can be used to compensate both ridge and slab waveguides, and hence can be used to fabricate polarization independent AWG and echelle grating demultiplexers.

Other solutions to the waveguide birefringence problem involve direct changes to the structure of the waveguide itself. The geometrical contribution to the birefringence depends directly on waveguide aspect ratio, the birefringence being largest for a slab waveguide and zero for a waveguide of square cross section. In glass, manipulation of waveguide aspect ratio is of little use since the stress birefringence completely dominates the waveguide

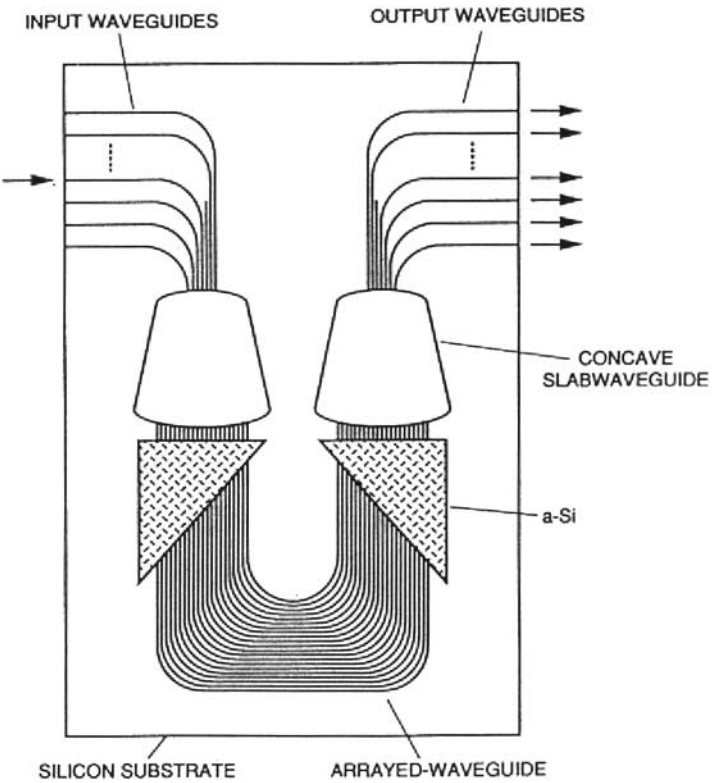


**Fig. 10.** AWG with two a-Si polarization compensation patches [48]

birefringence. However, aspect ratio can be a very useful tool for controlling birefringence in high index contrast waveguides.

It is not always necessary to eliminate birefringence. If the local waveguide birefringence can be modified it is often possible to design polarization independent devices using polarization compensation techniques. The first such polarization compensator was demonstrated on an AWG device shown in Fig. 10 [48]. The waveguide birefringence in the two triangular patches on the waveguide array is modified using an a-Si overlayer. This overlayer applies an additional stress to the underlying buried channel waveguides, modifying the birefringence. In an AWG with no compensator, the phase of TE polarized light in arriving at the output of array waveguide $i$ is related to the phase of the light at the output of waveguide $i+1$ by a constant $\Delta\phi_{\mathrm{TE}} = k_0 n_{\mathrm{TE}} (L_{i+1} - L_i)$. Here $n_{\mathrm{TE}}$ is the effective index of the TE mode, $k_0$ is the vacuum wavevector, and $\Delta L = (L_{i+1} - L_i)$ is the length increment between array waveguides $i$ and $i+1$. If the waveguide is birefringent, then the phase increment of the TM polarized light arriving at the array output will be $\Delta\phi_{\mathrm{TM}} = k_0 n_{\mathrm{TM}} (L_{i+1} - L_i)$. The difference between $\Delta\phi_{\mathrm{TE}}$ and

$\Delta\phi_{\mathrm{TM}}$ will cause the TM and TE polarized light to be diffracted in slightly different directions in the output combiner, and is the source of $\Delta\lambda$, the polarization dependent shift in demultiplexer channel wavelength. When the polarization compensator sections are added as in Fig. 10, each waveguide will have an unmodified length $L_i - L_i'$ with effective indices $n_{\mathrm{TE}}$ and $n_{\mathrm{TM}}$, and a modified length $L_i'$ with indices $n'_{\mathrm{TE}}$ and $n'_{\mathrm{TM}}$. The compensator patch dimensions can be chosen such that the phase increment is polarization independent, i.e. $\Delta\phi_{\mathrm{TE}} = \Delta\phi_{\mathrm{TM}}$ for all waveguides in the array. Imposing this condition on the phases defines the lengths $L_i'$ of the modified waveguides in the compensator section

$$L'_{i+1} - L'_i = \frac{\Delta n}{\Delta n - \Delta n'} (L_{i+1} - L_i) \; . \tag{8}$$

Here $\Delta n$ and $\Delta n'$ are the effective index birefringences of the unmodified and modified waveguides, respectively. Compensators of this form have been demonstrated in silica on silicon AWGs [48] and also in InP/InGaAsP AWG devices [48]. Implementing this method requires a manufacturable way of changing the local waveguide birefringence enough that the intrinsic stress birefringence can be compensated. Techniques to achieve this for ridge waveguides in AWG include the deposition of a-Si films on the compensator section, to apply additional stress to the underlying ridge waveguides. Using this technique polarization dependent channel shifts less than 0.01 nm have been achieved in a silica demultiplexer [48].

The important advantage of the compensator approach is that it is the one technique that can easily be adapted to echelle grating demultiplexer devices. It has been shown be *He* et al. [50] that the compensator concept can be extended naturally to the slab waveguide section in an echelle grating spectrometer (see Fig. 2) and also to the combiner/splitter section of an AWG [51]. In both cases the formulation of the compensator shape is identical to (8) except that the lengths $L_i$ and $L_i'$ now refer to the path lengths of two rays traced from the input waveguide through two adjacent array waveguides to the output waveguide, rather than the length of the array waveguides alone. In effect the triangular compensator section has simply been moved from the array section as in Fig. 10 to the slab waveguide sections.

When originally demonstrated in InP/InGaAsP waveguides, the compensator birefringence was modified simply by etching away a thin layer from the top of the waveguide. This same approach can be used to form compensators in glass AWG devices or echelle grating devices. However, because the stress induced birefringence is so large, all of the upper cladding and part of the waveguide core must be removed to achieve full compensation. This in turn causes a significant waveguide mode mismatch at the boundary between the unmodified slab waveguide and the compensator. This mode mismatch contributes to the overall insertion loss of the device, and since the mode mismatch is itself polarization dependent, it also contributes to the

polarization dependent loss (PDL). Hence an alternative method for modifying birefringence is necessary to compensate glass echelle grating devices. The solution we have found [28, 29] is similar to the BCL layer technique proposed by *Wörhoff* et al. [46]. Unlike the BCL layer, we use a very thin high index layer to shift the birefringence of the compensator slightly, but not eliminate it. The structure of the compensator is shown in Fig. 3. The upper silica cladding is etched until approximately 1 μm of material is left. This layer of silicon nitride with an index of $n \sim 2$ is deposited on top of the remaining cladding. As the light travels through the compensator the upper tail of the waveguide mode propagates in the silicon nitride layer. This interaction of the mode with the silicon nitride layer is polarization dependent, lowering the TM effective index relative to the TE effective index. The birefringence can be sufficiently enhanced that full polarization compensation can be achieved using a compensator of practical dimensions, as determined by (8). The critical feature of this compensator structure is that there is almost no change in the waveguide mode shape in the unmodified slab waveguide and the compensator waveguide. The addition insertion loss and PDL associated with this compensator structure are negligible. The polarization dependent wavelength shift $\Delta\lambda$ in our echelle grating devices described in Sect. 2 is routinely reduced from about 500 pm to less than 10 pm using this form of compensation.

## 4 Silicon-On-Insulator Waveguides

Although glass on silicon has evolved rapidly into a commercially viable waveguide platform, there has always been a strong interest in silicon compatible semiconductor waveguides because of the size reduction that could be achieved, and also the hope that silicon based active and passive optoelectronic devices could be integrated on chip. Although silicon-germanium waveguides were an early candidate in this role, the issues of lattice mismatch stress have so far curtailed its application for passive waveguides [52]. Silicon-on-insulator (SOI) wafers consist of a silicon substrate, a thin oxide layer on top of which is a thin single crystal layer of silicon. This top layer of silicon can act as a waveguide with the buried oxide layer providing vertical optical confinement. Photonic circuits can then be defined by etching the silicon to form ridge waveguides. SOI wafers fabricated by implantation of oxygen ions (SIMOX) were initially of poor optical quality [53]. Recently, new fabrication techniques have been developed to produce SOI wafers, and their availability and quality has improved tremendously. This is in large part due to the demand for SOI from the microelectronics industry for a variety of high-speed applications. The SOI waveguide system has now been demonstrated as a commercially viable platform for photonic integrated circuits [14]. Because of its high index contrast, it has also become an attractive platform for research in microphotonics and photonic crystal devices.

The technical issues encountered in creating a viable SOI waveguide technology are nominally similar to those that had to be met in the silica glass on silicon system – minimizing waveguide loss and controlling polarization effects. However, the engineering approaches can be very different. Glass waveguides are intrinsically multicomponent systems and achieving viable optical material requires good understanding and control over chemical composition and thermal processing.

The silicon guiding layer in SOI is a high purity single component material, and there are effectively no chemical or thermal processing degrees of freedom. The Si is also single crystal. Compared with glass technology, the intrinsic material uniformity is one of the advantages of the SOI platform. However, because of the high index contrast between the Si waveguide core and surrounding cladding (e.g. usually an oxide), details of waveguide geometry and dimension play a central role in determining the performance of SOI waveguides. For example in SOI the waveguide losses are largely determined by the roughness of the side-walls of the waveguide. Unlike silica glass on silicon, the waveguide layer in SOI has precisely the same thermal expansion coefficient as the substrate and there should be no stress-induce birefringence. However, because of the high index contrast between core and cladding the boundary conditions for the electric fields tangential and perpendicular to the core-cladding interface create a very strong geometrical birefringence. These effects become stronger as the waveguide size scales down to the microphotonic regime, where the modal electric field becomes quite large at the interface and even outside the waveguide core.

In the following, we again explore the critical issues in designing and fabricating high performance waveguides for WDM and other demanding applications, in particular as they relate to making microphotonic components, an area where SOI will most likely have a true niche. Research in SOI is less mature than in glass waveguides, but many of the design solutions reported to date closely parallel similar developments in glass waveguides.

### 4.1 Mode Control in SOI Waveguides

The issue of waveguide mode control arises in high index contrast materials systems. In silica waveguides, the core/cladding index step is usually so small that waveguides can easily be designed to be single mode. On the other hand, SOI waveguides larger than a few hundred nanometers in cross-section will support many modes. Each mode has a slightly different effective index, and therefore in a demultiplexer each mode will have a different effective wavelength. Thus when higher order modes are present, the output of each demultiplexer channel will have peaks or side lobes at a series of wavelengths corresponding to the modes in the demultiplexer waveguide array (or the slab waveguide in the case of an echelle grating demultiplexer). The peak corresponding to the fundamental mode is at the design channel wavelength, while the ghost peaks contribute to cross-talk. Side lobes due to higher order

modes have been observed in SOI demultiplexer spectra [54]. The amplitude of these side lobes will depend on the details of mode conversion processes occurring in the device.

Higher order slab modes in the combiner section of an AWG will create ghost peaks shifted slightly from the channel center wavelength. The relative shift $\Delta\lambda_{01}$ in peak wavelength $\lambda_m$ for channel $m$, between light in the fundamental mode and first higher order mode, will be proportional to the difference in their effective indices and the difference between $\lambda_m$ and the AWG center wavelength $\lambda_0$, i.e. $\Delta\lambda_{01} = (\lambda_m - \lambda_0)(n_0 - n_1)/n_1$. Assuming the usable bandwidth of a typical demultiplexer covers the C-band, this relation predicts that if excited, the second mode could introduce a ghost peak separated by approximately 0.1 nm from the peak wavelength, assuming typical SOI slab waveguide thickness of a few μm. This is much less than the standard 100 GHz (0.8 nm) channel spacing but be enough to cause noticeable distortions in the channel transmission spectrum.

On the other hand, if the fundamental and first modes are also present in the array waveguides, the modal wavelength shift may be estimated using the relation $\Delta\lambda_{01}/\lambda_0 = (n_1 - n_0)/n_0$. In this case modal ghost peaks will occur at a much larger shift of 10 nm or more from the design wavelength, and severely degrade the nonadjacent channel cross-talk of the device. This large wavelength shift would also occur in the case of an echelle grating demultiplexer, where the dispersive section is a slab waveguide. It may be attractive to fabricate an echelle grating demultiplexer in SOI, given the small sizes that can be achieved. However, given the above considerations, it is clear that some form of mode suppression will be a key element in the design of such devices.

Considerable attention has been given to the issue of higher order mode suppression in SOI waveguides [55, 56, 57, 58]. Although slab waveguides will support a number of slab modes, SOI ridge waveguides can be designed to have a width and an etch depth such that only the fundamental mode is supported. It has been shown that ridge waveguide will be single mode if the waveguide width $W$, height $H$, and ratio $r$ of lateral cladding thickness $h$ to ridge height $H$ (see Fig. 11) satisfy the relationship

$$\frac{W}{H} \leq 0.3 + \frac{r}{\sqrt{1 - r^2}}\,. \tag{9}$$

Complying with this condition is straightforward for ridge waveguides used in SOI AWG demultiplexers.

As will be discussed in the next section, modifying ridge profile is another method to achieve zero polarization birefringence. As noted by *Pearson* et al. [59], it may not be possible to simultaneously satisfy the single mode condition and the requirement that the waveguide have zero birefringence. When competing requirements of polarization insensitivity and minimizing bend loss make it difficult to satisfy the single mode relationship of (9), it

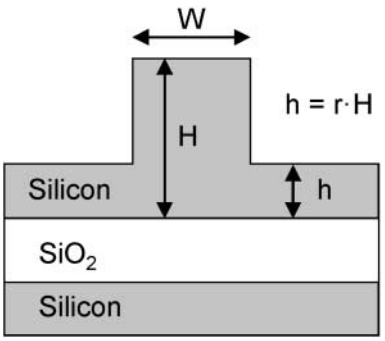


**Fig. 11.** SOI waveguide cross-section illustrating the critical dimensions for determining the single mode condition

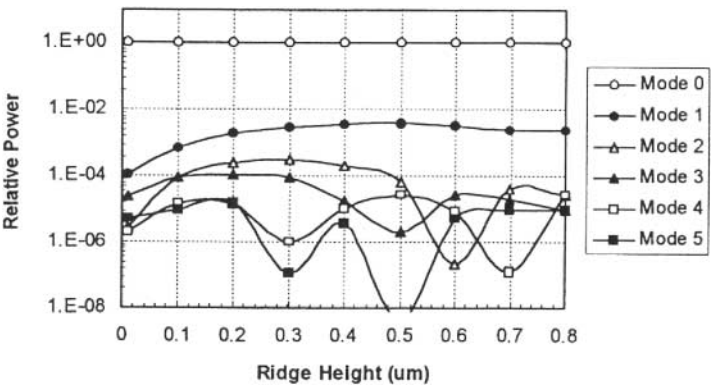


**Fig. 12.** Coupling efficiency from the fundamental ridge waveguide mode to the fundamental and higher order slab waveguide modes in a 1.5 μm thick SOI structure [59]

is still possible to work with multimode waveguides provided mode filtering is used. *Pearson* et al. [59] showed that in an SOI based AWG, waveguides supporting higher order modes may be used when the waveguide bend radii are small enough that the losses for the fundamental mode are negligible while losses for the second and higher order modes are extremely large. In this case only the fundamental mode will contribute to the AWG channel spectrum.

At present there are no known methods of suppressing higher order modes in a slab waveguide made out of high-index contrast material such as SOI. A multimode slab combiner section of an AWG can be tolerated provided that most of the optical power is coupled into the fundamental mode of the combiner at the point where the ridge waveguide joins the slab section [59]. Figure 11 shows the calculated power coupled to the first few slab modes from a single mode ridge waveguide, in 1.5 μm thick SOI. The ratio of power coupled into the second slab mode to that in the fundamental mode will be less than −20 dB. Since light is coupled to and from the slab by single mode

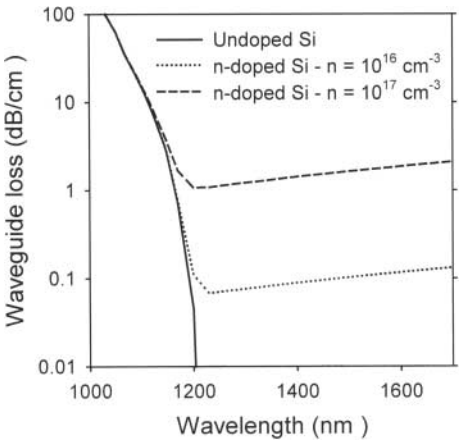


**Fig. 13.** Optical loss coefficient including interband absorption and free carrier absorption in intrinsic and doped silicon

ridge waveguides, this suggests that in this case the contribution of the second mode to the AWG output spectrum will be suppressed by more than −40 dB.

### 4.2 Losses in SOI Waveguides

Intrinsic loss in undoped single crystal silicon is very low for wavelengths longer than the absorption edge near 1100 nm, and reported losses in large cross-section processed waveguides are as low as 0.1 dB/cm in the near infrared [60, 61]. In the case of doped silicon waveguides, free carrier induced absorption varies linearly with the density of electrons and holes [62]. Figure 13 shows the calculated absorption due to interband transitions and doping in silicon. The loss due to free carriers does not become significant until carrier densities much higher than $10^{16}$ are reached. Although doping is not an issue for passive waveguide devices, in cases where active functions such as variable optical attenuators (VOA) [63] are integrated on chip, the overlap of the waveguide mode with doped areas must be minimized.

The more important source of loss in SOI waveguides is scattering from roughness at the waveguide cladding interface. The roughness can be qualitatively characterized by a root-mean square roughness $\sigma$, a measure of the typical height of the asperity, and the correlation length $l_c$, which is a measure of the width of an asperity. *Payne* and *Lacey* [37] derived a relation for the upper bound of the scattering loss coefficient for a waveguide of core index $n_1$ and width $d$

$$\alpha \leq \frac{\sigma^2}{k_0 d^4 n_1} \kappa \,. \tag{10}$$

Here $\kappa$ depends on the details of the waveguide geometry and the statistical distribution of the roughness, but is of order unity for most practical waveguide geometries. This relation predicts that for any given roughness,

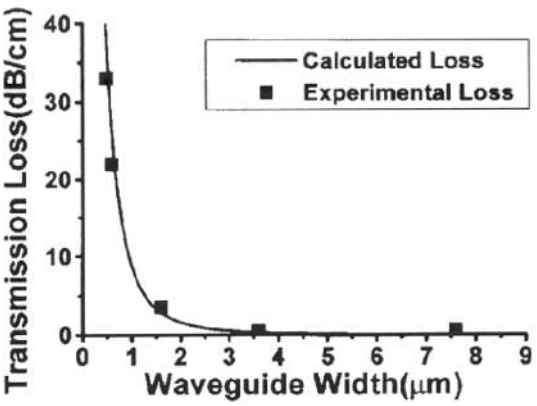


**Fig. 14.** Calculated and measured variation of waveguide loss with ridge width for silicon-on-insulator waveguides [64]

the scattering loss will increase rapidly as waveguide dimensions are reduced. Reducing scattering loss will be one of the major challenges to overcome in developing high performance microphotonic components. With modern dry etching tools such as reactive ion etching, rms roughness and correlation lengths of the order 100 nm or less may be achieved. Figure 6 shows a comparison of loss for the case of a 5 μm square glass waveguide and a 5 μm square SOI waveguide, and illustrates the importance of scattering loss in SOI. As the waveguide dimensions are scaled down the loss due to roughness scattering becomes very large [37, 64], as illustrated by the calculations of *Lee* et al. shown in Fig. 14 [64]. Unfortunately, it may not be straightforward to improve the side wall roughness that results during conventional lithography and dry etching. Thus if microphotonic waveguide and photonic crystal devices are ever to become practical, other means of creating smooth interfaces must be found.

By far the simplest approach to eliminating loss is to keep the waveguide dimensions so large (e.g. $> 5\,\mu m$) that the side-wall scattering is negligible. For example, a four channel AWG demultiplexer has been fabricated in the SOI platform using waveguide cross-sections with dimensions of approximately 5 μm [54]. On-chip insertion loss for the 2.7 cm long device is less than 6 dB. More recently commercial SOI based AWGs with much higher channel counts have been developed [63], with performance approaching that of silica glass demultiplexers. However, the reliance on large waveguide size means the devices must also be large – in fact comparable to the size of silica AWGs – and therefore abandons the promise of a silicon-based microphotonic platform for very high levels of integration. Pursuing this promise is one motivation for the ongoing search for improved waveguide fabrication techniques.

Dry etching techniques could also be abandoned altogether in favor of using wet etches for waveguide definition [64]. Lee et al. have reported that wet etching can reduce the rms roughness of a silicon side-wall from 10 nm to 2 nm. Most wet etches are anisotropic. Since the (111) set of planes usually have the slowest etch rate, wet etching often results in the preferential formation of smooth (111) facets. Thus wet etching is highly constrained with respect to the device geometries that can be fabricated. For example, if an anisotropic wet etch process is used to fabricate curved ridge waveguides, the width and profile of the ridge will vary with the angle of the waveguide relative to the crystal planes.

Given that dry etches are necessary to create complex waveguide circuits, roughness may be removed after ridge definition. One approach is to remove the residual roughness using a thermal oxidation [65]. Once the silicon waveguide has been etched using standard processes, the silicon is oxidized at high temperatures in steam. As the oxide forms, silicon is consumed faster in asperities than on flat planes, so that the oxide-silicon interface becomes flatter with increasing oxidation time. Initial results show that this method produces sidewalls with an rms roughness $\sigma$ of less than 2 nm, comparable to those formed by wet etching. However more recent results also suggest that the degree to which roughness decreases saturates with increasing oxidation time, to $\sigma$ values near 0.5 nm [66]. This limit may be sufficiently small that for total propagation lengths envisaged in microphotonic components, the scattering losses are acceptable.

To conclude this section, the control of scattering losses at the core-cladding interface is a key step in scaling down high performance optical components base on high index contract systems such as SOI. Preliminary work has demonstrated that methods for eliminating roughness are available, but these have not yet been proven on manufacturable working devices such as compact demultiplexer chips. The polarization dependence of sidewall scattering has not been extensively addressed theoretically or experimentally, and may play a role in determining device PDL in high index contrast waveguides.

### 4.3 Polarization Dependent Properties of SOI Waveguide Devices

Turning attention once again to dispersive devices specifically for WDM and other high performance applications, as in silica the control of waveguide birefringence is essential. Unlike silica on silicon, there is only minimal built-in stress in the SOI waveguiding layer, since the Si waveguide core has the same mechanical properties as the Si substrate. Hence the primary source of birefringence in SOI waveguides is the geometrical contribution. Figure 15 shows the calculated variation of the geometrical waveguide birefringence of an SOI slab waveguide with thickness. Two curves are shown, one corresponding to the effective index birefringence $\Delta n$ and the second to the waveguide group index birefringence $\Delta n_g$. As noted by *Vivien* et al. [58], in the case of SOI

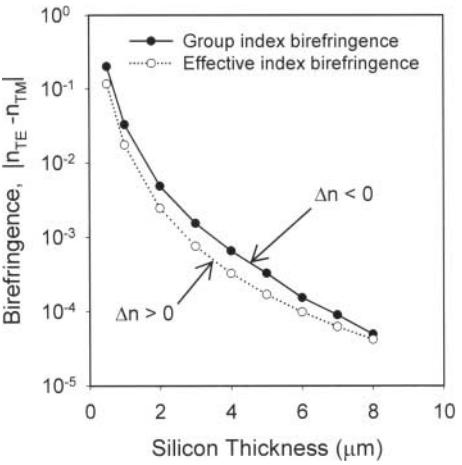


**Fig. 15.** Variation of the effective index birefringence $\Delta n$ and the group index birefringence $\Delta n_{\mathrm{g}}$ with silicon thickness for an SOI slab waveguide at $\lambda = 1550\,\mathrm{nm}$

the group index birefringence is opposite in sign and slightly larger than $\Delta n$. The polarization dependent wavelength shift $\Delta\lambda$ depends on the effective index birefringence, even though the dispersion of a spectrometer will depend on the group index. The effective index birefringence can cause a wavelength shift $\Delta\lambda = \lambda_0(\Delta n/n_{\mathrm{g}})$, while in the worst case the group index birefringence will cause a shift $\Delta\lambda = \lambda_{\mathrm{BW}}(\Delta n_{\mathrm{g}}/n_{\mathrm{g}})$, where $\lambda_{\mathrm{BW}}$ is the usable spectrometer bandwidth. This usable wavelength range is typically two orders of magnitude smaller than the wavelength. As a result, the group index birefringence will cause a much smaller change in any channel wavelength than the effective index birefringence. Compensation methods must therefore primarily counteract the polarization dependence of the effective index. Fortunately, the methods that minimize $\Delta n$ also suppress $\Delta n_{\mathrm{g}}$, although the conditions for zero birefringence will not be exactly the same [58].

Given that the polarization dependent channel wavelength shift in a WDM system demultiplexer should be of the order of $\Delta\lambda = 10\,\mathrm{pm}$ or smaller, $\Delta n/n_{\mathrm{g}}$ should be less than $10^{-5}$. Based on the results in Fig. 15, an SOI slab waveguide must be of the order of $10\,\mu\mathrm{m}$ or thicker to meet this criterium. Since such a large thickness is not practical for most integrated optics applications, some form of polarization compensation is again required.

The high index contrast that is the source of the polarization birefringence in SOI waveguides also provides one method of compensating that birefringence. The simplest way to eliminate the geometrical birefringence is simply to make the waveguide as symmetrical as possible, for a perfectly square buried channel waveguide will have zero birefringence. In the case of SOI ridge waveguides, it has been shown that a ridge width and etch depth can usually be chosen for which either the effective index or group index are polarization independent [58, 59].

Since the dispersive element of an AWG consists of ridge waveguides, ridge shape can be used as a tool for polarization compensation. This has been

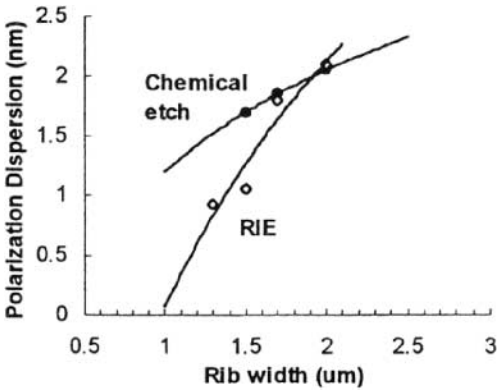


**Fig. 16.** Measured polarization dispersion (i.e. channel wavelength shift) in SOI AWG demultiplexers for different array waveguide rib widths. The ridge etch depth is 1 μm in all devices. Data is shown for sloped ridge sidewalls (wet etched) and vertical side walls (reactive ion etched) [59]

demonstrated in SOI by *Trinh* et al. in a four channel AWG [54] with a polarization dependent wavelength shift of $\Delta\lambda = 0.04$ nm and no other forms of compensation used. This AWG device was fabricated using 5 μm thick silicon waveguides, for which the birefringence is already small. This represents a factor of four reduction in birefringence compared with the 5 μm thick slab waveguide or a shallow etched ridge. Ridge waveguide compensation was also demonstrated by *Pearson* et al. in SOI microspectrometers based on 1.5 μm thick SOI [59]. Here, the measured channel shift $\Delta\lambda$ was reduced from the 4 nm expected for a slab waveguide, to $\Delta\lambda = 0.8$ nm. In both these examples full compensation was not achieved. One unresolved problem is that deeper etching would cause the array waveguides to become multimode, which would cause unwanted cross-talk. In many cases, single mode waveguides and polarization compensation cannot be achieved simultaneously for a given ridge profile.

Fabrication tolerance is another critical factor in compensating an AWG demultiplexer. Figure 16 shows the $\Delta\lambda$ measured at different ridge etch depths, for the SOI demultiplexer shown in Fig. 17. From the slopes of these curves, uncertainties in the array ridge widths of 100 nm lead to uncertainties in $\Delta\lambda$ of about 0.1 nm (or uncertainties in $\Delta n$ of $2 \times 10^{-5}$). *Vivien* et al. [58] show that for similar 1.5 μm thick waveguides, uncertainties of only ±10 nm in ridge etch depth result in wavelength shift compensation errors of similar magnitude. These results suggest that while ridge profile engineering is effective, it may be difficult to control with sufficient accuracy. As discussed in the previous section on SOI waveguide losses, ridge profile is also a design parameter that determines whether an SOI ridge waveguide is single mode. Since the requirements of mode suppression and birefringence suppression may sometimes conflict, there is a need for other methods of polarization compensation with relaxed fabrication tolerances.

Our research in this area parallels that on glass waveguides. The first approach is to adapt the polarization compensator described in Sect. 3 (see Fig. 2), and previously used in the silica and InP echelle grating demul-

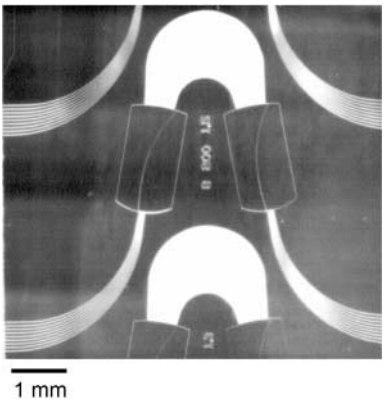


**Fig. 17.** SOI-based microspectrometer/demultiplexer fabricated using 1.5 µm thick Si waveguides, showing compensation regions in the input and output combiners [67]

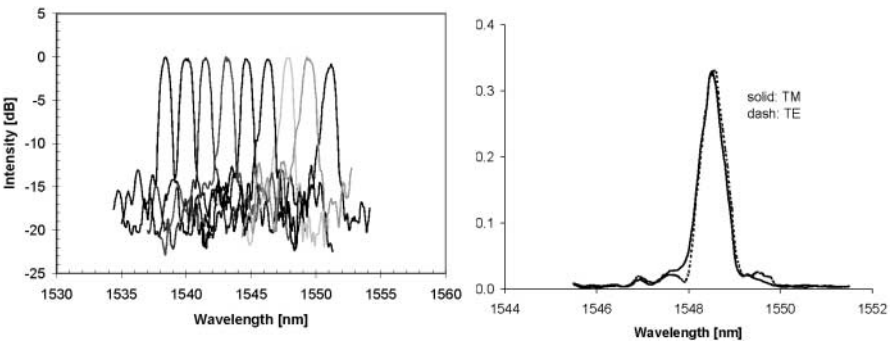


**Fig. 18.** The measured channel spectra for the demultiplexer shown in Fig. 17, and the superposed TE and TM spectra for one channel [67]

tiplexers. The use of compensators in SOI microspectrometers was demonstrated by *Cheben* et al. [67]. The device is shown in Fig. 17. It is an 8-channel 200 GHz spacing demultiplexer with overall device dimensions of approximately $0.5 \times 0.5\,\mathrm{cm}^2$. The AWG was fabricated using 1.5 µm thick SOI. The device pictured in Fig. 17 takes advantage of the fact that in an AWG complementary pairs of compensators can be placed in the input and output slab waveguide combiners. The birefringence change required in each compensator can then be half that for a single compensator, thereby reducing the mode mismatch loss that occurs at the compensator-slab boundary. The birefringence of the compensator sections was modified by a shallow etch. Etching the compensators did not result in any measurable deterioration in cross talk of the device. Before etching the compensator sections, the polarization dependent wavelength shift in this demultiplexer was $\Delta\lambda = 2.22\,\mathrm{nm}$. Depending on the etch depth used to define the compensator sections, $\Delta\lambda$ could be tuned from $\Delta\lambda = 2.22\,\mathrm{nm}$ to $\Delta\lambda = -3.65\,\mathrm{nm}$. The TE and TM channel spectra are shown in Fig. 18 for a compensated device with $\Delta\lambda = 0.04\,\mathrm{nm}$.

Tunability is a particularly useful feature of any compensator. As waveguide dimensions shrink, the uncompensated birefringence increases. At the same time, the wavelength shift $\Delta\lambda$ becomes more sensitive to the exact dimensions of the waveguide ridge profile and the compensator etch depth. Even with effective compensation methods, the challenge becomes to accurately cancel out the birefringence to give $\Delta\lambda < 10\,\text{pm}$, given the tolerances of standard lithography and fabrication tools. Therefore it is an attractive option if one can measure the residual polarization dependence and correct it after device fabrication. As demonstrated in the case of the etched AWG compensator of Fig. 17, final correction for birefringence can be made simply by a calibrated wet etch. A change in etch depth of 1 nm corresponds to a shift in $\Delta\lambda$ of approximately 10 pm for the demultiplexer in Fig. 17. Although effective, it may therefore be difficult to reduce $\Delta\lambda$ to less than 10 pm using compensator etch depth due to the small tolerances.

Again in parallel to similar developments in glass waveguide technology, cladding induced stress is another tool that may be used to control polarization sensitivity in SOI demultiplexers. The use of BPSG as a cladding to balance the thermally induced stress in glass ridge waveguides on silicon has already been described. In SOI there is very little intrinsic stress in the waveguide core, but silicon dioxide is often deposited on top of SOI waveguides as a final protective cladding layer. This oxide will be under varying degrees of stress depending on the deposition technique and processing history. In most cases the $SiO_2$ film will be under compressive stress of the order of a few hundred MPa. In an SOI ridge waveguide, the oxide cladding can therefore create a stress distribution within the ridge, which will in turn create an anisotropic refractive index distribution in the waveguide. Figure 19 shows the calculated distribution of in-plane and out-of-plane stress inside a 2.2 μm high SOI ridge waveguide, with a 1 μm thick compressively stressed oxide layer [68]. The ridge itself is 1.83 μm wide and the etch depth is 1.34 μm. The overlying oxide layer is 1 μm thick. These calculations show that the oxide compresses the Si waveguide in the plane of the wafer, and applies a tensile stress along the surface normal direction.

A simple estimate of the expected stress birefringence can be made using a buried channel waveguide model [69]. We assume an Si channel waveguide embedded in an oxide under compressive stress. In this case the Si will simply be compressed in the in-plane direction and stretched in the surface normal direction. The stress in the Si and corresponding index anisotropy have been evaluated assuming an oxide with an in-plane stress of $\sigma = -380\,\text{MPa}$. Using the photoelastic constants of silicon, (4) predicts changes in the demultiplexer channel wavelength of $\delta\lambda_{\text{TE}} = -0.2\,\text{nm}$ for TE polarized light and $\delta\lambda_{\text{TM}} = +2.2\,\text{nm}$ for TM polarized light. Here we make use of the fact that the stress induced channel wavelength shift is $\delta\lambda = \lambda_0(\Delta n/n)$. The oxide induced birefringence change is comparable and of opposite sign to the geometrical birefringence encountered in SOI slab waveguides, and can be used

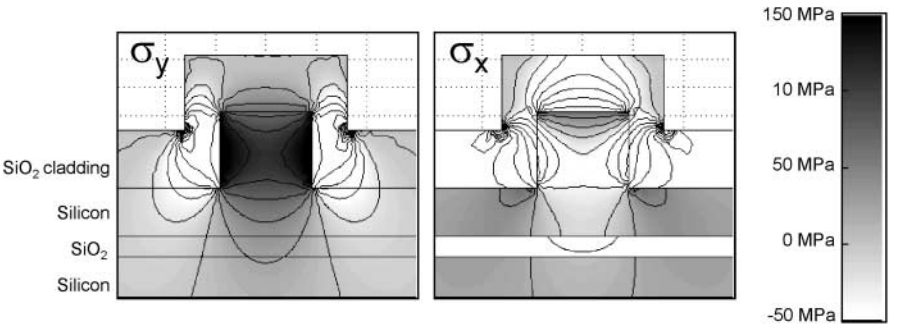


**Fig. 19.** Out-of plane ($\sigma_y$) and in-plane ($\sigma_x$) stress distribution in a 2 µm wide SOI ridge waveguide with a 1 µm thick compressively stressed $SiO_2$ cladding layer (tensile stress is positive, $\sigma_{x,y} > 0$) [68]

as a compensation tool. The effect of stress on real SOI waveguides has been measured using an AWG demultiplexer similar to the 8-channel device pictured in Fig. 17. The effect of oxide induced stress can be measured simply by measuring the change in TE and TM polarized peak channel wavelengths of an AWG as the oxide thickness is varied. The results of these measurements are presented in Fig. 20. For the case of 1 µm oxide upper cladding, the measured stress induced shifts in channel wavelength is $\delta\lambda_{\mathrm{TE}} = -0.4\,\mathrm{nm}$ for TE polarized light and $\delta\lambda_{\mathrm{TM}} = -1.2\,\mathrm{nm}$ for TM polarized light. The corresponding channel wavelength shift will be zero for an oxide thickness near 0.4 µm. These results are only in qualitative agreement with our simplified buried channel model, as would be expected given the complex shape of the realistic stress distribution in a ridge waveguide shown in Fig. 19. However, as in glass channel waveguide devices, these results demonstrate that overcladding induced stress in SOI waveguides can be a very effective tool for birefringence control.

The great advantage of using overcladding stress to compensate birefringence is that it is much easier to make fine adjustments after wafer fabrication, making it possible to correct process variations and hit stringent target polarization specifications at the device level. As the results in Fig. 20 suggest, in the simplest case the stress induced component of the birefringence can be adjusted by adding or removing oxide. The tolerances on the final target thickness of the overclad layer can themselves be increased or decreased by modifying the stress in the deposited oxide cladding. Alternatively the stress applied by the oxide layer may be adjusted using a calibrated thermal anneals. Measurements on PECVD grown oxides demonstrate that the compressive stress and hence the stress induced birefringence can be decreased by almost 50% using short anneals [68]. Corresponding changes in the demultiplexer channel wavelengths have been observed. Although the applications of stress compensation to high index contrast waveguide devices have not been fully explored yet, preliminary measurement and theory suggest that as

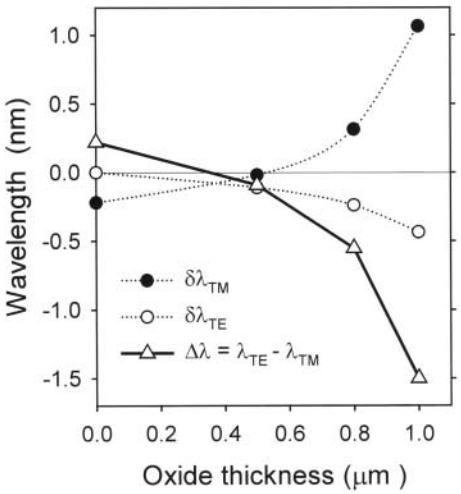


**Fig. 20.** The variations $\delta\lambda_{\mathrm{TE}}$ and $\delta\lambda_{\mathrm{TM}}$ in the measured AWG demultiplexer channel wavelengths with thickness of the stressed oxide overcladding, for TE and TM polarized light, and the corresponding change in birefringence $\Delta\,\lambda$

in the case of glass waveguide demultiplexers, cladding induced stress may likely become the preferred tool for polarization compensation is silicon microphotonic waveguide devices.

## 5 Summary

In this chapter, we have given an overview of some of the important material related design problems and solutions encountered in implementing high performance demultiplexers and spectrometers on silicon substrates. The first section covers the relatively mature subject of silica-on-silicon waveguide demultiplexers. The basic AWG and echelle grating demultiplexer designs are reviewed, and various approaches used to minimize loss and control the polarization birefringence are presented. In the second part of this chapter, we review progress in demultiplexers implemented in high-index contrast systems, in particular the silicon-on-insulator waveguide platform. Methods of achieving modal control, low waveguide loss, and polarization insensitivity are reviewed, illustrating where there are parallels with previous work in silica glass and where the properties of SOI demand unique solutions. The emphasis is on technical solutions that may enable the scaling down of high performance demultiplexers, spectrometers and other dispersive elements into the microphotonic regime. Such microphotonic spectrometers have applications in compact spectral sensors, optical network monitoring, wavelength channel multiplexing and demultiplexing, and will enable WDM as a low cost solution to parallel data transport inside the computer, between racks, and in smaller local area networks.

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