

You must show all your work! Answers without supporting work will not be given credit.

All problems are inspired by our *Introduction to Logic Design 3rd Edition* text.

Only neatly hand-written or typed work will be accepted.

Homework must be in PDF format and should be scanned using, at minimum, a phone camera scanning app.

This homework is worth 5 points.

Name: Damian Sclafani

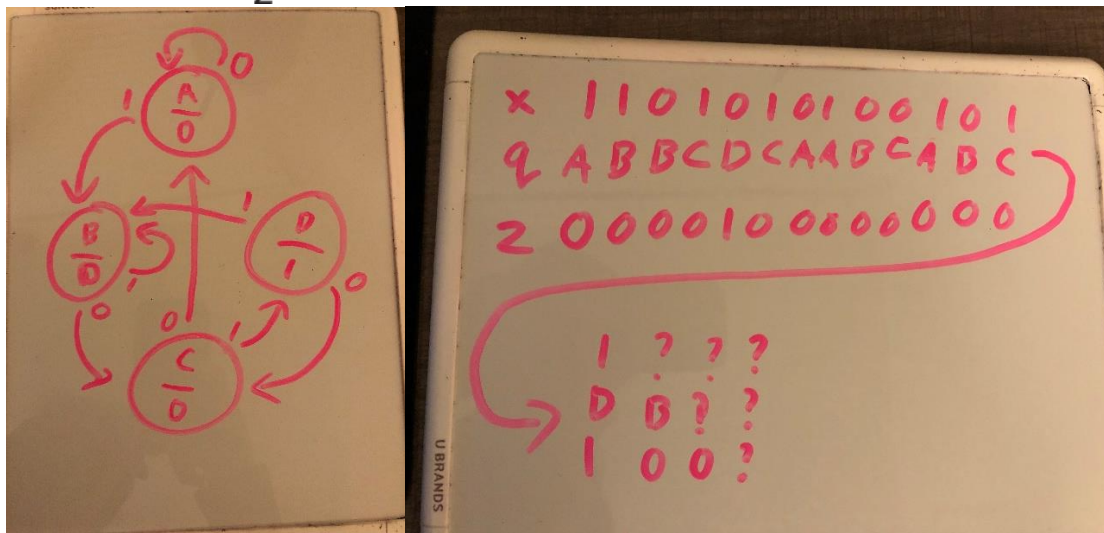
1. Draw both the state diagram and complete the timing sequence as x changes until you have no distinct state information remaining.

q	q^*		z
	$x = 0$	$x = 1$	
A	A	B	0
B	C	B	0
C	A	D	0
D	C	B	1

x 1 1 0 1 0 1 0 1 0 0 1 0 1 1

q A

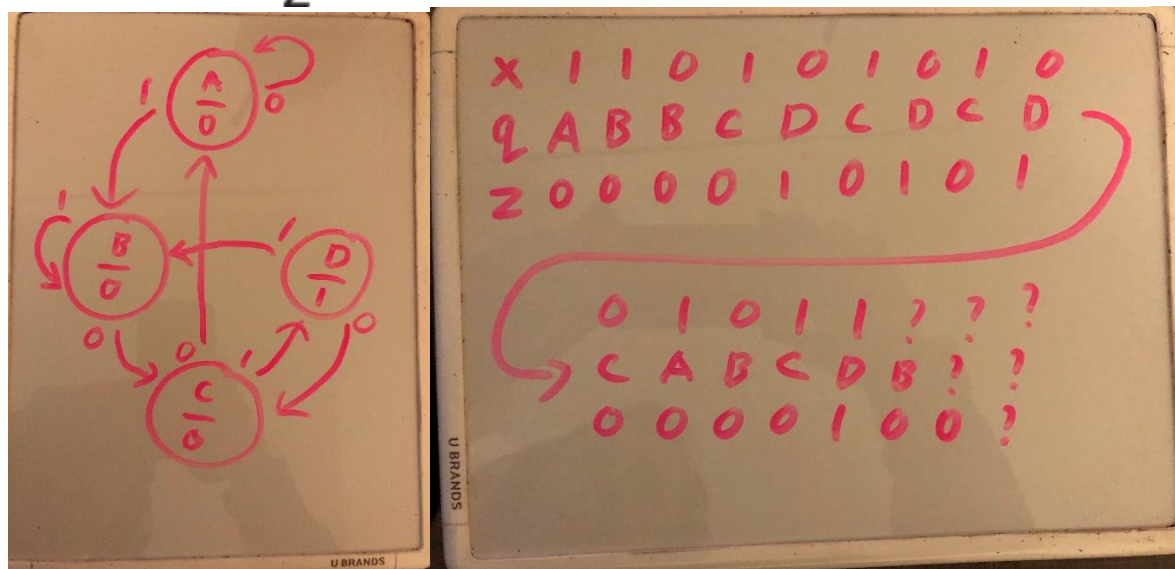
z



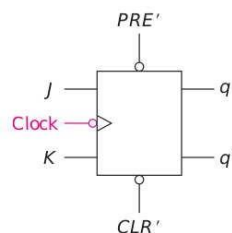
2. Draw both the state diagram and complete the timing sequence as x changes until you have no distinct state information remaining.

q	q^*		z
	$x = 0$	$x = 1$	
A	A	B	0
B	C	B	0
C	A	D	0
D	C	B	1

x 1 1 0 1 0 1 0 1 0 0 1 0 1 1
 q A
 z



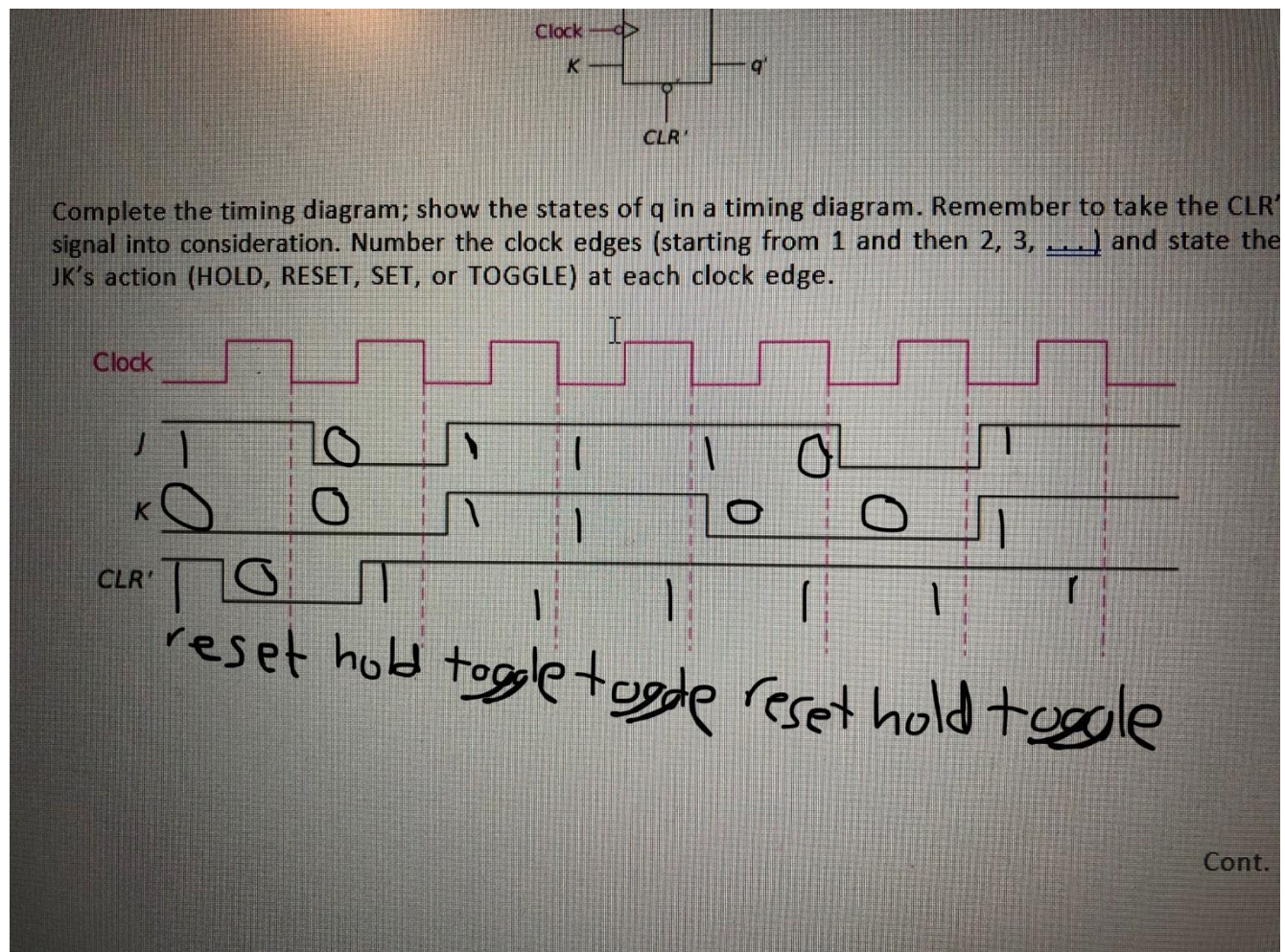
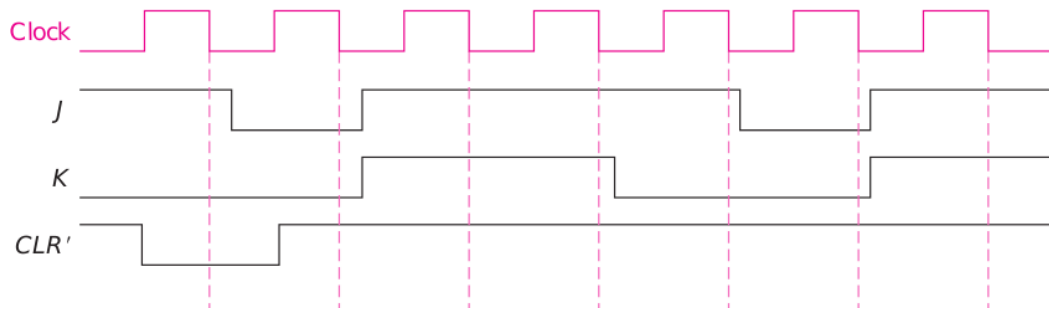
3. Given the following JK flip-flop,



Complete the timing diagram; show the states of q in a timing diagram. Remember to take the CLR' signal into consideration. Number the clock edges (starting from 1 and then 2, 3, ...) and state the

Cont.

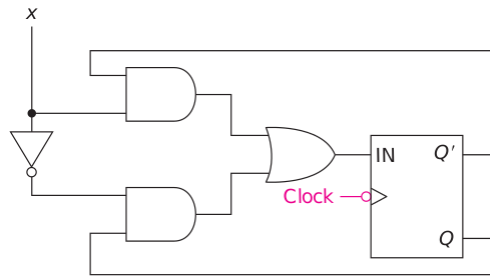
JK's action (HOLD, RESET, SET, or TOGGLE) at each clock edge.



Cont.

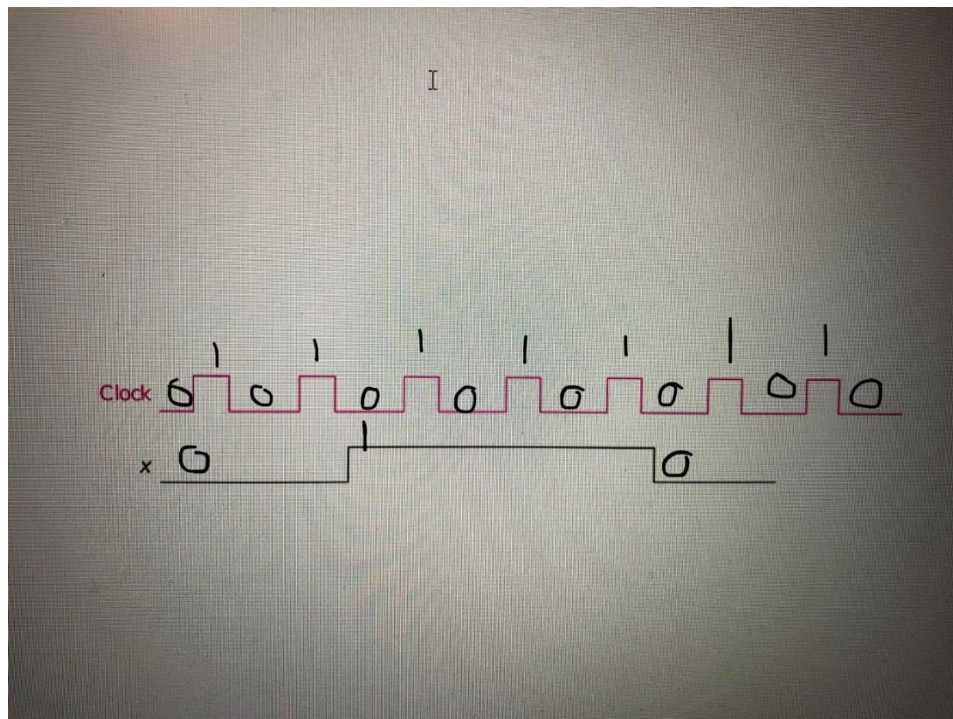
Cont.

4. Given the following sequential circuit,



Treat IN as the D-input to D flip-flop. Show the necessary state table (for states 0 and 1) and complete the following timing trace as long as the clock allows. Assume Q begins storing 0.

D	q	q*
0	0	0
0	1	0
1	0	1
1	1	1



Cont.

