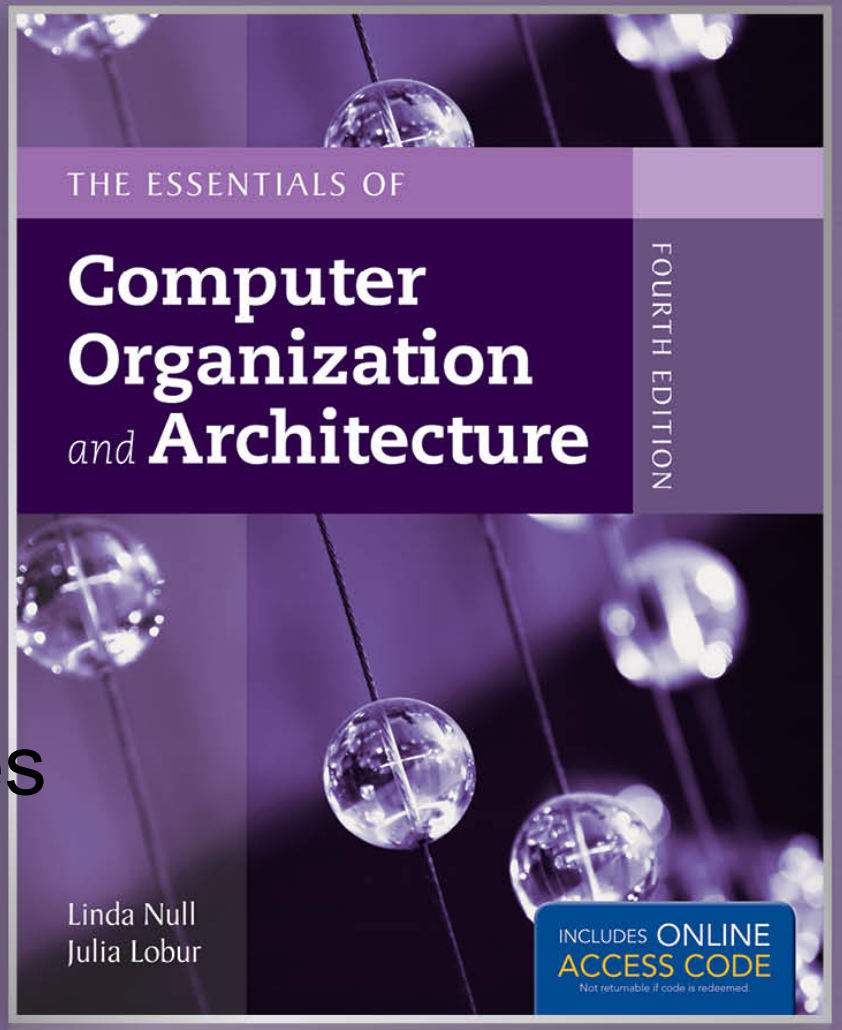
Chapter 3

Boolean Algebra and Digital Logic - Exercises



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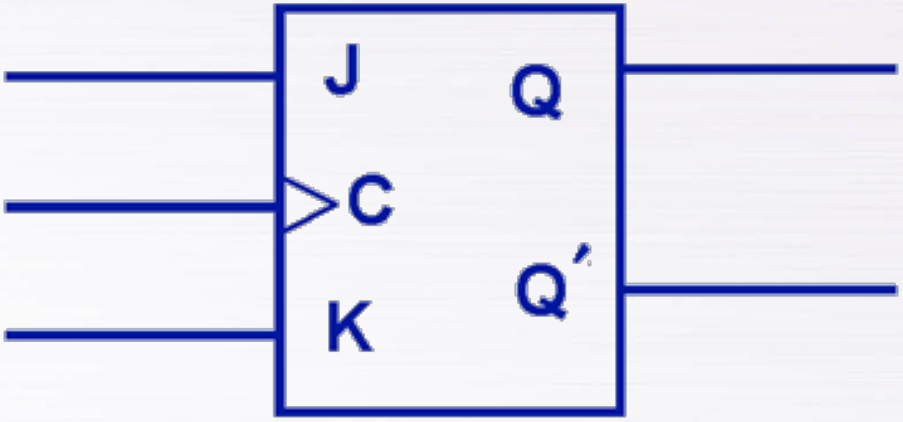
3.6 Sequential Circuits

- **JK flip-flop**.
- The **characteristic table** indicates that the flip-flop is stable for all inputs.



J	K	Q(t+1)
0	0	Q(t) (no change)
0	1	0 (reset to 0)
1	0	1 (set to 1)
1	1	$\bar{Q}(t)$

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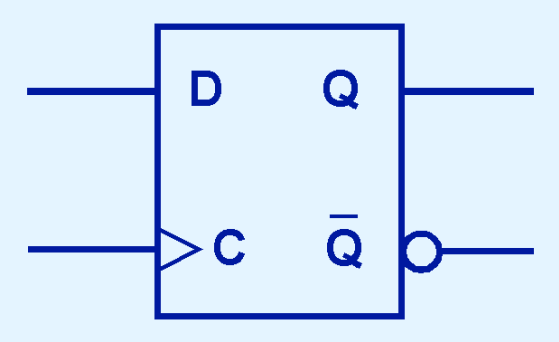
3.6 Sequential Circuits

- **D flip-flop**
- The **input D at time t** becomes the **output Q at time t+1**
- D flip-flops are also known as **memory cells**



D	Q(t+1)
0	0
1	1

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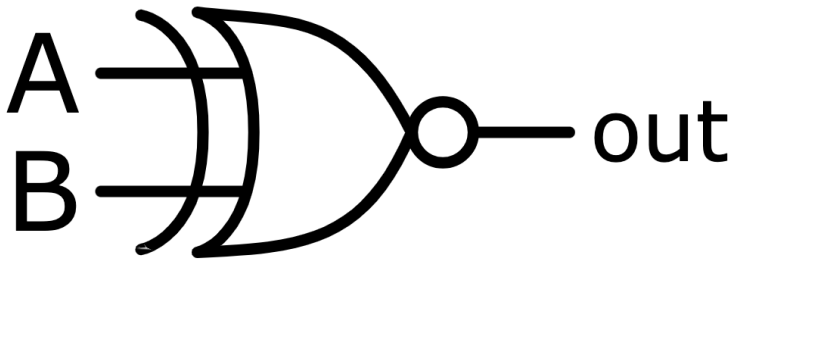
3.6 Sequential Circuits

- **XNOR Gate**



Input		Output
A	B	A XNOR B
0	0	1
0	1	0
1	0	0
1	1	1

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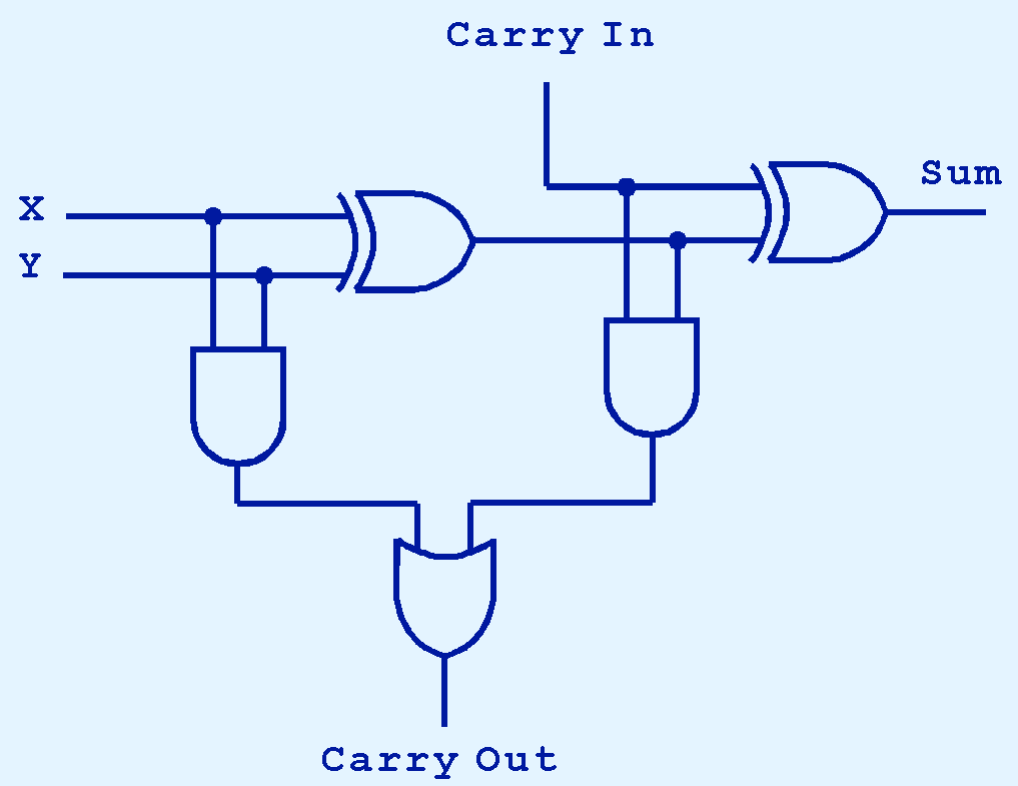
3.6 Sequential Circuits

- **Full Adder**



Inputs			Outputs	
X	Y	Carry In	Sum	Carry Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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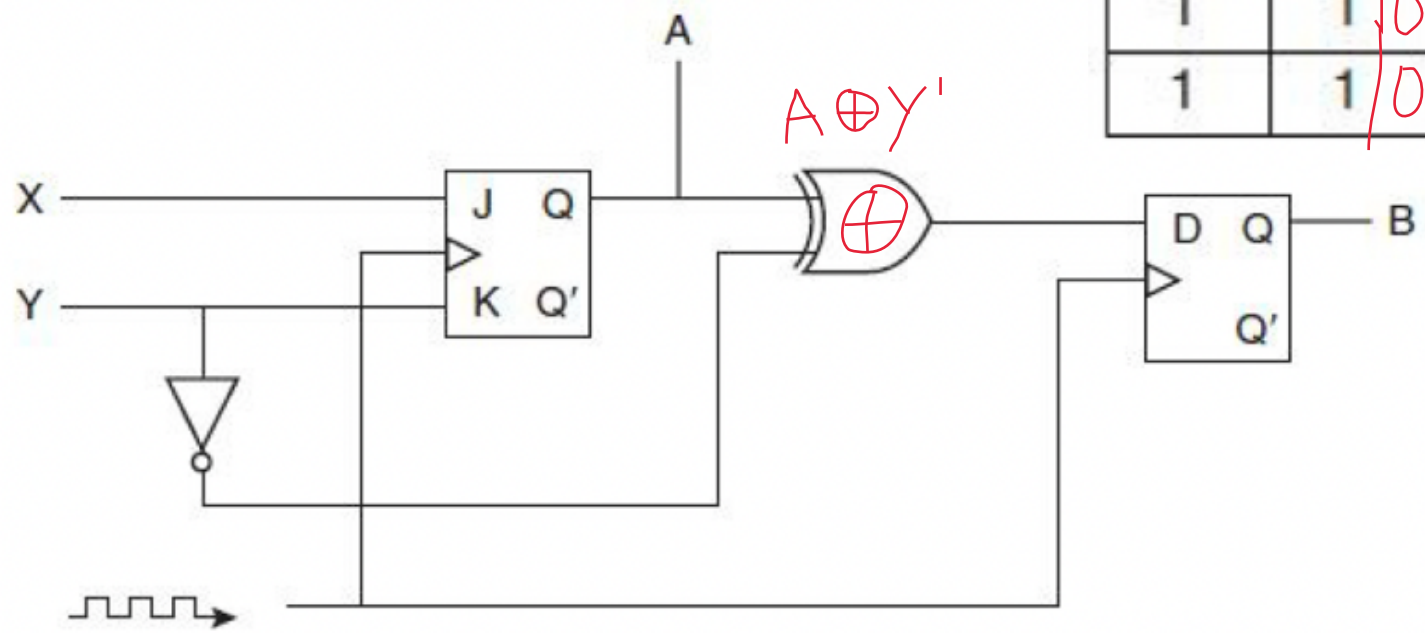
Exercise 1

X	Y	Y'	A	Next State A	Next State B
0	0	1	0	0	1
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	1	0	1
1	0	1	0	1	1
1	0	1	1	1	0
1	1	0	0	1	0
1	1	0	1	0	1



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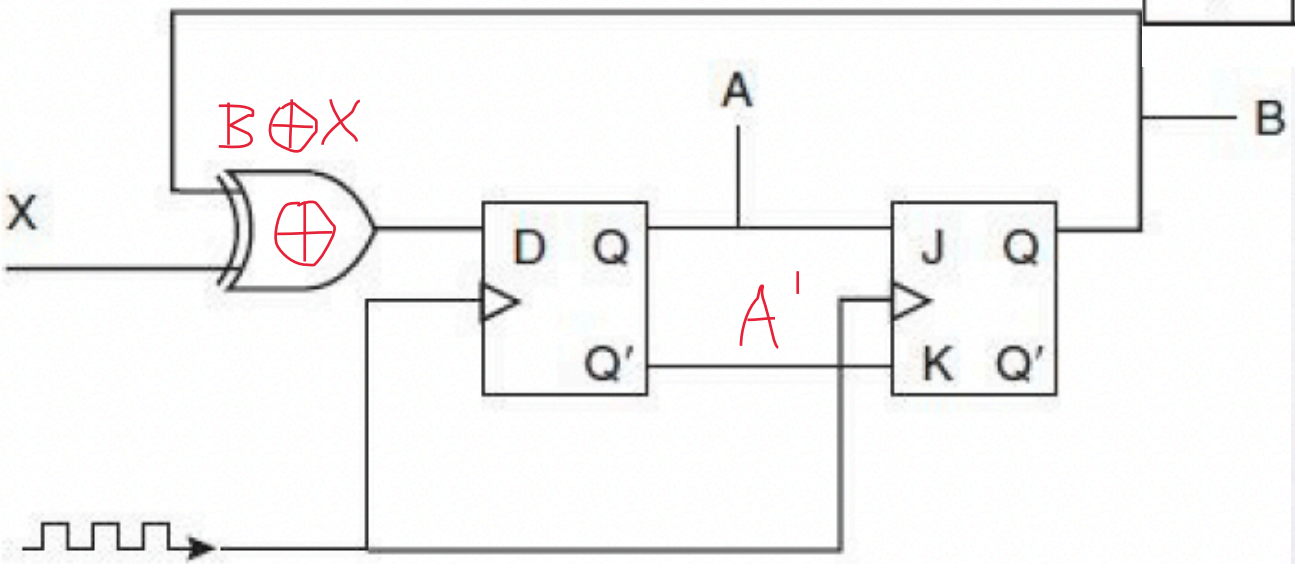
Exercise 2

A	B	X	Next State A	Next State B
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	1



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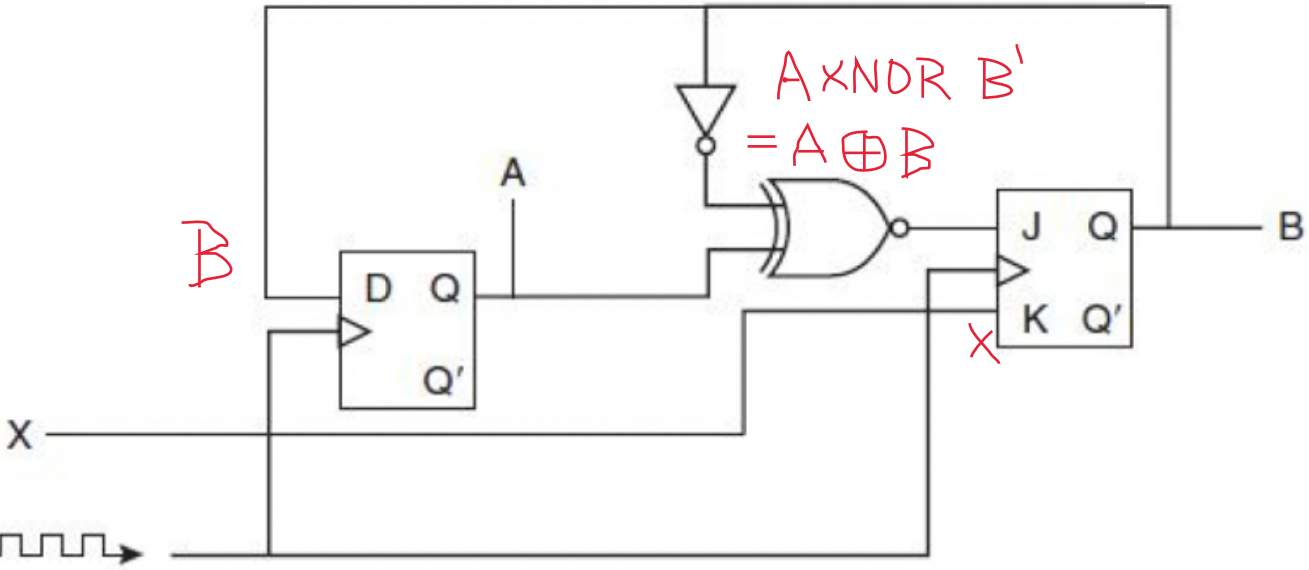
Exercise 3

A	B	A ⊕ B	X	Next State A	Next State B
0	0	0	0	0	0
0	0	0	1	0	0
0	1	1	0	1	1
0	1	1	1	1	0
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	1	1
1	1	0	1	1	0



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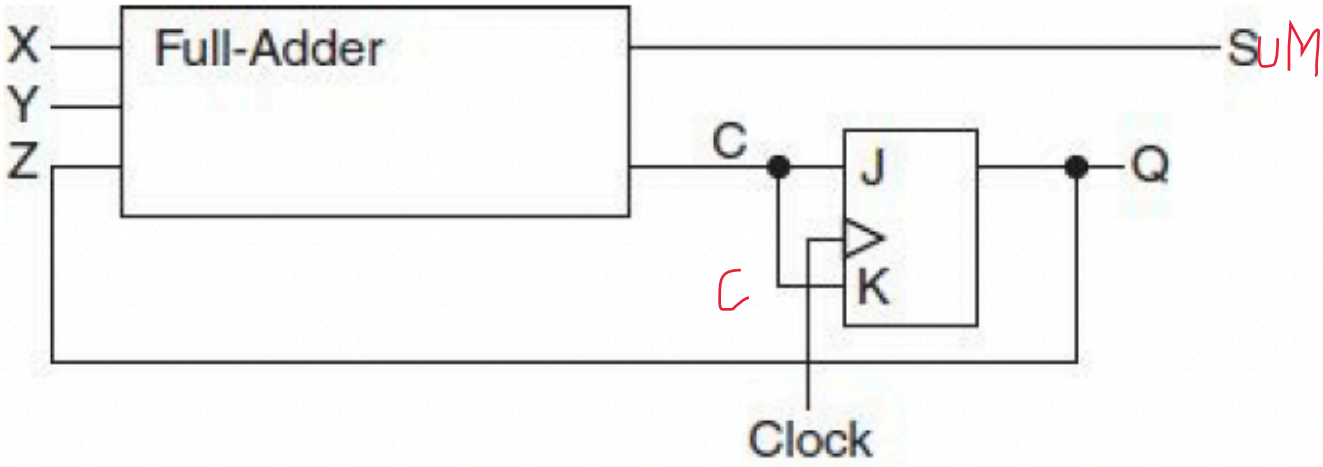
Exercise 4



Present State Q(t)	Inputs X	Y	C	Next State Q(t+1)	Output S
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	0
1	1	1	1	0	1