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Faculty of Engineering, Built Environment and Information Technology

Fakulteit Ingenieurswese, Bou-omgewing en Inligtingtegnologie / Lefapha la Boetšenere, Tikologo ya Kago le Theknolotši ya Tshedimošo

Department of Computer Science

COS 122 Operating Systems

Assignment 1

Due: 18 August 2022 @ 23:00

PLAGIARISM POLICY

UNIVERSITY OF PRETORIA

The Department of Computer Science considers plagiarism as a serious offence. Disciplinary action will be taken against students who commit plagiarism. Plagiarism includes copying someone else's work without consent, copying a friend's work (even with consent) and copying material (such as text or program code) from the Internet. Copying will not be tolerated in this course. For a formal definition of plagiarism, the student is referred to `http://www.ais.up.ac.za/plagiarism/index.htm` (from the main page of the University of Pretoria site, follow the *Library* quick link, and then click the *Plagiarism* link). If you have any form of question regarding this, please ask one of the lecturers, to avoid any misunderstanding. Also note that the OOP principle of code re-use does not mean that you should copy and adapt code to suit your solution.

Objectives

This assignment evaluates the understanding and application of various key concepts and functions found in computer and operating systems. It covers chapters 1 and 2 of the prescribed textbook. This assignment has 5 tasks for a total of 20 marks.

Upload Instructions

You need to provide written answers to the tasks in this assignment. You are then required to submit a document containing these answers in order for them to be marked. Show all the intermediate and calculation steps in your answers (excluding the multiple choice task). Some marks will be awarded for intermediate steps.

- Upload your document to the Assignment 1 assignment slot on COS 122 ClickUP before 23:00 on 18-Aug-2022. **No late submissions will be accepted!**
- All documents must be in either text, Word or PDF format (typed not handwritten) as no other formats will be marked.
- **Failure to upload your answers will result in 0 marks being awarded for your assignment!**

Task 1 ..... (3 marks)

1.1 The technique where a system clock generates interrupts, and at each clock interrupt the OS regains control and assigns the processor to another user, is called: (1)

A. time slicing
B. multithreading
C. round robin
D. clock cycling

1.2 Which of the following is NOT a technique for I/O: (1)

A. Programmed I/O
B. Interrupt-driven I/O
C. DMA
D. Serial I/O

1.3 Which of the given options is the highest on the memory hierarchy: (1)

A. USB Flash Drive
B. Solid State Drive
C. Main Memory
D. Cache Memory

Task 2 ..... (3 marks)

Suppose a processor has access to three levels of memory. Level 1 has an access time of 7 microseconds, level 2 has an access time of 21 microseconds and level 3 has an access time of 63 microseconds. Level 1 contains a subset of the bytes contained in level 2, and level 2 contains a subset of the bytes contained in level 3. It is estimated that 33 % of all requested bytes are contained in level 1, 66 % of all requested bytes are contained in level 2 and 100 % of all requested bytes are contained in level 3. If a byte to be accessed is in level 1, then the processor will directly access it from level 1. If a byte to be accessed is not in level 1 but in level 2, then the processor will directly access it from level 2. If a byte to be accessed is not in level 1 and not in level 2, then the processor will directly access it from level 3. For simplicity, assume that the accessed bytes are not transferred between the memory levels. Moreover, ignore the time that is required for the processor to determine whether a byte can be found in level 1, 2 or 3.

2.1 What is the average access time of this system? Write down all intermediate steps and explain the result briefly. (3)

Task 3 ..... (7 marks)

In a batch operating system, four jobs JOB1, JOB2, JOB3, JOB4 are submitted for execution. Each job involves an I/O activity, followed by a CPU time, followed by another I/O activity of the same time span as the first. Each job is associated with a different I/O device. JOB1 requires a total of 13 ms, with 3 ms CPU time. JOB2 requires 10 ms total time with 2 ms CPU time. JOB3 requires 56 ms total time with 8 ms CPU time. JOB4 requires 19 ms total time with 5 ms CPU time.

Assume a uni-programming system and answer the following:

3.1 What will be the total time to complete all jobs? (½)

3.2 What will be the total CPU time? (½)

3.3 What will be the CPU utilisation? (1)

Assume a multiprogramming system and answer the following:

3.4 What will be the total time to complete all jobs? (1)

3.5 What will be the CPU utilisation? (1)

3.6 What will be the turnaround time of JOB4? (1)

3.7 What will be the average turnaround time? (1)

Now answer the following:

3.8 Which system has better CPU utilisation? Explain why. (1)

Task 4 ..... (3 marks)

Consider figure 1.3 in the textbook and the hypothetical machine it represents. Given that before any action takes place, AC is 0000, PC is 100, IR is empty and the memory locations 100, 101, 205, 206 and 207 contain the values 1205, 2207, 000A, 000F and 0005 respectively. Answer the following:

4.1 What value will be contained in AC, IR and PC after the first instruction cycle?. (1)

4.2 What values will be contained in AC, IR and PC after the second instruction cycle? (1)

4.3 What values will be contained in memory locations 205, 206 and 207 after the second instruction cycle? (1)

Task 5 ..... (4 marks)

Consider a hypothetical 128-bit microprocessor having 128-bit instructions composed of two fields. The first 4 bytes contains the opcode, and the remainder an intermediate operand or an operand address.

5.1 What is the maximum directly addressable memory capacity? (1)

5.2 Assume that the data buses in the system have a size of 16 bits. How many fetch cycles will be required in order to transfer two instructions? (½)

5.3 If the size of the data buses are increased to 64 bits, how many fetch cycles will now be required in order to transfer two instructions? (½)

5.4 Which data bus size would be the most ideal? Explain why. (2)