2023 Digital IC Design

Homework 2: Rails

1. Introduction

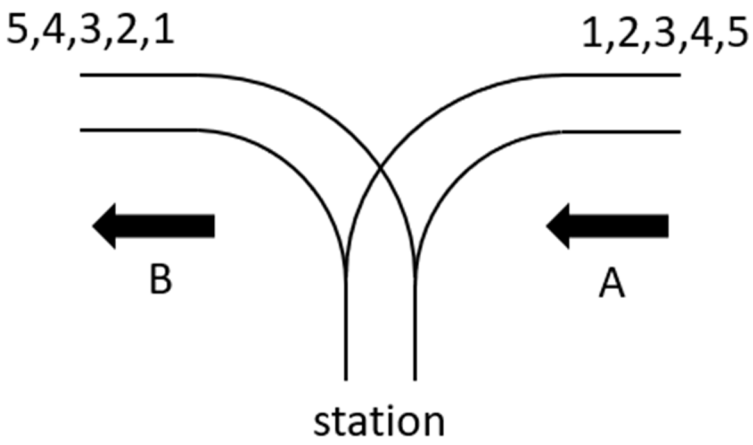

Fig. 1. Rails.

There is a railway station that established only a surface track. Furthermore, the station is designed as a dead-end station, as shown in Fig. 1. In this homework, you are required to design a circuit that determines whether it is possible to meet the given departure order. The specification and function of the circuit is detailed in the following sections.

2. Design Specifications

2.1 Block Overview

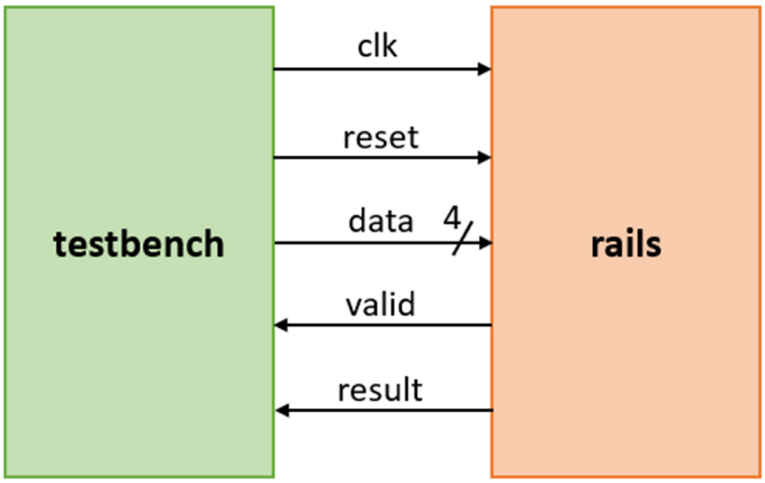

Fig. 2. The block overview.

2.2 I/O Interface

Table I. I/O interface.

Signal Name	I/O	width	Description
clk	I	1	This circuit is a synchronous design triggered at the positive edge of *clk*.
reset	I	1	Active-high asynchronous reset signal.
data	I	4	The number of coming trains followed by the required departure order.
valid	O	1	When output the determination result, set *valid* signal to high. The testbench will check the output *result* signal when *valid* signal is high.
result	O	1	If the given departure order is possible to meet, *result* should be set as high. Otherwise, it has to be set as low.

2.3 File Description

File Name	Description
rails.v	The top module of this design.
tb.v	The testbench file. The content in this file is **not allowed** to be modified.
test_data_rails.dat	Test data for rails verification.
golden_data_rails.dat	Golden data for rails verification.

3. Function Description

3.1 Description

Every train arrives at the station from direction A, and departs the station from direction B. The arriving trains will be numbered in ascending order from 1 to N, and the number of coming trains ranges from 3 to 10. Given a departure order *d1*, *d2*, . . . , *dN*, the circuit has to determine if the trains can leave the station in the required order. In the station, the order of trains can't be changed. For any train, there is no limit to its arrival time and staying time at the station. However, once a train has entered the station, it cannot return to the track in direction A. After a train has left the station in direction B, it cannot return to the station, either.

Hint: The station can be considered as a 'stack'.

3.2 Timing Specifications

After the system resets, the ***data*** signal will first input the number of coming trains for the first test pattern (T1), followed by the required departure order in sequence at each cycle (T2~T6). Once the testbench has finished inputting the input pattern, it will wait for the rails circuit to output a result. If the departure order is possible to meet, ***result*** should output high. Otherwise, it should output low. When the result is ready to be output, the ***valid*** signal must be set as high. The testbench will validate the ***result*** when it detects a high-level ***valid*** signal (T7). At the next cycle, ***valid*** should be set back to low to avoid the testbench misjudgment (T8). After ***valid*** is pulled down, the testbench will start inputting the next test pattern from the next cycle (T9).

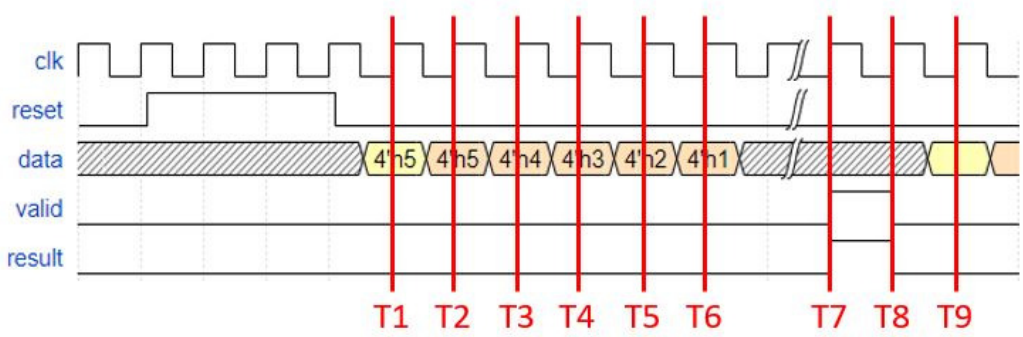

Fig. 3. Timing diagram of input and output.

4. Scoring

4.1 Functional Simulation [100%]

The grading rule for this homework is that one point can be obtained by passing one test pattern. After the simulation finished, you can get the score message in ModelSim. Please don't design specifically for the test pattern. Otherwise, you will get 0 point.

```
# ------------------------------------------------------------
# ----    Simulation finish,  ALL PASS,  Score = 100     ----
# ------------------------------------------------------------
```

Fig. 4. Simulation result for all passes.

```
# ------------------------------------------------------------
# -- Simulation finish,  Pass = 53 , Fail = 47, Score = 53 --
# ------------------------------------------------------------
```

Fig. 5. Simulation result for partial passes.

5. Submission

5.1 Submitted files

You should classify your files into two directories and compress them to .zip format. The naming rule is HW2_studentID_name.zip. If your file is not named according to the naming rule, you will lose five points.

	RTL category
*.v	All of your Verilog RTL code
	Documentary category
*.pdf	The report file of your design (in pdf).

5.2 Report file

Please follow the spec of report. You are asked to describe how the circuit is designed as detailed as possible.

5.3 Note

Please submit your .zip file to folder HW2 in moodle.

Deadline: 2023/4/10 23:55

If you have any problem, please contact TA by email

p76114040@gs.ncku.edu.tw

6. Examples

Case 1:

Number of coming trains: 5

Departure order: 4, 3, 2, 5, 1

Result: 1

Case 2:

Number of coming trains: 6

Departure order: 2, 4, 1, 3, 6, 5

Result: 0

Case 3:

Number of coming trains: 3

Departure order: 1, 2, 3

Result: 1

Case 4:

Number of coming trains: 4

Departure order: 2, 4, 3, 1

Result: 1

Case 5:

Number of coming trains: 5

Departure order: 4, 2, 3, 5, 1

Result: 0