ECE 506 - Project 2

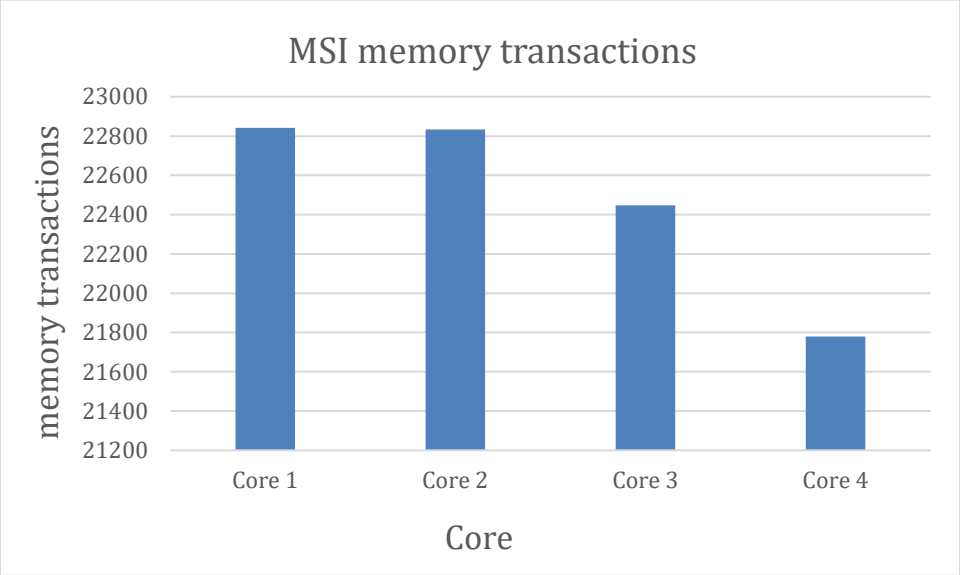
Name: Tzu-Ching Yeh **Student ID: 200542364**

Part 1. Modified MSI

a) (40 pt) Implement Modified MSI protocol as seen in the diagram

Implementation hint: add an instance of cache per processor, add coherence state support to a cache line, and ensure that Access() in the requestor emits coherence signals and that other snooping caches process those signals.

b) (10 pt) Plot the number of memory transactions for the long trace.



Graph 1. Number of memory transactions

Part 2. Dragon Protocol

a) (40 pt) Implement Dragon protocol as seen in the diagram

b) (10 pt) Compare Modified MSI optimization and Dragon protocols. Explain the results briefly

Modified MSI		Dragon protocol	
Core	1	Core	1
number of reads:	112661	number of reads:	112661
number of read misses:	21453	number of read misses:	9641
number of writes:	11942	number of writes:	11942
number of write misses:	689	number of write misses:	5
total miss rate:	17.77%	total miss rate:	7.72%
number of writebacks:	700	number of writebacks:	1006
memory transactions:	22842	memory transactions:	10625
number of invalidations:	20585	number of interventions:	1994
number of flushes:	93	number of flushes:	15
number of BusRdX:	689	Bus Transactions(BusUpd):	1290

Modified MSI		Dragon protocol	
Core	2	Core	2
number of reads:	110830	number of reads:	110830
number of read misses:	21491	number of read misses:	9472
number of writes:	11710	number of writes:	11710
number of write misses:	663	number of write misses:	6
total miss rate:	18.08%	total miss rate:	7.73%
number of writebacks:	679	number of writebacks:	979
memory transactions:	22833	memory transactions:	10457
number of invalidations:	20666	number of interventions:	1978
number of flushes:	77	number of flushes:	19
number of BusRdX:	663	Bus Transactions(BusUpd):	1309

Modified MSI		Dragon protocol	
Core	3	Core	3
number of reads:	114938	number of reads:	114938
number of read misses:	21043	number of read misses:	9456
number of writes:	12383	number of writes:	12383
number of write misses:	690	number of write misses:	6
total miss rate:	17.07%	total miss rate:	7.43%
number of writebacks:	714	number of writebacks:	984
memory transactions:	22447	memory transactions:	10446
number of invalidations:	19988	number of interventions:	1937
number of flushes:	97	number of flushes:	17
number of BusRdX:	690	Bus Transactions(BusUpd):	1404

Modified MSI		Dragon protocol	
Core	4	Core	4
number of reads:	113428	number of reads:	113428
number of read misses:	20337	number of read misses:	9568
number of writes:	12108	number of writes:	12108
number of write misses:	684	number of write misses:	4
total miss rate:	16.74	total miss rate:	7.62%
number of writebacks:	759	number of writebacks:	986
memory transactions:	21700	memory transactions:	10558
number of invalidations:	18552	number of interventions:	1977
number of flushes:	76	number of flushes:	10
number of BusRdX:	684	Bus Transactions(BusUpd):	1304

Explanation: the drawback of an invalidate-based protocol is that it incurs in a high number of coherence miss. Each read to a block that has been invalidated incurs a cache miss. Dragon protocol, update-based protocol, relies on directly updating cached values to achieve write propagation. Therefore, MSI protocol's total miss rate is higher than Dragon protocol, and have more memory transactions.