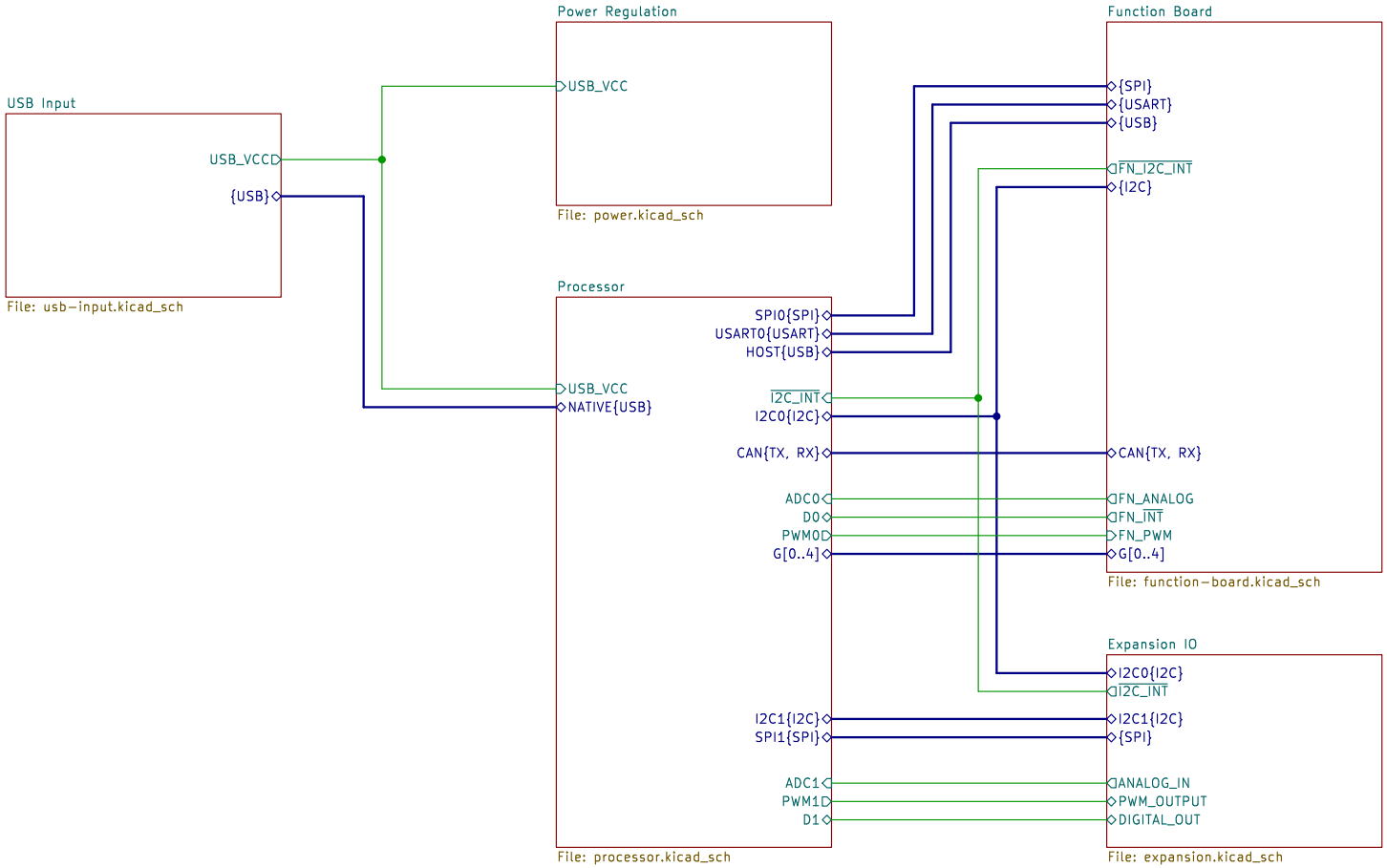


NOTES

General findings after diving into MicroMod ecosystem for this design!

ESP32, STM32, SAMD51, RP2040 don't connect (or oversubscribe) TX2.
ESP32, SAMD51, STM32 boards don't connect SPI1.
Only STM32, SAMD51 have CAN pinout connected.
RP2040 lacks second (I2C1) bus connections.
RP2040 shares G5-8 with SPI0 lines.

As a result, a lot of IO supports disconnection
to more easily allow remapping of IO after fab...

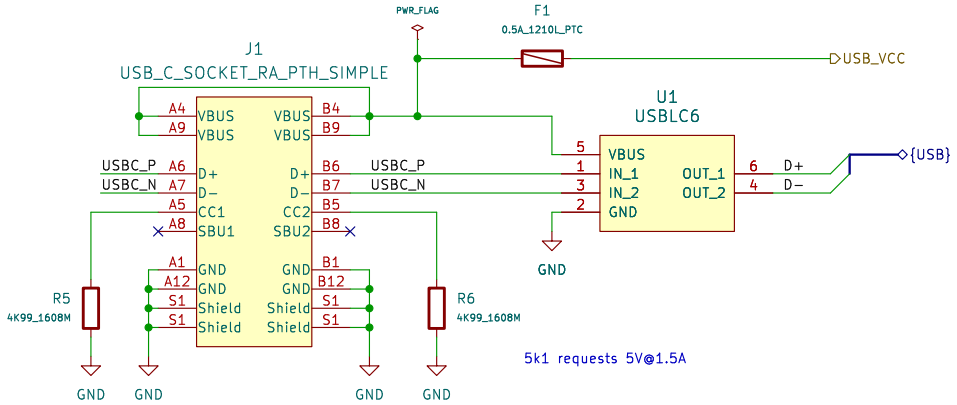
I haven't found any boards which correctly implement:
- RTC battery connection
- SWO pin on designated G11

Sheet: /
File: backplane.kicad_sch

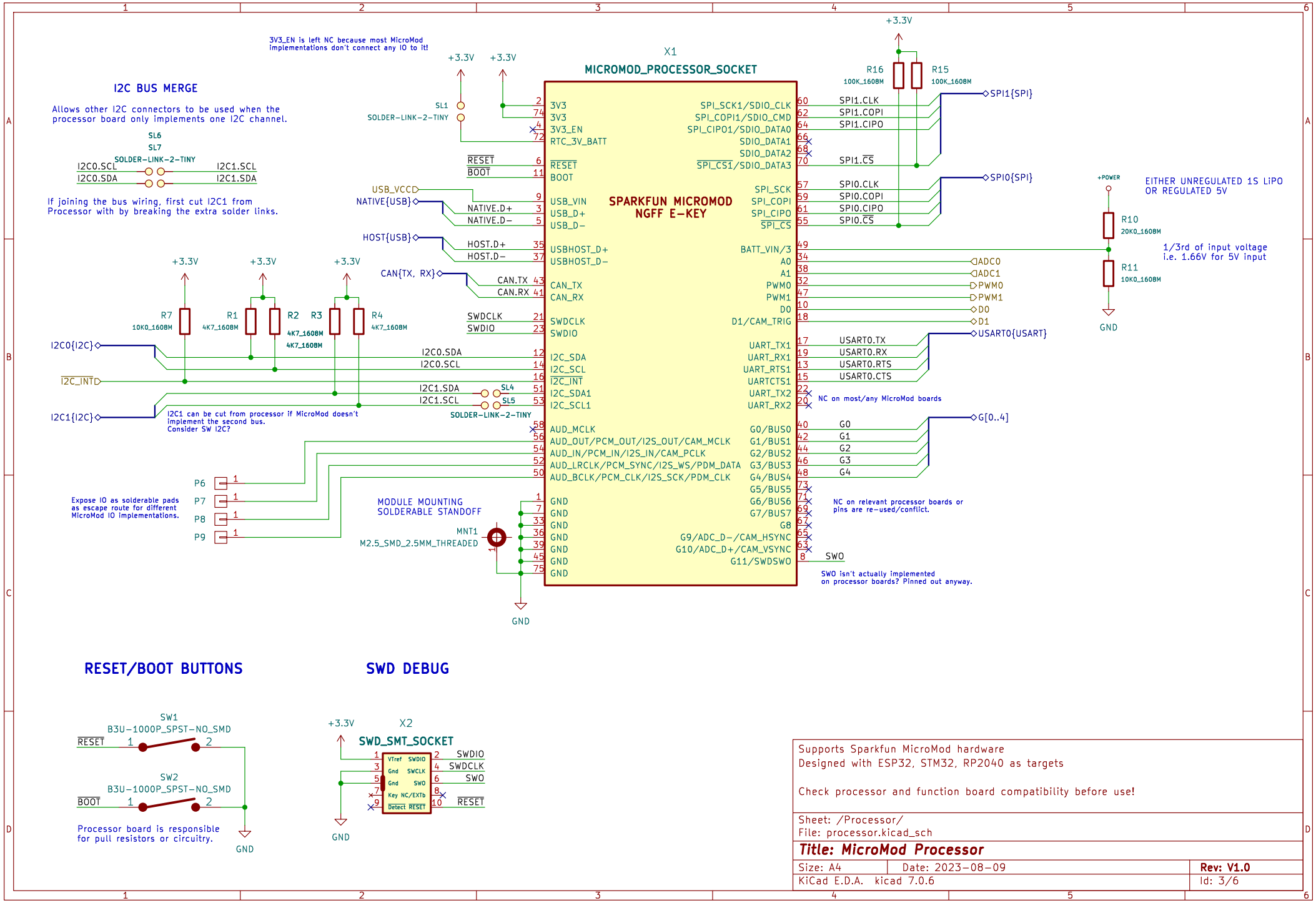
Title: SPE-NODE-BACKPLANE

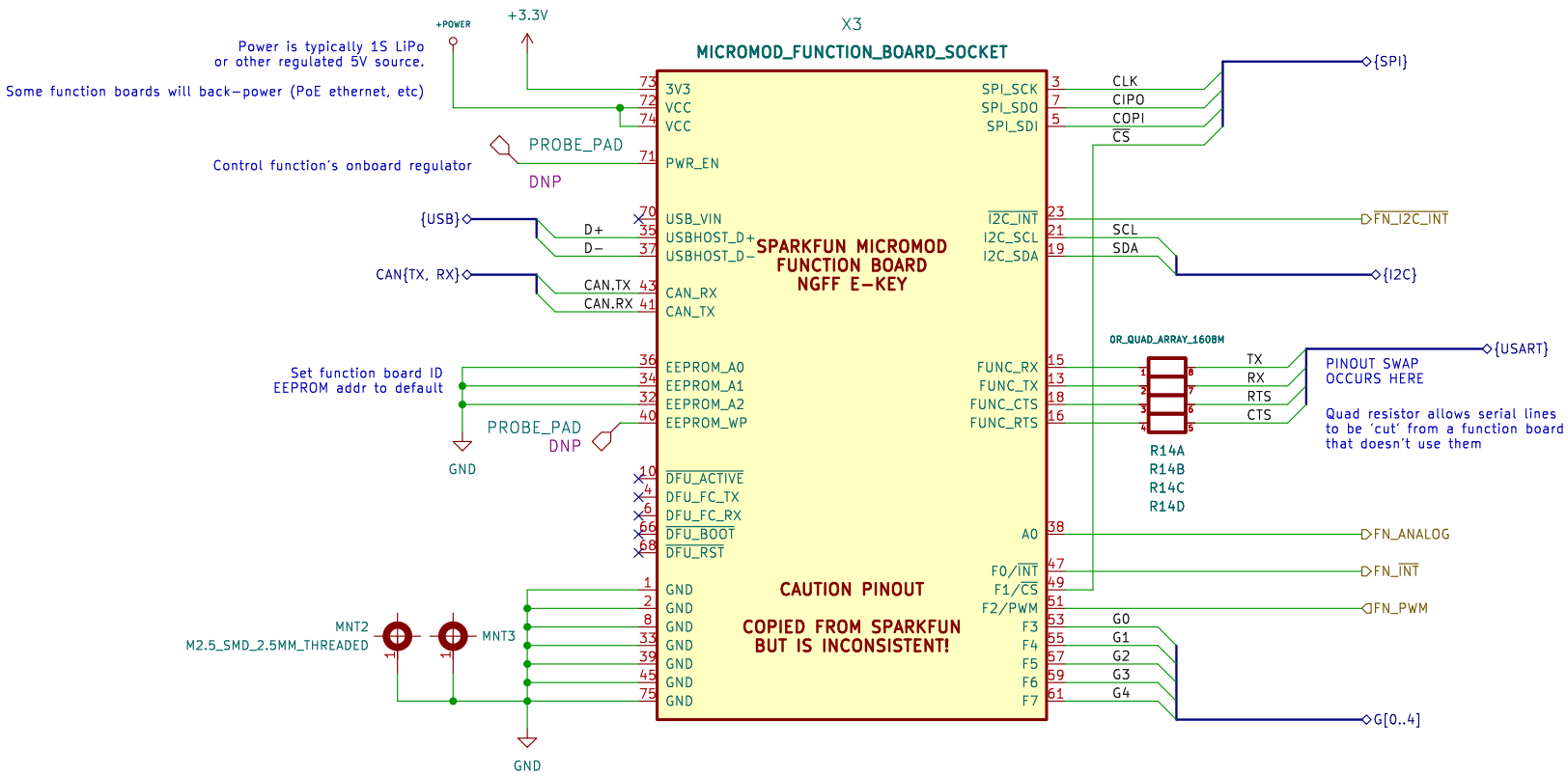
Size: A4	Date: 2023-08-09	**Rev: V1.0**
KiCad E.D.A. kicad 7.0.6		Id: 1/6

USBC CONNECTOR



Sheet: /USB Input/		
File: usb-input.kicad_sch		
Title: USB CONNECTION		
Size: A4	Date: 2023-08-09	**Rev: V1.0**
KiCad E.D.A. kicad 7.0.6		Id: 2/6


3V3_EN is left NC because most MicroMod implementations don't connect any IO to it!
X1
MICROMOD_PROCESSOR_SOCKET
SPARKFUN MICROMOD NGFF E-KEY
3V3
3V3
3V3_EN
RTC_3V_BATT
RESET
BOOT
USB_VIN
USB_D+
USB_D-
USBHOST_D+
USBHOST_D-
CAN_TX
CAN_RX
SWDCLK
SWDIO
I2C_SDA
I2C_SCL
I2C_INT
I2C_SDA1
I2C_SCL1
AUD_MCLK
AUD_OUT/PCM_OUT/I2S_OUT/CAM_MCLK
AUD_IN/PCM_IN/I2S_IN/CAM_PCLK
AUD_LRCLK/PCM_SYNC/I2S_WS/PDM_DATA
AUD_BCLK/PCM_CLK/I2S_SCK/PDM_CLK
GND
SPI_SCK1/SDIO_CLK
SPI_COPI1/SDIO_CMD
SPI_CIPO1/SDIO_DATA0
SDIO_DATA1
SDIO_DATA2
SPI_CS1/SDIO_DATA3
SPI_SCK
SPI_COPI
SPI_CIPO
SPI_CS
BATT_VIN/3
A0
A1
PWM0
PWM1
D0
D1/CAM_TRIG
UART_TX1
UART_RX1
UART_RTS1
UARTCTS1
UART_TX2
UART_RX2
G0/BUS0
G1/BUS1
G2/BUS2
G3/BUS3
G4/BUS4
G5/BUS5
G6/BUS6
G7/BUS7
G8
G9/ADC_D-/CAM_HSYNC
G10/ADC_D+/CAM_VSYNC
G11/SWDSWO
SWO
I2C BUS MERGE
Allows other I2C connectors to be used when the processor board only implements one I2C channel.
SL6
SL7
SOLDER-LINK-2-TINY
I2C0.SCL
I2C0.SDA
I2C1.SCL
I2C1.SDA
If joining the bus wiring, first cut I2C1 from Processor with by breaking the extra solder links.
SL1
SOLDER-LINK-2-TINY
USB_VCCD
NATIVE{USB}
NATIVE.D+
NATIVE.D-
HOST{USB}
HOST.D+
HOST.D-
CAN{TX, RX}
CAN.TX
CAN.RX
SWDCLK
SWDIO
I2C0{I2C}
I2C_INT
I2C1{I2C}
I2C0.SDA
I2C0.SCL
I2C1.SDA
I2C1.SCL
SL4
SL5
SOLDER-LINK-2-TINY
I2C1 can be cut from processor if MicroMod doesn't implement the second bus. Consider SW I2C?
R7
10KΩ_1608M
R1
4K7_1608M
R2
4K7_1608M
R3
4K7_1608M
R4
4K7_1608M
+3.3V
P6
P7
P8
P9
Expose IO as solderable pads as escape route for different MicroMod IO implementations.
MODULE MOUNTING SOLDERABLE STANDOFF
MNT1
M2.5_SMD_2.5MM_THREADED
GND
R16
100K_1608M
R15
100K_1608M
SPI1{SPI}
SPI1.CLK
SPI1.COPI
SPI1.CIPO
SPI1.CS
SPI0{SPI}
SPI0.CLK
SPI0.COPI
SPI0.CIPO
SPI0.CS
+POWER
EITHER UNREGULATED 1S LiPO OR REGULATED 5V
R10
20KΩ_1608M
R11
10KΩ_1608M
1/3rd of input voltage i.e. 1.66V for 5V input
ADC0
ADC1
PWM0
PWM1
D0
D1
USART0{USART}
USART0.TX
USART0.RX
USART0.RTS
USART0.CTS
NC on most/any MicroMod boards
G[0..4]
G0
G1
G2
G3
G4
NC on relevant processor boards or pins are re-used/conflict.
SWO
SWO isn't actually implemented on processor boards? Pinned out anyway.
RESET/BOOT BUTTONS
SW1
B3U-1000P_SPST-NO_SMD
RESET
SW2
B3U-1000P_SPST-NO_SMD
BOOT
Processor board is responsible for pull resistors or circuitry.
SWD DEBUG
X2
SWD_SMT_SOCKET
VTref
SWDIO
Gnd
SWCLK
Gnd
SWO
Key
NC/EXTb
Detect
RESET
Supports Sparkfun MicroMod hardware
Designed with ESP32, STM32, RP2040 as targets
Check processor and function board compatibility before use!
Sheet: /Processor/
File: processor.kicad_sch
Title: MicroMod Processor
Size: A4
Date: 2023-08-09
Rev: V1.0
KiCad E.D.A. kicad 7.0.6
Id: 3/6



Accepts Sparkfun's function boards

Check function board and processor support before use!

Sheet: /Function Board/
File: function-board.kicad_sch

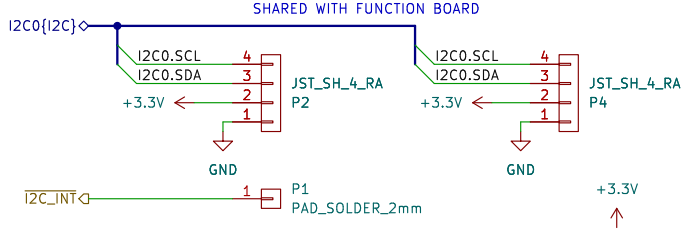
Title: MicroMod Function Board

Size: A4	Date: 2023-08-09	**Rev: V1.0**
KiCad E.D.A. kicad 7.0.6		Id: 4/6

QWIIC HEADERS

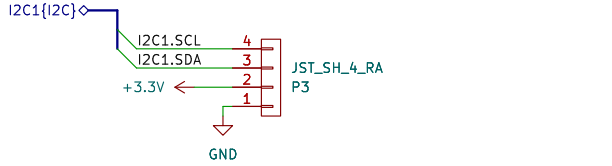
I2C BUS 0

SHARED WITH FUNCTION BOARD

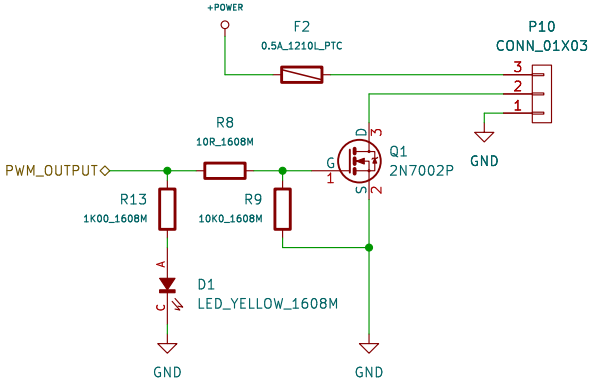


I2C BUS 1

CHECK PROCESSOR SUPPORT
IF UNSUPPORTED, CONSIDER MERGE BRIDGES

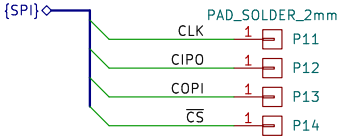


PWM OUTPUT

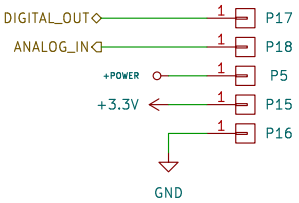


SPI1 BREAKOUT

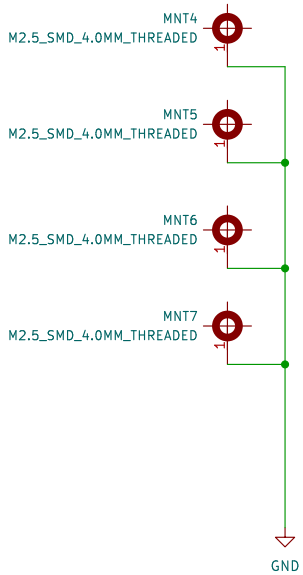
Most MicroMod Processors don't connect SPI1.
These pads allow for expansion/bodge wires.



SPARE IO



EXPANSION MOUNTS



Intended for mounting and connection of Sparkfun Qwiic sensors

Spare IO broken out as pads.
Check processor support before use!

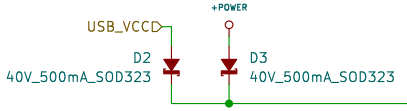
Sheet: /Expansion IO/
File: expansion.kicad_sch

Title: Expansion IO

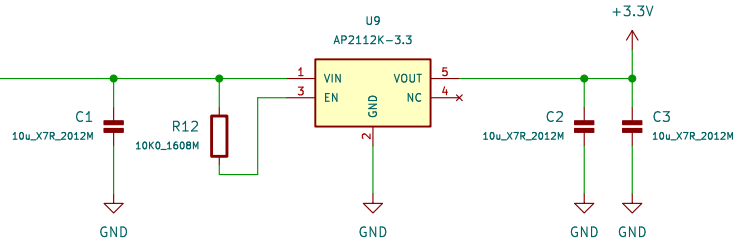
Size: A4	Date: 2023-08-09	**Rev: V1.0**
KiCad E.D.A. kicad 7.0.6		Id: 5/6

POWER INPUTS

POWER is probably +5V regulated,
back fed from PDoE/PoE function boards.



3.3V REGULATOR



Function board is meant to provide it's own regulator, so this reg supports the Processor

Sheet: /Power Regulation/		
File: power.kicad_sch		
Title: REGULATION		
Size: A4	Date: 2023-08-09	**Rev: V1.0**
KiCad E.D.A. kicad 7.0.6		Id: 7/6