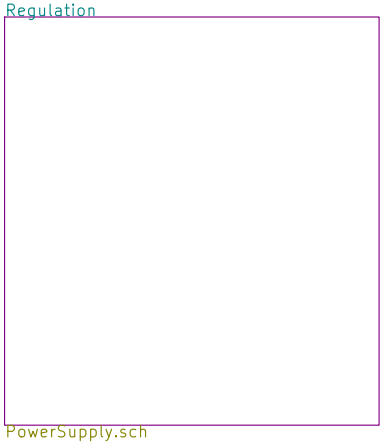
STM32-Camera Board Overview

Regulator to power microcontroller and sensor.
Input protection and filtering as required.

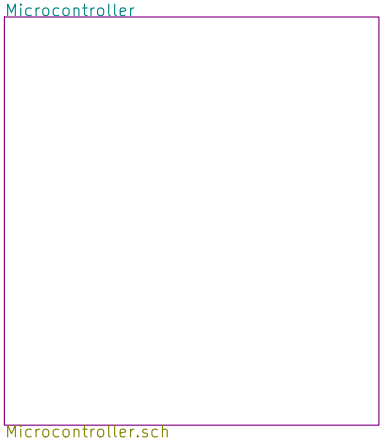
Regulation



PowerSupply.sch

STM32F4 based processor handles the show.
Clocks, debug and related hardware.
Uses standard ARM CORTEX SWD 10-pin to program

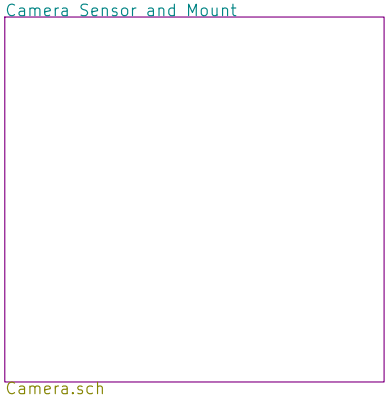
Microcontroller



Microcontroller.sch

Sensor, mounts and supporting electronics

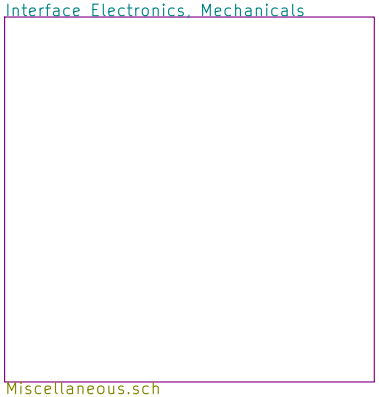
Camera_Sensor_and_Mount



Camera.sch

Miscelaneous periphery. MicroSD card.
Mounting holes, fiducials, branding, etc

Interface_Electronics, Mechanicals



Miscellaneous.sch

Sheet: / File: stm32-camera.sch		
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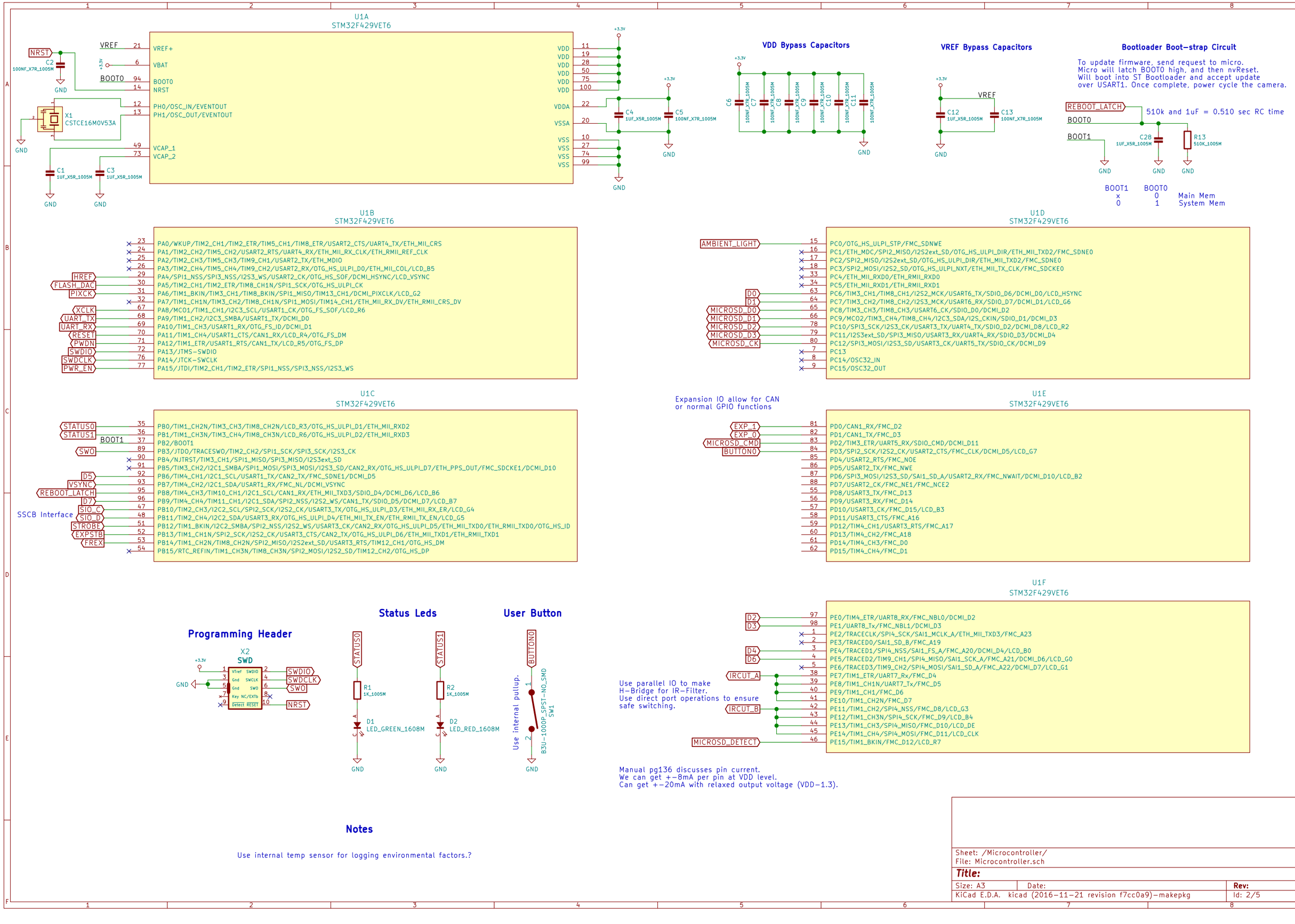
KiCad E.D.A. kicad (2016-11-21 revision f7cc0a9)-makepkg		Id: 1/5


U1A
STM32F429VET6
NRST
C2
100NF_X7R_1005M
GND
VREF
21
VREF+
+3.3V
6
VBAT
BOOT0
94
BOOT0
14
NRST
12
PH0/OSC_IN/EVENTOUT
13
PH1/OSC_OUT/EVENTOUT
X1
CSTCE16M0V53A
GND
49
VCAP_1
73
VCAP_2
C1
1UF_X5R_1005M
C3
1UF_X5R_1005M
GND
GND
VDD
11
VDD
19
VDD
28
VDD
50
VDD
75
VDD
100
VDDA
22
VSSA
20
VSS
10
VSS
27
VSS
74
VSS
99
+3.3V
C4
1UF_X5R_1005M
C5
100NF_X7R_1005M
GND
GND
VDD Bypass Capacitors
+3.3V
C6
100NF_X7R_1005M
C7
100NF_X7R_1005M
C8
100NF_X7R_1005M
C9
100NF_X7R_1005M
C10
100NF_X7R_1005M
C11
100NF_X7R_1005M
GND
VREF Bypass Capacitors
+3.3V
VREF
C12
1UF_X5R_1005M
C13
100NF_X7R_1005M
GND
Bootloader Boot-strap Circuit
To update firmware, send request to micro.
Micro will latch BOOT0 high, and then nvReset.
Will boot into ST Bootloader and accept update
over USART1. Once complete, power cycle the camera.
REBOOT_LATCH
510k and 1uF = 0.510 sec RC time
BOOT0
BOOT1
C28
1UF_X5R_1005M
R13
510K_1005M
GND
GND
GND
BOOT1 BOOT0
x 0 Main Mem
0 1 System Mem
U1B
STM32F429VET6
23
PA0/WKUP/TIM2_CH1/TIM2_ETR/TIM5_CH1/TIM8_ETR/USART2_CTS/UART4_TX/ETH_MII_CRS
24
PA1/TIM2_CH2/TIM5_CH2/USART2_RTS/UART4_RX/ETH_MII_RX_CLK/ETH_RMII_REF_CLK
25
PA2/TIM2_CH3/TIM5_CH3/TIM9_CH1/USART2_TX/ETH_MDIO
26
PA3/TIM2_CH4/TIM5_CH4/TIM9_CH2/USART2_RX/OTG_HS_ULPI_D0/ETH_MII_COL/LCD_B5
HREF
29
PA4/SPI1_NSS/SPI3_NSS/I2S3_WS/USART2_CK/OTG_HS_SOF/DCMI_HSYNC/LCD_VSYNC
FLASH_DAC
30
PA5/TIM2_CH1/TIM2_ETR/TIM8_CH1N/SPI1_SCK/OTG_HS_ULPI_CK
PIXCK
31
PA6/TIM1_BKIN/TIM3_CH1/TIM8_BKIN/SPI1_MISO/TIM13_CH1/DCMI_PIXCLK/LCD_G2
32
PA7/TIM1_CH1N/TIM3_CH2/TIM8_CH1N/SPI1_MOSI/TIM14_CH1/ETH_MII_RX_DV/ETH_RMII_CRS_DV
XCLK
67
PA8/MCO1/TIM1_CH1/I2C3_SCL/USART1_CK/OTG_FS_SOF/LCD_R6
UART_TX
68
PA9/TIM1_CH2/I2C3_SMBA/USART1_TX/DCMI_D0
UART_RX
69
PA10/TIM1_CH3/USART1_RX/OTG_FS_ID/DCMI_D1
RESET
70
PA11/TIM1_CH4/USART1_CTS/CAN1_RX/LCD_R4/OTG_FS_DM
PWDN
71
PA12/TIM1_ETR/USART1_RTS/CAN1_TX/LCD_R5/OTG_FS_DP
SWDIO
72
PA13/JTMS-SWDIO
SWDCLK
76
PA14/JTCK-SWCLK
PWR_EN
77
PA15/JTDI/TIM2_CH1/TIM2_ETR/SPI1_NSS/SPI3_NSS/I2S3_WS
U1C
STM32F429VET6
STATUS0
35
PB0/TIM1_CH2N/TIM3_CH3/TIM8_CH2N/LCD_R3/OTG_HS_ULPI_D1/ETH_MII_RXD2
STATUS1
36
PB1/TIM1_CH3N/TIM3_CH4/TIM8_CH3N/LCD_R6/OTG_HS_ULPI_D2/ETH_MII_RXD3
BOOT1
37
PB2/BOOT1
SWO
89
PB3/JTDO/TRACESWO/TIM2_CH2/SPI1_SCK/SPI3_SCK/I2S3_CK
90
PB4/NJTRST/TIM3_CH1/SPI1_MISO/SPI3_MISO/I2S3ext_SD
91
PB5/TIM3_CH2/I2C1_SMBA/SPI1_MOSI/SPI3_MOSI/I2S3_SD/CAN2_RX/OTG_HS_ULPI_D7/ETH_PPS_OUT/FMC_SDCKE1/DCMI_D10
D5
92
PB6/TIM4_CH1/I2C1_SCL/USART1_TX/CAN2_TX/FMC_SDNE1/DCMI_D5
VSYNC
93
PB7/TIM4_CH2/I2C1_SDA/USART1_RX/FMC_NL/DCMI_VSYNC
REBOOT_LATCH
95
PB8/TIM4_CH3/TIM10_CH1/I2C1_SCL/CAN1_RX/ETH_MII_TXD3/SDIO_D4/DCMI_D6/LCD_B6
D7
96
PB9/TIM4_CH4/TIM11_CH1/I2C1_SDA/SPI2_NSS/I2S2_WS/CAN1_TX/SDIO_D5/DCMI_D7/LCD_B7
SSCB Interface
SIO_C
47
PB10/TIM2_CH3/I2C2_SCL/SPI2_SCK/I2S2_CK/USART3_TX/OTG_HS_ULPI_D3/ETH_MII_RX_ER/LCD_G4
SIO_D
48
PB11/TIM2_CH4/I2C2_SDA/USART3_RX/OTG_HS_ULPI_D4/ETH_MII_TX_EN/ETH_RMII_TX_EN/LCD_G5
STROBE
51
PB12/TIM1_BKIN/I2C2_SMBA/SPI2_NSS/I2S2_WS/USART3_CK/CAN2_RX/OTG_HS_ULPI_D5/ETH_MII_TXD0/ETH_RMII_TXD0/OTG_HS_ID
EXPSTB
52
PB13/TIM1_CH1N/SPI2_SCK/I2S2_CK/USART3_CTS/CAN2_TX/OTG_HS_ULPI_D6/ETH_MII_TXD1/ETH_RMII_TXD1
FREX
53
PB14/TIM1_CH2N/TIM8_CH2N/SPI2_MISO/I2S2ext_SD/USART3_RTS/TIM12_CH1/OTG_HS_DM
54
PB15/RTC_REFIN/TIM1_CH3N/TIM8_CH3N/SPI2_MOSI/I2S2_SD/TIM12_CH2/OTG_HS_DP
U1D
STM32F429VET6
AMBIENT_LIGHT
15
PC0/OTG_HS_ULPI_STP/FMC_SDNWE
16
PC1/ETH_MDC/SPI2_MISO/I2S2ext_SD/OTG_HS_ULPI_DIR/ETH_MII_TXD2/FMC_SDNE0
17
PC2/SPI2_MISO/I2S2ext_SD/OTG_HS_ULPI_DIR/ETH_MII_TXD2/FMC_SDNE0
18
PC3/SPI2_MOSI/I2S2_SD/OTG_HS_ULPI_NXT/ETH_MII_TX_CLK/FMC_SDCKE0
33
PC4/ETH_MII_RXD0/ETH_RMII_RXD0
34
PC5/ETH_MII_RXD1/ETH_RMII_RXD1
D0
63
PC6/TIM3_CH1/TIM8_CH1/I2S2_MCK/USART6_TX/SDIO_D6/DCMI_D0/LCD_HSYNC
D1
64
PC7/TIM3_CH2/TIM8_CH2/I2S3_MCK/USART6_RX/SDIO_D7/DCMI_D1/LCD_G6
MICROSD_D0
65
PC8/TIM3_CH3/TIM8_CH3/USART6_CK/SDIO_D0/DCMI_D2
MICROSD_D1
66
PC9/MCO2/TIM3_CH4/TIM8_CH4/I2C3_SDA/I2S_CKIN/SDIO_D1/DCMI_D3
MICROSD_D2
78
PC10/SPI3_SCK/I2S3_CK/USART3_TX/UART4_TX/SDIO_D2/DCMI_D8/LCD_R2
MICROSD_D3
79
PC11/I2S3ext_SD/SPI3_MISO/USART3_RX/UART4_RX/SDIO_D3/DCMI_D4
MICROSD_CK
80
PC12/SPI3_MOSI/I2S3_SD/USART3_CK/UART5_TX/SDIO_CK/DCMI_D9
7
PC13
8
PC14/OSC32_IN
9
PC15/OSC32_OUT
Expansion IO allow for CAN
or normal GPIO functions
U1E
STM32F429VET6
EXP_1
81
PD0/CAN1_RX/FMC_D2
EXP_0
82
PD1/CAN1_TX/FMC_D3
MICROSD_CMD
83
PD2/TIM3_ETR/UART5_RX/SDIO_CMD/DCMI_D11
BUTTON0
84
PD3/SPI2_SCK/I2S2_CK/USART2_CTS/FMC_CLK/DCMI_D5/LCD_G7
85
PD4/USART2_RTS/FMC_NOE
86
PD5/USART2_TX/FMC_NWE
87
PD6/SPI3_MOSI/I2S3_SD/SAI1_SD_A/USART2_RX/FMC_NWAIT/DCMI_D10/LCD_B2
88
PD7/USART2_CK/FMC_NE1/FMC_NCE2
55
PD8/USART3_TX/FMC_D13
56
PD9/USART3_RX/FMC_D14
57
PD10/USART3_CK/FMC_D15/LCD_B3
58
PD11/USART3_CTS/FMC_A16
59
PD12/TIM4_CH1/USART3_RTS/FMC_A17
60
PD13/TIM4_CH2/FMC_A18
61
PD14/TIM4_CH3/FMC_D0
62
PD15/TIM4_CH4/FMC_D1
U1F
STM32F429VET6
D2
97
PE0/TIM4_ETR/UART8_RX/FMC_NBL0/DCMI_D2
D3
98
PE1/UART8_Tx/FMC_NBL1/DCMI_D3
1
PE2/TRACECLK/SPI4_SCK/SAI1_MCLK_A/ETH_MII_TXD3/FMC_A23
2
PE3/TRACED0/SAI1_SD_B/FMC_A19
D4
3
PE4/TRACED1/SPI4_NSS/SAI1_FS_A/FMC_A20/DCMI_D4/LCD_B0
D6
4
PE5/TRACED2/TIM9_CH1/SPI4_MISO/SAI1_SCK_A/FMC_A21/DCMI_D6/LCD_G0
5
PE6/TRACED3/TIM9_CH2/SPI4_MOSI/SAI1_SD_A/FMC_A22/DCMI_D7/LCD_G1
IRCUT_A
38
PE7/TIM1_ETR/UART7_Rx/FMC_D4
39
PE8/TIM1_CH1N/UART7_Tx/FMC_D5
40
PE9/TIM1_CH1/FMC_D6
41
PE10/TIM1_CH2N/FMC_D7
IRCUT_B
42
PE11/TIM1_CH2/SPI4_NSS/FMC_D8/LCD_G3
43
PE12/TIM1_CH3N/SPI4_SCK/FMC_D9/LCD_B4
44
PE13/TIM1_CH3/SPI4_MISO/FMC_D10/LCD_DE
45
PE14/TIM1_CH4/SPI4_MOSI/FMC_D11/LCD_CLK
MICROSD_DETECT
46
PE15/TIM1_BKIN/FMC_D12/LCD_R7
Use parallel IO to make
H-Bridge for IR-Filter.
Use direct port operations to ensure
safe switching.
Manual pg136 discusses pin current.
We can get +-8mA per pin at VDD level.
Can get +-20mA with relaxed output voltage (VDD-1.3).
Programming Header
X2
SWD
+3.3V
GND
VTref SWDIO
Gnd SWCLK
Gnd SWO
Key NC/EXTb
Detect RESET
SWDIO
SWDCLK
SWO
NRST
Status Leds
STATUS0
R1
1K_1005M
D1
LED_GREEN_1608M
GND
STATUS1
R2
1K_1005M
D2
LED_RED_1608M
GND
User Button
BUTTON0
Use internal pullup.
B3U-1000P_SPST-NO_SMD
SW1
GND
Notes
Use internal temp sensor for logging environmental factors.?
Sheet: /Microcontroller/
File: Microcontroller.sch
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Size: A3
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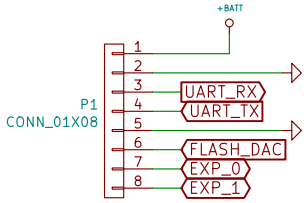
Id: 2/5

Input Protection and Regulation

Main Connector

This mimics the 2mm pitch of the adafruit VC0706
module. Unsure if this should attempt to be pin-compatible or not...



DAC output pin is also timer and ADC capable.

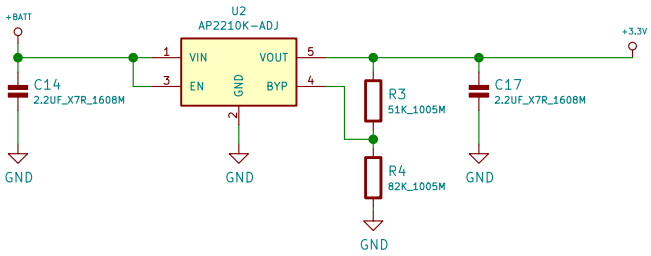
EXP pins are generic I/O (and also CAN pins)

Input Filter and polarity/esd protection???
Currently incredibly plain. Assume user is intelligent.

3.3V Regulator

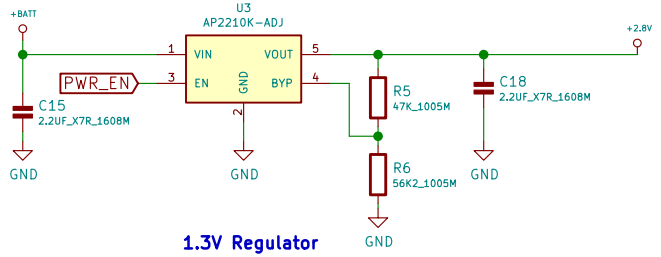
Regulator provides for microcontroller, other IC's
and is used predominantly on all pullups etc.

VOUT=1.25V*(1+R2/R1)



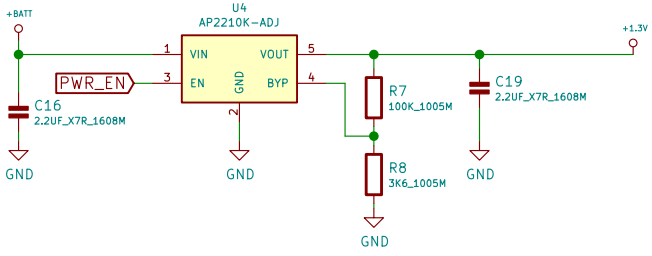
Aims for 3.259V

2.8V Regulator



Aims for 2.744V

1.3V Regulator



Aims for 1.295V

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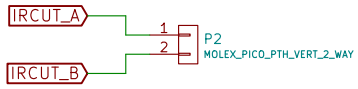
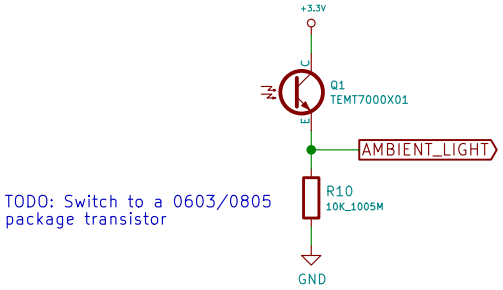
IR Cut Filter Driver

Hardware switching IR-Cut is bistable solenoid.
Use a H-Bridge style drive for control. Approx 100mA rating.
See the electronics readme for test info.



Ambient Light Sensor

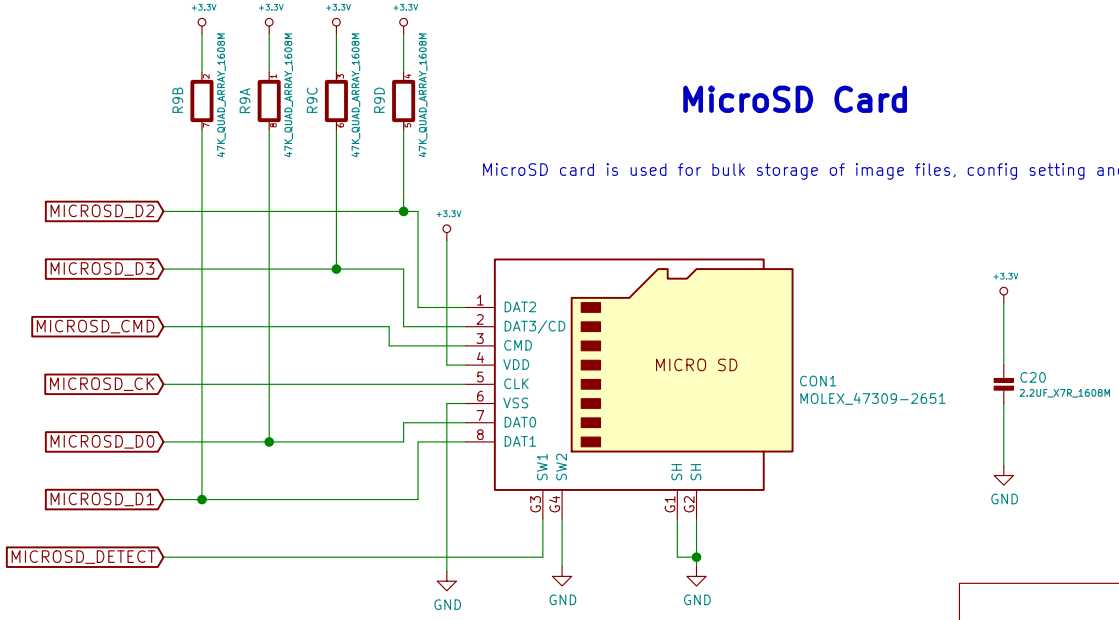
Read ambient light to select IR-cut filter etc.



TODO: Switch to a 0603/0805 package transistor

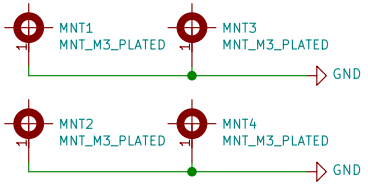
MicroSD Card

MicroSD card is used for bulk storage of image files, config setting and logs.



Fiducials

Mounting Holes



Logos and Markings

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Size: A4	Date:	**Rev:**
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2MP CMOS Camera

Camera Specifications

1600x1200px resolution.
140mW for 15fps 2MP.
1/4" sensor. 2.2um pitch.
0.6V/Lux-sec sensitivity.
40dB S/N with 50dB dynamic range.
ADC run at 20Mhz at 10-bit.

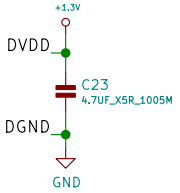
In 8-bit mode, Y0 and Y1 aren't used.
Thus LSB is D2.
No pull resistors on these pins.

PIXCK - Pixel clock from sensor
6Mhz = 2.5fps
36Mhz = 15fps

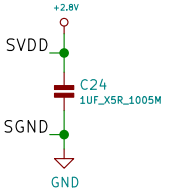
VSYNC - Active FRAME
HREF - Active Pixels/Line
See page 7 of overview appnote

If DOVDD is same as AVDD, share reg and use hardware RC to separate.
Otherwise use 3 regs...

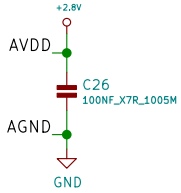
Sensor Core



Sensor Array



Analog Frontend



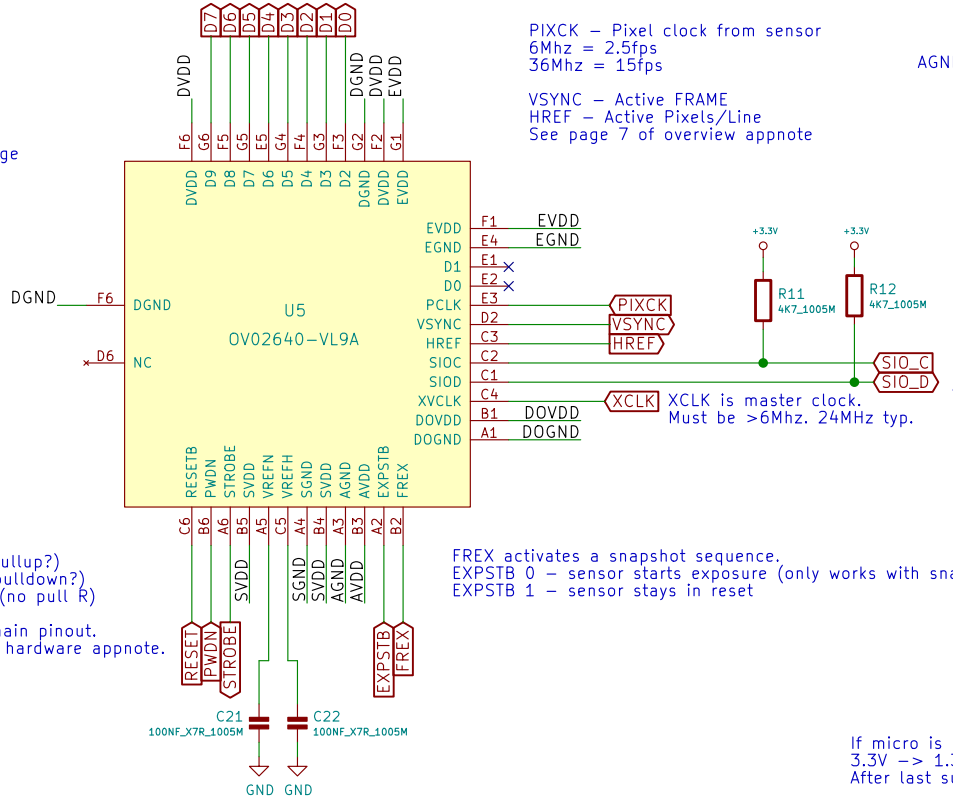
AGND and DGND should be connected outside sensor area grounding

IR-Cut Switchable Filter Lens Mount

Bisable Solenoid drive and connector on last page

MP1
M12_LENS_MOUNT_IR_SWITCHNG

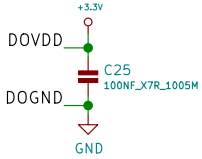
HAS FLYING LEAD WITH
1.25mm 2x1 PLUG



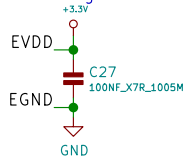
I2C Config Interface.
Recommended 100k during bringup.
400kHz capable.

XCLK is master clock.
Must be >6Mhz. 24MHz typ.

Digital IO



Internal Regulator



RESET Active Low (internal pullup?)
PWDN Active High (internal pulldown?)
STROBE indicates flash LED (no pull R)

Pull Up/Down specified in main pinout.
Specified as not included in hardware appnote.

FREX activates a snapshot sequence.
EXPSTB 0 - sensor starts exposure (only works with snapshot)
EXPSTB 1 - sensor stays in reset

If micro is disabling/enabling regs sequentially, ensure turn on order is:
3.3V -> 1.3V -> 2.8V or the camera gets angry.
After last supply is on for 3ms, the reset line on the OV2460 can go high.

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