Electrical specification and QC procedures for ITkPixV1.1 modules

rev.
https://gitlab.cern.ch/atlas-itk/pixel/module/itkpix-electrical-qc

Abstract

This document describes the electrical specifications for fully assembled pre-production (ITkPixV1.1) modules, and the quality control (QC) testing procedures to be used to verify that the modules meet the electrical specifications. The electrical specifications for the pre-production and production modules are identical, except for the numerical values of the requirements, that will be updated for production based on the experience acquired during pre-production.

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Distribution List

History of Changes

Rev. No.	*Date*	*Sections*	*Description of changes*
Draft	01 Apr 2022	All	Git repo
	06 Apr 2022	All	Injection capacitance
1.0	26 Jan 2023	All	Finalise specs and procedures for release 1
2.0	10 May 2023	All	
2.1	24 Oct 2023	All	
2.2	21 Feb 2024	Powering, Testing Flow	Add sensor operational voltages for sensor types
2.2	02 Mar 2024	Appendix	Add PSU specifications from RD53A document
2.2	xx Jul 2024	Powering, Testing Flow, criteria	L1 cuts, remove ROSC and current cuts post PRR
2.2	26 Aug 2024	All	Clean up code and make more readable
2.2	29 Oct 2024	Testing Flow	Remove OVP and USP from testing flow
2.2	04 Nov 2024	Appendix	Update multimeter voltage precision for currents
2.2.1	12 Dec 2024	Powering, Testing Flow	Add back depletion voltage based operational voltage for planar sensors as discussed with Koji and Richard
2.2.2	11 Mar 2025	Testing Flow	Add core column scan to testing flow

Contents

1 Introduction

This document describes the electrical specifications for fully assembled pre-production (ITkPixV1.1) modules, and the quality control (QC) testing procedures to be used to verify that the modules meet the electrical specifications.

The electrical specifications for the pre-production and production modules are identical, except for the numerical values of the requirements, that will be updated for production based on the experience acquired during pre-production.

Pre-production and production modules use different version of the ASIC: version ITkPixV1.1 for pre-production and version ITkPixV2 for production.

ITkPixV1.1 implements a fix for a bug in the time-over-threshold (ToT) memory discovered when the first ITkPixV1.0 chips were tested. This fix reduces the ToT to a binary output, hence limiting the ability to test some of the properties of this part of the chip. The test that will be needed for ITkPixV2 ToT circuit that can't be performed with ITkPixV1.1 are listed in this document.

The powering behaviour of the triplet/quad modules are driven by the components placed on the hybrid. These components control the share of current between the analog and the digital domain in each chip (and hence the effective resistance of the chips) and the offset voltage of the V-I curve for normal and low-power mode. The values of these components are extracted from on complex simulations that rely on the chip current consumption in operation and chip-to-chip variations to maximize module yield while minimizing the power dissipated by the modules. Hence, the large statistics of pre-production modules will provide useful information on some of the assumptions of the simulation, and will inform the final values of these components for production. The pre-production modules will also provide a better understanding of the noise and defects of the modules, and will be used to update the criteria used in wafer-probing to grade chips as green in time for production.

In the main part of this document the technical specifications are given and in the appendices are procedures for testing and technical details for developers.

2 Specifications

2.1 Powering

This section provides the list of tests and the criteria to be used to select good modules. The details about the procedures on how to perform the measurement are detailed in Appendix B.
For each chip, 3 different configuration files are needed:

- warm temperature: based on values from waferprobing, specific to the type of module
- cold temperature: based on values from waferprobing, specific to the type of module. Needs different analog-to-digital converter (ADC) calibration from the warm temperature config. After tuning, it will be different wrt to warm temperature config.

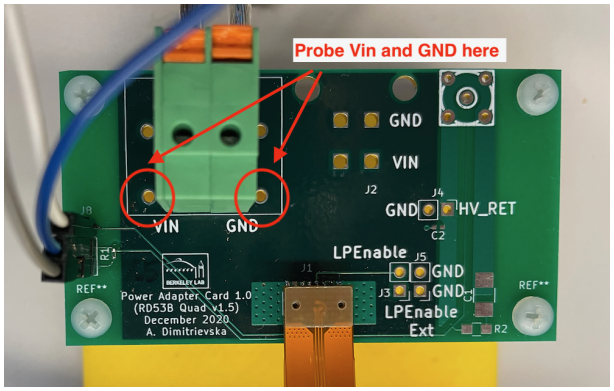

Figure 1: Probe Vin on the power adapter card.

- low power (LP) configuration

Section A.3.1 list the parameters in the config files that are changed for the different configurations. Make sure to use the correct config file for the type of module under test (L0/triplet, L1 or L2-L4).

The sensor tile has to be reverse biased at the operational voltage to ensure over-depletion for all electrical tests (except for the first power-up which is meant to be a quick check). The jumper GND-HV_RET on the power adapter board, shown in Fig. 1, should be closed. These values below are the operational voltages for the corresponding sensor types [1] to be used throughout electrical testing. Between the voltage based on the full depletion voltage V_{fd} and the fixed value, the more convenient one can be used.

- 3D sensor: 10 V
- 100 µm planar sensor: $V_{fd} + 50$ V or 80 V
- 150 µm planar sensor: $V_{fd} + 50$ V or 120 V

2.2 First Power-up

- **Goal**: check minimal functionality of the module
- **Pass criteria**: Vin is within expected range (see Table 1)

Power up the module with the nominal input current and measure Vin using a multimeter. The nominal current to be used depends on the type of module being powered. See Table 1 for the value of nominal current for different types of modules. To measure Vin, probe with a multimeter as described in Fig. 1. Use a separate multimeter and do not connect any sense line to the power supply. The measured value of Vin needs to satisfy the requirement in Table 1 to pass this test. The expected value of Vin measured on the adapter card needs to take into account the roundtrip voltage drop from the adapter card to the module and back. This was measured to be 0.045 Ω for quads using the 15 cm long power pigtail [**?**] and 0.040 for triplets using the 15 cm power pigtail [2].

2.3 Sensor IV

- **Goal**: ensure that the sensor leakage current as a function of the bias voltage (IV) is within specs defined in the module specs [3]

type of module	RextA [Ω]	RextD [Ω]	I_{in}/FE chip [A]	nominal Vin [V]
L0/triplets	511	407	1.85	$(1.498\,\mathrm{V} + 1.85\,\mathrm{A} * 3 * 0.040\,\Omega) \pm 0.038\,\mathrm{V}$
L1	732	549	1.65	$(1.488\,\mathrm{V} + 1.65\,\mathrm{A} * 4 * 0.045\,\Omega) \pm 0.038\,\mathrm{V}$
L2-L4	866	590	1.47	$(1.493\,\mathrm{V} + 1.47\,\mathrm{A} * 4 * 0.045\,\Omega) \pm 0.038\,\mathrm{V}$

Table 1: Nominal input current and voltage values for different types of modules in more details.

Pass criteria [3]:

- Maximum sensor leakage current increase compared to that measured on the bare module at bare module reception: factor of 2 for both 3D and planar.
- The absolute sensor leakage current for
  - 3D at V_{depl}+20 V: less than 5.0 μA/cm2
  - planar at V_{depl}+50 V: less than 1.5 μA/cm2
- Maximum reduction in the breakdown voltage compared to that measured at sensor reception
  - 3D: 10 V
  - planar: If the breakdown voltage measured at sensor reception is > 200 V then the final module breakdown voltage must be > 200V, otherwise the change of the breakdown voltage compared to the bare module sensor acceptance test: < 10 V
- The absolute breakdown voltage
  - 3D: $> V_{depl}$+20 V
  - planar: $> V_{depl}$+70 V

Sensor IV has to be measured both warm and cold in a **dark** environment with RH<50 %. Specifications for sensor characteristics are only defined for warm temperature (20 °C). Both warm and cold measurements will be analysed against the specifications at 20 °C, where the warm IV will be normalised to 20 °C while the cold will not. We do not expect any failure mode that does not occur at high temperatures but only occurs at low temperatures. Under normal circumstances, only the warm IV will be considered for the overall module grading, while the pass/fail of the cold IV will not contribute. This is because at low temperatures, the leakage current of the sensor might be below the sensitivity of the measuring instrument. Despite this possibility, IV should still be measured at low temperatures. If breakdown is observed during a cold IV, the increased sensor leakage current will become detectable to the measuring instrument.

2.4 Shunt Low Drop Out regulator (SLDO) Qualification

- **Goal**: check that after configuration all the front-end (FE) chip internal values are within normal operational range; verify the performance of the SLDO

Pass criteria:

- All internal voltages at the nominal current are within expected range (see Table 2)

- All internal currents at the nominal current are within expected range (see Table 3)
- VinA and VinD agree within 0.05 V
- The Analog and digital shunt currents are higher than a minimal value (see Table 4)
- The input voltage Vin as a function of the input current Iin for SLDO (VI) curve is linear, and follows the prediction (see Table 5) ¿¿¿¿¿¿¿ master

This test should be performed at both warm and cold temperatures. Power on the module at nominal current, configure each chip with the warm configuration file associated with module type, and measure all internal currents/voltages using VMux (see Appendix B.5 for detailed explanations). Repeat at low temperature. Since the analog and digital parts are powered in parallel, VinA and VinD should be identical. If they do not agree within 0.01V, the chip fails this test. If the values of the internal current/-voltages of all FE chips do not fall in the expected range, the module failed this test. To guarantee that enough analog and digital current overhead is available during operation, the analog and digital shunt currents during testing have to be higher than the values given in Table 4. The overhead is defined as IshuntA/(I_{in}A - IshuntA) for analog and IshuntD/(I_{in}D - IshuntD) for digital.

type of module	RextA [Ω]	RextD [Ω]	I_{in}/FE [A]	VDDA/D [V]	VinA/D [V]	Voffs [V]
L0/triplets	511	407	1.85	1.2 ± 0.01	$1.498^{+0.038}_{-0.035}$	1.1 ± 0.011
L1	732	549	1.65	1.2 ± 0.01	$1.488^{+0.038}_{-0.035}$	0.990 ± 0.011
L2-L4	866	590	1.47	1.2 ± 0.01	$1.493^{+0.038}_{-0.035}$	0.990 ± 0.011

Table 2: Nominal values for internal voltages

type of module	RextA [Ω]	RextD [Ω]	I_{in}/FE chip [A]	I_{in}A [A]	I_{in}D [A]	IRef [μA]
L0/triplets	511	407	1.85	0.81905 ± 0.0313	1.02835 ± 0.0537	4 ± 0.3
L1	732	549	1.65	0.70766 ± 0.0270	0.94354 ± 0.0489	4 ± 0.3
L2-L4	866	590	1.47	0.59665 ± 0.0294	0.87575 ± 0.0383	4 ± 0.3

Table 3: Nominal values for internal currents, with target/minimal overhead during operation of 10%/1% for analog and 20%/10% for digital.

type of module	RextA [Ω]	RextD [Ω]	I_{in}/FE chip [A]	IshuntA [A]	Overhead(A)	IshuntD [A]	Overhead(D)
L0/triplets	511	407	1.85	$0.0691 - 0.0613$	1%	$0.3463 - 0.0809$	10%
L1	732	549	1.65	$0.0597 - 0.0529$	1%	$0.2615 - 0.0762$	10%
L2-L4	866	590	1.47	$0.0566 - 0.0510$	1%	$0.1938 - 0.0656$	10%

Table 4: Chip shunt current and overhead while testing, with target/minimal overhead during operation of 10%/1% for analog and 20%/10% for digital, assuming input current and Rext as in Table 2.

Perform a VI scan of the module following the procedure in Appendix B.5. Perform the VI scan using the config corresponding to module type. Perform it both warm and cold. To determine if the VI curve is linear, compare the value of Vin measured via VMUX with the expected value V_{theory}. Vin in this case is defined as the average value of

VinA and VinD for a given I_{in}. The expected value V_{theory} is calculated with the following formula, as a function of I_{in}:

$$V_{theory}(I_{in}) = R_{eff} \cdot I_{in} + Vofs,$$

where

$$R_{eff} = \frac{1}{\frac{kA}{RextA} + \frac{kD}{RextD}},$$

where kA and kD are taken from waferprobing, RextA and RextD are the SLDO resistor loaded on the flex, and Vofs is taken from Table 2. The VinA and VinD measured via VMux needs to satisfy

$$||V(I_{in}) - V_{theory}(I_{in})||_2 = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(V({I_{in}}^i) - V_{theory}({I_{in}}^i)\right)^2} < 0.035V$$

for each value of the input current, for each chip for the module to pass this test.

type of module	RextA [Ω]	RextD [Ω]	Threshold
L0/triplets	511	407	$\lvert V(I_{in}) - V_{theory}(I_{in})\rvert < 0.035V$
L1	732	549	$\lvert V(I_{in}) - V_{theory}(I_{in})\rvert < 0.035V$
L2-L4	866	590	$\lvert V(I_{in}) - V_{theory}(I_{in})\rvert < 0.035V$

Table 5: Requirements for SLDO

2.5 Low power (LP) Mode

- **Goal:** verify functionality of the LP mode for the nominal LP current

Pass criteria :

- Vin and Voffs within specification
- Digital current within specification
- The analog and digital shunt currents (IshuntA/IshuntD) are non-zero
- The LP digital scan when run has to return a histogram to check if there is connectivity.

type of module	$RIoff_{LP}$ [Ω]	RextA [Ω]	RextD [Ω]	${I_{in}}^{LP}$/FE chip [A]	$VinA^{LP}$ / $VinD^{LP}$ [V]	V_{offs}^{LP} [V]
L0/triplets	7060	511	407	0.542	1.493 $\pm TBD$	1.383 $\pm TBD$
L1	8450	732	549	0.528	1.493 $\pm TBD$	1.340 $\pm TBD$
L2-L4	8200	866	590	0.503	1.494 $\pm TBD$	1.329 $\pm TBD$

Table 6: Nominal values for internal voltages and currents for the LP mode. Tolerances to be updated.

When the module is powered with LP nominal current given in Table 6 (depending on the layer), the values of VinA, VinD and Voffs in the LP mode should be in the ranges given in Table 6, while the ranges of accepted internal currents are given in Table 7. See Appendix B.8 for detailed measurement explanations.

type of module	RextA [Ω]	RextD [Ω]	IinA^{LP}/FE chip [A]	IinD^{LP}/FE chip [A]	IshuntA^{LP}/FE chip [A]	IshuntD^{LP}/FE chip [A]
L0/triplets	511	407	0.242 $\pm TBD$	0.30 ±0.02	0.092	0.050
L1	732	549	0.228 $\pm TBD$	0.30 ±0.02	0.078	0.050
L2-L4	866	590	0.203 $\pm TBD$	0.30 ±0.02	0.053	0.050

Table 7: Nominal values for internal currents per FE chip in the LP mode. Tolerances to be updated.

2.6 Over-voltage protection (OVP)

- **Goal:** verify functionality of the OVP mechanism

Pass criteria :

- for a given current $|\text{Vin(theory)} - \text{Vin(measured)}| > 0.040\,\text{V}$
- total current is less than what is being put in by the power supply (PS): IinA+IinD $<$ Iin^{PS}

When powered in LP mode using the currents given in Table 8 the measured voltages should be in the ranges given in Table 8. See Appendix B.9 for detailed measurement explanations.

type of module	Iin^{PS}/FE chip [A]	Vin (theory) [V]	VrefOVP [V]	Vin (measured) [V]
L0/triplets	TBD	2.1	< 2.05	VrefOVP
L1	TBD	2.1	< 2.05	VrefOVP
L2-L4	1.75	2.1	< 2.05	VrefOVP

Table 8: Input current and input voltage, and expected values of VrefOVP.

type of module	Iin/FE chip [A]	IinA [A]	IinD [A]
L0/triplets	TBD	TBD	TBD
L1	TBD	TBD	TBD
L2-L4	1.75	0.71	0.95

Table 9: Input current and expected values of internal currents.

2.7 Under-shunt protection (USP)

- **Goal:** verify functionality of the USP mechanism (we can only test steady state)

Pass criteria :

- Vin is unchanged when the under-shunt protection mechanism is triggered
- VrefD/A, VDDD/VDDA and IshuntD/A values change when the under-shunt protection mechanism is triggered in the digital/analog domain

The expected change in internal voltages (currents) when USP is triggered according to the procedure described in Appendix B.10 is shown in Table 10 (11).

type of module	RextA [Ω]	RextD [Ω]	I_{in}/FE chip [A]	ΔVDDA [V]	ΔVDDD [V]	ΔVinA[V]	ΔVinD [V]	ΔVrefA [V]	ΔVrefD[V]
L0/triplets	511	407	TBD	$TBD \pm TBD$	$TBD \pm TBD$	$TBD \pm TBD$	$TBD \pm TBD$	$TBD \pm TBD$	$TBD \pm TBD$
L1	732	549	0.528	0.125 ± 0.075	0.125 ± 0.075	0.0 ± 0.005	0.0 ± 0.005	0.09 ± 0.06	0.09 ± 0.06
L2-L4	866	590	0.503	0.125 ± 0.075	0.125 ± 0.075	0.0 ± 0.005	0.0 ± 0.005	0.09 ± 0.06	0.09 ± 0.06

Table 10: Expected decrease in internal voltages when USP is triggered.

type of module	RextA [Ω]	RextD [Ω]	I_{in}FE chip [A]	ΔIinA[A]	ΔIinD [A]	ΔIshuntA [A]	ΔIshuntD[A]
L0/triplets	511	407	TBD	$TBD \pm TBD$	$TBD \pm TBD$	$TBD \pm TBD$	$TBD \pm TBD$
L1	732	549	0.528	0.0 ± 0.005	0.0 ± 0.005	0.075 ± 0.025	0.075 ± 0.025
L2-L4	866	590	0.503	0.0 ± 0.005	0.0 ± 0.005	0.075 ± 0.025	0.075 ± 0.025

Table 11: Expected decrease in internal currents when USP is triggered.

2.8 E-fuses

- **Goal**: E-fuse is written correctly and readable

Pass criteria:

- Read e-fuse register and compare to correct value.

While it does not impact operation if the e-fuse is not correctly written or readable and e-fuses are not radiation tolerant, during the production and early commissioning phase e-fuses are a vital tool to map out which front-end chips are connected where.

2.9 Data Transmission

2.9.1 Eye diagram

- **Goal**: Data-link quality is sufficient for operation in the detector system with full services and connected to Low Power GigaBit Transceiver (lpGBT)

Pass criteria:

- In the eye diagram measured with all data links from a module, the eye width and eye height have to satisfy the criteria of Table 12.

- The eye diagram height shall be measured with two different CmlTapBias0 1 settings to observe the correct function of the CML current setting.

parameter	min. value	comment
eye width [ns]	0.7	90% open
eye height [mV]	500	

Table 12: Requirements for Eye diagram under nominal settings

As eye diagram measurements on the module level will be performed with temporary services, the pass criteria for the eye are a proxy for what is expected if a module which passes these criteria will correctly work within the detector system with full services and connected to an lpGBT.

2.9.2 Link sharing

- **Goal**: Ensure that chip to chip communication within a module is fully working with margin

Pass criteria:

- In a specialized test which occupies the data links to 100% with data non of the data shall be lost
- Test all possible chip to chip data transmission modes (2 secondary chips transmitting on two lanes to 2 primary chips and 3 secondary chips transmitting on one lane to 1 primary chip)
- Test potential failure modes (chip defect or wirebond defect which could lead to loosing one lane)

Many other chip parameters have been measured and optimised during wafer probing. Ideally, these values can be used directly on the module, if the same parameters measured on a module agree well with the wafer probing data, or if discrepancies are well understood.

- **Goal**: During pre-production we want to cross-check these parameters by comparing measurements done at wafer probing with measurements taken on the module, in order to determine which measurements can be dropped for production.

2.10 ADC Calibration

- **Goal**: Cross-check and update the ADC calibration done at wafer probing with the help of an external multimeter. The calibrated ADC then can be used to measure all internal voltages and currents without the necessity of an external multimeter.

Pass Criteria

- Calibration Slope = $(0.187 \pm 0.037)\,\mathrm{mV}$/least significant bit (LSB)
- Calibration Offset = $(11 \pm 20)\,\mathrm{mV}$
- Calibration Linearity = $(0 \pm 4)\,\mathrm{mV}$

See Appendix B.3 for detailed calibration explanations.

2.11 Vcal Calibration

- **Goal**: Cross-check and update the Vcal calibration measured at wafer probing. The Vcal is the internal calibration voltage used for chip tuning.

Pass Criteria

- Calibration Slope (large range) = $(0.2 \pm 0.04)\,\mathrm{mV/LSB}$
- Calibration Offset (large range) = $(-3 \pm 20)\,\mathrm{mV}$
- Small Range Slope/Large Range Slope = $(50 \pm 1)\,\%$
- Calibration Linearity = $(0 \pm 4)\,\mathrm{mV}$

See Appendix B.6 for detailed calibration explanations.

2.12 Injection Capacitance

- **Goal**: Cross-check and update the injection capacitance measured at wafer probing. This capacitance is used to calculate the injected charge used for chip tuning.

Pass Criteria

- Injection capacitance = (7.87± 1.13) fF

See Appendix B.7 for detailed calibration explanations.

2.13 Analog Readback

- **Goal**: Read back and verify all chip internal voltages and currents.

See Appendix B.4 for detailed explanations.

2.13.1 Temperature sensors

Pass Criteria

- Chip negative temperature coefficient (NTC) ($T_{ChipNTC}$) and External NTC should match with ±2 °C
- Temperature of the metal-oxide-semiconductor (MOS) sensors = ($T_{ChipNTC} + 3 \pm 5$) °C
- Temperature of the Poly sensors = ($T_{ChipNTC} + 3 \pm 8$) °C

See Appendix B.4.2 for detailed explanations.

2.13.2 Miscellaneous

Pass Criteria

- GADC : (0.824 ± 0.082) V
- VcalDac : (0.828 ± 0.083) V
- AnaGND30 : (0.023 ± 0.002) V
- VrefCore : (0.464 ± 0.046) V
- VrefOVP : (1.965 ± 0.196) V
- VrefA : (0.573 ± 0.057) V
- VrefD : (0.568 ± 0.057) V

2.14 Pixel Performance

The number of pixels is 153600 (384 rows × 400 columns) in one chip (614400 in a quad). A full tuning procedure should be performed at both warm and cold temperatures (using different configuration files). Bad pixel classification is performed using the cold temperature configuration.

Total percentage of failed pixels is 1%, and this is after all detector construction steps (including loading). See Appendix B.11 for detailed explanations.

2.14.1 Minimum Health Test

- **Goal**: Minimal set of scans to check functionality of chip in between stages.
- **Pass criteria**:
  - Total number of failing pixels in digital and analog scan is less than 0.1%, where a failure is defined as the number of hits in a pixel being ± 2 of the number of injections.
  - The number of failing s-curve fits in a threshold scan (threshold = 0) is less than 1%.
  - The number of pixels with excessive noise (mean noise from threshold scan $< 200e$ (L0) or $< 300e$ (L1/L2)) is less than 1%.

This test serves as a very fast crosscheck of the functionality of a chip. It will not be possible to determine any pixel specific count from this test, but it will identify gross defects.

2.14.2 Tuning performance

- **Goal**: Check that a tuning was overall successful and the chip behaves as expected.
- **Pass criteria**:
  - Untuned mean threshold is 2000e ± 500e.
  - Untuned number of pixels failing a s-curve fit (threshold = 0) is less than 1%.
  - Untuned (all TDACs = 0) threshold dispersion (RMS) is less than 400e.
  - Tuned mean threshold is 1000e ± 100e
  - Tuned threshold dispersion (RMS) is less than 50e.
  - Tuned mean ToT response is 7 ± 1 bc for L0 or 7 ± 1 bc for a test charge of 6000e.
  - Tuned ToT dispersion is less than 1 bc for a test charge of 6000e.
  - Tuned mean TDAC is 0 ± 1.
  - Tuned TDAC dispersion (RMS) is 10.5 ± 2.

This test serves to determine if the overall "tune-ability" of the chip is consistent with expectations. Outliers could indicate that the specific chip has less dynamic tuning range or can't be tuned as well as other chips in the detector.

This test also serves as a container to store the chip configurations post tuning for future use.

2.14.3 Pixel Failure Test

To accurately account for the bad pixels, the results of the digital and analog scan are taken after full tuning of the module as it is possible that the analog scan reports some pixels as bad which might come from them just being far from ideal tuning.

2.14.3.1 Electrical Pixel Failure Test

Bad pixels include digital dead, digital bad, analog dead, analog bad, and noisy pixels. Criteria for pixels to fall in each of these categories are given in Table 13. The categories are mutually exclusive and each bad pixel can only fall into one of the categories. The order of the categories is such that the highest level pixel functionality is tested and categorised first. E.g. if the digital part of a pixel fails, there is no way to make any statement about the analog behaviour, thus the pixel counts as digitally dead/bad and is excluded from any further categorisation. The percentage of bad pixels is required to be less that 0.1% after module assembly.

Failure	Scan type	Criteria
Digital Dead	Digital Scan	Occupancy<1% of injections
Digital Bad	Digital Scan	Occupancy<98% or>102% of injections
Analog Dead	Analog Scan	Occupancy<1% of injections
Analog Bad	Analog Scan	Occupancy<98% or>102% of injections
Tuning Bad	Threshold Scan	|Pixel threshold - Mean threshold distribution| > 5×40e^* [4]
High ENC	Threshold Scan	Mean pixel noise > 200e (L0) or > 300e (L1/L2)
Noisy	Noise Scan	Occupancy> 10^{-6} hits per BC
ToT Memory Failure	ToT Memory test	Occupancy <100% of injections

Table 13: Electrical pixel failure categories

2.14.3.2 Full Pixel Failure Test

The full pixel failure test will aim to measure in addition to the electrical failure modes described above if a pixel is connected to the sensor element. The various methods and criteria for identify disconnected and merged bumps are listed in Table 14.

Scan type	Criteria
Disconnected bump Scan	Occupancy<50% of injections
Source scan (self-trigger)	Occupancy<10 hits
Zero-bias scan	-
Merged bump scan	Occupancy>50% of injections and neighboring another failing pixel

Table 14: Disconnected bump failure categories

If source scan data is present, pixels failing either the disconnectd bump scan or the source scan are considered disconnected. If source scan data is not present, pixels failing the disconnected bump scan are considered disconnected. The zero-bias scan data is currently not used to determine if a bump is disconnected.

According to Ref. [3] the number of disconnected / merged bumps allowed is 600 (0.39%) per chip after thermal cycling.

3 Testing Flow

Prepare the experimental setup! See Section A.2.

- Non-electrical test: Visual Inspection
- Electrical test
  - First power-up (without data acquisition (DAQ) to check power consumption)
  - Module sensor leakage current as a function of the bias voltage (IV) without LV
  - (Apply operational voltage to the sensor for all following tests)
    - 3D sensor: 10 V
    - 100 µm planar sensor: $V_{fd} + 50$ V or 80 V
    - 150 µm planar sensor: $V_{fd} + 50$ V or 120 V
  - Eye Diagram
  - Core column scan
  - ADC Calibration and update chip configurations
  - Analog Readback and update chip configurations
  - SLDO Qualification
  - Vcal Calibration and update chip configurations
  - Injection Capacitance and update chip configurations
  - Low Power Mode
  - Data Transmission incl. data merging (link sharing)
  - Minimum Health Test
  - Tuning
  - Pixel Failure Analysis

The recommended tools to be used for module QC can be found in Inner Tracker (ITk) Pixel Module git repository [5]. The module connectivity and chip configuration files are generated with the database tools [6] using the data from the production database. It is recommended to use the measurement tools [7] to perform QC measurements. Appendix B provides some details on how to take the measurements. To guarantee that the module grading is done uniformly at all sites, common analysis tools were developed. They can be found in Module QC Analysis Tools [8]. After each calibration measurement (ADC Calibration, Analog Readback, Vcal calibration and injection capacitance), the result of the analysis should be used to update the chip config. To do this, tools are provided in the Module QC Analysis Tools.

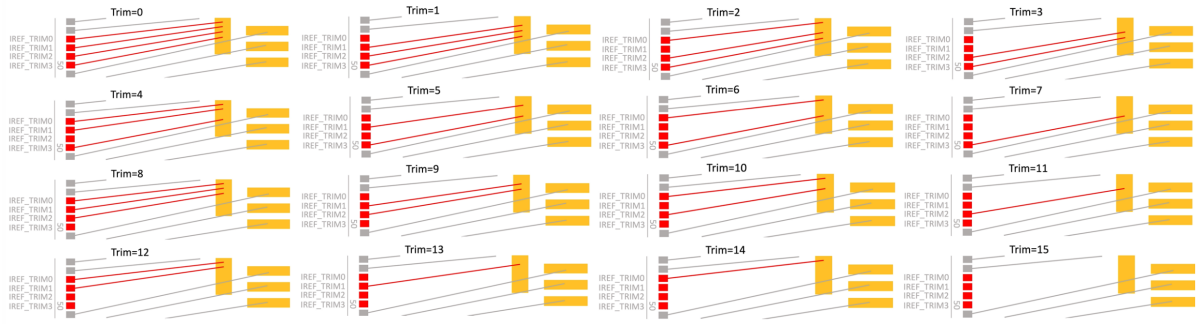

Figure 2: Iref Trim

A General Information

A.1 Visual Inspection of Iref Trim

Make sure that the Iref trim bonds are bonded according to wafer probing data. Iref trim bit can be found in the ITk Production Database. Fig. 2 show how the wirebonds should be bonded for each trim value.

A.2 Experimental Setup

A.2.1 Equipment for electrical test

- Low voltage (LV) Power supply
- High voltage (HV) Power supply
- Power adapter card
- Readout adapter card 1 Display Port
- Power pigtail
- Power cable of American wire gauge (AWG) 16 or better
- Data pigtail
- Multimeter (VMUX measurements) [9]
  - The minimum required precision on extracted quantities measured through VMUX and IMUX are listed in Table 15. These values are determined from the precision of the QC selection criteria. The ground value (VMUX 30 and IMUX 63) should be measured with at least the precision of the VMUX/IMUX value from which it will be subtracted.
  - Require min. 5.5 digit resolution (down to 0.1 mV), high input impedance (>1 MΩ), differential input
  - Recommended models: Keithley DMM6500 [10] (1.4 k$) plus 10-channel multiplexer card (800 $), Keithley 2100 [11], Keithley 2700 [12] (multiplexer cards available with up to 40 channels) [13]

- NTC readout from the power adapter card

VMUX	Precision	IMUX	Precision
0	1 mV	0	1 mV
1	See Imux column	1	1 mV
2	1 mV	2	1 mV
3	100 μV	3	1 mV
4	100 μV	4	1 mV
7	1 mV	5	1 mV
8	1 mV	6	1 mV
14	1 mV	7	1 mV
16	1 mV	8	1 mV
18	1 mV	10	100 μV
30	Ground	11	100 μV
31	1 mV	12	1 mV
32	100 μV	13	1 mV
33	100 μV	14	1 mV
34	100 μV	15	1 mV
35	1 mV	16	10 mV
36	100 μV	17	1 mV
37	100 μV	18	1 mV
38	100 μV	19	1 mV
39	1 mV	20	1 mV
		21	1 mV
		22	1 mV
		23	1 mV
		24	1 mV
		25	1 mV
		28	1 mV
		29	1 mV
		30	1 mV
		31	1 mV
		63	Ground

Table 15: Minimum required precision on multimeter for voltages read through the VMUX and IMUX.

A.2.2 Readout System

Readout adapter card version v1.5 should be used. Make sure that the card has correct surface-mount device (SMD) components loaded (**need reference**).

Use the latest tagged YARR version found at this link https://gitlab.cern.ch/YARR/YARR. Table 16 shows the firmware (FW) and controller config to be used. Use the 1.28 GHz firmware which corresponds to your PCIe.

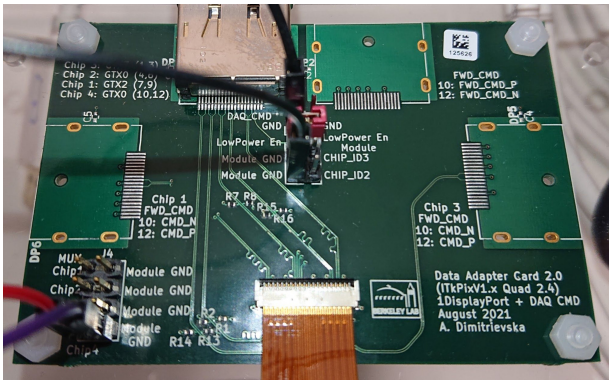

Figure 3: Config of the data adapter card. The VMUX output of the 4 chips are shorted on the backside. The Module GND should be connected to the DAQ_CMD GND via a jumper wire. The red jumper connects LowPower En (from the DAQ) and LowPower En Module required for measurements in LP mode and can be left in place for other measurements.

Readout adapter	FW	Controller config
1DP	16×1	`specCfg-rd53b-16x1.json`

Table 16: Readout adapter card, FW and controller config.

A.3 Electrical Test

A.3.1 Configurations

There are different configuration files depending on the layer the module is meant for and if it is low power (LP) config or not and depending on the temperature. These are summerized in Table 17 and Table 18. When testing LP mode and OVP, it should be done with LP config. Normal powering mode should be tested using both default config. Module configs are also different depending on the temperature (one config for warm test and one for cold test). Summary of various testing settings is shown in Table 19.

To generate all the configuration and connectivity files the module-qc-database-tools package should be used following the instruction in the git repository.

	L0 (triplet)	L1	L2-4
DiffPreampL	900	730	550
DiffPreampM	900	730	550
DiffPreampR	900	730	550
DiffPreampT	900	730	550
DiffPreampTL	900	730	550
DiffPreampTR	900	730	550
DiffVff	150	150	60

Table 17: Config differences depending on the layer

	Default(example L0)	LP Config
DiffPreComp	350	0
DiffPreampL	900	0
DiffPreampM	900	0
DiffPreampR	900	0
DiffPreampT	900	0
DiffPreampTL	900	0
DiffPreampTR	900	0
EnCoreCol0	65535	0
EnCoreCol1	65535	0
EnCoreCol2	65535	0
EnCoreCol3	65	0

Table 18: Default and LP config differences

	Default config	LP config
Normal powering	✓	x
LP enable	x	✓

Table 19: Configuration summary

A.3.2 Reading VMUX

Table 20 and Table 21 show the signals used for the voltage multiplexer (VMUX) and the current multiplexer (IMUX) (full Tables are given in Section B.12). In order to use any of the multiplexers, the register `MonitorEnable: 1` in the chip configuration has to be set. To select monitored values use `MonitorI` and `MonitorV`. To select IMUX, the setting 1 (I mux pad voltage) on the VMUX has to be set (`MonitorV: 1`) together with the chosen IMUX setting (`MonitorI: `).

Setting	Selected Input
0	Vref_ADC (GADC)
1	I_mux pad voltage
3	VCAL_DAC/2
4	VDDA/2 from capmeasure
7	VCAL_HI
8	VCAL_MED
30	Ana. GND
31	Vref_CORE
32	Vref_PRE
33	VINA/4
34	VDDA/2
35	VrefA
36	VOFS/4
37	VIND/4
38	VDDD/2
39	VrefD
63	high Z

Table 20: Voltage multiplexer (VMUX) assignments.

Setting	Selected Input
0	IREF main ref. current
10	Capmeasure circuit
11	Capmeasure parasitic
28	Ana. input current/21000
29	Ana. shunt current/26000
30	Dig. input current/21000
31	Dig. shunt current/26000
63	high Z

Table 21: Current multiplexer (IMUX) assignments.

A.3.2.1 Example VMUX measurement and analysis For all the VMUX measurements, first subtract the GNDA (VMUX=30) from the VMUX voltage, then apply the multiplicator (can be found in Table 27). To measure VDDA, one does the following:

- Set `MonitorV: 34`
- Measure the voltage from the VMUX pins on the data adapter card.
- Set `MonitorV: 30` (GNDA)
- Measure the voltage from the VMUX pins on the data adapter card.
- Subtract the GNDA
- Multiply the multiplicator 2

$$VDDA = (V(\texttt{MonitorV: 34}) - V(\texttt{MonitorV: 30})) \times 2 \quad (1)$$

A.3.2.2 Example IMUX measurement and analysis All IMUX measurements are performed with VMUX setting 1 (I mux pad voltage) and the current is calculated using the 10 kΩ resistor. For example to measure Analog input current (IinA), one does the following:

- Set `MonitorV: 1` and `MonitorI: 28` (Analog Input current - IinA)
- Measure the voltage from the VMUX pins on the data adapter card.
- Set `MonitorV: 1` and `MonitorI: 63` (GND)
- Measure the voltage from the VMUX pins on the data adapter card.
- Subtract the GND
- Convert to current using 10 kΩ [14]
- Multiply the multiplicator 21000

$$\text{IinA} = (\text{V}(\texttt{MonitorV: 1and MonitorI: 28}) - \text{V}(\texttt{MonitorV: 1and MonitorI: 63}))/10k\Omega \times 21000 \quad (2)$$

B Testing Procedure

B.1 First Power-up

After connecting the module into the setup, set the 2 V compliance (or higher to take into account the voltage drop across the power cables) on the LV power supply. Ideally, the output voltage on the LV power supply unit (PSU) should not be higher than 2.2 V including all voltage drops. Therefore, the power cables connecting the PSU and the power adapter card are recommended to be AWG 16 or better, with less than 14.7 Ω/m resistance to minimise the voltage drop. Set a constant current according to the type of the module, as given in Table 22. Do not use sense lines due to problems observed for some power supplies during RD53A testing [15]. Instead, measure Vin at the power adapter card with a multimeter as indicated in Fig. 1. The measured Vin of the module should agree with values given in Table 22. Also measure the resistance and the voltage drop across the power cables and crosscheck with the output voltage of the power supply.

type of module	RextA (Ω)	RextD (Ω)	I_{in}/module (A)	nominal Vin (V)
L0/triplets	511	407	5.55	$1.72\ ^{+0.038}_{-0.035}$
L1	732	549	6.6	$1.785\ ^{+0.038}_{-0.035}$
L2-L4	866	590	5.88	$1.758\ ^{+0.038}_{-0.035}$

Table 22: Nominal input current and voltage values for different types of modules, calculated from Table 1.

B.2 Sensor IV

Note that the bias voltages and leakage currents given here are absolute values. Both 3D as well as planar sensors use n-in-p technology and shall be reverse-biased with the positive potential at the n-electride and the negative potential at the p-electrode. A planar sensor has n-implants in a p-bulk. The n-implants are contacted via the FE pixels at their potential (close to 0 V) - "HV_return". While a negative voltage shall be applied to the p-bulk connected via wirebonds onto the module printed circuit board (PCB) - "HV".

B.2.1 Modules with 3D Sensors

For modules with 3D sensors [16], the leakage current shall be measured in steps of 1 V, with a maximum compliance of 100 µA. The settling time after each step shall be 2 s. Leakage current shall be measured up to 100 V or until the breakdown or the compliance is reached.

The breakdown voltage V_{bd} is defined as the bias voltage for which the leakage current ratio I_{leak}(V+10 V) / I_{leak}(V+5 V) < 2, with the exception of bias voltages between 0 and V_{depl}.

B.2.2 Modules with Planar Sensors

For modules with planar sensors [17], the leakage current shall be measured in steps of 5 V, with a maximum compliance of 100 µA. The settling time after each step shall be 2 s. The leakage current shall be measured up to 200 V or until the breakdown or the compliance is reached.

The breakdown voltage V_{bd} is defined as the minimum voltage value for which the leakage current increases by more than 20 % over a voltage step of 5 V, with the exception of bias voltages between 0 and V_{depl}.

B.3 ADC Calibration

ADC shall be calibrated as soon as the initial powering-up test is done. This way all voltages and currents can be measured via the VMUX output through the ADC. This can be done via a scan and the result checked against the wafer probing data.

The ITkPix chip has an internal ADC which can be used to readout the voltages on the monitoring multiplexer (MUX). For module QC we want to calibrate the ADC and compare with the calibration data from wafer probing.

For the ADC calibration, the automated procedure is the following:

On the power supply, set the voltage compliance of 2 V for the chip, however account for voltage drop over the power cables. Set the constant current according to the module type given in Table 22.

1. In the chip config, set for each chip
   `"MonitorEnable": 1,`
   `"MonitorV": 8,`
   `"InjVcalMed": 500,`
   `"InjVcalRange": 1,`
2. The register `"InjVcalMed":` shall be scanned through from 500 to 3500 in steps of 200.
3. For each step
   (a) Configure the chip with the above digital-to-analog converters (DACs)
   (b) Probe the voltage of `"InjVcalMed"` on the VMUX pad as described in Section A.3.2.1
   (c) Read the chip's register to extract the ADC count for `InjVcalMed`.
4. Measure GND by setting: `"MonitorV": 30`
5. Make a line equation with all the probed voltages as a function of ADC count.
6. Update the chip configuration with the new calibration offset and slope (both in mV):
   `"ADCcalPar": [<offset>, <slope>, <R_imux=10e3>],`

This procedure uses more data points than for the RD53A chip hence the uncertainty of this calibration should be better than 1–1.5 mV [18].

The chip configuration files shall be updated with this calibration in order to proceed with further measurements as the latter utilise this calibration.

The value of ANAGND30 is measured x times and its value (and standard deviation from it) are saved in the PDB so that it can be used in case subsequent tests use calibrated ADC.

B.4 Analog Readback

B.4.1 Voltage Measurements

Measure all VMUX and IMUX at nominal input current and voltage. Full tables of VMUX and IMUX settings are given in Sec. B.12. To enable monitoring `MonitorEnable: 1` in the chip configuration has to be set. To select monitored values use `MonitorI` and `MonitorV`. To select IMUX, setting 1 on the VMUX has to be used (`MonitorV: 1`) together with the chosen IMUX setting (`MonitorI: `). Measure the following quantities:

- VMUX: 0, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 17, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 63
- IMUX: 0, 1, 2, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 28, 29, 30, 31, 63

B.4.2 Temperature Measurements

Similarly, measure the temperatures using VMUX and IMUX:

- Measure NTC from VMUX (2) and GND (30)
- Measure NTC from IMUX (9) and GND (63)
- Measure temperature sensors VMUX (14, 16, 18)

It is necessary to set IMUX=63 when measuring NTC pad voltage through VMUX2.

RD53B has three pairs of active temperature and radiation transistor sensors and two resistance temperature sensors [19]. Two 12-bit registers (MON_SENS_SLDO and MON_SENS_ACB) are dedicated to the transistor sensor configuration which control the sensors on the SLDO regulators and chip bottom center, respectively.

- Enable by setting "MonSensSldoDigEn": 1
- Set the bias switch to "MonSensSldoDigSelBias": 0
- Cycle through dynamic element matching (DEM) bits by setting "MonSensSldoDigDem": [0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15]
- Enable by setting "MonSensSldoAnaEn": 1
- Set the bias switch to "MonSensSldoAnaSelBias": 0

- Cycle through DEM bits by setting "MonSensSldoAnaDem": [0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15]
- Enable by setting "MonSensAcbEn": 1
- Set the bias switch to "MonSensAcbSelBias": 1
- Cycle through DEM bits by setting "MonSensAcbDem": [0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15]

B.4.3 VDDA/D vs Trim

- Measure VDDA (VMUX 34) as a function of analog trim value: "SldoTrimA": [0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15]
- Measure VDDD (VMUX 38) as a function of analog trim value: "SldoTrimD": [0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15]

It is especially important to update the chip configuration files after the analysis of this test to proceed with the power measurements.

B.4.4 Ring Oscillators

B.5 SLDO Qualification

This measurement modifies nominal powering of the chips. At the beginning of the scan, check and record the module powering status (status of output, set current and voltage). Then scan the input current in the ranges documented in Table 23.

type of module	Nominal current [A]	Max current [A]	Step size [A]
L0/triplets	5.55	7.55	0.2
L1	6.6	8.0	0.2
L2-L4	5.88	7.48	0.2

Table 23: Current ranges for the VI scan.

Then measure VMUX33, VMUX37, VMUX34, VMUX38, VMUX36, VMUX32, VMUX30 (which is the analog ground), IMUX0, IMUX28, IMUX29, IMUX30, IMUX31 and IMUX63 (which is the GND reference for current measurements). The temperature of the external module NTC should be recorded during the measurements.

Note that the VMUX channels for all chips are merged on a single VMUX ouput, so make sure to set `MonitorV: 63` for all chips except the one being probed.

- Turn on power supply with a scanned input current, and voltage limit of the power supply set to 2 V (or higher to take into account the voltage drop across the power cable).
- Measure the temperature of the external NTC
- Set `MonitorV:` for the chip being tested. Set `MonitorV: VMUX63` for all other chips.

- Measure the voltage from the VMUX pins on the data adapter card.
- Set `MonitorV: 30`
- Measure the analog ground (GNDA) from the VMUX pins on the data adapter card (needed to obtain accurate VMUX measurements).
- Set `MonitorV: 1` and `MonitorI: 0 (for IMUX0, for example)`
- Measure the voltage from the VMUX pins on the data adapter card.
- Set `MonitorV: 1` and `MonitorI: 63`
- Measure GND reference for the current measurement from the VMUX pins on the data adapter card.
- After all the measurements, change the current to the next scanned input current and repeat.

At the end of this measurement, set the power supply back to the nominal power.

B.6 Vcal Calibration

Vcal DAC controls the injection circuits and thus has to be calibrated. This can be done via a scan by using the calibrated ADC.

The calibration injection circuit injects the differential charge between two DACs, Vcal_Med and Vcal_Hi. The circuit also has two ranges: a high dynamic range and one with half the voltage range and slope but a finer step size. The high dynamic range with `"InjVcalRange": 1,` is the default range that will be used for the chip in module QC. We do the calibration using the calibrated ADC circuit and compare the results with wafer probing. In total, 4 sets of measurements are taken: Vcal_Med, Vcal_Hi each in large and small range.

On the power supply, set the voltage compliance of 2 V for the chip, and account for voltage drop over the power cables as explained in Section B.1. Set the constant current according to the module type given in Table 22.

1. Enable and set the monitoring output and set the voltage range
   `"MonitorEnable": 1,`
   `"MonitorV": 8(7),` for Vcal_Med(Vcal_Hi)
   `"InjVcalRange": 1(0),` for large(small) range,
2. Go through the Vcal_Med(_Hi) in large and small voltage range from 100 to 4000 in increments of 100
3. For each Vcal step set `"InjVcalMed(High)": <step>,` and read through the ADC the converted voltage
4. At the end of the measurement make a line fit with these voltage vs DAC points and determine the offset and slope. Vcal_Med and Vcal_Hi should be identical in each voltage range.
5. Update the chip config with the offset and slope of the large range
   `"VcalPar": [<offset>, <slope>],`

It's important to update the chip configuration files with the result of this test as this calibration is relevant for chip tuning.

B.7 Injection Capacitance

The capacitance in the injection circuit of the FE chip determines the amount of charge injected into the pixel during tuning and thus should be precisely measured. See Ref. [19] Section 13.8 and Ref. [20].

$$C_{\text{pix}} = (C_{\text{meas}} - C_{\text{par}})/100 - \Delta C$$

with

- $C_{\text{meas}} = |\frac{I_{\text{capmeas}}}{10\,\text{MHz}\cdot(\text{VDDA}_{\text{capmeas}} - V_{\text{IMUX(10)}})}|$
- $C_{\text{par}} = |\frac{I_{\text{cappar}}}{10\,\text{MHz}\cdot(\text{VDDA}_{\text{capmeas}} - V_{\text{IMUX(11)}})}|$
  - I_{capmeas} from IMUX(10)
  - I_{cappar} from IMUX(11)
  - $\text{VDDA}_{\text{capmeas}}$ from VMUX(4): VDDA/2 from capmeasure
- $\Delta C = 0.48\,\text{fF}$ obtained from layout extraction.

The measurements of C_{meas} and C_{par} are made separately. The capmeasure circuit should be reset before making a measurement. This is achieved by selecting capmeasure in the global pulse routing and issuing a global pulse with a 3 clock width (this is longer than the default width of 1 clock).

For C_{meas} (C_{par}), first enable the clock by setting `CapMeasEn = 1 (CapMeasEnPar = 1)` and selecting the IMUX channel `Mon_injcap (Mon_injcap_par)`. One must wait at least 0.5 ms for the output to settle (with the nominal 5 K and 22 nF external components). At this point the voltage at the Imux_Pad can be measured either with an external instrument or the GADC.

Average measured values over 5 repetitions.

Note that it is important to use VMUX(4) for "VDDA/2 from capmeasure". Also take into consideration the additional voltage drop of VDDA over R_{IMUX} for the C_{meas} and C_{par}, respectively, as shown in Ref. [19] Figure 79. Hence the terms $\text{VDDA}_{\text{capmeas}} - V_{\text{IMUX(10)}}$ and $\text{VDDA}_{\text{capmeas}} - V_{\text{IMUX(11)}}$ [20].

From wafer probing, the voltage is obtained through the needle card as VDDA − GNDA_REF (not through MUX).

After the analysis of this measurement, the chip configuration files shall be updated because the result is relevant for chip tuning.

B.8 Low power (LP) Mode

This test deviates from the nominal power. Thus at the beginning of this test, check and record the module power status (status of output, set current and voltage). Switch off the power, set the PSU to the nominal LP power according to Table 6.

The procedure for testing LP Mode is as follows:

- Inject an AC signal that is provided directly by the DAQ.

- Power the module with the LP nominal current, given in Table 6. Register the value of the input voltage from the PS.
- The chips are configured using the LP config (see Appendix A.3.1).
- Measure VinA (VMUX33), VinD (VMUX37), Vofs (VMUX36), IinA (IMUX28), IinD (IMUX30), IshuntA (IMUX29) and IshuntD (IMUX31) (as well as VMUX30 and IMUX63) and they should be compared to values given in Table 6 and Table 7.
- Run a digital scan using a LP config and check that the output is meaningful. Register the value of the input voltage from the PS.

At the end of the test set the module back to the nominal power.

B.9 Over-voltage protection (OVP) (Removed from testing procedure)

This test is performed in LP mode. At the beginning of the measurement make sure to check and record the module powering status (output, set current and voltage). Power off the module and power it back up with the nominal LP values as described in Table 6.
The procedure for testing OVP is as follows:

- OVP testing is performed in LP mode using current given in Table 9.
- Measure VrefOVP (VrefPRE, VMUX32) (also VMUX30) and compare the values to Table 8
- Measure IinA (IMUX28) and IinD (IMUX30) (also IMUX63) and compare to Iin/4 (from PS).

At the end of the test supply the module back with the nominal normal power settings.

B.10 Undershunt Protection (Removed from testing procedure)

This test is performed in LP mode. The module is started up with a configuration consuming minimal power. The appropriate input currents are given in Table 24. Analog and digital USP are tested separately from another.

type of module	Iin [A]
L0/triplets	1.63
L1	2.1
L2-L4	2.1

Table 24: Input currents for USP test.

Once at the testing input current, all default voltages VrefD/A, VIND/A, VDDD/A and currents IIND/A, IshuntD/A should get measured on all chips. Afterwards the configuration of one chip is modified to consume more power then it is provided. The register settings are listed in Table 25.

register	low consumption	analog test	digital test
DiffPreampL	0	900	0
DiffPreampR	0	900	0
DiffPreampTL	0	900	0
DiffPreampTR	0	900	0
DiffPreampT	0	900	0
DiffPreampM	0	900	0
EnCoreCol_0	0	0	0xff

Table 25: Input current and expected values of internal currents.

The corresponding Vref should drop and compensate with a reduced power need. With the procedure described above, the MUX should still be configurable even after USP is triggered. If this is not the case, then in order to read all voltages in USP mode, the input current has to be raised between each measurement while re-configuring the MUX. Even after raising the input current the chip might not exit the USP unaffected and even can influence communication with the whole module. Thus, a chip reset has to be performed after logging all internal voltages.

This procedure has to be repeated for each individual chip with both tests.

B.11 Pixel Performance

B.11.1 Minimum Health Test

- Digital Scan
- Analog Scan
- Threshold Scan (high range, use std_thresholscan_hr.json)
- ToT scan, 6000e injection charge

B.11.2 Tuning performance

Please note that ToT scans or tunings are not available for ITkPixV1.1.

- Tuning:
  - Global threshold tune @1200e (L0) or @1700e (L1/L2)
  - ToT tune 7bc @ 6000e
  - Global threshold tune @1200e (L0) or @1700e (L1/L2)
  - Pixel threshold tune @1000e (L0) or @1500e (L1/L2)
  - Injection delay tuning (not ready)
- Post-tuning:
  - Threshold Scan (high def, use std_thresholdscan_hd.json)
  - In-time threshold measurement
  - ToT scan, 6000e injection charge

B.11.3 Pixel Failure Test

B.11.3.1 Electrical Pixel Failure Test

- Digital Scan with clear mask (supply '-m 1' option)
- Analog Scan
- Threshold Scan (high def, use std_thresholdscan_hd.json)
- Noise Scan (10M trigger)
- ToT Memory Scan (Release 3: not ready)

B.11.3.2 Full Pixel Failure Test

- Disconnected bump scan
- Merged bump scan with 1500e (2000e) injected charge for chip tuned at 1000e (1500e)
- Threshold scan with no bias (removed from the testing procedure)
  - Turn off HV
  - Pixel threshold re-tune to 1000e (L0) or 1500e (L1/L2)
  - Zero-bias threshold scan
  - Turn on HV
  - Revert chip configs to state before re-tuning[1].
- Source scan
  - Obtain at least 10 hits on connected pixels (setup dependent)

Prior to running the source scan, make sure to have a working pixel mask. This can be achieved by running the following scans first:

1. Digital scan with clear mask (supply '-m 1' option)
2. Analog scan
3. Noise scan

or by running the source scan immediately after the electrical pixel failure test scans (for which the above scans are included). During the noise scan, the module should not be exposed to the source.

B.12 VMUX complete table

Table 26 and Table 27 show the available signals for IMUX and VMUX.

[1] In YARR, the pixel threshold re-tuning will store the original chip configs in the retuning output directory. Use the `./bin/revert-chip-configs` script in YARR to revert to these chip configs.

Setting	Selected Input	Setting	Selected Input	Setting	Selected Input
0	IREF main ref. current	11	Capmeasure parasitic	22	DIFF FE Preamp Top-Left
1	CDR VCO main bias	12	DIFF FE Preamp Main array	23	DIFF FE VTH1 Right
2	CDR VCO buffer bias	13	DIFF FE PreComp	24	DIFF FE Preamp Top
3	CDR CP current	14	DIFF FE Comparator	25	DIFF FE Preamp Top-Right
4	CDR FD current	15	DIFF FE VTH2	26	not used
5	CDR buffer bias	16	DIFF FE VTH1 Main array	27	not used
6	CML driver tab 2 bias	17	DIFF FE LCC	28	Ana. input current/21000
7	CML driver tab 1 bias	18	DIFF FE Feedback	29	Ana. shunt current/26000
8	CML driver main bias	19	DIFF FE Preamp Left	30	Dig. input current/21000
9	NTC_pad current	20	DIFF FE VTH1 Left	31	Dig. shunt current/26000
10	Capmeasure circuit	21	DIFF FE Preamp Right	32-62	not used
				63	high Z

Table 26: Current multiplexer (IMUX) assignments.

Setting	Selected Input	Setting	Selected Input	Setting	Selected Input
0	Vref_ADC (GADC)	10	DIFF FE VTH1 Main array	31	Vref_CORE
1	I_mux pad voltage	11	DIFF FE VTH1 Left	32	Vref_PRE
2	NTC_pad voltage	12	DIFF FE VTH1 Right	33	VINA/4
3	VCAL_DAC/2	13	RADSENS Ana. SLDO	34	VDDA/2
4	VDDA/2 from capmeasure	14	TEMPSENS Ana. SLDO	35	VrefA
5	Poly TEMPSENS top	15	RADSENS Dig. SLDO	36	VOFS/4
6	Poly TEMPSENS bottom	16	TEMPSENS Dig. SLDO	37	VIND/4
7	VCAL_HI	17	RADSENS center	38	VDDD/2
8	VCAL_MED	18	TEMPSENS center	39	VrefD
9	DIFF FE VTH2	19–30	Ana. GND	40-62	not used
				63	high Z

Table 27: Voltage multiplexer (VMUX) assignments.

C Device Specifications

C.1 PSU

Brand	Requirements	Rohde&Schwarz (Hameg)	Rigol		TDK-Lambda	Wiener
Model		HMP4040	DP821A			MPOD MPV8008
No. of channels		4	2		1	8
Channel			1	2		all
Delivered voltage	2 V	32 V	60 V	8 V	20 V	8 V
Delivered current	8 A	10 A	1 A	10 A	76 A	10 A
Constant current mode	yes	yes	yes		yes	yes
Set voltage accuracy	0.5%	<0.05% + 5 mV	0.1%+25 mV	0.05%+10 mV	0.05%+20 mV	0.1%
Set current accuracy	0.5%	<0.1% + 5 mA	0.2%+10 mA	0.2%+10 mA	0.1%+150 mA	0.5%
Set voltage limit	yes	yes	yes		yes	yes
Set current limit		yes	yes		yes	yes
Measured voltage resolution	0.01 V	1 mV	1 mV to 66 V	1 mV to 8.8 V	2.4 mV	0.5 mV%
Measured voltage accuracy	0.5%	<0.05% + 5 mV	<0.01%+2 mV		0.1%+40 mV	0.1% of full scale
Measured current resolution	1 mA	<1 A: 0.2 mA; ≥1 A: 1 mA	0.1 mA to 1.1 A	1 mA to 11 A	9 mA	0.5 mA
Measured current accuracy	0.5%	0.1% + 2 mA	<0.01%+250 µA		0.1%+300 mA	0.5% of full scale
Ramp-up speed	<10 ms (≥800 A/s)	<5 ms (>2 kA/s)	<110 ms	<15 ms	prog: 80 ms	-
Ramp-down speed			<800 ms	<15 ms	prog: 50 ms	-
Programmable ramp			yes: max, min, points, interval, symmetry, inverted		no	yes
Ripple for $f \leq$=20 MHz	<20 mVpp	<1.5 mV rms, <1 mA rms	<350 µVrms/2 mVpp, <2 mArms		8 mV rms (<1 MHz); 60 mV p-p (<20 MHz); 150 mA (<1 MHz)	<3 mV (pp), 0.5 mV (rms)
Ripple for $f >$20 MHz	<1 mVpp					<5 mV p-p; 0.5 mV rms (<100 MHz)
Remote control interface	GPIB/RS232/ Ethernet/USB					TBD
Multi-channel ground	individual	individual				TBD
Price estimate (CHF)	floating	floating	788			3000 (module only, controller and crate needed)
Price/module (CHF)	1800	455				
Can be used for		RD53A, ITkPixV1	RD53A, ITkPixV1		RD53A, ITkPixV1	RD53A, ITkPixV1

Table 28: LV PSU models.

Brand	Requirements		TTi				
Model		CPX400S(P)[2]	QL335(T)P		PL303QMD(-P)	PL303QMT(-P)	QPX1200
No. of channels		1	1		2	3	1
Channel			Range 1	Range 2	1, 2 | 1+2 (parallel)	3	
Delivered voltage	2 V	$0-60$ V	35 V	15 V	30 V		60 V
Delivered current	8 A	$20-7$ A	3 A	5 A	3 A | 6 A	8 A	50 A
Constant current mode	yes	yes	yes		yes		yes
Set voltage accuracy	0.5%	10 mV	0.03%+5 mV		10 mV		0.1%+2 mV
Set current accuracy	0.5%	10 mA	0.2%+5 mA	0.2%+0.5 mA	3 mA		0.3%+20 mA
Set voltage limit	yes	yes	yes		yes		yes
Set current limit		yes	yes		yes		yes
Measured voltage resolution	0.01 V	10 mV	1 mV (CV) or 10 mV (CI)		10 mV		1 mV
Measured voltage accuracy	0.5%	0.1%+2digit	0.1%+10 mV		0.1%+10 mV		0.1%+2 digits
Measured current resolution	1 mA	10 mA	1 mA		1 mA		10 mA
Measured current accuracy	0.5%	0.3%+20 mA	0.2%+5 mA		0.3%+3 mA		0.3%+2 digits
Ramp-up speed	<10 ms (≥800 A/s)		20 ms	6 ms	switch: <15 ms, progr.: 45 ms		
Ramp-down speed			25 ms	6 ms	switch: unknown, progr.: 6..20 ms		
Programmable ramp			no		no		no
Ripple for f≤=20 MHz	<20 mVpp	<3 mV rms, <15 mV pk-pk, (5 mV rms max.)	<0.35 mV rms, <0.2 mA rms		<0.4 mV rms, 2 mV p-p, <0.2 mA rms		<3 mV rms, <20 mV pk-pk
Ripple for f>20 MHz	<1 mVpp						
Remote control interface	GPIB/RS232/ Ethernet/USB	(GPIB/RS232/ Ethernet/USB)	GPIB/RS232/ Ethernet/USB		(GPIB/RS232/Ethernet/USB)		
Multi-channel ground	individual floating						
Price estimate (CHF)		805					1400
Price/module (CHF)							1400
Can be used for		RD53A		RD53A	RD53A	RD53A	

Table 29: LV PSU models by TTi.

Note: It has been observed that this model has active voltage spikes when remote sensing is used, despite output being off! See [15].

692

Brand	Requirements	Agilent/Keysight							
Model		E3631A			E3634A		E3648A		
No. of channels		3			1		2		
Channel		1	2	3	Range 1	Range 2	1	2	
Delivered voltage	2 V	6 V	25 V	−25 V	25 V	50 V	8 V	20 V	
Delivered current	8 A	5 A		1 A	7 A	4 A	5 A	2.5 A	
Constant current mode	yes		yes			yes		yes	
Set voltage precision	0.01 V					0.05%+10 mV		0.01%+3 mV	
Set current precision	1 mA	0.2%+10 mA	0.15%+4 mA			0.2%+10 mA		0.01%+0.250 mA	
Set voltage limit	yes		yes			yes		yes	
Set current limit	yes		yes			yes		yes	
Measured voltage resolution	0.01 V	1 mV		10 mV		3 mV		10 mV	
Measured voltage precision	0.01 V	0.1%+5 mV	0.05%+10 mV		0.05%+5 mV		0.05%+5 mV	0.1%+25 mV	
Measured current resolution	1 mA	1 mA			0.5 mA		1 mA		
Measured current precision	1 mA	0.2%+10 mA	0.15%+4 mA		0.15%+5 mA		0.15%+5 mA	0.15%+10 mA	
Ramp-up speed	<10 ms (≥800 A/s)	11 ms	50 ms		80 ms		90 ms		
Ramp-down speed		13 ms	45 ms		30 ms		90 ms		
Programmable ramp		no			no		no		
Ripple for f≤=20 MHz	<20 mVpp	<0.35 mVrms, <2 mVpp			<0.5 mVrms/3 mVpp (CV), <2 mArms (CI)		<5 mVpp/0.5 mVrms (CV), <4 mArms (CI)		
Ripple for f>20 MHz	<1 mVpp								
Remote control interface	GPIB/RS232/ Ethernet/USB	GPIB/RS232			GPIB/RS232		GPIB/RS232		
Multi-channel ground	individual floating								
Price estimate (CHF)									
Price/module (CHF)									
Can be used for		RD53A			RD53A		RD53A		

Table 30: More LV PSU models (mainly Agilent/Keysight).

693

Brand	Requirements	CAEN[3]	ISEG		Keithley
Model		DT1415ET	SHQ 122M	SHQ 224M	2410
No. of channels		8	1	2	1
Channel					
Delivered voltage	200 V	1 kV	2 kV	4 kV	1.1 kV@21 mA
Delivered current	1 mA	1 mA	6 mA	3 mA	1.05 A@21 V
Constant voltage mode	yes	yes	yes		yes
Set voltage accuracy	(0.5%)	20 mV	30 mV	60 mV	5 µV@200 mV
Set current accuracy	(0.5%)	20 nA			50 pA@1 µA
Set voltage limit		yes			yes
Set current limit	yes	yes			yes
Measured voltage resolution	0.1 V	20 mV	100 mV		1 µV@200 mV
Measured voltage accuracy	(0.5%)	0.2%+0.2 V+50 ppm/°C	0.05%Vout+0.02%Vnom		0.012%+300 µV
Measured current resolution	5 nA	0.1 nA@high res, 1 nA@high power	1 nA@1 µA		10 pA@1 µA
Measured current accuracy	0.02%	0.5%+5 nA+50 ppm/°C (10–100% full scale CV), 2%+5 nA+50 ppm/°C (10% full scale CV)	0.1%Iout+20 nA		0.029%+300 pA
Programmable ramp	1–50 V/s	1–100 V/s, 1 V/s step	2–255 V/s remote control		
Over/under-voltage trip reaction time	10–1000 ms				
Over-current trip reaction time	10 ms	programmable in 0.1 s steps			
Ripple for f≤=20 MHz	<20 mVpp	differential mode <5 mV; max 10 mV, common mode <10 mV; max 15 mV	<2 mV typ, 5 mV max		
Ripple for f>20 MHz	<1 mVpp				
Remote control interface	GPIB/RS232/ Ethernet/USB	yes			
(Emergency ramp down)	100–400 V/s				
(Off-mode)	high-ohmic (3D), low-ohmic <10 Ω (planar)	low-ohmic			adjustable
Multi-channel ground	individual floating	individual floating		common floating (0–47 V), common ground (>47 V)	
Price estimate (CHF)		6400			
Price/module (CHF)		800			
Can be used for		RD53A, ITkPixV1, SP	RD53A		RD53A, ITkPixV1

Table 31: HV PSU models. Requirement items in brackets are only necessary if the same PSU would also be used for serial powering tests.

Note: CAEN PSUs are often less sensitive than given in the specs.

List of Acronyms

ADC analog-to-digital converter

AWG American wire gauge

DAC digital-to-analog converter

DAQ data acquisition

FE front-end

FW firmware

HV high voltage

ITk Inner Tracker

IV sensor leakage current as a function of the bias voltage

LP low power

lpGBT Low Power GigaBit Transceiver

LSB least significant bit

LV low voltage

MOS metal-oxide-semiconductor

MUX multiplexer

NTC negative temperature coefficient

OVP over-voltage protection

USP under-shunt protection

PCB printed circuit board

PSU power supply unit

PS power supply

QC quality control

SLDO Shunt Low Drop Out regulator

SMD surface-mount device

ToT time-over-threshold

VI input voltage Vin as a function of the input current Iin for SLDO

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