

Figure 1: Ultra-Lightweight Quantum-Safe IoT Protocol Stack - System Architecture

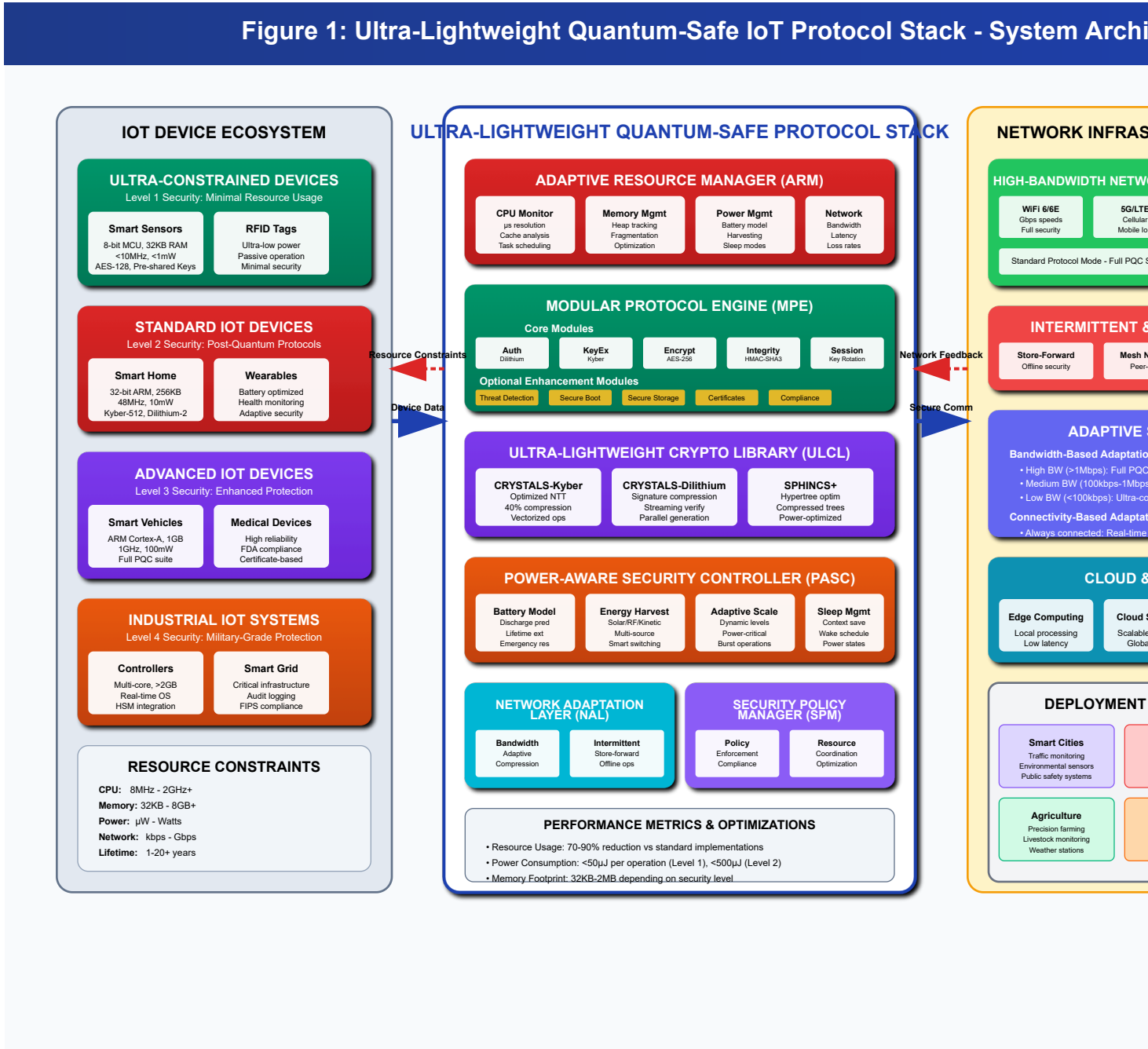


Figure 2: Adaptive Resource Management Engine - Real-Time Optimization Flow

This page contains the following errors:

error on line 696 at column 15: xmlParseEntityRef: no name

Below is a rendering of the page up to the first error.

Figure 2: Adaptive Resource Management Engine - Real-Time Optimization Flow

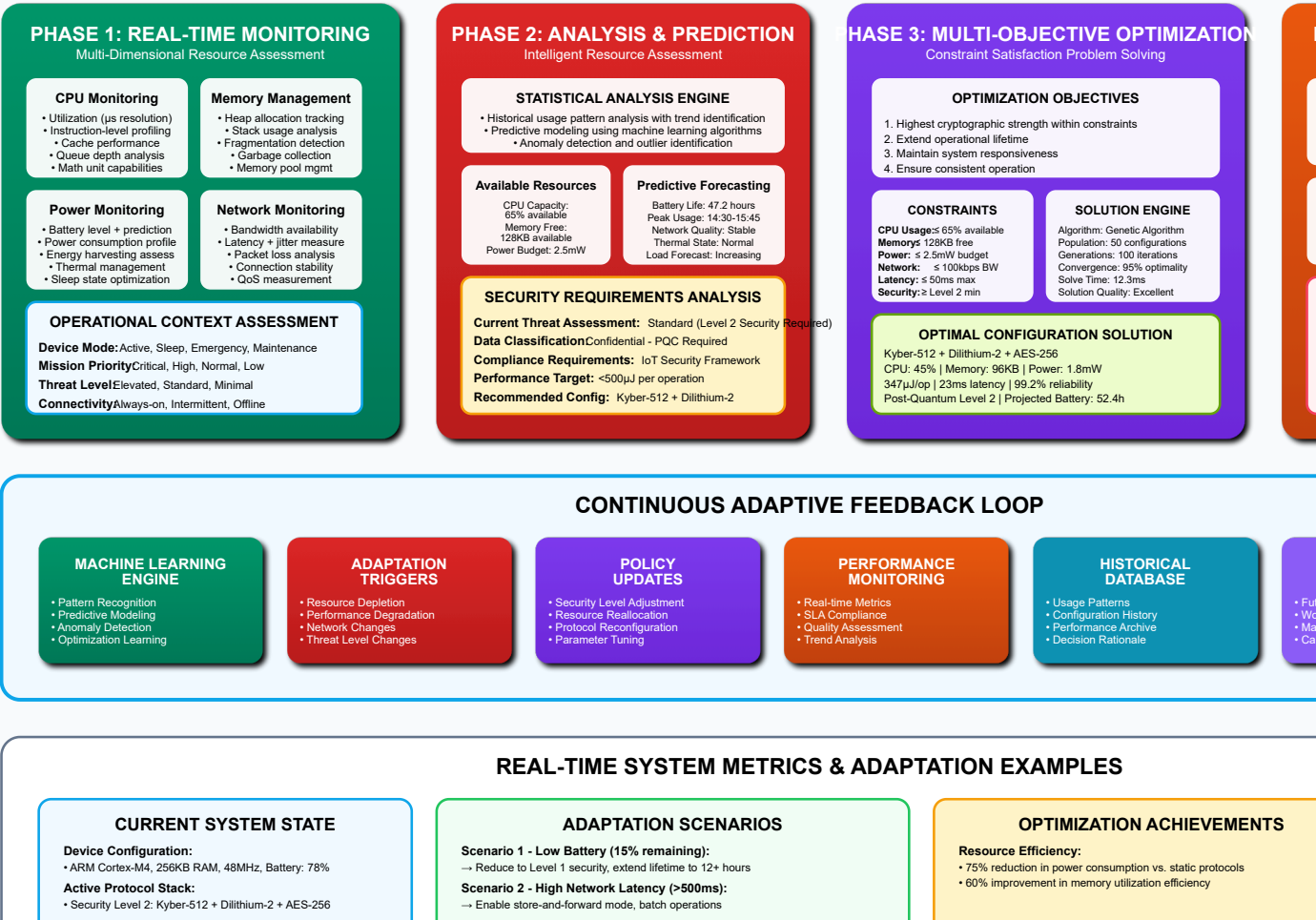
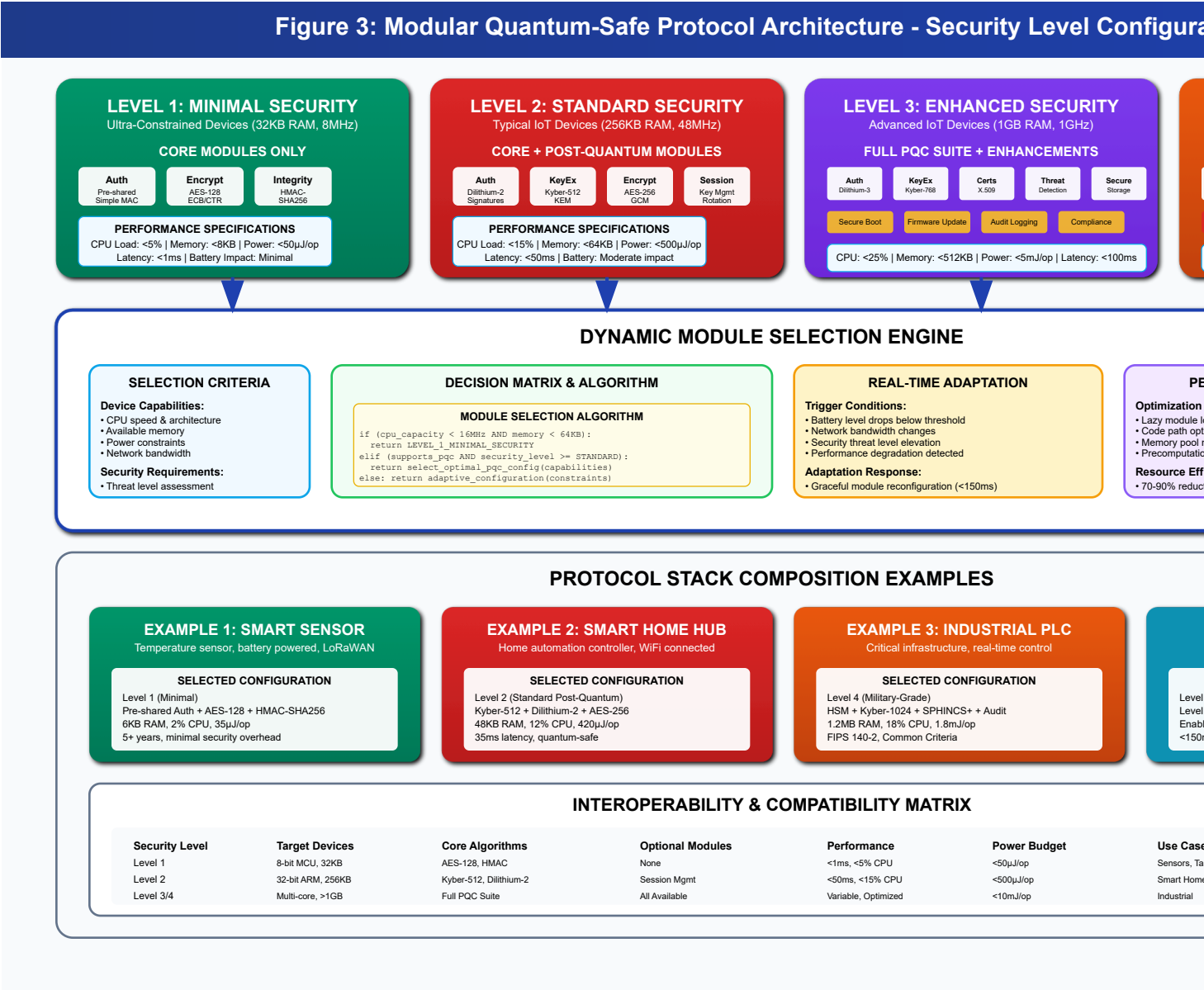


Figure 3: Modular Quantum-Safe Protocol Architecture - Security Level Configurations



DYNAMIC MODULE SELECTION ENGINE

SELECTION CRITERIA

Device Capabilities:

CPU speed & architecture

Available memory

Power constraints

Network bandwidth

Security Requirements:

Threat level assessment

DECISION MATRIX & ALGORITHM

MODULE SELECTION ALGORITHM

if (cpu\_capacity < 16MHz AND memory < 64KB):

return LEVEL\_1\_MINIMAL\_SECURITY

elif (supports\_pqc AND security\_level >= STANDARD):

return select\_optimal\_pqc\_config(capabilities)

else: return adaptive\_configuration(constraints)

REAL-TIME ADAPTATION

Trigger Conditions:

Battery level drops below threshold

Network bandwidth changes

Security threat level elevation

Performance degradation detected

Adaptation Response:

Graceful module reconfiguration (<150ms)

PE

Optimization

Lazy module l

Code path opt

Memory pool r

Precomputatio

Resource Eff

70-90% reduc

PROTOCOL STACK COMPOSITION EXAMPLES

EXAMPLE 1: SMART SENSOR

Temperature sensor, battery powered, LoRaWAN

SELECTED CONFIGURATION

Level 1 (Minimal)

Pre-shared Auth + AES-128 + HMAC-SHA256

6KB RAM, 2% CPU, 35µJ/op

5+ years, minimal security overhead

EXAMPLE 2: SMART HOME HUB

Home automation controller, WiFi connected

SELECTED CONFIGURATION

Level 2 (Standard Post-Quantum)

Kyber-512 + Dilithium-2 + AES-256

48KB RAM, 12% CPU, 420µJ/op

35ms latency, quantum-safe

EXAMPLE 3: INDUSTRIAL PLC

Critical infrastructure, real-time control

SELECTED CONFIGURATION

Level 4 (Military-Grade)

HSM + Kyber-1024 + SPHINCS+ + Audit

1.2MB RAM, 18% CPU, 1.8mJ/op

FIPS 140-2, Common Criteria

Level

Level

Enabl

<150r

INTEROPERABILITY & COMPATIBILITY MATRIX

Security Level	Target Devices	Core Algorithms	Optional Modules	Performance	Power Budget	Use Case
Level 1	8-bit MCU, 32KB	AES-128, HMAC	None	<1ms, <5% CPU	<50µJ/op	Sensors, Ta
Level 2	32-bit ARM, 256KB	Kyber-512, Dilithium-2	Session Mgmt	<50ms, <15% CPU	<500µJ/op	Smart Home
Level 3/4	Multi-core, >1GB	Full PQC Suite	All Available	Variable, Optimized	<10mJ/op	Industrial