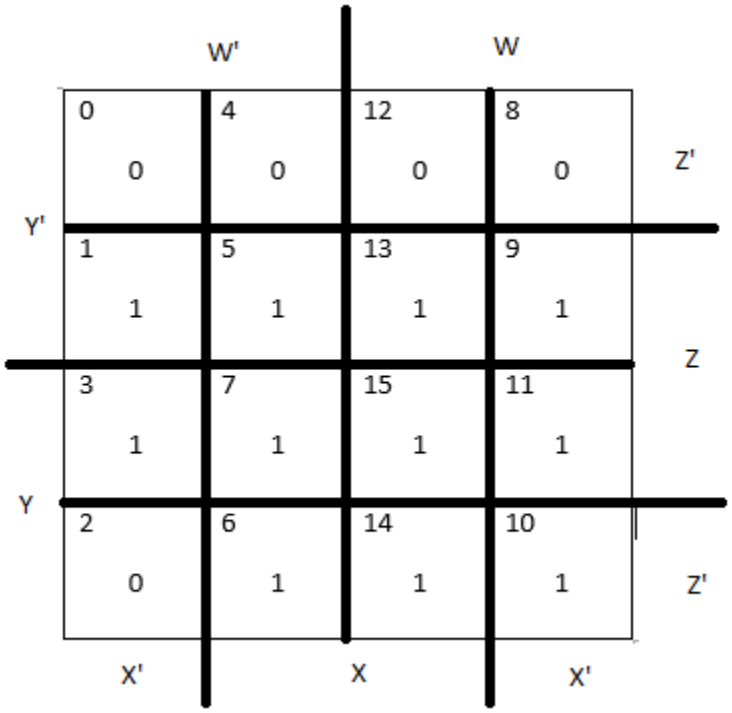
‘WXYZ’ Sensor Configuration	Event
0000	0
0001	1
0010	0
0011	1
0100	0
0101	1
0110	1
0111	1
1000	0
1001	1
1010	1
1011	1
1100	0
1101	1
1110	1
1111	1

7.1 Digital Design Refresher (Postlab)

Karnaugh Map with SoP expression of 2-level logic ciruit

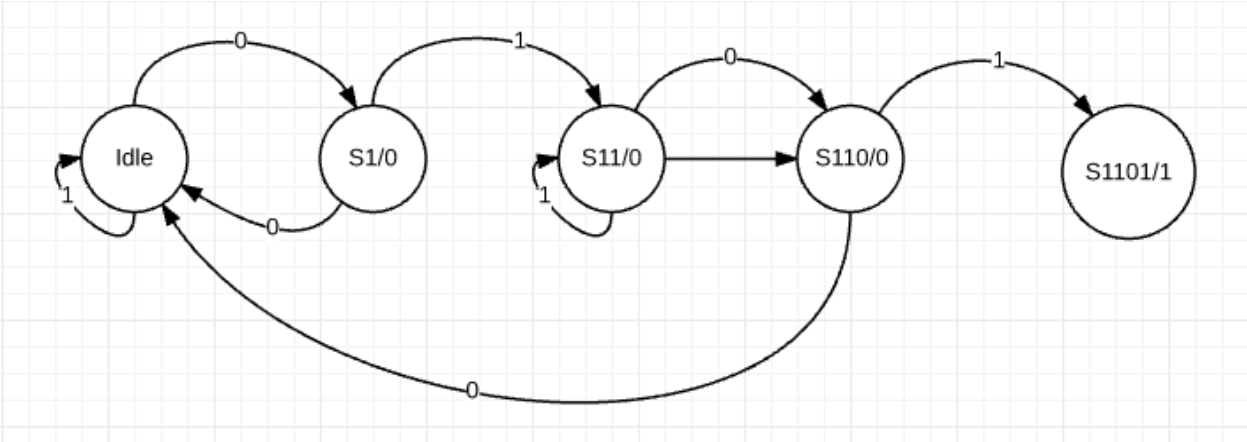


F(W,X,Y,Z) = Z + YW + YX

= Z + Y(W + X)

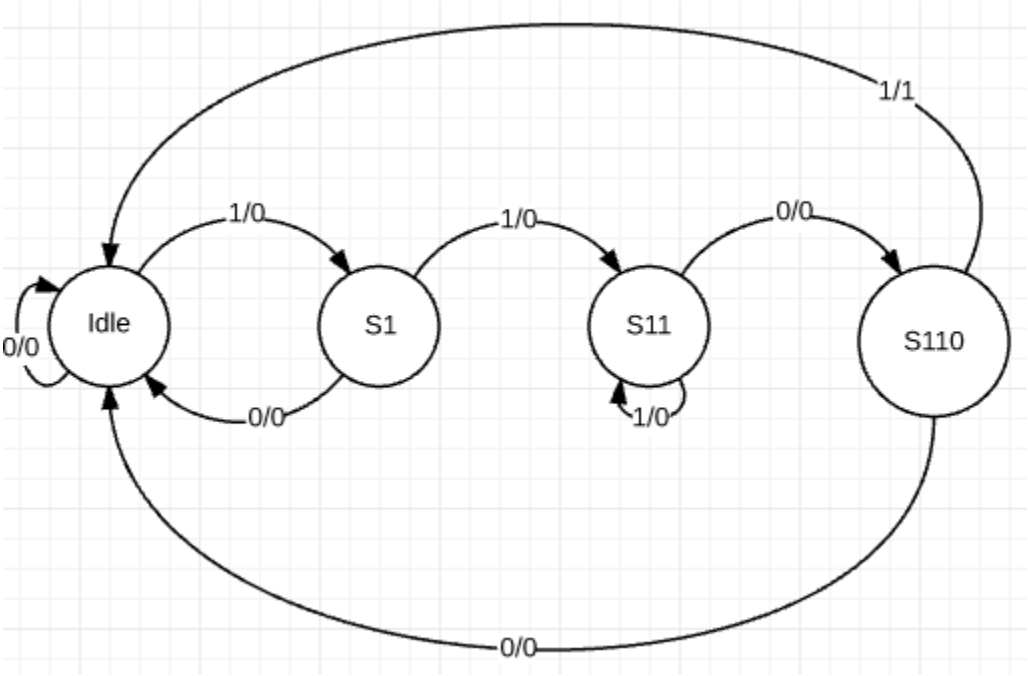
7.2

Moore Model State Transition Diagram



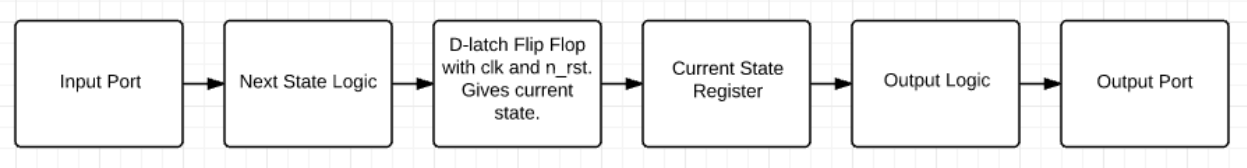
***Note:** There are two “0” inputs for the state transition from “Idle” state to “S1” state. The top “0” input should be a “1” input instead. Also, the arrow without an input from S11 to S110 should be omitted entirely.

Mealy Model State Transition Diagram

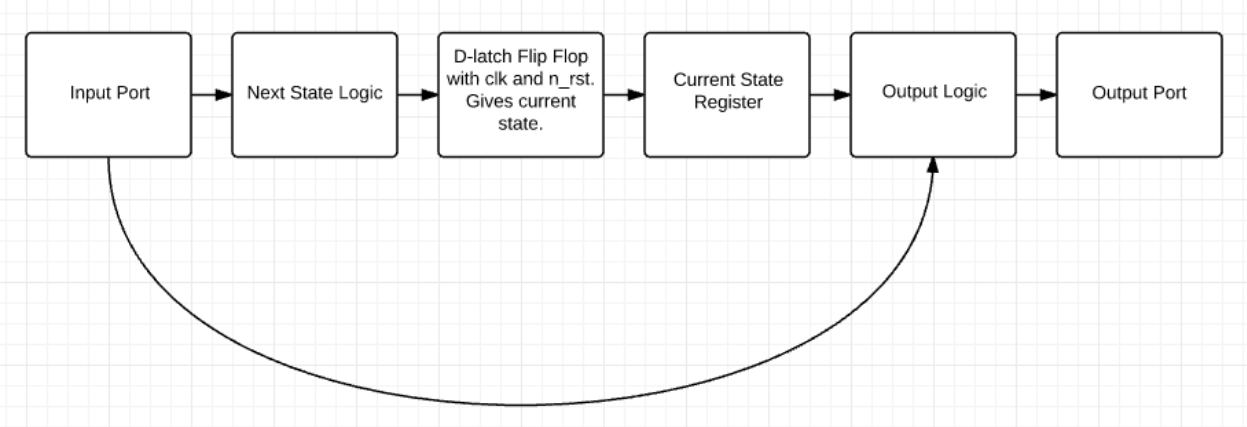


Mealy model requires fewer states because upon completion, it loops back to idle state instead of going to an extra “completion” state (as the Moore model does).

Moore RTL diagram

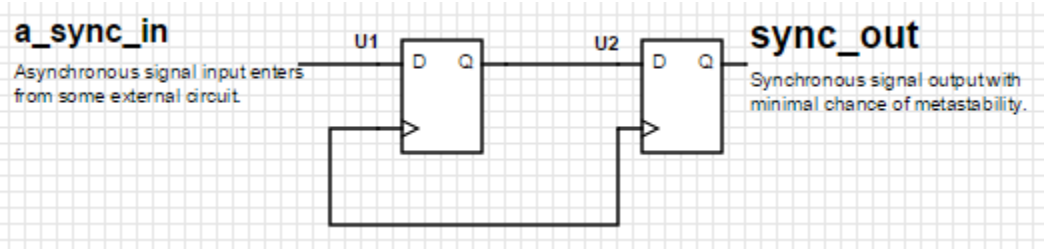


Mealy RTL diagram



7.3.1 Synchronizer

Schematic for 2 FF Synchronizer



A 2 Flip-Flop (FF) synchronizer. A signal may change its state while the first FF is capturing data or during the setup or hold time. The second FF is connected in series to the first FF. Possibility of metastable output is greatly reduced.

Both FF's are clocked by the same system/bus clock. The input to FF U2 is the output of FF U1.

7.3.2 MSB SIPO Shift Register

Schematic for MSB Serial-to-Parallel Shift-Register