Ain Shams University
Faculty of Engineering
ASU-ICHEP - COMM
CSE212: Computer Organization

Course Project (Major Task)

Spring2022

Aim

The aim of this project is to design and simulate a single-cycle and pipelined MIPS processor.

The project includes the architecture form, where the students will focus on developing a tailored architecture to perform a specific function.

Task

Using Verilog, **design and simulate** a simple version of a ***single-cycle*** *and* ***pipelined MIPS processor*** that supports the memory-refrence (`lw, sw`), arithmetic and logic (`add, addi, sub, and, or, slt`), and jumping and branching instructions (`j, beq`); where the format of each instruction is as follows:

	6-bits	5-bits	5-bits	5-bits	5-bits	6-bits
`I-type`	op	rs	rt	immediate		
`J-type`	op	---	address			
`R-type`	op	rs	rt	rd	---	func

The control unit should issue control signals that are needed to execute the fetched instruction; the set of control signals vary from one instruction to another.

Some Design Details/Notes/Constraints

- The length of the clock cycle will always be determined by the slowest operation.
- Each clock cycle, fetch the instruction from the address specified by the program counter, and increments it by 4.
- To ease the design of your control unit, build a table of the signals' values first.
- Simulation and testing:
    - For the single-cycle processor, you need to check all ten instructions implemented in your design give the expected results.
    - For the pipelined processor, you need to check that your pipelined processor can realize the basic functions as in single-cycle processor. In addition, check the data and control hazards since there are cases

with control flow and data dependences. Different cases concerning the data and control hazards will be given throughout the course.

Deliverables:

1. ***Verilog codes*** for each component and the whole project.
2. ***Modelsim simulation files and results.***
3. ***Presentation***, should contain, at least, the following for each processor:
   - **a.** A title slide with your name, your partners' name, and the date.
   - **b.** Acknowledgments, if any.
   - **c.** Table of Contents.
   - **d.** One-slide introduction.
   - **e.** Detailed design steps.
   - **f.** Detailed block diagram of your design.
   - **g.** Simulation and testing strategy.
   - **h.** Screenshot of the simulation results for each block and the overall system.
   - **i.** Conclusions
   - **j.** References in IEEE citation format.

Marks Distribution:

- Coding: **20%** (Can your Verilog code demonstrate all functionalities and components?)
- Viva: **25%** (Do you understand properly what you have done?)
- Design presentation: **20%** (Can you complete all the steps of your design eg: individual blocks, internal connectivity, simplification, integration, etc.)
- Testing strategy, simulations, and code coverage: **30%** (all the required blocks(s))
- Unique/interesting: **5%** (Is this something uncommon?)

- ***You will work in a team of* 3 *students.***
