

# **Signal Converter DMS Projekt**

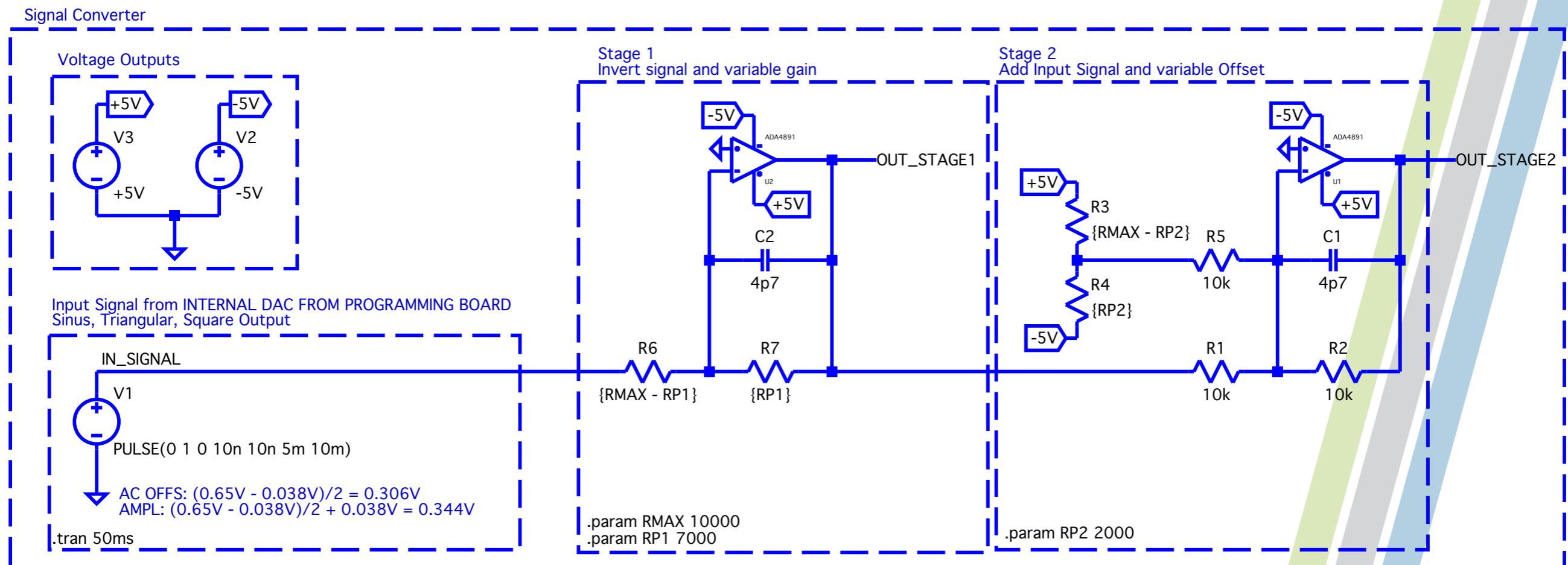
Dichler Sebastian & Egermann Werner

# Inhalt

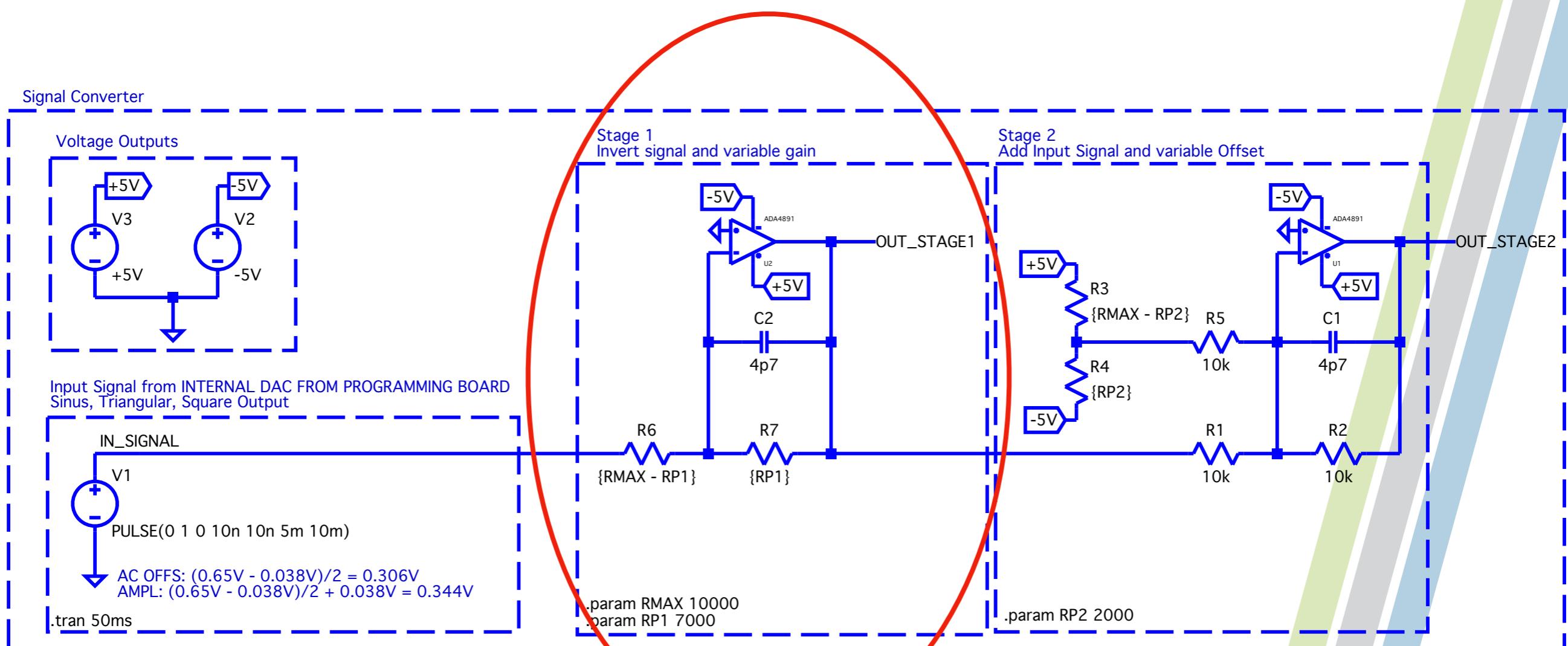
- **Hardware**
  - ▶ Simulation
  - ▶ Stückliste
  - ▶ Bedrahtung
- **Firmware**
  - ▶ NXP1549
  - ▶ AD9833
- **Software**

# **Hardware**

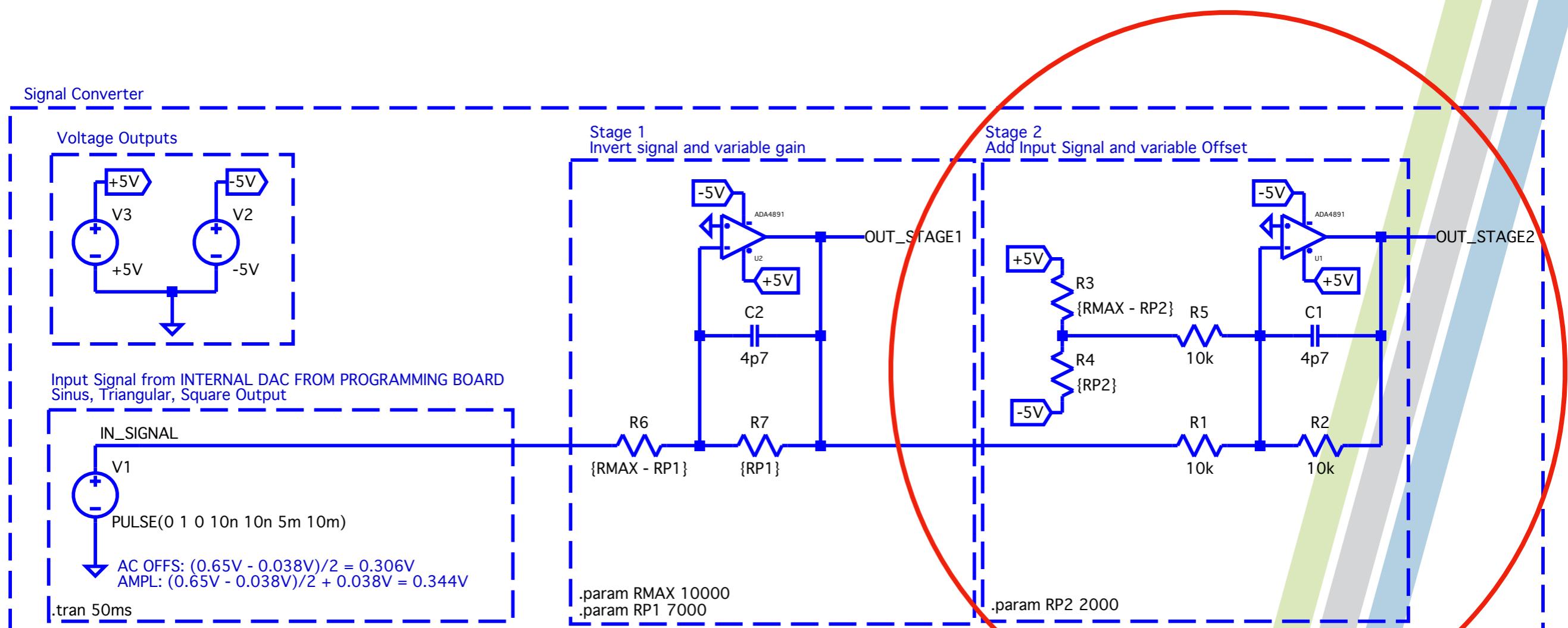
# Hardware - Simulation



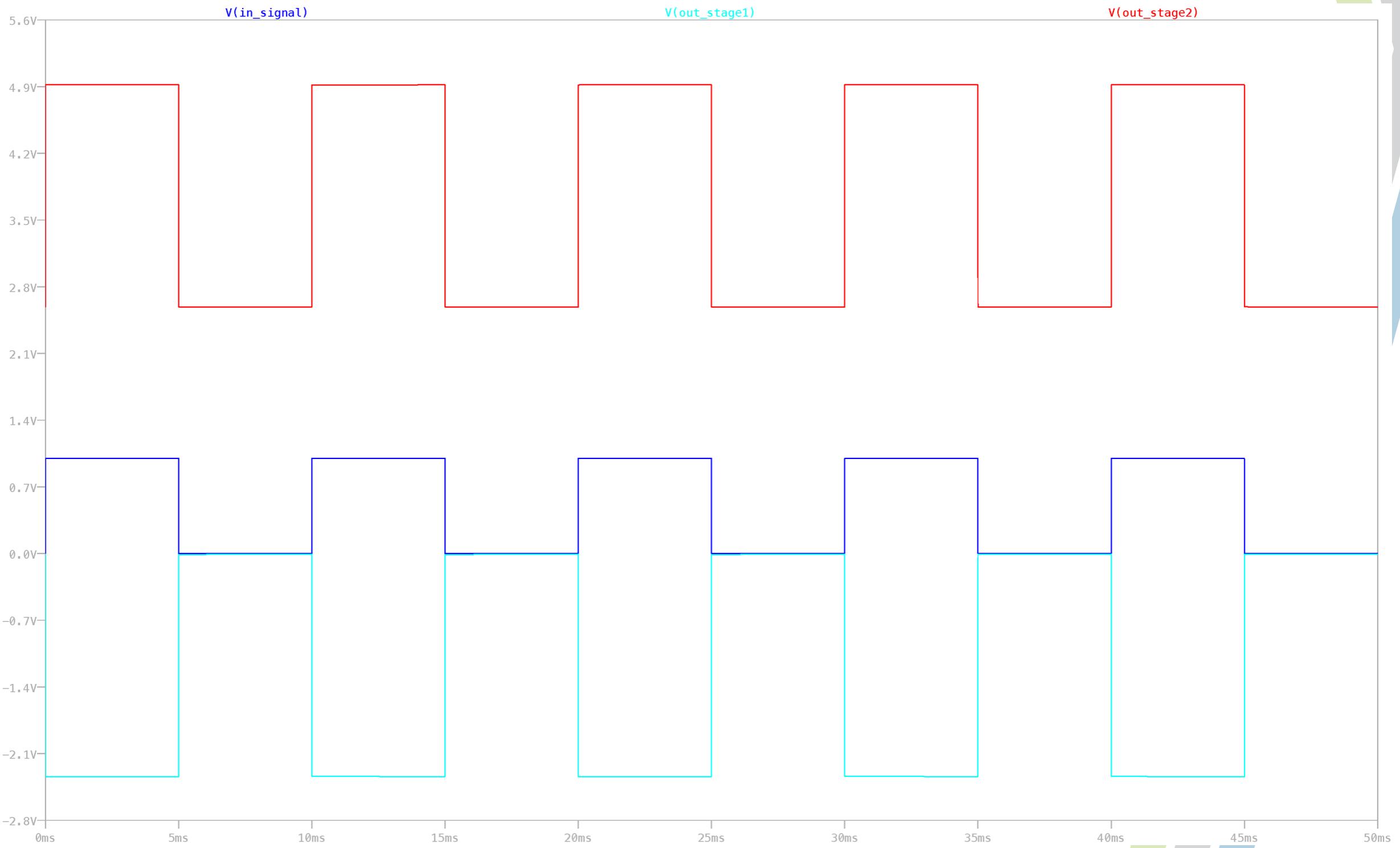
# Hardware - Simulation



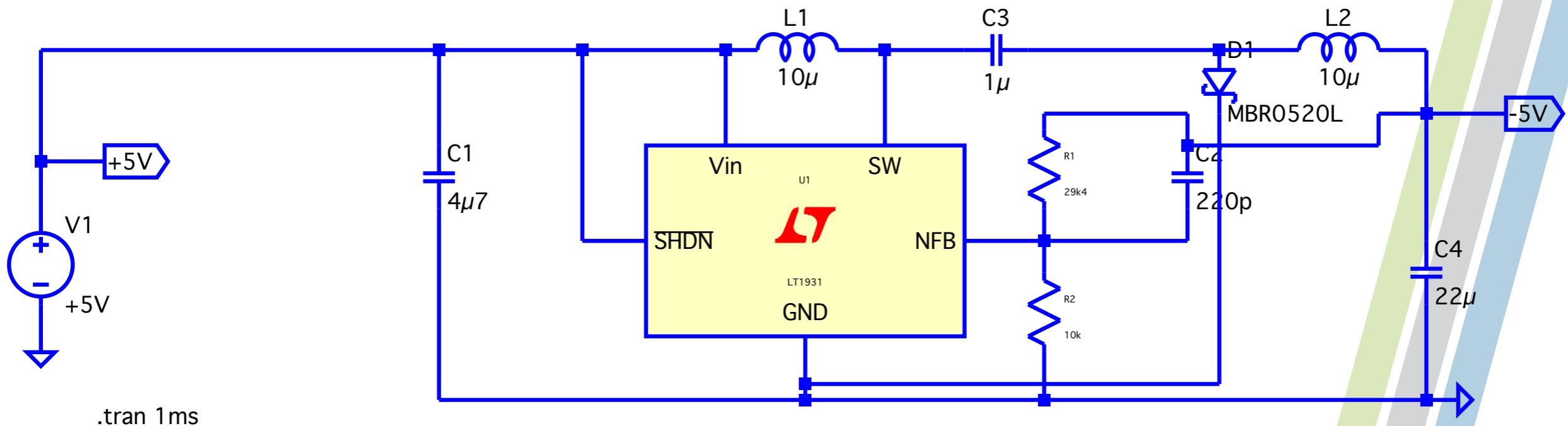
# Hardware - Simulation



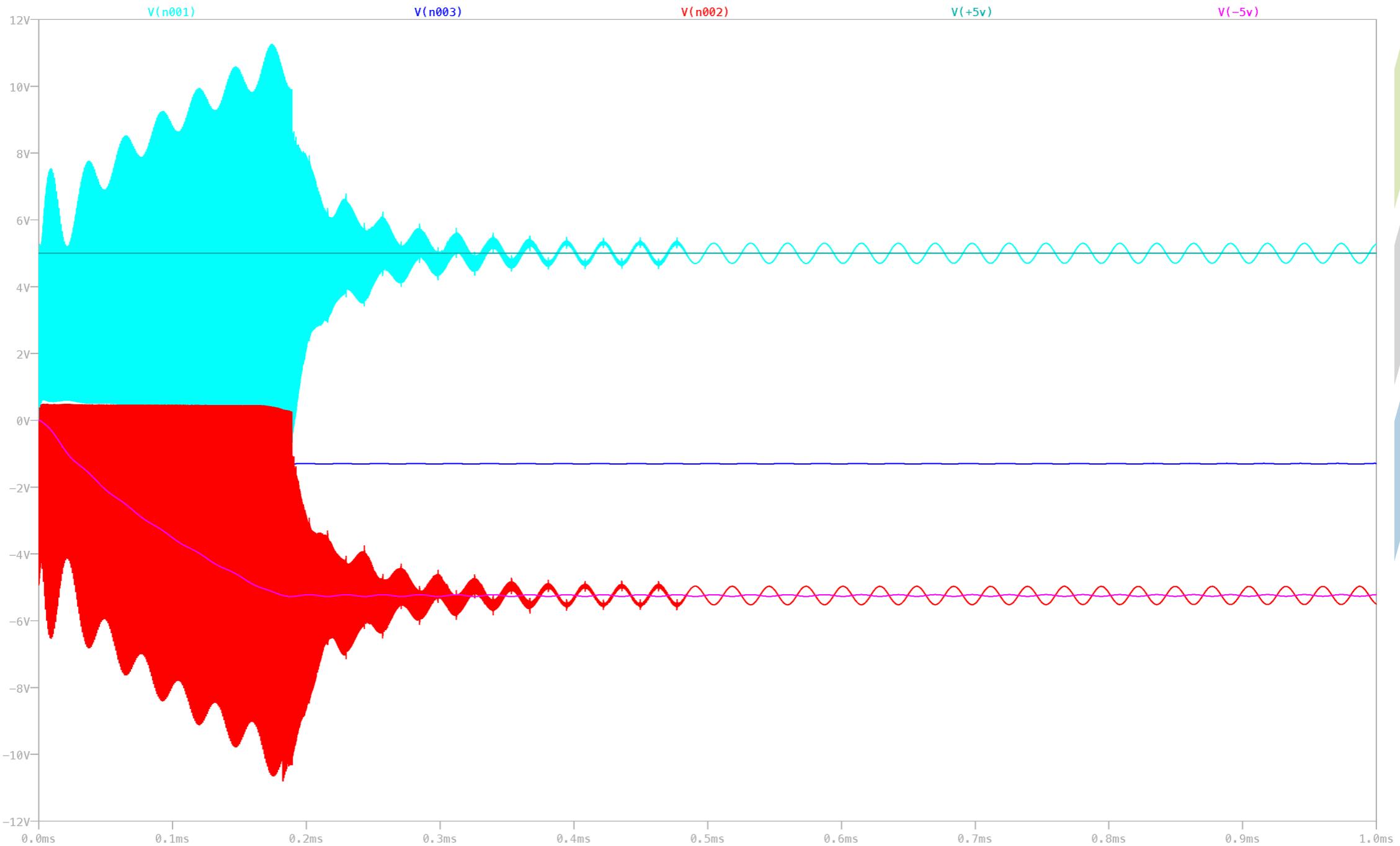
# Hardware - Simulation



## Hardware - Simulation

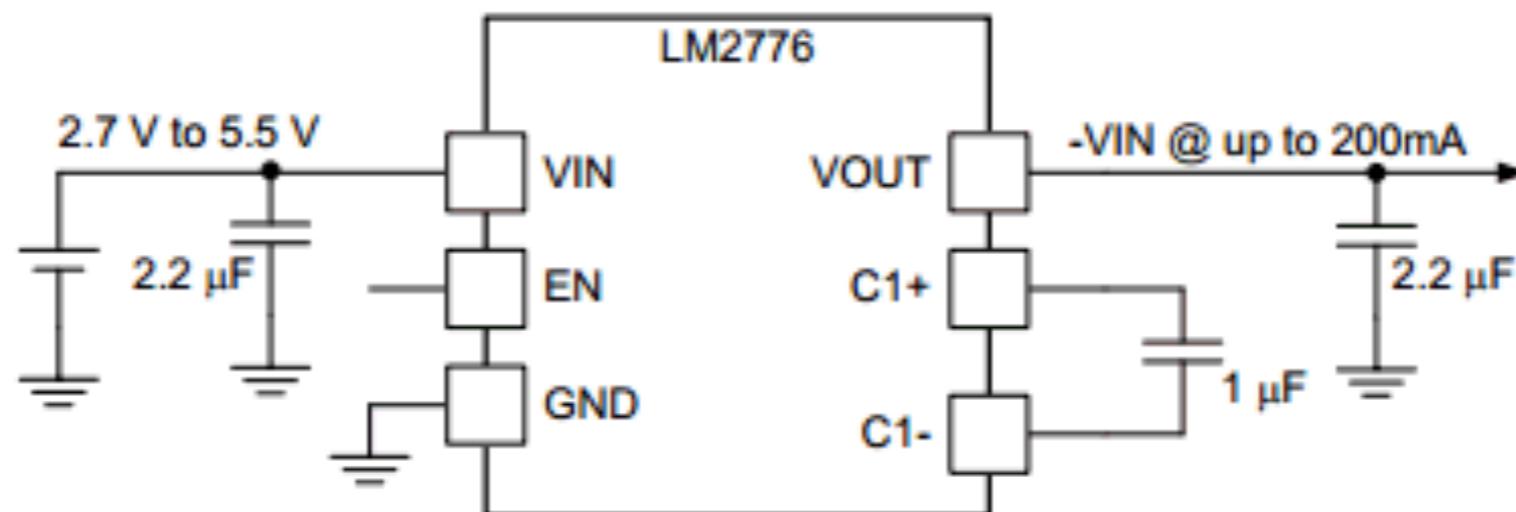


# Hardware - Simulation



# Hardware - Simulation

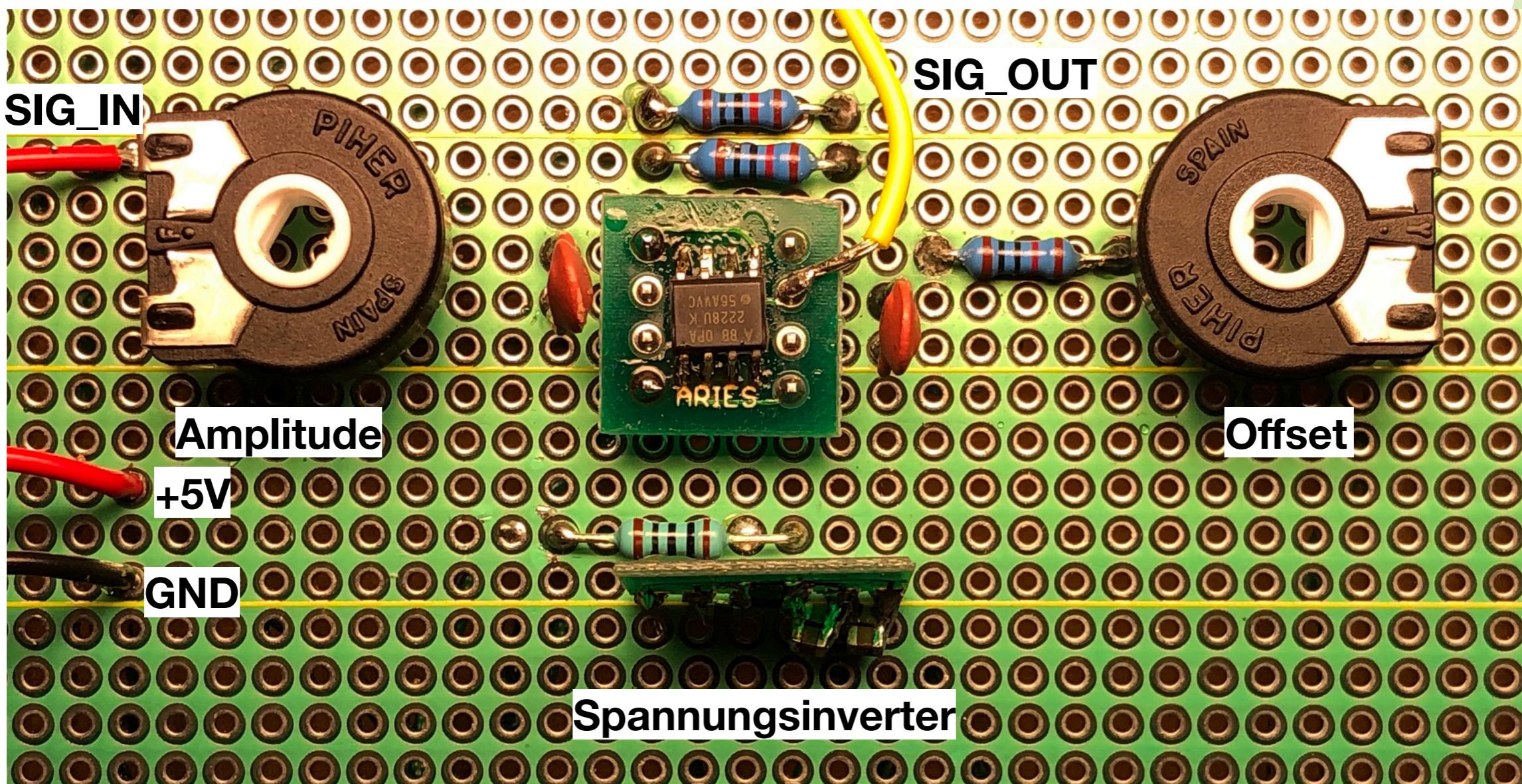
## Typical Application



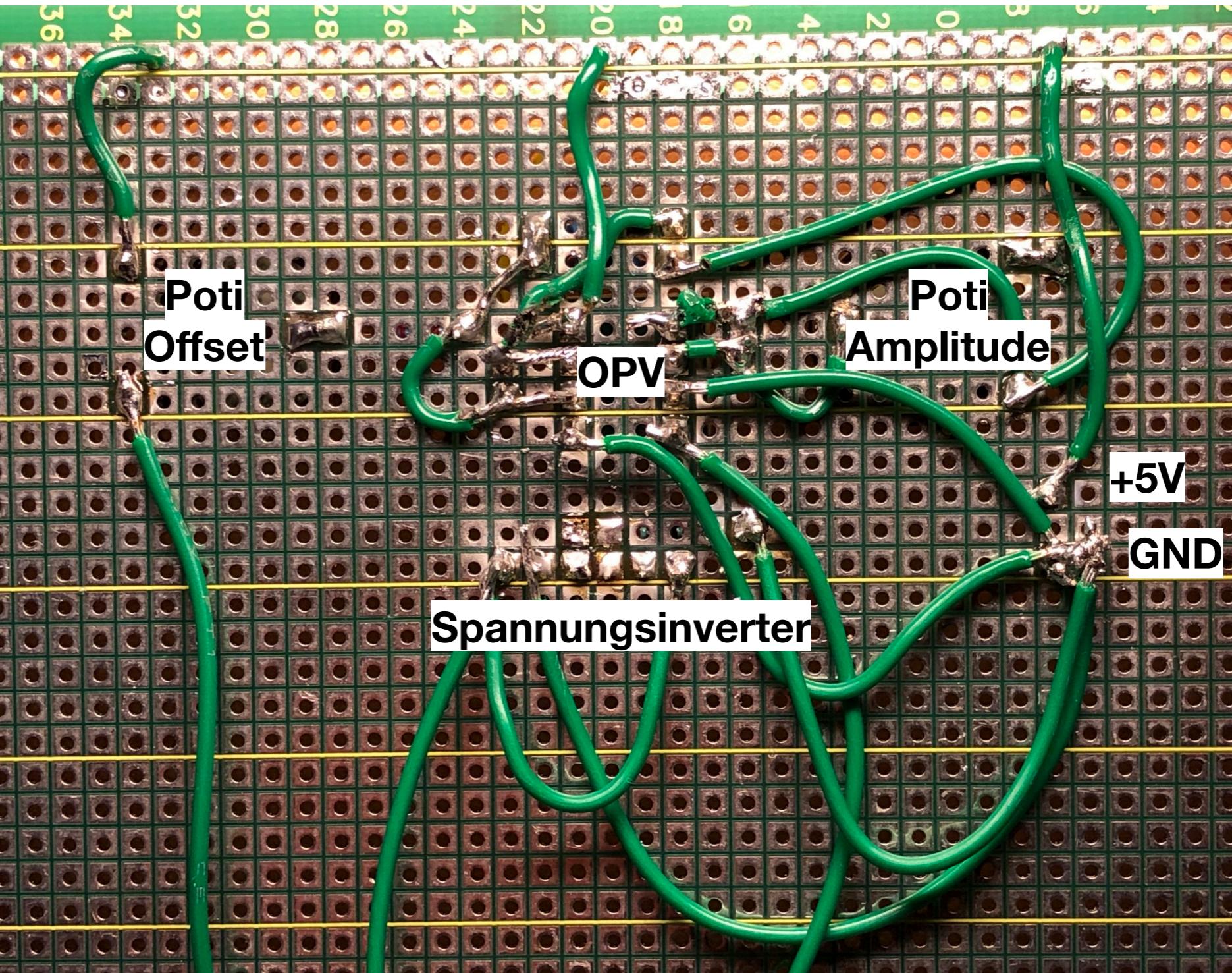
# Hardware - Stückliste

Abschluss	Bauteil	Stück	Bauteilbezeichnung	RS-Online Bestellnummer	Farnell Bestellnummer	Lagernummer	Verpackung	Gehäuse	Preis gesamt	Distributor
✓	ADA4891	1	OPV	759-1534			Gurtabschnitt (CT)	8-SOIC	€ 1,940	rs-online.com
✓	SOIC to DIP Adapter	1	Adapter		2476033				€ 4,210	farnell.com
✓	LM2776DBVR	1	Spannungsinverter		2817376		Gurtabschnitt (CT)	SOT-23-6	€ 0,853	farnell.com
✓	SOT23 to DIP Adapter	1	Adapter		1654365				€ 1,510	farnell.com
✓	Potentiometer	2	Potentiometer, 10k			B000204				FHTW
✓	Widerstand	3	Widerstand, 10k, bedrahtet							FHTW
✓	Kondensator	2	Kondensator, 4p7, bedrahtet							FHTW
✓	Kondensator	2	Kondensator, 2u2, bedrahtet							FHTW
✓	Kondensator	1	Kondensator, 1u, bedrahtet							FHTW
<b>Summe</b>									<b>€ 8,513</b>	

# Hardware - Bedrahtung

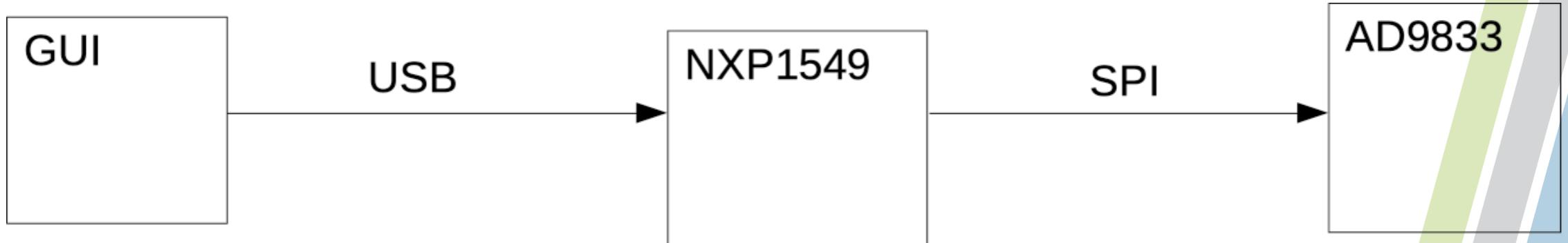


# Hardware - Bedrahtung



# **Firmware**

# Firmware



- **max. SPI data rate = 17Mbit/s**

21	reserved	0x4005 8000
20	I2C0	0x4005 4000
19	SPI1	0x4005 0000
18	SPI0	0x4004 C000
17	USART1	0x4004 8000
16	USART0	0x4004 4000
15	DMII	0x4004 0000

```
Chip_SWM_MovablePinAssign(SWM_SPI0_SCK_IO, 3);
Chip_SWM_MovablePinAssign(SWM_SPI0_MOSI_IO, 4);
Chip_SWM_MovablePinAssign(SWM_SPI0_MISO_IO, 10);
Chip_SWM_MovablePinAssign(SWM_SPI0_SSELSN_0_IO, 5);
```

# AD9833

- **clock frequency 25MHz**
  - ▶ 40ns period
- **frequency register: 28 bit**
- **phase offset register: 12 bit**
- **byte order important!**

$$f_{MCLK}/2^{28} \times FREQREG$$

$$2\pi/4096 \times PHASEREG$$

# AD9833 registers

## FREQUENCY AND PHASE REGISTERS

The AD9833 contains two frequency registers and two phase registers, which are described in Table 7.

**Table 7. Frequency and Phase Registers**

Register	Size	Description
FREQ0	28 bits	Frequency Register 0. When the FSELECT bit = 0, this register defines the output frequency as a fraction of the MCLK frequency.
FREQ1	28 bits	Frequency Register 1. When the FSELECT bit = 1, this register defines the output frequency as a fraction of the MCLK frequency.
PHASE0	12 bits	Phase Offset Register 0. When the PSELECT bit = 0, the contents of this register are added to the output of the phase accumulator.
PHASE1	12 bits	Phase Offset Register 1. When the PSELECT bit = 1, the contents of this register are added to the output of the phase accumulator.

The analog output from the AD9833 is

$$f_{MCLK}/2^{28} \times FREQREG$$

where *FREQREG* is the value loaded into the selected frequency

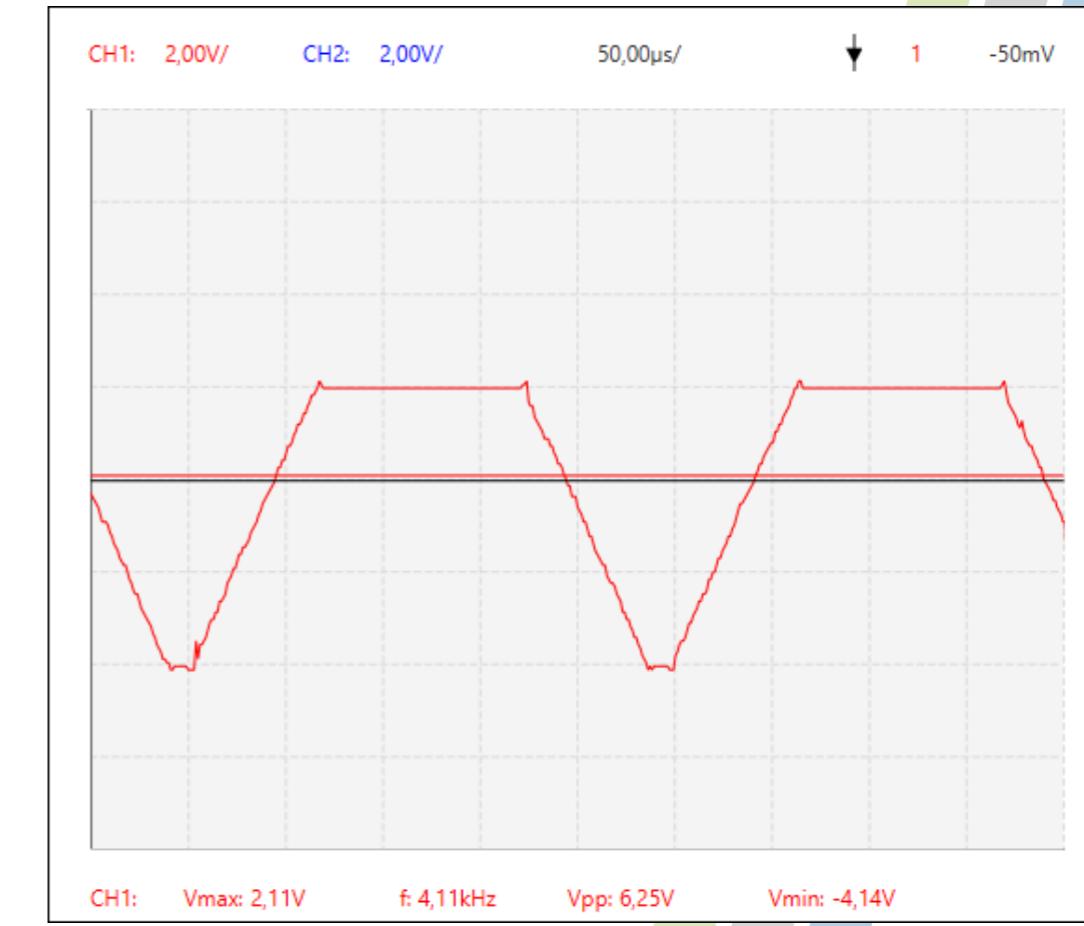
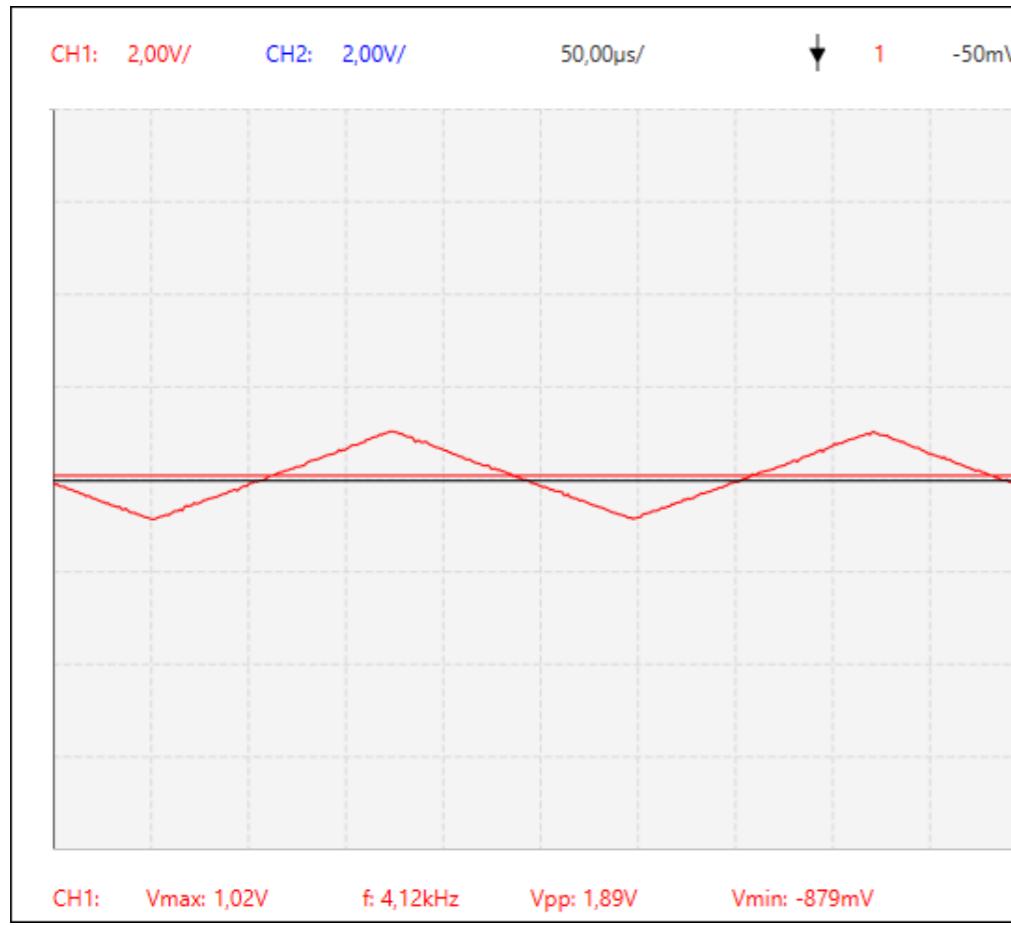
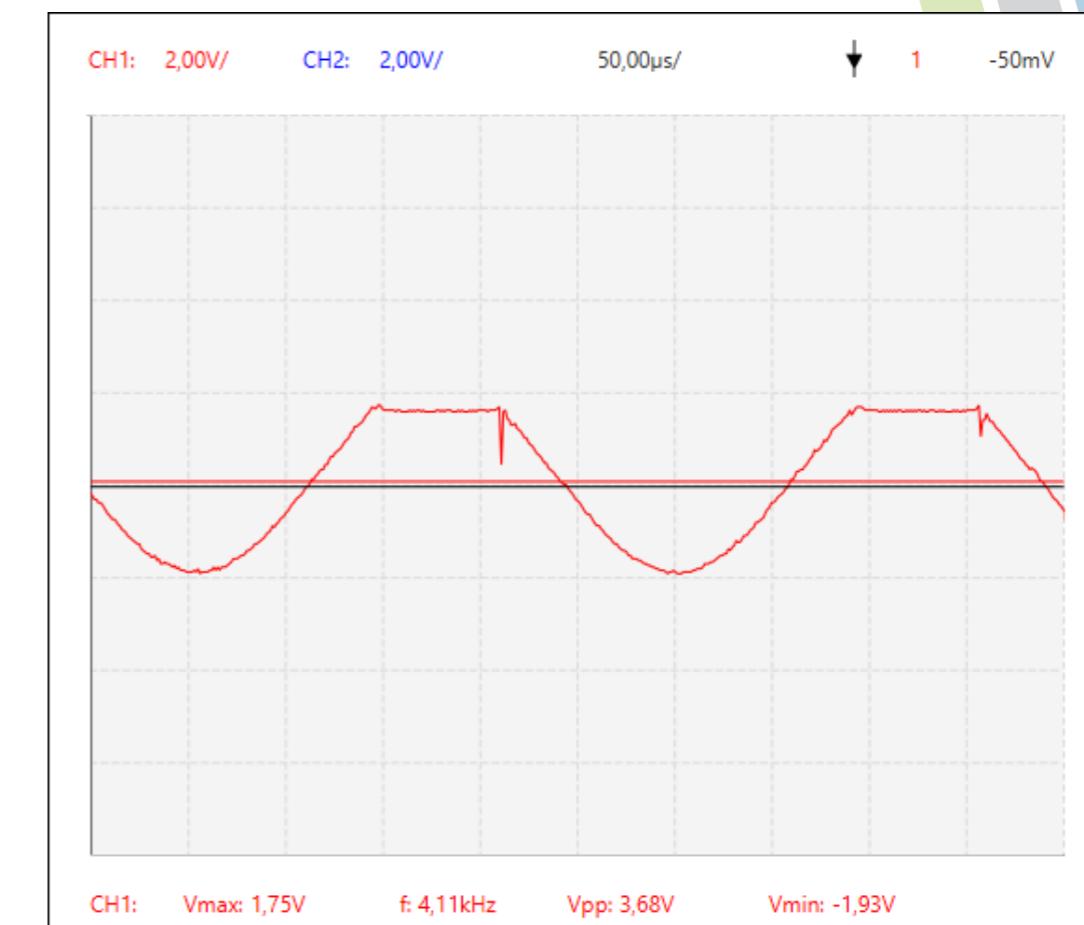
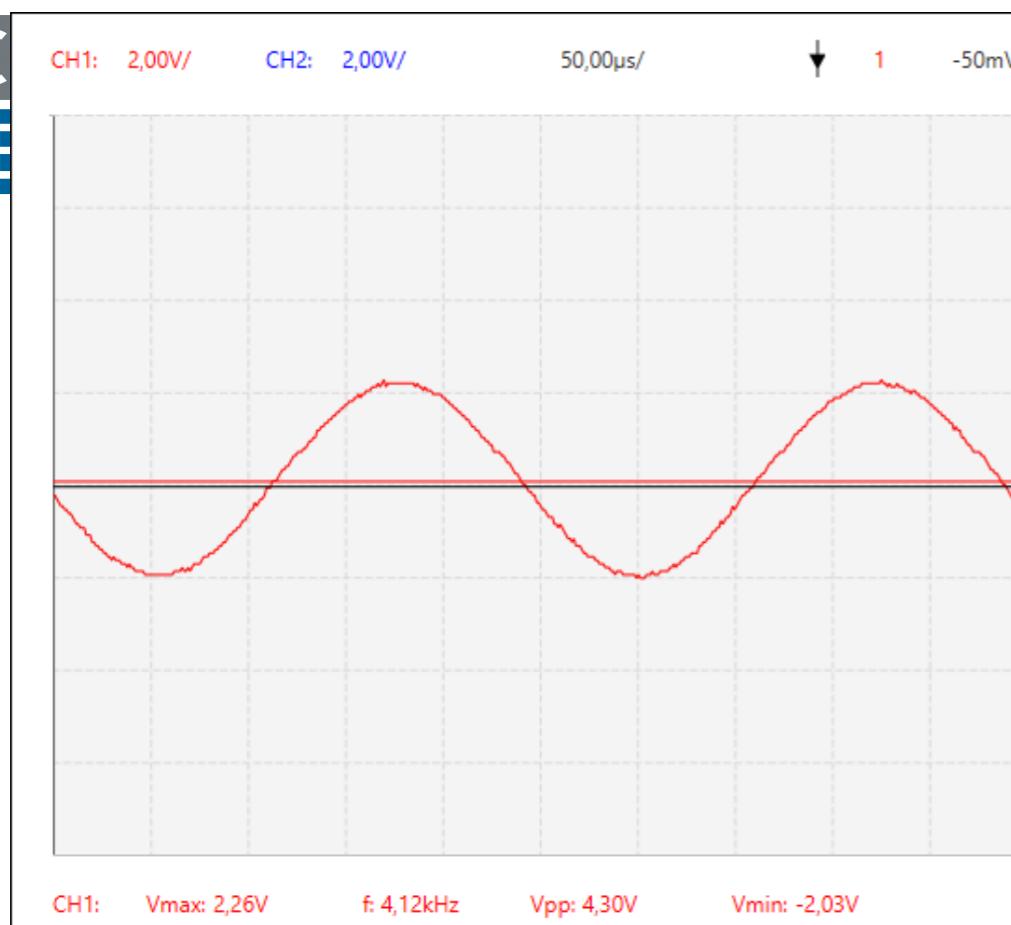
**Table 9. Writing 0xFFFFC000 to the FREQ0 Register**

SDATA Input	Result of Input Word
0010 0000 0000 0000	Control word write (D15, D14 = 00), B28 (D13) = 1, HLB (D12) = X
0100 0000 0000 0000	FREQ0 register write (D15, D14 = 01), 14 LSBs = 0x0000
0111 1111 1111 1111	FREQ0 register write (D15, D14 = 01), 14 MSBs = 0x3FFF

In some applications, the user does not need to alter all 28 bits of the frequency register. With coarse tuning, only the 14 MSBs are altered, while with fine tuning, only the 14 LSBs are altered. By setting the B28 (D13) control bit to 0, the 28-bit frequency register operates as two, 14-bit registers, one containing the 14 MSBs and the other containing the 14 LSBs. This means that the 14 MSBs of the frequency word can be altered independent of the 14 LSBs, and vice versa. Bit HLB (D12) in the control register identifies which 14 bits are being altered. Examples of this are shown in Table 10 and Table 11.

**Table 10. Writing 0x3FF to the 14 LSBs of the FREQ1 Register**

SDATA Input	Result of Input Word
0000 0000 0000 0000	Control word write (D15, D14 = 00), B28 (D13) = 0; HLB (D12) = 0, that is, LSBs
1011 1111 1111 1111	FREQ1 REG write (D15, D14 = 10),



# Software

# Software - GUI

by Helmut Resch & Christoph Swoboda

