

# Seah Kim

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## Introduction

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I am a computer architecture researcher with broad interests and strong expertise across the full stack, from chip design and hardware development to system software and application algorithms. Throughout my Ph.D., I have demonstrated the ability to establish a cohesive research agenda, addressing interconnected challenges of scalable specialization in domain-specific SoC design, with rigorous, comprehensive research from concept to silicon validation.

I have published seven architecture papers (five as first author) and in top computer architecture conferences including MICRO, ASPLOS, ISCA, HPCA, and DAC. All of my dissertation work is implemented as a full-stack real-system, evaluated rigorously with FPGA-accelerated RTL simulations, physically validated for feasibility, and fully open-sourced for reproducibility. My work has been recognized with IEEE Micro Top Picks (MICRO 2023), Best Paper Award (DAC 2021), and Distinguished Artifact Award (ISCA 2023).

I have also led a successful chip tape-out, in which I was in charge of the entire physical design and testing process, and I have a first-authored draft under submission to VLSI.

## Education

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**University of California, Berkeley**  
Ph.D. in Electrical Engineering and Computer Sciences

Aug 2019 – May 2025  
(expected)

**Seoul National University**  
BS in Electrical and Computer Engineering

Mar 2014 – Feb 2019

## Research Interests

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**Research Topic:** System Approaches for Scalable Domain-Specific SoC Architectures

Computer Architecture, VLSI, SoC Design, Hardware-Software Co-Design, System Scheduling, Robotics, Systems for ML

## Publications

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**MAVERIC: A 16nm 72 FPS, 10 mJ/frame Heterogeneous Robotics SoC with 4 Cores and 13 INT8/FP32 Accelerators**

Seah Kim, Jerry Zhao, Roger Hsiao, Yufeng Chi, Vighnesh Iyer, Vikram Jain, Borivoje Nikolić, Yakun Sophia Shao  
International Symposium on VLSI Technology and Circuits (**VLSI**), June 2025 (To appear).

**SuperNoVA: Algorithm-Hardware Co-Design for Resource-Aware SLAM**

Seah Kim, Roger Hsiao, Borivoje Nikolić, James Demmel, Yakun Sophia Shao  
International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), Volume 1, April 2025.

**Artifact Review Badges:** Artifact Available, Artifact Evaluated, Artifact Reproduced

**AuRORA: A Full-Stack Solution for Scalable and Virtualized Accelerator Integration**

Seah Kim, Jerry Zhao, Krste Asanović, Borivoje Nikolić, Yakun Sophia Shao  
IEEE Micro (**Top Picks of 2023**), July-August 2024.

**AuRORA: Virtualized Accelerator Orchestration for Multi-Tenant Workloads**

Seah Kim, Jerry Zhao, Krste Asanović, Borivoje Nikolić, Yakun Sophia Shao  
International Symposium on Microarchitecture (**MICRO**), October 2023.

**ACM Artifact Review Badges:** Artifact Available, Artifact Evaluated, Artifact Reproduced  
**Selected as one of “Top Picks from Computer Architecture Conferences, 2023”**

**RoSÉ: A Hardware-Software Co-Simulation Infrastructure Enabling Pre-Silicon Full-Stack Robotics SoC Evaluation**

Dima Nikiforov, Shengjun Chris Dong, Chengyi Lux Zhang, Seah Kim, Borivoje Nikolić, Yakun Sophia Shao  
International Symposium on Computer Architecture (**ISCA**), June 2023.

**ACM Artifact Review Badges:** Artifact Available, Artifact Evaluated, Artifact Reproduced  
**ISCA Distinguished Artifact Award**

### **DREAM: A Dynamic Scheduler for Dynamic Real-time Multi-model ML Workloads**

**Seah Kim**, Hyoukjun Kwon, Jinook Song, Jihyuck Jo, Yu-Hsin Chen, Liangzhen Lai, Vikas Chandra  
International Conference on Architectural Support for Programming Language and Operating Systems (ASPLOS),  
Volume 4, April 2023.

### **MoCA: Memory-Centric, Adaptive Execution for Multi-Tenant Deep Neural Networks**

**Seah Kim**, Hasan Genc, Vadim Vadimovich Nikiforov, Krste Asanović, Borivoje Nikolić, Yakun Sophia Shao  
International Symposium on High-Performance Computer Architecture (HPCA), March 2023.

**IEEE Artifact Review Badges:** Open Research Objects, Research Objects Reviewed, Results Reproduced

### **Gemmini: Enabling Systematic Deep-Learning Architecture Evaluation via Full-Stack Integration**

Hasan Genc, **Seah Kim**, Alon Amid, Ameer Haj-Ali, Vighnesh Iyer, Pranav Prakash, Jerry Zhao, Daniel Grubb, Harrison Liew, Howard Mao, Albert Ou, Colin Schmidt, Samuel Steffl, John Wright, Ion Stoica, Jonathan Ragan-Kelley, Krste Asanović, Borivoje Nikolić, Yakun Sophia Shao

Design Automation Conference (DAC), December 2021.

**DAC Best Paper Award**

## **Tutorials**

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### **Full-System, Full-Stack ML SoC Architecture Research with FireSim, Chipyard, Gemmini and AuRORA**

**Seah Kim**, Abraham Gonzalez, Jerry Zhao, Joonho Whangbo, Vikram Jain

Full Day Tutorial at International Symposium on Microarchitecture (MICRO), November 2024.

### **Gemmini: Generate Custom DNN Accelerators with Full-System Full-Stack Evaluation**

Hasan Genc, Simon Guo, **Seah Kim**, Vadim Nikiforov

Half Day Tutorial at Machine Learning and Systems (MLSys), August 2022.

## **Workshops, Invited Talks**

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### **Algorithm-Hardware Co-Design of SLAM with SuperNoVA**

**Seah Kim**, Roger Hsiao, Borivoje Nikolić, James Demmel, Yakun Sophia Shao

3rd Workshop on Robotics Acceleration with Computing Hardware (RoboARCH) in conjunction with MICRO 2024.

### **Democratizing DNN Accelerators**

**Seah Kim**

3rd Workshop on Democratizing Domain-Specific Accelerators (WDDSA) in conjunction with MICRO 2024.

### **AuRORA: Virtualized Accelerator Orchestration for Multi-Tenant Workloads**

**Seah Kim**, Jerry Zhao, Krste Asanović, Borivoje Nikolić, Yakun Sophia Shao

9th Career Workshop for Inclusion and Diversity in Computer Architecture (CWIDCA) in conjunction with MICRO 2023.

### **An Open-source Framework for Virtualized and Disaggregated RISC-V Accelerators**

Jerry Zhao, **Seah Kim**, Borivoje Nikolić, Krste Asanović, Yakun Sophia Shao

2nd Open-Source Computer Architecture Research (OSCAR) in conjunction with ISCA 2023.

### **Memory-Centric, Adaptive Execution for Multi-Tenant DNNs**

**Seah Kim**, Hasan Genc, Vadim Vadimovich Nikiforov, Krste Asanović, Borivoje Nikolić, Yakun Sophia Shao

2nd Architecture, Compiler, and System Support for Multi-model DNN Workloads (ACSMD) in conjunction with ISCA 2022.

### **Gemmini: An Open-Source, Full-System DNN Accelerator Design and Evaluation Platform**

Hasan Genc, **Seah Kim**, Vadim Vadimovich Nikiforov, Simon Zirui Guo, Borivoje Nikolić, Krste Asanović and Yakun Sophia Shao

1st Open-Source Computer Architecture Research (OSCAR) in conjunction with ISCA 2022.

## **Awards**

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MICRO PhD Forum	2024
Rising Stars in EECs	2024
Qualcomm Innovation Fellowship Finalist	2024
IEEE Micro's Top Pick in Computer Architecture	2024

Machine Learning and Systems Rising Star	2023
Qualcomm Innovation Fellowship Finalist	2023
ISCA Distinguished Artifact Award	2023
DAC Best Paper Award	2021
AI Compute Symposium Top Poster Award - IBM and IEEE CAS/EDS	2020
EECS Departmental Fellowship	2019
Study Abroad Fellowship - Kwanjeong Educational Foundation	2019-2023
National Scholarship for Science and Engineering - Korean Student Aid Foundation	2016-2018

## Experience

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### [ Industry ]

**AI Research Intern**, Meta, Sunnyvale, CA May 2022 - Aug 2022

- Worked on creating the benchmark and dynamic scheduler for the AR/VR application
- Paper accepted to ASPLOS 2023

**Special Project Group (SPG) Intern**, Apple, Cupertino, CA May 2021 - Aug 2021

- Created a cycle-accurate performance model for sparse graph workload
- Designed an accelerator architecture for sparse graph workload

### [ Academic ]

**Graduate Student Researcher**, UC Berkeley, Berkeley Architecture Research Group Nov 2019 - Present

- Advisors: Borivoje Nikolić, Yakun Sophia Shao

**Graduate Student Researcher**, UC Berkeley, Berkeley Wireless Research Center Aug 2019 - Present

- Led an Intel16 chip tape-out (first-author): design submitted in December 2023, successfully tested in Summer 2024

**Undergraduate Researcher**, Integrated Systems Design Lab, Seoul National University Jan 2018 - July 2019

- Advisor: Deog-Kyoon Jeong
- Participated in a Samsung 28nm and a TSMC 40nm CMOS tape-out of a fractional digital phase locked loop using Injection Locking Oscillators
- Designed a transmitter for an automotive imaging sensor

## Teaching Experiences

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Guest Lecturer for Hardware for Machine Learning (EE 290) Spring 2024

Graduate Student Instructor for Digital Design and Integrated Circuits (EECS 151/251A) Fall 2022

Graduate Student Instructor for Great Ideas in Computer Architecture (CS 61C) Fall 2020

Tutor for Analog Integrated Circuits (Seoul National University) Fall 2018

## Service

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UC Berkeley KGSA x KSEA undergraduate student mentoring 2024

IISWC Artifact Evaluation Committee 2024

Visit Day Area Student Lead Organizer 2024

Visit Day Peer Advisor 2021-2024

Visit Day Area Student Organizer 2021-2023

Campus Mentoring Program (Seoul National University) 2015

Class Representative (Department of ECE, Seoul National University) 2014

## Skills

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**Languages:** C++, C, Scala, Chisel, Verilog, SystemVerilog, Python, RISC-V Assembly, Make, Bash, Pytorch, TensorFlow

**Hardware Platforms, Tools:** Cadence Physical Design Tools (Genus, Innovus, Virtuoso, Joules), Vivado, Verdi, VCS, Xilinx FPGAs, Arduino, Raspberry Pi