# Sean Chou

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## Skills

**Languages:** SystemVerilog, SVA, Verilog, C, assembly, Python, tcl, OCaml

**Methodologies:** UVM, formal verification, RIS/ISSCMP, portable stimulus

**Design Knowledge:** ARM/RISC-V CPU arch/uarch, cache coherency, USB

## Experience

**Anshingtek** Hsinchu, Taiwan

*Principal Manager* *Dec 2020 – Present*

- ARM v9a small-core CPU IP co-DV Lead: 2022-2024 I lead around 40 DV engineers in our customer (ARM China) and Anshingtek, separated into 10 DV Units: 1 top level, 2 multi-unit level, 6 units and a formal team.
- Anshingtek co-Engineer Manager (manage 20+ engineers) - host Anshingtek monthly all-hands since 2022-Jan.
- I created a tool to interpret ARMv9a ASL and deployed it to gem5 model, DPU/VPU/MU DV and ISA Formal.
- I verified GIC CPU interface from zero to sign-off and FPU (MUL/FMA/DIV) formal equivalence w/ SoftFloat.

**MediaTek. Inc** Hsinchu, Taiwan

*Senior Manager (lead 28 people DV team)* *Mar 2018 – Dec 2020*

- DV of In-house RISC-V cores (based on UVM and Spike model)
  Core 1: 2-way 6 stages in-order pipeline processor. FPU, L1, branch predict, exception/interrupt, debug, trace.
  Core 2: 3-way 8 stages with shared L2, vector extension and user defined extension. (only differences are listed)
- DV of an In-house cache coherency interconnect for v8.0a cores such as Cortex-A53 with snoop filter.
- DV of Integrated ARM licensed CPU sub-system: multiple core scenarios based on portable stimulus.
- DV of in-house DLA: data types conversion, convolution, activation, compression, flow controller.

**MediaTek. Inc** Hsinchu, Taiwan

*Verification Methodology (CAD) Manager* *Mar 2013 – Mar 2018*

- UVM/SV training, collaboration and deployment with needed teams such bus interconnect or ethernet switch.
- Emulators: Palladium, Zebu, Veloce: porting, speed optimize, enable peripherals and management
- In-house VIP/AIP and regression utilities (coverage, regression, permission management, CI)
- Establish Power Aware (UPF) simulaiton flow for phone; static flow: formal/SVA, CDC, lint
- DV related management: people, licenses, EDA collaboration, IT for LSF queue (machine slots).

**MediaTek. Inc** Hsinchu, Taiwan

*Technical Manager* *June 2010 – Feb 2013*

- USB 3.0 controller DV (2 DUT: xHCI Host and proprietary device): hands on and finish the 1st project (around 180 RTL bugs fixed in 10 months and make FPGA/Silicon mass production smoothly) then transfer to others.
- In charge of H/W accelerators flow and successfully deploy Palladium to modem team.
- Attend to DVCon 2012 and read all 2010-2011 DVCon Papers.

**Ambarella** Hsinchu, Taiwan

*Researcher* *Nov 2009 – May 2010*

- Self study OVM and coached 3 members to verify USB20 Device and NAND Flush Controller.

**Sunplus** Hsinchu, Taiwan

*Technical Manager* *Jul 2002 – Oct 2009*

- USB 1.0 controllers design from scratch alone. from read spec., understand the request from PCI-USB card, design RTL coding, setup FPGA environment, post-silicon validation, customer engagement.
- Lead 3 people-team for 2 USB 2.0 designs: standard OHCI/EHCI host and dual-role proprietary design
- Help to build a 14 people design/verification team in Chengdu at 2006. (they grew to 37 people in 2009) include recruiting/training/goal setting/tracking/review. (try to build DV to prevent bugs found by head quarter)

## Education

**National Chaio Tung University** Hsinchu, Taiwan

*Master's Degree in Electronics Engineering* *Sep 2000 – Jun 2002*

*Bachelor of Engineering - BE, Electronics Engineering* *Sep 1996 – Jun 2000*