

# MASTERS PROJECT V3

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Description:



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A

A

B

B

C

C

D

D

E

E

Description:



Block Diagram

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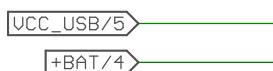
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1 2 3 4 5 6 7 8

# INPUTS

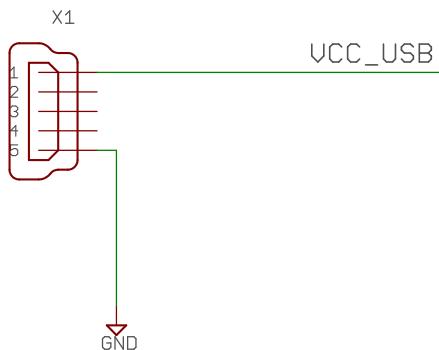


# OUTPUTS



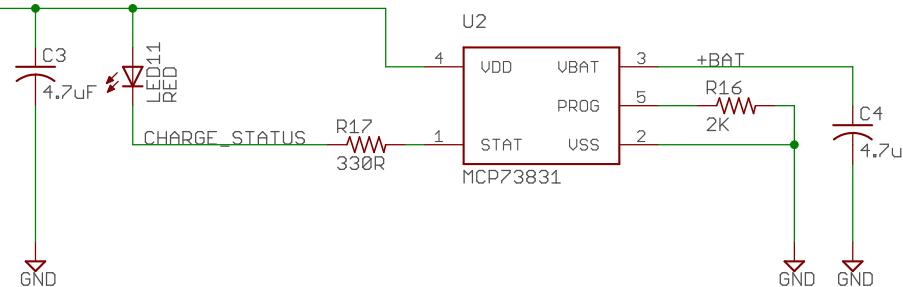
## USB Power

Micro USB connector  
Only used for charging,  
No data connections lines  
are connected on the device



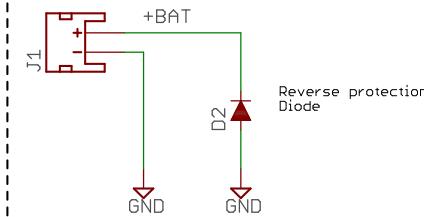
## Battery Management

LED is okay here. Charger circuit is powered by USB. No current will flow if USB not connected so LED will draw now current here



## Battery Connector

Use a standard 2-Pin keyed JST connector as all LiPo batteries have standardized on this.



## Test Points

### Battery

TP3  
UCC\_USB  
TP11  
GND

### USB

TP1  
+BAT  
TP2  
GND

### CHARGER

TP25  
CHARGE\_STATUS

#### Description:

1 2 3 4 5 6 7 8

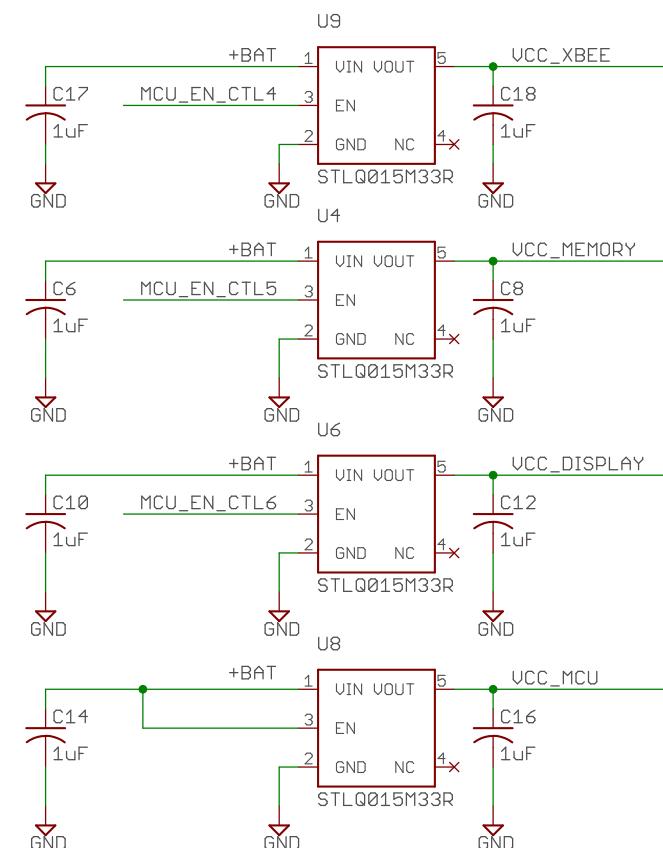
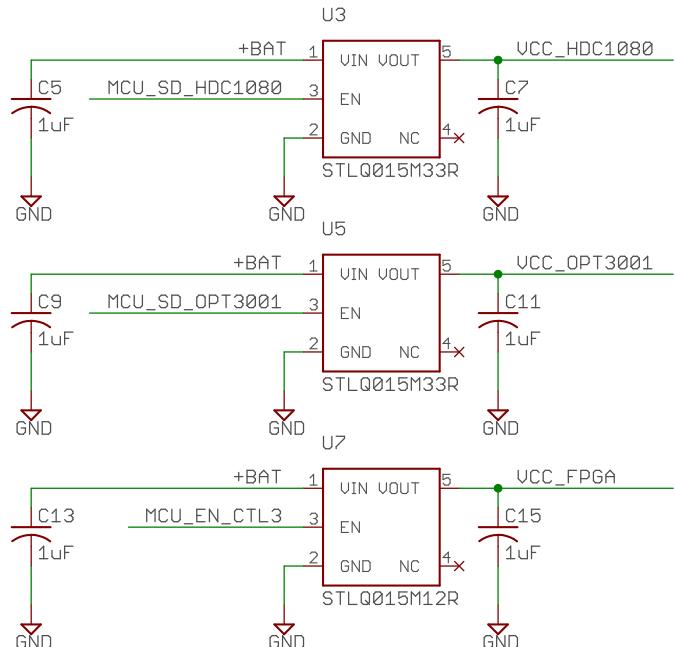
1 2 3 4 5 6 7 8

## INPUTS

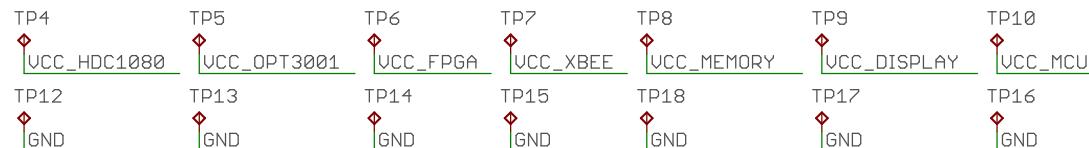
- +BAT/3
- MCU\_SD\_HDC1080/11
- MCU\_SD\_OPT3001/11
- MCU\_EN\_CTL3/11
- MCU\_EN\_CTL4/11
- MCU\_EN\_CTL5/11
- MCU\_EN\_CTL6/11

## OUTPUTS

- VCC\_HDC1080/5
- VCC\_OPT3001/5
- VCC\_FPGA/5
- VCC\_XBEE/5
- VCC\_MEMORY/5
- VCC\_DISPLAY/5
- VCC MCU/5



## TEST POINTS



**Description:** DC/DC converter for each subsystem. Input to all converters is BAT+. The DC/DC converter steps the voltage down to a range acceptable for each device.

NOTE: MCU DC/DC converter is always on.

NOTE: Should use switching regulators. TI makes some switching regulators that are similar footprint.

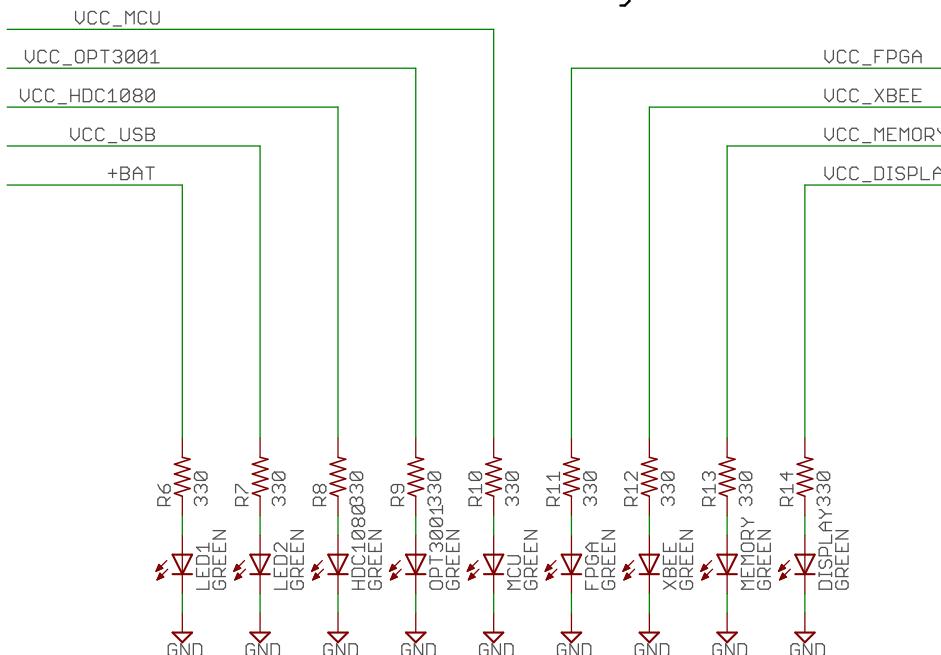
NOTE: Voltage supplied to each device should be minimized.

1 2 3 4 5 6 7 8

# INPUTS

VCC MCU/4  
 VCC OPT3001/4  
 VCC HDC1080/4  
 VCC USB/3  
 +BAT/4  
 VCC DISPLAY/4  
 VCC MEMORY/4  
 VCC XBEE/4  
 VCC FPGA/4

## Power Indicators For Each Subsystem



Note: Do not populate LEDs in production.  
Each LED would consume current which is unneeded.

**Description:** Visual indicators used for visually checking power to a subsystem is being supplied

# INPUTS

VCC\_HDC1080/5

# COMMUNICATION

MCU\_SCL/7

MCU\_SDA/7

A

A

B

B

C

C

D

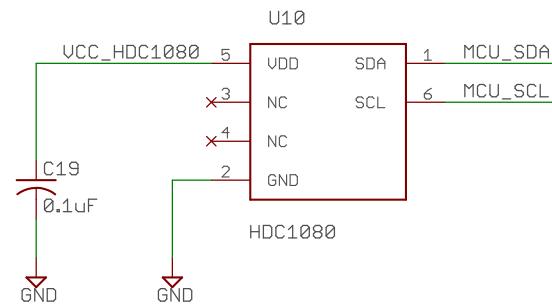
D

Vdd: 2.7 - 5.5V, Nominal = 3v  
 Recomended Max Sample Rate: 1sps  
 Capacitor recommended to be 0.1uF ceramic X7R

NOTE: No copper plane under IC  
 Place IC away from heat generating parts

NOTE: I2C Address = 0x40

NOTE: System can have only ONE HDC1080,  
 unless a I2C expander is used to isolate  
 busses



## Description:



Sensor: Temperature & Humidity

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## INPUTS

VCC\_OPT3001/5

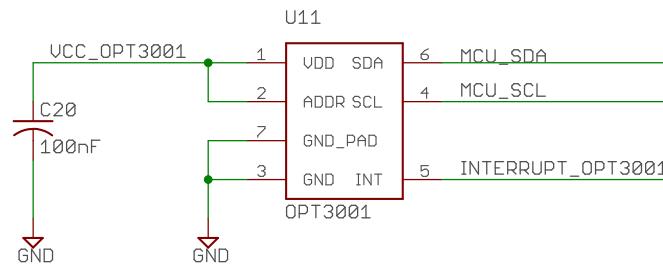
## OUTPUTS

INTERRUPT\_OPT3001/11

## COMMUNICATION

MCU\_SCL/6

MCU\_SDA/6



Vdd: 1.6 - 3.6V

Note: Keep area around IC clear.

Note: Place Capacitor on bottom of board

NOTE: I2C Address = 0x45

### Description:



Sensor: UV Index& Ambient Light

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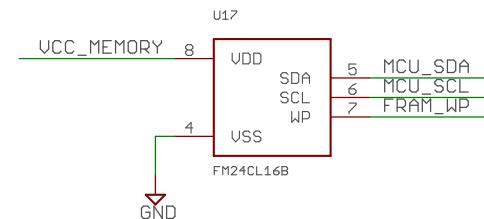
1 2 3 4 5 6 7 8

## INPUTS

UCC\_MEMORY/5  
FRAM\_WP/11

## COMMUNICATION

MCU\_SDA/7  
MCU\_SCL/7



## TEST POINTS

TP34  
FRAM\_WP

Description:



Memory: FRAM	
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1 2 3 4 5 6 7 8

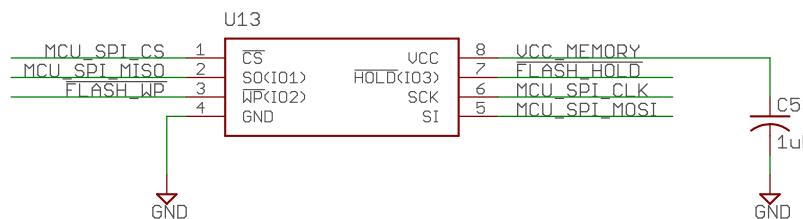
1 2 3 4 5 6 7 8

## INPUTS

FLASH\_HOLD/12  
FLASH\_WP/12  
MCU\_SPI\_CS/12  
VCC\_MEMORY/8

## COMMUNICATION

MCU\_SPI\_CLK/12  
MCU\_SPI\_MOSI/12  
MCU\_SPI\_MISO/12



## TEST POINTS

TP37 MCU\_SPI\_CS TP36 MCU\_SPI\_MISO TP33 FLASH\_WP TP35 FLASH\_HOLD TP38 MCU\_SPI\_CLK TP39 MCU\_SPI\_MOSI

### Description:

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

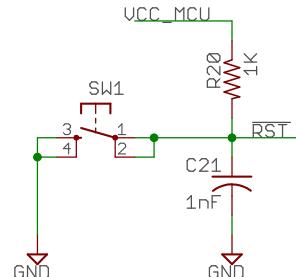
## INPUTS

VCC MCU/5

## OUTPUTS

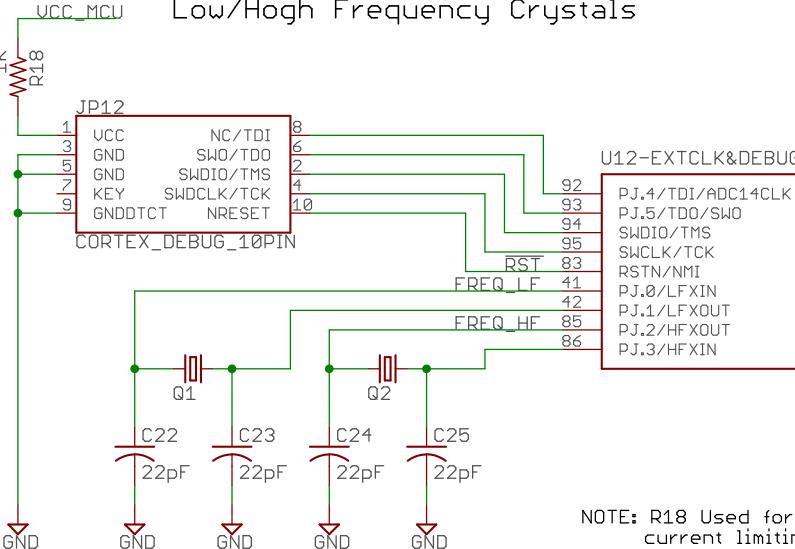
RST

## Reset Switch



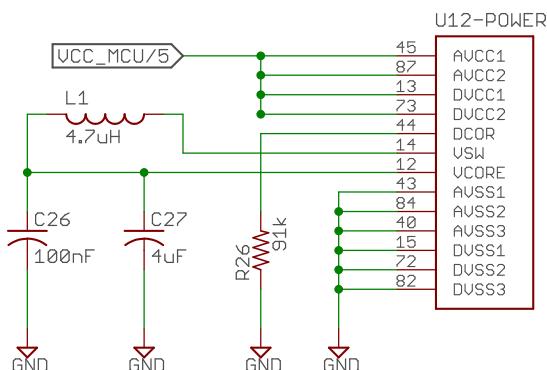
NOTE: RST line also uses internal R of MCU for filtering

External JTAG/SWD To MCU & Low/Hogh Frequency Crystals



NOTE: R18 Used for current limiting

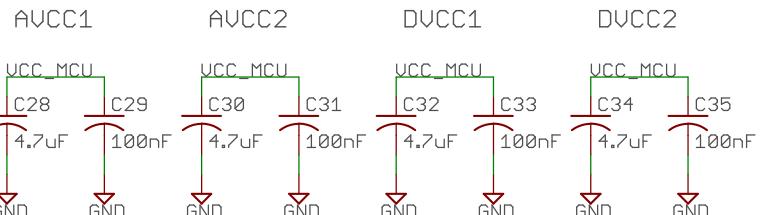
## Power



NOTE: L = LQM21PN4R7NGR

NOTE: Place as close to indicated pins as possible

NOTE: 100nF decoupling capacitor should be a low-ESR ceramic



## TEST POINTS

TP19 RST  
TP21 FREQ\_LF  
TP20 FREQ\_HF

## Description:

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

## INPUTS

- CHARGE\_STATUS/3
- UCC MCU/10
- FPGA\_DONE/13
- RTC\_CLKOUT/15
- RTC\_INT1/15
- INTERRUPT\_OPT3001/7

## OUTPUTS

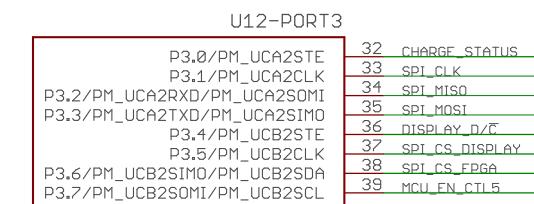
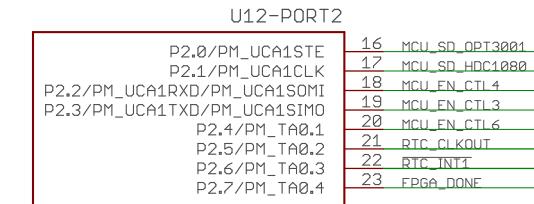
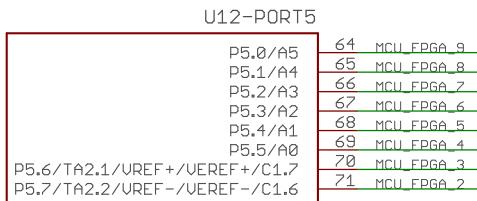
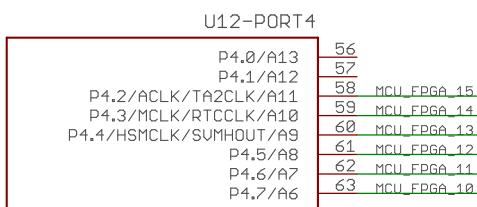
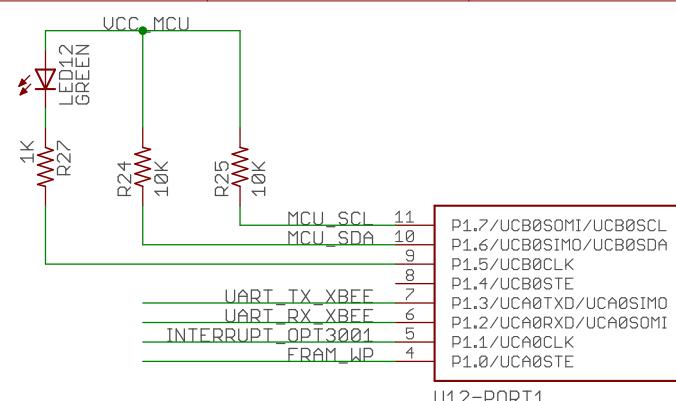
MCU_SD_OPT3001/4	MCU_EN_CTL6/4
MCU_SD_HDC1080/4	MCU_EN_CTL5/4
MCU_EN_CTL4/4	FRAM_WP/8
MCU_EN_CTL3/4	

## I/O

P10.5/12

## COMMUNICATION

MCU_FPGA_2/13	SPI_CLK/16
MCU_FPGA_3/13	SPI_MISO
MCU_FPGA_4/13	SPI_MOSI/16
MCU_FPGA_5/13	DISPLAY_D/C/16
MCU_FPGA_6/13	SPI_CS_DISPLAY/16
MCU_FPGA_7/13	SPI_CS_FPGA/13
MCU_FPGA_8/13	UART_TX_XBEE/14
MCU_FPGA_9/13	UART_RX_XBEE/14
MCU_FPGA_10/13	MCU_SCL/8
MCU_FPGA_11/13	MCU_SDA/8
MCU_FPGA_12/13	
MCU_FPGA_13/13	
MCU_FPGA_14/13	
MCU_FPGA_15/13	



## TEST POINTS



### Description:

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

## INPUTS

VCC\_MCU/11  
EINK\_BUSY/16

## OUTPUTS

XBEE\_RESET/14  
EINK\_RST/16  
FLASH\_HOLD/9

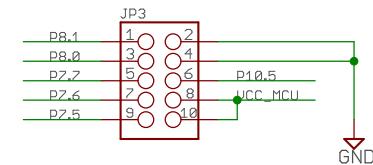
## I/O

P10.5/11

## COMMUNICATION

MCU\_FPGA\_1/13

## External Pin Connections



U12-PORT7

88	
89	
90	
91	
26	XBFF_RESET
27	P2.5
28	P2.6
29	P2.7

U12-PORT8

30	p8.0
31	p8.1
46	EINK_RST
47	EINK_BUSY
48	
49	
50	
51	

U12-PORT6

54	P6.0/A15
55	P6.1/A14
76	MCU_SPI_CS
77	MCU_SPI_CLK
78	MCU_SPI_MOSI
79	MCU_SPI_MISO
80	FLASH_WP
81	

U12-PORT9

52	P9.0/A17
53	P9.1/A16
74	MCU_FPGA_1
75	FLASH_HOLD
96	
97	
98	
99	

## TEST POINTS

TP31  
EINK\_RST

TP32  
EINK\_BUSY

### Description:



MSP432: I/I Cont.

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## INPUTS

`UCC_FPGA/5`

`SPI_CS_FPGA/11`

## OUTPUTS

`FPGA_DONE/11`

## COMMUNICATION

<code>MCU_FPGA_1/12</code>	<code>MCU_FPGA_9/11</code>
<code>MCU_FPGA_2/11</code>	<code>MCU_FPGA_10/11</code>
<code>MCU_FPGA_3/11</code>	<code>MCU_FPGA_11/11</code>
<code>MCU_FPGA_4/11</code>	<code>MCU_FPGA_12/11</code>
<code>MCU_FPGA_5/11</code>	<code>MCU_FPGA_13/11</code>
<code>MCU_FPGA_6/11</code>	<code>MCU_FPGA_14/11</code>
<code>MCU_FPGA_7/11</code>	<code>MCU_FPGA_15/11</code>
<code>MCU_FPGA_8/11</code>	

## UNUSED

### U1-PORTR

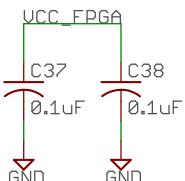
75	PR2A	60	PL6A	16
74	PR2B	59	PL6B	17
71	PR2C	58	PL6C	18
70	PR2D	57	PL6D	19
69	PR3A	54	PL7A/PCLKT3_2	20
68	PR3B	53	PL7B/PCLKT3_0	21
67	PR3C	52	PL7C	24
66	PR3D	51	PL7D	25
65	PR5A			
64	PR5B			
63	PR5C/PCLKT1_0			
62	PR5D/PCLKC1_0			

### U1-PORTL

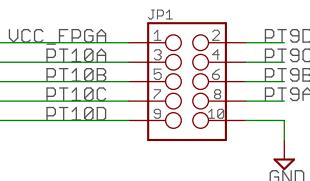
4	PL2A	16	PL6A	95
2	PL2B	17	PL6B	98
3	PL2C/PCLKT3_2	18	PL6C	97
4	PL2D/PCLKC3_2	19	PL6D	96
7	PL3A	20	PT6A	PT10A
8	PL3B	21	PT6B	PT10B
9	PL3C	22	PT6C	PT10C
10	PL3D	23	PT6D	PT10D
12	PL5A/PCLKT3_1	24	PT7A/TDO	PT10C/JTAGENB
13	PL5B/PCLKC3_1	25	PT7B/TDI	PT10D/PROGRAM
14	PL5C		PT7C/TCK	PT11A
15	PL5D		PT7D/TMS	PT11C/INITN

NOTE: Place close to indicated voltage pins.

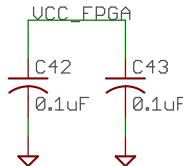
## Decoupling capacitors



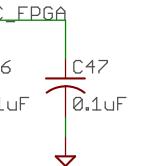
## External Header



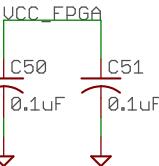
VCCIO0



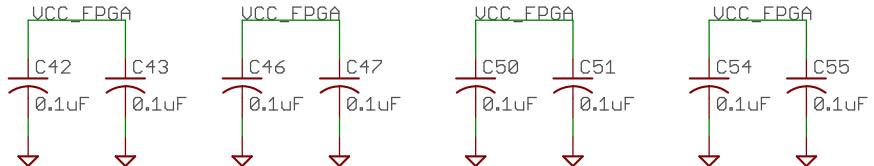
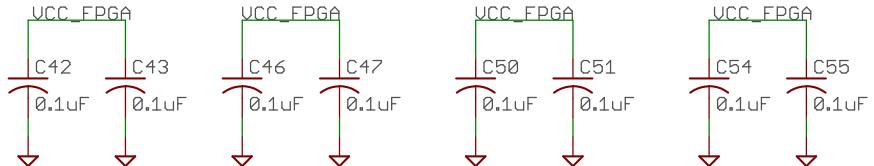
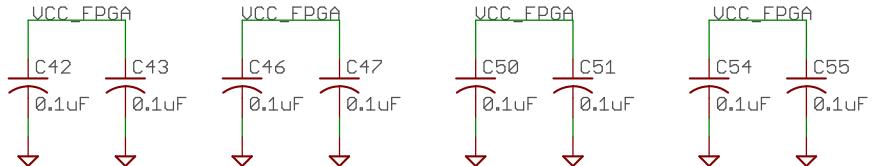
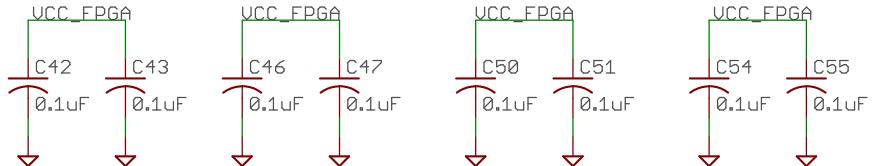
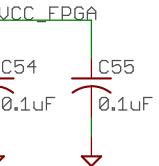
VCCIO1



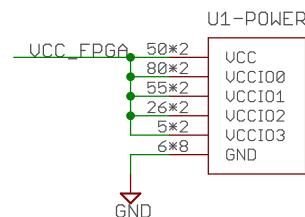
VCCIO2



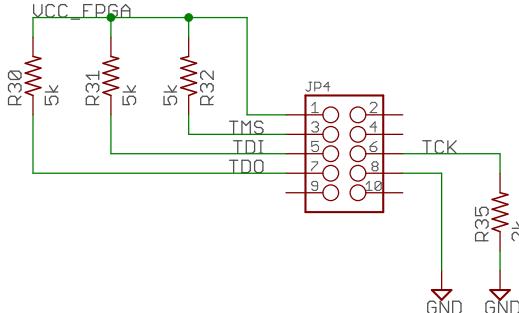
VCCIO3



## POWER



## JTAG Programmer



## I/O Connections

U1-PORTR	PT6A	PT10A
	PT6B	PT10B
	PT6C	PT10C
	PT6D	PT10D
	PT7A/TDO	PT10C/JTAGENB
	PT7B/TDI	PT10D/PROGRAM
	PT7C/TCK	PT11A
	PT7D/TMS	PT11C/INITN
	PT9A/PCLKT0_1	PT11D/DONE
	PT9B/PCLKC0_1	
	PT9C/SCL/PCLKT0_0	
	PT9D/SDA/PCLKC0_0	

## MCU-FPGA Connections

### U1-PORTB

22	MCU_FPGA_1/28	PB12A	MCU_FPGA_12
24	MCU_FPGA_2/29	PB12B	MCU_FPGA_13
26	MCU_FPGA_3/30	PB12C	MCU_FPGA_14
28	MCU_FPGA_4/31	PB12D	MCU_FPGA_15
30	MCU_FPGA_5/32	PB14A	
32	MCU_FPGA_6/34	PB14B	
34	MCU_FPGA_7/35	PB14C/SN	
36	MCU_FPGA_8/36	PB14D/SI/SISPI	
38	MCU_FPGA_9/37		
40	MCU_FPGA_10/38		
42	MCU_FPGA_11/39		
44		PB10A	
46		PB10B	
48		PB10C/PCLKT2_1	
49		PB10D/PCLKC2_1	

## Description:



FPGA

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## INPUTS

UCC\_XBEE/5

XBEE\_RESET/12

## COMMUNICATION

UART\_RX\_XBEE/11

UART\_TX\_XBEE/11

## Decoupling Capacitors

UCC\_XBEE/5

UART\_RX\_XBEE

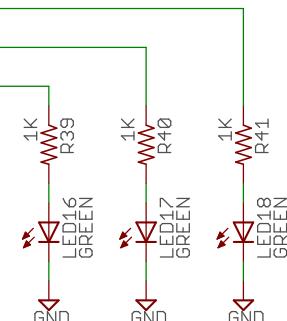
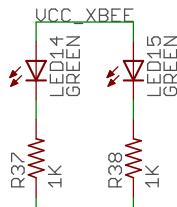
UART\_TX\_XBEE

RSSI

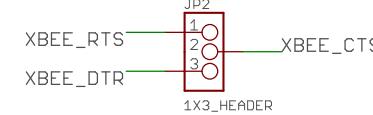
STATUS\_LED

ASSOCIATE\_LED

NOTE: Do not populate  
for reduced current



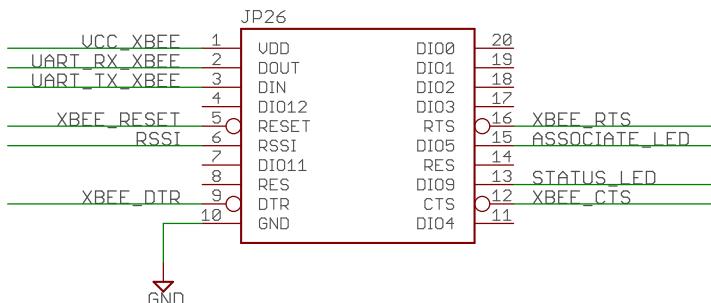
## XBee Update



NOTE: Use to update software  
on XBee SOC

NOTE: Populate J2 only if XBee  
upgrades are needed

## XBee



NOTE: This module can be swapped for any module that is pin compatible with XBee.  
For example the WiFi or RF modules by digi can be placed here.

NOTE: Minimum connections: VCC, GND, DOUT & DIN

NOTE: Minimum connections for updating firmware: VCC, GND, DIN, DOUT, RTS & DTR

## Description:



Wireless: XBee

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## INPUTS

+BAT/5

## OUTPUTS

RTC\_INT1/11

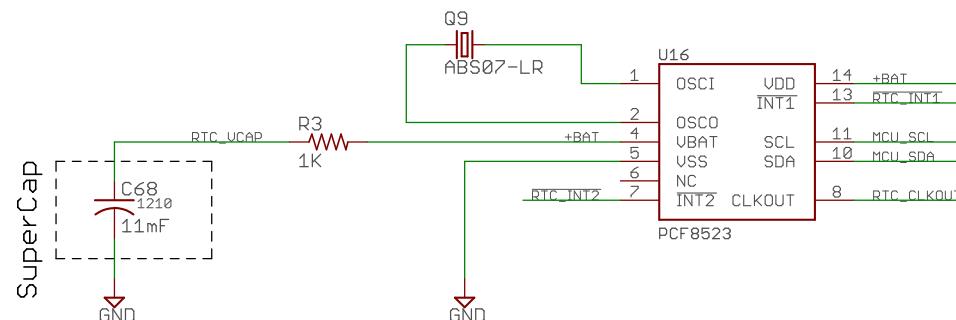
RTC\_INT2/11

## COMMUNICATION

MCU\_SDA/11

MCU\_SCL/11

# Real Time Clock



## TEST POINTS

TP41  
RTC\_CLKOUT  
TP42  
RTC\_INT2  
TP40  
RTC\_INT1

### Description:



Real Time Clock

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NOTE: Resistor used to provide current limiting to the capacitor.  
Larger resistor = longer RC time constant = longer time to charge

NOTE: At ambient temperature the average supply  
is 150nA. The maximum supply current is 3.6uA.

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

## INPUTS

EINK\_RST/12  
DISPLAY\_D/C/11  
SPI\_CS\_DISPLAY/11

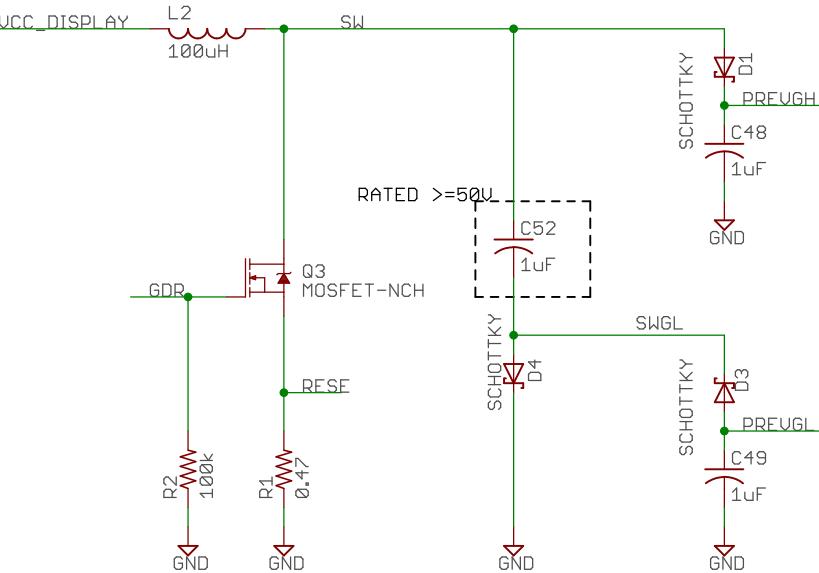
## OUTPUTS

EINK\_BUSY/12

## COMMUNICATION

SPI\_CLK/11  
SPI\_MOSI/11

## Power Converter



RATED >= 50V

C44 1uF

C45 1uF

GND

1 2 3 4 5 6 7 8

A

A

B

B

C

C

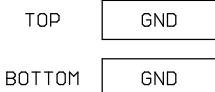
D

D

E

E

Stackup



Description:



Notes: Mechanical

Masters Project

4/3/2020 11:35 AM

Sean Alling

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Rev: U3

1 2 3 4 5 6 7 8

A  
TP1: +BAT  
TP2: GND  
TP3: VCC\_USB  
TP4: VCC\_HDC1080  
TP5: VCC\_OPT3001  
TP6: VCC\_FPGA  
TP7: VCC\_XBEE  
TP8: VCC\_MEMORY  
TP9: VCC\_DISPLAY  
TP10: VCC MCU  
TP11: GND  
TP12: GND  
TP13: GND  
TP14: GND  
TP15: GND  
TP16: GND  
TP17: GND  
TP18: GND  
TP19: RST  
TP20: N\$139

A  
TP21: N\$131  
TP22: UART\_TX\_XBEE  
TP23: UART\_RX\_XBEE  
TP24: SPI\_CLK  
TP25: CHARGE\_STATUS  
TP26: SPI\_MOSI  
TP27: DISPLAY\_D/C  
TP28: SPI\_CS\_DISPLAY  
TP29: MCU\_SCL  
TP30: MCU\_SDA  
TP31: EINK\_RST  
TP32: EINK\_BUSY  
TP33: FLASH\_WP  
TP34: FRAM\_WP  
TP35: FLASH\_HOLD  
TP36: MCU\_SPI\_MISO  
TP37: MCU\_SPI\_CS  
TP38: MCU\_SPI\_CLK  
TP39: MCU\_SPI\_MOSI  
TP40: RTC\_INT1  
TP41: RTC\_CLKOUT  
TP42: RTC\_INT2

E  
Description:

Notes: Test Points	
Masters Project	
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1 2 3 4 5 6 7 8

A

A

B

B

C

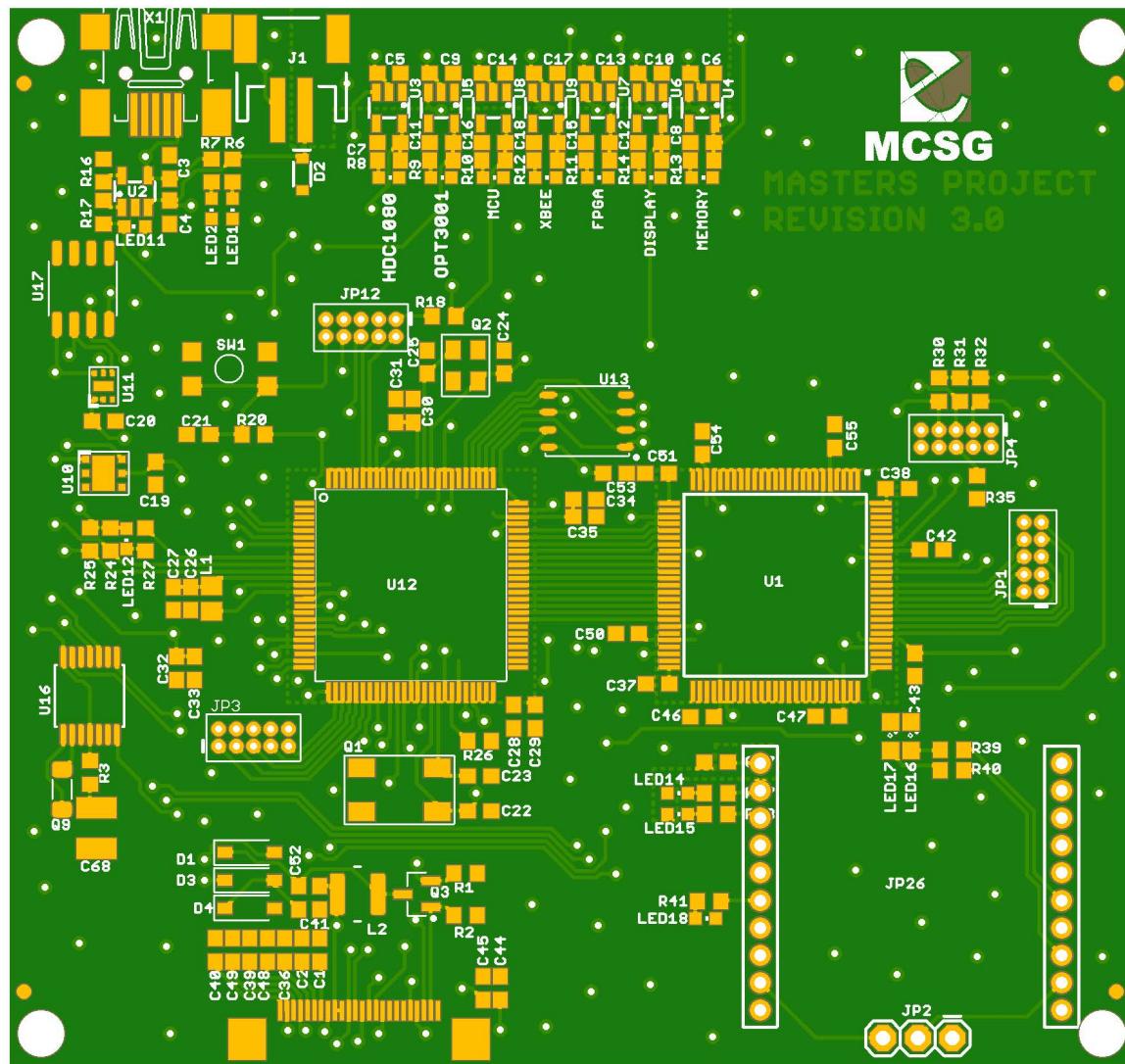
C

D

D

E

E



Description:



PCB: Top	
Masters Project	
4/3/2020 11:35 AM	Sean Alling
Sheet: 19/35	Rev: U3

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

A

A

B

B

C

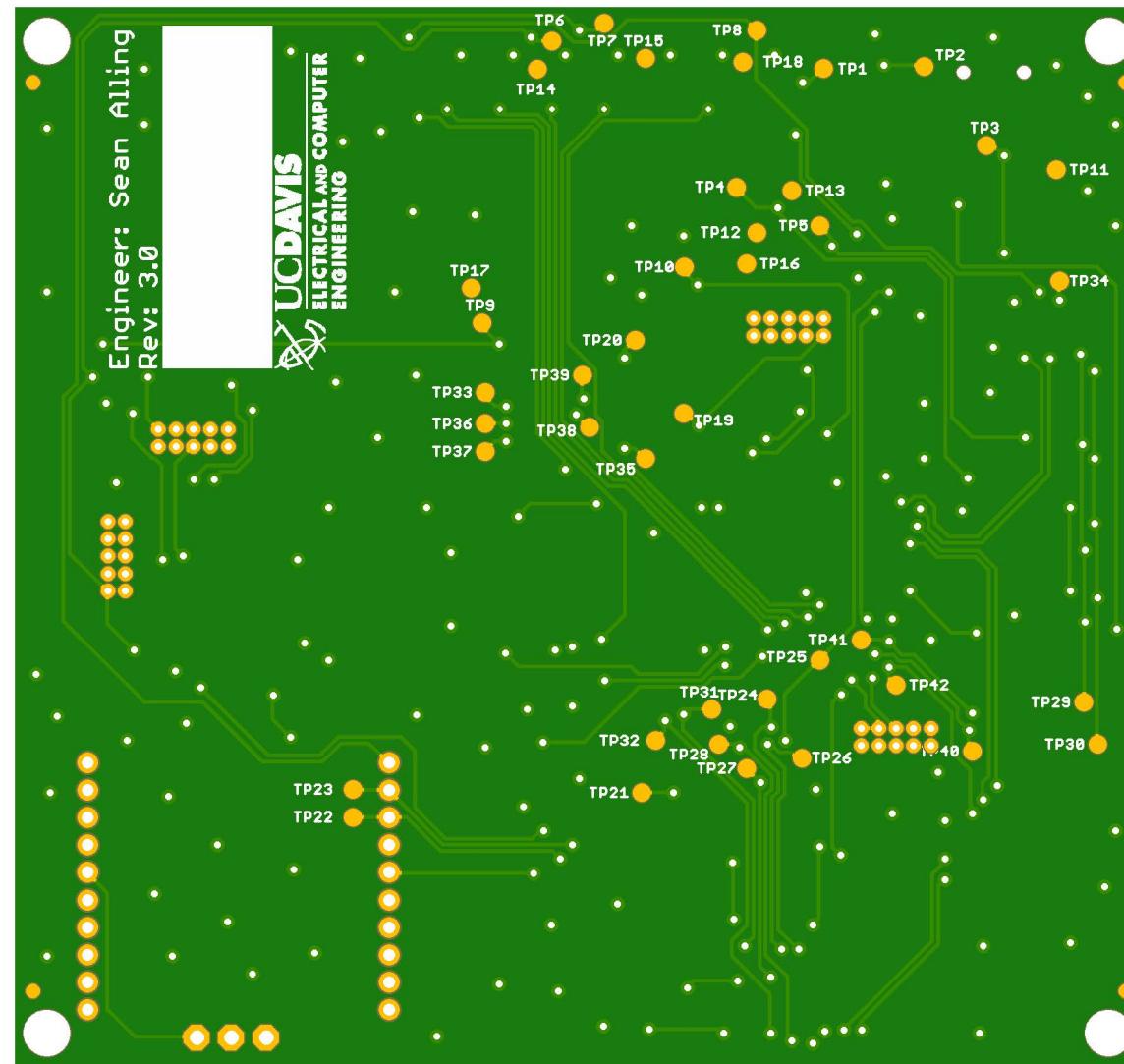
C

D

D

E

E



Description:



PCB: Bottom	
Masters Project	
4/3/2020 11:35 AM	Sean Alling
Sheet: 20/35	Rev: U3

1 2 3 4 5 6 7 8

1            2            3            4            5            6            7            8

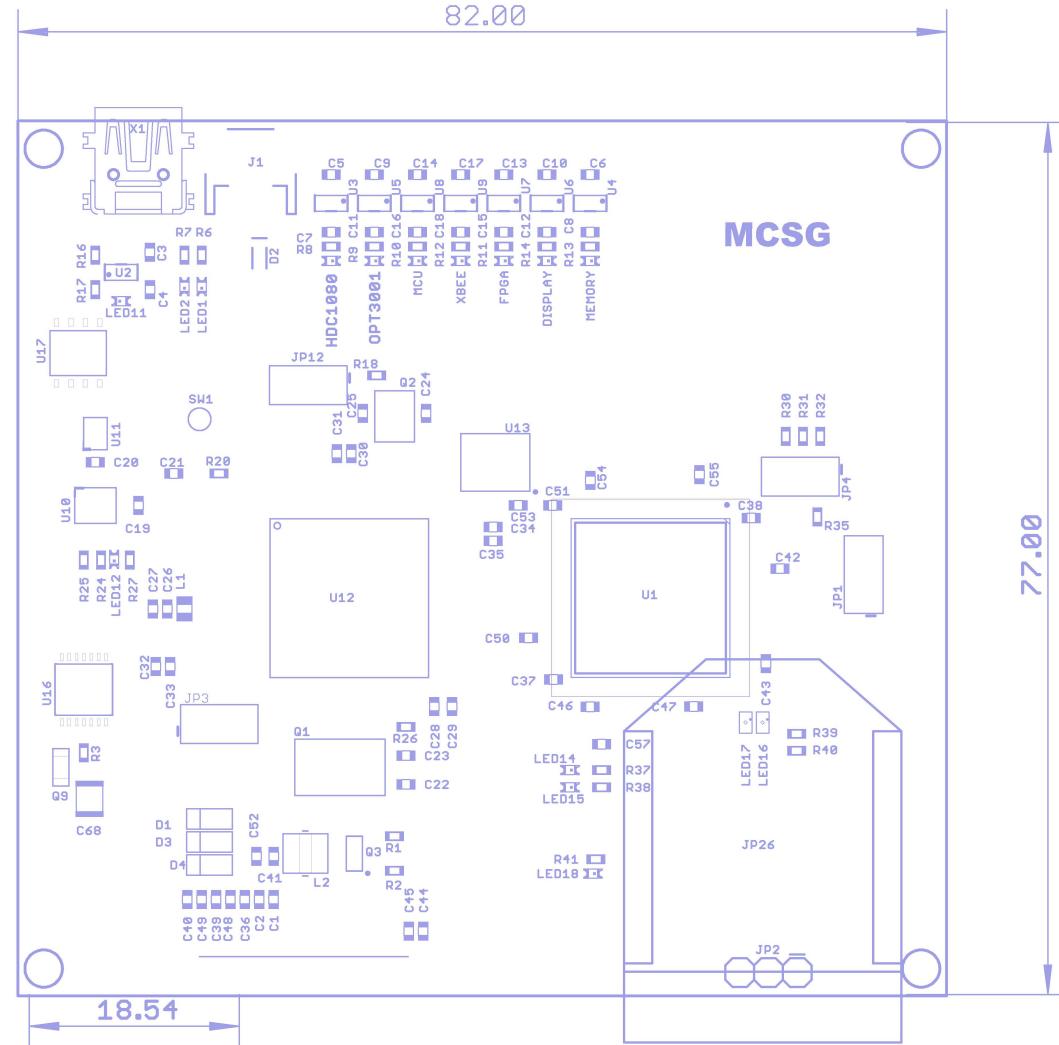
A

B

C

D

E



### Description:



## Assembly: Top

Masters Project

4/3/2020 11:35 AM

Sheet: 21/35

Sean Alling  
Rev: V3

1            2            3            4            5            6            7            8

1 2 3 4 5 6 7 8

A

A

B

B

C

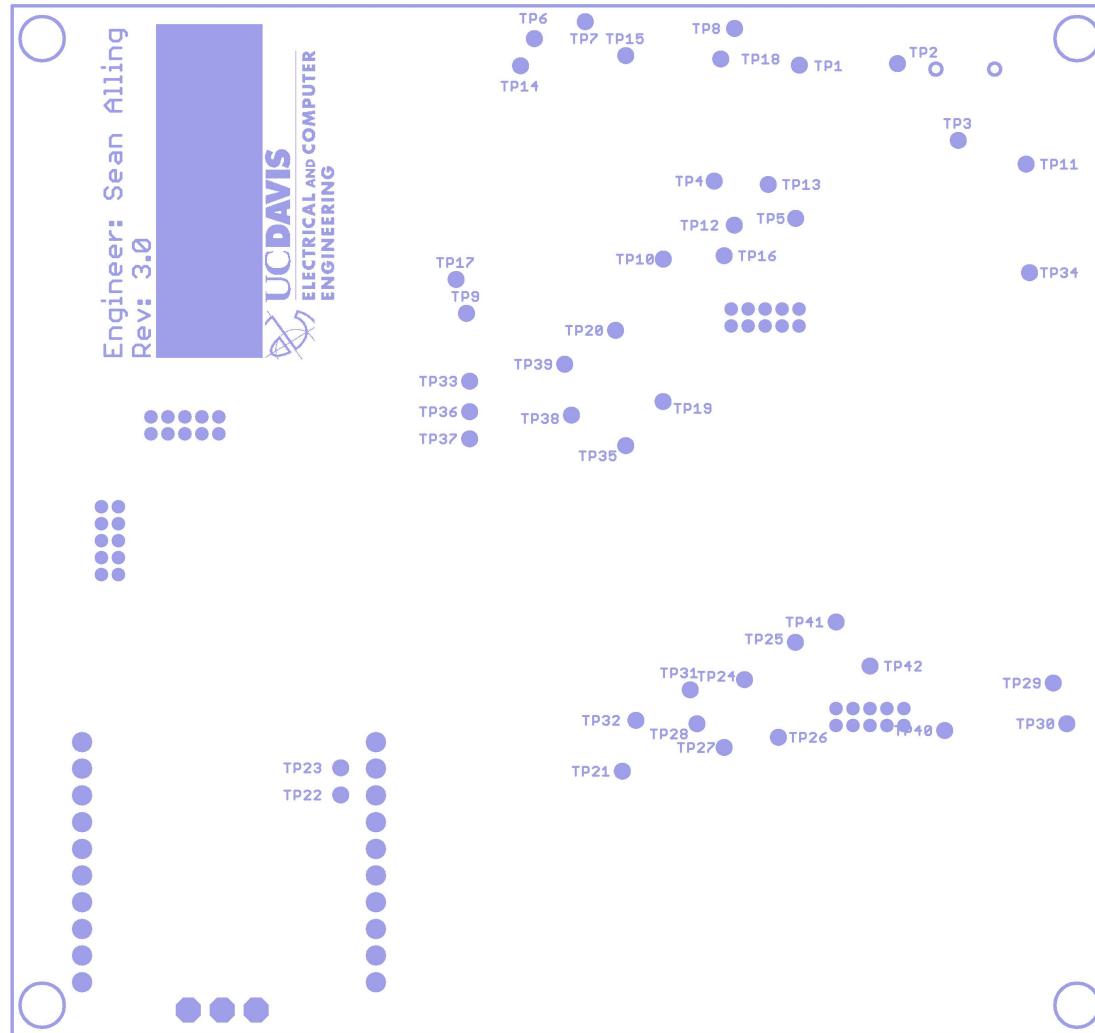
C

D

D

E

E



Description:



Assembly: Bottom

Masters Project

4/3/2020 11:35 AM

Sean Alling

Sheet: 22/35

Rev: U3

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

A

A

B

B

C

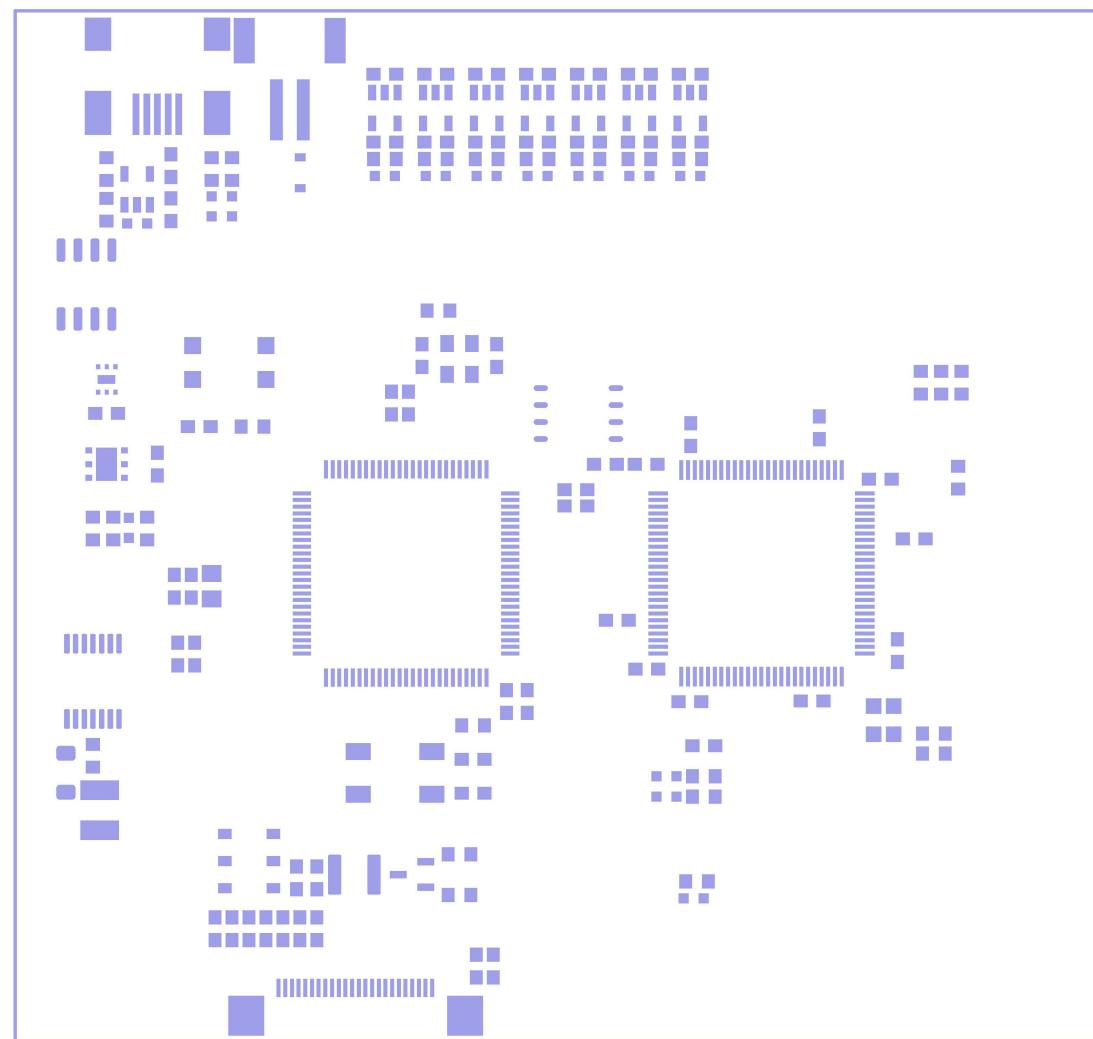
C

D

D

E

E



Description:



Stencil: Top

Masters Project

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Sean Alling

Sheet: 23/35

Rev: U3

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

A

A

B

B

C

C

D

D

E

E

N / A

Description:



Stencil: Bottom

Masters Project

4/3/2020 11:35 AM

Sean Alling

Sheet: 24/35

Rev: U3

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

A

A

B

B

C

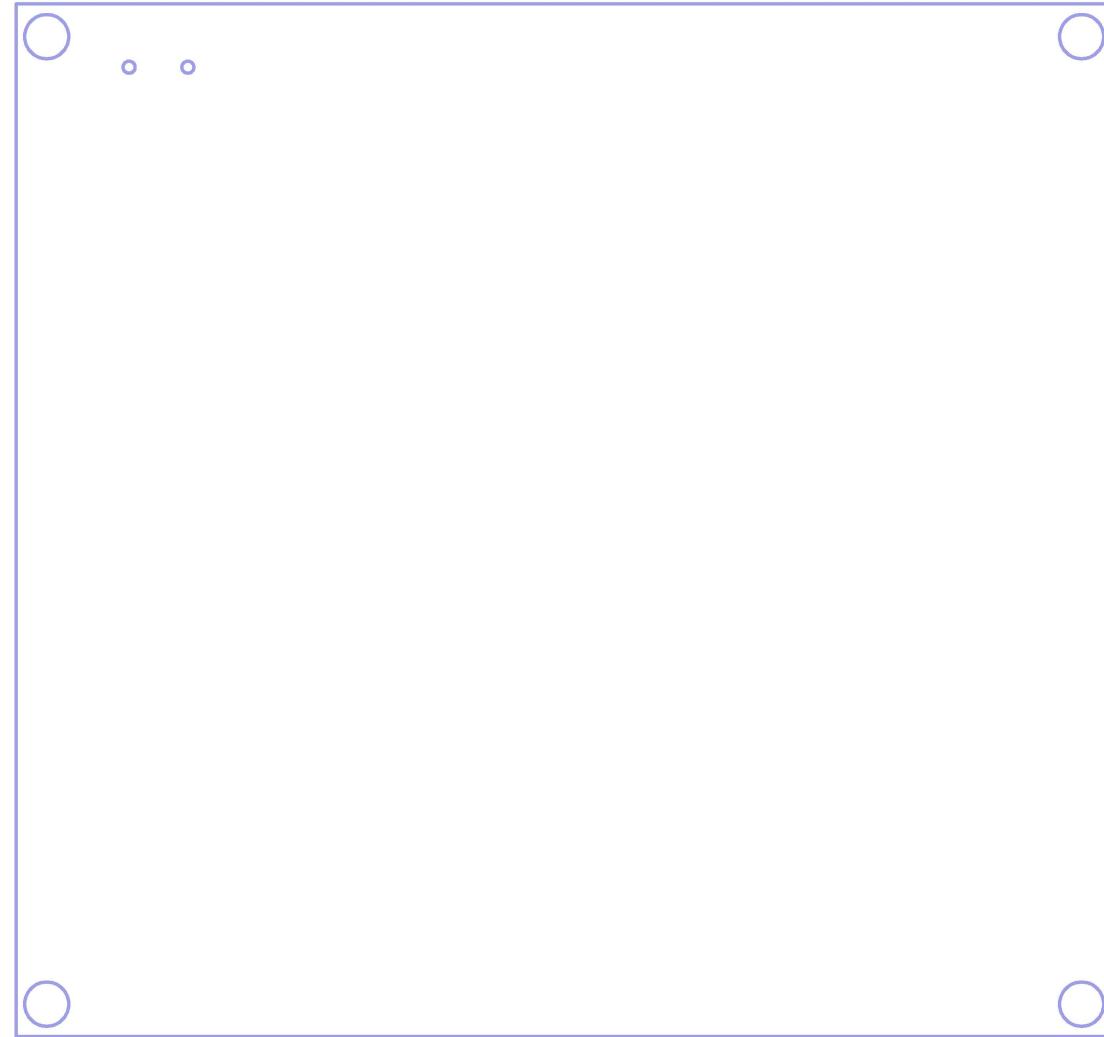
C

D

D

E

E



Description:



Gerber: Board Outline

Masters Project

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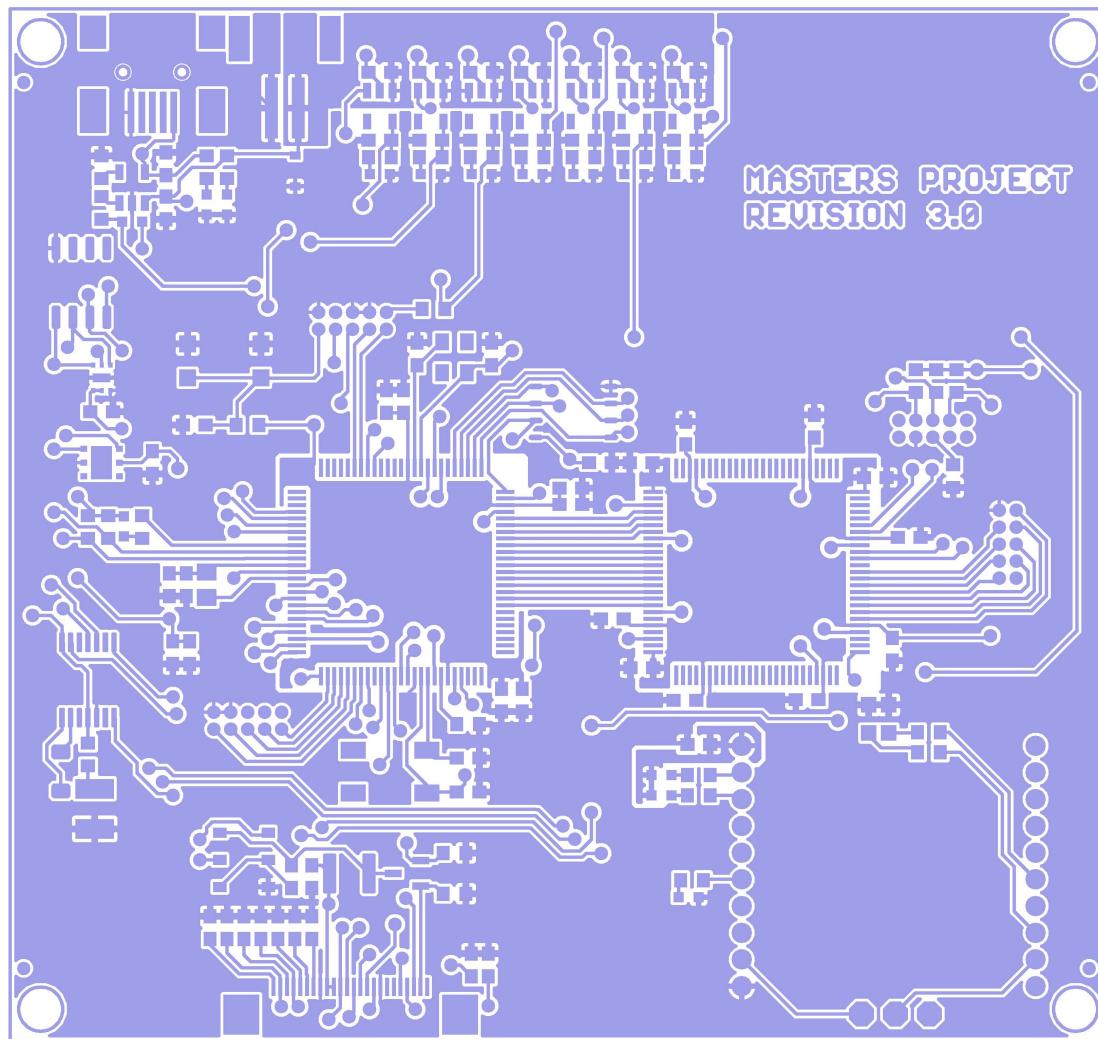
Sean Alling

Sheet: 25/35

Rev:U3

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8



A

B

C

D

E

A

B

C

D

E

Description:



Gerber: Top Copper

Masters Project

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Sheet: 26/35

Rev: U3

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

A

A

B

B

C

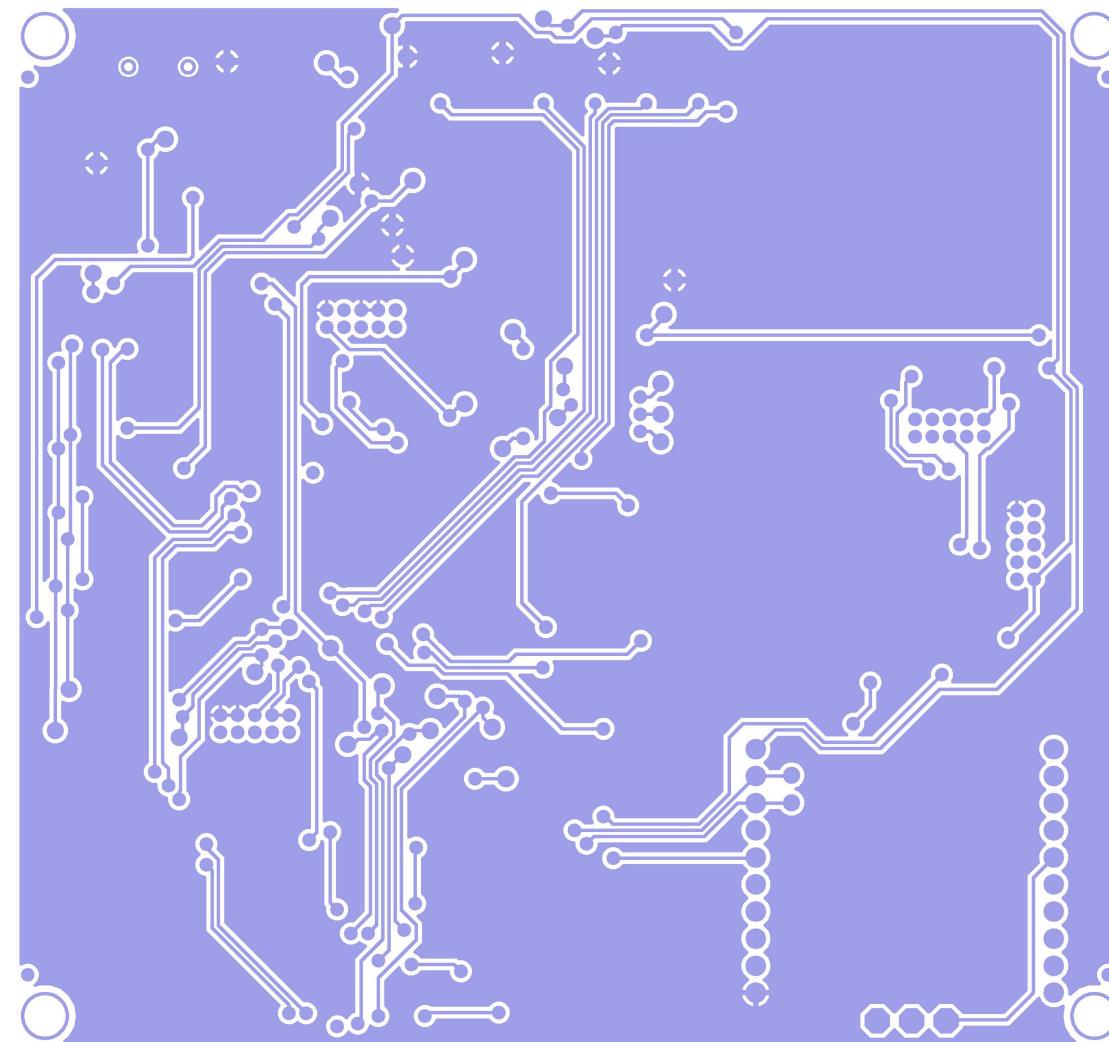
C

D

D

E

E



Description:



Gerber: Bottom Copper

Masters Project

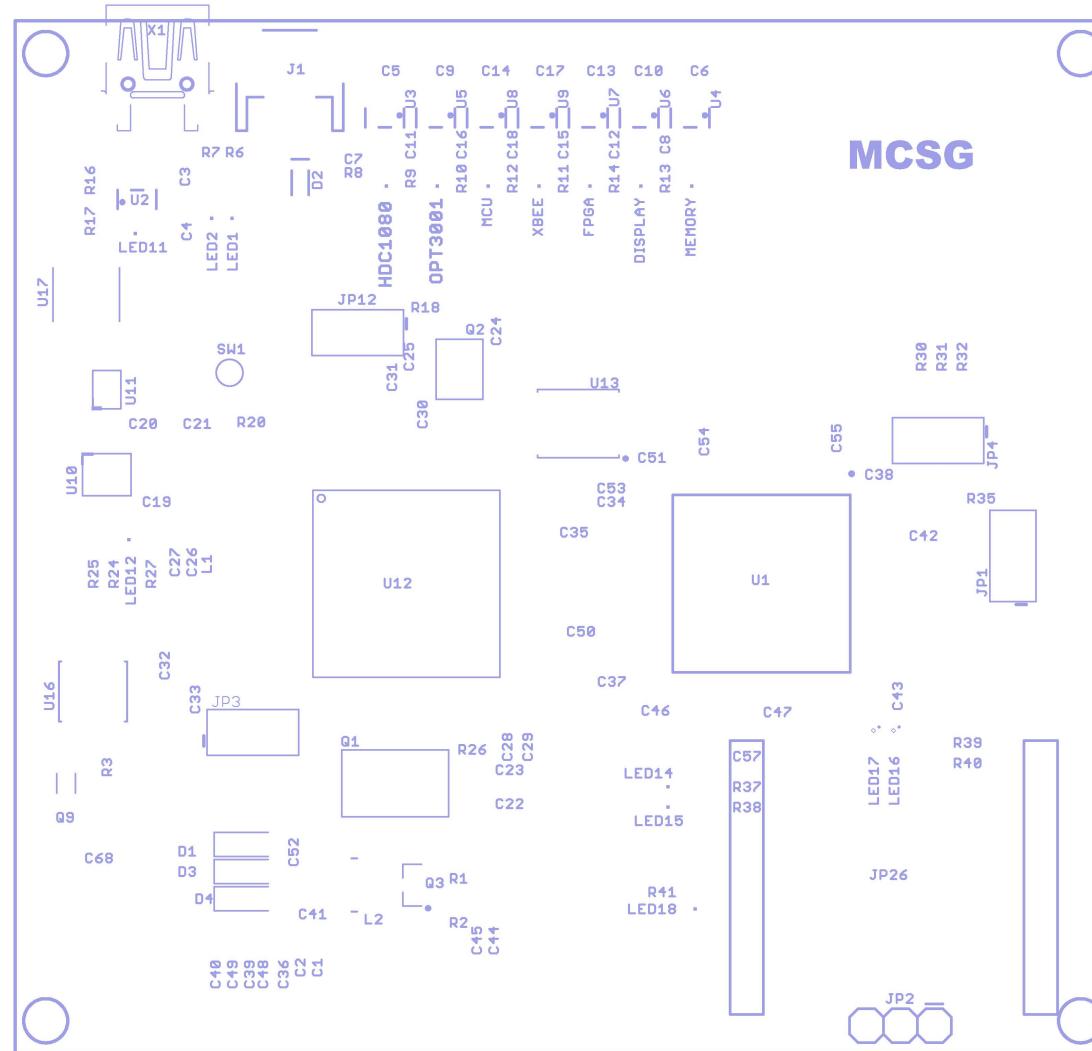
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1 2 3 4 5 6 7 8



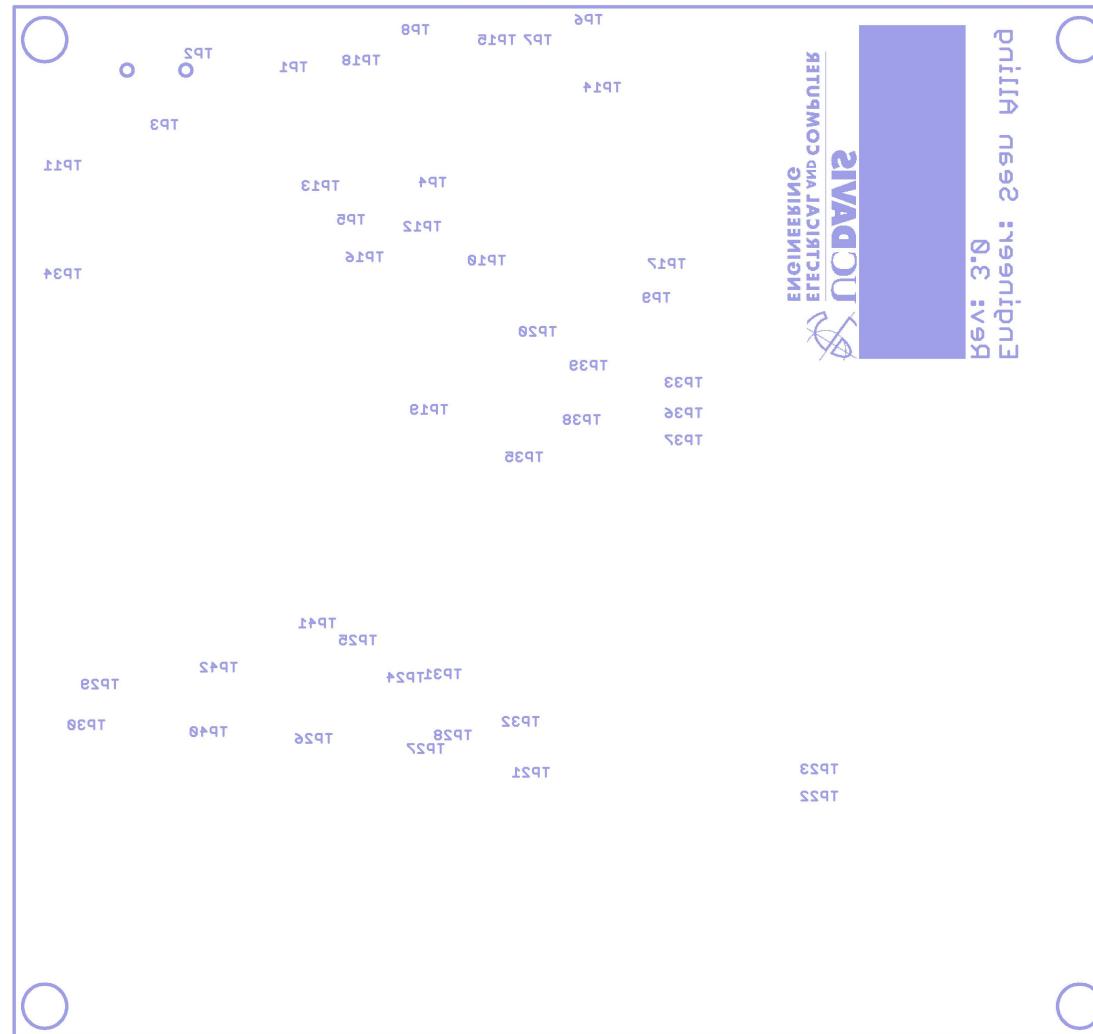
MCSG

## Description:



Gerber: Top Silkscreen	
Masters Project	
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1 2 3 4 5 6 7 8



Description:



Gerber: Bottom Silkscreen

Masters Project

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Sean Alling

Sheet: 29/35

Rev: U3

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

A

A

B

B

C

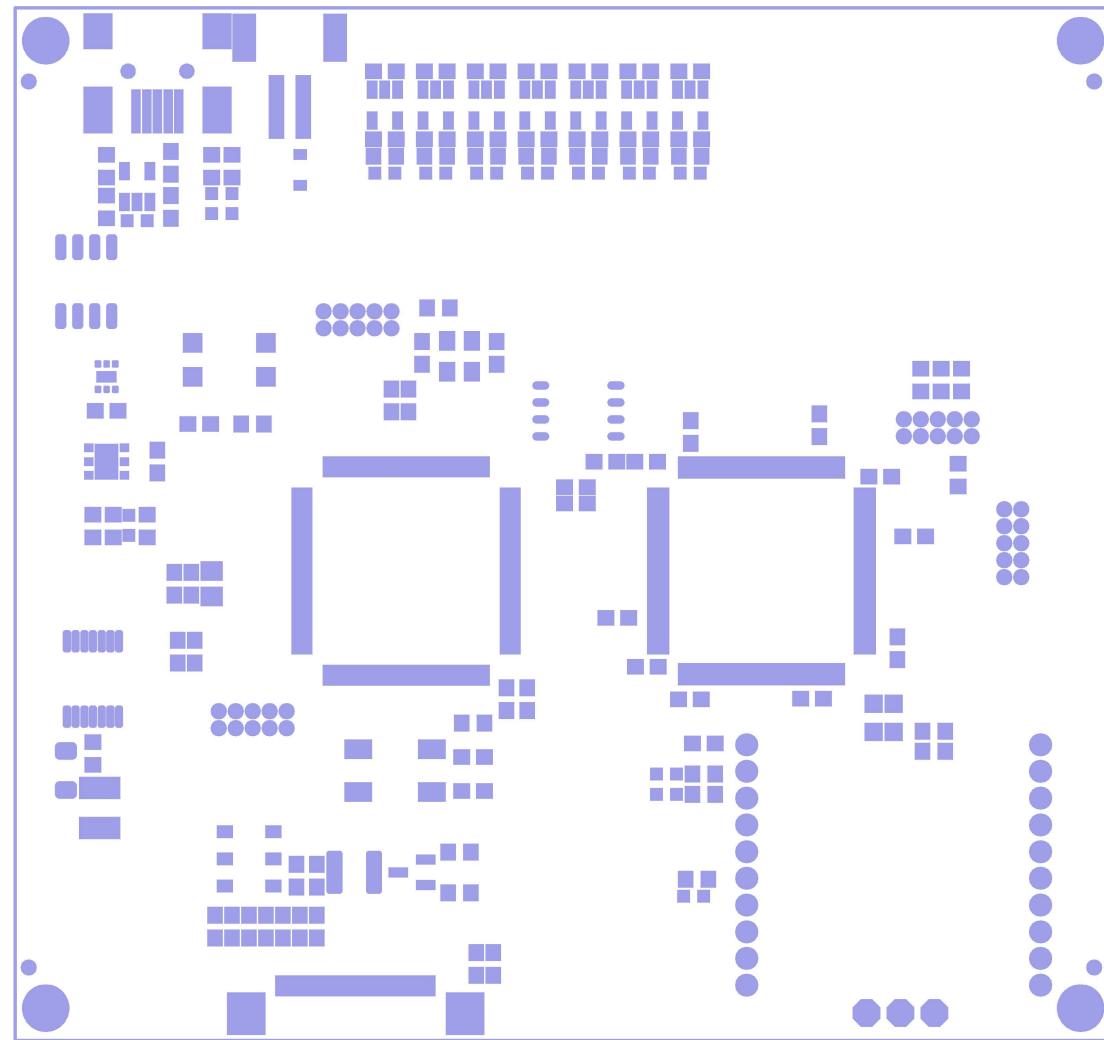
C

D

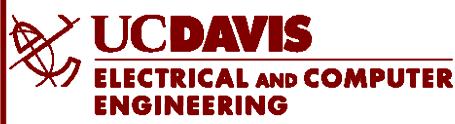
D

E

E



Description:



Gerber: Top Soldermask

Masters Project

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Sean Alling

Sheet: 30/35

Rev: U3

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

A

A

B

B

C

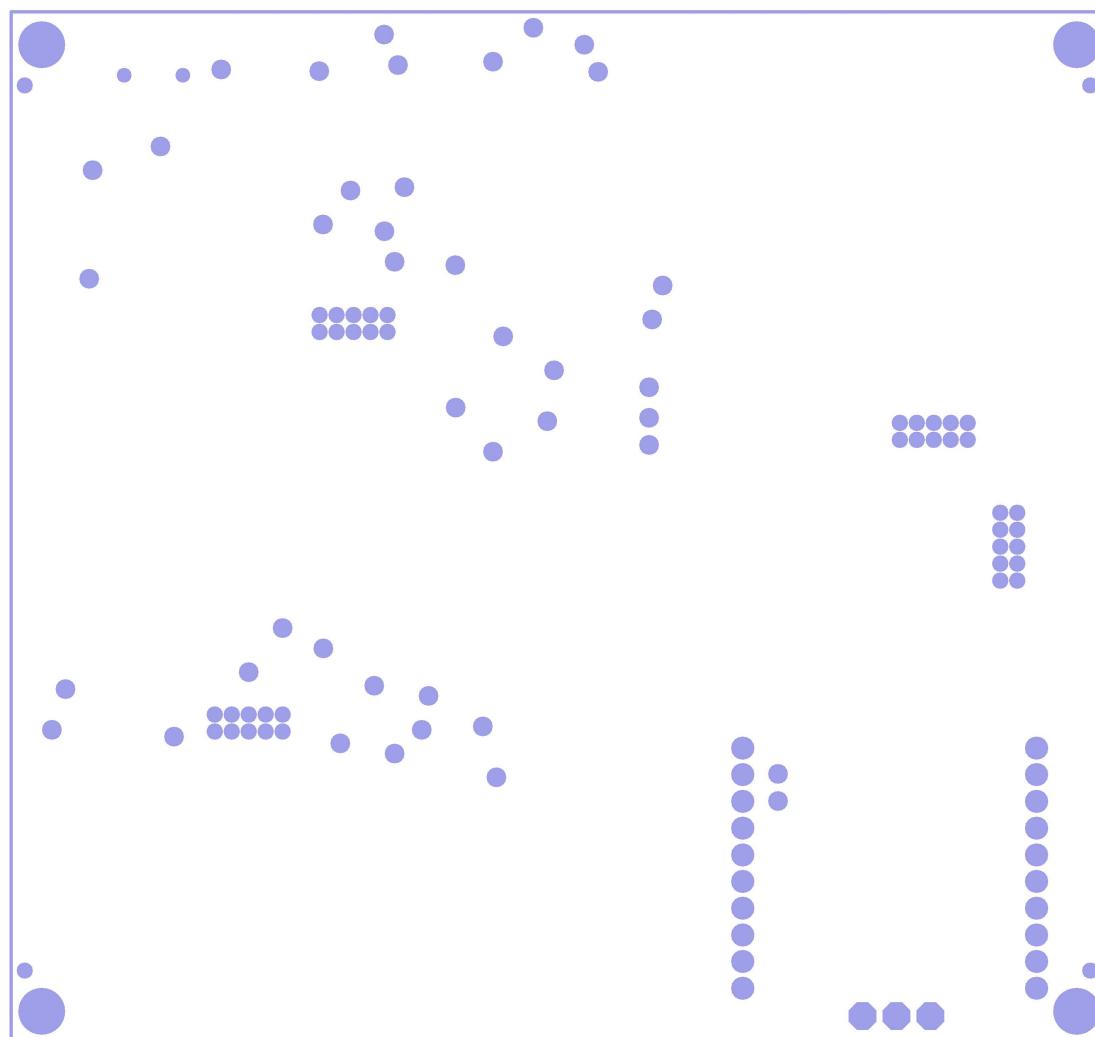
C

D

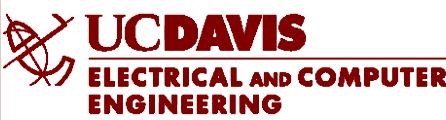
D

E

E



Description:



Gerber: Bottom Soldermask

Masters Project

4/3/2020 11:35 AM

Sean Alling

Sheet: 31/35

Rev: U3

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

A

A

B

B

C

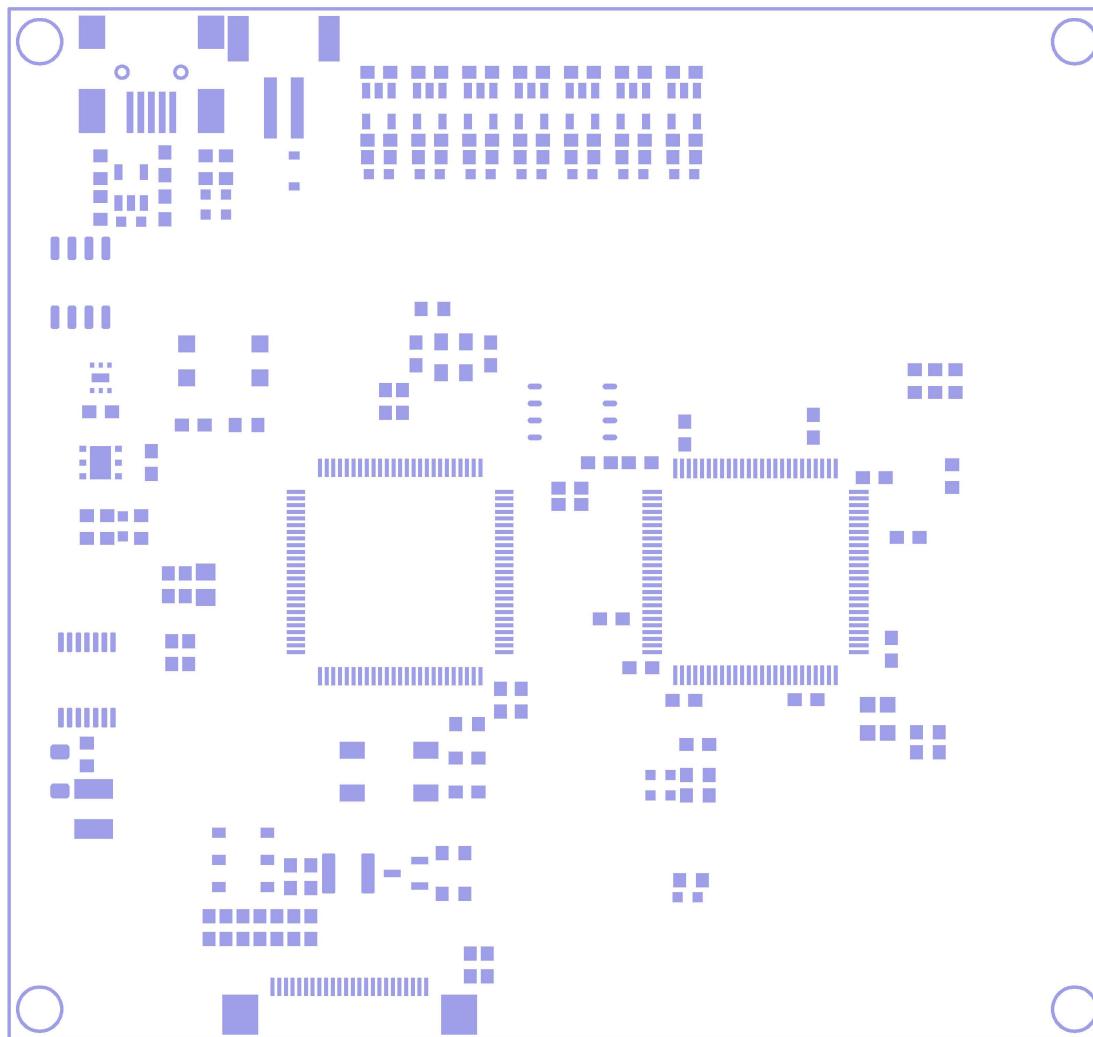
C

D

D

E

E



Description:



Gerber: Top Paste

Masters Project

4/3/2020 11:35 AM

Sean Alling

Sheet: 32/35

Rev: U3

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

A

A

B

B

C

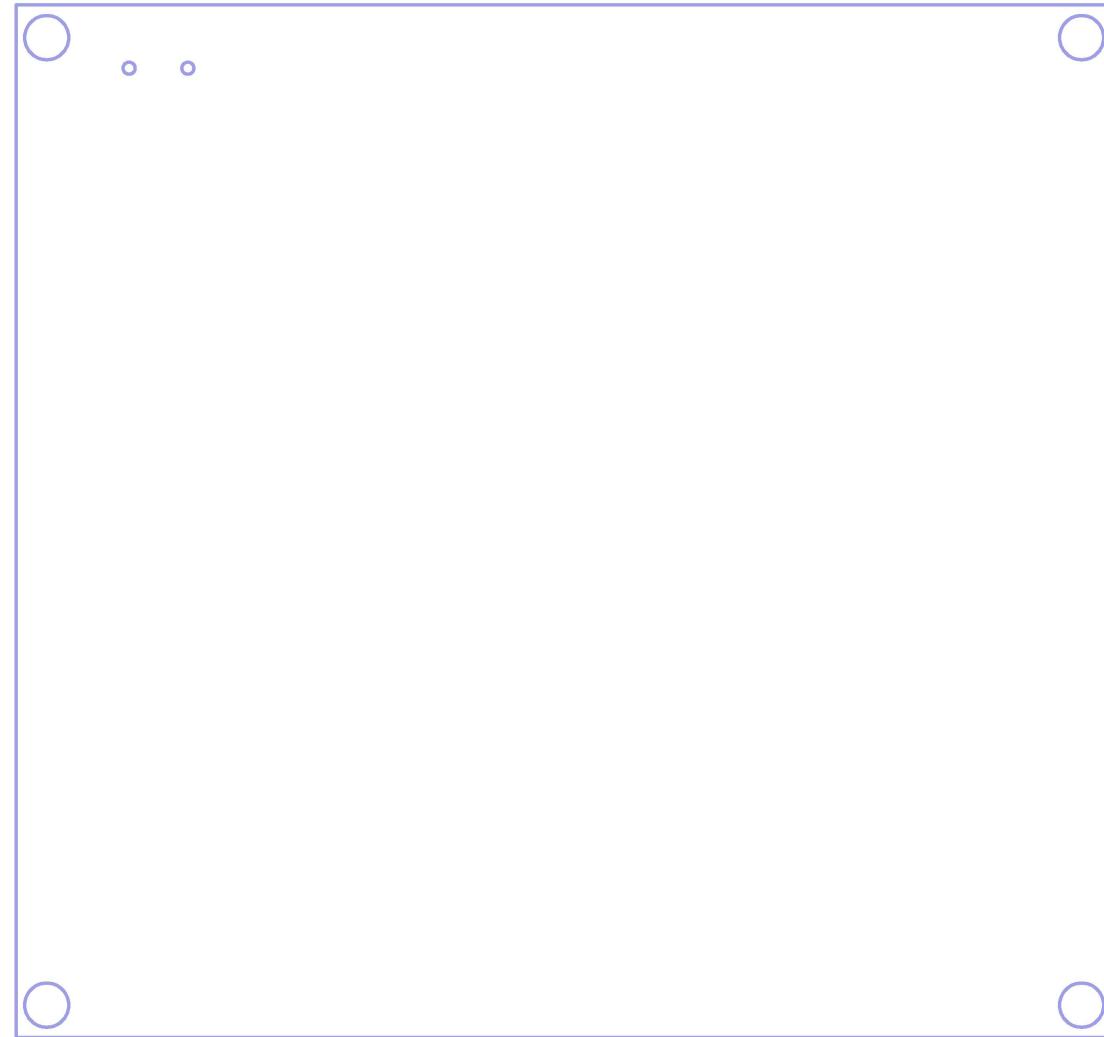
C

D

D

E

E



Description:



Gerber: Bottom Paste

Masters Project

4/3/2020 11:35 AM

Sean Alling

Sheet: 33/35

Rev: U3

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8

A

A

B

B

C

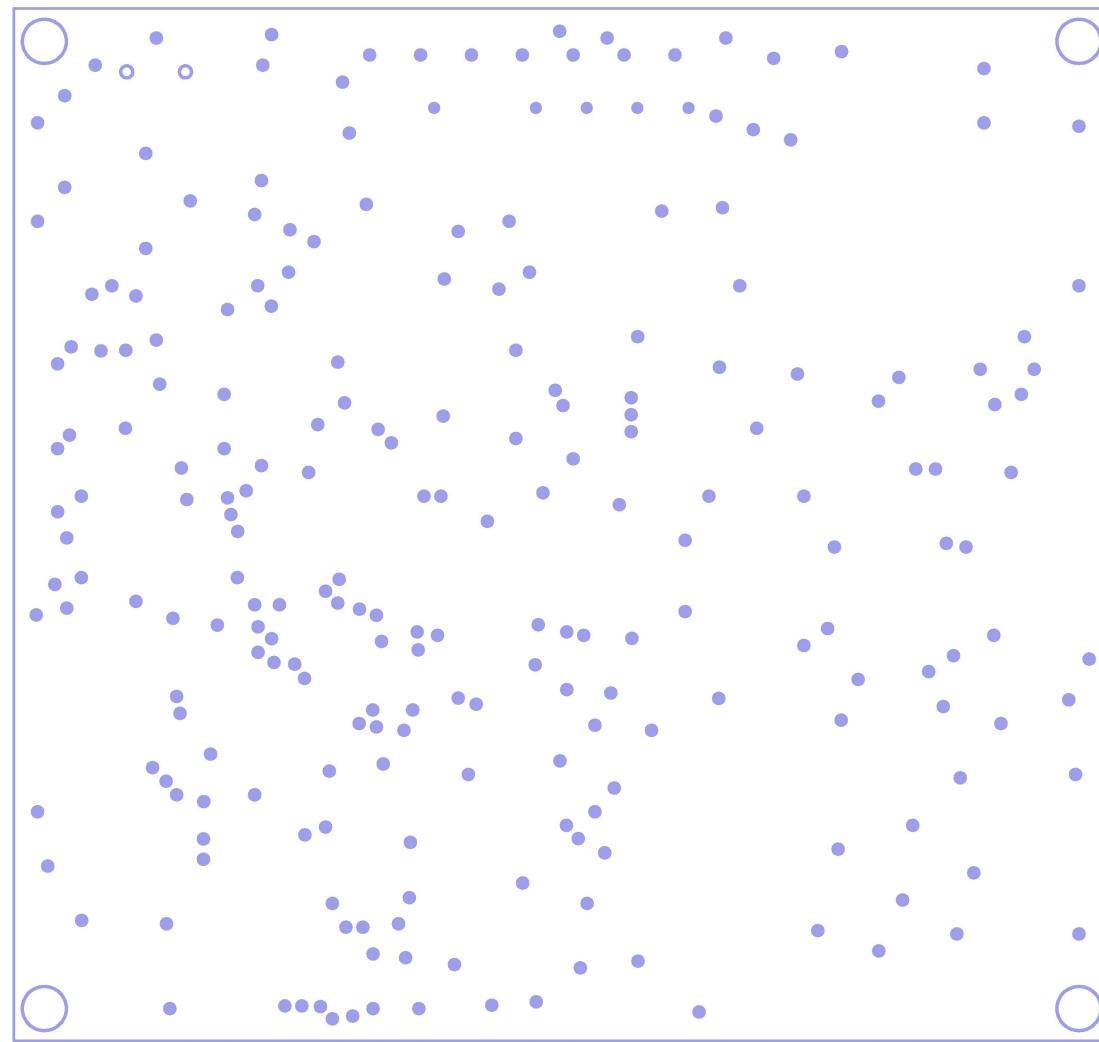
C

D

D

E

E



Description:



Drills: PTH & NPTH

Masters Project

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Sean Alling

Sheet: 34/35

Rev: U3

1 2 3 4 5 6 7 8

1 2 3 4 5 6 7 8



# MCSG

Description:



Sponsors		
Masters Project		
4/3/2020 11:35 AM	Sean Alling	
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1 2 3 4 5 6 7 8