RISC-V CPU Animation

The RISC-V CPU Animation is a learning tool built to convey CPU pipelining concepts and techniques as well as other computing concepts such as a calling convention and parallel execution via an implementation of the official RISC-V (pronounced "risk five") ISA (instruction set architecture). The animation is designed to be of optimum benefit to students learning about CPU architecture and also to instructors, allowing them to teach dynamic concepts via a non-static method as opposed to lecture slides and textbooks. The RISC-V CPU Animation is particularly designed to complement the Trinity College Computer Science 3rd Year Module CSU34021 (Computer Architecture II).

The animation is built atop the pre-existing MIPS/DLX CPU Animation, already familiar to those students who have taken the CSU34021 (previously CS3021) module. The RISC-V CPU updates the instruction set of that animation to an adaptation of RISC-V, a new open source hardware ISA based on established RISC (reduced instruction set computer) principles. This more modern instruction set led to a morphing of the animation's pipeline and allowed for an expansion of the concepts covered by the animation. It is built using VivioJS, a C-like object-oriented language that compiles into JavaScript, to be run on any machine with a browser. It is the hope of the project that the RISC-V CPU Animation will be published freely online for anybody with an interest in the subject to use and learn from.