Sean Michael Manger

Watsonville, CA seanmanger22@gmail.com Personal Website & Project Portfolio 831-269-1918
Sean Manger SeanM25

Engineering Projects

- "Watch Your Step" platformer game with Verilog & Basys 3 FPGA
- Power Line Inspection with UAVs for UCSC
- Flight Sim in Python
- Simulated Toaster Oven using C & STM-32 Nucleo MCU
- Ground Bouce PCB

Please See my Personal Website & Project Portfolio linked above for further detail.

Engineering Skills & Professional Licenses

- **Programming Languages:**

  Python, **(Fully Proficent)** C, **(Fully Proficent)** C++, **(Fully Proficent)** Verilog HDL, **(Fully Proficent)** RISC-V Assembly, **(Fully Proficent)** Embedded Systems Development using C, **(Proficent)** Tcl Scripting **(Intermediate)**
- **Engineering Software:**

  AMD Vivado, **(Fully Proficent)** OnShape CAD, **(Intermediate)** MATLAB, Simulink, and the Control Systems Toolbox, **(Fully Proficent)** Cadence PSpice, **(Proficent)** Altium Designer **(Upper Intermediate)**
- **Business Skills & Licenses:**

  Microsoft Office, **(Fully Proficent)** Zoom, **(Fully Proficent)** Windows & macOS, **(Fully Proficent)** LaTeX, **(Fully Proficent)** Linux, **(Intermediate)** Soldering Electrical Components,**(Intermediate)** FAA Commercial Licensed Small UAS Pilot.

Education

University of California, Santa Cruz *Expected: Mar. 2026*
Pursuing Bachelor's of Science in Electrical Engineering

- Current GPA: 3.61 **(Dean's List Fall 2024)**
- Relevent Coursework: **Feedback Control Systems, UAV Theory & Controls, Analog Electronics, Logic Design, High-Speed Digital Design, Signals & Systems, Properties of Materials, Embedded C Programming**

Cabrillo College, Aptos, CA *Aug. 2019 - Dec. 2023*
AS Computer Science, AS Physics, AS Mathematics, AA Liberal Arts and Science

- Cumulative GPA: 3.75

Relevant Work & Lab Experience

Hardware Systems Collective Lab Engineer & Researcher *Santa Cruz, CA*
University of California *Jul. 2025 – Present*

- I am working with Prof. Dustin Richmond researching cybersecurity vulnerabilities using FPGAs. Over the summer, I successfully implemeted and tested a time-to-digital converter design on a ZUBoard 1CG FPGA.
- For a senior thesis, I am characterizing the behavior of our time-to-digital converter under different conditions. This involves working with MMCM registers and gathering data using pandas. I then perform a statistical analysis of route behavior over time, and plot histograms and scatter plots using the gathered data.

Baskin Engineering Course Reader *Santa Cruz, CA*
University of California *Sept. 2024 – Present*

- Currently the Course Reader for CSE-100 **Logic Design**. I have also been the reader for ECE-101 **Intro to Electronic Circuits** and ECE-102 **Properties of Materials**
- I have graded Homeworks, Midterms, and Final Exams. I worked with each Professor to ensure fair grading standards for every student.

Physics Learning Center & STEM Center Tutor *Aptos, CA*
Cabrillo College *Jan. 2022 – Dec. 2023*

- I assisted students during my tenure in the Cabrillo STEM Center with any questions & problems related to Math, Physics, Computer Science, Electronic Circuits, etc.
- I checked off students' weekly PLC Assignments, which were conceptual Physics assignments, for completeness and accuracy.
- TA for Phys 4A **Classical Mechanics** and Phys 4B **Electricity & Magnetism**

Languages

English	**Native**
Russian	**Elementary Level**
Spanish	**Limited Working Level**