Sean Michael Manger

Watsonville, CA seanmanger22@gmail.com Personal Website & Project Portfolio 831-269-1918
Sean Manger SeanM25

Engineering Projects

- "Watch Your Step" platformer game with Verilog & Basys 3 FPGA
- Flight Sim in Python
- Simulated Toaster Oven using C & STM-32 Nucleo MCU
- Ground Bouce PCB

Please See my Personal Website & Project Portfolio linked above for further detail.

Engineering Skills & Professional Licenses

- **Programming Languages:**

  Python, **(Fully Proficent)** C, **(Fully Proficent)** C++, **(Fully Proficent)** Verilog HDL, **(Fully Proficent)** RISC-V Assembly, **(Fully Proficent)** Embedded Systems Development using C, **(Proficent)** Tcl Scripting **(Intermediate)**
- **Engineering Software:**

  AMD Vivado, **(Fully Proficent)** OnShape CAD, **(Intermediate)** MATLAB, Simulink, and the Control Systems Toolbox, **(Fully Proficent)** Cadence PSpice, **(Proficent)** Altium Designer **(Upper Intermediate)**
- **Business Skills & Licenses:**

  Microsoft Office, **(Fully Proficent)** Zoom, **(Fully Proficent)** Windows & macOS, **(Fully Proficent)** LaTeX, **(Fully Proficent)** Linux, **(Intermediate)** Soldering Electrical Components,**(Intermediate)** FAA Commercial Licensed Small UAS Pilot.

Education

University of California, Santa Cruz *Expected: Mar. 2026*
Pursuing Bachelor's of Science in Electrical Engineering

- Current GPA: 3.61 **(Dean's List Fall 2024)**
- Relevent Coursework: **Feedback Control Systems, UAV Theory & Controls, Analog Electronics, Logic Design, High-Speed Digital Design, Signals & Systems, Properties of Materials, Embedded C Programming**

Cabrillo College, Aptos, CA *Aug. 2019 - Dec. 2023*
AS Computer Science, AS Physics, AS Mathematics, AA Liberal Arts and Science

- Cumulative GPA: 3.75

Relevent Work & Lab Experience

Hardware Systems Collective Lab Engineer & Researcher *Santa Cruz, CA*
University of California *Jul. 2025 – Present*

- I am working with Prof. Dustin Richmond researching cybersecurity vulnerabilities using FPGAs. Over the summer, I successfully implemeted and tested a time-to-digital converter design on a ZUBoard 1CG FPGA.
- For a senior thesis, I am characterizing the behavior of our time-to-digital converter under different conditions. This involves working with MMCM registers and gathering data using pandas. I then perform a statistical analysis of route behavior over time, and plot histograms and scatter plots using the gathered data.

Languages

English	**Native**
Russian	**Elementary Level**
Spanish	**Limited Working Level**