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# E344 Report

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Report submitted in partial fulfilment of the requirements of the module  
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and Electronic Engineering at Stellenbosch University.

August 12, 2022

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# Nomenclature

## Variables and functions

$R_{sense}$  Resistor used to in series with the load to measure current

## Acronyms and abbreviations

op amp Operational amplifier

# Chapter 1

## Literature survey

### 1.1. Operational amplifiers

#### Operational amplifiers: limitations and considerations

There are many practical limitations to operational amplifiers in comparison to the ideal model. The limit on the common mode voltage is a concern as the limit is usually around the rail voltage and since the negative rail will be ground and the common mode voltage will be close to 0 the data sheet should be consulted to ensure normal operation of the op amp [3].

A significant consideration is the offset voltage between the inputs of the opamp as when the inputs are equal (no current is being given to the load) there will be an offset voltage on the order of mV which is a similar magnitude to the relevant voltages [4]. This will result in significant output voltages at no load. However a negative feedback will greatly reduce the impact of input offset voltage and current [4].

The output voltage won't be able to go all the way to the rail voltages. Therefore there will be some output voltage when there is no current through the load due to the output not able to go below a certain voltage above ground.

#### Operational amplifier configurations

There are many different configurations for operational amplifiers, this section will cover 4 basic configurations that could be useful for the current sensor.

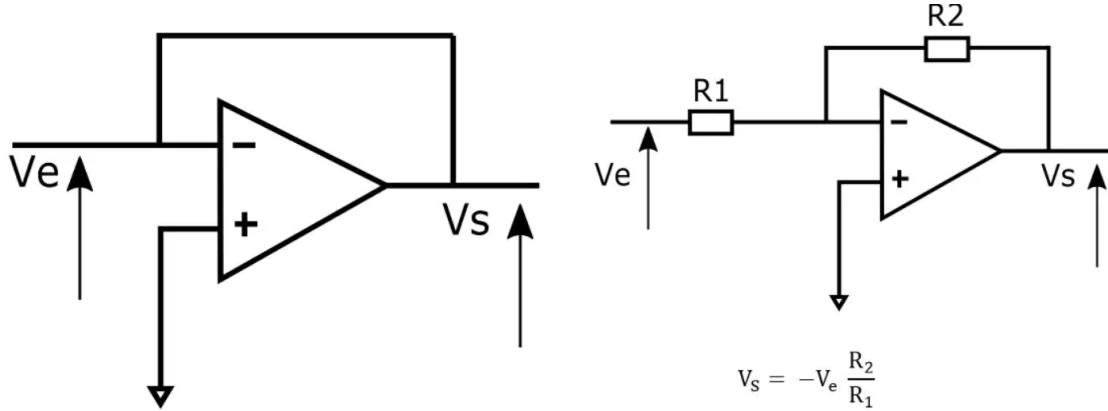
The simplest circuit is the voltage follower, it requires no other components and causes the output voltage to track the input voltage. The op amp in this configuration provides a large input impedance and very low output impedance which can allow signals to pass between logic components without them loading each other and can be used to stabilize a voltage divider [5].

The inverting op amp is a configuration where the output is connected to the inverting input terminal using a resistor, there is a second resistor connecting this terminal to the circuit input. The non-inverting input is connected to ground. This configuration results in a gain equal to the negative of the ratio between the two resistors. The negative gain cause the output to be exactly out of phase with the input [5].

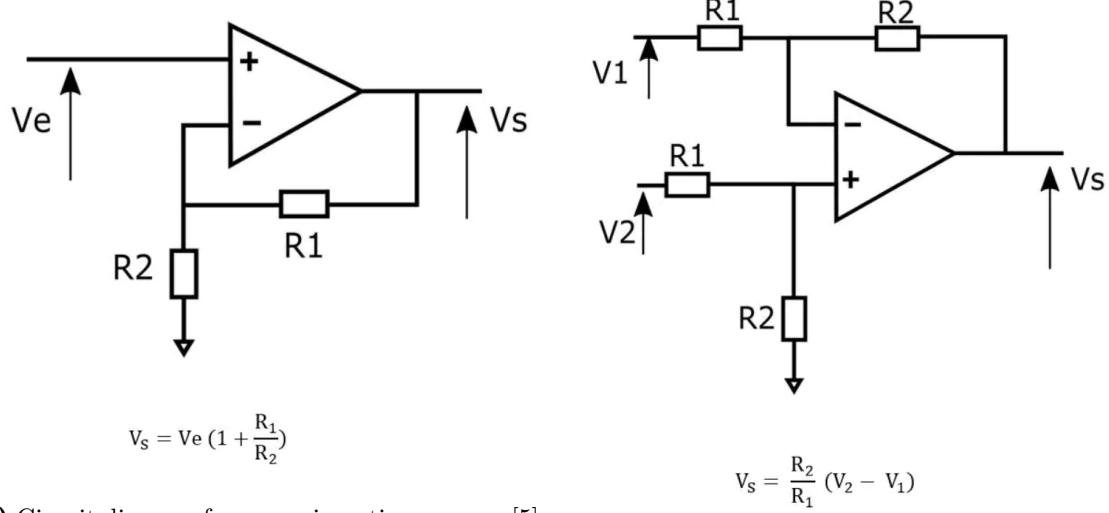
The non-inverting op amp configuration is similar to the inverting amplifier except the input is connected directly to the non-inverting input and the inverting input terminal has a resistor connecting it to the ground. This results in the gain being equal to 1 plus the ratio

between the two resistors [5].

The differential amplifier is similar to the inverting amplifier, but instead of connecting the non-inverting input to ground a second signal is connected to the input of this terminal through a resistor of the same value as the other terminal. This results in the output being the difference between the two signals scaled by the ratio of the feedback resistor to the input resistor. This configuration is good at filtering out noise common to both input terminals [5].



**(a)** Circuit diagram for a voltage follower [5]    **(b)** Circuit diagram for an inverting op amp [5].



**Figure 1.1:** Circuit diagrams of 4 op amp configurations

## 1.2. Current sensing

There are many different techniques to measure current. Both invasive and non invasive methods each with their own advantages and disadvantages that make them suitable for different situations. An invasive current sensor negatively affect the system and decreases performance whereas a non-invasive current sensor doesn't affect the operation of the system at a meaningful level.

### Hall effect

The Hall effect current sensor is a non invasive method of current sensing that uses the magnetic field generated around a current carrying conductor [6]. This magnetic field creates a voltage across the material of the sensor. Hall effect sensors measure this voltage to determine the current flowing in a conductor [7]. There are many advantages to using a Hall effect sensor however, besides the amplifier circuit additional circuits are required and is more costly than other measurement methods [6].

### Rogowski coil

The Rogowski coil is a non invasive current sensing method that uses a helical shaped coil that is wrapped around the conductor that you want to measure current in. The coil outputs a voltage depending on the rate of change of current through the conductor, this requires an integrator circuit to create an output voltage that is proportional to the current. The Rogowski coil is very useful for high frequency currents and does not require complex temperature compensation. However this method is only suitable for AC current [6].

### Shunt Resistor

The shunt resistor is the most common current sensing technique and uses a resistor in series with the current to be measured. This is a invasive current measuring method. The shunt resistor produces a voltage drop proportional to the current, however the resistance and hence the voltage must be kept low in order to reduce the power consumption. This requires a high gain amplifier circuit to increase the small voltages to meaningful levels. The shunt resistor is a very cost effective solution that works on both AC and DC however it creates a decrease in system efficiency and can't handle high currents due to power dissipation across the resistor. Thermal drift also results in error [6].

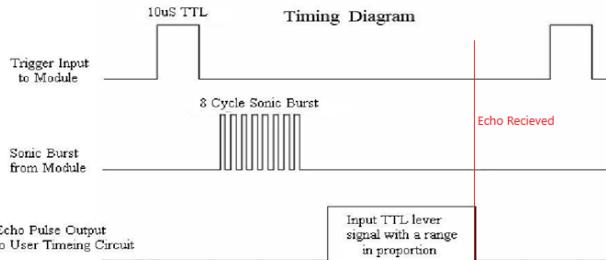
High-side vs low-side current sensing is only applicable for invasive methods like the shunt resistor. Low-side has the advantages of being simple and low cost and low input common mode voltage however it can't detect high current due to a short [8]. High-side current sensing removes the ground disturbance and can detect accidental shorts however it has a higher complexity and cost because the gain circuit must be able to handle high common mode voltages [8].

## 1.3. Ultrasonic range sensor

### 1.3.1. Interfacing with the ultrasonic range sensor

The datasheet of the HC-SR04 shows a 5 V supply is required and the sensor uses 15 mA when operating [1]. Which results in an operating power usage of 75 mW.

In order to trigger the sensor to send out a sonic pulse an input trigger is required for atleast 10  $\mu$ s at high TTL levels [1]. The trigger must be sent at least 60 ms apart to prevent false outputs due to the delayed echo [1]. See Figure: 1.2 for a timing diagram showing the relationship between the input trigger the sonic pulse and the output from the module.



**Figure 1.2:** Timing diagram for ultrasonic sensor [1]

The ultrasonic sensor determines the range of an object that it is pointed at by sending out a set of 8 sonic pulses at 40 kHz when triggered [1]. Once the set of pulse is sent the output is set to high until the sensor detects the return of pulse, at which point it drives the output low. With a regular interval trigger this results in a PWM output signal where the duty cycle corresponds to the distance between the sensor and the object it is facing. This distance is determined by using the speed of sound through air and half the time it takes for the echo to come back as shown in Equation: 1.1 [1].

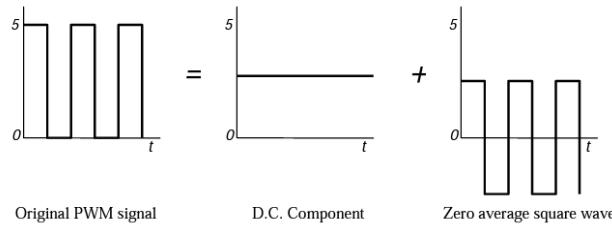
$$Distance = \frac{OutputHighTime \cdot SpeedOfSound}{2} \quad (1.1)$$

### 1.3.2. Converting PWM signals to analogue signals

A PWM signal can be treated as the sum of a DC signal and a square-wave of equivalent duty cycle, as shown in Figure: 1.3. Converting a PWM signal to its Fourier series equivalent shows that this DC component is equal to the amplitude of the PWM signal multiplied with the duty cycle [2].

The core concept behind getting a analogue signal from a PWM signal is to use a low pass filter to remove the higher frequency components and leave the DC component [2]. The frequency of the PWM signal determines the frequency of the first harmonic as this harmonic will occur at the same frequency of the PWM signal.

Since it is impossible to physically realise a idea low pass filter the cut-off frequency must be set lower than the frequency of the PWM signal. This results in a trade off between the attenuation of the ripple voltage caused by the first harmonic of the PWM signal and the frequency at which the duty cycle of the PWM signal can be varied [2]. Increasing the order of the filter result in a better approximation of ideal low pass filter and allows for the cut-off frequency to be increased without sacrificing attenuation of the first harmonic.



**Figure 1.3:** Decomposition of a PWM signal [2].

### 1.3.3. Digital to analogue converter opamp

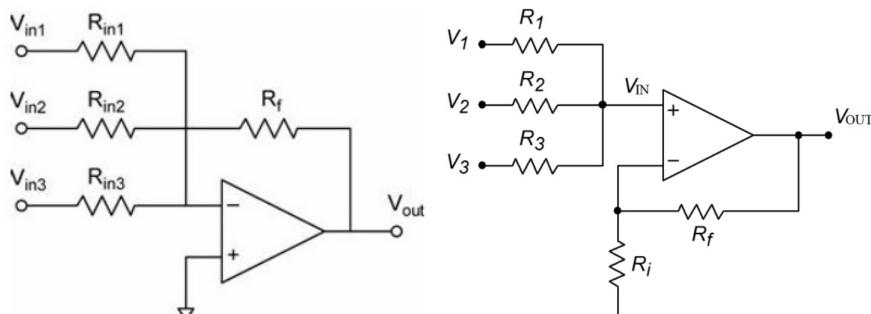
A summing amplifier works by combining several voltage inputs into one signal with no interference [9]. The most common summing amplifier configuration is the inverting summing amplifier shown in Figure: 1.4a. This configuration makes the inverting node ideal for summing voltages as the non-inverting node is connected to ground the inverting node is now "virtual ground" [9]. The gain for each input is given by the ratio between the feedback resistor and the input resistor.

A non-inverting summing amplifier is similar to the inverting one however the inputs are connected to the positive terminal of the opamp as shown in Figure: 1.4b. What makes this configuration less common is the fact that all inputs have an effect on all other inputs, this is due to the lack of "virtual ground" as seen in the inverting case [9]. The advantages of a non-inverting configuration are that the input impedance is much higher than the inverting case and that the input summing part of the circuit is not affected by the changes to the amplifier's closed loop gain [10].

Common mode voltage range is based on the rail voltages supplied to the op amp but the specifics vary from op amp to op amp. Non-inverting op amps with the positive input terminal connected to ground don't have to consider common mode voltage however if the op amp has a offset at this terminal or is in a non-inverting configuration the common mode voltage gain will restrict what inputs result in a linear output. Since the common mode range is based on the rail voltage to increase the input range the rail voltages should be increased.

Since the source for the binary signals are unideal they will have small output impedances, these sources typically can't drive high current. So in order to have most of the voltage drop occur across the summing circuit, the input impedance at the input terminals should be high.

Op amps are unable to source infinite current so if the receiving circuit has too low of an input impedance the op amp won't be able to sustain the desired voltage output.



(a) Circuit diagram for an inverting summing amplifier [9]. (b) Circuit diagram for a non-inverting summing amplifier [9].

**Figure 1.4:** Circuit diagrams of 2 summing opamp configurations

# Chapter 2

## Detail design

### 2.1. Current sensor

Currently being rewritten.

#### 2.1.1. Opamp configuration

#### 2.1.2. Opamp design

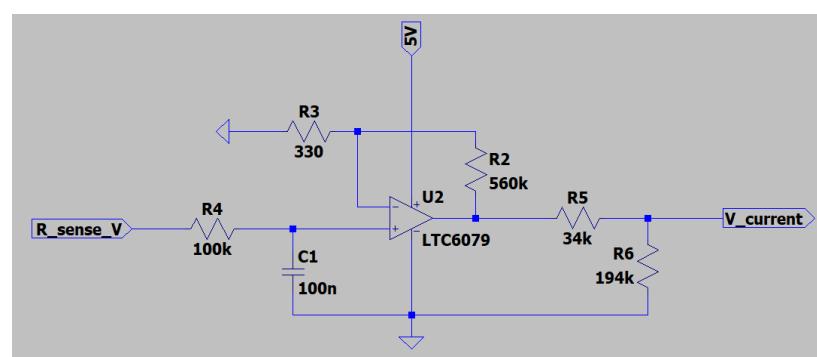


Figure 2.1: Current sensing circuit design

## 2.2. Analogue range sensor

The HC-SR04 ultrasonic sensor requires a 5 V supply and requires 15 mA to operate [1]. The frequency of the sensor output is the same as the input trigger frequency which is 16 Hz. Using a maximum distance of 1 m and a minimum distance of 5 cm results in a minimum duty cycle of 0.4% and a maximum duty cycle of 10%. The output pulses will have a maximum amplitude of [1].

Equation 2.1 is used to calculate the needed gain of the system. In order to have the gain stage output a maximum of 5 V at 1 m a gain of 10.77 is required.

$$Gain = \frac{V_{Expected}}{V_{DutyCycle \cdot V_{Amplitude}}} \quad (2.1)$$

In order to determine the corner frequency first the minimum attenuation must be calculated. The minimum attenuation can be calculated using the gain and amplitude of the first harmonic frequency component in the square wave to determine the size of the output ripple voltage, see Equation 2.2. Since the second harmonic and higher will all be attenuated more aggressively than the first harmonic it will contribute the most to the ripple voltage.

$$FirstHarmonicAmplitude = V_{Amplitude} \cdot DutyCycle \cdot sinc(\pi \cdot DutyCycle) \quad (2.2)$$

$$MinimumAttenuation = 20 \log\left(\frac{MaximumNoise}{FirstHarmonicAmplitude \cdot Gain}\right) \quad (2.3)$$

Using Equation 2.3 it is determined that an attenuation of atleast  $-41$  dB is needed at 16 Hz. The corner frequency is then determined solving a simple straight line graph equation as shown in Equation 2.5.

$$\log(w) = \frac{MinimumAttenuation + AttenuationSlope \cdot \log(2\pi \cdot F_{trigger})}{AttenuationSlope} \quad (2.4)$$

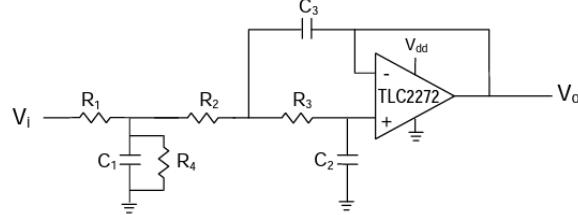
$$F_{cutoff} = 10^{2\pi \cdot \log(w)} \quad (2.5)$$

To determine what order filter to use Equation 2.5 was solved using the different gradients for 1st, 2nd and 3rd order filters. Table 2.1 shows the results of these calculations. In order to adhere to the response time specifications of 1.5 s it was decided that a 3rd order filter would have the best response time and noise attenuation without being to complex to build.

Design document [2] was used in the design of the 3rd order filter. Figure: 2.2 shows the filter configuration that will be used. A simple gain stage will be appended to the end of the filter and then a voltage divider will ensure that the final output voltage is less than 3.3 V. The whole circuit diagram is shown in Figure: 2.3. The circuit is designed to take input with an amplitude of 5 V with a duty cycle between 0% and 10%.

Filter	Gradient	Maximum corner frequency
1st	-20 dB	0.13 Hz
2nd	-40 dB	1.44 Hz
3rd	-60 dB	3.2 Hz

**Table 2.1:** Filters and their maximum required corner frequency

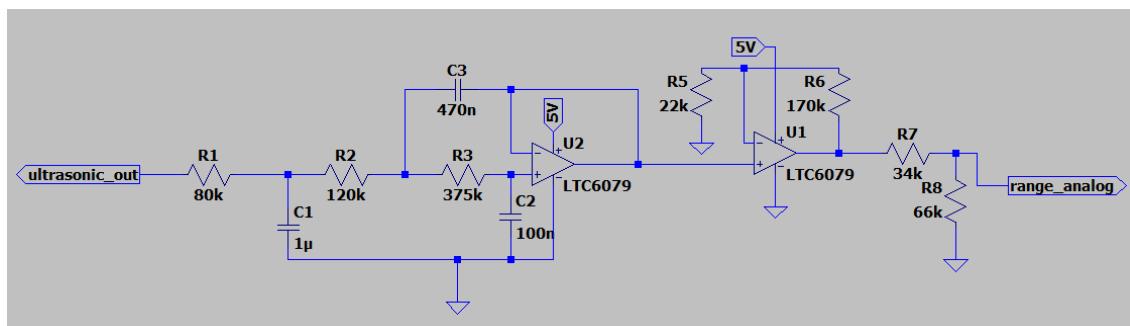


**Figure 2.2:** Filter configuration from [2]

The design document gives nominal values of  $R_1=1.6\text{ k}\Omega$   $R_2=2.4\text{ k}\Omega$   $R_3=7.5\text{ k}\Omega$   $C_1=100\text{ nF}$   $C_2=10\text{ nF}$   $C_3=47\text{ nF}$  to construct a third order filter with a corner frequency of 1 kHz. It was decided to design for a corner frequency of 2 Hz as this provides a good compromise between noise reduction and response time. In order to achieve this corner frequency frequency and impedance scaling was used on the given component values to get them to acceptable values that are easy to implement and result in minimal current draw.

For the gain stage resistors  $R_5 = 22\text{ k}\Omega$  and  $R_6 = 220\text{ k}\Omega$  potentiometer. This will allow for a gain of up to 10 as calculated, however as shown in Figure: 2.3 a lower gain is required to achieve the desired circuit response. This is due to practicalities such as rise time increasing the DC component of the input signal.

The voltage divider,  $R_7$  and  $R_8$  in Figure: 2.3, is to reduce the maximum output of 5 V from the gain stage to a maximum of 3.3 V to be used as input to the micro-controller. The resistor values are chosen to reduce current draw.



**Figure 2.3:** Filter configuration from [2]

## 2.2.1. Digital to Analogue converter

The input impedance seen by each source is equal to the resistor between it and the inverting input [10]. Thus to reduce the effect of the output impedance of the source the smallest input resistor must be much larger than the output impedance.

The operation of the DAC is not affected by the input impedance of the receiving circuit unless the input impedance is so low as to cause the op amp to reach its current limits of 23 mA [11]. This will result in the op amp being unable to drive the required output voltage and the output voltage will be limited. A buffer will be added between the DAC and the output, this separates the output from the input and prevents any signal reflections from making it back to the input terminals.

The MCP6242 has a common mode voltage range of  $V_{SS} - 0.3 < V_{CMR} < V_{DD} + 0.3$  [11]. For the configuration shown in 2.4 the common mode voltage will be the offset voltage applied at the positive terminal. As long as this offset voltage is less than the rail voltage there will be no problems with the op amps common mode voltage restrictions.

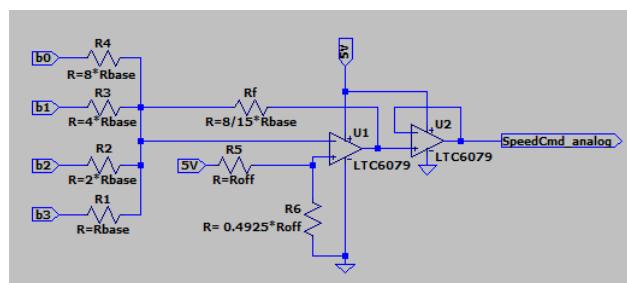
The maximum expected input will be 3.3 V. The maximum output is 3.3 V however the configuration shown in Figure: 2.4 can output up to 5 V, this can only happen if the input voltages go negative.

$R_{off}$  is chosen to be 100 k $\Omega$  in order to reduce current draw and  $R_{base}$  is chosen to be 50 k $\Omega$  to ensure high input impedance. Equation: 2.6 shows the relationship between the base resistor and the feedback resistor based on the maximum desired output. Equation: 2.7 shows what  $V_{off}$  will be based on the maximum desired output.

Potentiometers will be used to control the offset voltage and gain of the op amp as these values are critical to the correct operation of the circuit and will require tuning.

$$\frac{R_f}{R_1} = \frac{8 \cdot V_{OutMax}}{15 \cdot V_{InMax}} \quad (2.6)$$

$$V_{off} = \frac{V_{OutMax}}{1 + \frac{V_{OutMax}}{V_{InMax}}} \quad (2.7)$$



**Figure 2.4:** Summing amplifier configuration

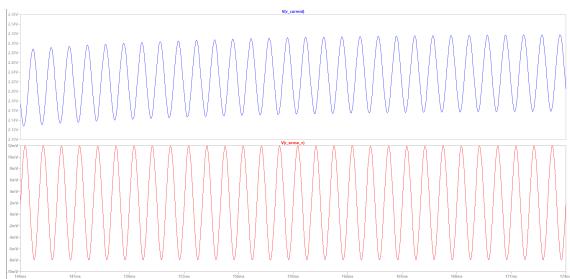
# Chapter 3

## Results

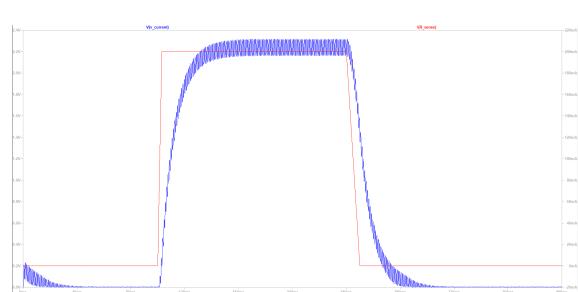
### 3.1. Current sensor

#### 3.1.1. Simulation

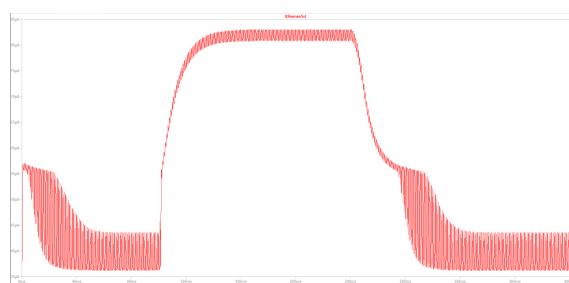
Figure 3.1 shows the simulation results for the circuit shown in Figure: 2.1. The requirement for a 10 mV signal at 1 kHz to result in less than 250 mV at the output, is shown to be met in 3.1a where the 10 mV signal at 1 kHz results in an output of  $\approx 160$  mV. Figure 3.1b shows that the circuit has a response time less than 100ms, with a response time of  $\approx 30$  ms. The requirement that the amplification circuit draws less than 150  $\mu$ A is met in Figure: 3.1c where the maximum current draw is 83  $\mu$ A.



(a) Noise input vs output of current sensing circuit.



(b) Step response of current sensing circuit.



(c) Current draw of 5V supply to current sensing circuit.

**Figure 3.1:** Current sensing circuit simulation results

### 3.1.2. Practical

As shown in Figure:3.2 the practical results match the simulated results shown in Figure: 3.1.

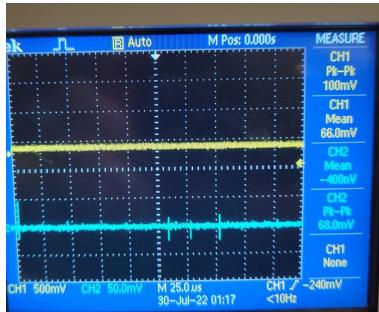
The practical response to no input (3.2a) shows an output of 66 mV, this differs from the simulation output of 0 V due to the non ideal nature of practical op amps and is due to the offset voltage between the input terminals.

Figure: 3.1b shows an output voltage of 2.2 V to a 200 mA input while Figure: 3.2c shows a 1.82 V output to a 200 mA input. This is due to the practical circuit having a reduced gain in comparison to the simulation. This was done to reduce the affect of the input offset voltage mentioned previously.

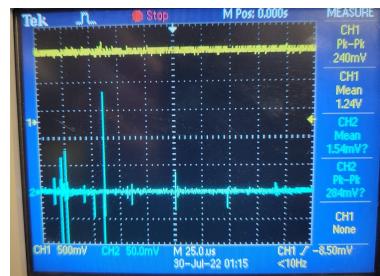
Figure: 3.2d shows the output clips sat 3.28 V which is very close to the theoretical 3.3 V.

Figure: 3.2e shows a lesser response to noise than the simulation, this is due to the noise input to the practical circuit is different to the simulated noise and at a higher frequency so the low pass filter attenuates it more heavily.

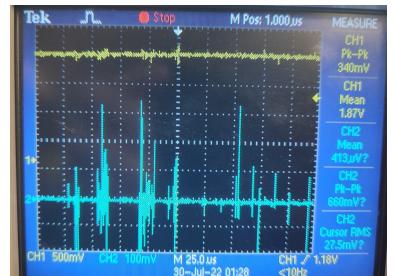
The measure response time in Figure: 3.2f is 24 ms which is very close to the response time measured in the simulation of 30 ms.



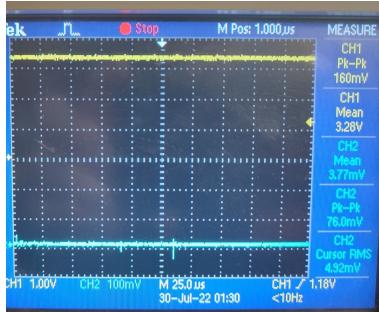
(a) Circuit response to no input.



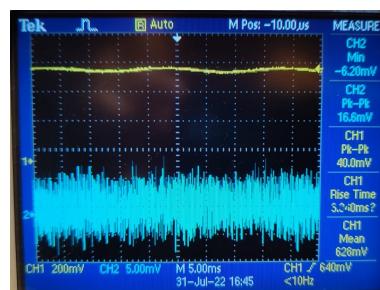
(b) Circuit response to free running motor.



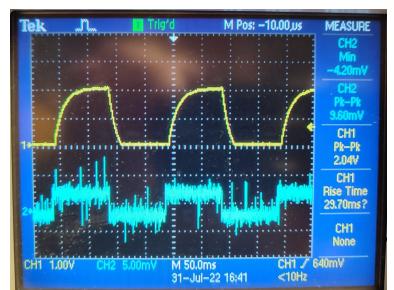
(c) Circuit response to slight restriction on the motor.



(d) Circuit response to motor stall.



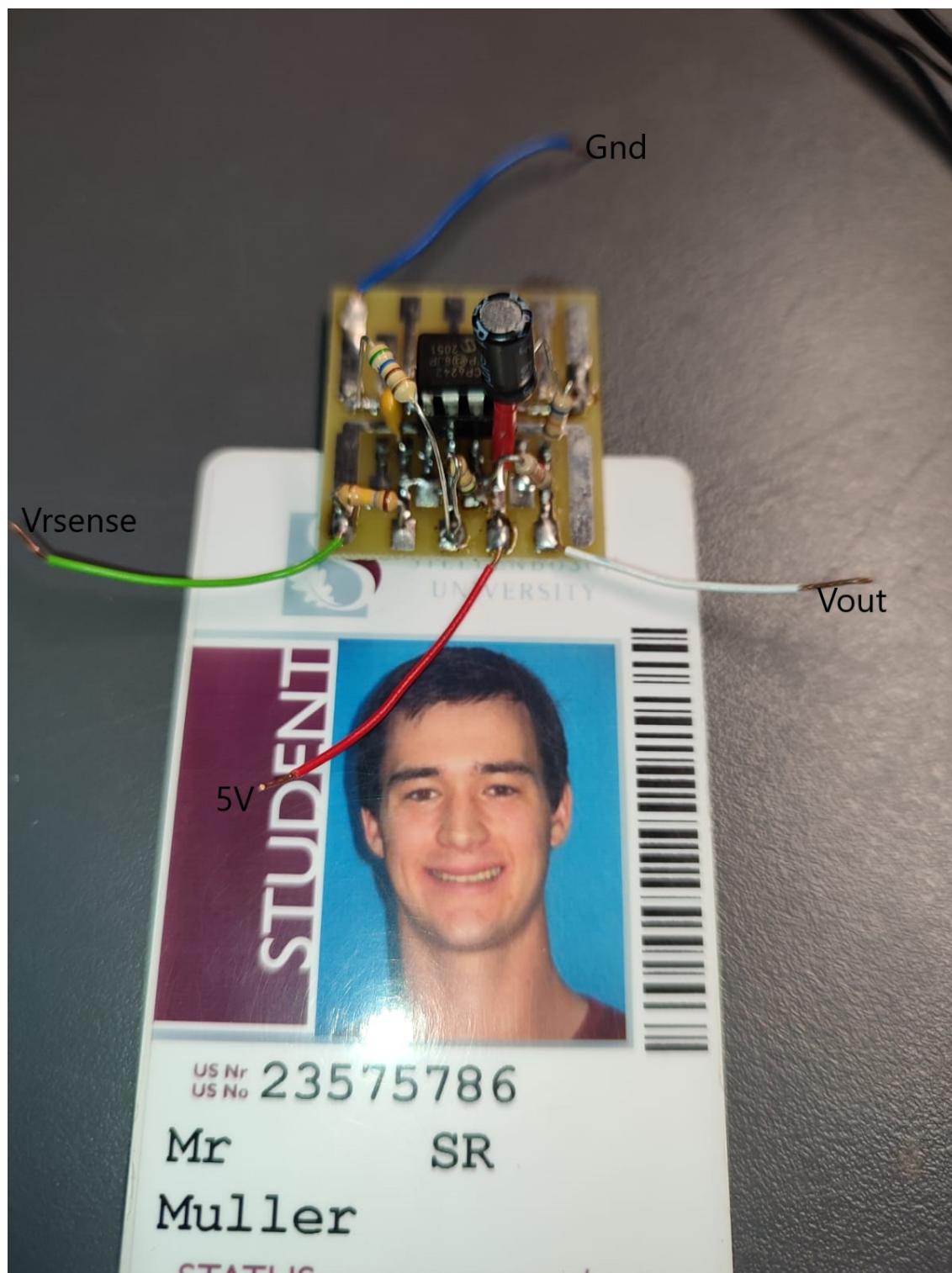
(e) Circuit response to noise.



(f) Circuit response to step input.

**Figure 3.2:** Circuit response to different input conditions

### 3.1.3. Circuit



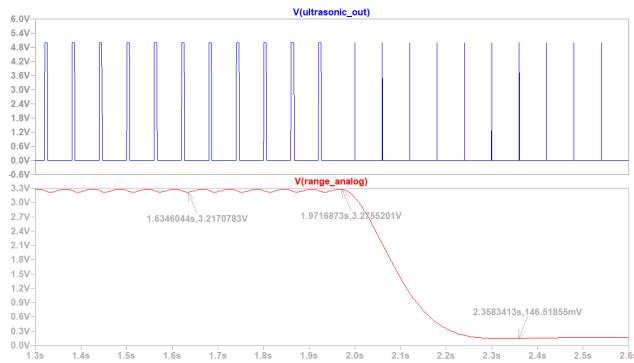
**Figure 3.3:** Labelled circuit and student card.

## 3.2. Ultrasonic range sensor

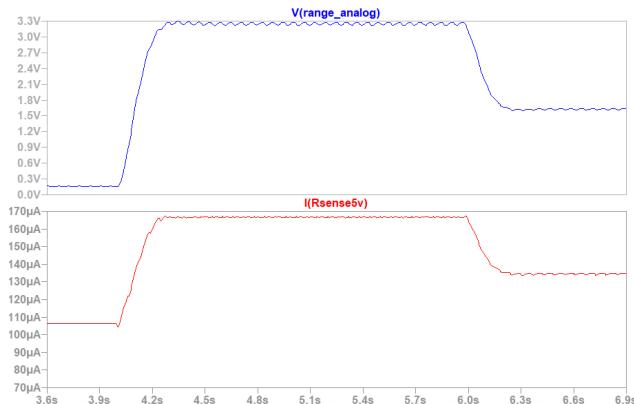
### 3.2.1. Simulation

Figure: 3.4 shows the circuit response to a step input change from the maximum 10% duty cycle to a 0.5% duty cycle. As shown in the figure the circuit outputs  $\approx 3$  V for a maximum input and  $\approx 0.3$  V for the minimum input. The figure also demonstrates the circuits compliance to the noise and response time requirements with noise levels of 58 mVpk-pk and a response time of 386 ms.

Figure: 3.5 shows that throughout circuit operation current draw is  $\approx 170 \mu\text{A}$ .



**Figure 3.4:** Circuit response to a full range step from 10% to 0.5% duty cycle



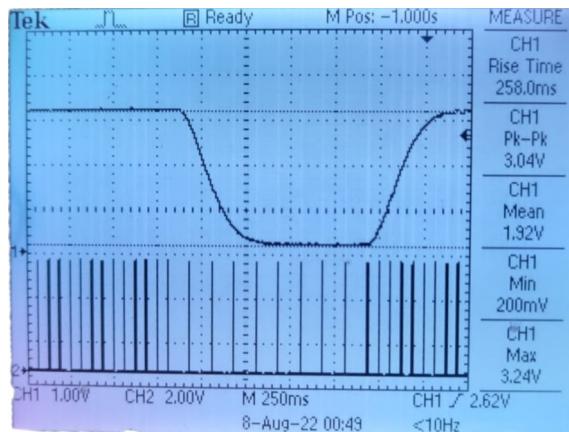
**Figure 3.5:** Current draw vs circuit output

### 3.2.2. Practical

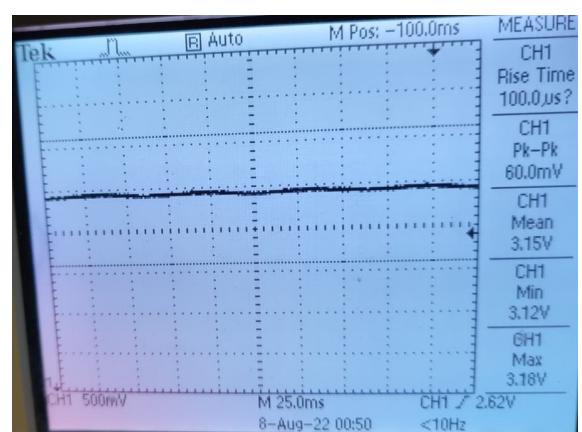
Figure: 3.4 shows the output response to a step change from 1 m to 5 cm back to 1 m. The figure also shows the compliance to the requirements with the 1 m measurement having an output of 3.24 V and an output of 200 mV at 5 cm. The figure also shows a compliance with the rise time of 258 ms.

Figure: 3.6b shows that the output ripple voltage is less than 70 mVpk-pk at 1 m when the ripple voltage will be at its worst.

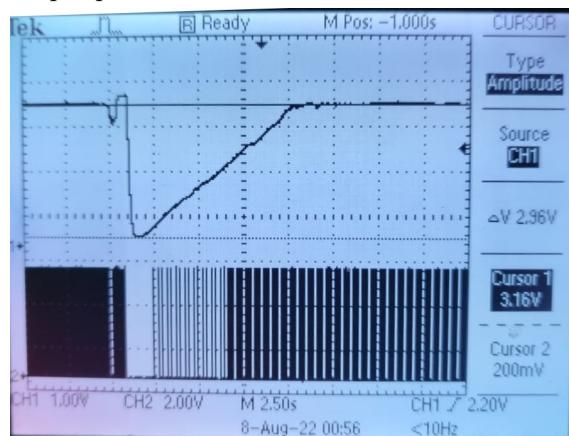
Figure: 3.6c shows the circuit response to a gradual change in the input across the full range from close to far.



(a) Circuit response a step input.



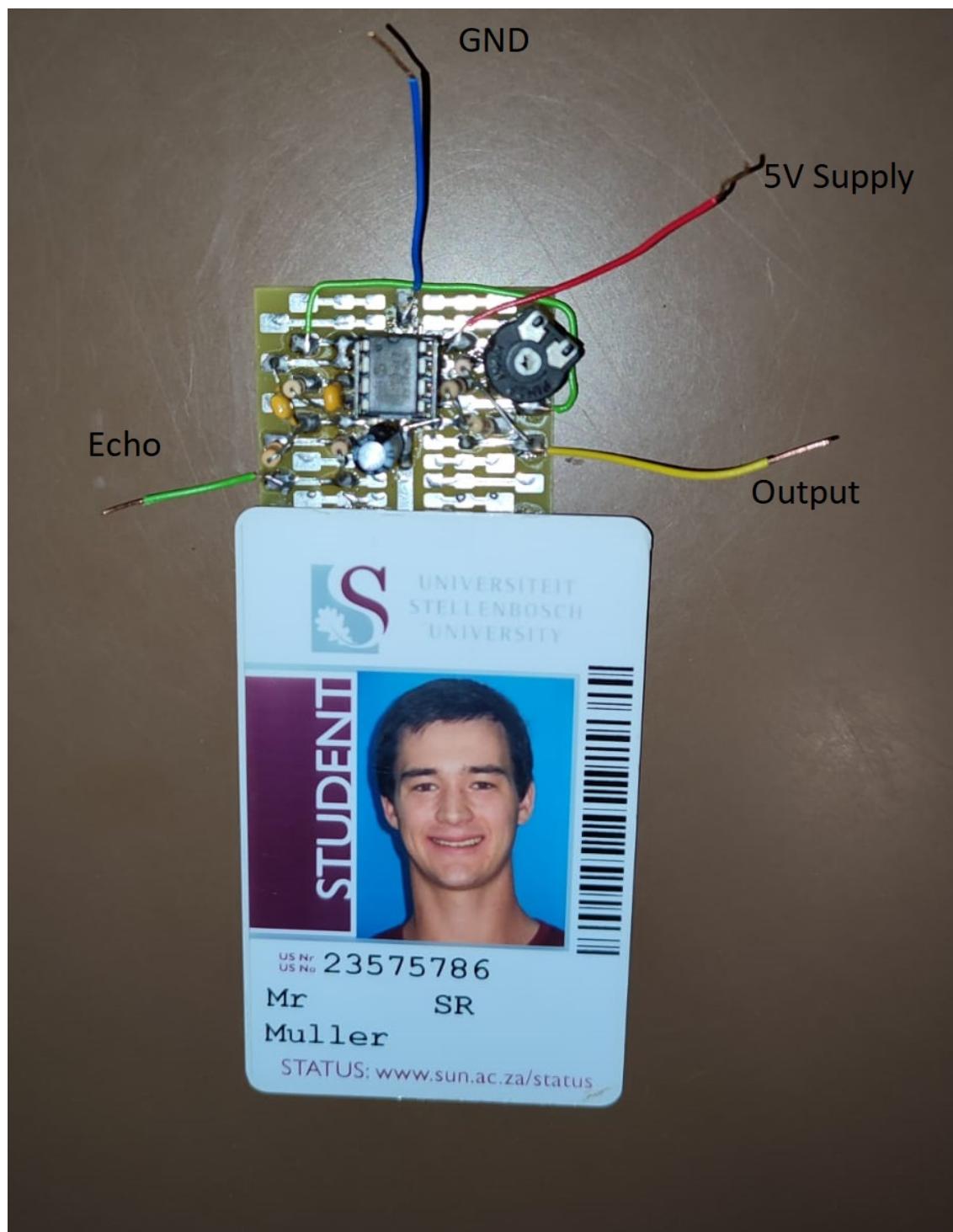
(b) Circuit ripple voltage at 1m.



(c) Circuit response to smooth change in range measurement.

**Figure 3.6:** Ultrasonic sensor filter circuit responses.

### 3.2.3. Circuit

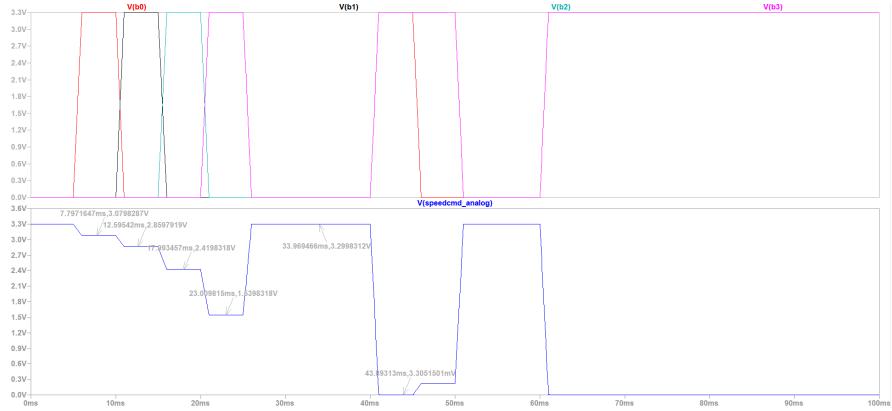


**Figure 3.7:** Labelled circuit and student card.

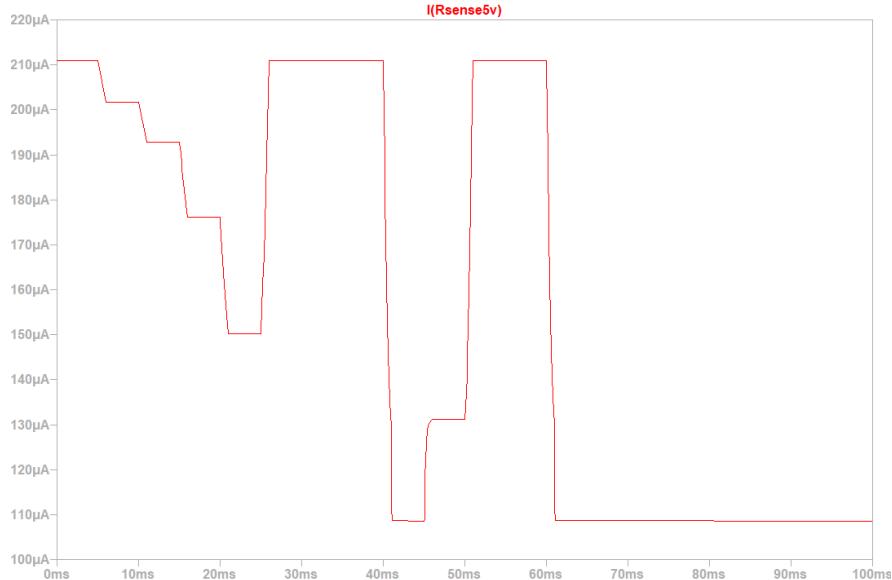
### 3.3. Digital to analogue converter

#### 3.3.1. Simulation

Figure: 3.8 shows the simulation output vs the given input and that the simulated results match the requirements. Figure: 3.9 shows that the current draw for the simulated circuit is at acceptable levels.



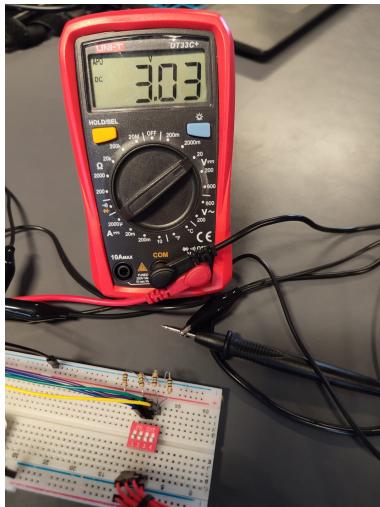
**Figure 3.8:** Output vs input of DAC.



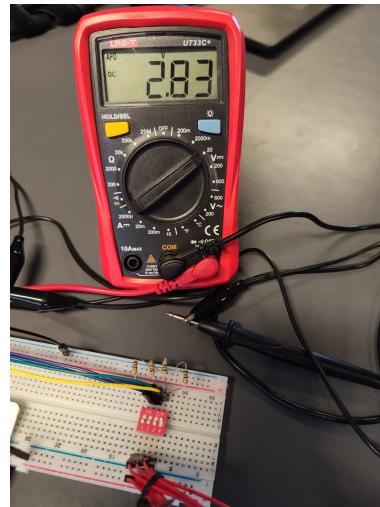
**Figure 3.9:** Current draw of the DAC circuit

### 3.3.2. Practical

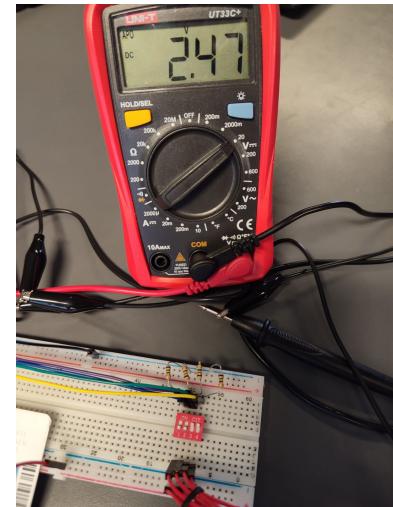
Figure: 3.10 shows the DAC response to different inputs. Figure: 3.10a shows that the circuit complies with the requirement to have an output larger than 3 V for an input of 0. Figure: 3.10e shows the circuit complies with the requirement that the output is less than 0.5 V.



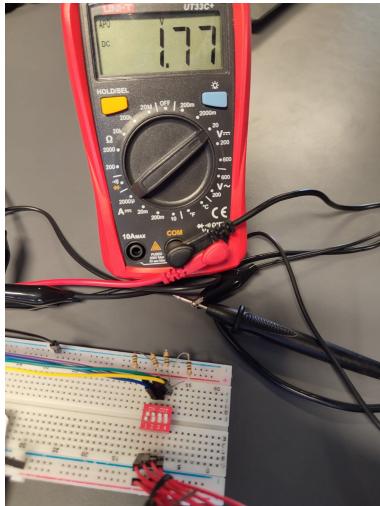
(a) DAC output for 0000 input.



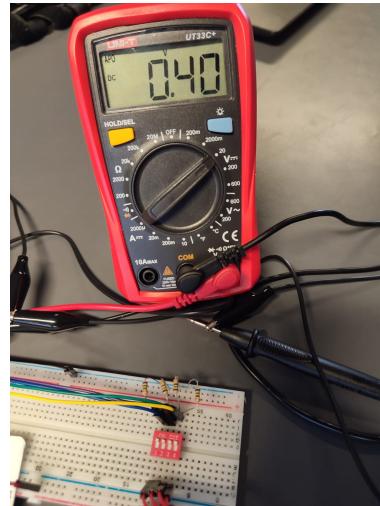
(b) DAC output for 0001 input.



(c) DAC output for 0011 input.



(d) DAC output for 0111 input.



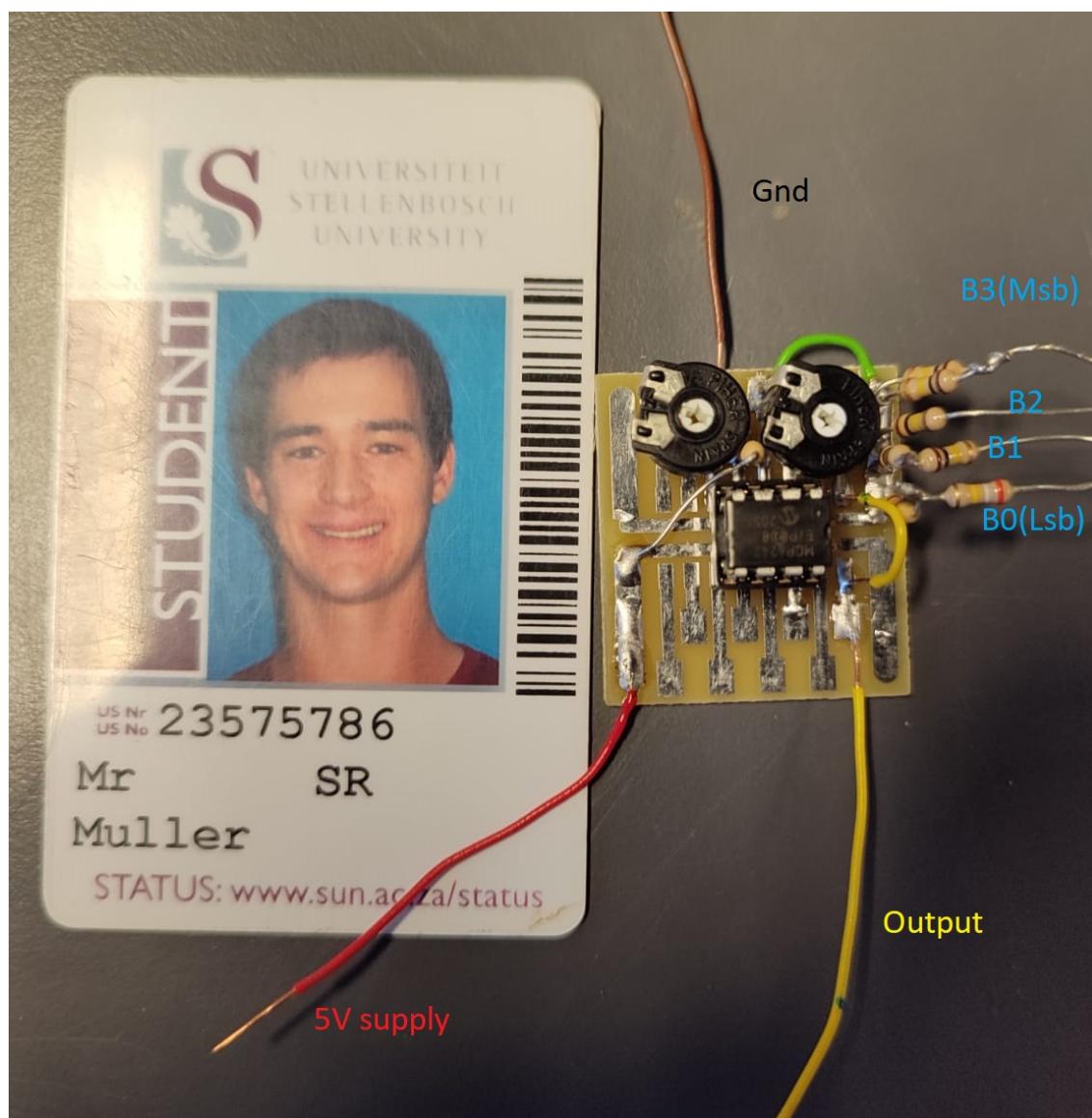
(e) DAC output for 1111 input.



(f) DAC output for 1110 input.

**Figure 3.10:** DAC output for different inputs.

### 3.3.3. Circuit



**Figure 3.11:** Labelled circuit and student card for the DAC.

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# Appendix A

## Social contract



UNIVERSITEIT-STELLENBOSCH-UNIVERSITY  
jou kennisvennoot • your knowledge partner

### E-design 344 Social Contract

2022

The purpose of this document is to establish commitment between the student and the organisers of E344. Beyond the commitment made here, it is not binding.

In the months preceding the term, the lecturer (Thinus Booyens) and a few paid helpers (Rita van der Walt, Keegan Hull, and Michael Ritchie) spent countless hours to prepare for E344 to ensure that you get your money's worth, that you are enabled to learn from the module, and demonstrate and be assessed on your skills. We commit to prepare the assignments, to set the assessments fairly, to be reasonably available, and to provide feedback and support as best and fast we can. We will work hard to give you the best opportunity to learn from and pass analogue electronic design E344.

I, **Sean Muller**, have registered for E344 of my own volition with the intention to learn of and be assessed on the principals of analogue electronic design. Despite the potential publication online of supplementary videos on specific topics, I acknowledge that I am expected to attend the scheduled lectures to make the most of these appointments and learning opportunities. Moreover, I realise I am expected to spend the additional requisite number of hours on E344 as specified in the yearbook.

I acknowledge that E344 is an important part of my journey to becoming a professional engineer, and that my conduct should be reflective thereof. This includes doing and submitting my own work, working hard, starting on time, and assimilating as much information as possible. It also includes showing respect towards the University's equipment, staff, and their time.

Prof. MJ (Thinus) Booyens

MJ Booyens  
Signature: \_\_\_\_\_  
Date: 2022-07-09  
13:22:08 +0200

Student number: 23575786

Sean Muller  
Signature: \_\_\_\_\_  
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09:50:25 +0200

Date: 1 July 2022

Date: 25 July 2022

# Appendix B

## GitHub Activity Heatmap

