|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Cases | Input | | | Output |
|  | D | CLK | Reset | Q |
| B | 1 | ↑ | 0 | 1 |
| A | 0 | ↑ | 0 | 0 |
| C | 0/1 | ↑ | 1 | 0 |

Q changes state on the rising edge of the clock, Q = 1 when D = 1 and Q = 0 when D = 0.

Q is reset to 0 on the rising edge of the clock when the Reset signal = 1.