|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Cases | Input | | | | Output | |
|  | J | K | CLK | Reset | Q | Q\_not |
| A | 0 | 1 | ↑ | 0 | 0 | 1 |
| C | 1 | 0 | ↑ | 0 | 1 | 0 |
| E | 1 | 1 | ↑ | 0 | Q\_not | Q |
| B, D | 0 | 0 | ↑ | 0 | Q | Q\_not |
| F | 0/1 | 0/1 |  | 1 | 0 | 1 |

Q changes state on the rising edge of the clock, Q = 1 when J= 1 and K = 0, and Q = 0 when J = 0 and K = 1.

Q\_not is the inverse of the output Q.

When both J and K = 0, Q = the same state it was last clock cycle, the same with Q\_not, and when J and K both equal 1, Q and Q\_not become inverted.

Q is reset to 0 and Q\_not is reset to 1 when the Reset signal = 1.