Lecture 5

- No lecture next week
- Project presentations Feb. 25, 2021
  - Piazza @22 gives outline of what's required
  - 11 submissions to Assignment 1
- Assignment 2 is posted
  - Watch for Piazza post with further instructions

THE AXI BUS AND INTERFACE

Resources

- The Zynq Book, Chapter 19 (pdf download available)
- Slides borrowed from https://people-ece.vse.gmu.edu/coursewebpages/ECE/ECE699_SW_HW/S16/viewgraphs/ECE699_lecture_6.pdf
- AMBA AXI and ACE Protocol Specification
- AMBA 4 AXI4-Stream Protocol Specification

Xilinx

- Most IP blocks provided use AXI4 interfaces
- Many useful cores that you can plug-and-play

- Vivado Design Suite AXI Reference Guide
- AXI Interconnect v2.1
- AXI4-Stream Interconnect v1.1
- AXI Video Direct Memory Access

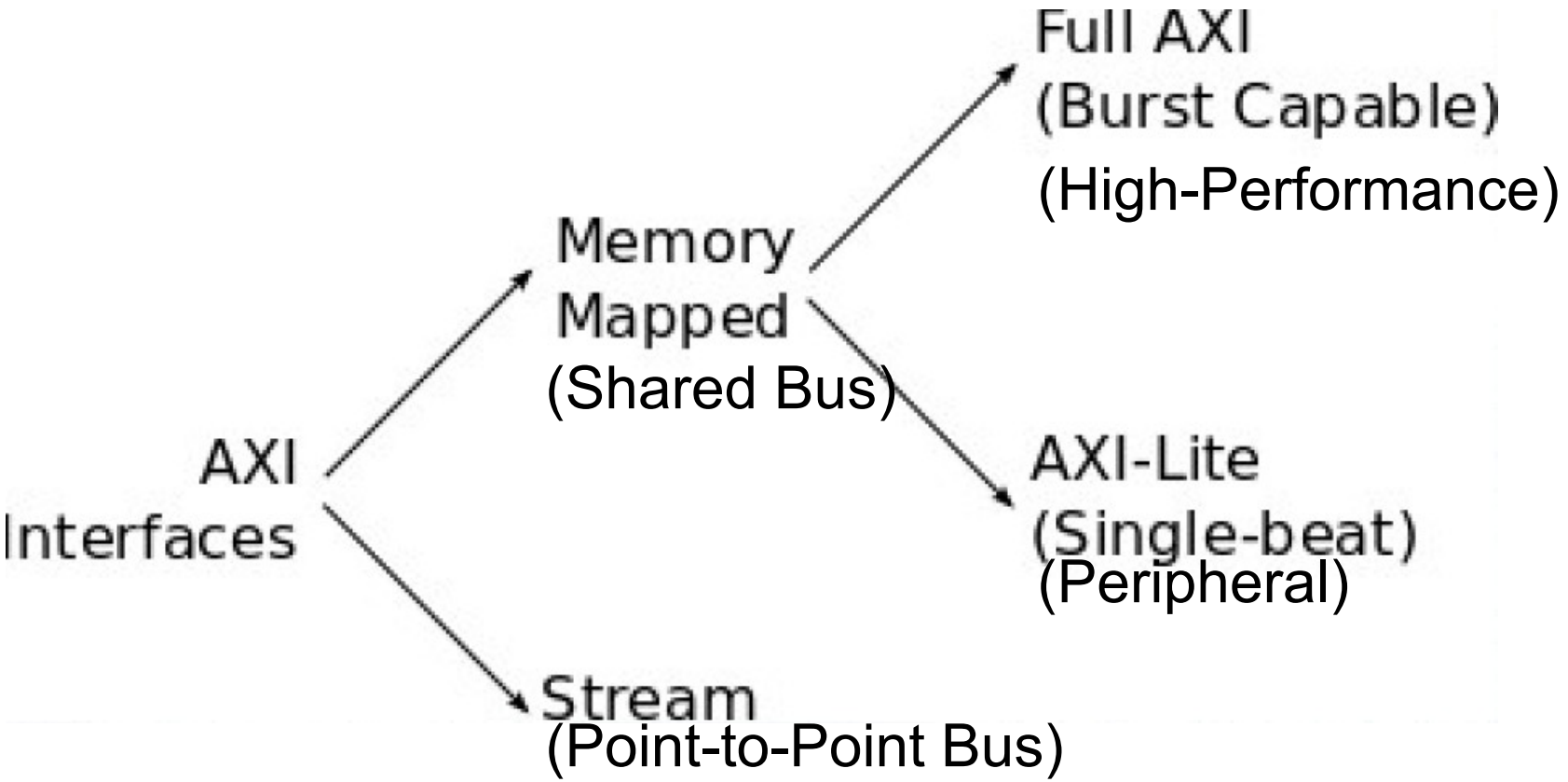
Borrowed from
ECE 699: Lecture 6

AXI Interfacing

Selected Slides

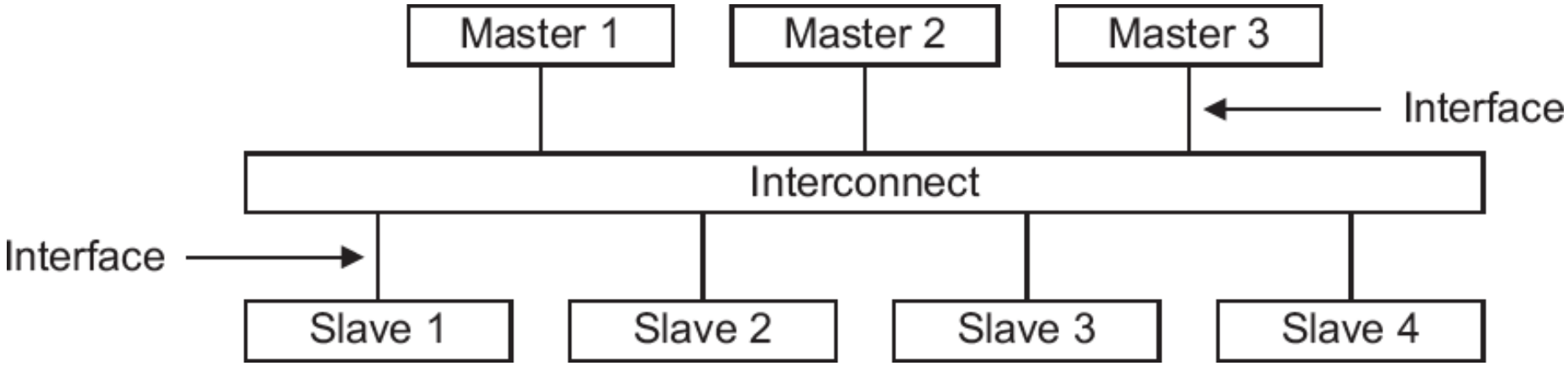
(Reorganized)

AXI Interfaces



Source: M.S. Sadri, Zynq Training

Interconnect vs. Interface



AXI Interfaces and Interconnects

Interface

A point-to-point connection for passing data, addresses, and hand-shaking signals between master and slave clients within the system

Interconnect

A switch which manages and directs traffic between attached AXI interfaces

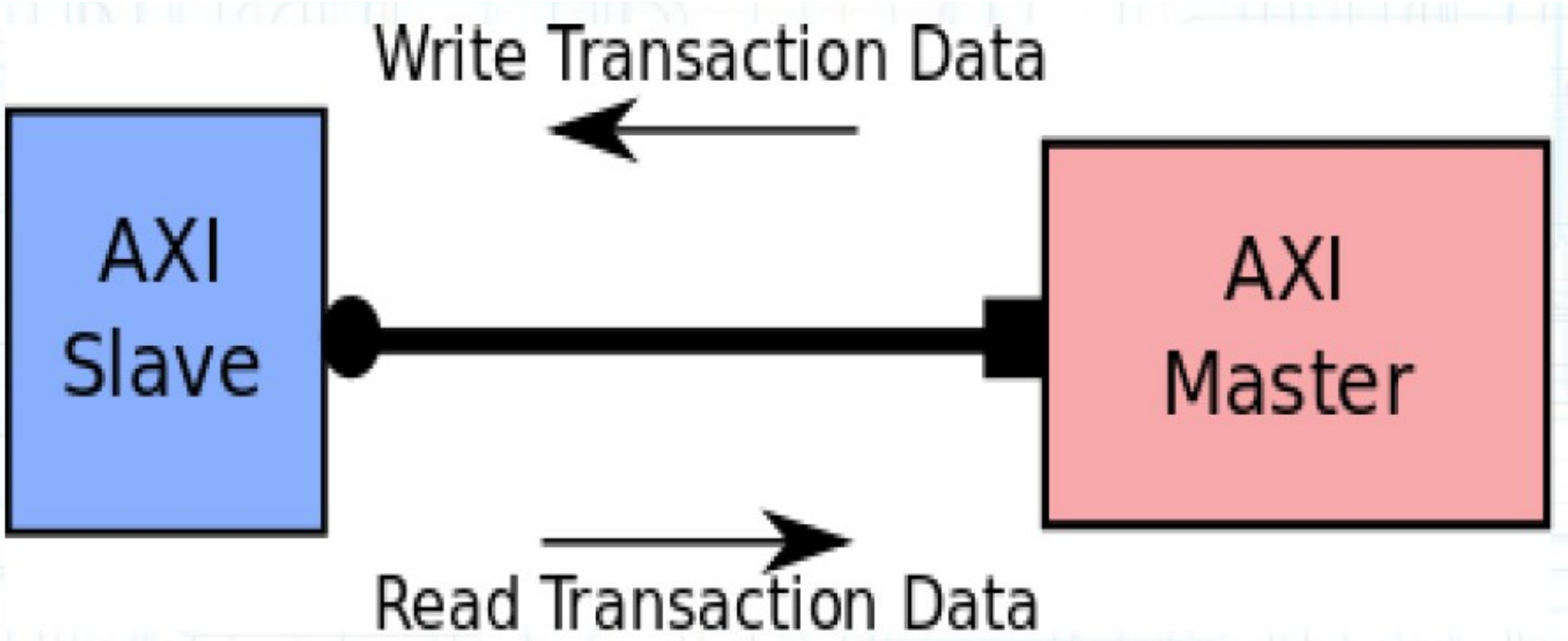
Source: The Zynq Book

Basic Concepts

- Transaction :
  - Transfer of data from one point in the hardware to another point
- Master : Initiates the transaction
- Slave : Responds to the initiated transaction

Source: M.S. Sadri, Zynq Training

Communication Between AXI Master and AXI Slave



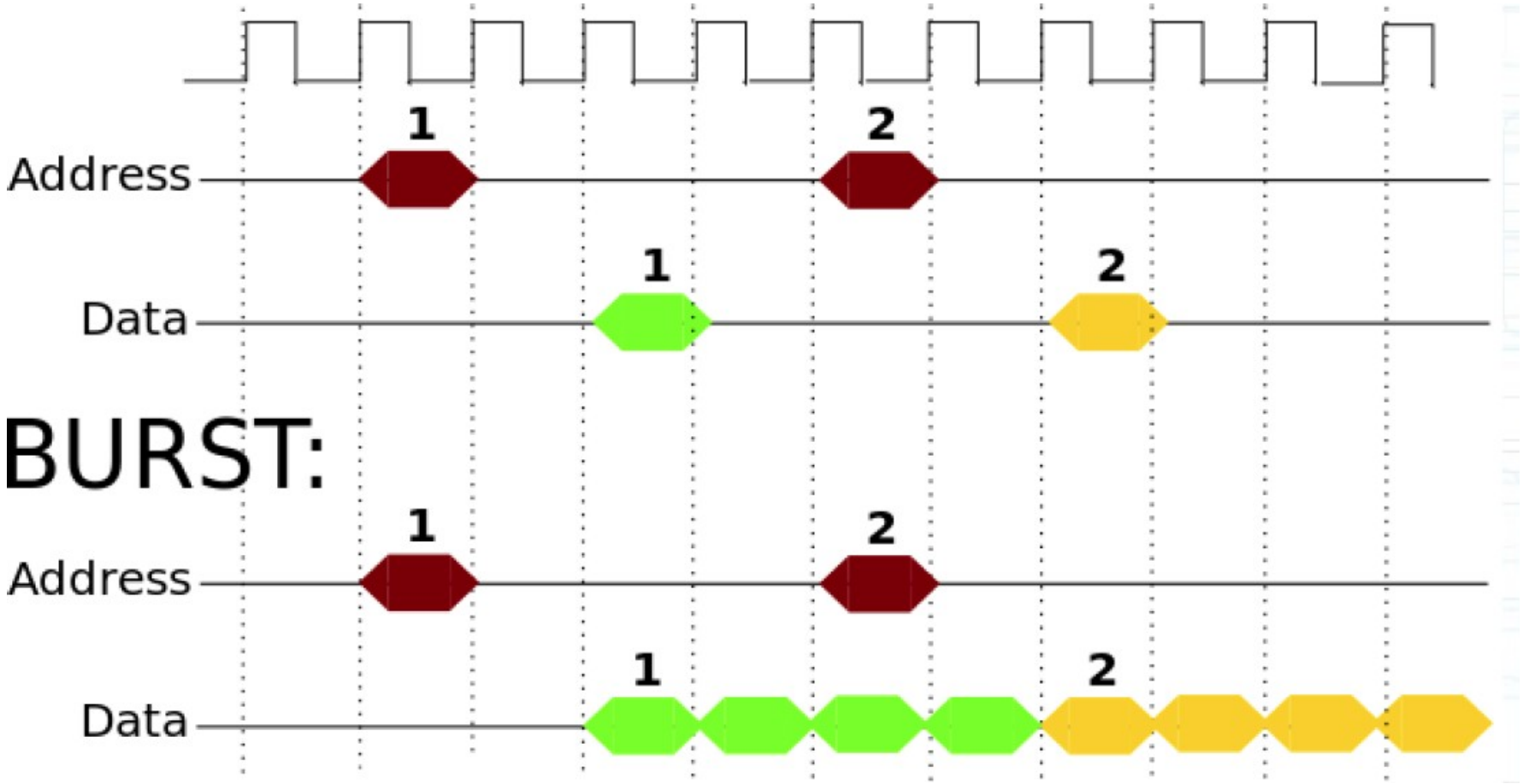
Source: M.S. Sadri, Zynq Training

AXI4 MEMORY MAPPED (FULL AND LITE)

AXI4 vs AXI4-LITE

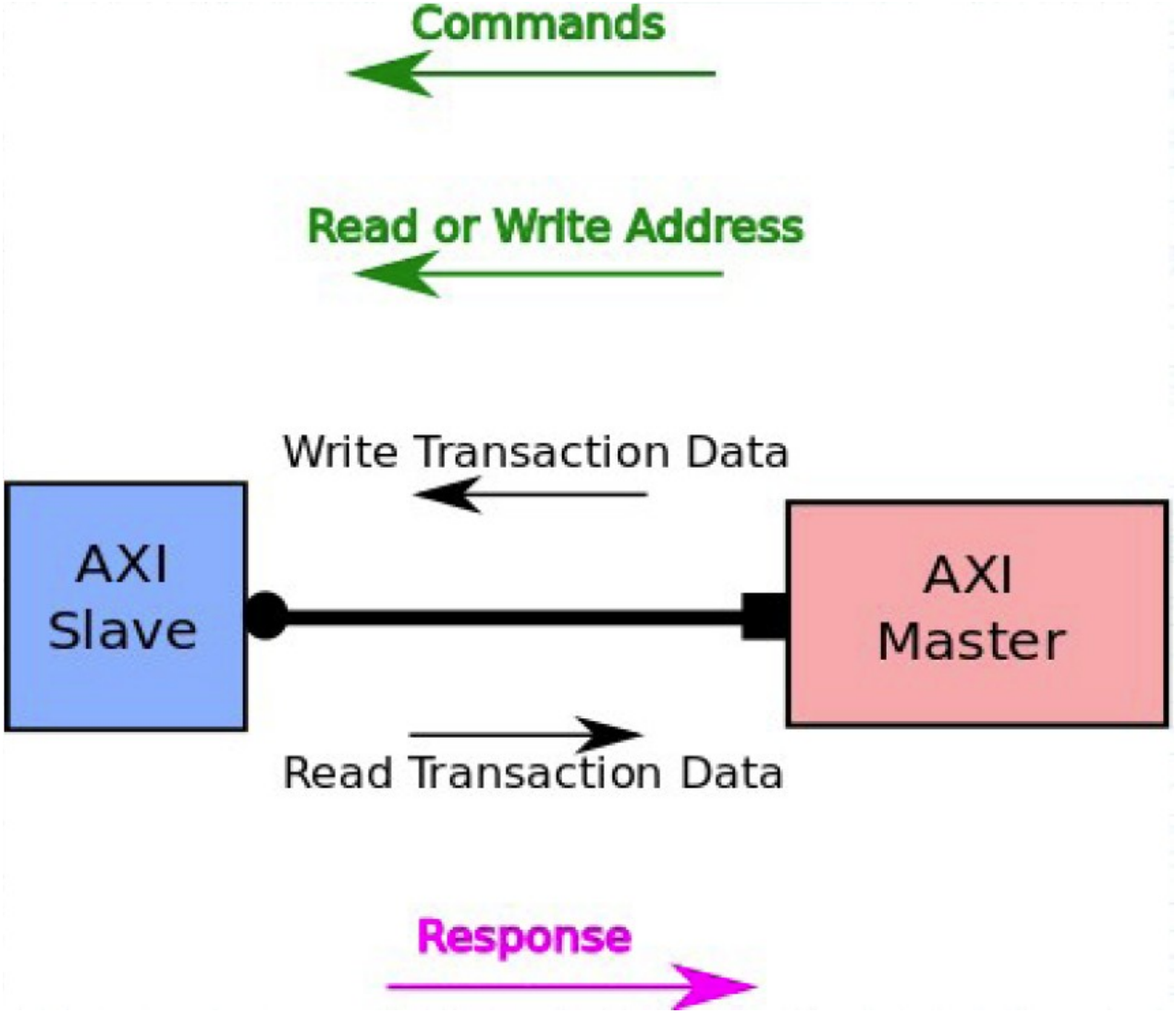
- AXI4-LITE
  - Simple, low-throughput memory-mapped communication
  - Access control and status registers
  - 32-bit
- AXI4
  - High-performance memory-mapped access
  - Various bit widths
  - Burst transfers

Concept of a Burst



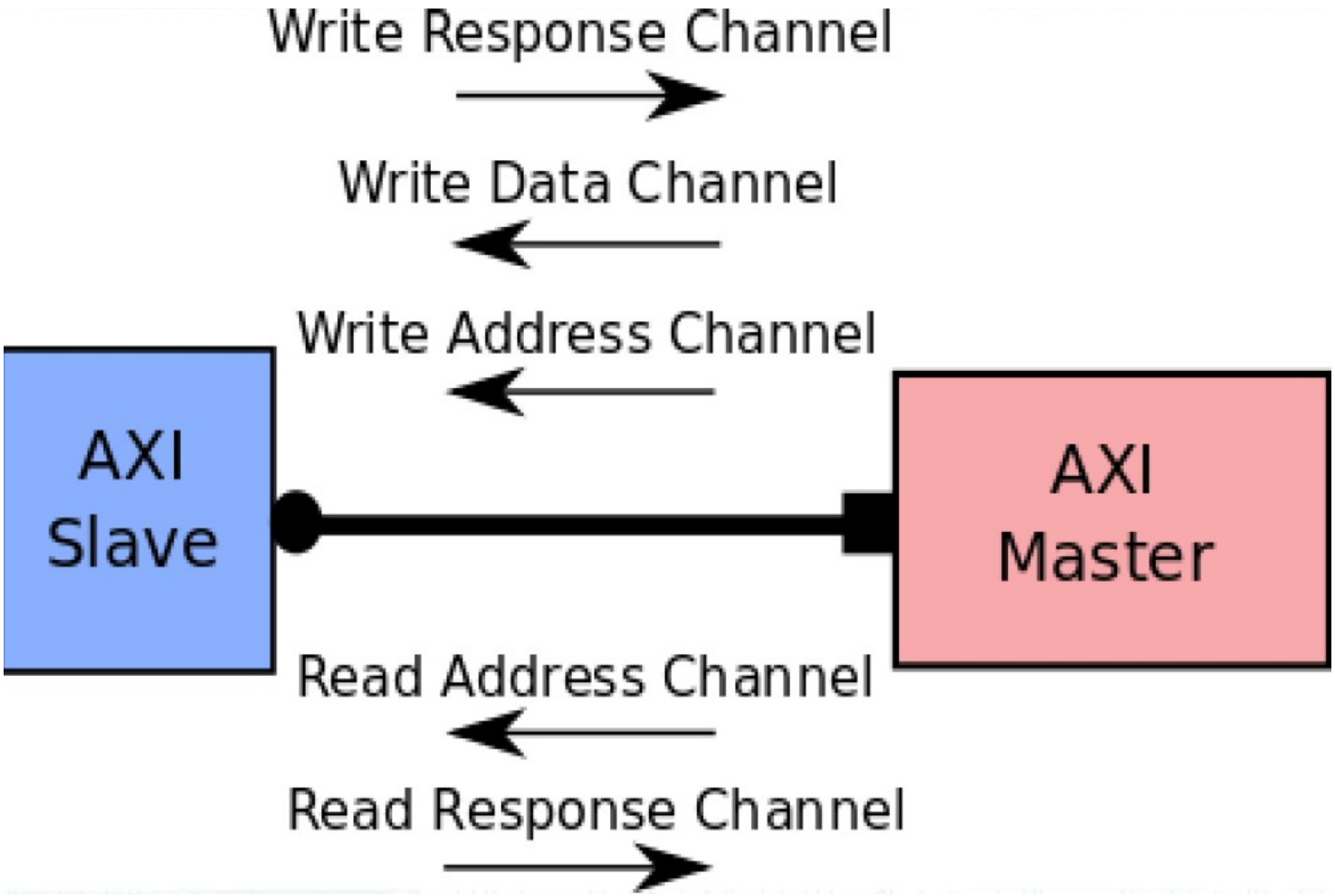
Source: M.S. Sadri, Zynq Training

Additional Information Exchanged Between AXI Master and AXI Slave



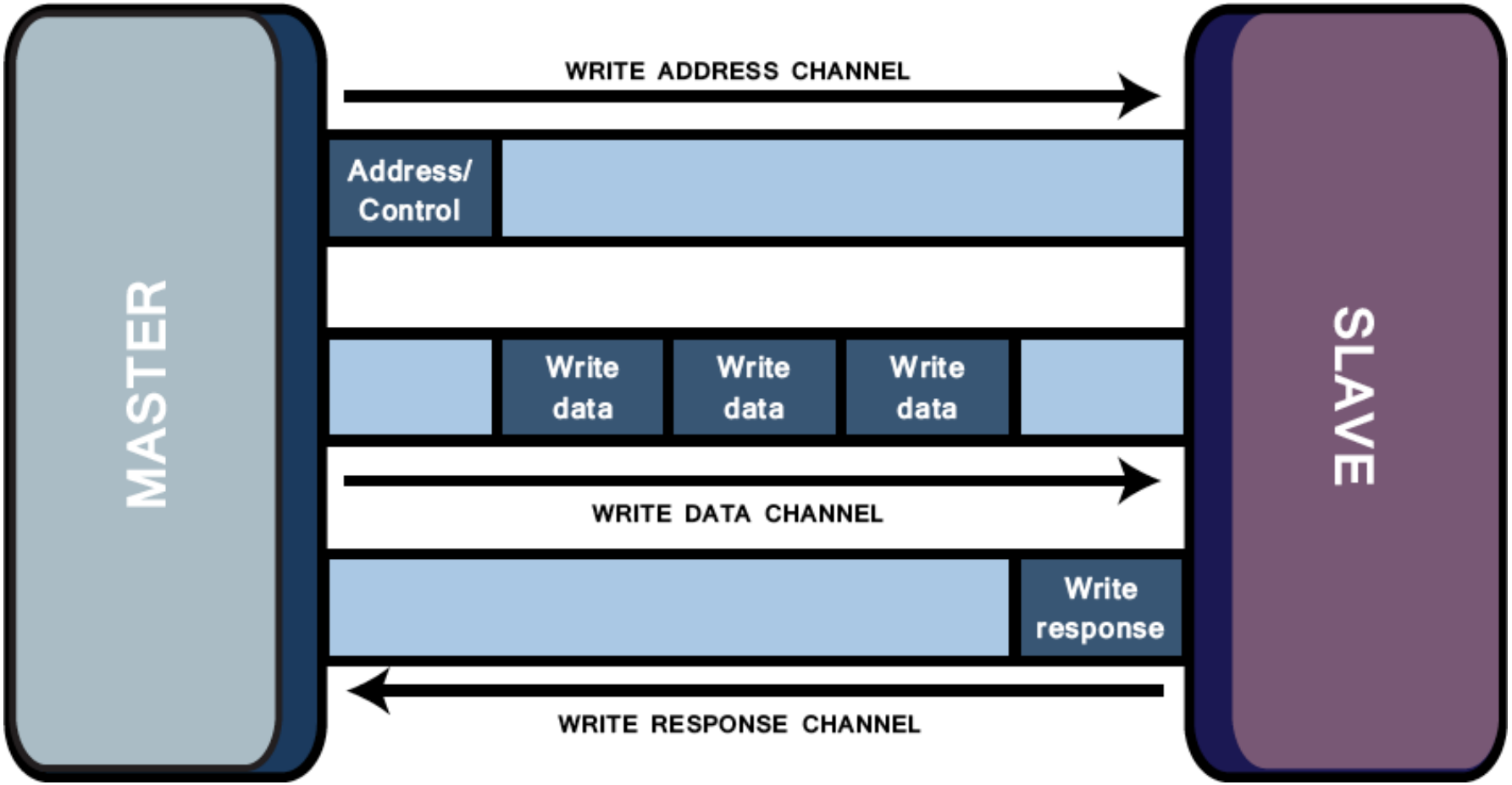
Source: M.S. Sadri, Zynq Training

Five Channels of AXI Interface



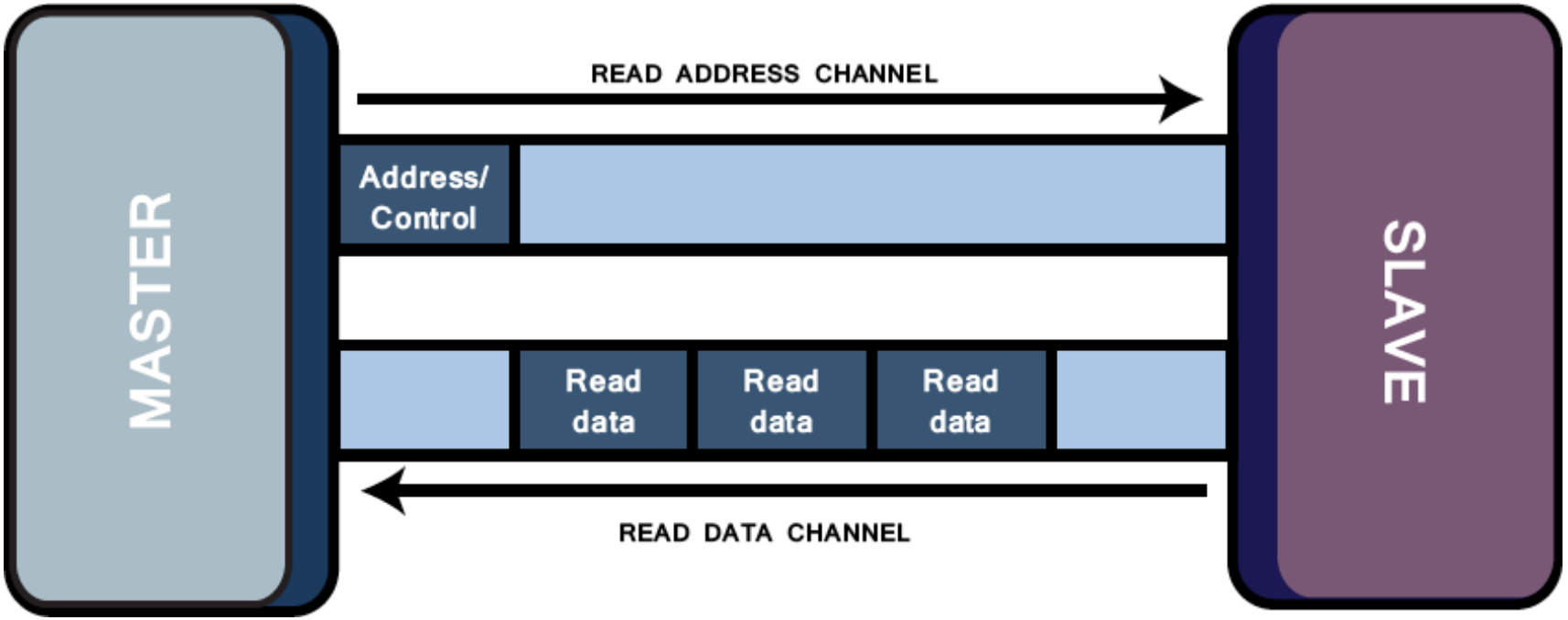
Source: M.S. Sadri, Zynq Training

AXI4 Write



Source: The Zynq Book

AXI4 Read



Source: The Zynq Book

AXI4 Interface

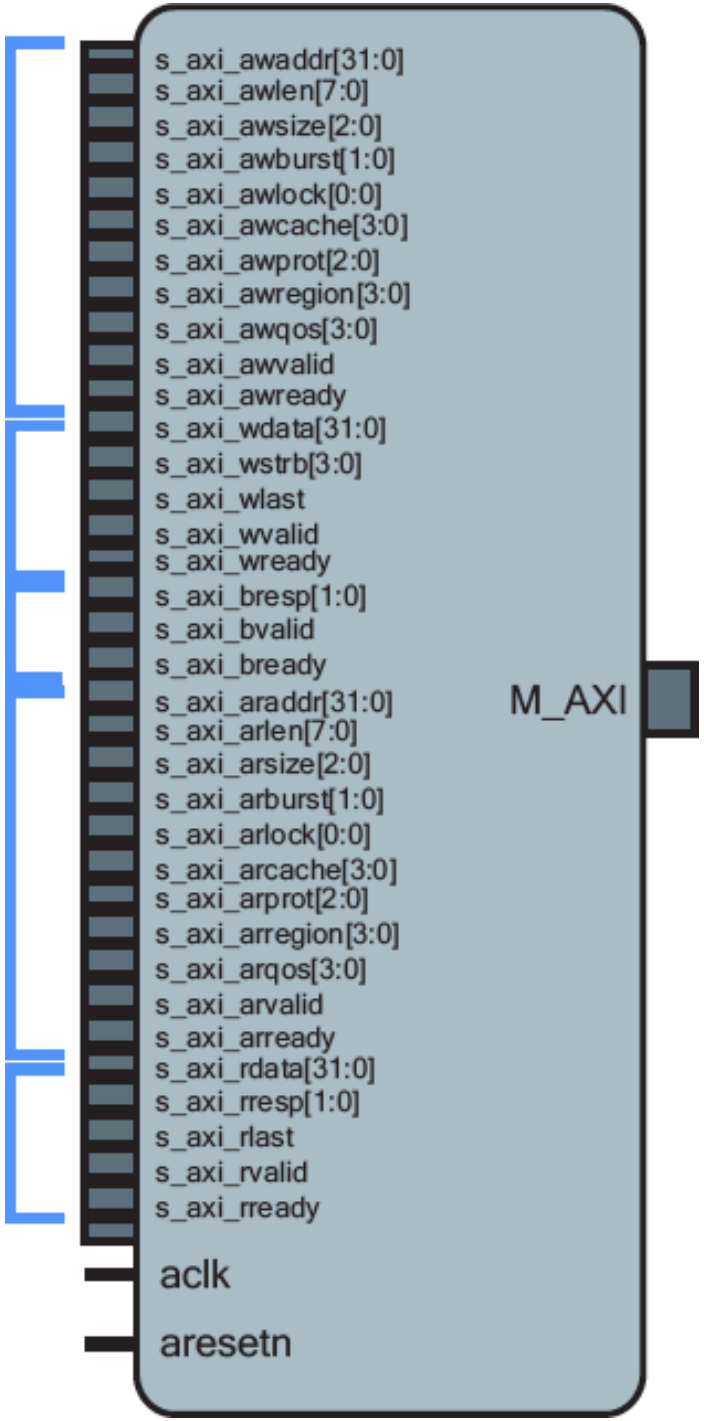
Write Address Channel

Write Data Channel

Write Response Channel

Read Address Channel

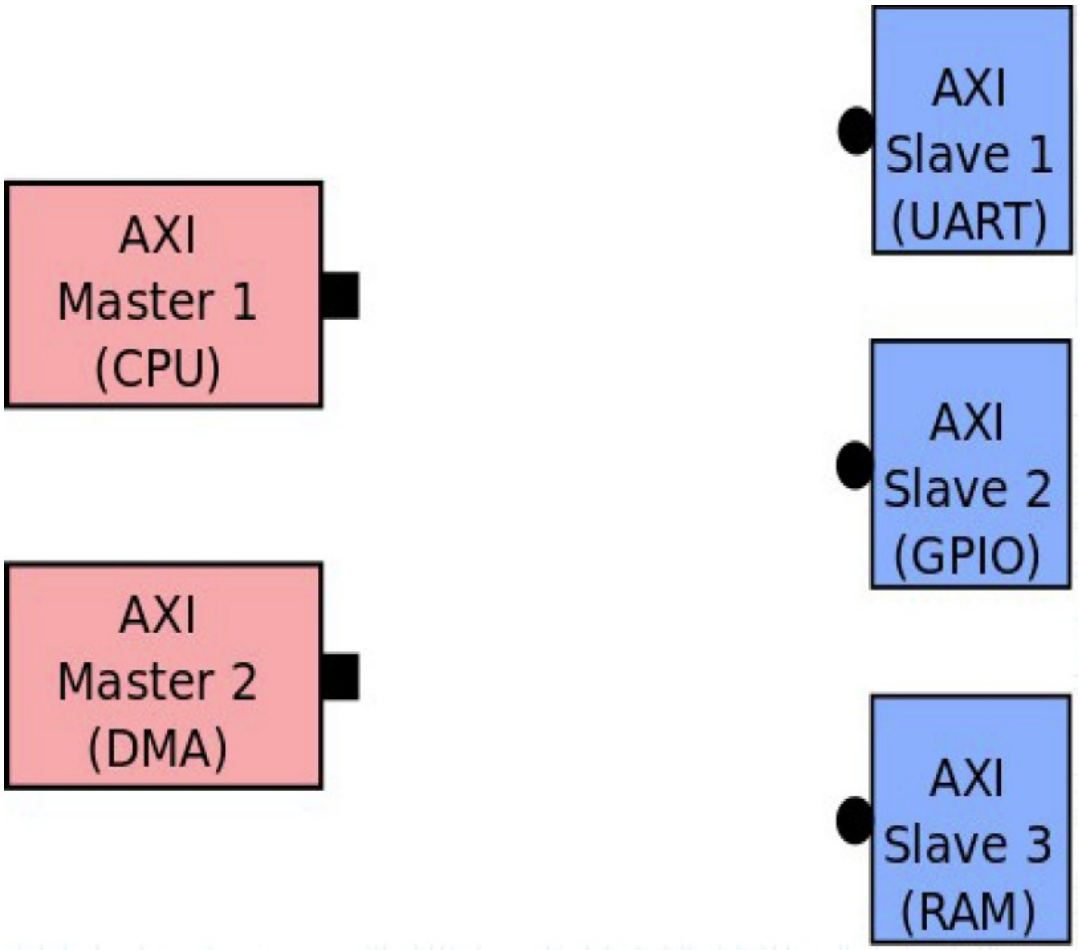
Read Data Channel



Source: The Zynq Book

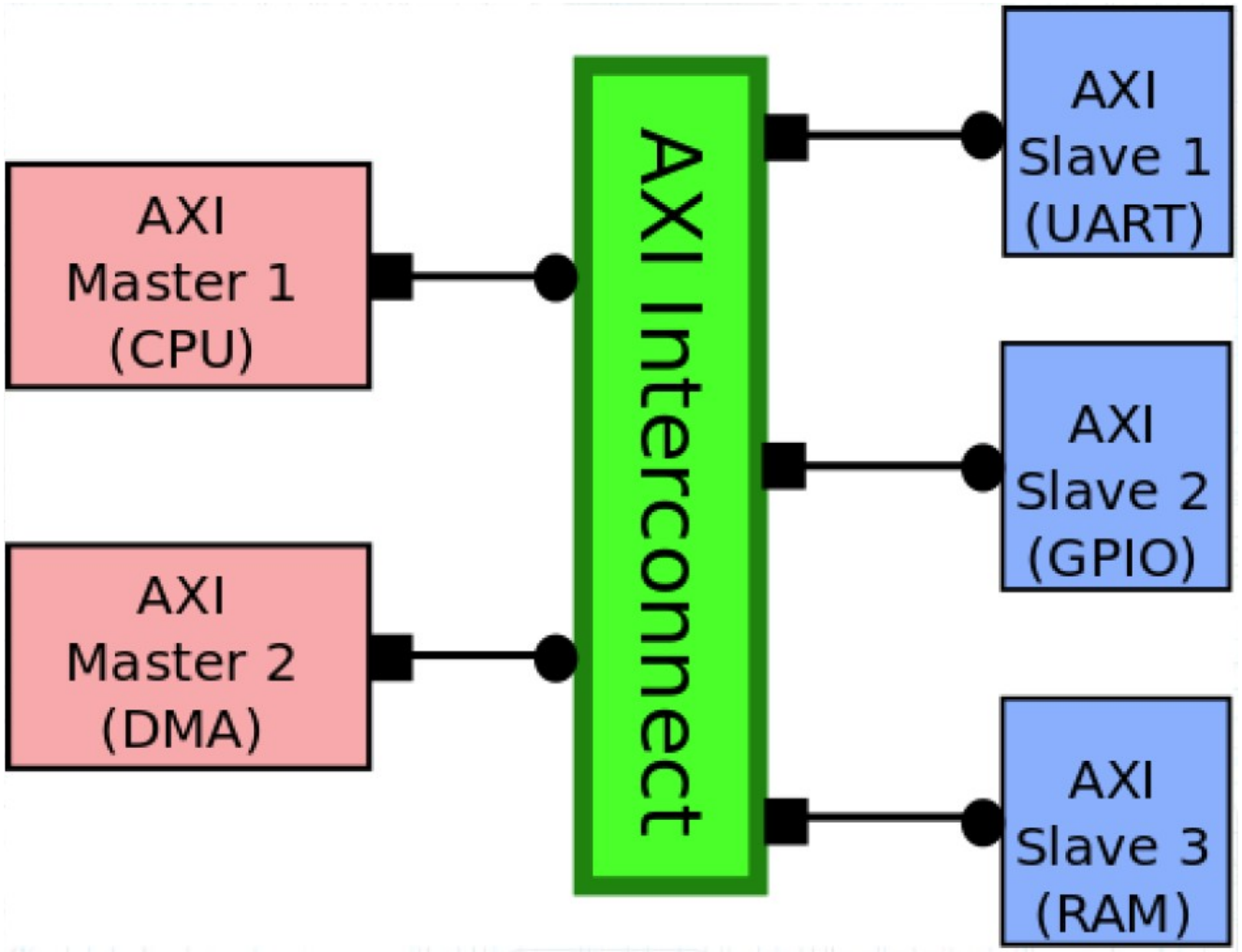
AXI INTERCONNECT

Connecting Masters and Slaves

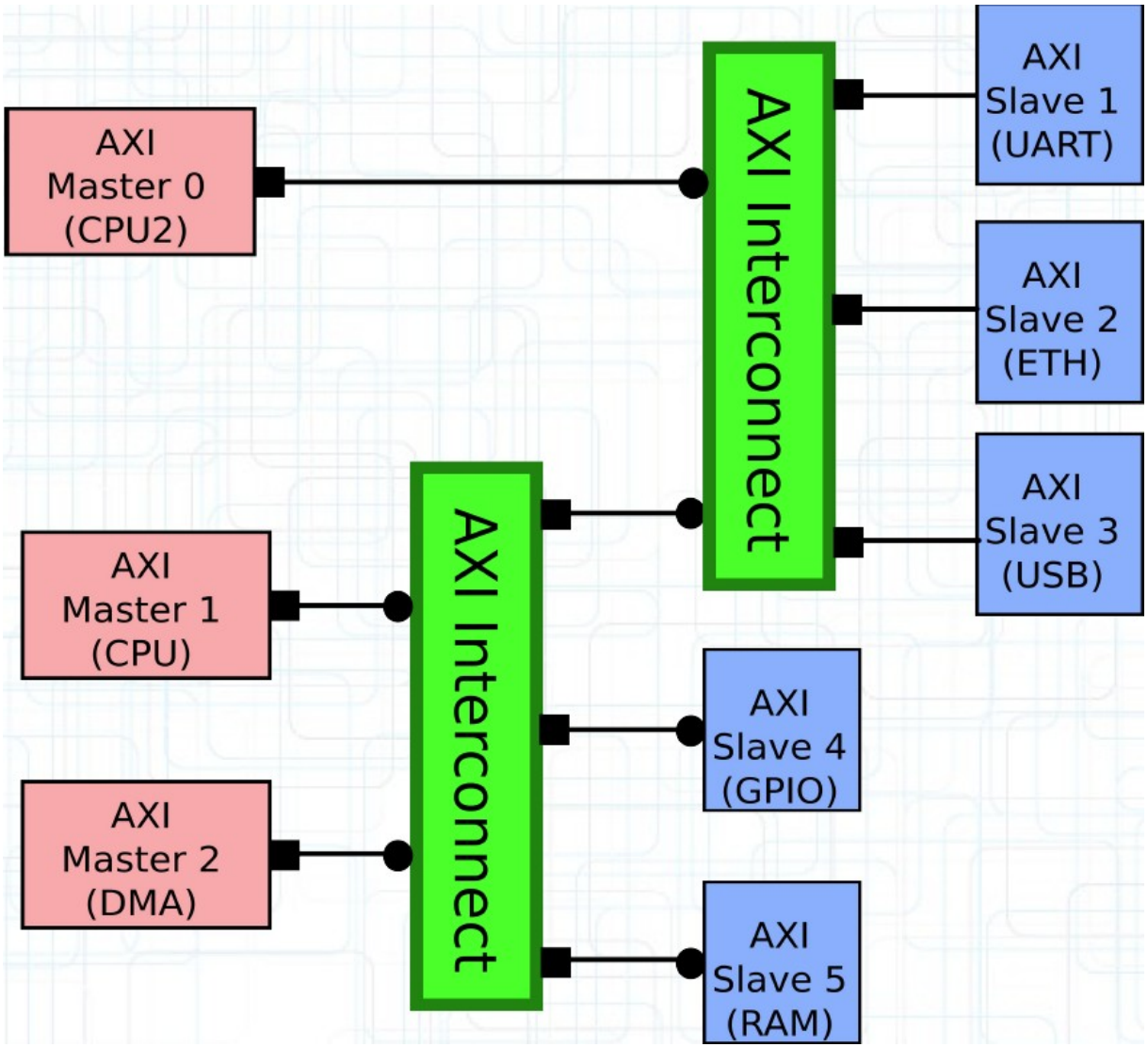


Source: M.S. Sadri, Zynq Training

AXI Interconnect

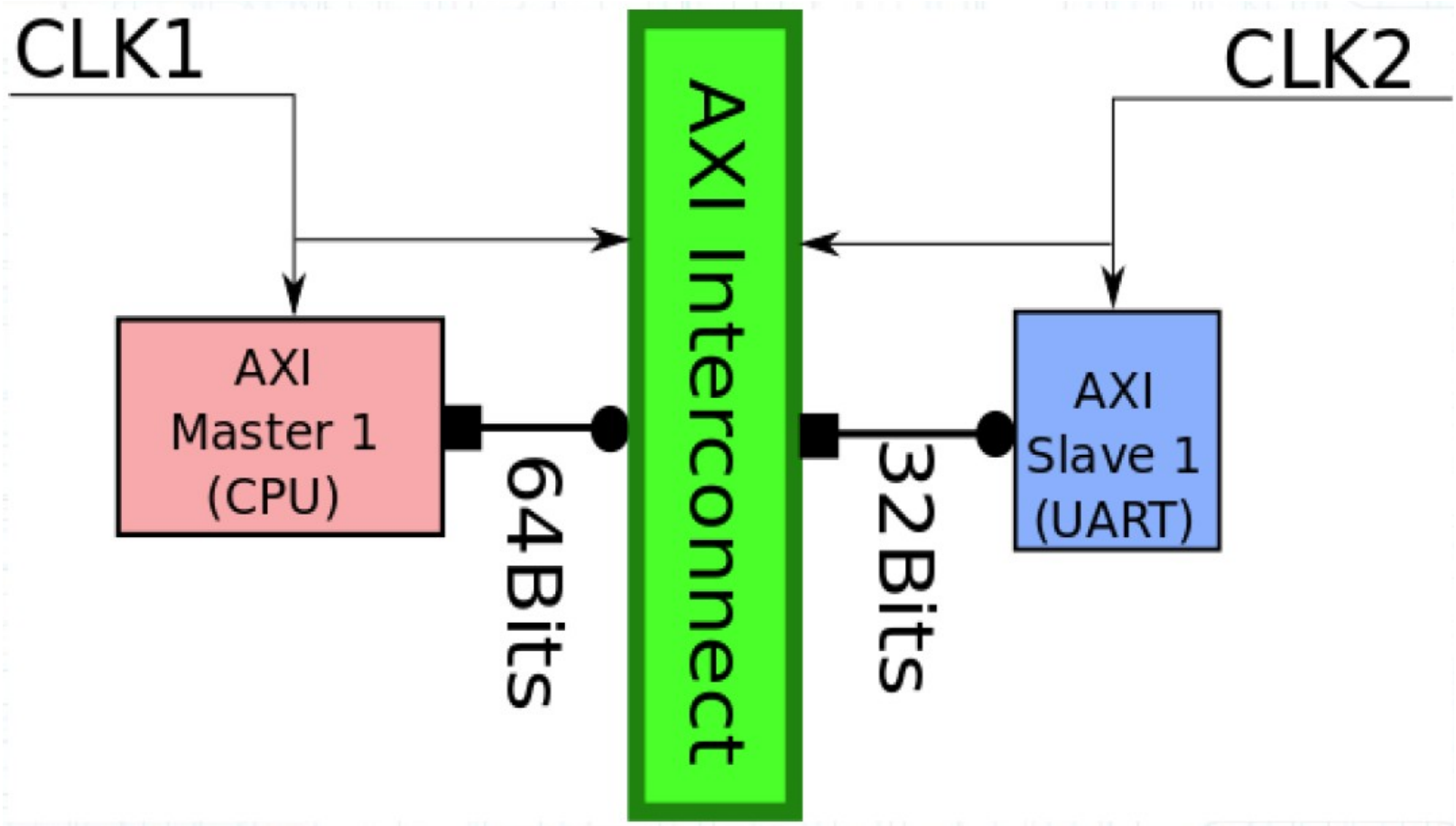


Hierarchical AXI Interconnects



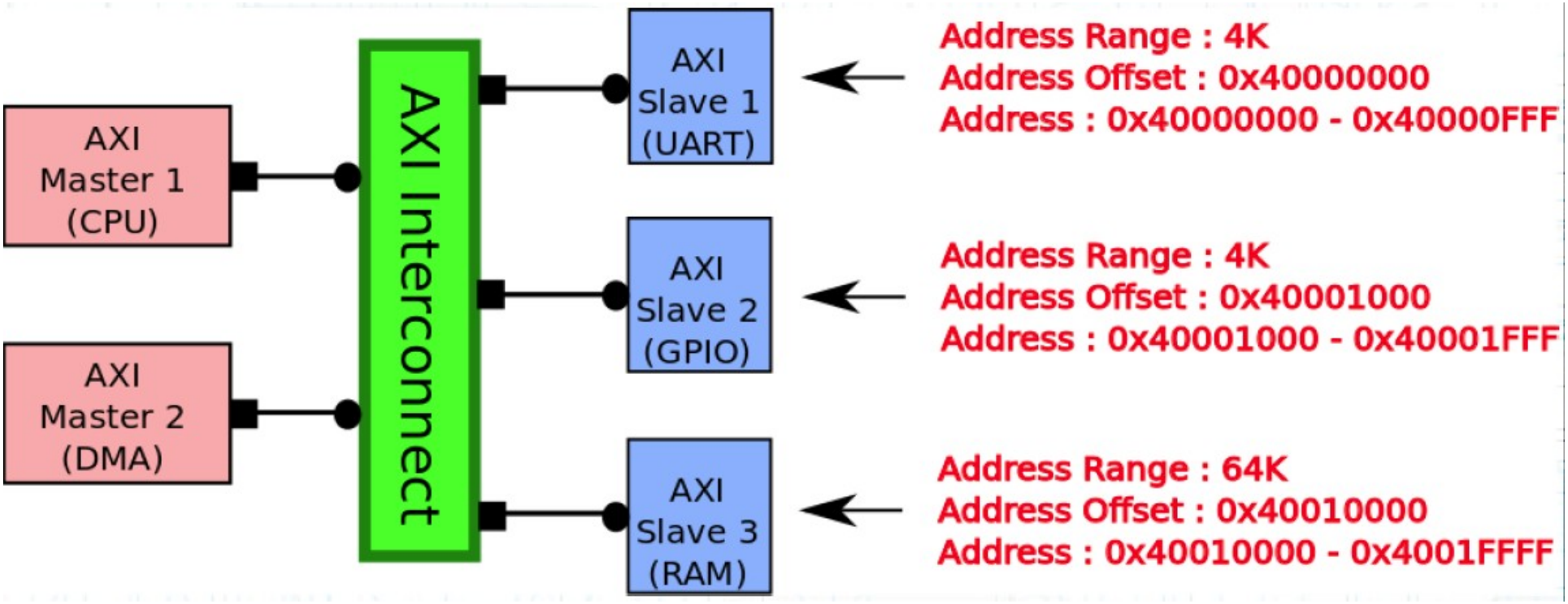
Source: M.S. Sadri, Zynq Training

Clock Domain and Width Conversion



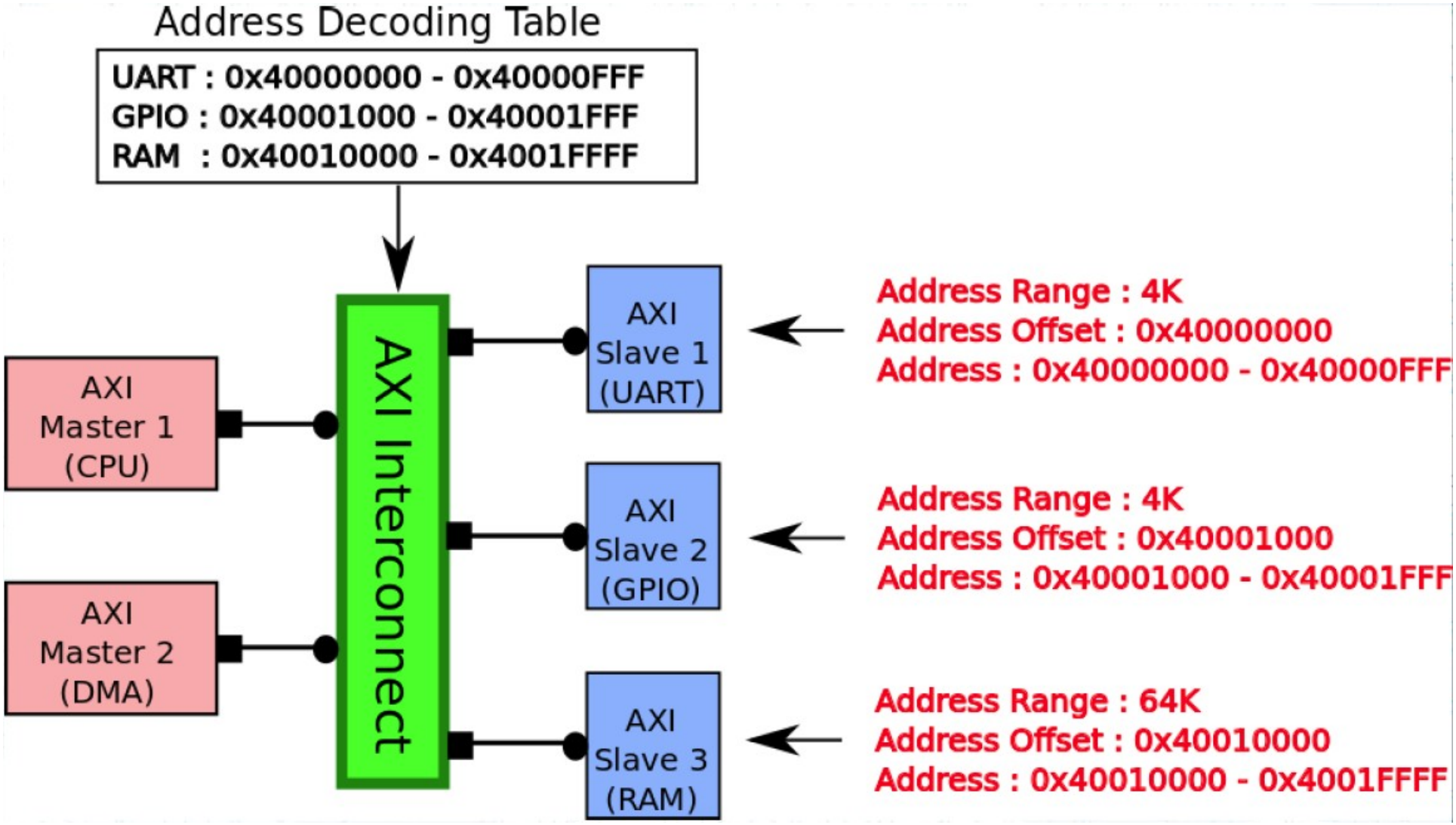
Source: M.S. Sadri, Zynq Training

Addressing of Slaves



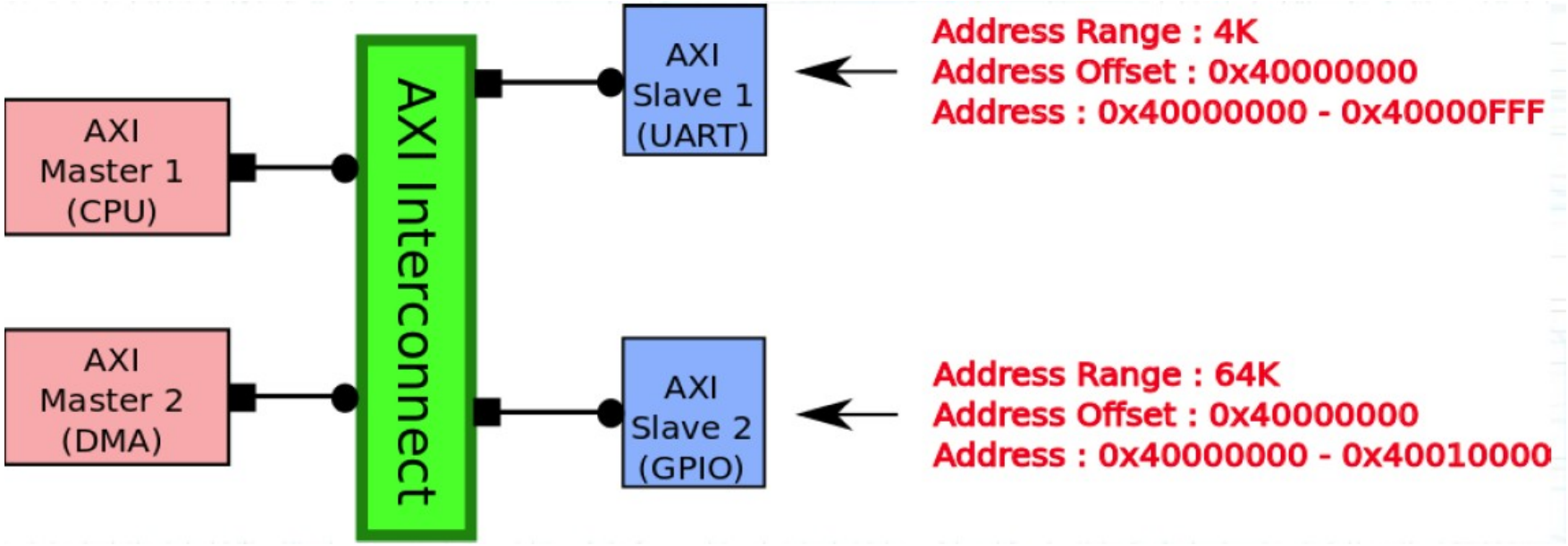
Source: M.S. Sadri, Zynq Training

AXI Interconnect Address Decoding



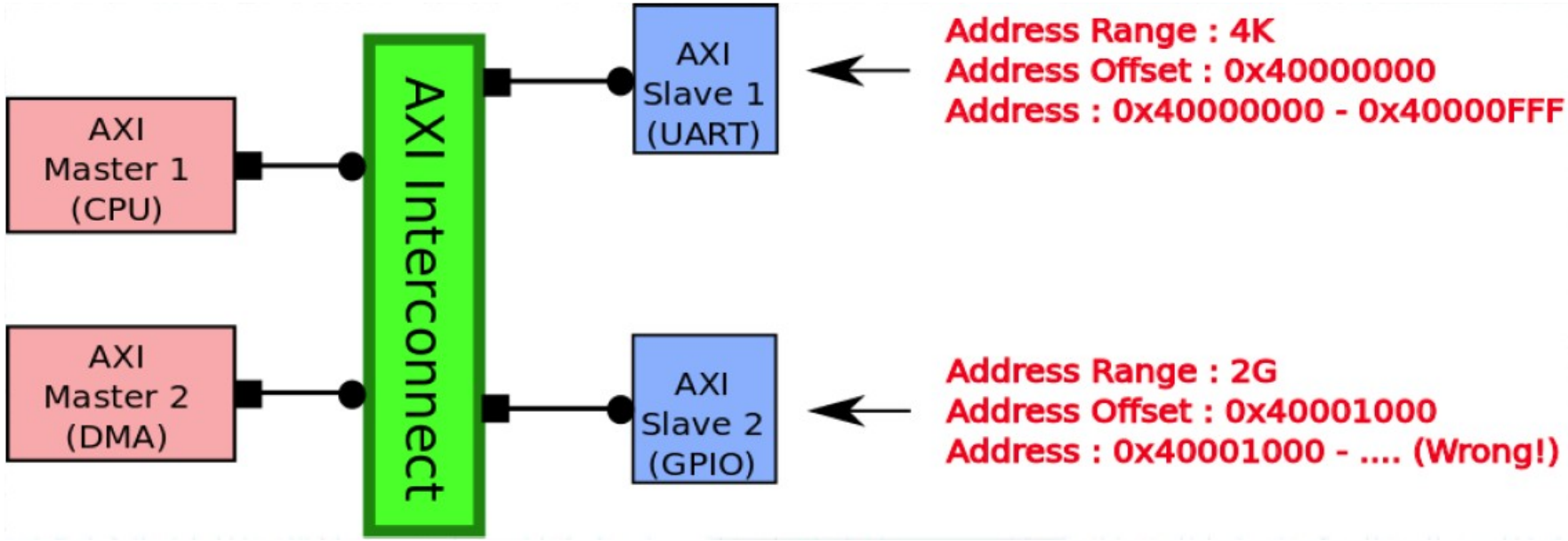
Source: M.S. Sadri, Zynq Training

Simple Address Definition Rules
No Overlaps



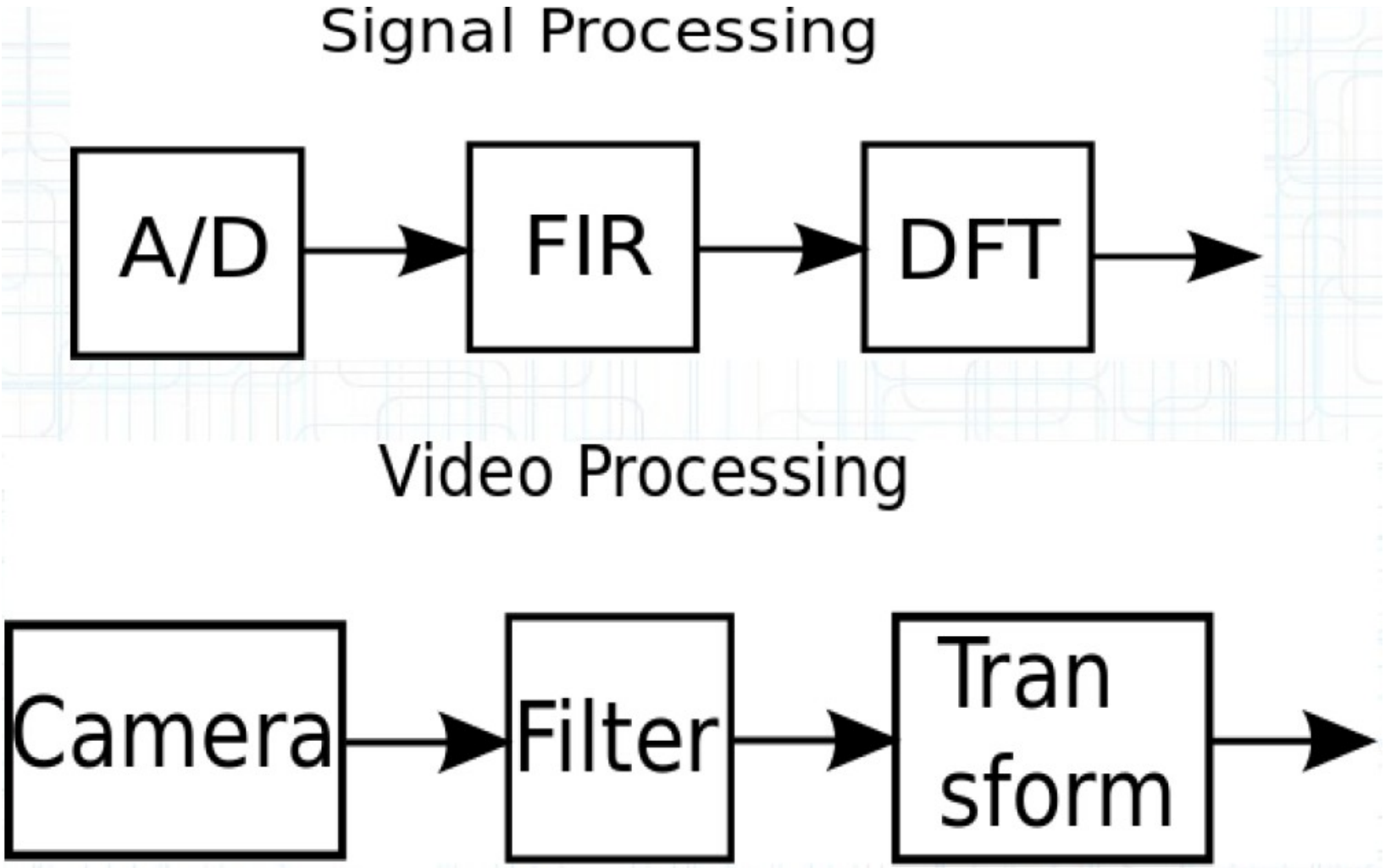
Source: M.S. Sadri, Zynq Training

Simple Address Definition Rules
Address Alignment



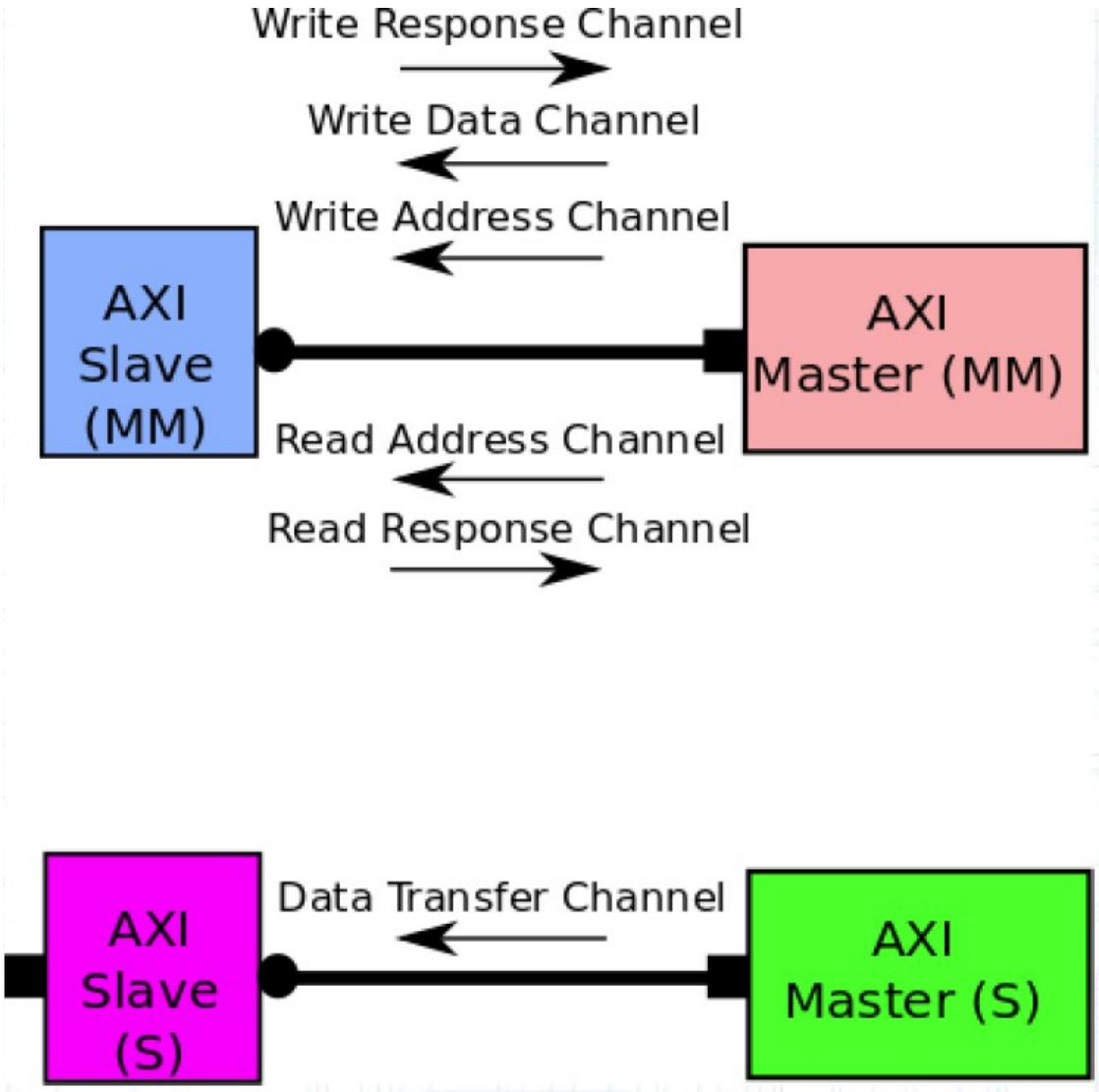
AXI4-STREAM

Point-to-Point Data Flows



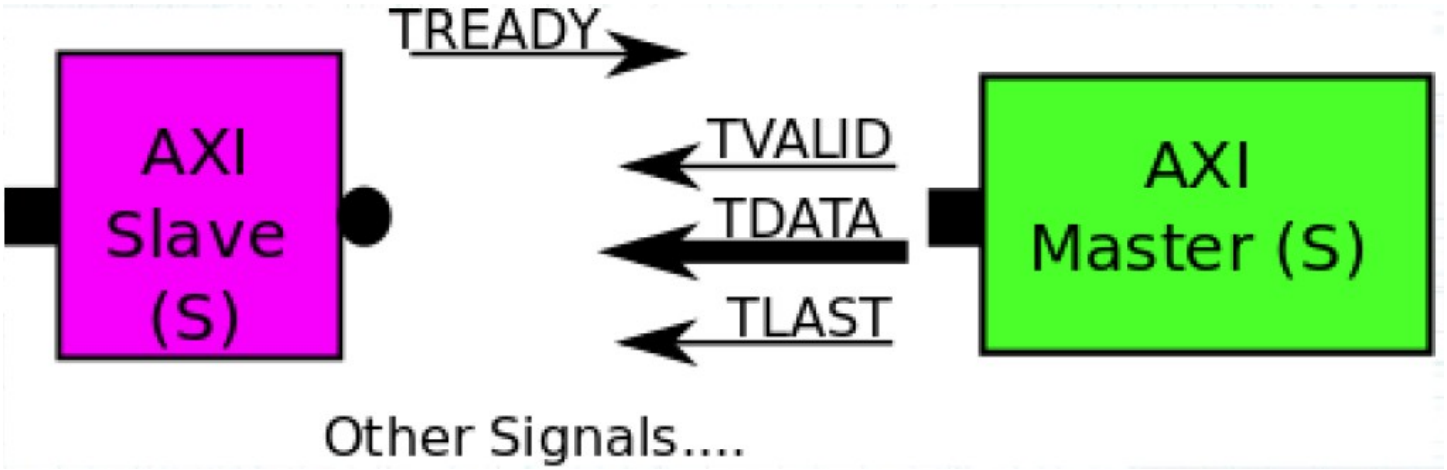
Source: M.S. Sadri, Zynq Training

AXI Memory-Mapped vs. AXI Stream



Source: M.S. Sadri, Zynq Training

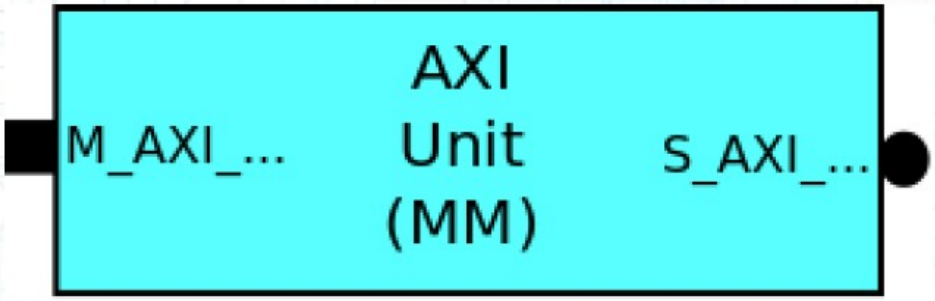
Selected AXI Stream Ports



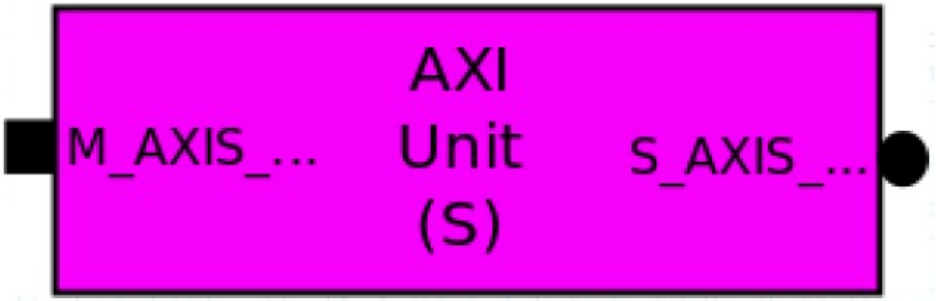
Source: M.S. Sadri, Zynq Training

AXI Port Naming Conventions

- Memory Mapped



- Stream



- Signal names:
  - e.g. S_AXI_awid, M_AXI_arready ….

Source: M.S. Sadri, Zynq Training