Lecture 7

Clocking continued

Quick Review

- Synchronous
- Mesochronous
- Plesiochronous
- Asynchronous

GENERAL PURPOSE ASYNCHRONOUS CLOCK CROSSING

Observe

- Can build mesochronous and plesiochronous synchronizers with no failure probability

Asynchronous Clock Crossing

- Most common scenario in ASIC/FPGA design
- Non-zero probability of failure
- Can only reduce probability

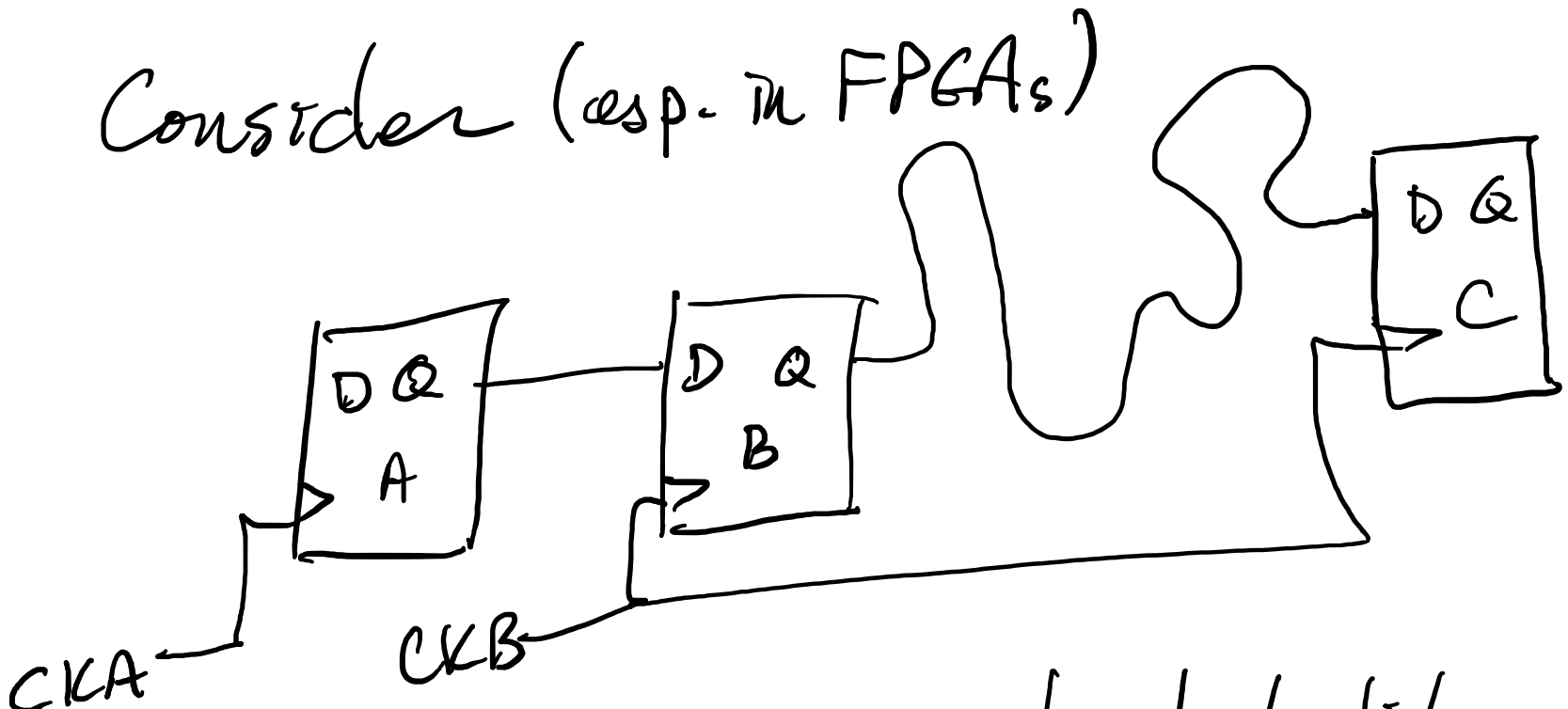
Basics Again

Crude Exercise

Crossing 1 Signal

Solution

One More Thing

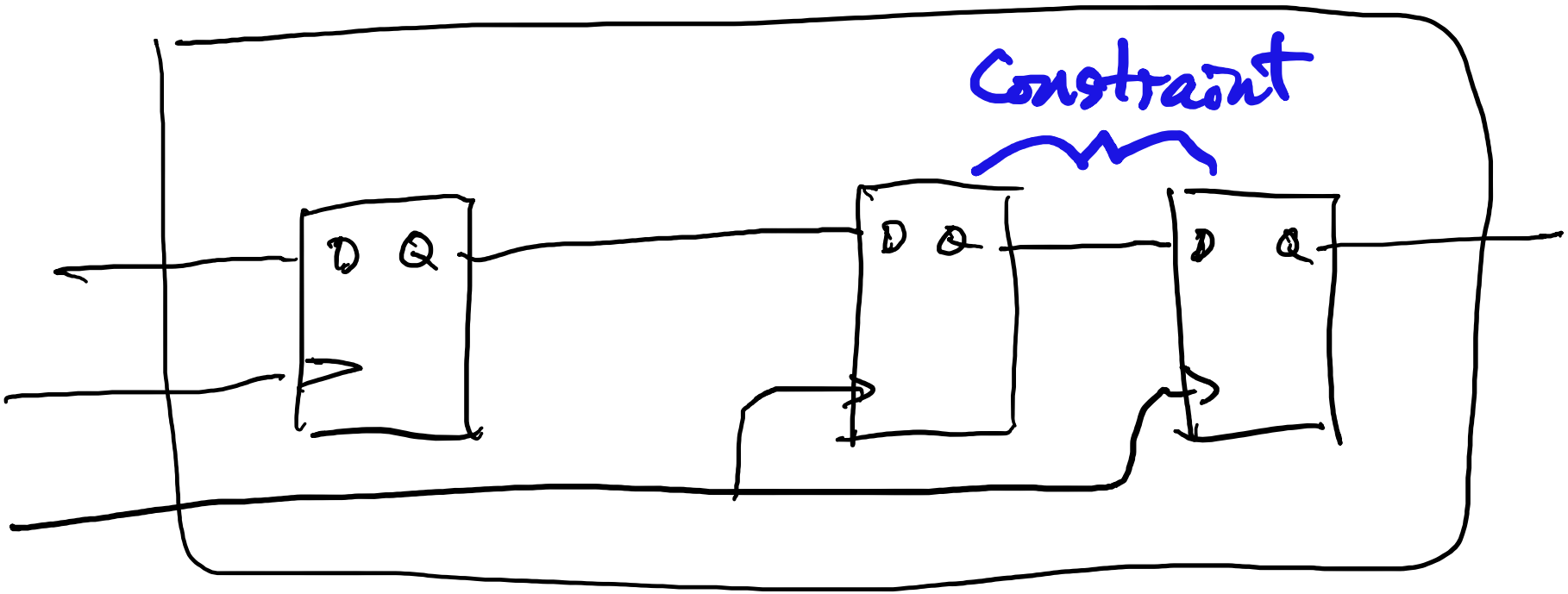


C can still see metastability at input

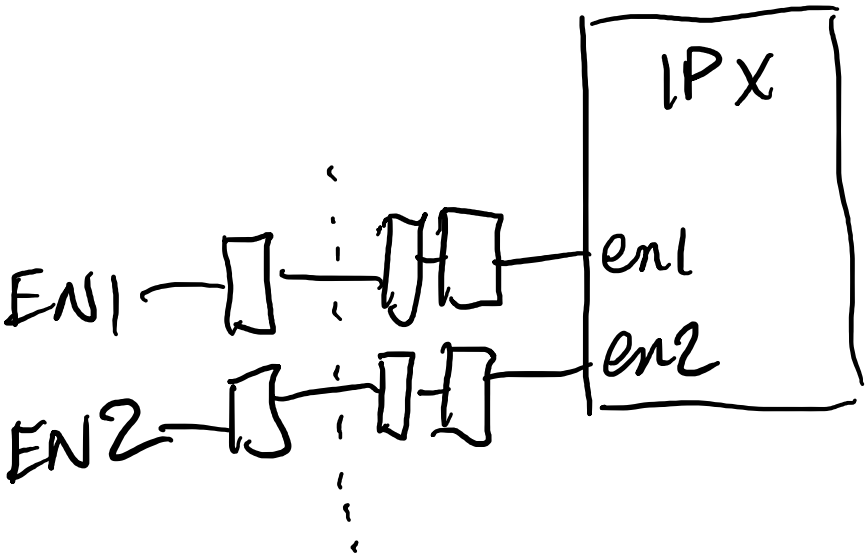
Why?

The Fix

Synchronizer Block

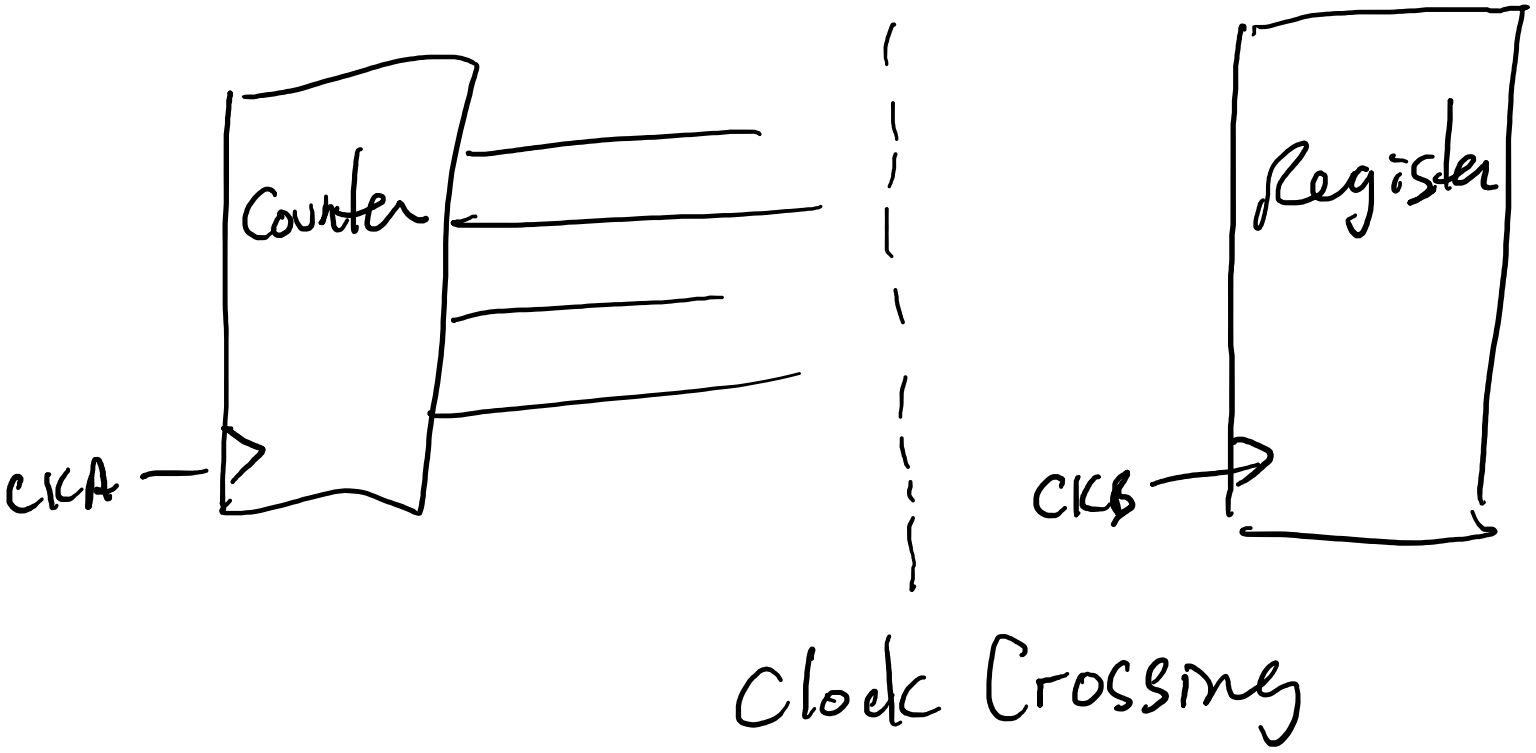


Multiple Control Signals

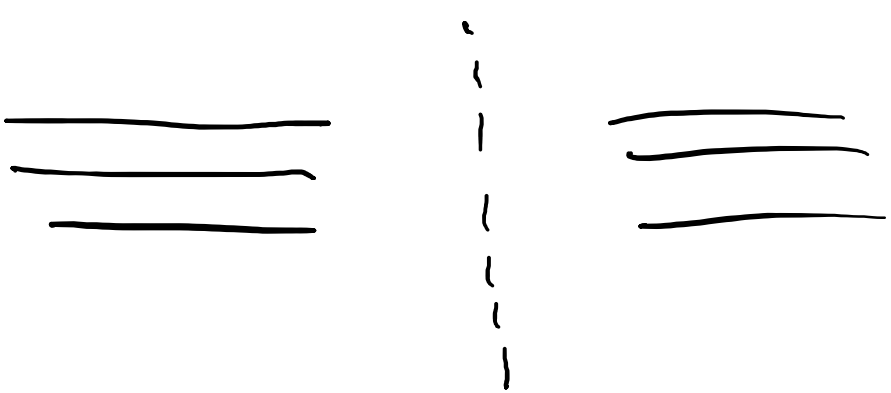


EN1 & EN2 Change at same time

Counter

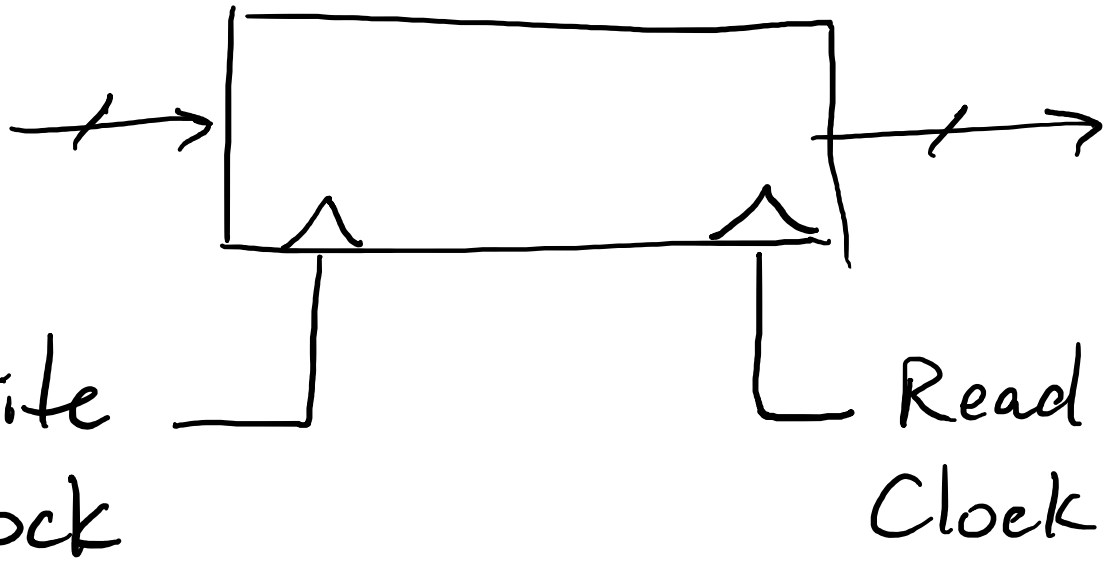


Datapath – Bus



Again, multiple bits crossing

FIFO



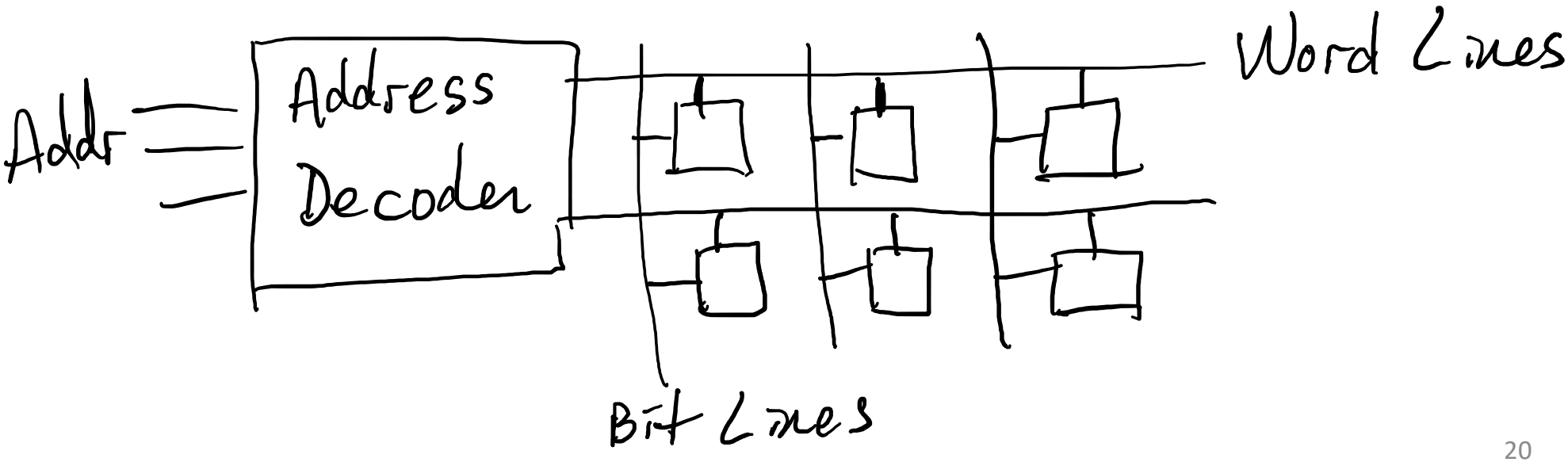
Synch: Write Clock = Read Clock
Rate matching

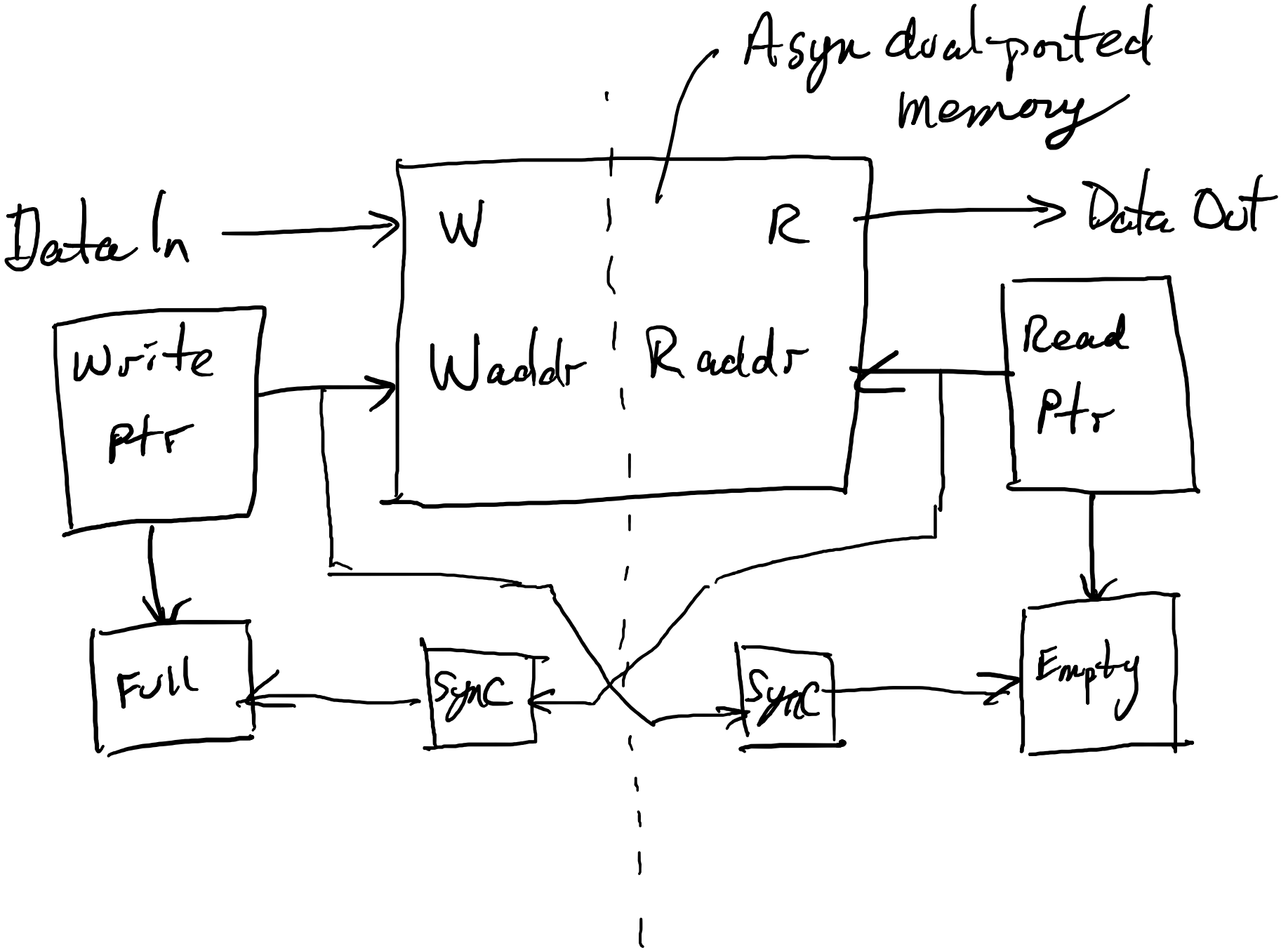
Asynch: Also for Clock Crossing

Use a dual-ported Asynch memory

Asynch memory

- address in → data out
- all combinational



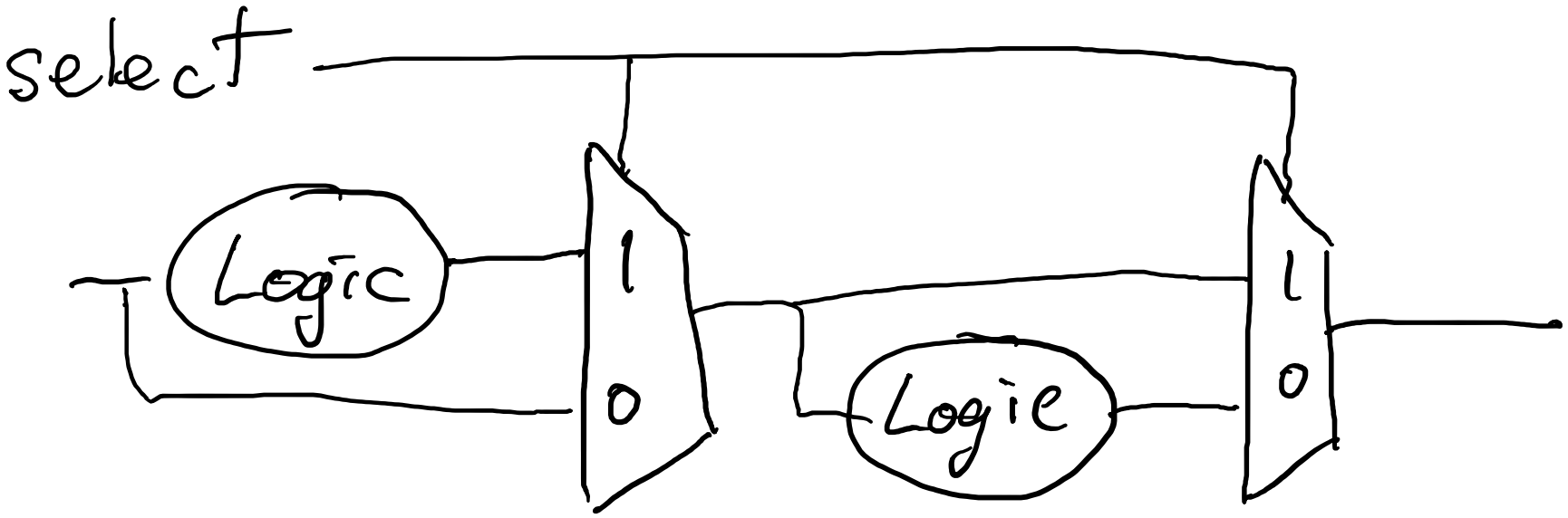

Asyn dual-ported memory
Data In
W
R
Data Out
Write Ptr
Waddr
Raddr
Read Ptr
Full
Sync
Sync
Empty

STATIC TIMING ANALYSIS (STA)

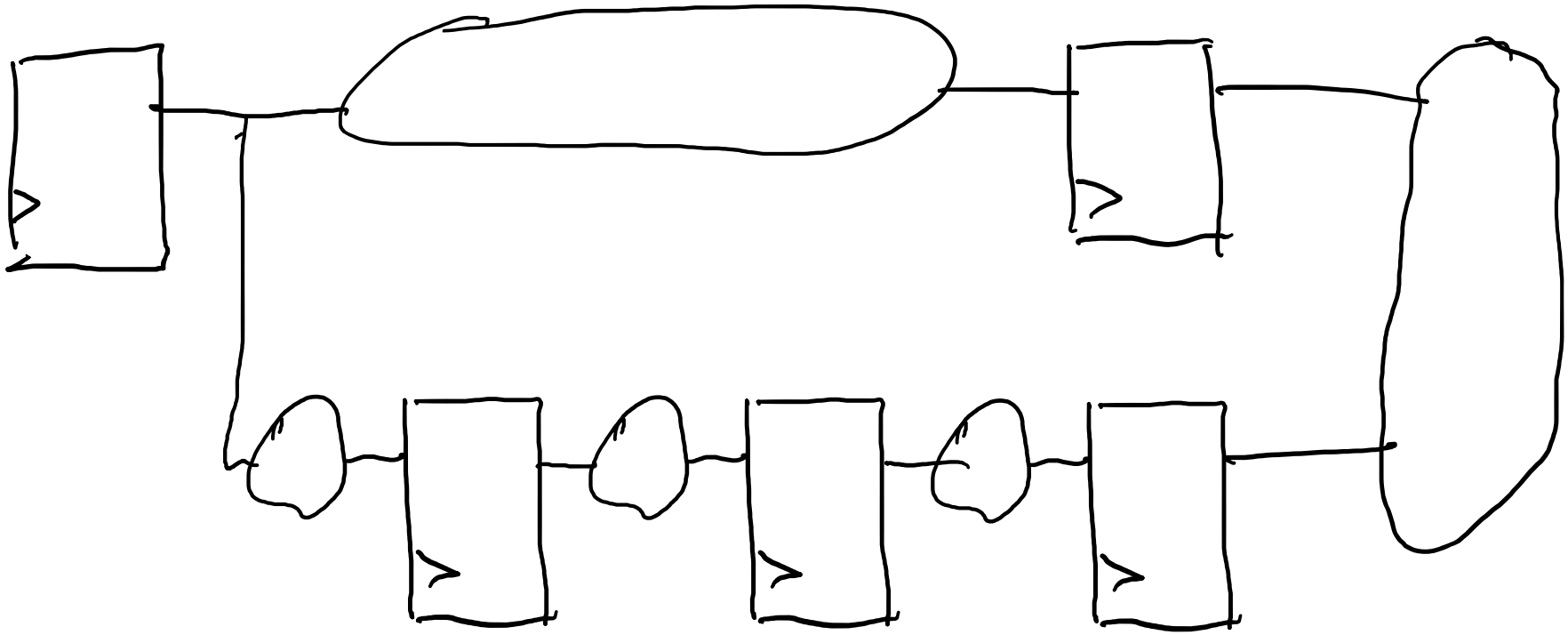
Timing Simulation

Static Timing Analysis

False Path



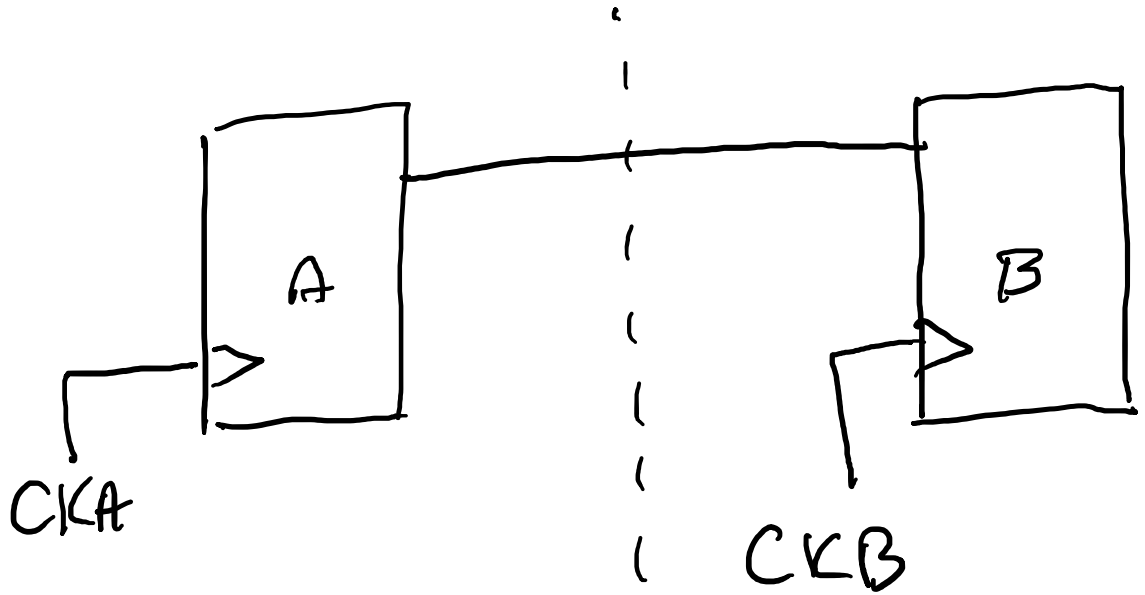
Multi-cycle Path



Constraints and P&R Time

Timing and Clock Crossing

Synchronizer



STA

Simulation

Style: Partition