Clocking

Overview

- Multi-clock designs
- Synchronizers
  - Mesochronous
  - Plesiochronous
  - General-purpose asynchronous clock crossing
    - Single bit
    - Multiple bits
    - Buses
    - FIFOs

Overview Continued

- Static Timing Analysis (STA)
- Clock distribution
- Clock generation

MULTI-CLOCK DESIGNS

References

- Synthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs
  - Cliff Cummings
    - Has many
    - excellent papers about hardware design
- Digital Systems Engineering, Dally and Poulton, Ch. 10

Scenario

- Passing information from one *clock domain* to another

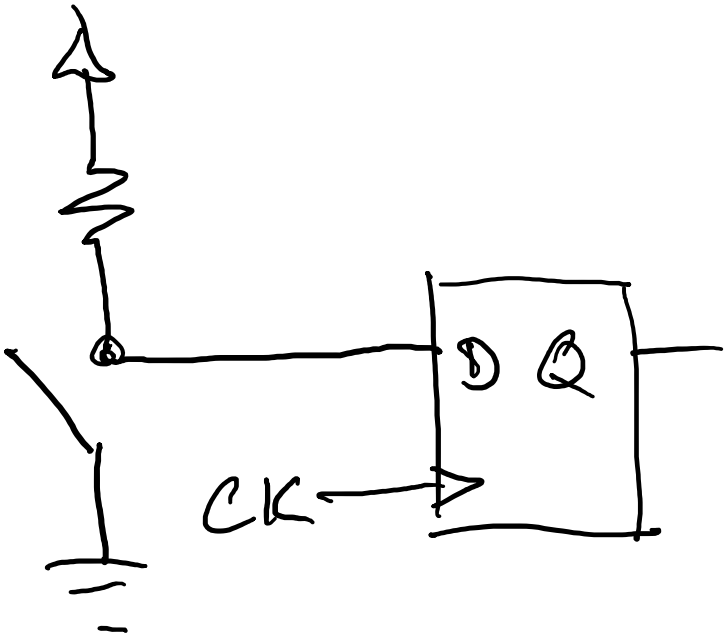
Clock Domain

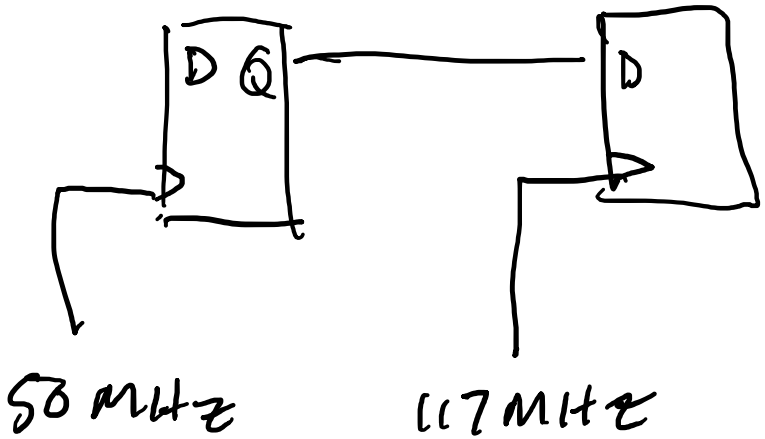
Classification of Clocking Scenarios

- Recognize and know what to do
  - Asynchronous
  - Synchronous
  - Mesochronous
  - Plesiochronous

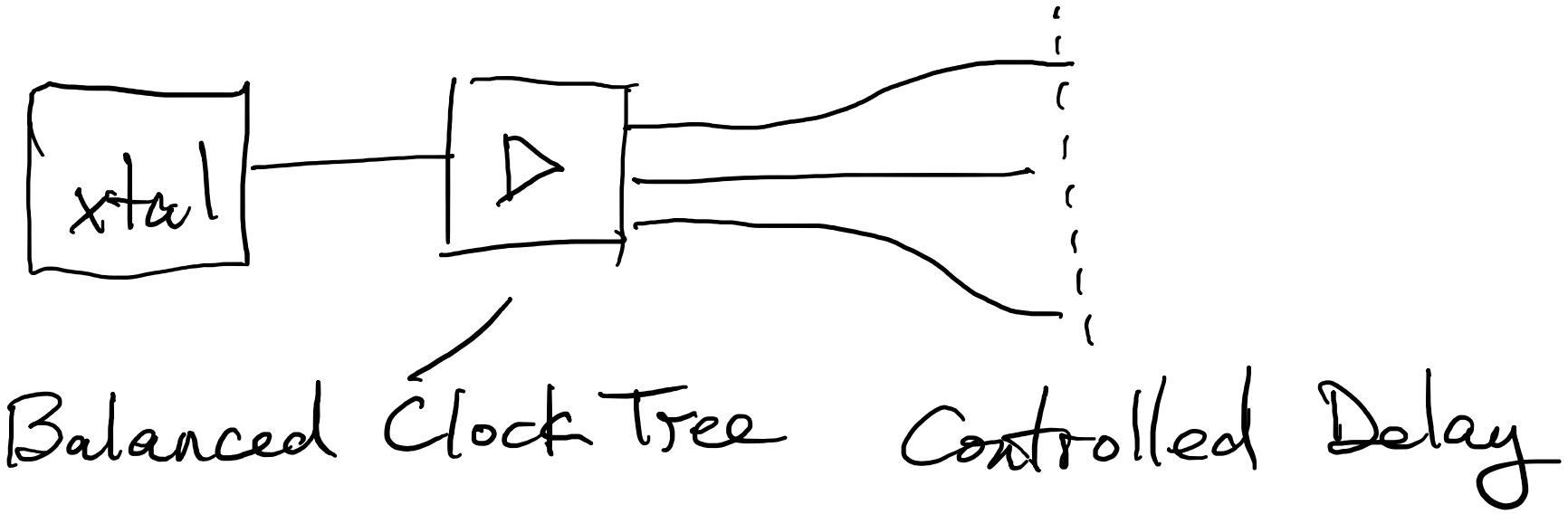
Asynchronous

- Source signals occur at arbitrary times
- No phase relationship between source and receiver clocks

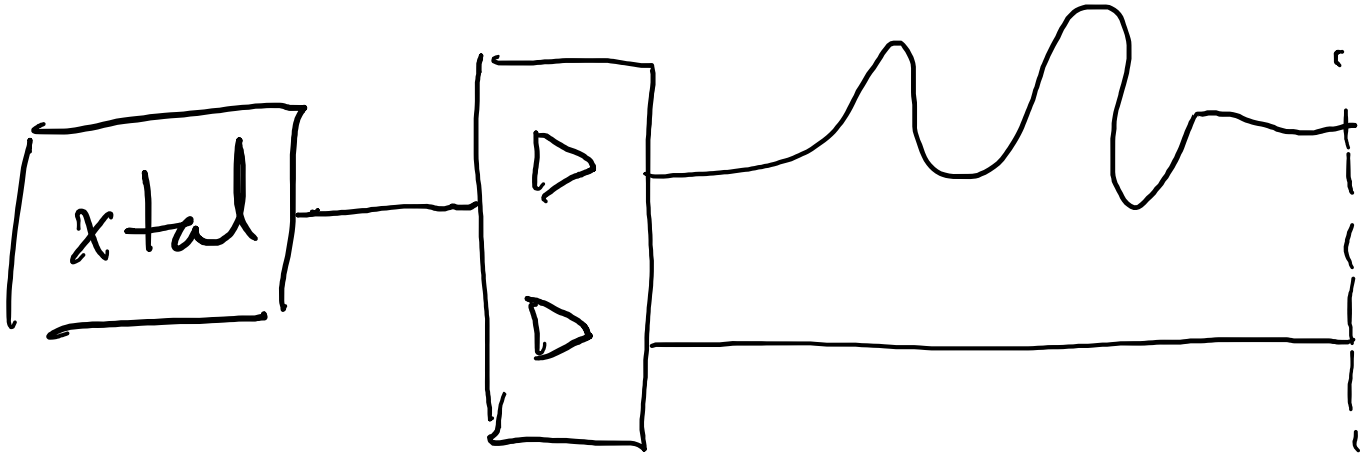




Synchronous



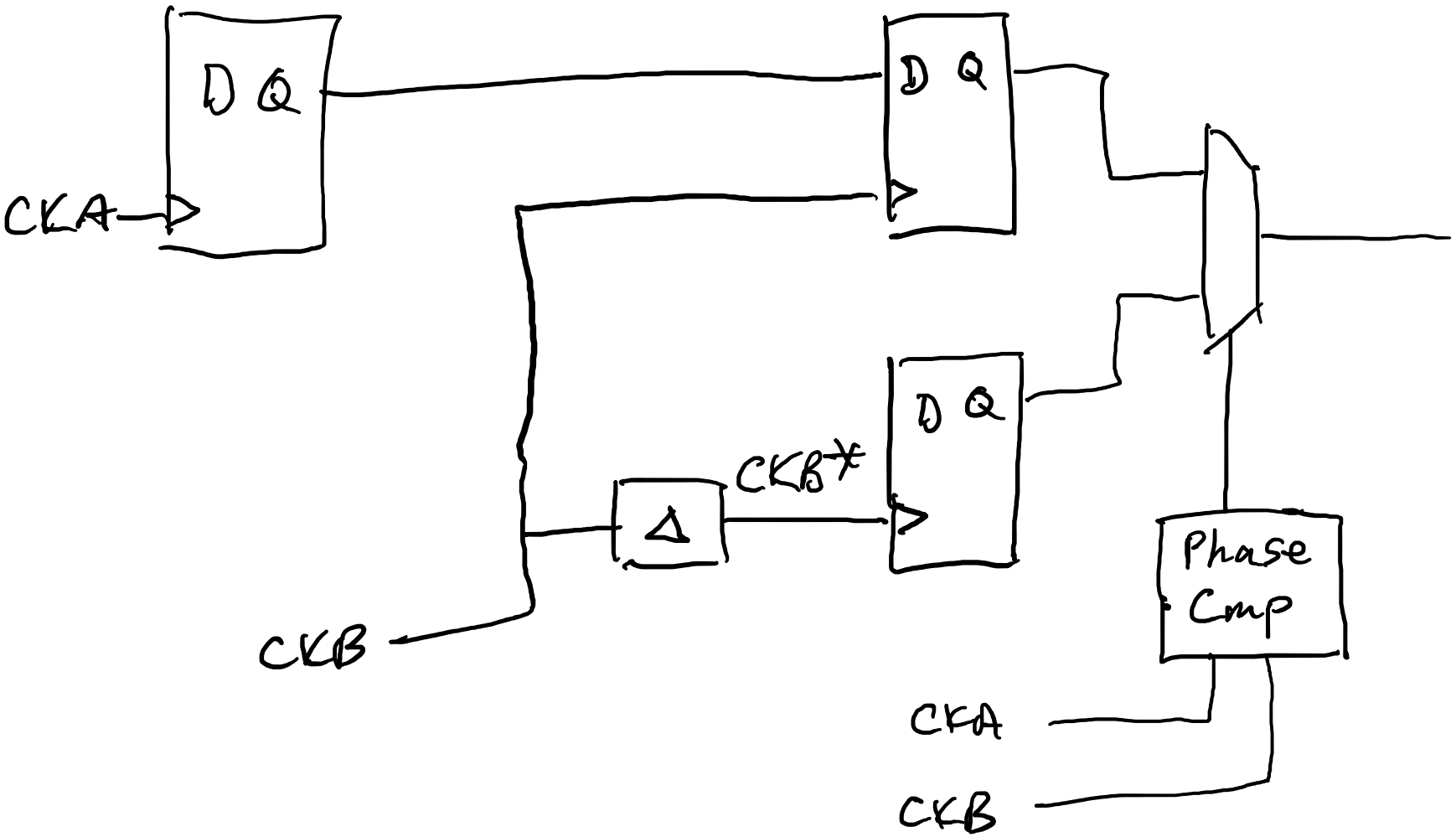
Mesochronous

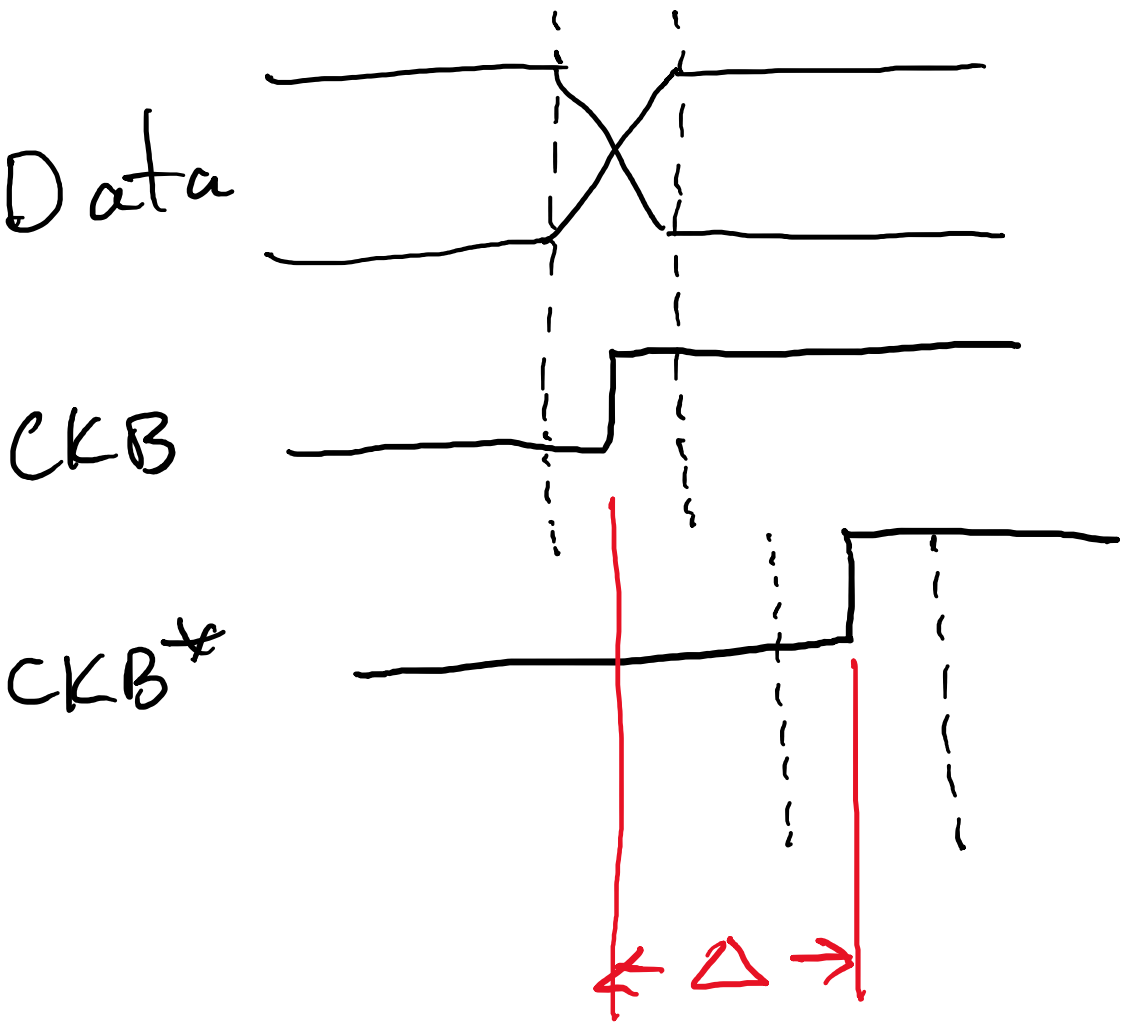


Example: GALS

Globally Asynchronous, Locally Synchronous

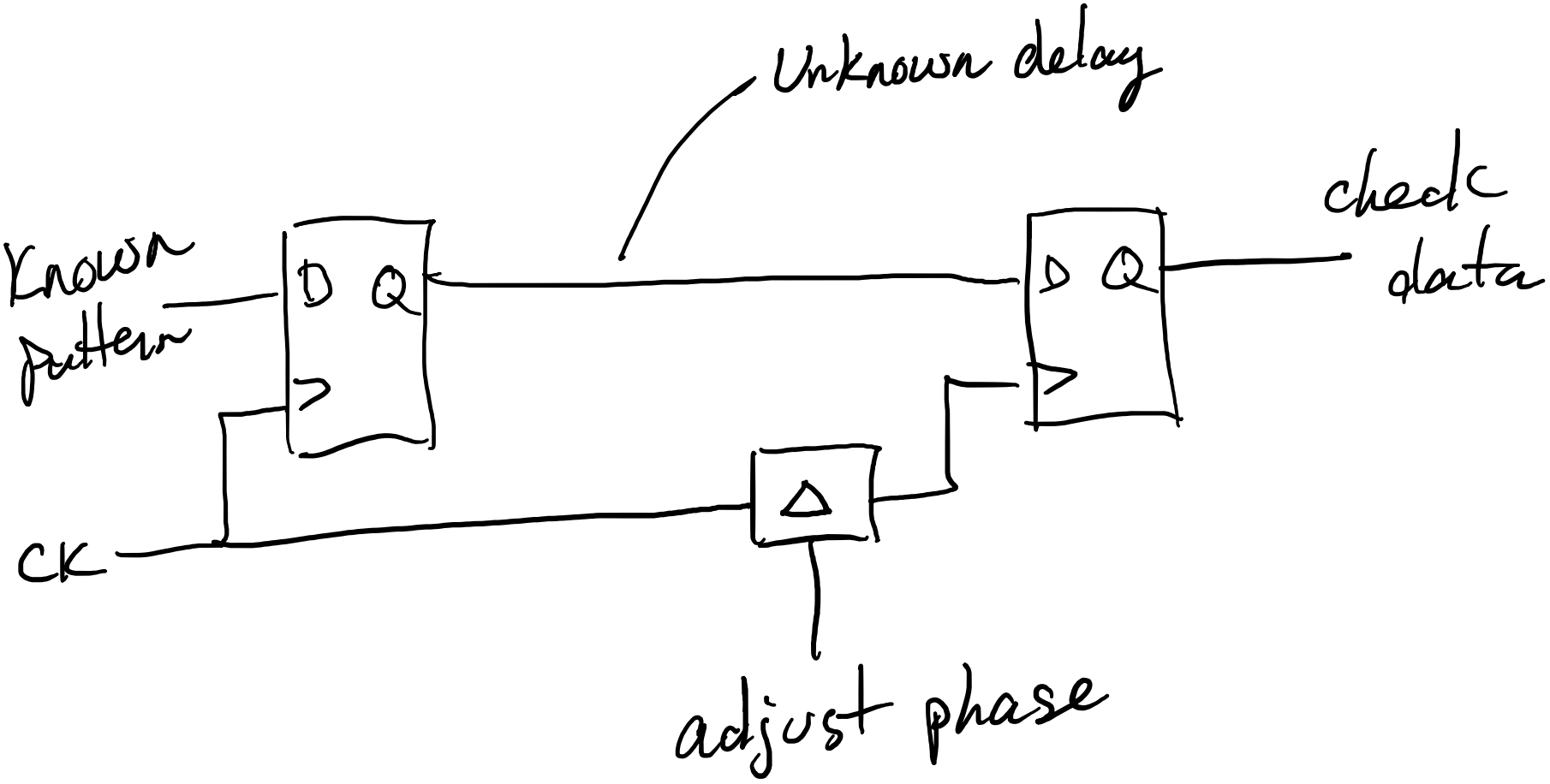
Mesochronous Synchronizer



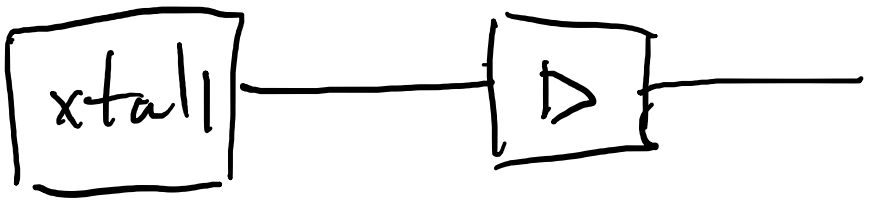


Δ is large enough such that if Data transitions in CKB Keep out then it cannot be transitioning in CKB* Keep Out
— could use $\overline{CKB}$

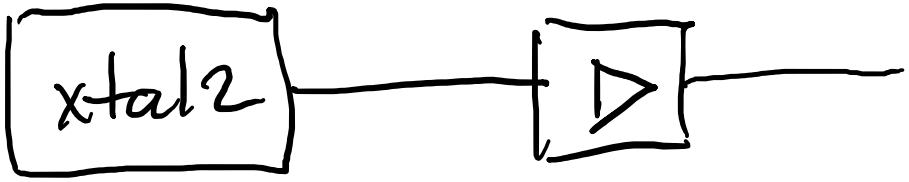
Training


Unknown delay
Known pattern
D Q
D Q
check data
CK
adjust phase

Plesiochronous



100 MHz
20 ppm



100 MHz
20 ppm

$$\frac{2\ \text{kHz}}{100\ \text{MHz}} = 1.73\ \text{s/day}$$

SONET - Synchronous Optical Network

Plesiochronous Synchronization

Slip bits

Flow Control