ECE1373S

2021

Lecture 2

High-Level Synthesis

Admin

- Assignment 1 released – due Feb. 10 11:59pm
- Think about projects, teams
- HLS labs and tutorials

Levels of Abstraction

Software

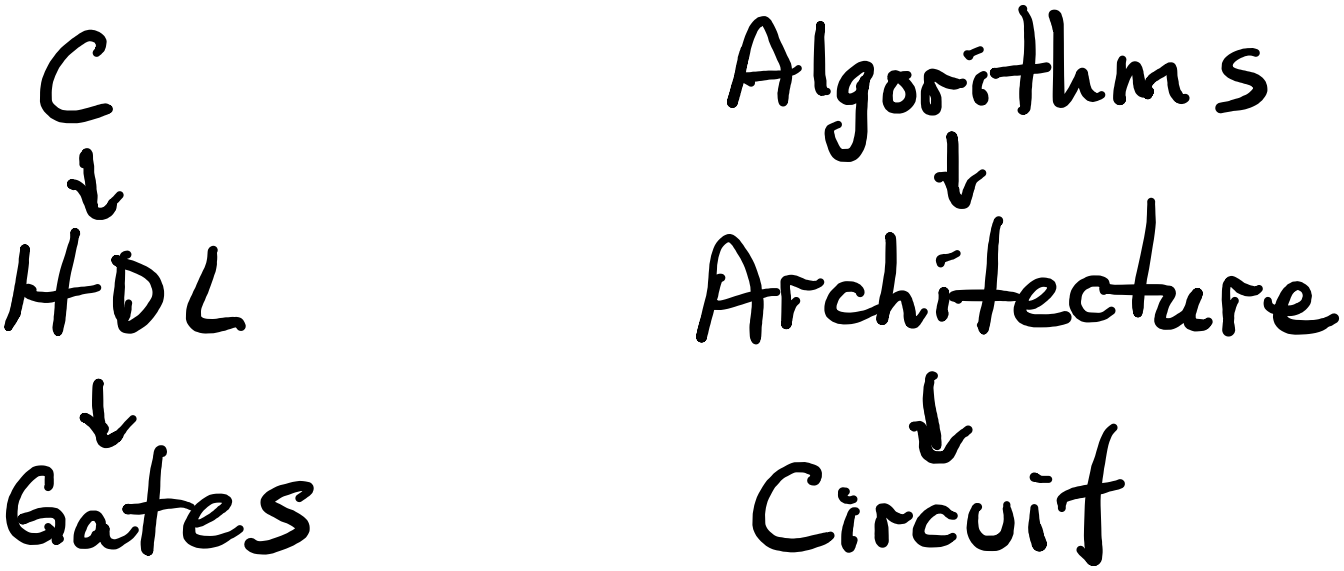
- Describe an algorithm
- Loops, branches
- Memory model
  - Arrays, data structures
- Hierarchy: functions, procedures

HDL

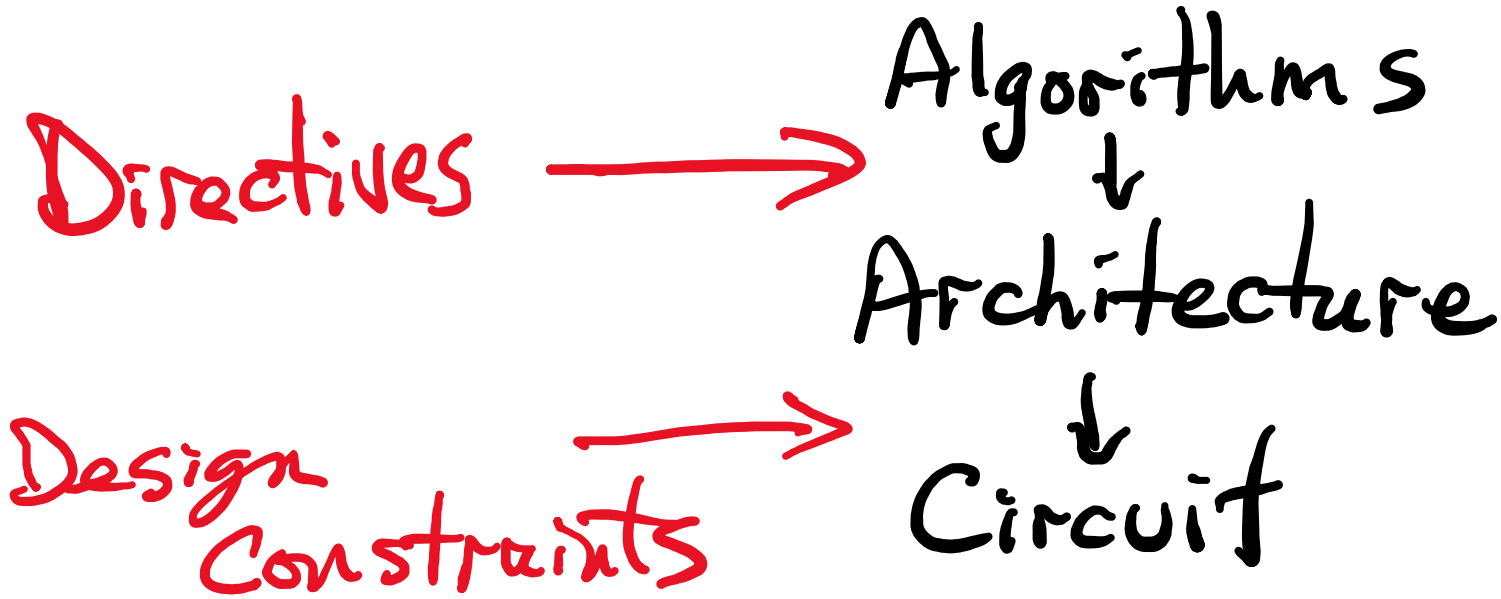
- Describe an architecture
  - Data path
- Control: FSMs
- Memory
  - Registers
  - Memory blocks (Address, data)
- IP blocks, modules

High-Level Synthesis

It's about levels of abstraction

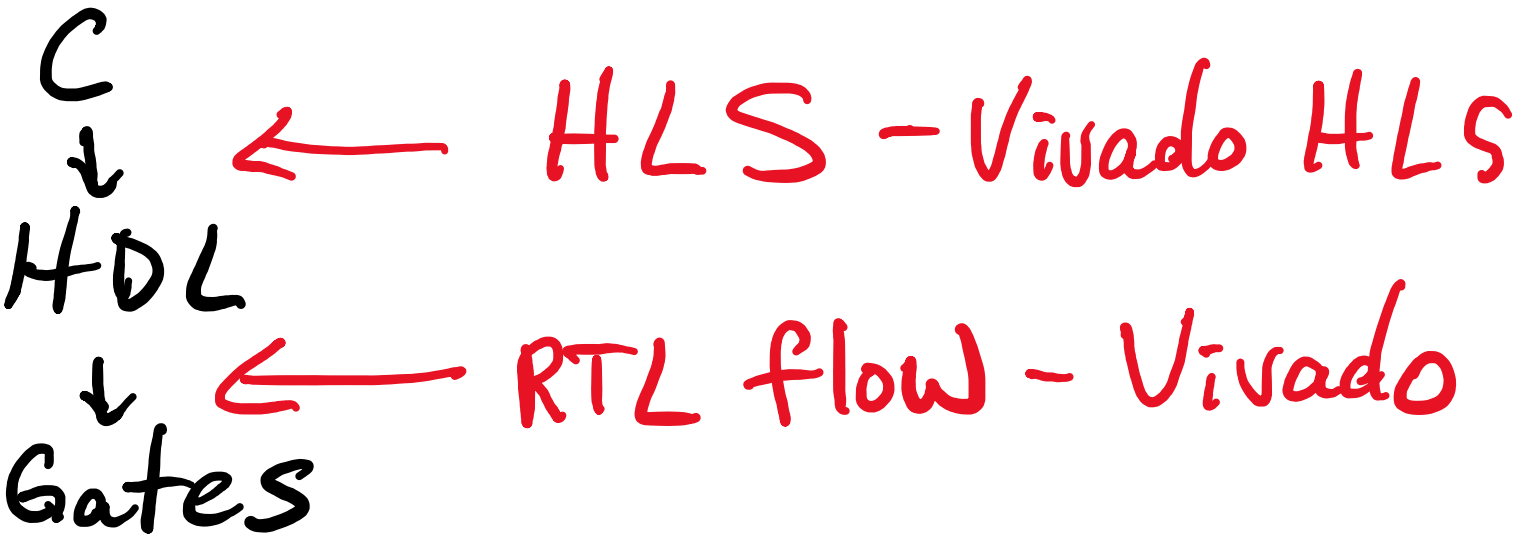


High-Level Synthesis



High-Level Synthesis

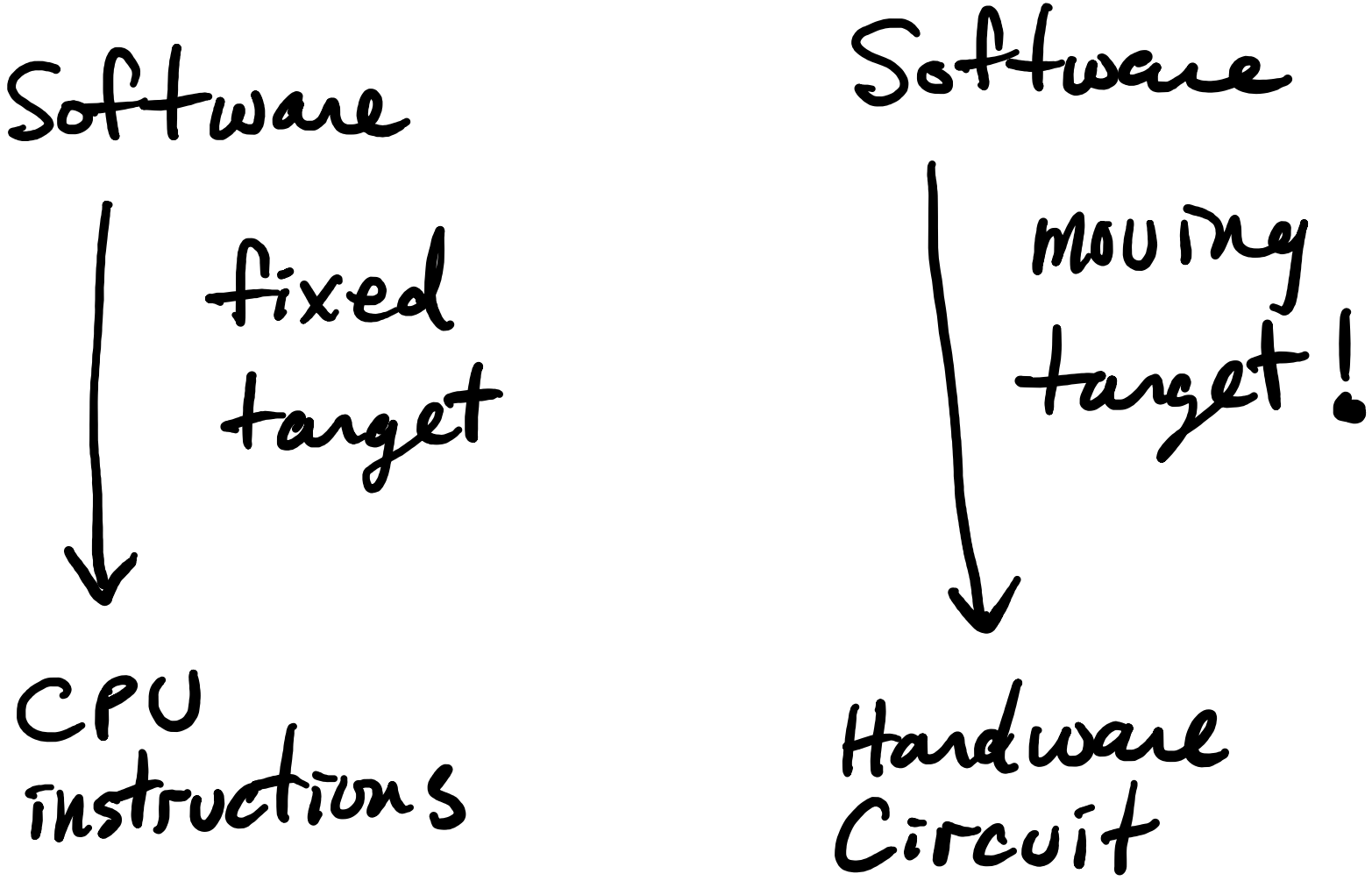
Tool Flow



Important Mind Set

- You are writing ``software'' but really describing hardware
- Hardware is static, i.e., does not change
- Cannot write software that does not describe a static functionality
  - No recursion
  - No dynamic memory allocation
  - No variable loop bounds (some exceptions)
  - **What is the hardware that will implement this?**

Tool Complexity



Xilinx Workshop

- Keep the above in mind as we go through the Xilinx workshop slides
- Piazza Post @20