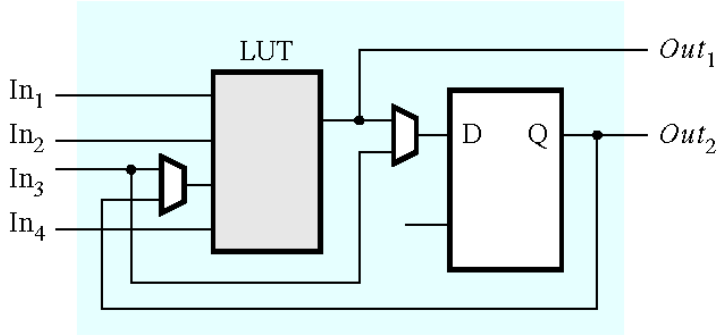
FPGAs

Fundamentals

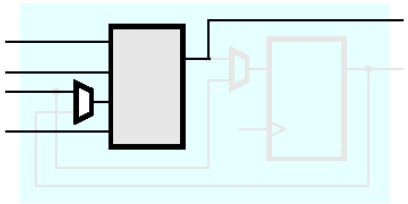
Lookup Tables (LUTs)

4-LUTs vs 6-LUTs

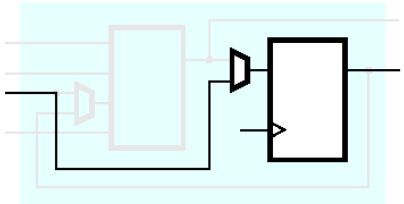
Logic Blocks (Elements)



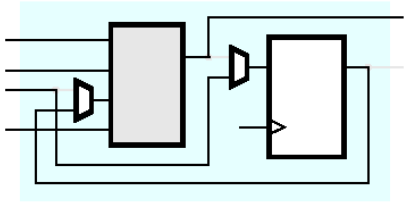
(a) An FPGA logic element.



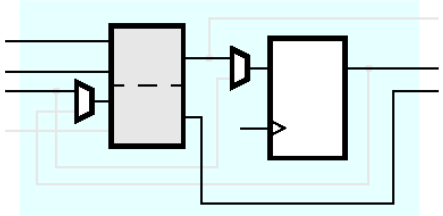
(b) Combinational mode



(c) Synchronous mode



(d) Synchronous feedback mode



(e) Arithmetic (synchronous) mode

Figure 12.5. Different modes of an FPGA logic block.

Routing

- Island style
- Connection blocks, switch blocks, routing segments

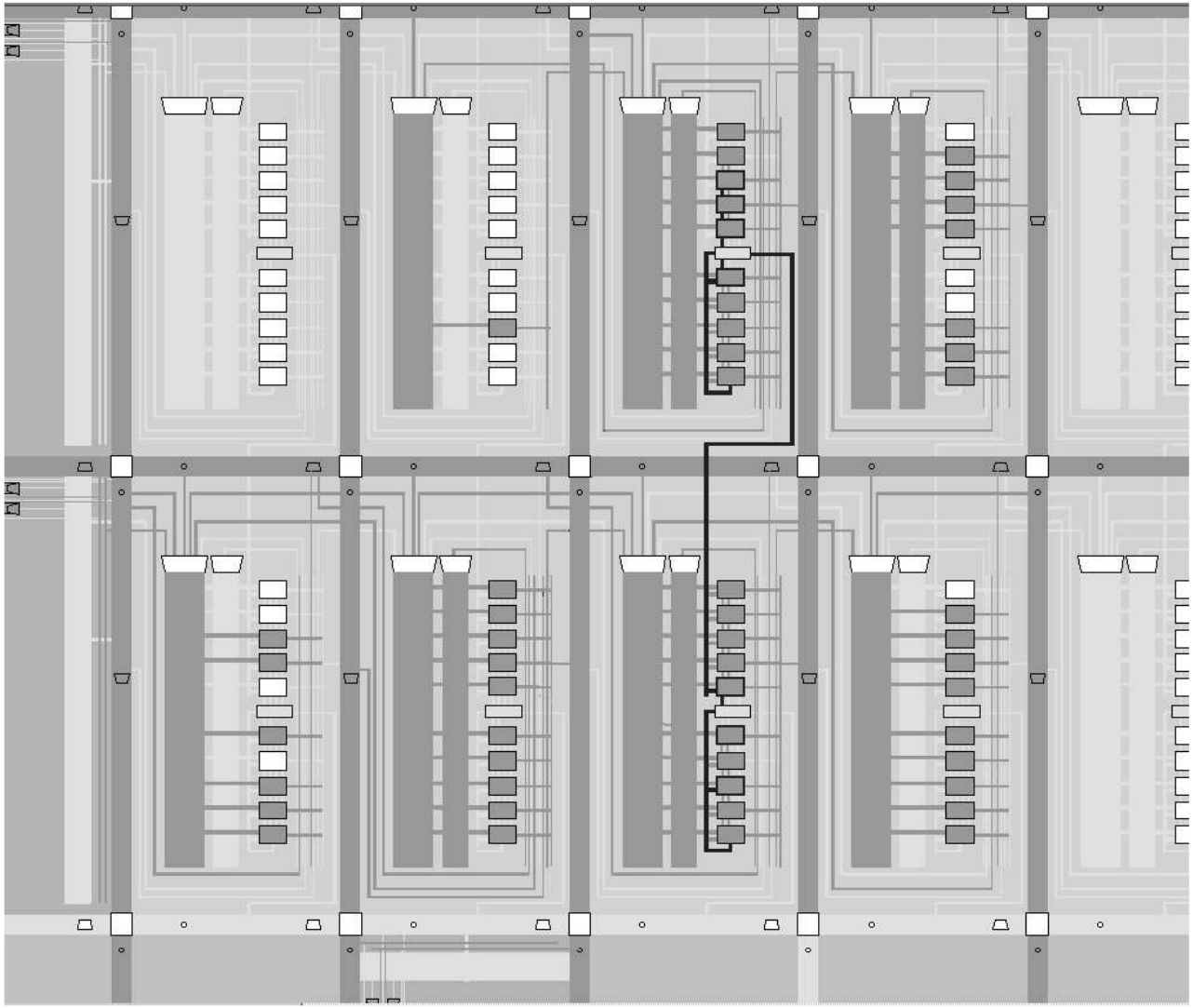


Figure 12.9. Routing for the placement in Figure 12.8.

FPGAs

Tools

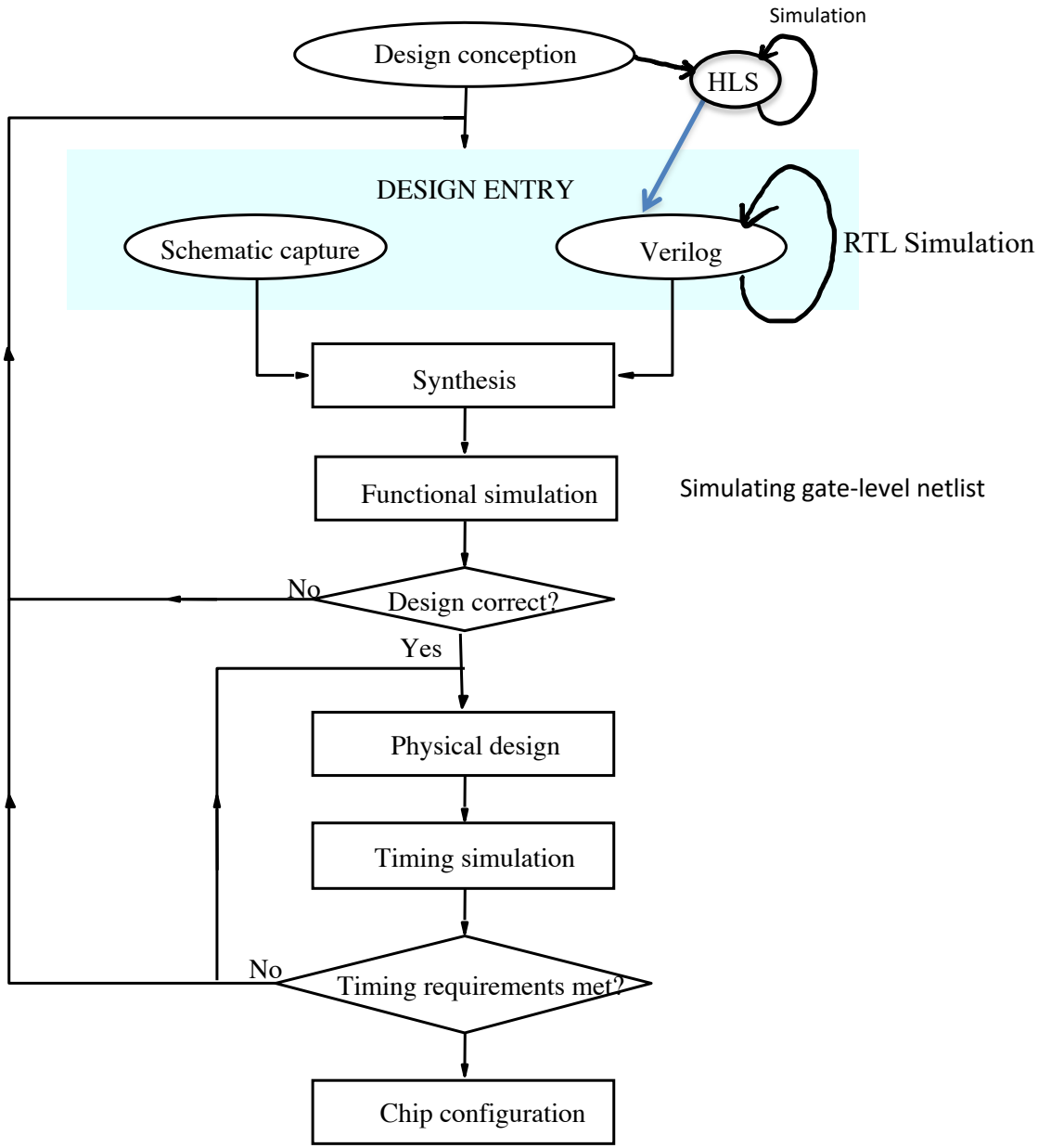


Figure 12.1. A typical CAD system.

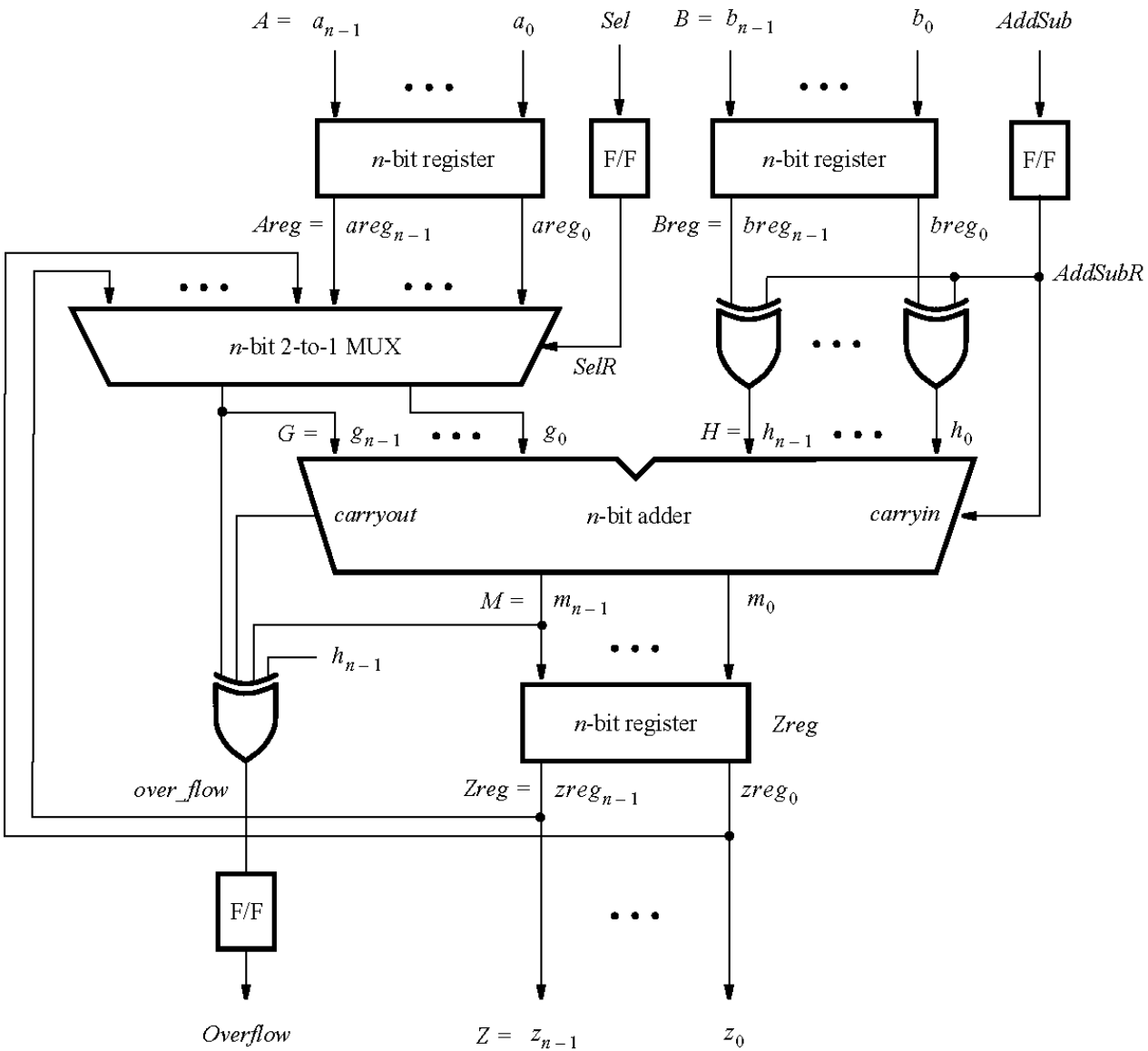


Fig. 12. 4 Circuit specified

Brown and Vranesic, Fundamentals of Digital Logic

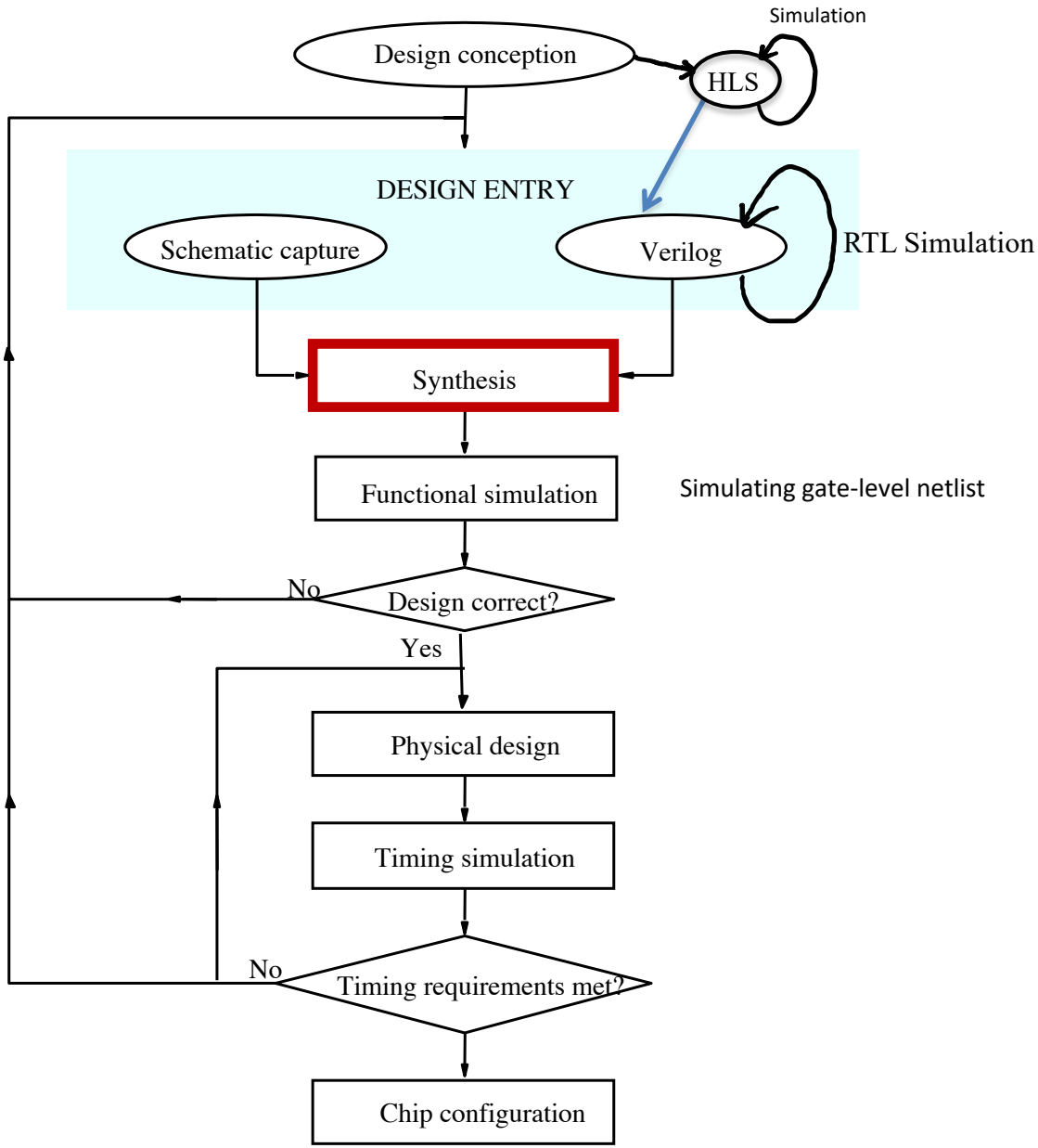


Figure 12.1. A typical CAD system.

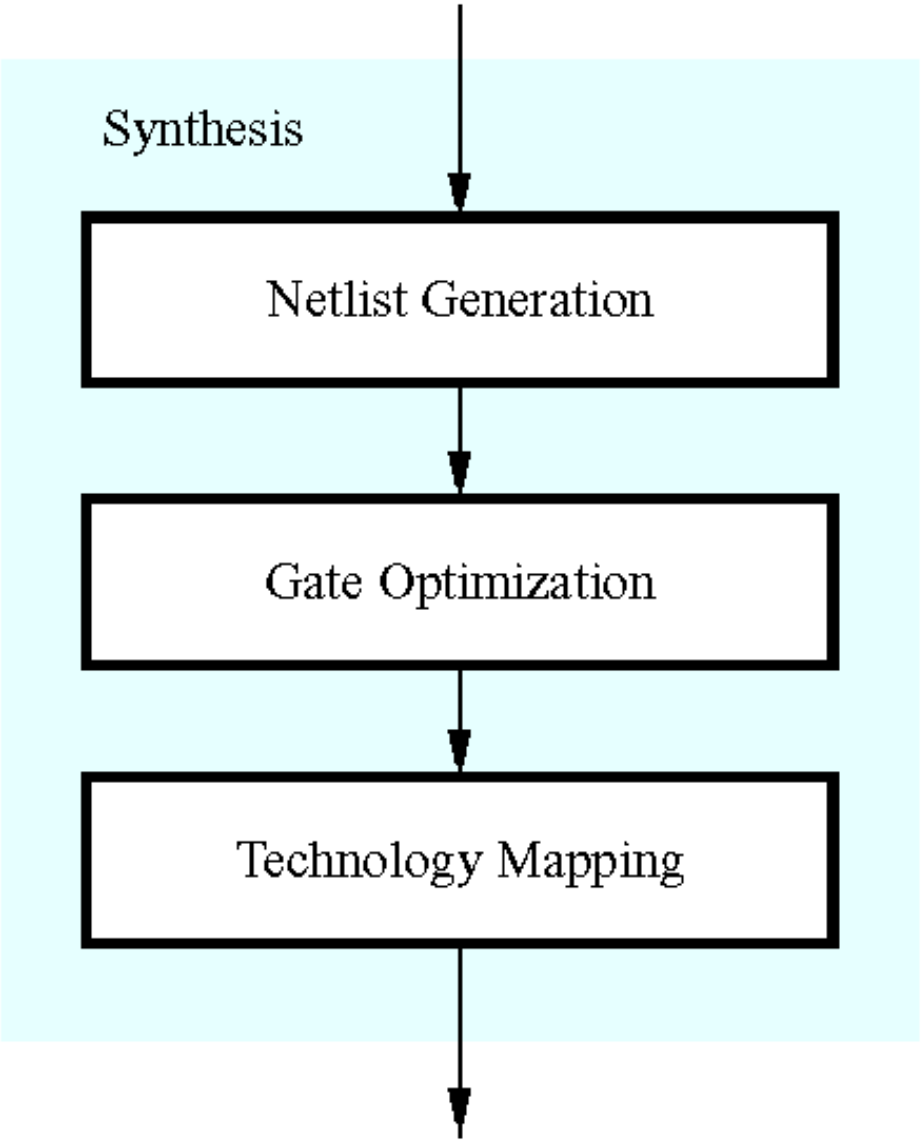


Figure 12.2. The stages included in a synthesis tool.

Netlist

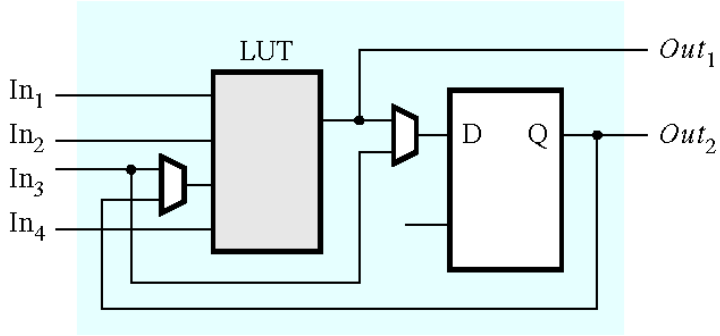
- Circuit description
  - components and connectivity

Gate Optimization

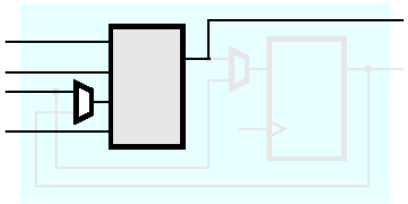
- Working at abstraction level of logic functionality
- Optimize the netlist

Technology Mapping

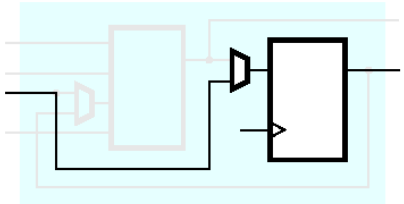
- Map the circuit description to the available resources
- ASIC library
  - TSMC, Samsung, Intel
  - Process – 22nm, 5nm, high-power, low-power
- FPGA
  - Intel, Xilinx, Lattice, which chip family, …



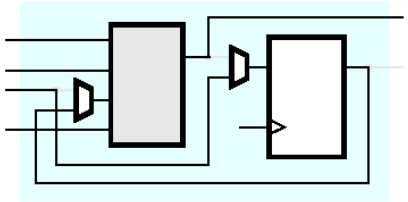
(a) An FPGA logic element.



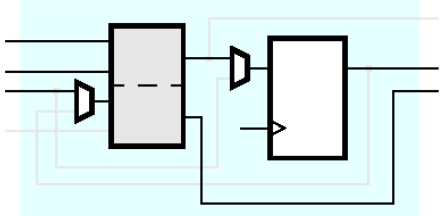
(b) Combinational mode



(c) Synchronous mode



(d) Synchronous feedback mode



(e) Arithmetic (synchronous) mode

Figure 12.5. Different modes of an FPGA logic block.

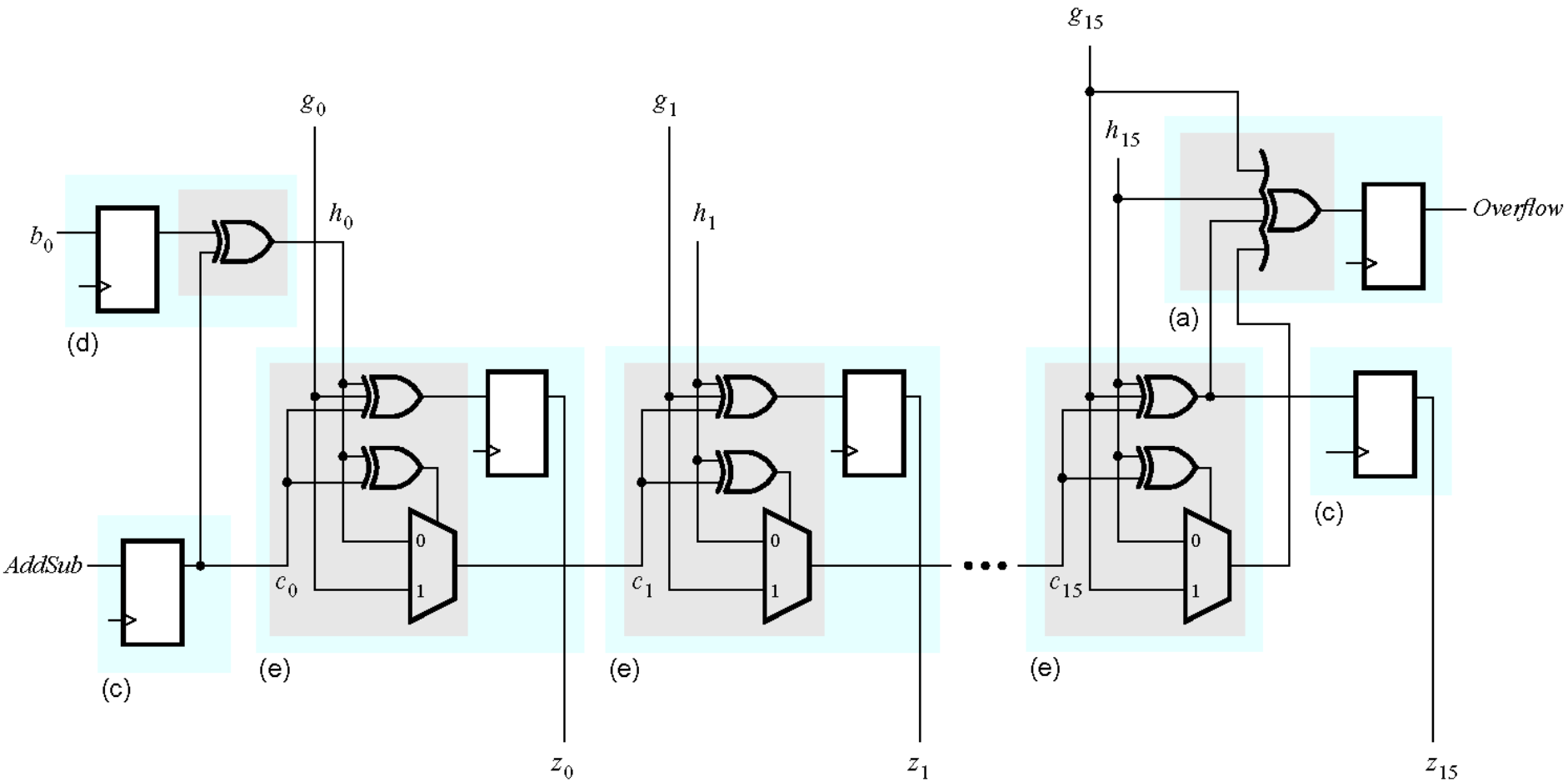
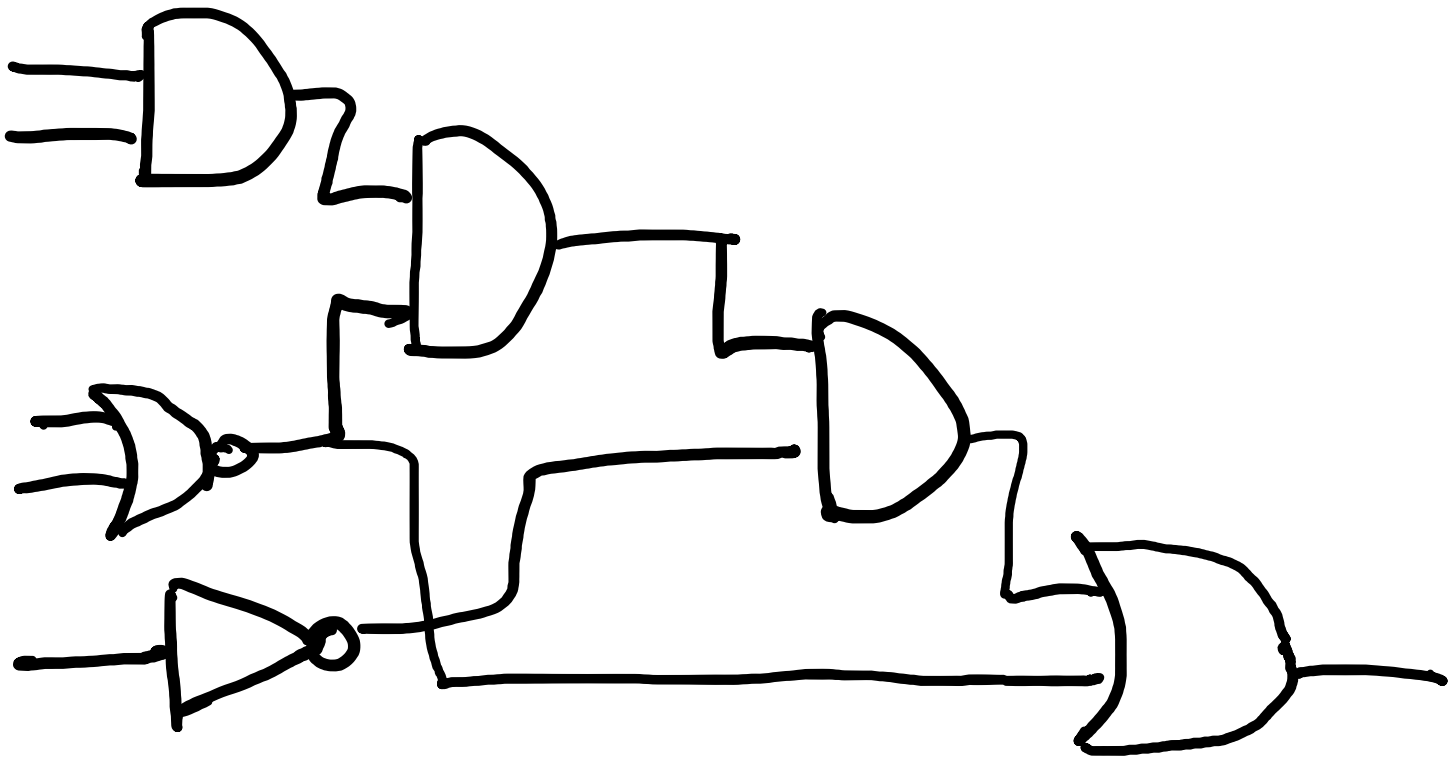


Figure 12.6. A part of the circuit in Figure 12.4 after technology mapping.

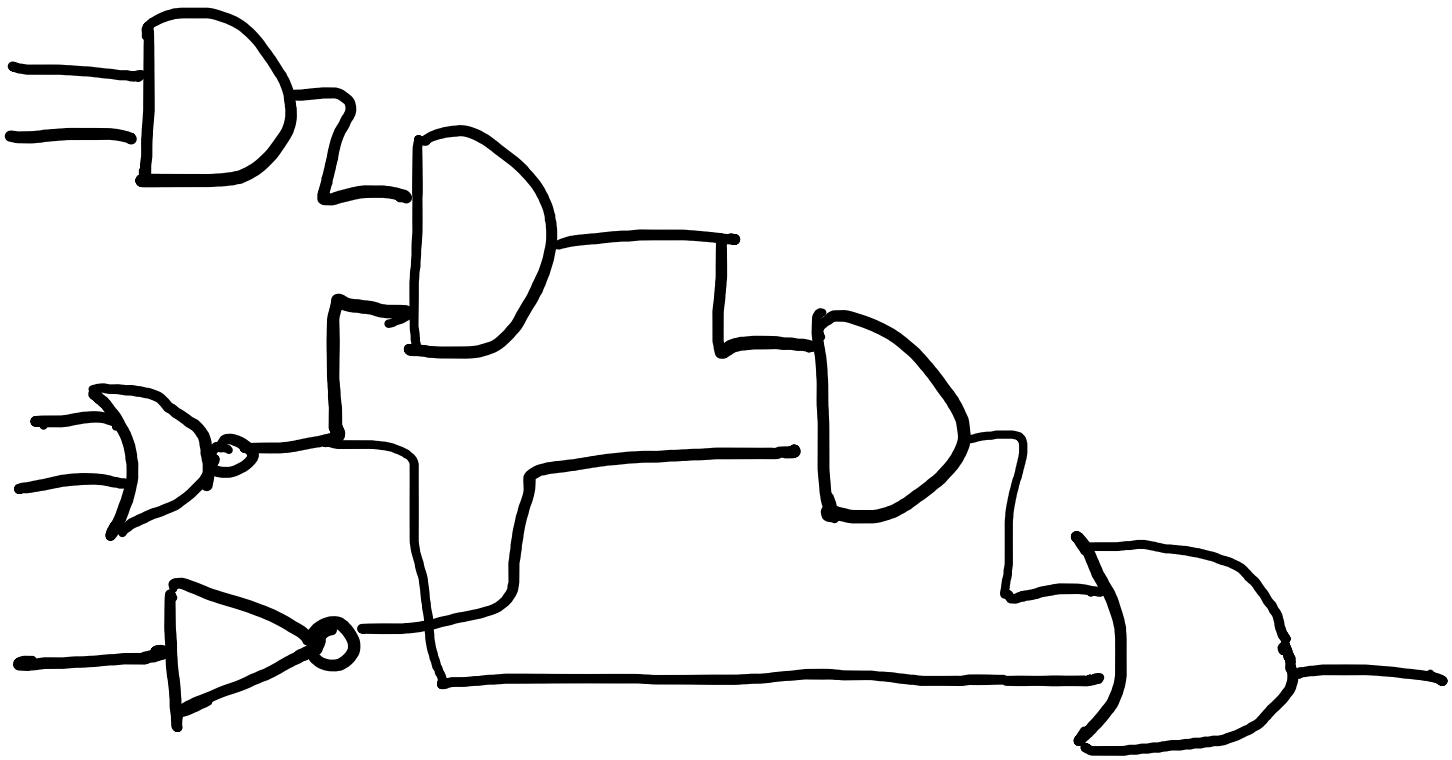
ASIC vs LUT Mapping

- Key difference between mapping to ASIC library of gates and LUTs

4-LUT Mapping



6-LUT Mapping



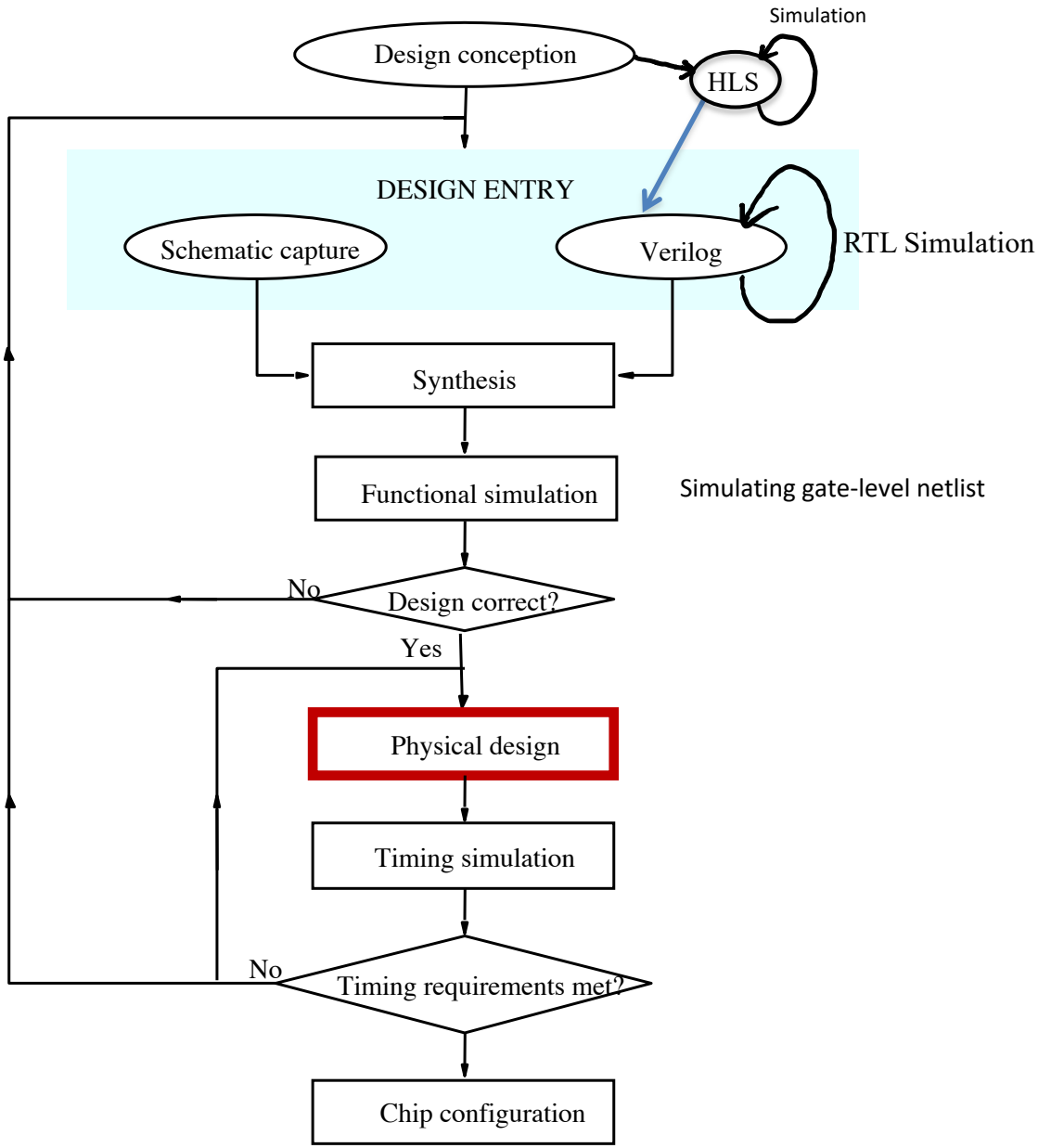


Figure 12.1. A typical CAD system.

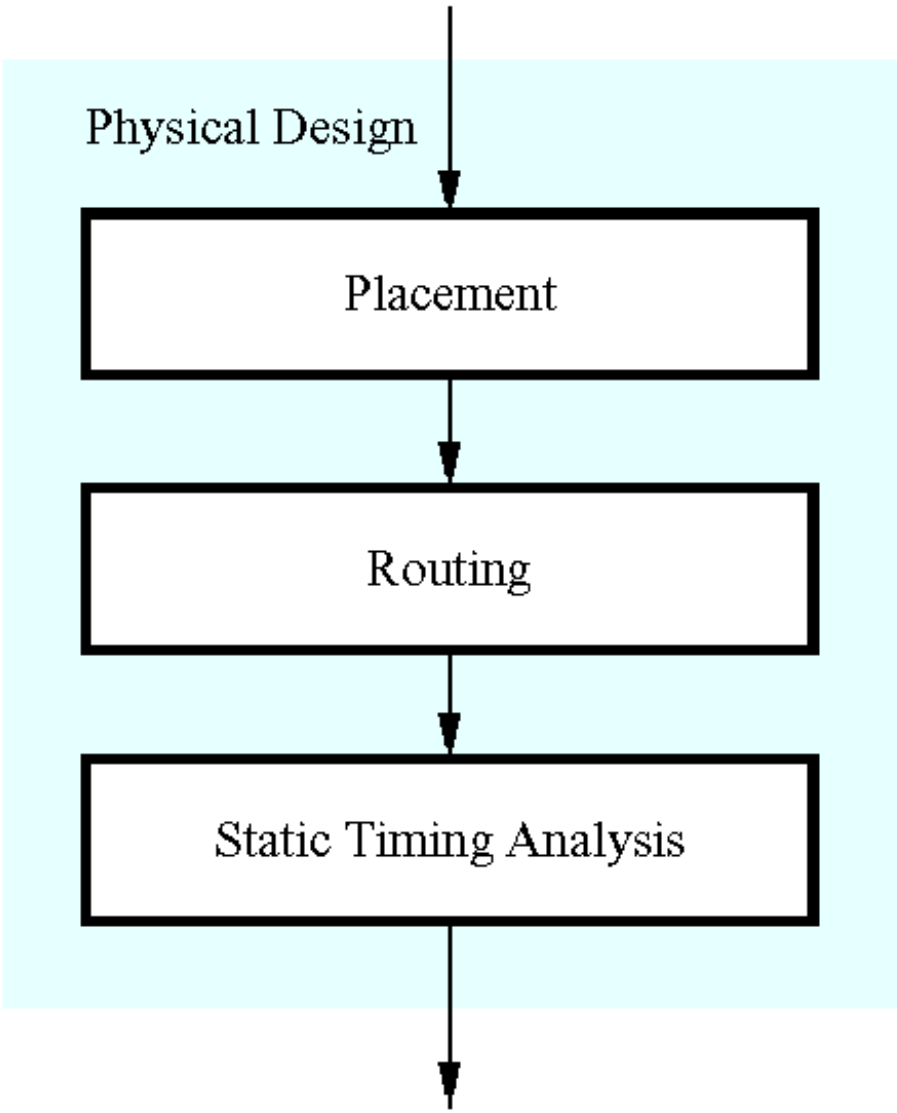
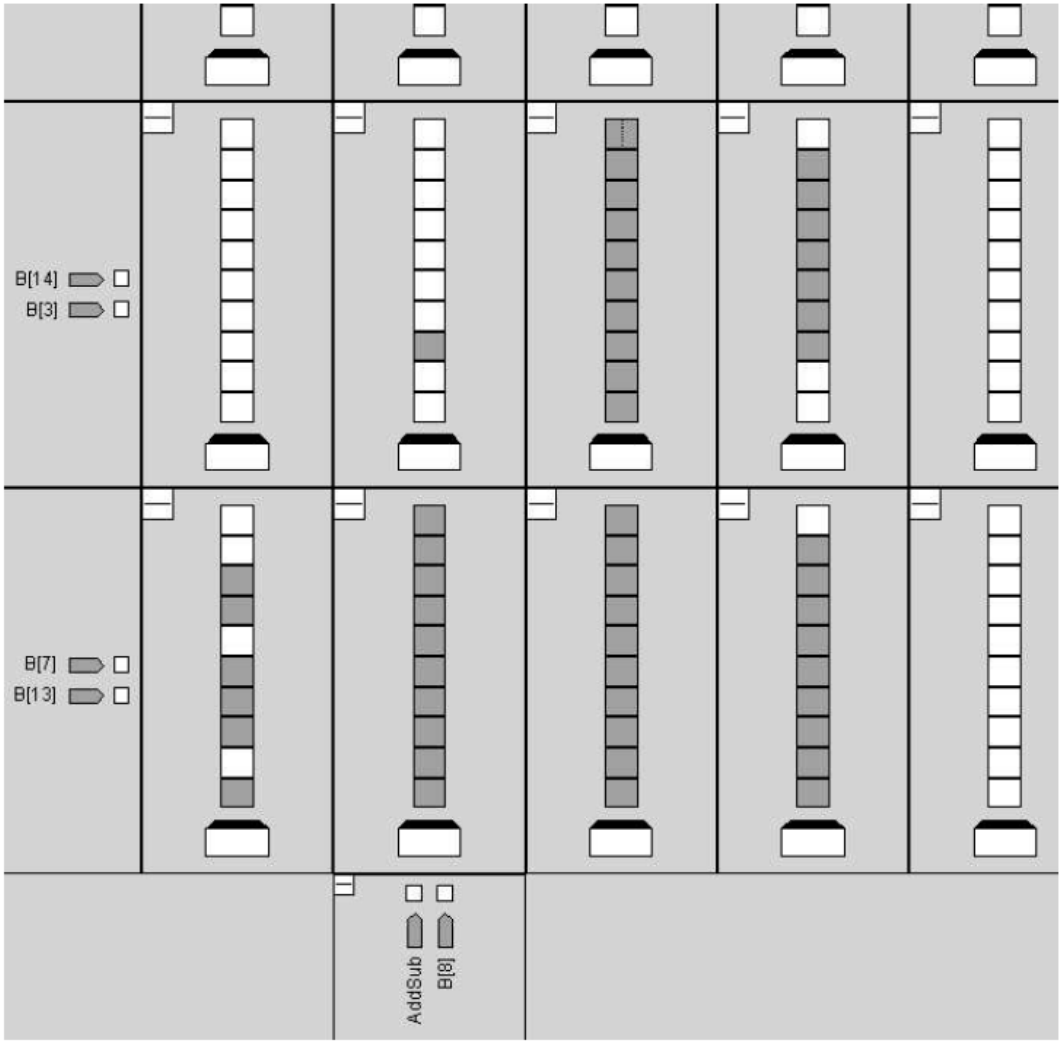


Figure 12.7. Phases in physical design.



LABs have 10 LE/ALM

Figure 12.8. Placement of the circuit in Figure 12.6.

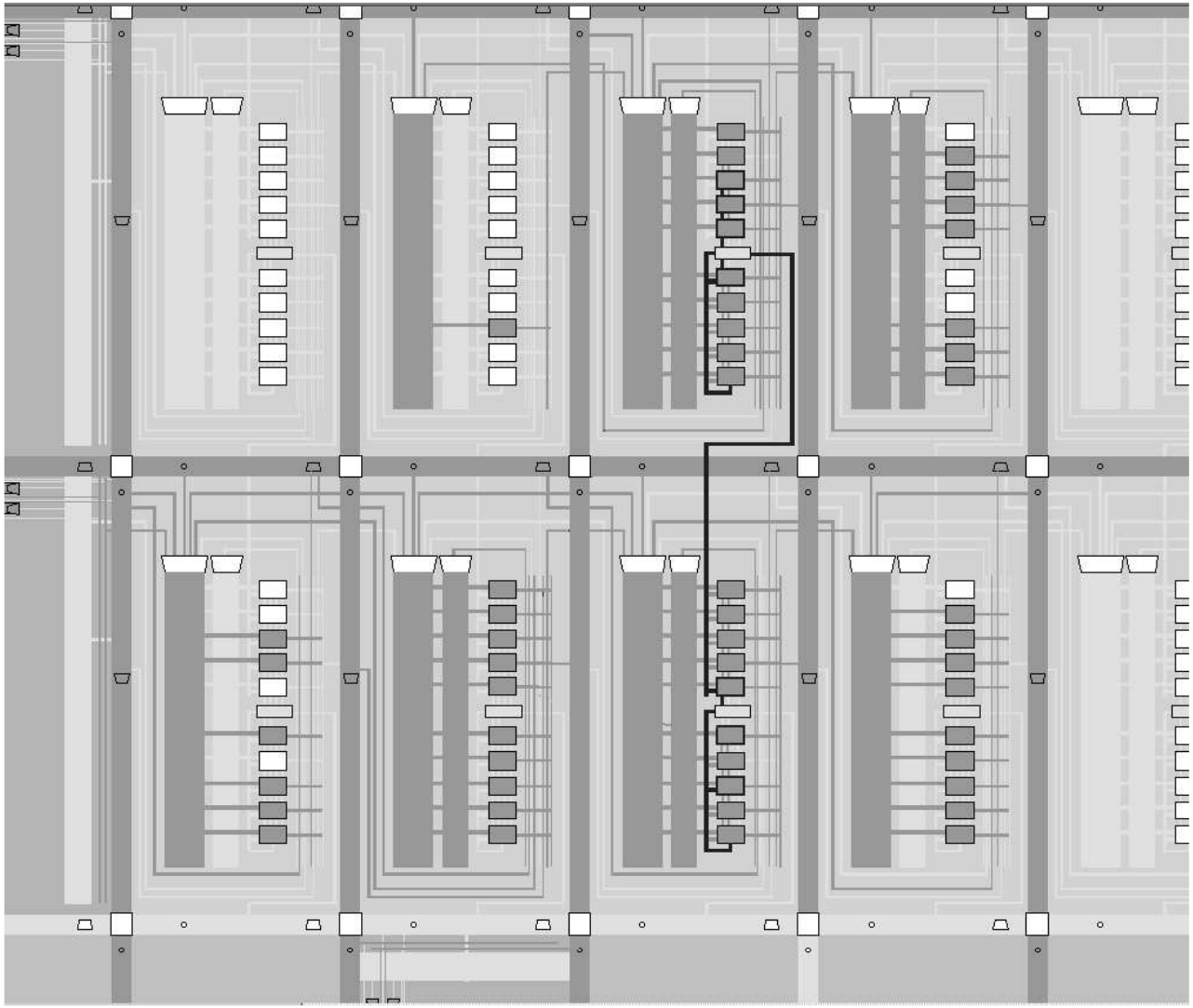


Figure 12.9. Routing for the placement in Figure 12.8.

Parameter	Actual	Required	Slack	From	To
f_{max}	261.1 MHz	200 MHz	1.17 ns	$AddSub$	$Overflow$
t_{su}	2.356 ns	10.0 ns	7.644 ns	b_0	$breg_0$
t_{co}	6.772 ns	10.0 ns	3.228 ns	$zreg_0$	z_0
t_h	0.240 ns	10.0 ns	9.76 ns	b_1	$breg_1$

Table 12.1. A summary of static timing analysis results.

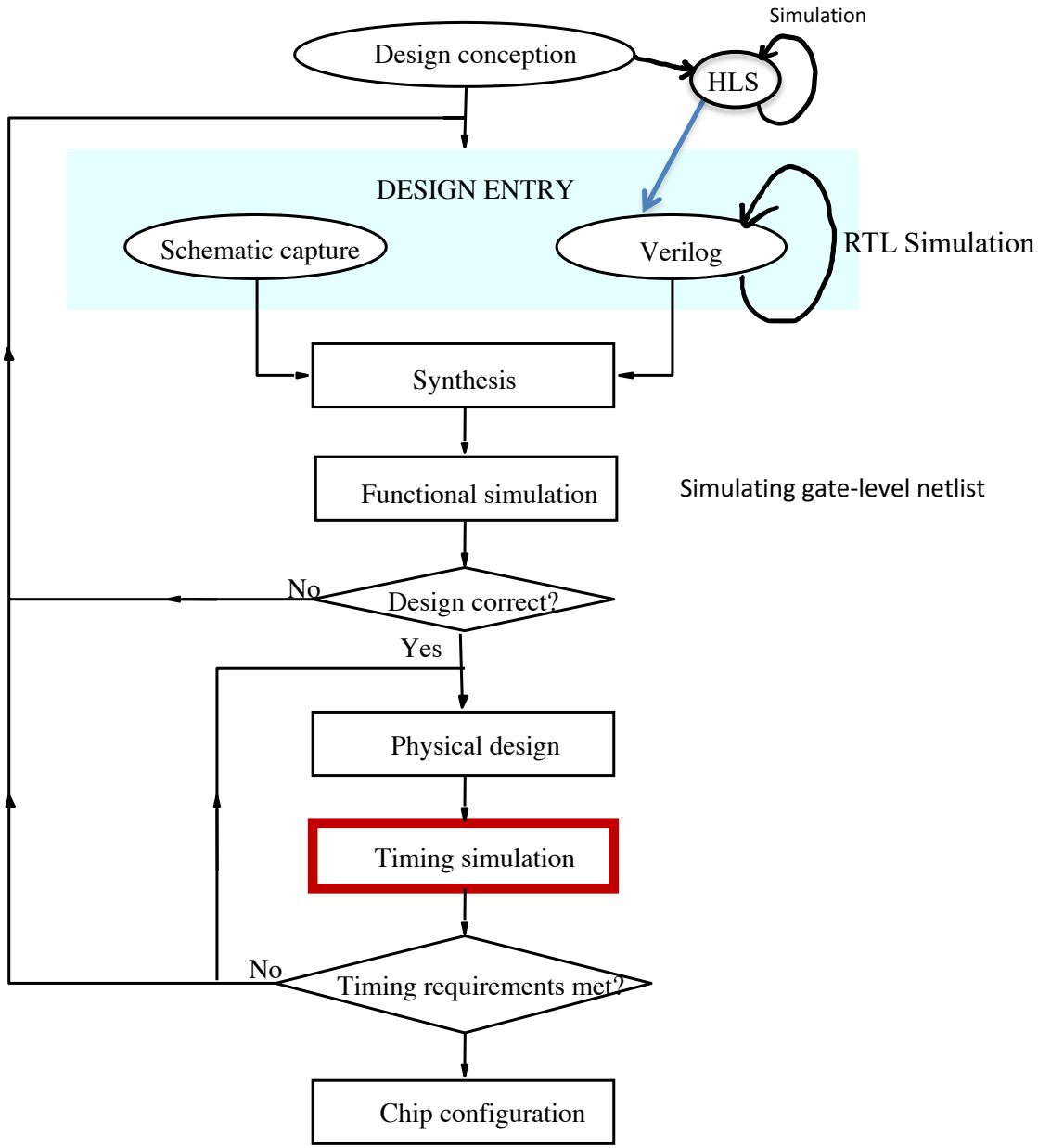


Figure 12.1. A typical CAD system.

FPGAs

Architecture

XILINX VIRTEX 7

Many Features

- Most of the time you “don’t care”
  - The tool will do the work for you
- To achieve high-performance, high-utilization you need to pay attention
- Know what the chip can do

Virtex-7 FPGA Feature Summary

Table 6: **Virtex-7 FPGA Feature Summary**

Device[1]	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices[3]	Block RAM Blocks[4]			CMTs[5]	PCIe[6]	GTX	GTH	GTZ	XADC Blocks	Total I/O Banks[7]	Max User I/O[8]	SLRs[9]
		Slices[2]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)									
XC7V585T	582,720	91,050	6,938	1,260	1,590	795	28,620	18	3	36	0	0	1	17	850	N/A
XC7V2000T	1,954,560	305,400	21,550	2,160	2,584	1,292	46,512	24	4	36	0	0	1	24	1,200	4
XC7VX330T	326,400	51,000	4,388	1,120	1,500	750	27,000	14	2	0	28	0	1	14	700	N/A
XC7VX415T	412,160	64,400	6,525	2,160	1,760	880	31,680	12	2	0	48	0	1	12	600	N/A
XC7VX485T	485,760	75,900	8,175	2,800	2,060	1,030	37,080	14	4	56	0	0	1	14	700	N/A
XC7VX550T	554,240	86,600	8,725	2,880	2,360	1,180	42,480	20	2	0	80	0	1	16	600	N/A
XC7VX690T	693,120	108,300	10,888	3,600	2,940	1,470	52,920	20	3	0	80	0	1	20	1,000	N/A
XC7VX980T	979,200	153,000	13,838	3,600	3,000	1,500	54,000	18	3	0	72	0	1	18	900	N/A
XC7VX1140T	1,139,200	178,000	17,700	3,360	3,760	1,880	67,680	24	4	0	96	0	1	22	1,100	4
XC7VH580T	580,480	90,700	8,850	1,680	1,880	940	33,840	12	2	0	48	8	1	12	600	2
XC7VH870T	876,160	136,900	13,275	2,520	2,820	1,410	50,760	18	3	0	72	16	1	13	650	3

Notes:

1. EasyPath™-7 FPGAs are also available to provide a fast, simple, and risk-free solution for cost reducing Virtex-7 T and Virtex-7 XT FPGA designs
2. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
3. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
4. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
5. Each CMT contains one MMCM and one PLL.
6. Virtex-7 T FPGA Interface Blocks for PCI Express support up to x8 Gen 2. Virtex-7 XT and Virtex-7 HT Interface Blocks for PCI Express support up to x8 Gen 3, with the exception of the XC7VX485T device, which supports x8 Gen 2.
7. Does not include configuration Bank 0.
8. This number does not include GTX, GTH, or GTZ transceivers.
9. Super logic regions (SLRs) are the constituent parts of FPGAs that use SSI technology. Virtex-7 HT devices use SSI technology to connect SLRs with 28.05 Gb/s transceivers.

Virtex® UltraScale+™ FPGAs

Device Name	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU31P	VU33P	VU35P	VU37P
System Logic Cells (K)	862	1,314	1,724	2,586	2,835	3,780	962	962	1,907	2,852
CLB Flip-Flops (K)	788	1,201	1,576	2,364	2,592	3,456	879	879	1,743	2,607
CLB LUTs (K)	394	601	788	1,182	1,296	1,728	440	440	872	1,304
Max. Distributed RAM (Mb)	12.0	18.3	24.1	36.1	36.2	48.3	12.5	12.5	24.6	36.7
Total Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5	23.6	23.6	47.3	70.9
UltraRAM (Mb)	90.0	132.2	180.0	270.0	270.0	360.0	90.0	90.0	180.0	270.0
HBM DRAM (GB)	–	–	–	–	–	–	4	8	8	8
HBM AXI Interfaces	–	–	–	–	–	–	32	32	32	32
Clock Mgmt Tiles (CMTs)	10	20	20	30	12	16	4	4	8	12
DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288	2,880	2,880	5,952	9,024
Peak INT8 DSP (TOP/s)	7.1	10.8	14.2	21.3	28.7	38.3	8.9	8.9	18.6	28.1
PCIe® Gen3 x16 / Gen4 x8	2	4	4	6	3	4	4	4	5	6
CCIX Ports[1]	–	–	–	–	–	–	4	4	4	4
150G Interlaken	3	4	6	9	6	8	0	0	2	4
100G Ethernet w/ RS-FEC	3	4	6	9	9	12	2	2	5	8
Max. Single-Ended HP I/Os	520	832	832	832	624	832	208	208	416	624
GTY 32.75Gb/s Transceivers	40	80	80	120	96	128	32	32	64	96
Extended[2]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
Industrial	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	–	–	–	–

Footprint compatible with 20nm UltraScale Devices with same footprint identifier

Footprint[3,4]	Dimensions (mm)	HP I/O, GTY 32.75Gb/s									
C1517	40x40	520, 40									
F1924[5]	45x45					624, 64					
A2104	47.5x47.5		832, 52	832, 52	832, 52						
	52.5x52.5[6]						832, 52				
B2104	47.5x47.5		702, 76	702, 76	702, 76	572, 76					
	52.5x52.5[6]						702, 76				
C2104	47.5x47.5		416, 80	416, 80	416, 104	416, 96					
	52.5x52.5[6]						416, 104				
D2104	47.5x47.5				676, 76	572, 76					
	52.5x52.5[6]						676, 76				
A2577	52.5x52.5				448, 120	448, 96	448, 128				
H1924	45x45							208, 32			
H2104	47.5x47.5								208, 32	416, 64	
H2892	55x55									416, 64	624, 96

Be wary of units of capacity

Up to Virtex-7

Device capacity is often measured in terms of logic cells, which are the logical equivalent of a classic four-input LUT and a flip-flop. The 7 series FPGA CLB's six-input LUT, abundant flip-flops and latches, carry logic, and the ability to create distributed RAM or shift registers in the SLICEM, increase the effective capacity. The ratio between the number of logic cells and 6-input LUTs is 1.6:1.

Starting with Ultrascale

- System Logic Cells?

Slice Description

Every slice contains:

- four logic-function generators (or look-up tables)
- eight storage elements
- wide-function multiplexers
- carry logic

These elements are used by all slices to provide logic, arithmetic, and ROM functions. In addition, some slices support two additional functions: storing data using distributed RAM and shifting data with 32-bit registers. Slices that support these additional functions are called SLICEM; others are called SLICEL. SLICEM (shown in Figure 2-3) represents a superset of elements and connections found in all slices. SLICEL is shown in Figure 2-4. Each CLB can contain two SLICEL or a SLICEL and a SLICEM.

Slices vs LUTs

- LUTs are actual resources used
- Slice utilization not accurate measure of resource usage
  - Slice packing effects

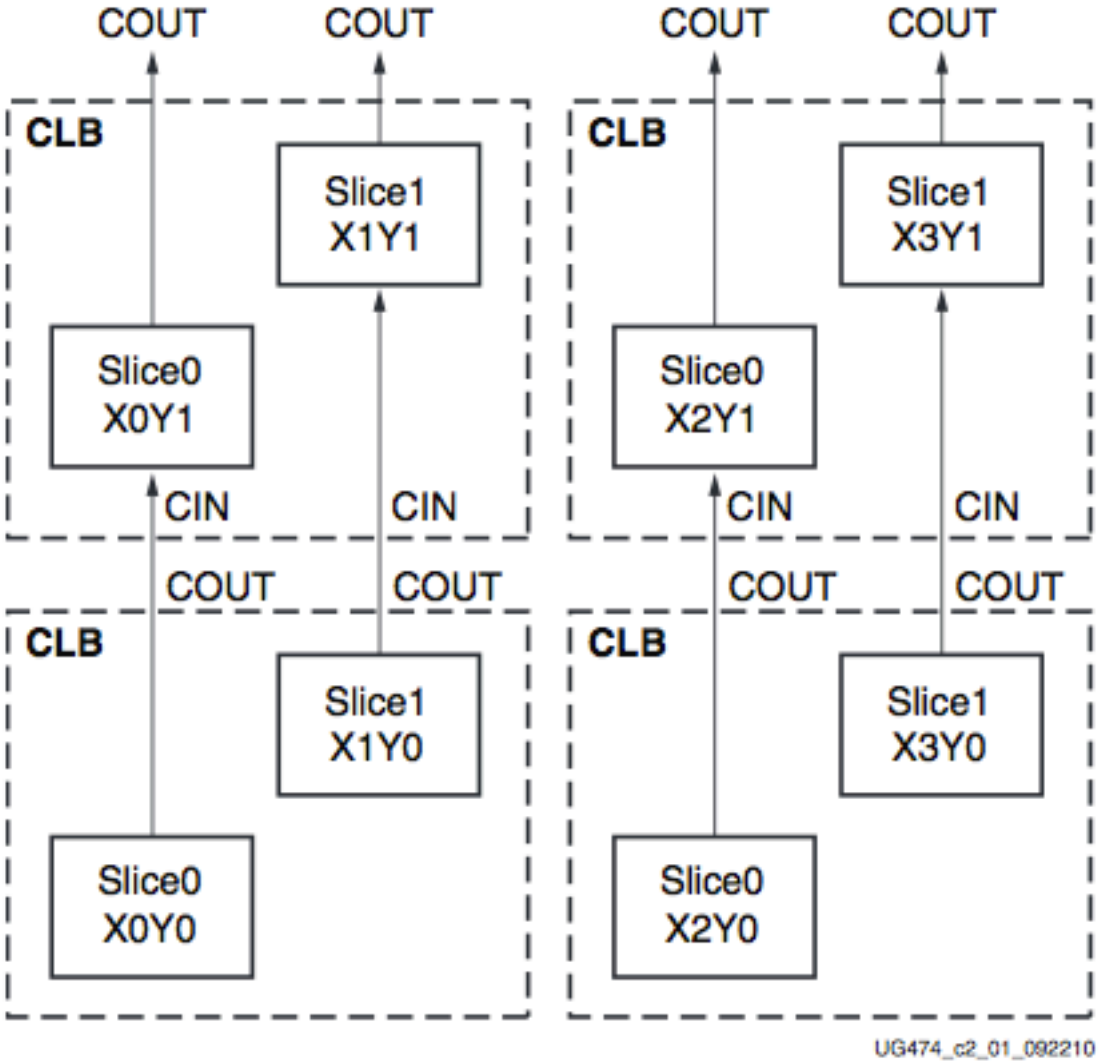


Figure 2-2: **Row and Column Relationship between CLBs and Slices**

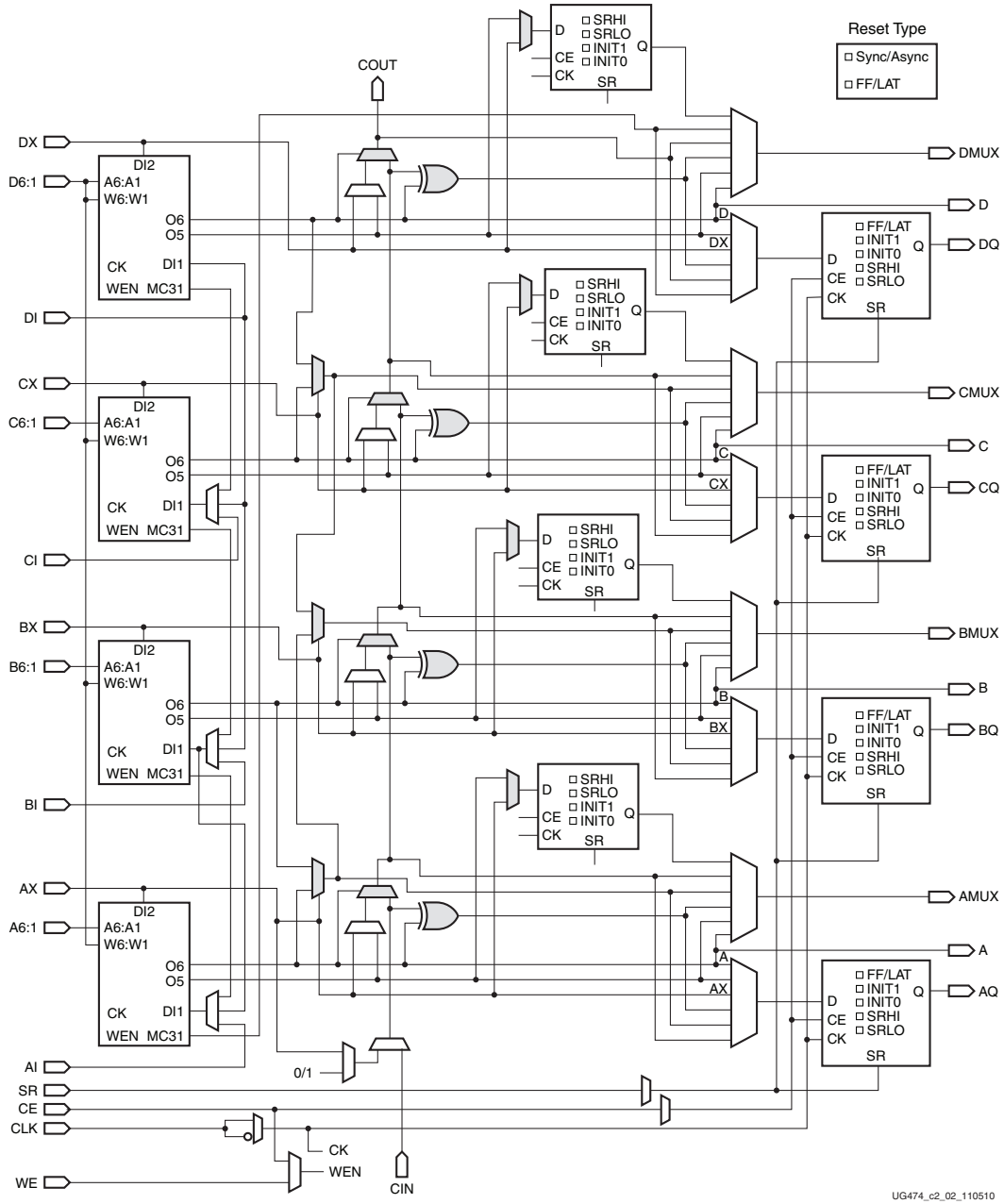
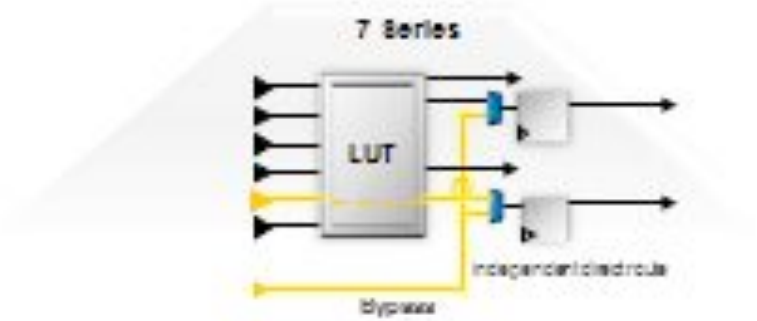
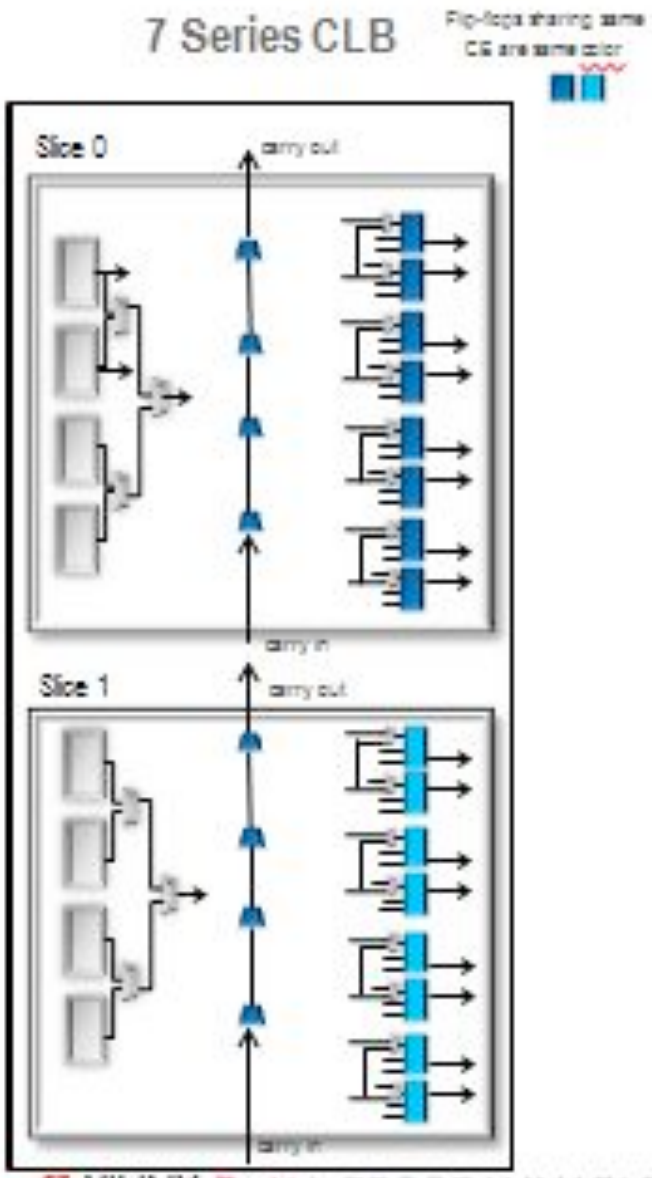


Figure 2-3: **Diagram of SLICEM**

Improving Upon the 7 Series Architecture





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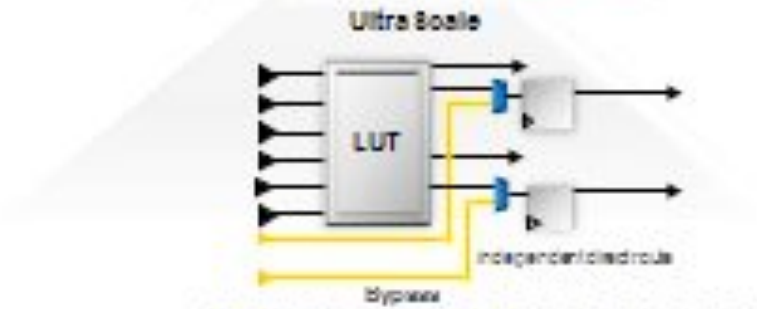
CLB Innovations Enable Tighter Packing in the UltraScale Architecture

Removed slice boundary & added MUX
- Wider functions per block
- 2x distributed RAM density

Wider carry chain
- Wider functions per block

Dedicated inputs for each flip-flop
- Higher performance
- Avoids LUT route-thru
- Reduces LUT utilization



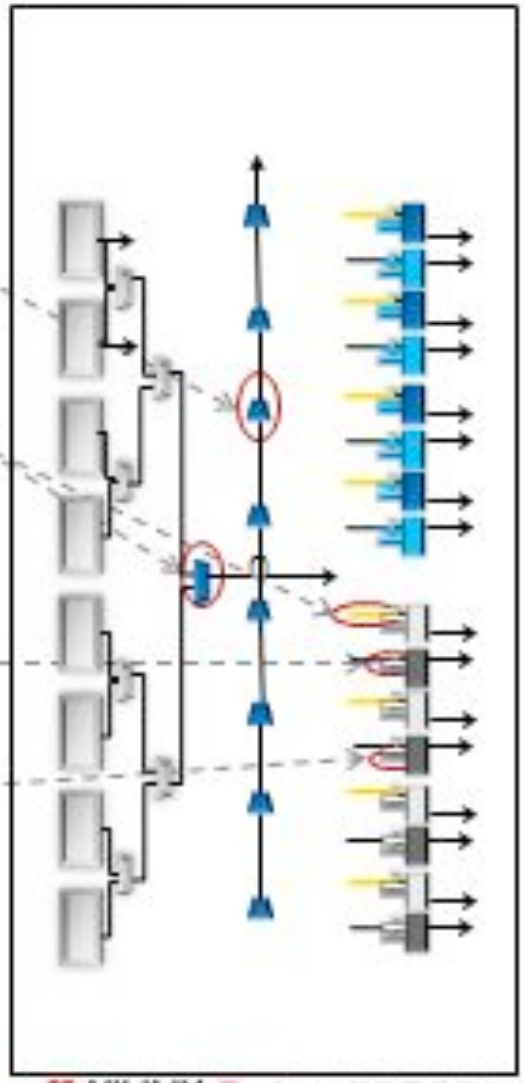
CE ignore, RST inversion
- Higher performance
- Eliminates synchronous reset bottlenecks

2x the number of CE's
- Improves CLB packing

Flip-flops sharing same CE are same color

UltraScale™ CLB

CLB = Slice



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XILINX ALL PROGRAMMABLE.

Table 2-3: **Distributed RAM Configuration**

RAM[1]	Number of LUTs
32 x 1S	1
32 x 1D	2
32 x 2Q[2]	4
32 x 6SDP[2]	4
64 x 1S	1
64 x 1D	2
64 x 1Q[3]	4
64 x 3SDP[3]	4
128 x 1S	2
128 x 1D	4
256 x 1S	4

Notes:

1. S = single-port configuration; D = dual-port configuration; Q = quad-port configuration; SDP = simple dual-port configuration.
2. RAM32M is the associated primitive for this configuration.
3. RAM64M is the associated primitive for this configuration.

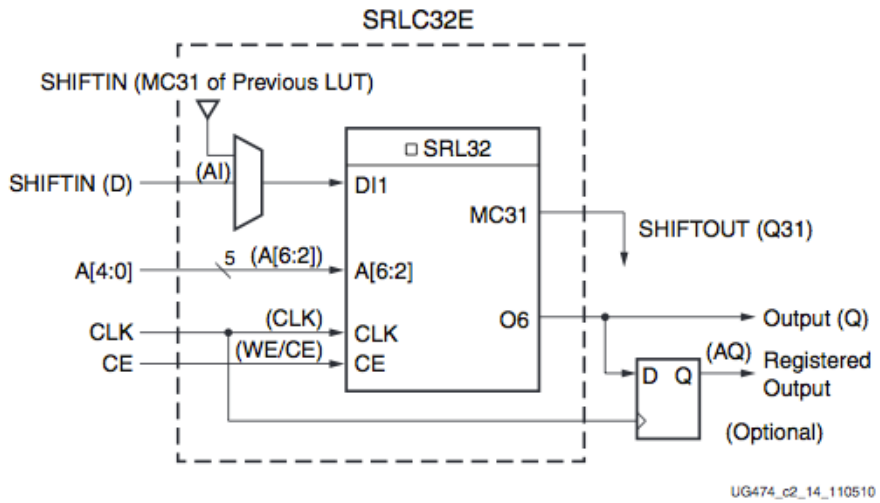


Figure 2-15: **32-bit Shift Register Configuration**

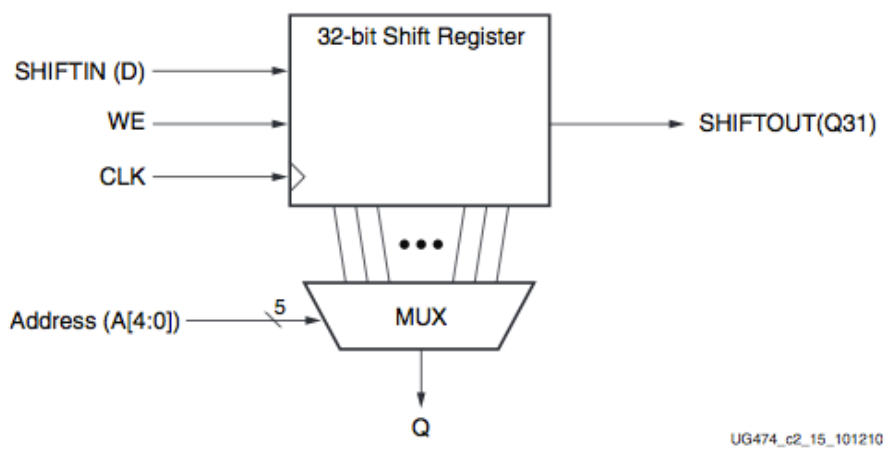


Figure 2-16: **Representation of a Shift Register**

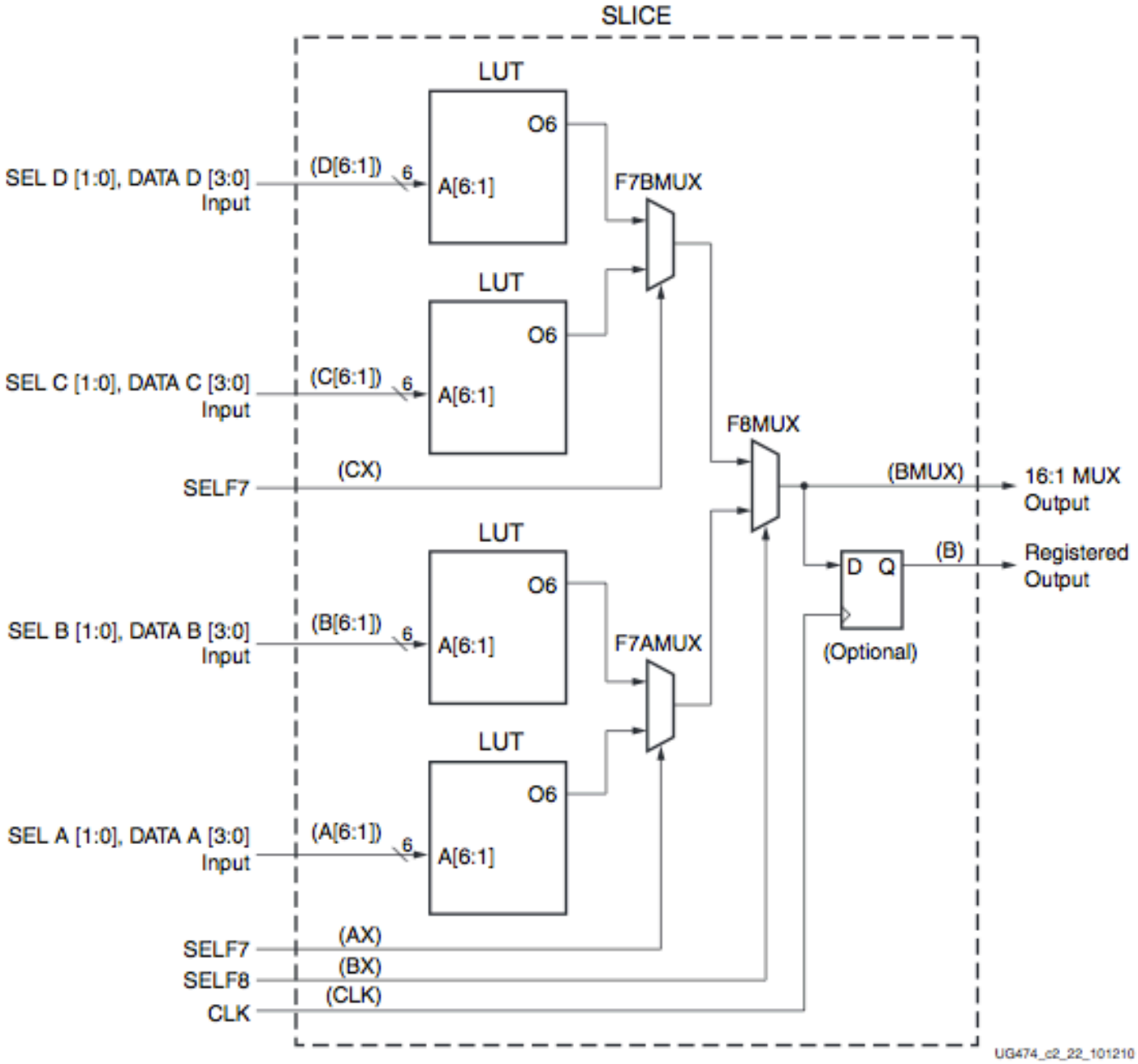


Figure 2-23: **16:1 Multiplexer in a Slice**

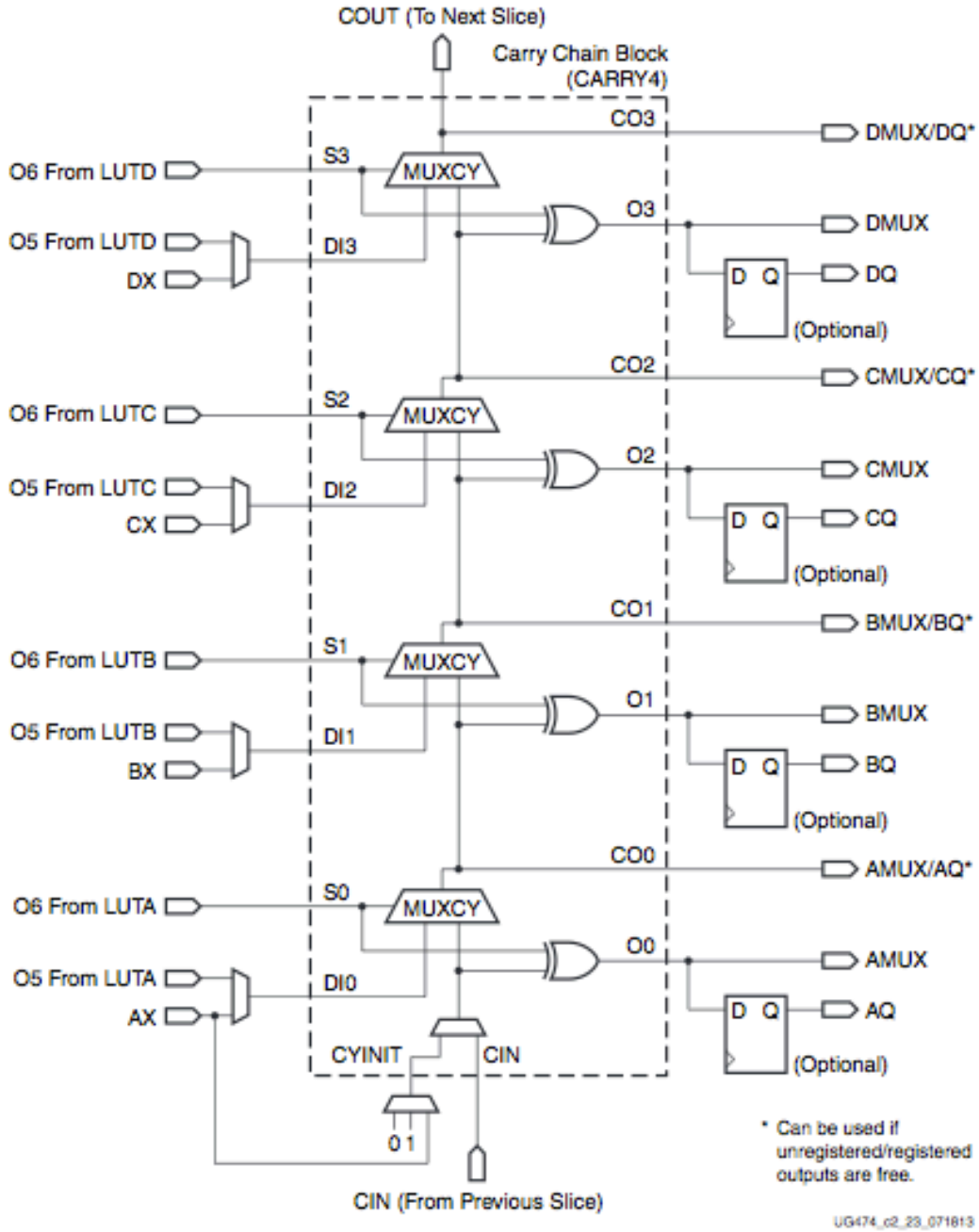


Figure 2-24: **Fast Carry Logic Path and Associated Elements**

Block RAMs

The block RAM in Xilinx® 7 series FPGAs stores up to 36 Kbits of data and can be configured as either two independent 18 Kb RAMs, or one 36 Kb RAM. Each 36 Kb block RAM can be configured as a 64K x 1 (when cascaded with an adjacent 36 Kb block RAM), 32K x 1, 16K x 2, 8K x 4, 4K x 9, 2K x 18, 1K x 36, or 512 x 72 in simple dual-port mode. Each 18 Kb block RAM can be configured as a 16K x 1, 8K x2 , 4K x 4, 2K x 9, 1K x 18 or 512 x 36 in simple dual-port mode.

Some of the key features of the block RAM include:

- Dual-port 36 Kb block RAM with port widths of up to 72
- Programmable FIFO logic
- Built-in optional error correction circuitry

Every 7 series FPGA has between 50 and 1,880 dual-port block RAMs, each storing 36 Kb. Each block RAM has two completely independent ports that share nothing but the stored data.

UltraScale+ UltraRAM

- 288 Kb
- 4096 x 72 bits fixed configuration
- Dual port
- 360 Mb in largest devices

UltraScale+ HBM

- High Bandwidth memory
- Up to 8GB
- Separate die in same package

HBM Packaging

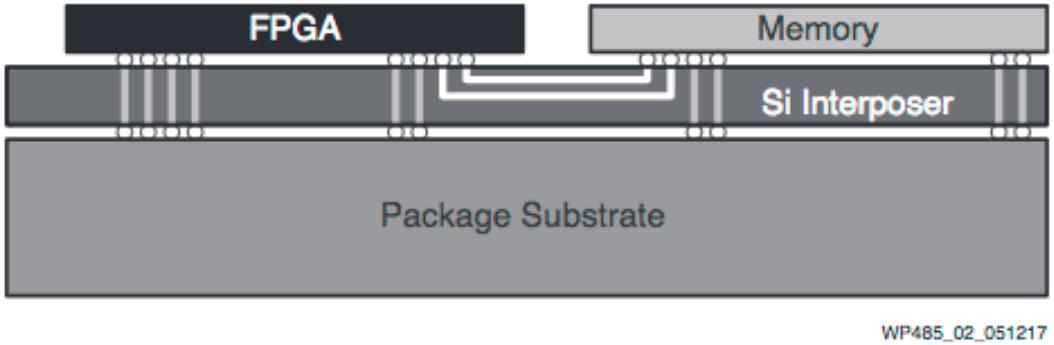


Figure 2: **TSMC CoWoS Assembly Allows for Thousands of Very Small Wires Connecting Adjacent Die**

CoWoS: chip-on-wafer-on-substrate
Same technology for multi-die devices

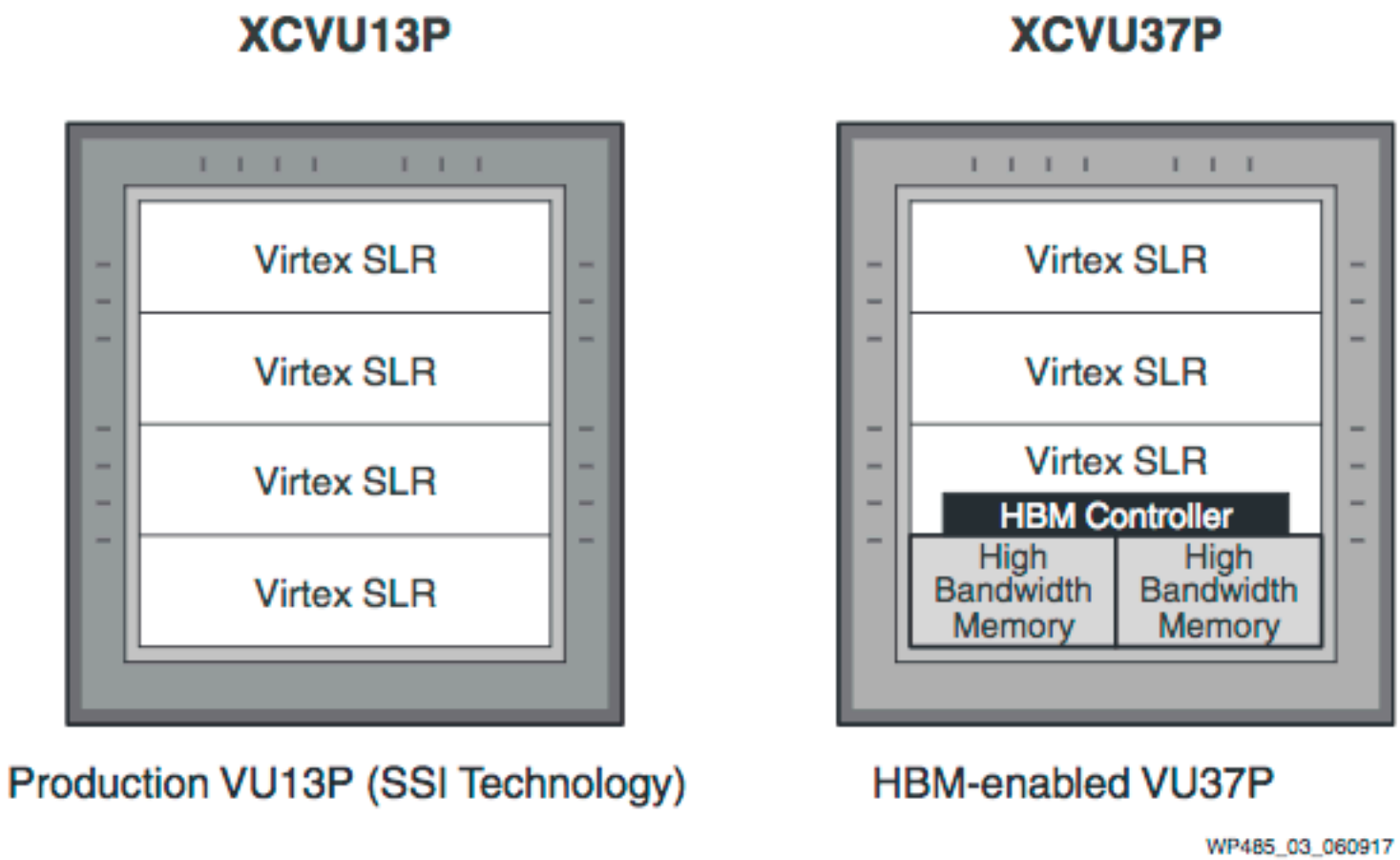


Figure 3: **SSI Technology and HBM-enabled XCVU37P**

SLR: Super logic region – separate die
SSI: Stacked silicon interconnect

Virtex® UltraScale+™ FPGAs

Device Name	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU31P	VU33P	VU35P	VU37P
System Logic Cells (K)	862	1,314	1,724	2,586	2,835	3,780	962	962	1,907	2,852
CLB Flip-Flops (K)	788	1,201	1,576	2,364	2,592	3,456	879	879	1,743	2,607
CLB LUTs (K)	394	601	788	1,182	1,296	1,728	440	440	872	1,304
Max. Distributed RAM (Mb)	12.0	18.3	24.1	36.1	36.2	48.3	12.5	12.5	24.6	36.7
Total Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5	23.6	23.6	47.3	70.9
UltraRAM (Mb)	90.0	132.2	180.0	270.0	270.0	360.0	90.0	90.0	180.0	270.0
HBM DRAM (GB)	–	–	–	–	–	–	4	8	8	8
HBM AXI Interfaces	–	–	–	–	–	–	32	32	32	32
Clock Mgmt Tiles (CMTs)	10	20	20	30	12	16	4	4	8	12
DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288	2,880	2,880	5,952	9,024
Peak INT8 DSP (TOP/s)	7.1	10.8	14.2	21.3	28.7	38.3	8.9	8.9	18.6	28.1
PCIe® Gen3 x16 / Gen4 x8	2	4	4	6	3	4	4	4	5	6
CCIX Ports[1]	–	–	–	–	–	–	4	4	4	4
150G Interlaken	3	4	6	9	6	8	0	0	2	4
100G Ethernet w/ RS-FEC	3	4	6	9	9	12	2	2	5	8
Max. Single-Ended HP I/Os	520	832	832	832	624	832	208	208	416	624
GTY 32.75Gb/s Transceivers	40	80	80	120	96	128	32	32	64	96
Extended[2]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
Industrial	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	–	–	–	–

Footprint compatible with 20nm UltraScale Devices with same footprint identifier

Footprint[3,4]	Dimensions (mm)	HP I/O, GTY 32.75Gb/s									
C1517	40x40	520, 40									
F1924[5]	45x45					624, 64					
A2104	47.5x47.5		832, 52	832, 52	832, 52						
	52.5x52.5[6]						832, 52				
B2104	47.5x47.5		702, 76	702, 76	702, 76	572, 76					
	52.5x52.5[6]						702, 76				
C2104	47.5x47.5		416, 80	416, 80	416, 104	416, 96					
	52.5x52.5[6]						416, 104				
D2104	47.5x47.5				676, 76	572, 76					
	52.5x52.5[6]						676, 76				
A2577	52.5x52.5				448, 120	448, 96	448, 128				
H1924	45x45							208, 32			
H2104	47.5x47.5								208, 32	416, 64	
H2892	55x55									416, 64	624, 96

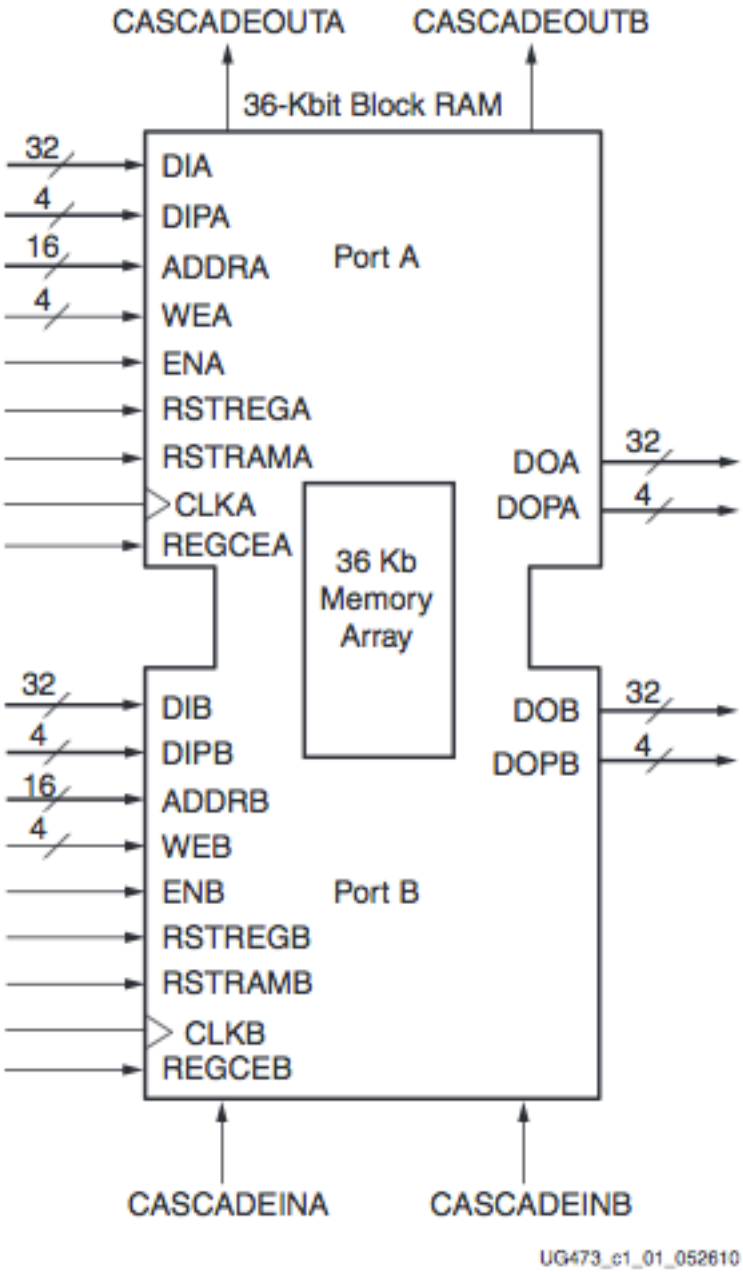


Figure 1-1: **True Dual-Port Data Flows for a RAMB36**

DSP Block/Hard Multiplier

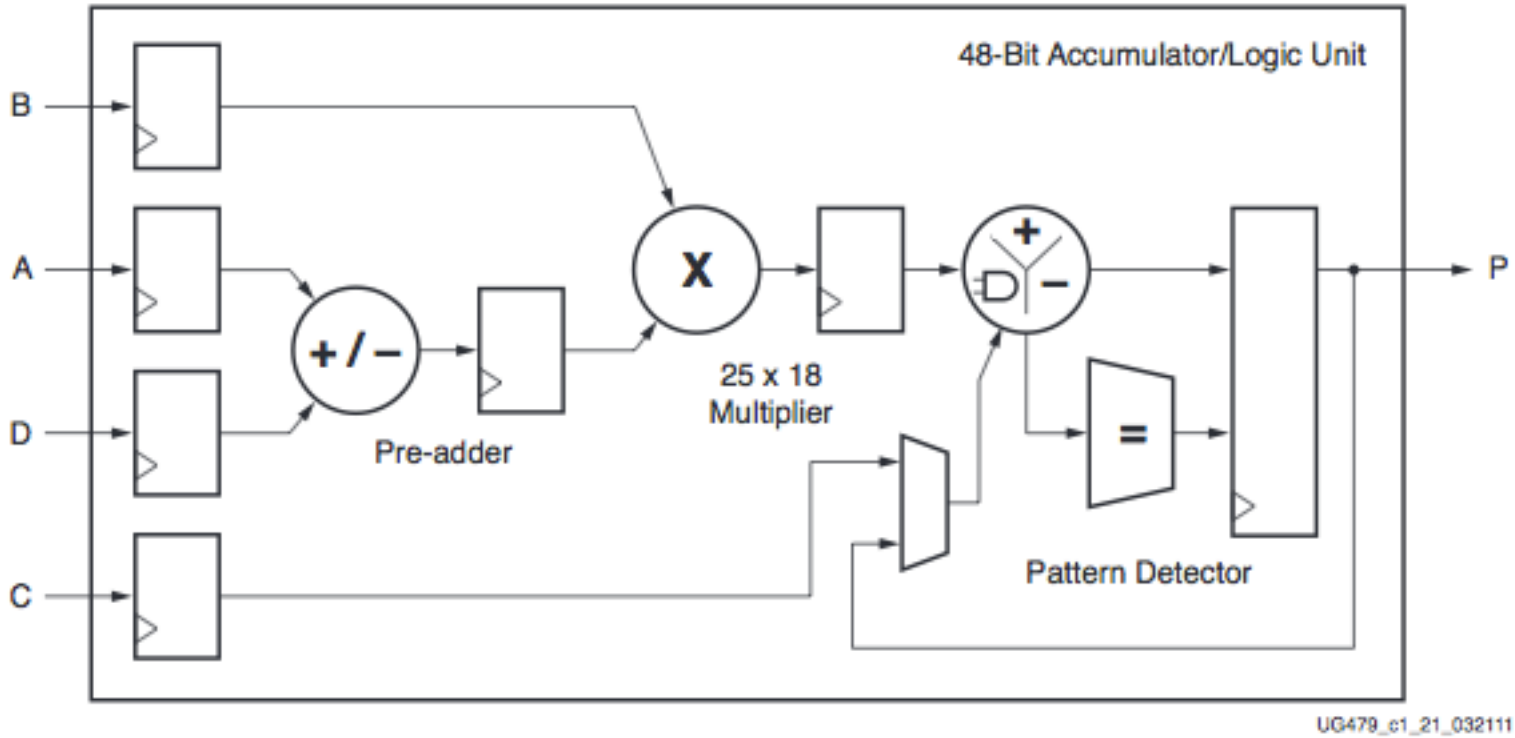
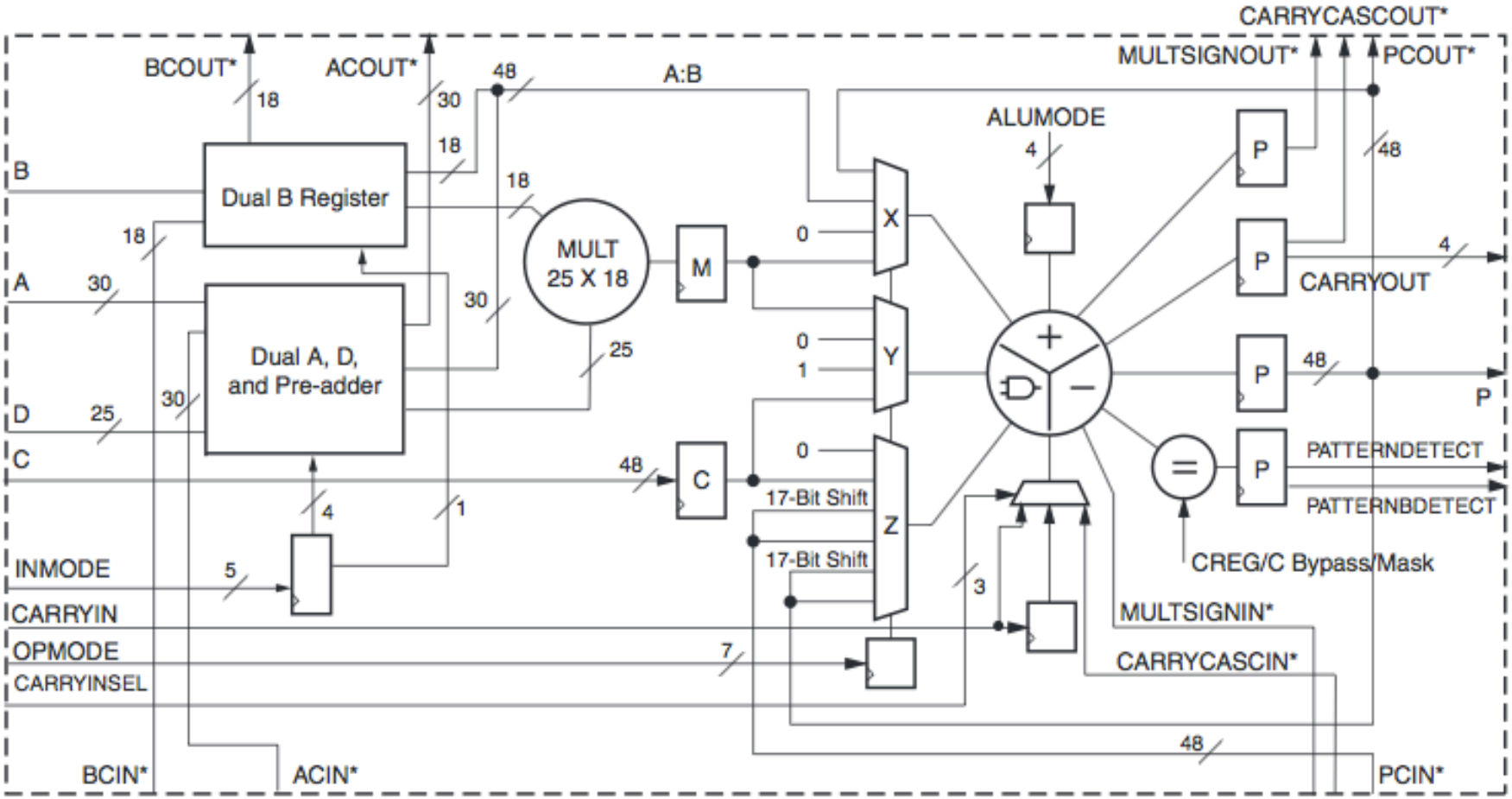


Figure 1-1: **Basic DSP48E1 Slice Functionality**



*These signals are dedicated routing paths internal to the DSP48E1 column. They are not accessible via fabric routing resources.

UG369_c1_01_052109

Figure 2-1: **7 Series FPGA DSP48E1 Slice**

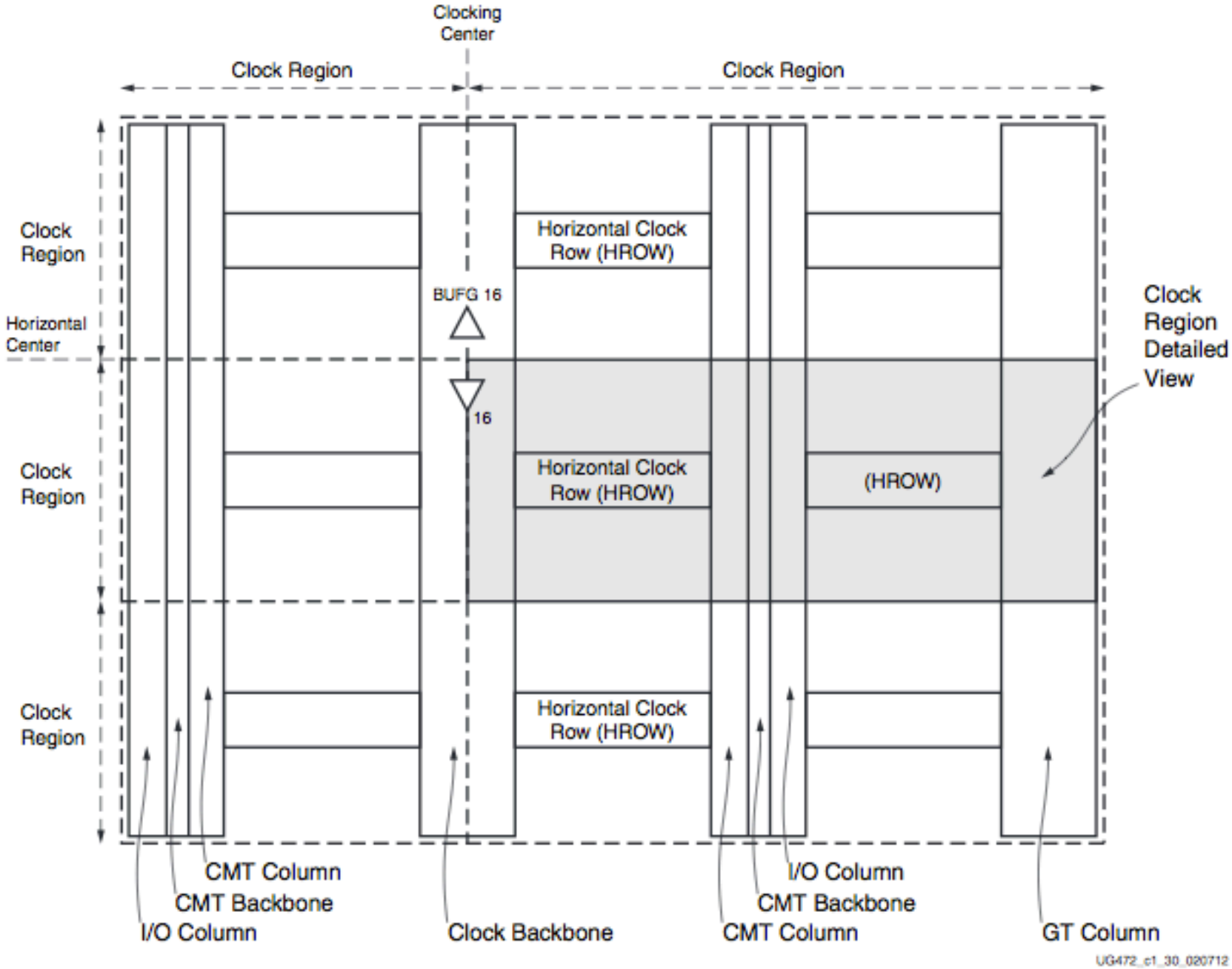


Figure 1-1: **7 Series FPGA High-Level Clock Architecture View**

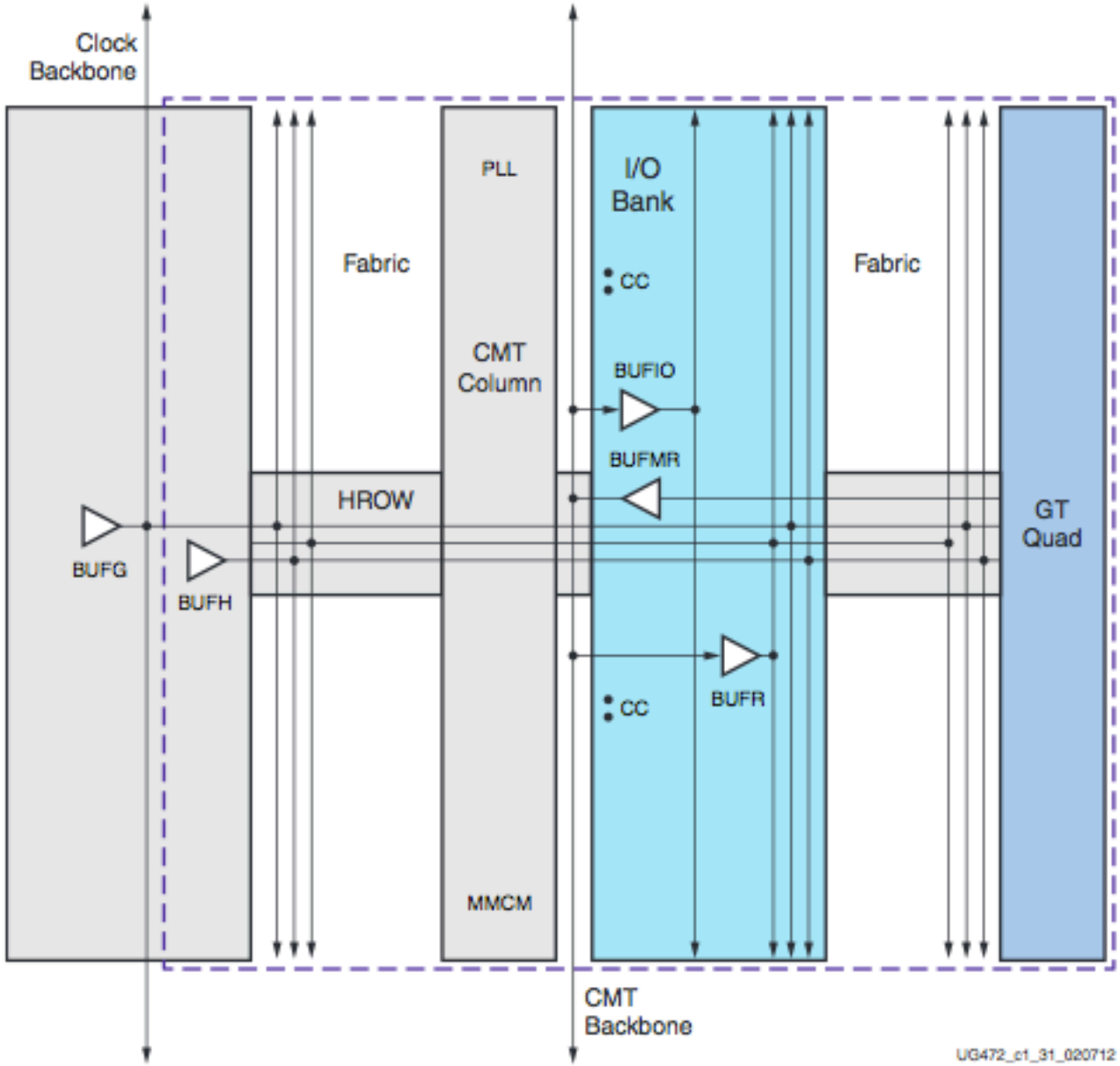


Figure 1-2: **Basic View of Clock Region**

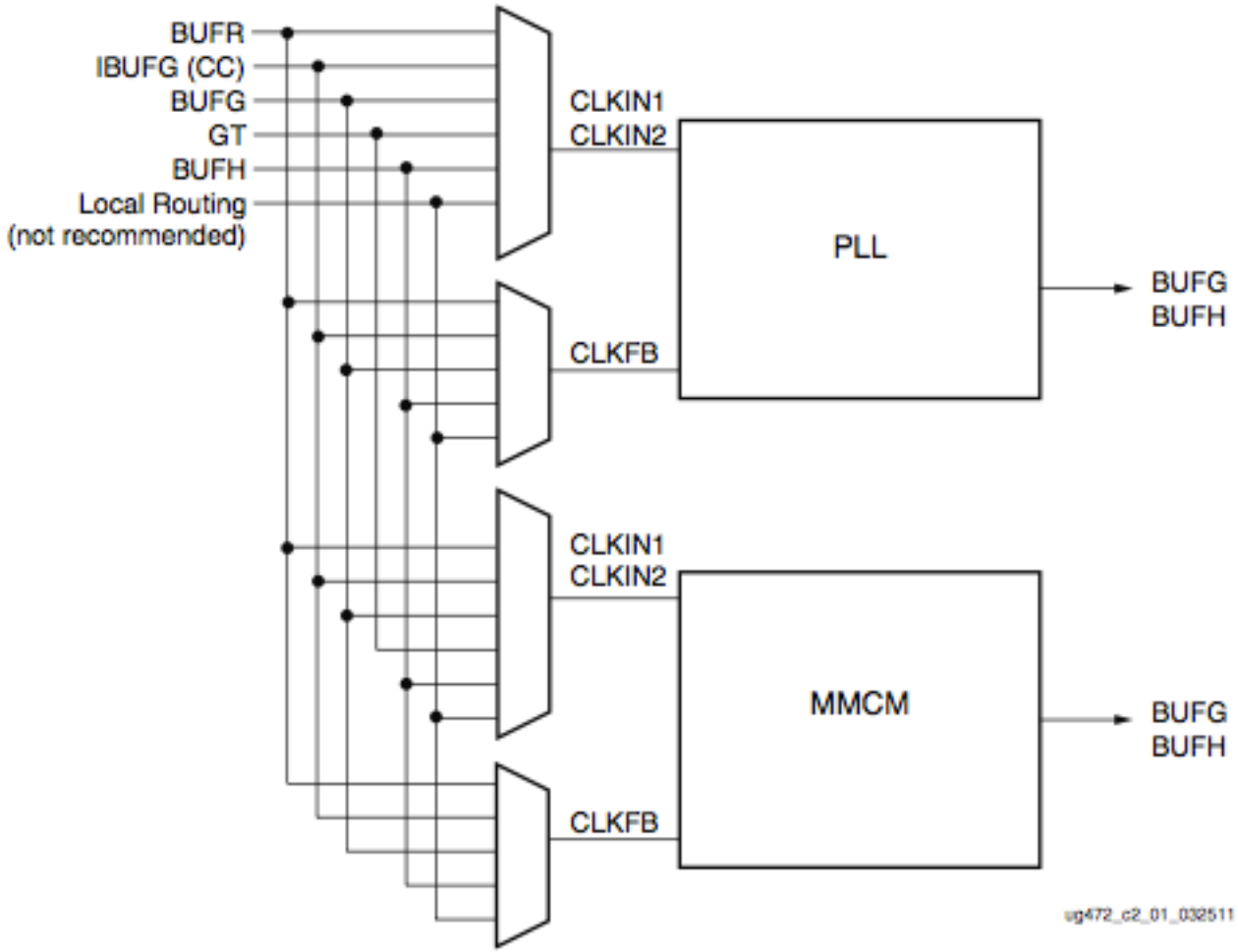


Figure 3-1: **Block Diagram of the 7 Series FPGAs CMT**

Chip Resource Architecture

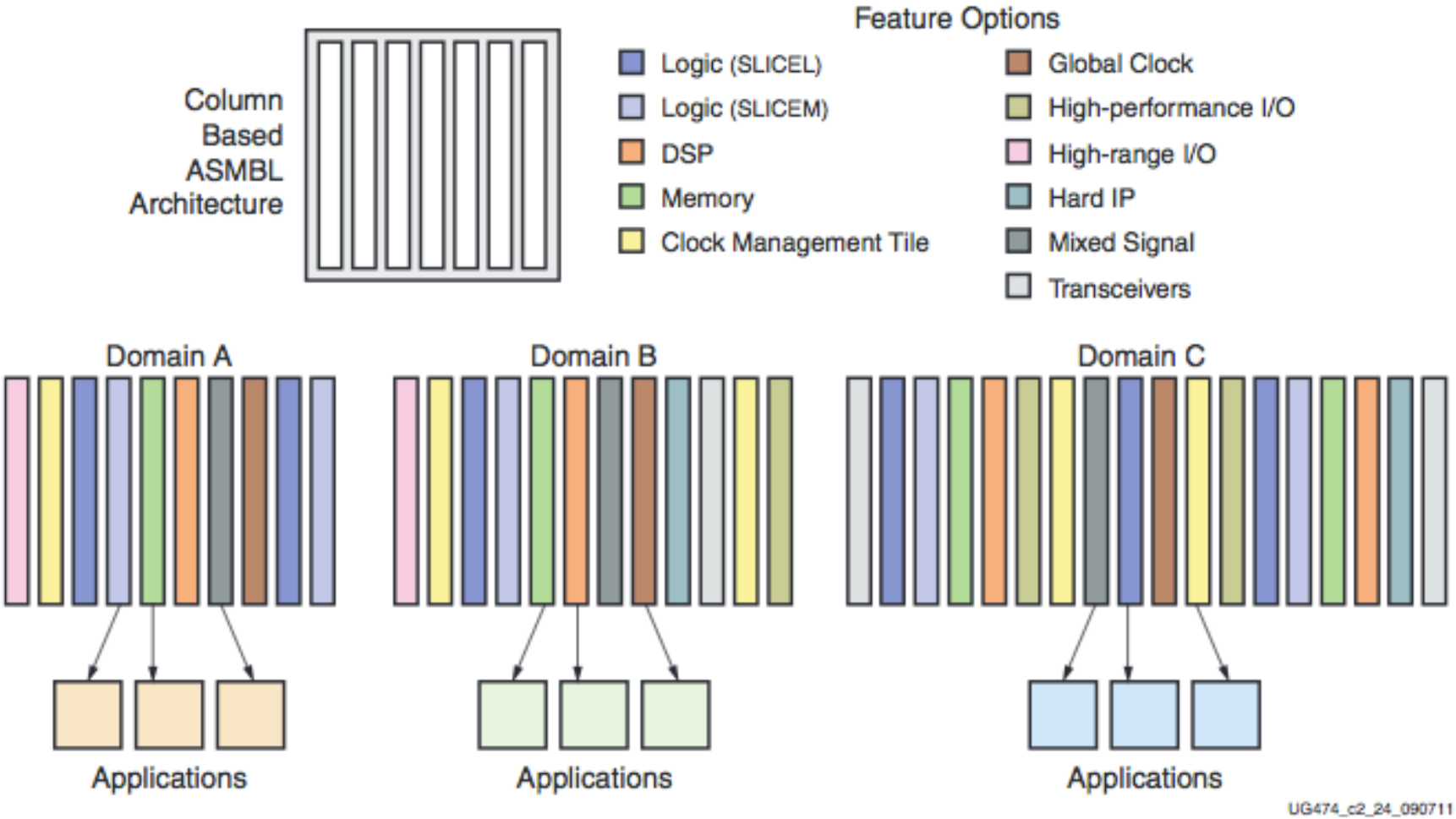


Figure 2-1: **ASMBL Architecture**

Placement Considerations

- Where are BRAMs?
- Where are DSP slices?
- Clock regions?
- Where are other resources used?
- Floor planning
  - Andraka.com
  - rapidwright.io

I/O Banks

- Groups of 50 IOBs (pins)
- Separate reference voltages for different types of I/O standards
- HP – high performance
- HR – high range
- Need to consider how many pins of each I/O standard you require
- Not just a pin, lots of logic

Select I/O

Table 1-1: **Supported Features in the HR and HP I/O Banks**

Feature	HP I/O Banks	HR I/O Banks
3.3V I/O standards[1]	N/A	Supported
2.5V I/O standards[1]	N/A	Supported
1.8V I/O standards[1]	Supported	Supported
1.5V I/O standards[1]	Supported	Supported
1.35V I/O standards[1]	Supported	Supported
1.2V I/O standards[1]	Supported	Supported
LVDS signaling	Supported[2]	Supported
24 mA drive option for LVCMOS18 and LVTTL outputs	N/A	Supported
V_{CCAUX_IO} supply rail	Supported	N/A
Digitally-controlled impedance (DCI) and DCI cascading	Supported	N/A
Internal V_{REF}	Supported	Supported

Table 1-1: **Supported Features in the HR and HP I/O Banks *(Cont'd)***

Feature	HP I/O Banks	HR I/O Banks
Internal differential termination (DIFF_TERM)	Supported	Supported
IDELAY	Supported	Supported
ODELAY	Supported	N/A
IDELAYCTRL	Supported	Supported
ISERDES	Supported	Supported
OSERDES	Supported	Supported
ZHOLD_DELAY	N/A	Supported

Notes:

1. Not all I/O standards and drive strengths are supported in both the HP and HR I/O banks. The I/O Bank Availability column in Table 1-55 shows the specific I/O standards that are available in the HP and HR I/O banks.
2. Although LVDS is generally considered a 2.5V I/O standard, it is supported in both the HR and HP I/O banks.

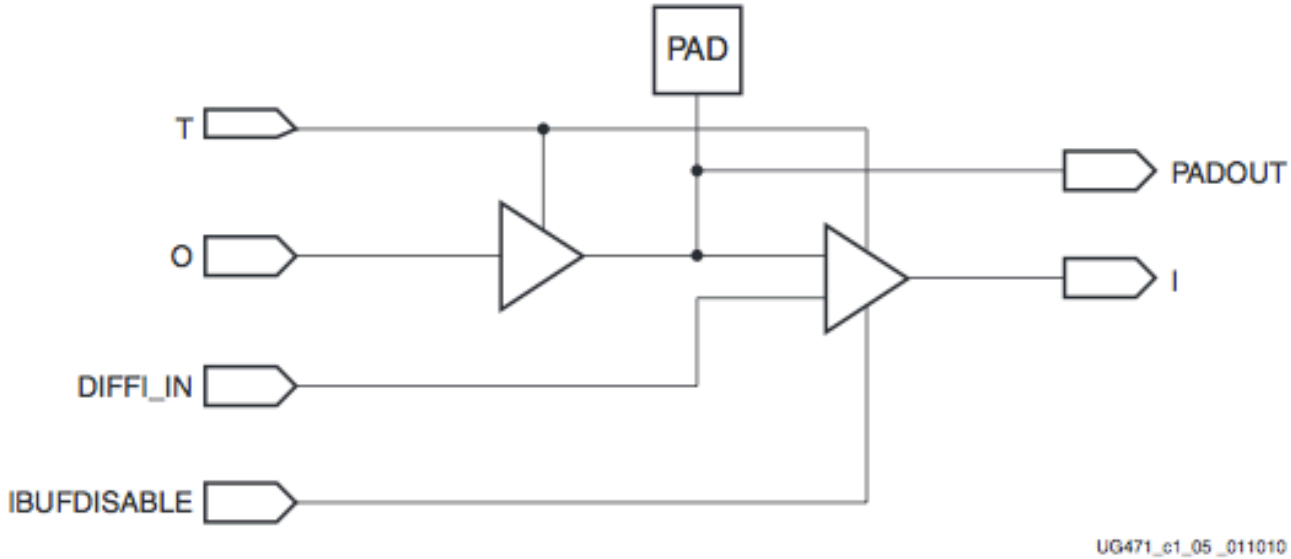


Figure 1-3: **Single-Ended (Only) HR IOB Diagram**

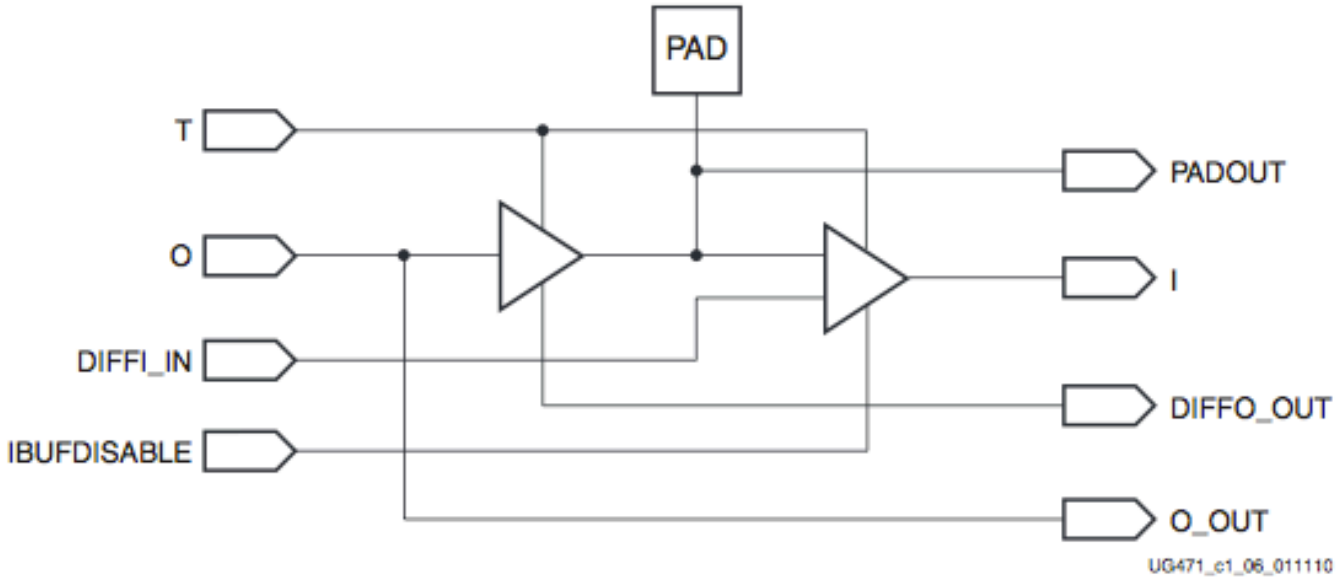


Figure 1-4: **Regular HR IOB Diagram**

I/O Logic Resources

7 series FPGAs contain the basic I/O logic resources from previous Xilinx FPGAs. These resources include the following:

- Combinatorial input/output
- 3-state output control
- Registered input/output
- Registered 3-state output control
- Double-Data-Rate (DDR) input/output
- DDR output 3-state control
- IDELAY provides users control of an adjustable, fine-resolution delay taps
- ODELAY provides users control of an adjustable, fine-resolution delay taps
- SAME_EDGE output DDR mode
- SAME_EDGE and SAME_EDGE_PIPELINED input DDR mode

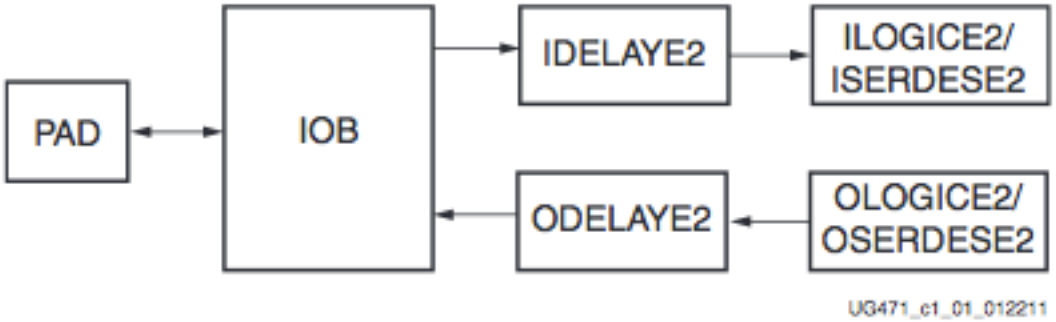


Figure 2-1: **7 Series FPGA HP Bank I/O Tile**

ISERDES/OSERDES

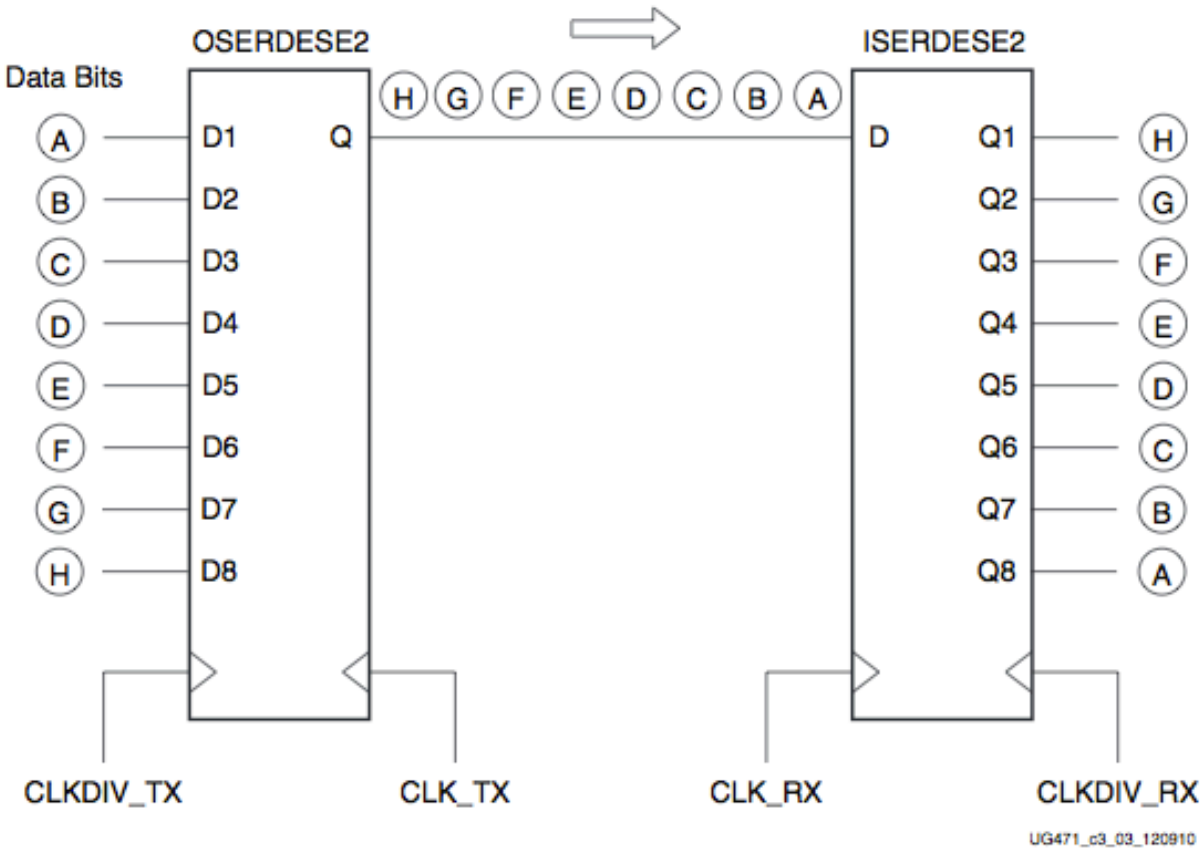


Figure 3-3: **Bit Ordering on Q1–Q8 Outputs of ISERDESE2 Ports**

Other Features

- PCIe
- Tri-mode ethernet MAC
- Multi-Gbit transceivers
- A/D block
- Stacked Silicon Interconnect (SSI)

Packaging

Table 8: **Virtex-7 FPGA Device-Package Combinations and Maximum I/Os - Continued**

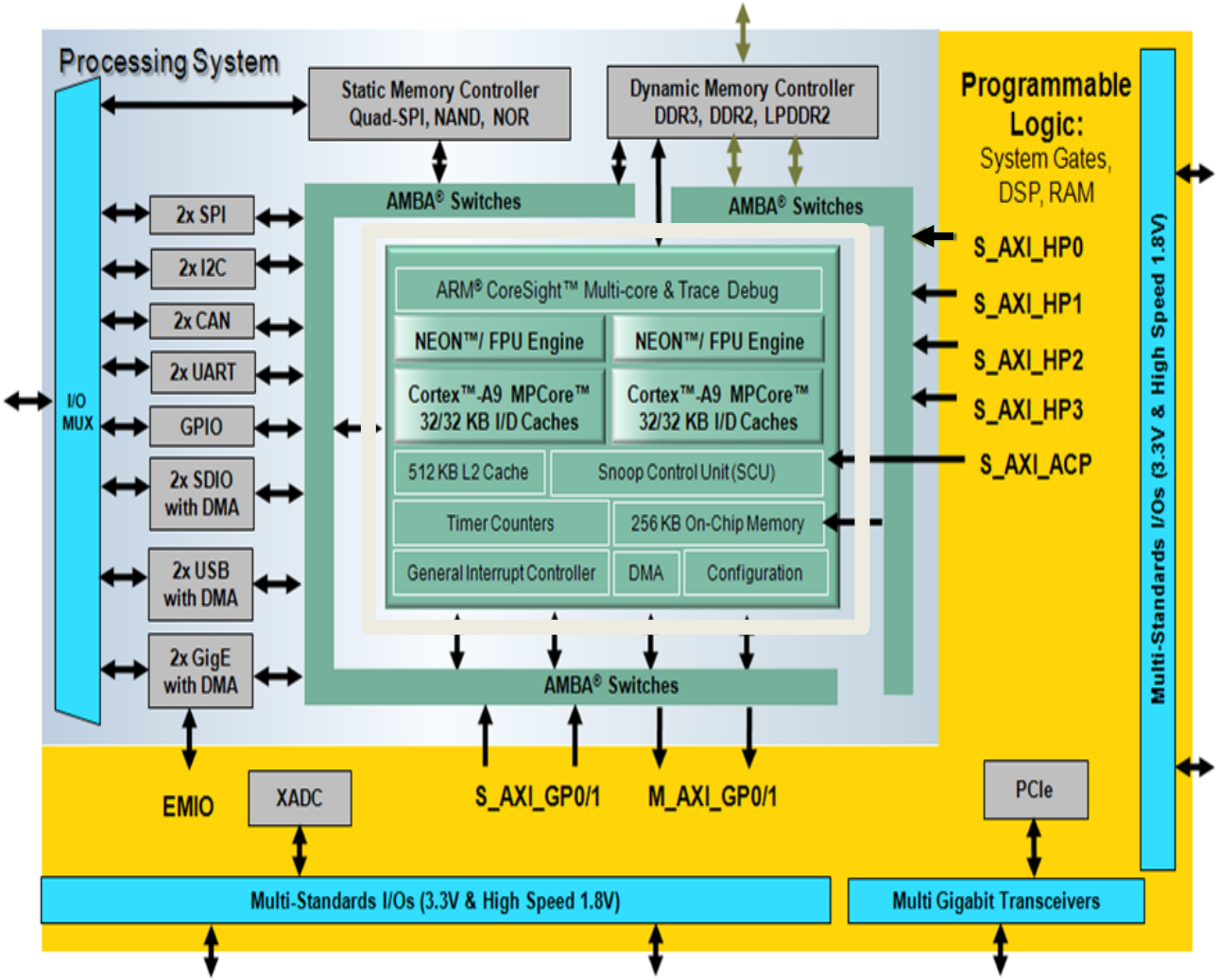
Package[1]	FFG1158			FFG1926[2]			FLG1926[2]			FFG1927			FFG1928[3]			FLG1928[3]			FFG1930[4]			FLG1930[4]		
Size (mm)	35 x 35			45 x 45			45 x 45			45 x 45			45 x 45			45 x 45			45 x 45			45 x 45		
Ball Pitch	1.0			1.0			1.0			1.0			1.0			1.0			1.0			1.0		
Device	GTX	GTH	I/O HP (5)	GTX	GTH	I/O HP (5)	GTX	GTH	I/O HP (5)	GTX	GTH	I/O HP (5)	GTX	GTH	I/O HP (5)	GTX	GTH	I/O HP (5)	GTX	GTH	I/O HP (5)	GTX	GTH	I/O HP (5)
XC7V585T																								
XC7V2000T																								
XC7VX330T																								
XC7VX415T	0	48	350							0	48	600												
XC7VX485T	48	0	350							56	0	600							24	0	700			
XC7VX550T	0	48	350							0	80	600												
XC7VX690T	0	48	350	0	64	720				0	80	600							0	24	1,000			
XC7VX980T				0	64	720							0	72	480				0	24	900			
XC7VX1140T							0	64	720							0	96	480				0	24	1,100

Notes:

1. All packages listed are Pb-free. Some packages are available in Pb option.
2. Devices in FFG1926 and FLG1926 are footprint compatible.
3. Devices in FFG1928 and FLG1928 are footprint compatible.
4. Devices in FFG1930 and FLG1930 are footprint compatible.
5. HP = High Performance I/O with support for I/O voltage from 1.2V to 1.8V.

SOC DEVICES

Zynq-7000 AP SoC Block Diagram



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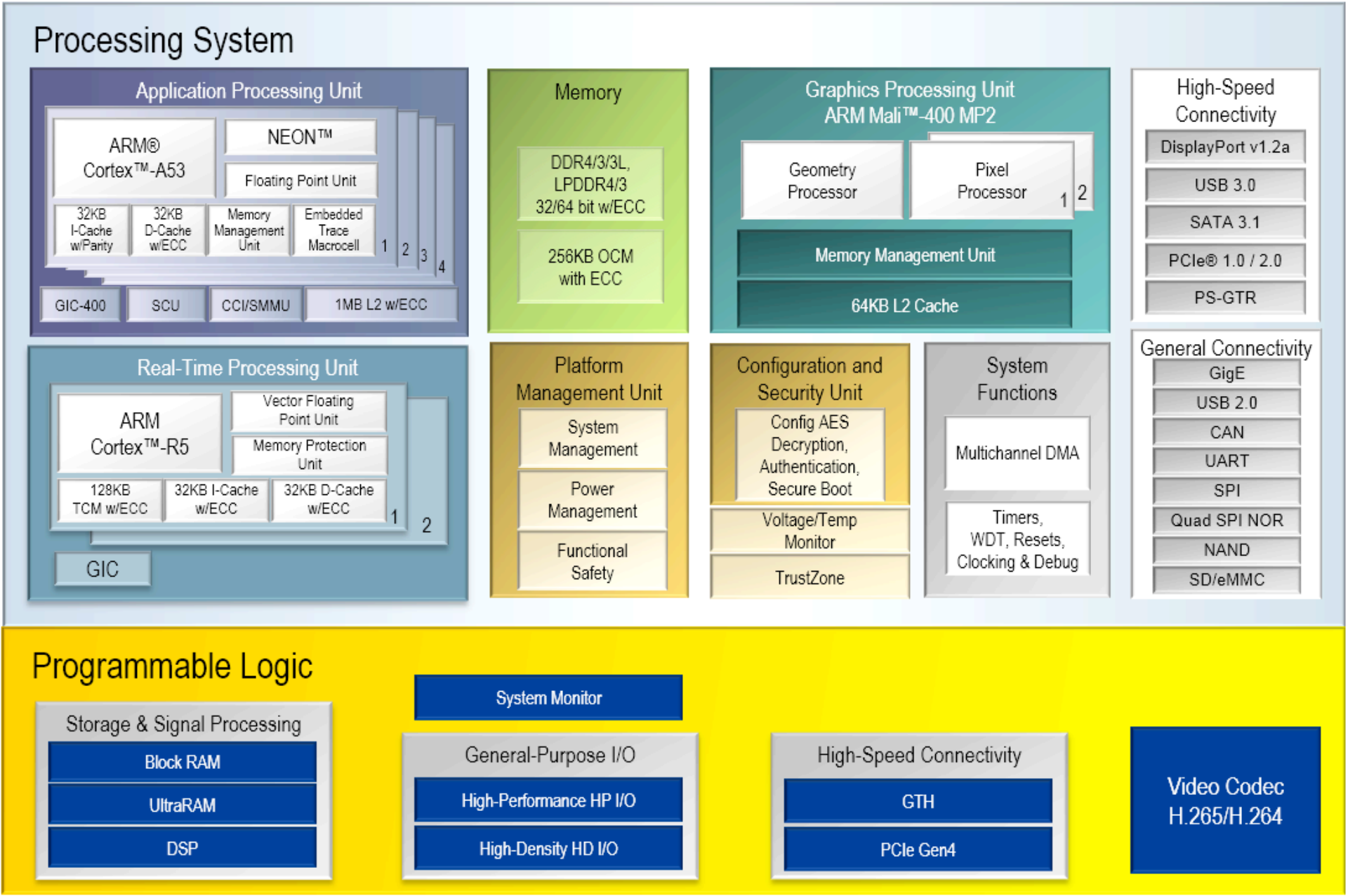
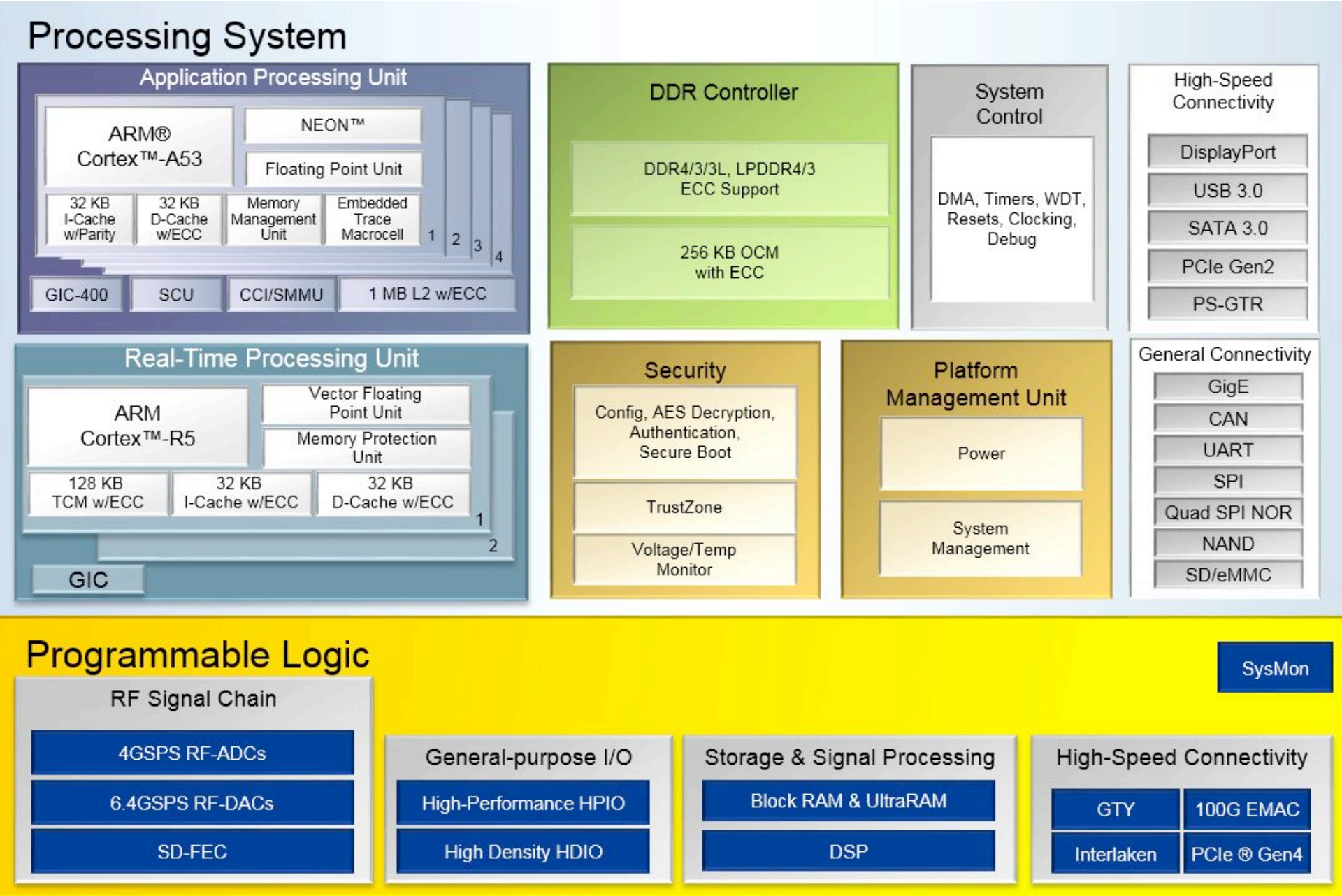
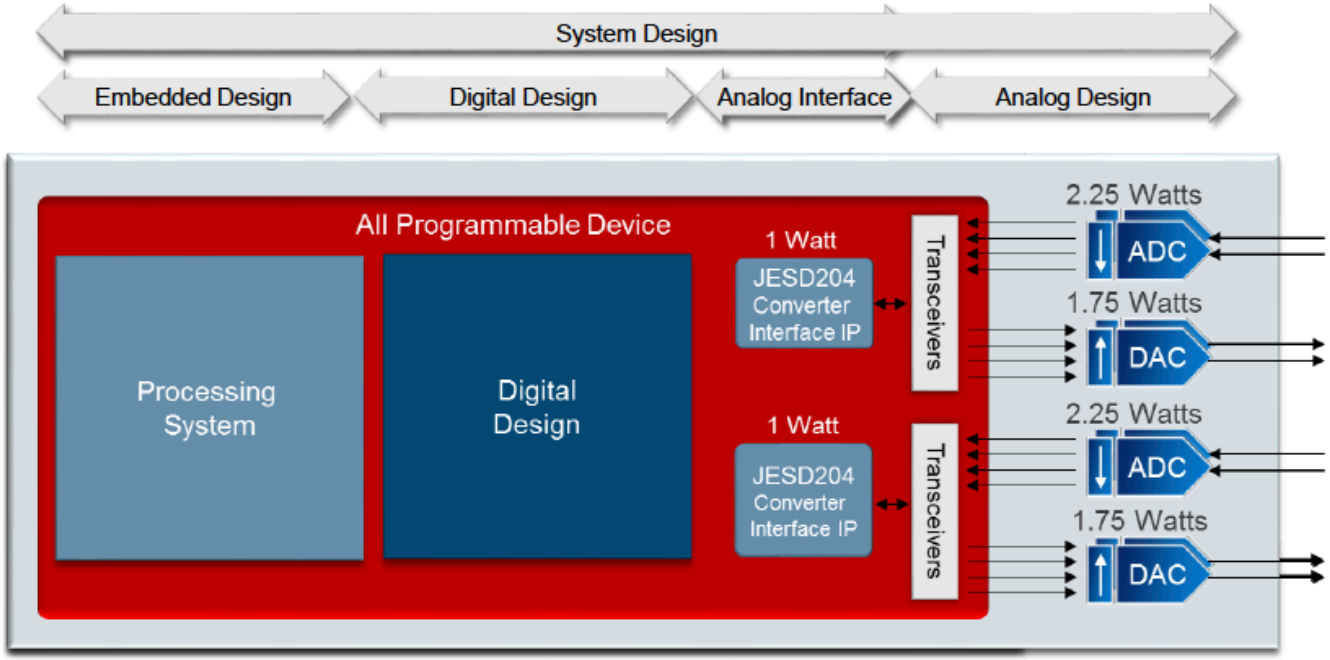
Zynq UltraScale+ EV



Zynq UltraScale+ RFSoCs

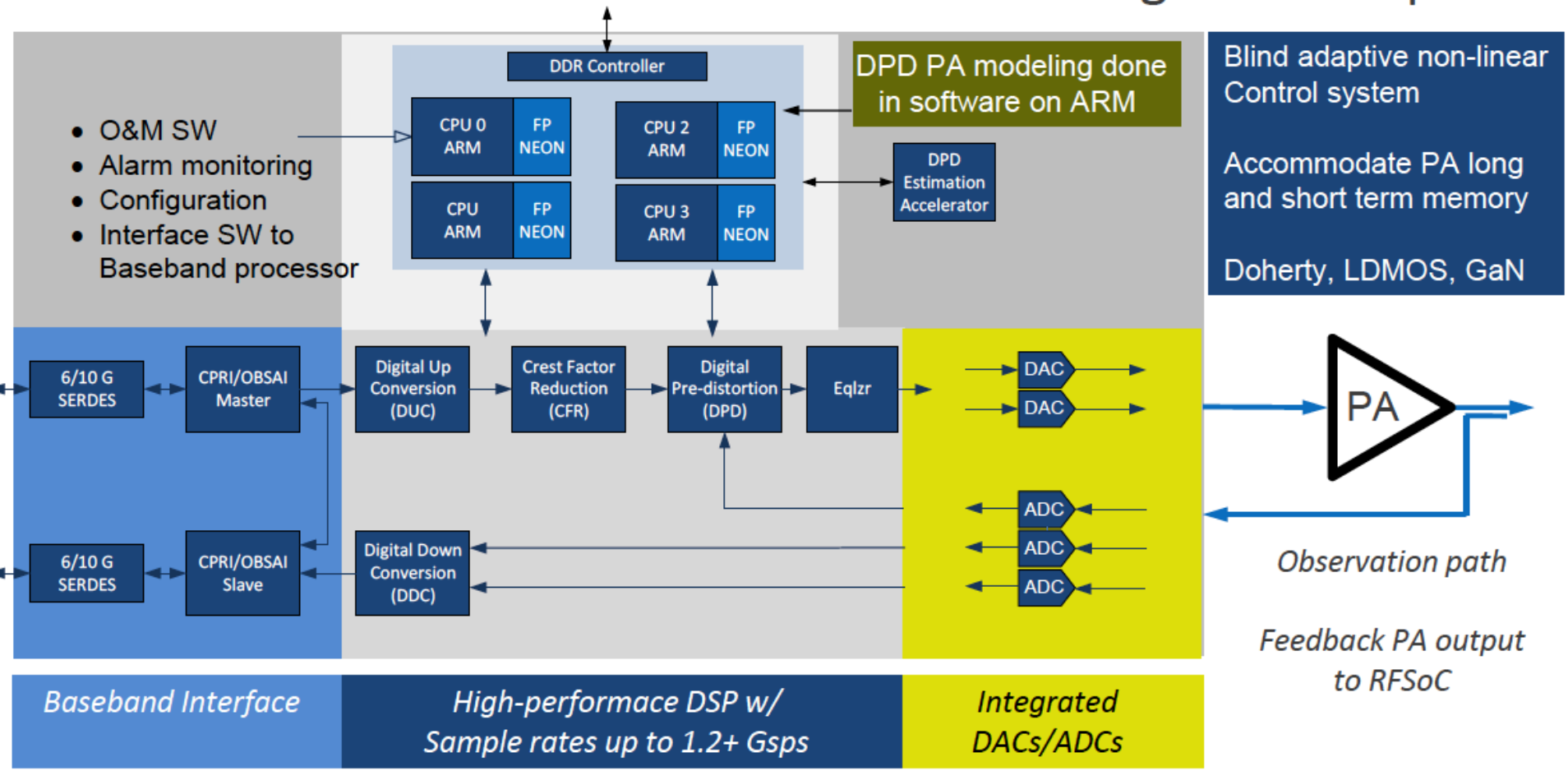


Reduced Power, Form Factor, and Design Cycle

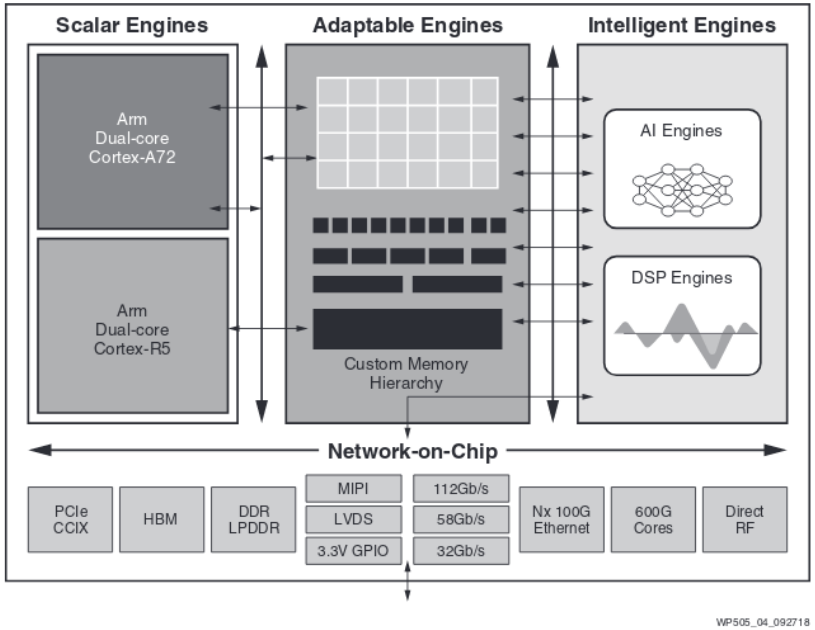


XILINX ALL PROGRAMMABLE.

Xilinx 16nm RFSoC Radio :: DSP + Mixed Signal on Chip

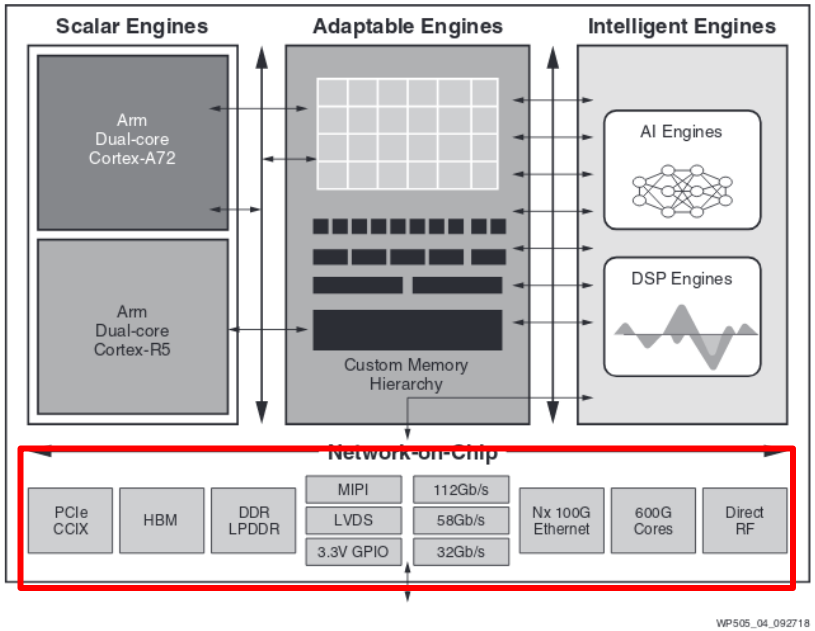


Adaptive Compute Acceleration Platform



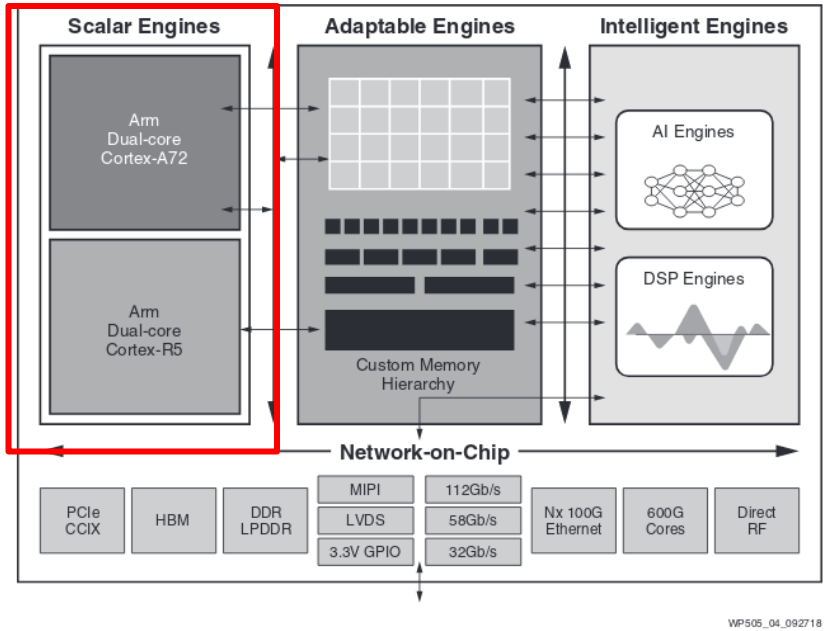
- Versal is first of ACAP
- Entire compute platform on one device
- Combines Scalar Processors (CPUs) with Adaptive Logic (FPGA) and Systolic Array Processing engine (GPU)
- Connected with a hardened NOC
- 7 nm

Adaptive Compute Acceleration Platform



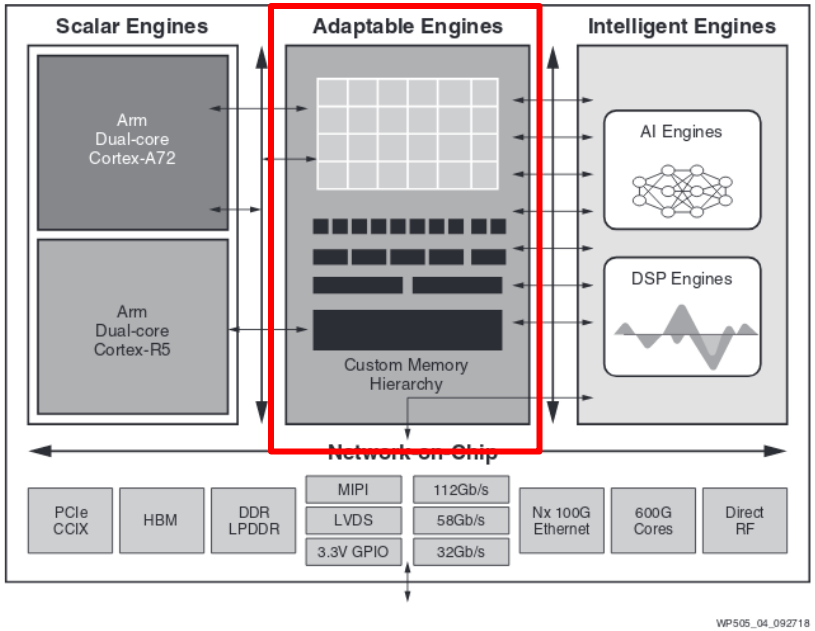
- Hardened I/O
  - Allows ready to use from start up
  - Includes:
    - PCIe
    - HBM interface
    - DDR interface
    - High speed Sertis

Adaptive Compute Acceleration Platform



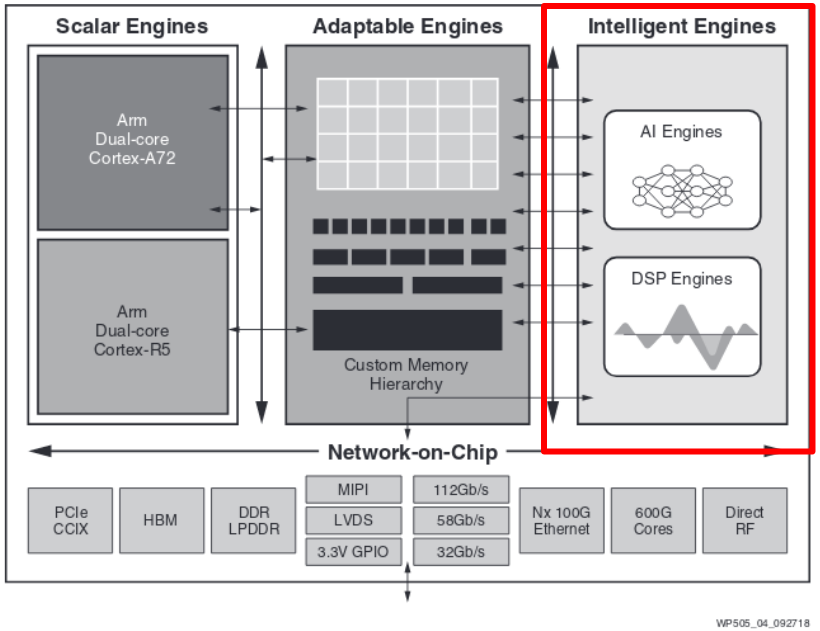
- Processor and Platform Management
  - ARM A72 – 4 Core processor
  - Arm R5- dual core real time processor
  - Used for platform management
    - SW Libraries to manage rest of connected device
  - Platform management controller is hardened microblaze

Adaptive Compute Acceleration Platform



- Close to traditional FPGA
  - 4x larger CLBs than Ultrascale
    - Intra-CLB routing
  - Cascade chains between LUTs within CLB
  - More details later

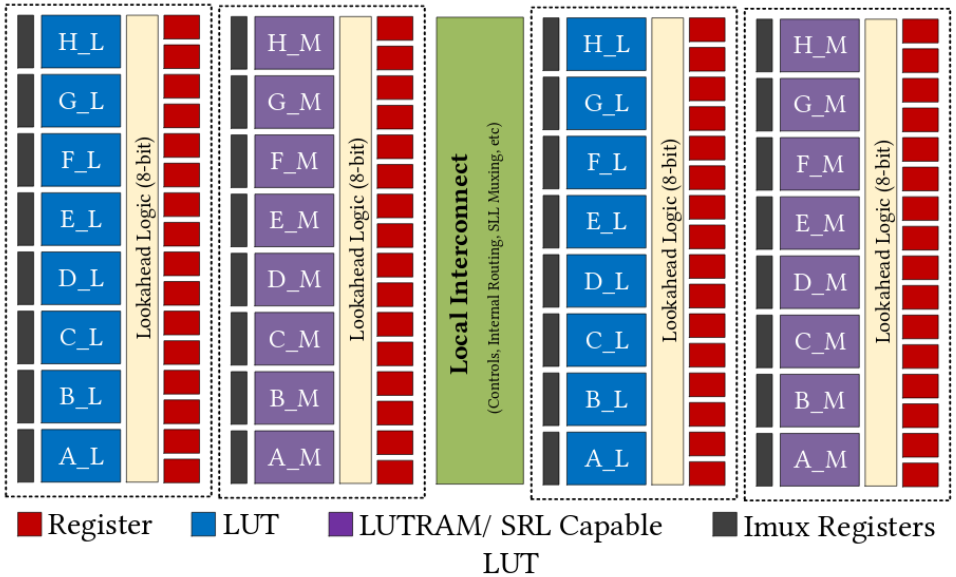
Adaptive Compute Acceleration Platform



- Systolic Array
  - Configurable end points
  - Can create pipes between cores
  - Entirely software programmable
  - More details Later

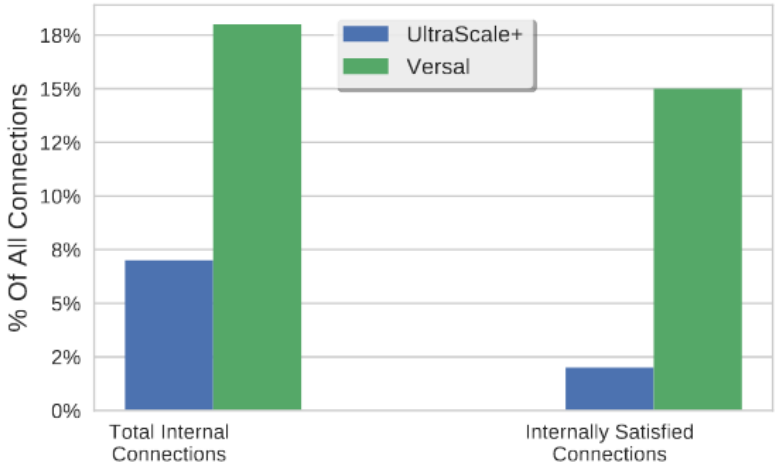
ADAPTIVE ENGINES (PROGRAMMABLE LOGIC)

Configurable Logic Block



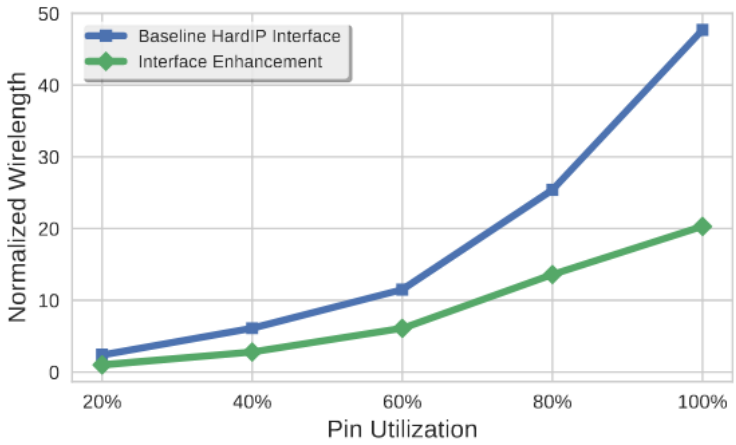
- 32 LUTs 64 registers, 4x from UltraScale
- Larger CLB internalizes lot of logic reducing strain on global routing
- Can create larger LUT with cascading logic

Local Interconnect within CLB



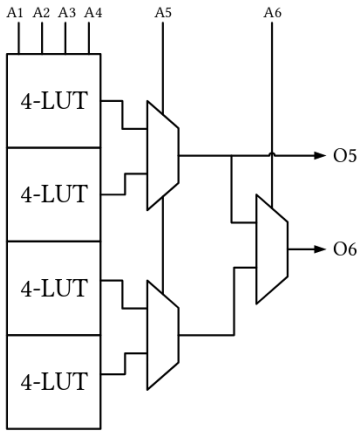
- Larger CLB more connections can fit within CLB
- Theoretical routing from pin to pin, 83 % possible in Versal as opposed to 28 % in UltraScale

Local Interconnect Connections to Hardened IP

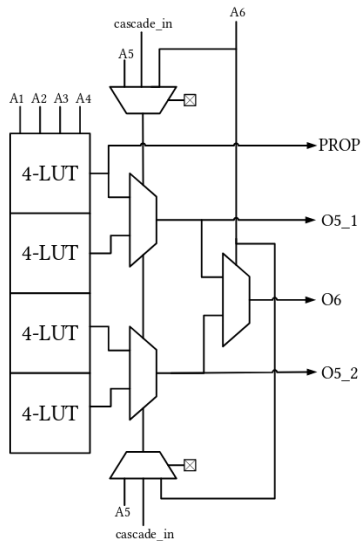


- Local interconnect for Hardened IP as well (PCIe, BRAM, etc.)
- The gapening of wirelength at higher utilization suggests global routing resources are being saved

Versal Lookup Table



(a) UltraScale 6LUT



(b) Versal 6LUT

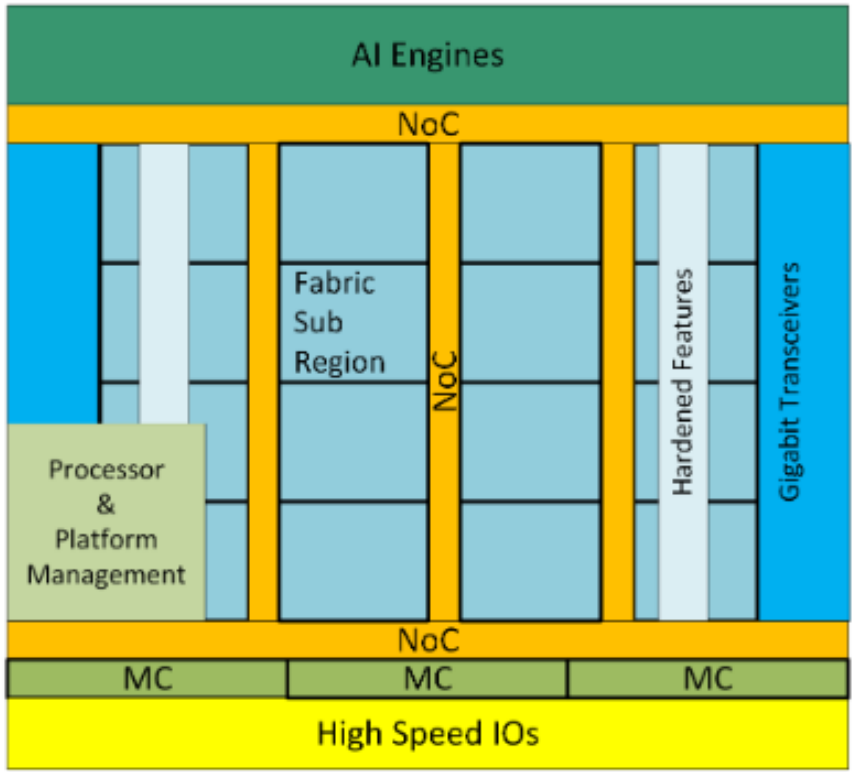
- Ultrascale LUT Functions
  - Any 6 input function
  - Or two smaller 5 input functions
- Versal LUT Functions
  - Any 6 input function
  - Two smaller 6 input functions
- Cascading logic helps meeting timing

NETWORK ON CHIP

Network On Chip Intro

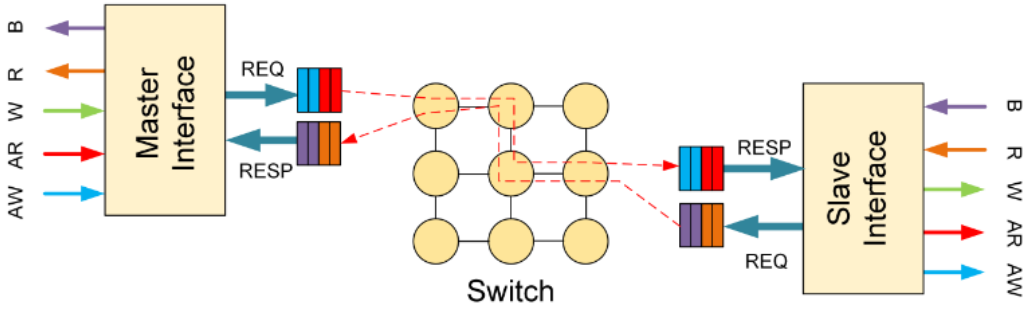
- Needed as bandwidth requirments on chip have increased
  - Eg. HBM 16 to 32 times memory requirements
  - Used in ASICs and SOCs
- Efficient since same physical resource across several endpoints
- Some sideband information
  - Ordering ID
  - Memory attributes (security, read-write priveliges)
  - Cache attributes
  - Packing
  - Strobes
  - Burst
  - QoS

Versal Chip Overview



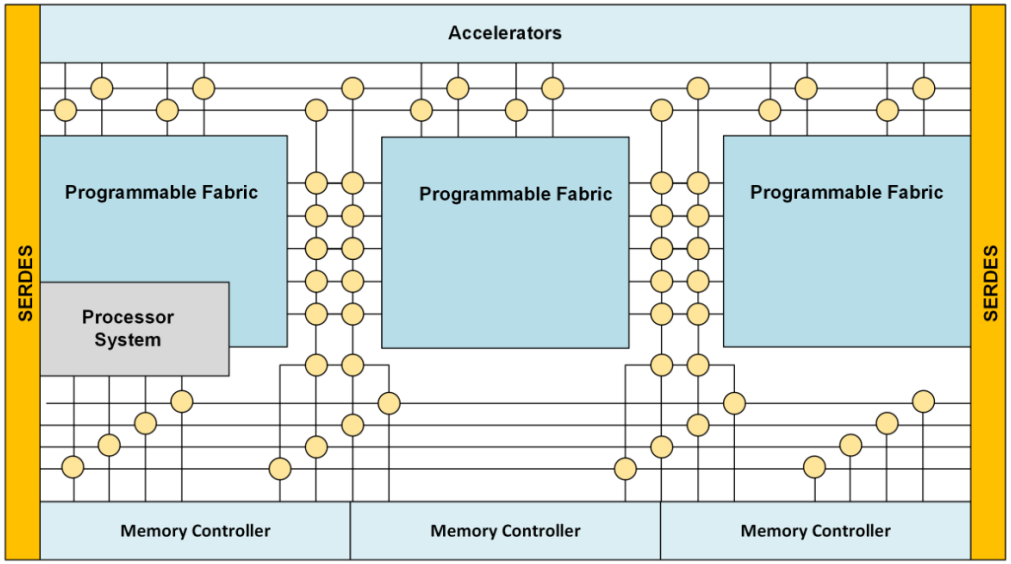
- Bottom of device: high speed IOS, memory controllers
- Top of device, AI engines
- Left and right side, transceivers
- Processor subsystem and platform management on lower left
- Rest of device is traditional FPGA fabric
- NOC is skeleton
- Wormhole routing
- QoS

Packet Transport



- Standard AXI for hard/soft masters and slaves
- Ingress NMU (NOC master)
- Egress NSU (NOC Slave)
- Write address and data combined in packet
  - Reduces flexibility from standard as standard allows write transaction to begin before data is ready
- Ingress and Egress different frequency than packet frequency
- Proprietary physical transport protocol with AXI endpoints

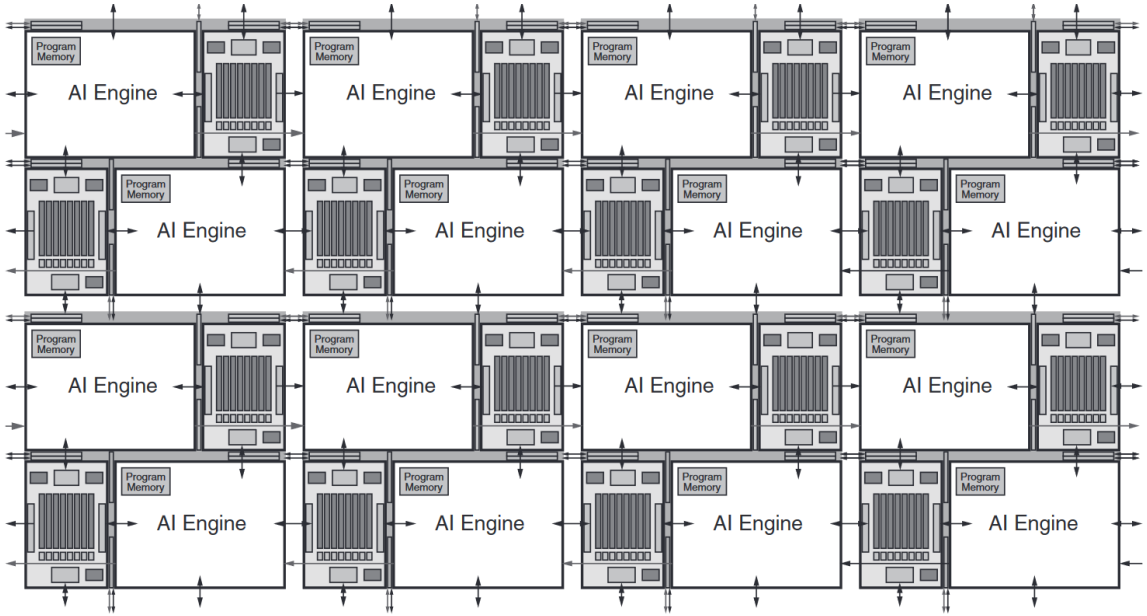
NOC Topology



- HNOCs at top and bottom
  - Asymmetrical because goal for unified memory space across all NMUs (requiring more cross sectional bandwidth)
- VNOCs form columns next to FPGA to connect to fabric
- Not regular mesh as FPGA only connects to VNOCs and not HNOCs directly
- Each lane is 128 bits running between 900 MHz and 1GHz

ARTIFICIAL INTELLIGENCE ENGINE

AIE



- Each engine consists:
  - Simple scalar engine
  - Vector engine for fixed and floating point
  - Program and data memory
  - AXI movement channels
- Insns are SIMD and VLIW

AIE (cont)

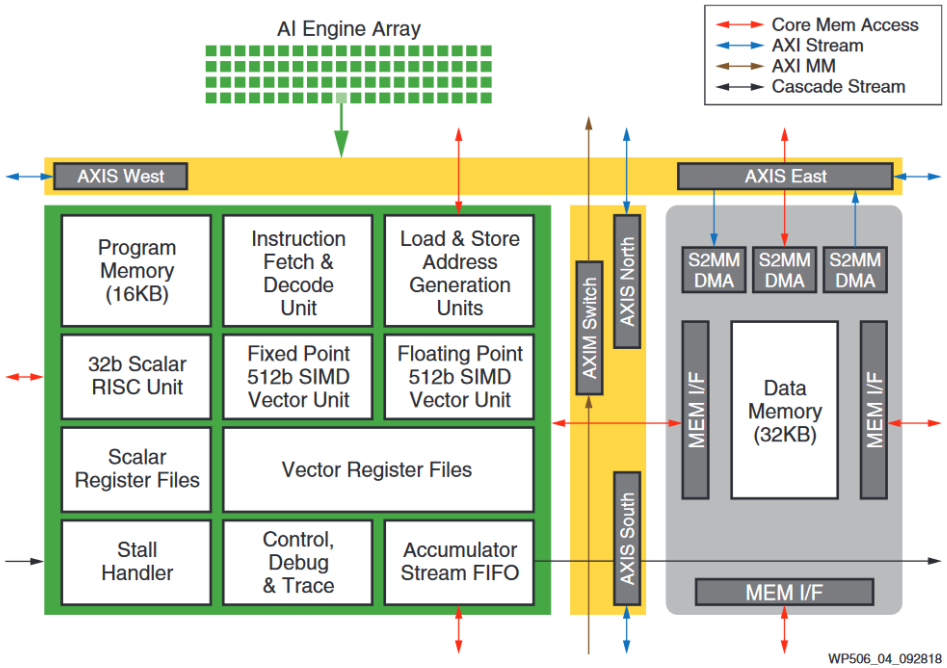
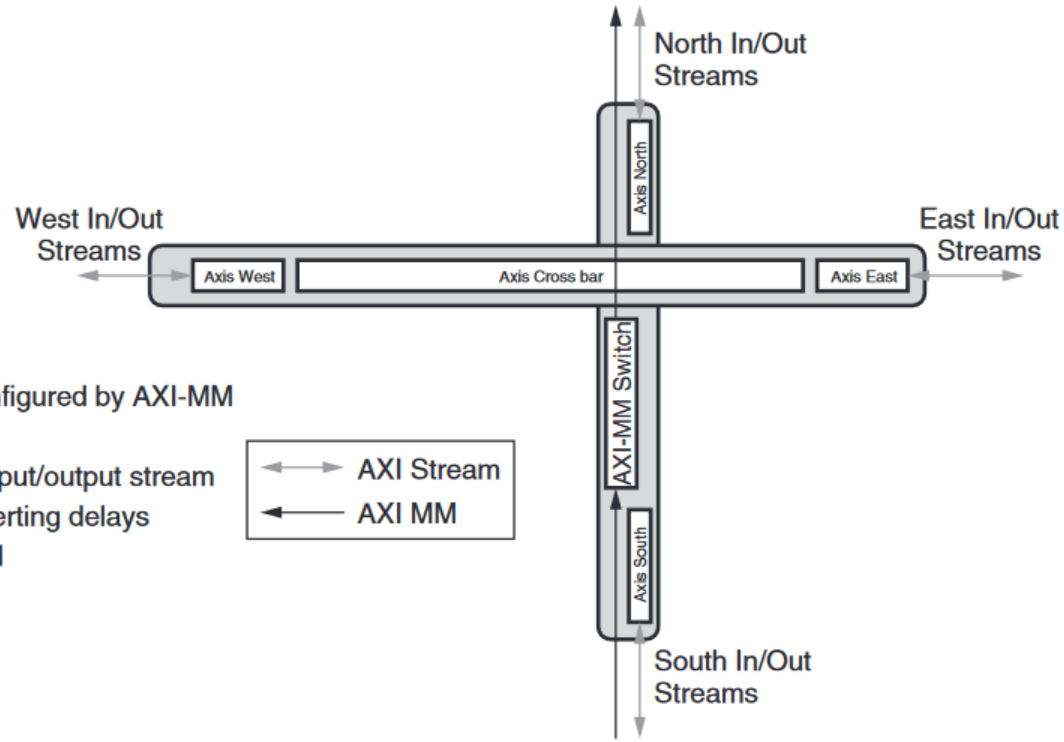


Figure 4: **Detail of AI Engine Tile**

- AXIMM to neighbouring AI engines
- AXIS crossbar
- Neighbouring AI engines also share memory

AIE Routing



AXI-Stream Interconnect Statically configured by AXI-MM
- Master and slave ports
- Each port handler selects route for input/output stream
- Each switch has FIFO buffers for inserting delays
- Port can be circuit or packet switched