1 chip XDP debug component list(CXDP@)			
item	Qty	Part reference	Part description
1	2	CC17,CC21	SE00000G880 (S CER CAP 0.1U 25V K X5R 0402)
2	4	RC98,RC99,RC109,RC112	SD028000080 (S RES 1/16W 0 +-5% 0402)
3	4	RC102,RC106,RC113,RC120	SD028100180 (S RES 1/16W 1K +-5% 0402)
4	1	UC7	SA00005X900 (S IC 74CBTLV3126BQ DHVQFN 14P BUS SWITCH)
5	1	JXDP1	SP02000L900 (S W-CONN SAMTEC BSH-030-01-L-D-A-TR 60P)

COMPAL CONFIDENTIAL

MODEL NAME : ZAM70

PCB NO : DAA0007U000

BOM P/N : 4319R031L01 (SMT MB AA901 ZAM70 U W/DOCK I5 1.9G R1)
4319R031L02 (SMT MB AA901 ZAM70 U W/DOCK I3 1.9G R1)

GPIO MAP: 3.6C

Huston 14" UMA

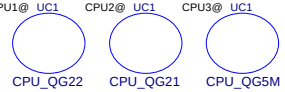
Broadwell U

2014-03-07

REV : 0.3 (X01)

@ : Nopop Component
EMC@ : EMI, ESD and RF Component
@EMC@ : EMI, ESD and RF Nopop Component
CXDP@ : XDP Component
VPRO@ : Support VPRO
CONN@ : Connector Component

CPU1@ UC1 CPU2@ UC1 CPU3@ UC1



MB PCB

Part Number	Description
DAA0007U000	PCB 13D LA-A901P REV0 MB/UMA DOCK 1

Layout Dell logo

REV: X01
PWB: DKNFC
DATE: 1410-06

Compal Electronics, Inc.

Title: Cover Sheet

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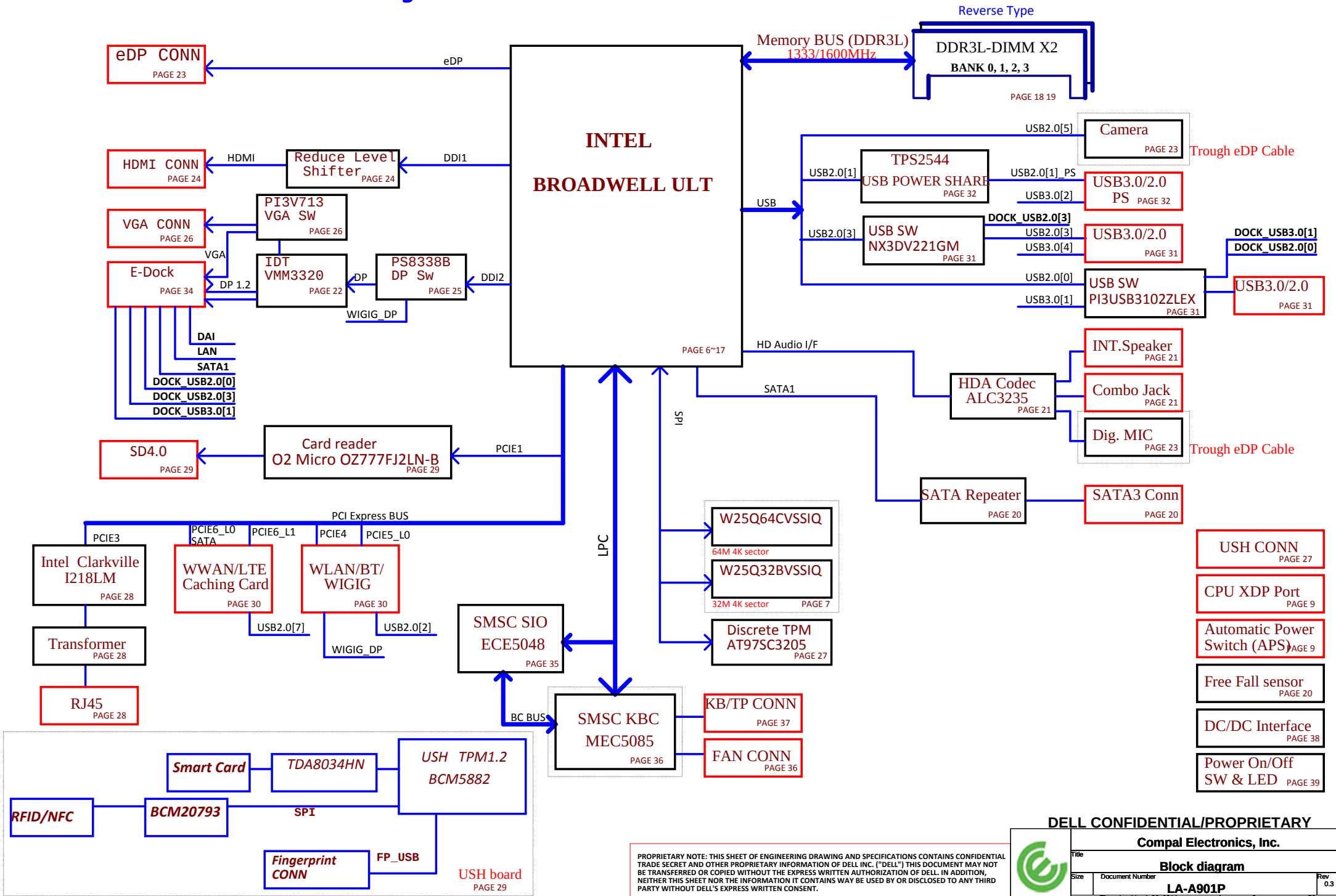
Houston 14 UMA Dock Block Diagram



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	Block diagram
Size	Document Number: LA-A901P
Rev	0.3
Date:	Thursday, March 06, 2014
Sheet	2 of 53

POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

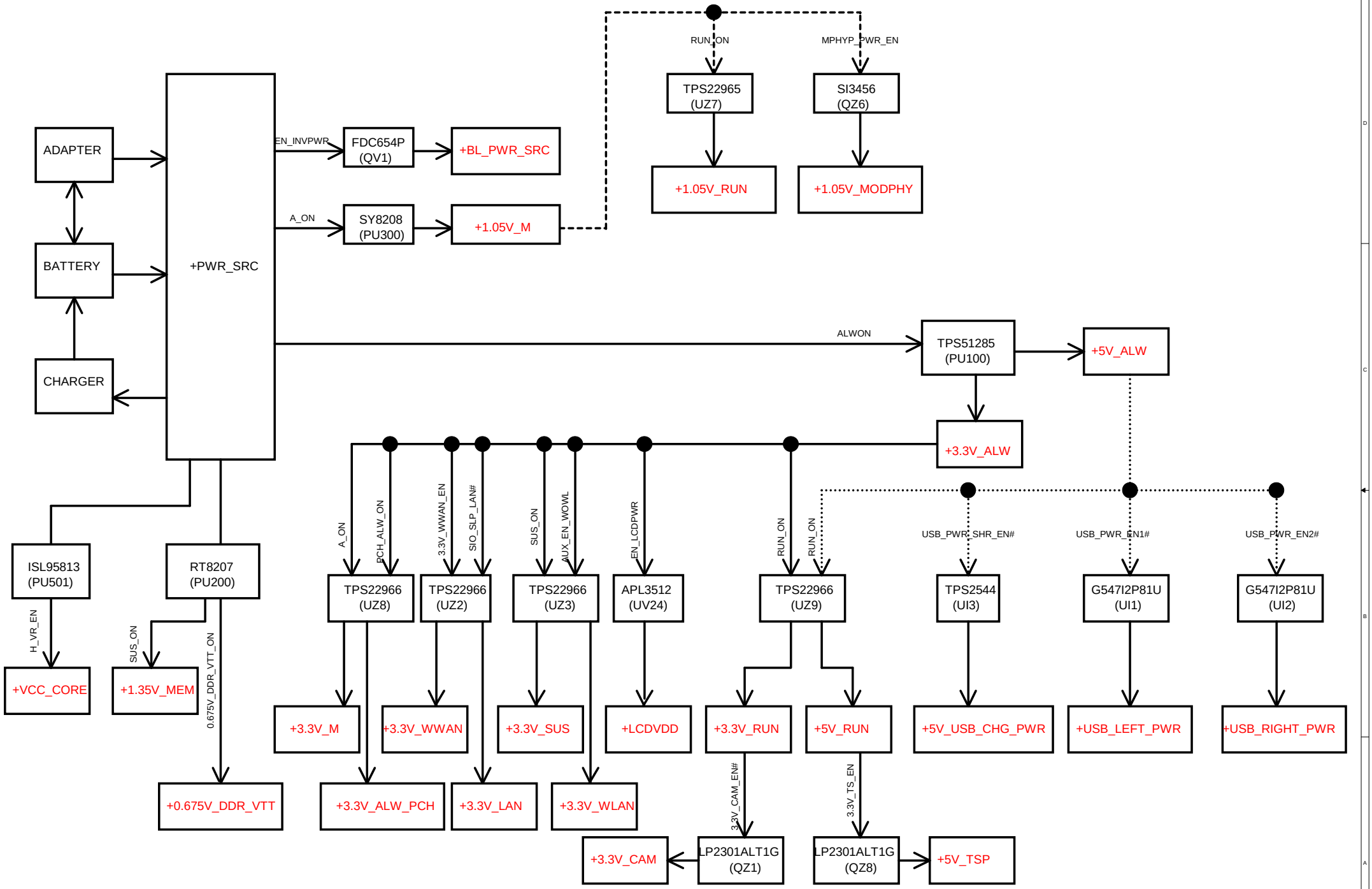
power plane / State	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE +1.5V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and PM Table

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN
PCIE 5			WIGIG
PCIE 6	L3	SATA 0	JDOCK1 (DOCK)
	L2	SATA 1	JSATA1 (HDD)
	L1	SATA 2	SSD Cache (PCIE)
	L0	SATA 3	SSD Cache (SATA/PCIE)/HCA

	USB PORT#	DESTINATION
BDW ULT	0	JUSB1
	1	JUSB3
	2	WLAN + BT
	3	JUSB2
	4	Touch Screen
	5	CAMERA
	6	USH
	7	WWAN

USH	0	BIO
	1	NA



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Title: Power rails

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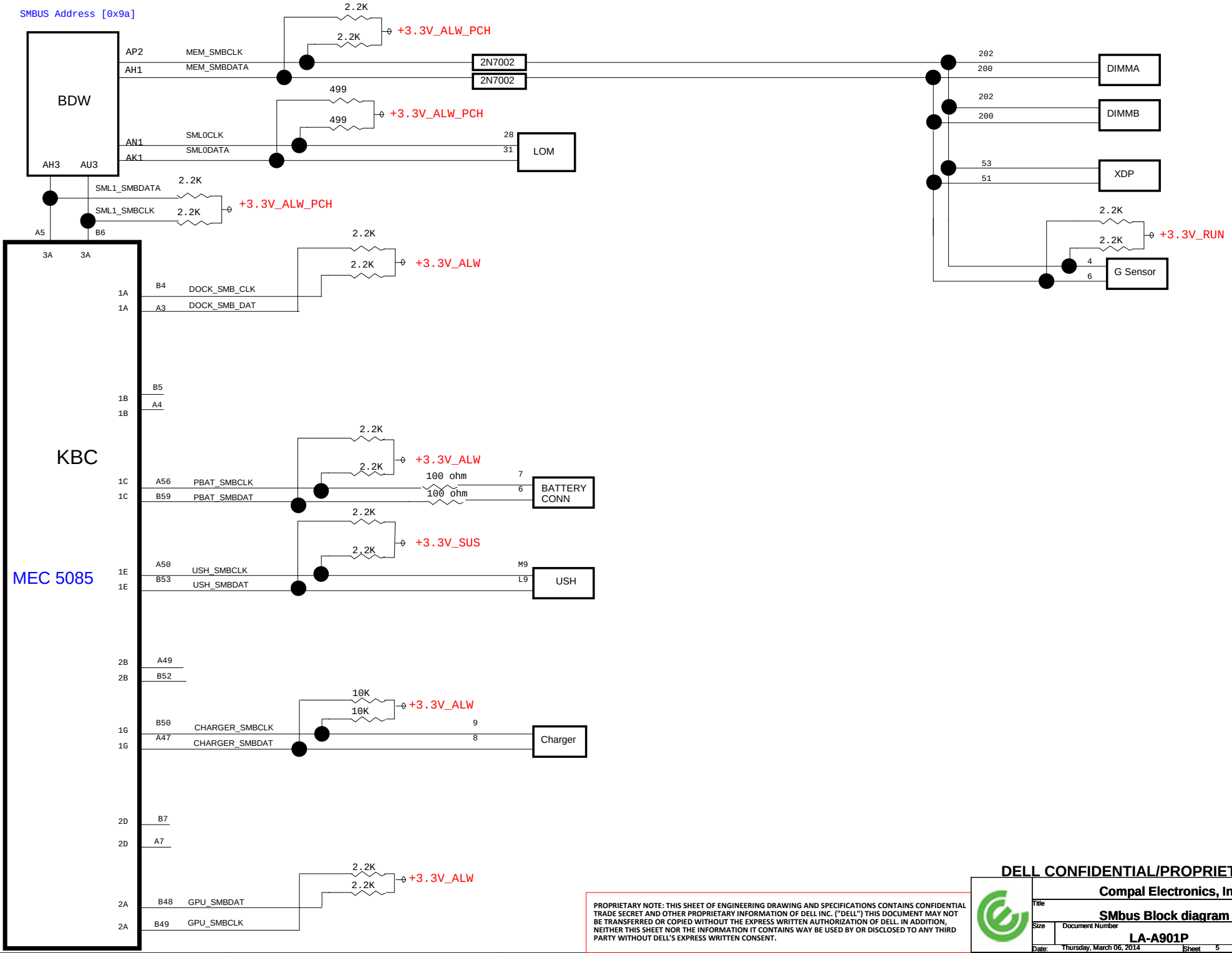

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: SMbus Block diagram

Size | Document Number: LA-A901P | Rev: 0.3

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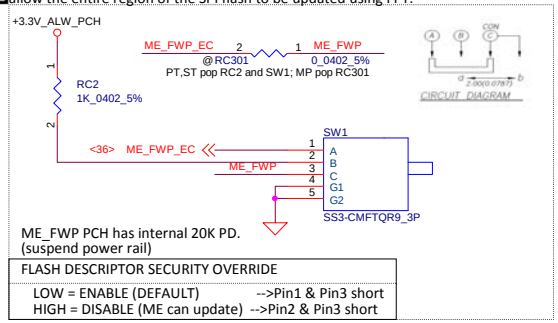
UMA SATA port

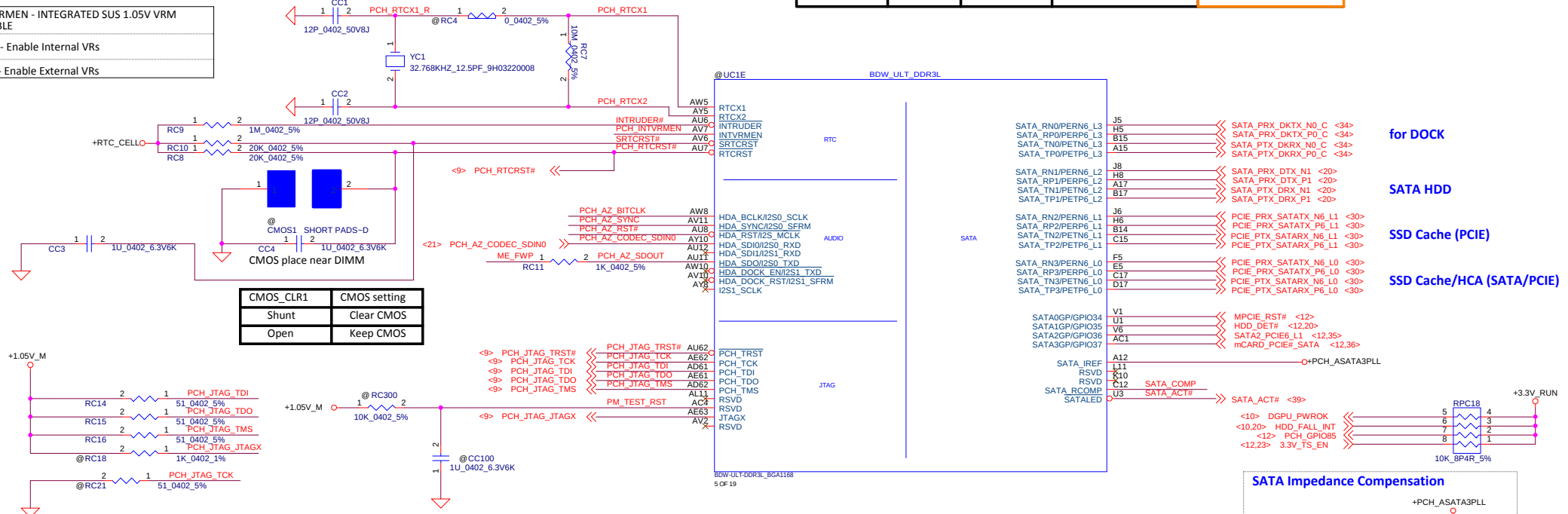
SATA0	SATA1	PCB	SATA2/PCIE6 L1	SATA3/PCIE6 L0	
E-Dock	HDD	H12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	HDD	H12 Entry	NA	NA	
E-Dock	HDD	H14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG	SATA2/PCIE6_L1 contact to WWAN SATA3/PCIE6 L0 contact to WLAN
E-Dock	HDD	H14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	HDD	H14D_En	NA	M2 3030 WIGIG	contact to WLAN
NA	HDD	H14U_En	NA	NA	
E-Dock	HDD	H15 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG	SATA2/PCIE6_L1 contact to WWAN SATA3/PCIE6 L0 contact to WLAN
E-Dock	HDD	H15 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	HDD	H15D_En	NA	M2 3030 WIGIG	contact to WLAN
NA	HDD	H15U_En	NA	Express card	contact to Express card

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.



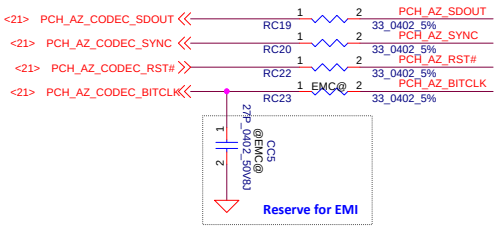
FLASH DESCRIPTOR SECURITY OVERRIDE	
LOW = ENABLE (DEFAULT)	-->Pin1 & Pin3 short
HIGH = DISABLE (ME can update)	-->Pin2 & Pin3 short

INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

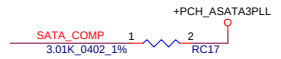


CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

HDA for Codec



SATA Impedance Compensation



CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

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Title: CPU (1/12)

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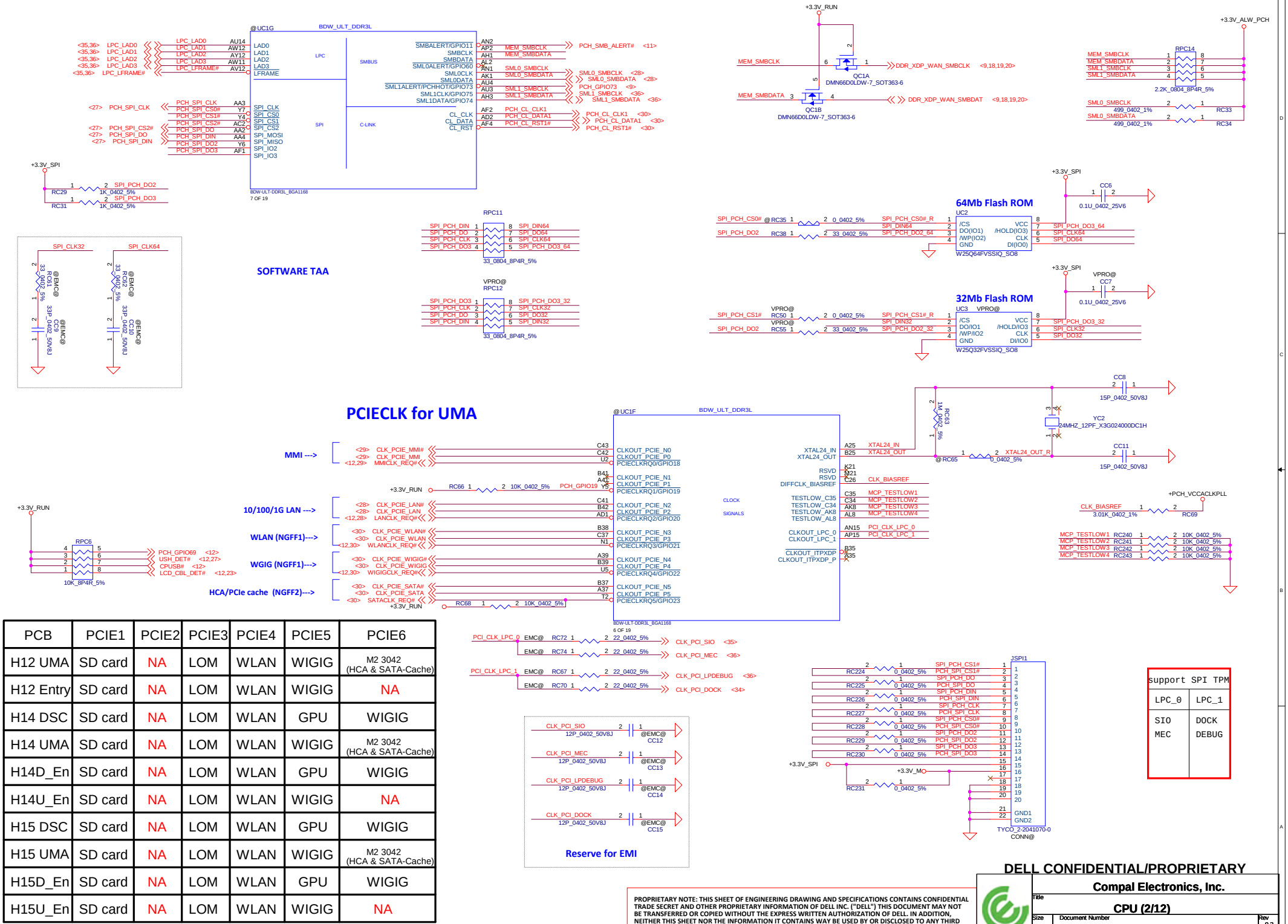

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	NA

support SPI TPM	
LPC_0	LPC_1
SIO	DOCK
MEC	DEBUG

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Title: CPU (2/12)

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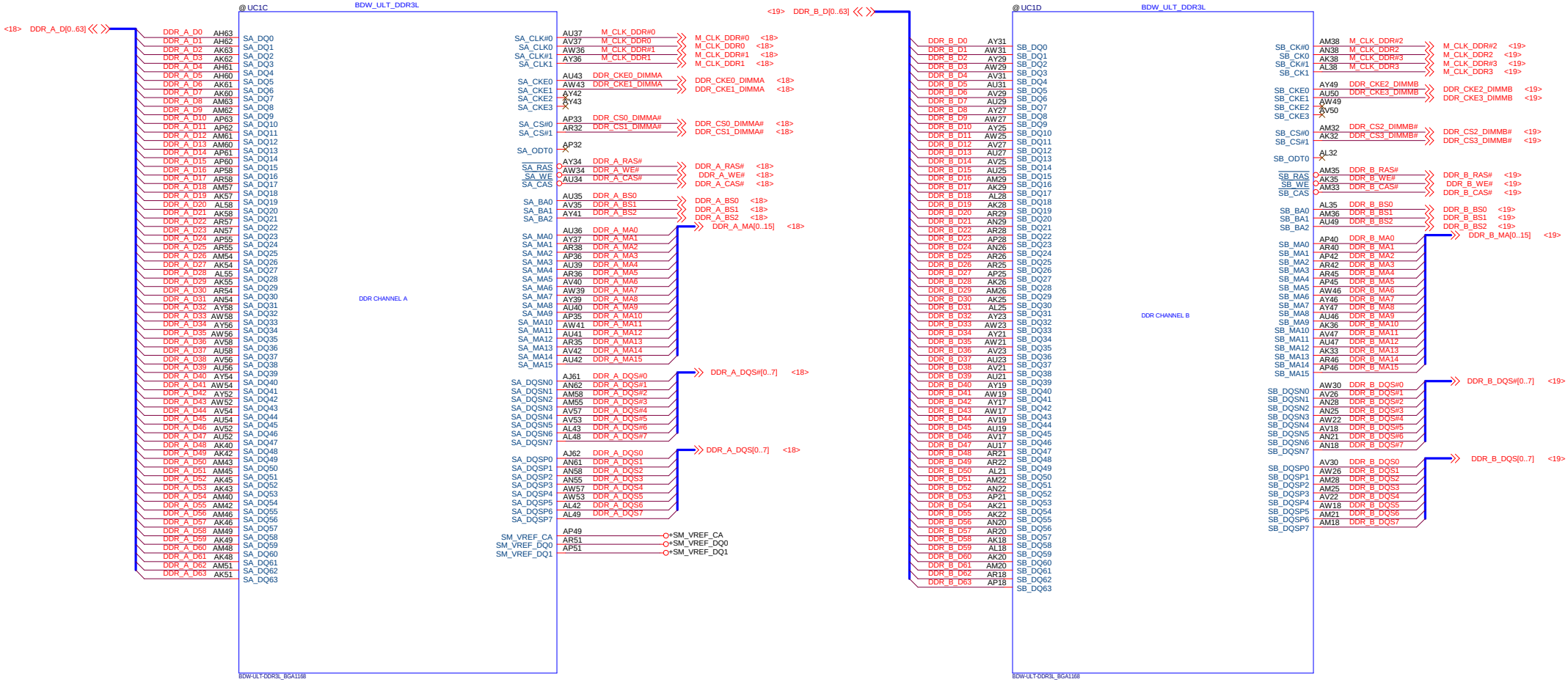

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Title: CPU (3/12)

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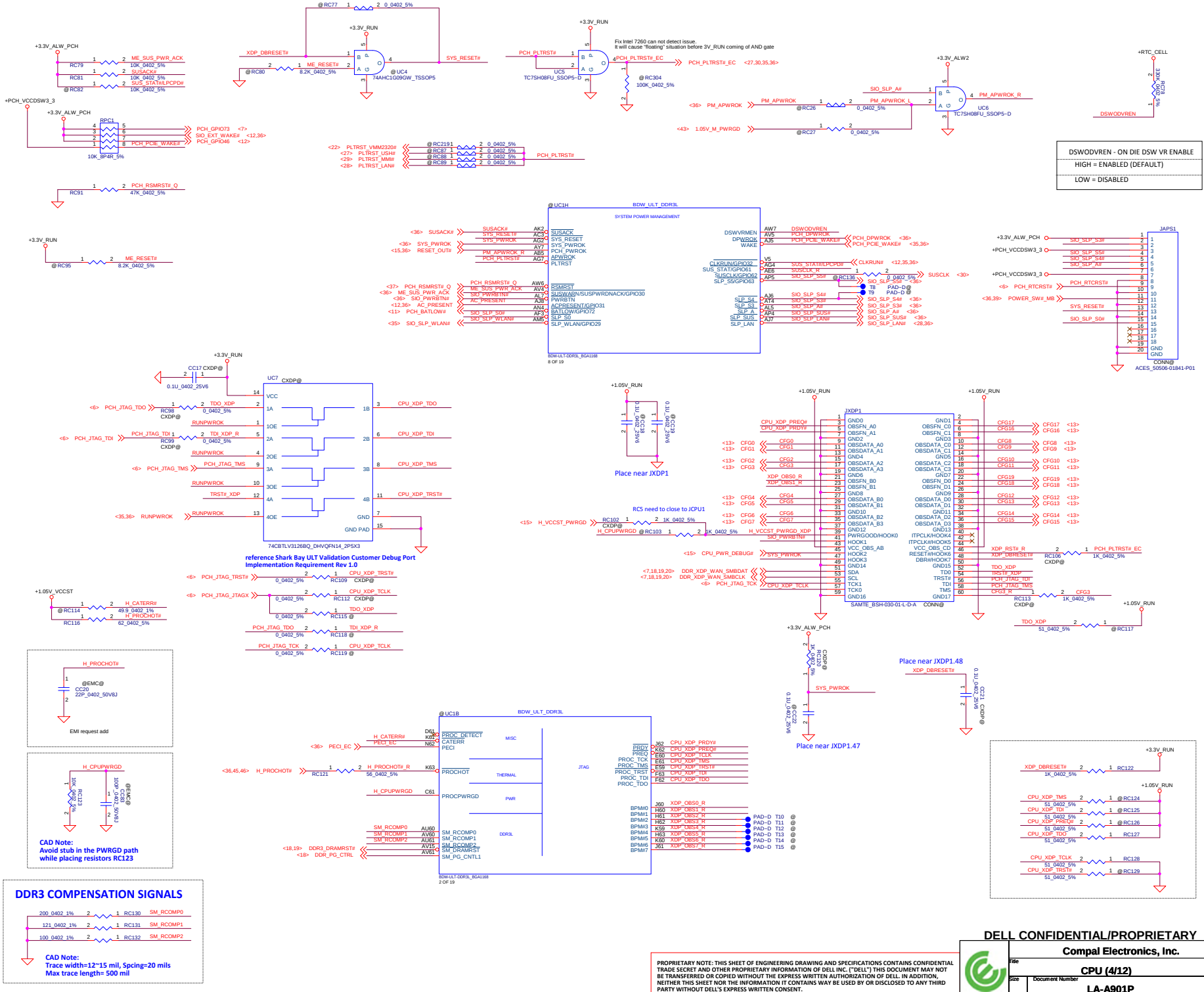

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Title: CPU (4/12)

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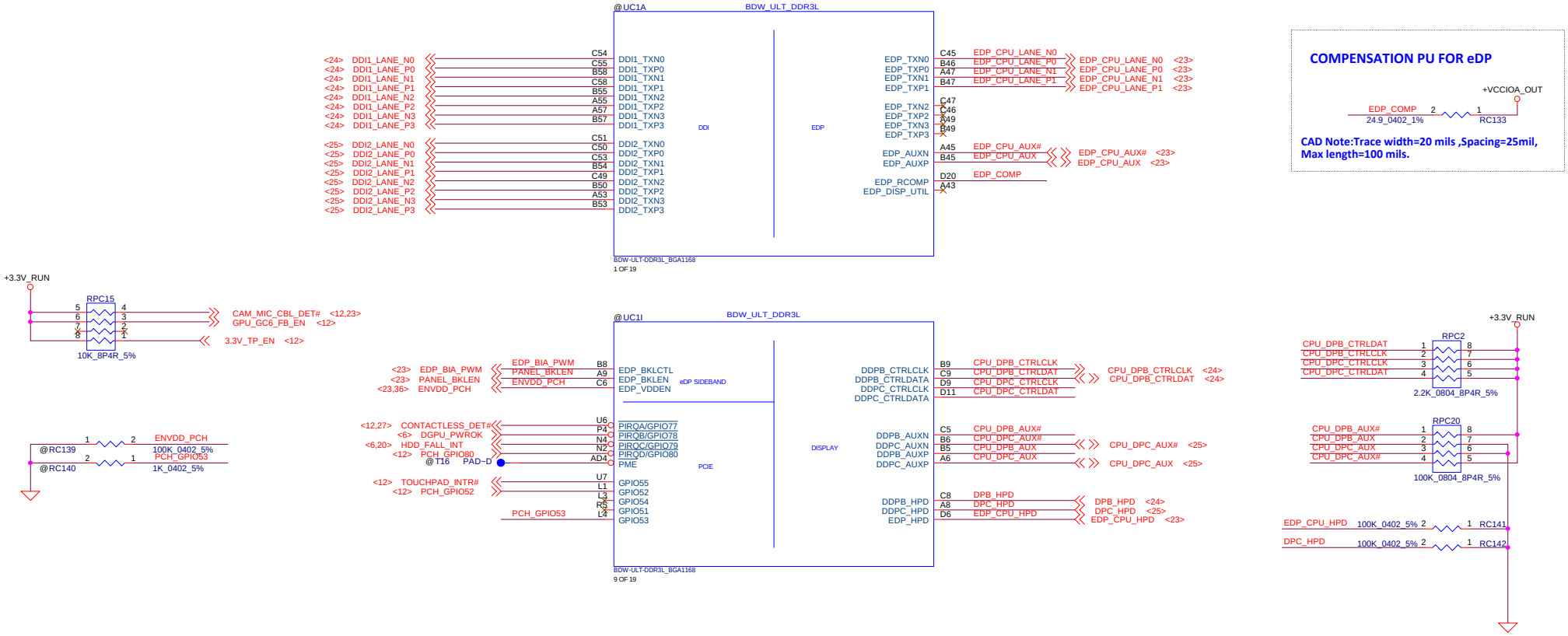

Compal Electronics, Inc.

Title: CPU (5/12)

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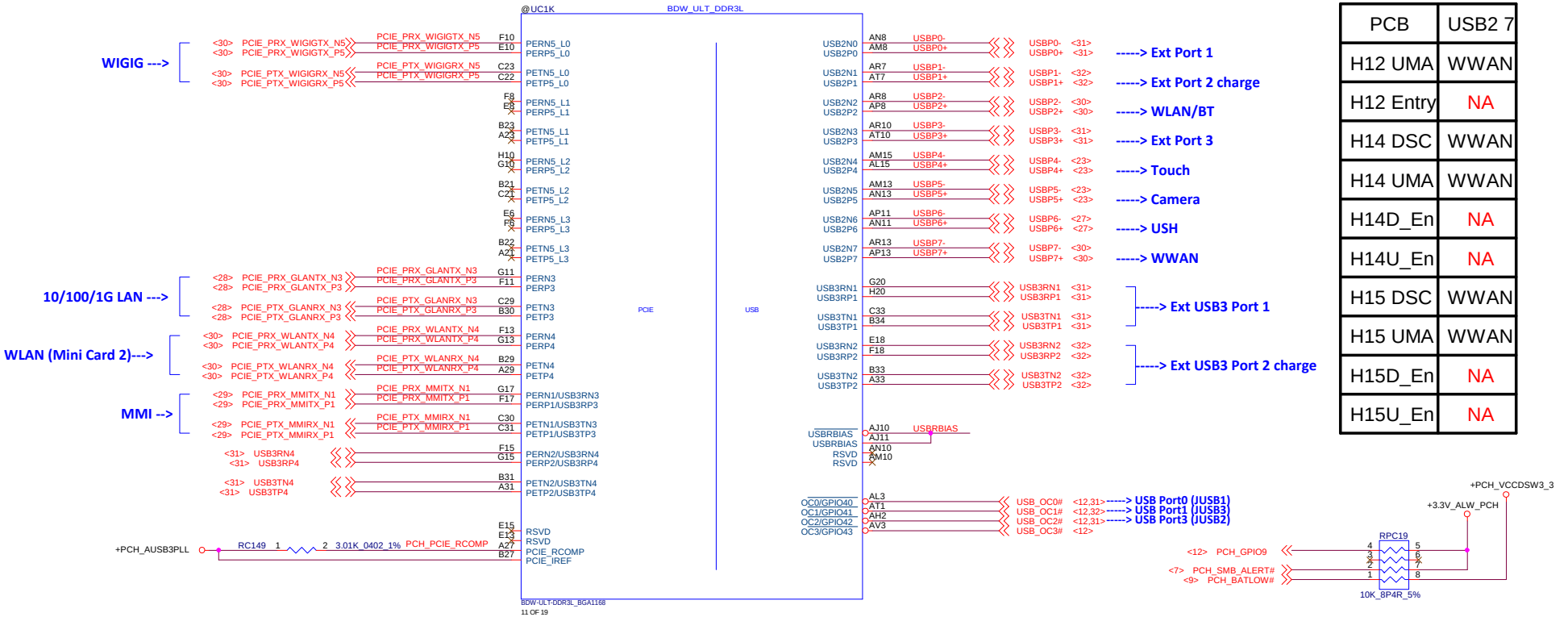
PCIE for UMA



PCB	USB2 7
H12 UMA	WWAN
H12 Entry	NA
H14 DSC	WWAN
H14 UMA	WWAN
H14D_En	NA
H14U_En	NA
H15 DSC	WWAN
H15 UMA	WWAN
H15D_En	NA
H15U_En	NA

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
H12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
H14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H14U_En	SD card	NA	LOM	WLAN	WIGIG	NA
H15 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
H15 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
H15D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
H15U_En	SD card	NA	LOM	WLAN	WIGIG	NA

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Title: CPU (6/12)

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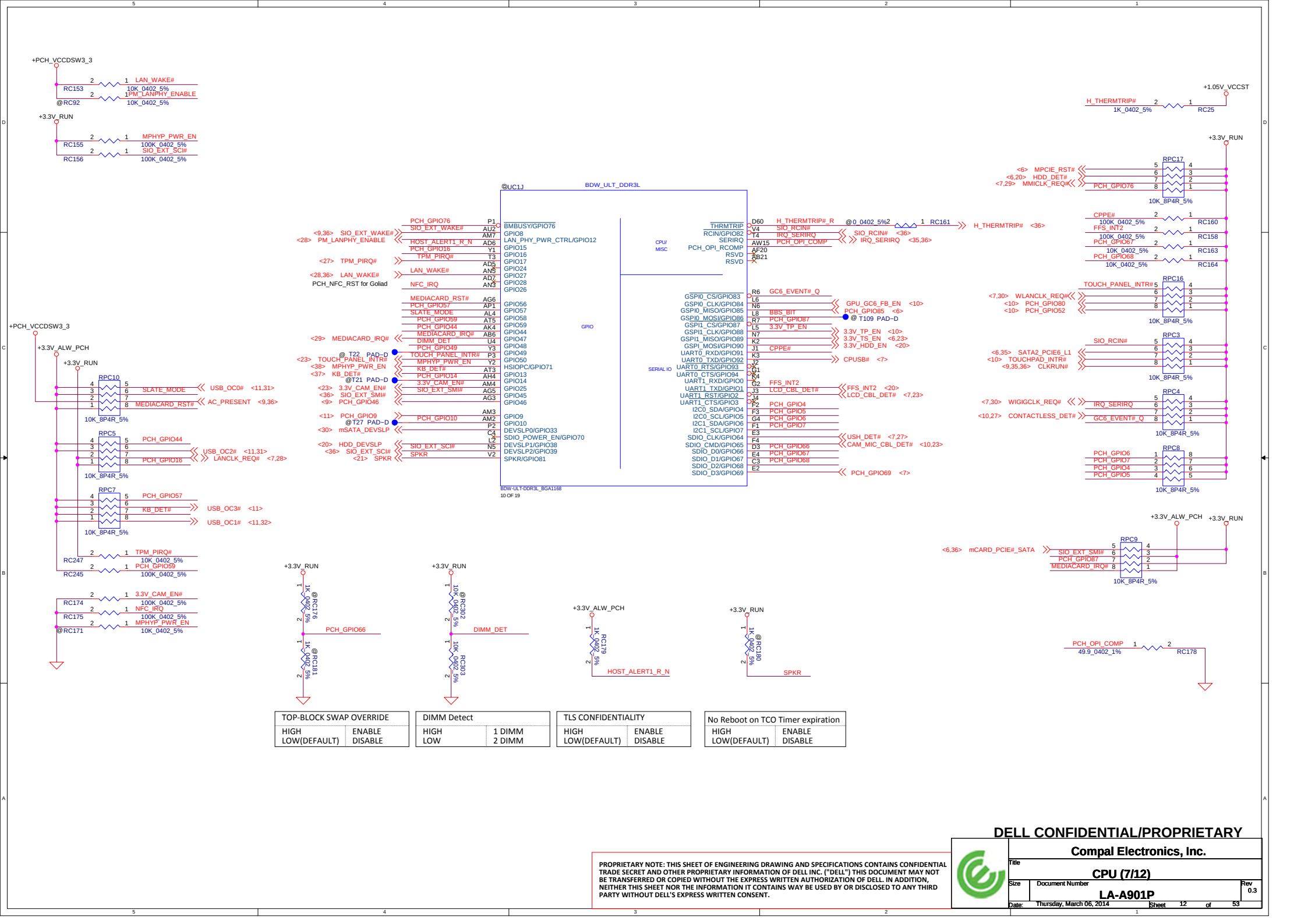

TOP-BLOCK SWAP OVERRIDE	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

No Reboot on TCO Timer expiration	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

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Title: CPU (7/12)

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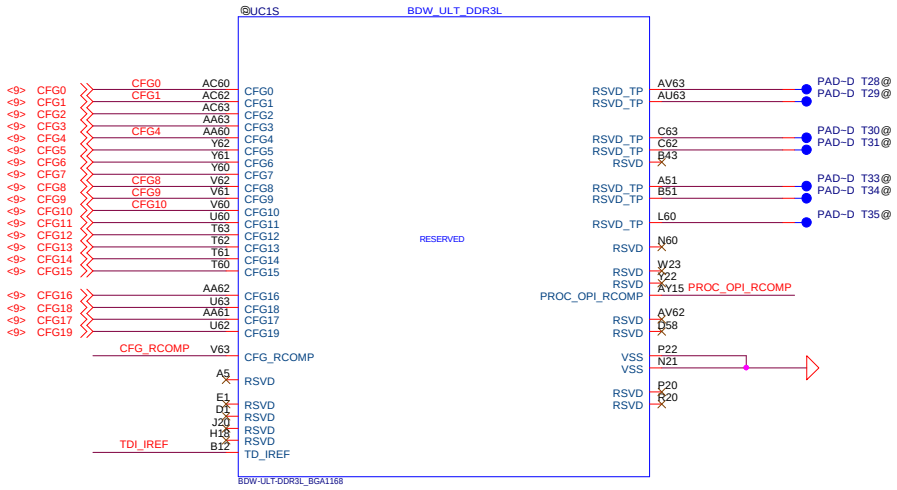
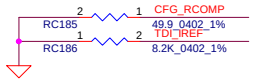
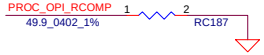
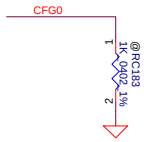
CFG STRAPS for CPU

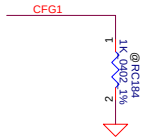




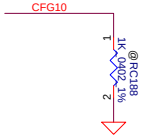


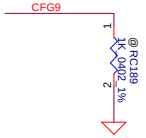


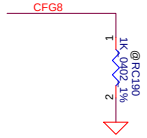
EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

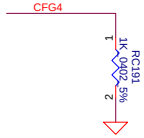


PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed









SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegardless of the locking of the unit

	Display Port Presence Strap
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Compal Electronics, Inc.

Title: CPU (8/12)

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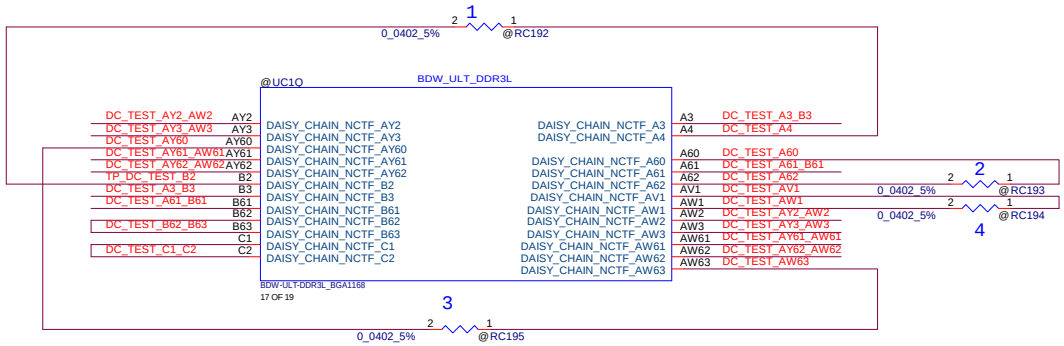
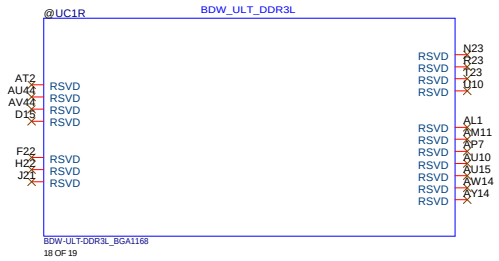


Package Daisy Chain:

1.B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4
2.A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60
3.AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
4.AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1



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Title: CPU (9/12)

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ESD Request

+1.05V_RUN
+VCCIO_OUT
@RC196
0_0603_5%

RESISTOR STUFFING OPTIONS ARE PROVIDED FOR TESTING PURPOSES

+1.05V_RUN
RC197 150_0402_5%
CPU_PWR_DEBUG#
10K_0402_5% @RC198

+1.05V_VCCST
10K_0402_5% @RC199
H_VR_EN
1.5K_0402_5%
RC201
H_VR_READY

+1.05V_VCCST
UC8
NC
VCC
A
GND
Y
<9,36> RESET_OUT#
+3.3V_ALW
@CC35
0.1U_0402_25V6
H_VCCST_PWRGD
1K_0402_5% RC202
74AUP1G07GW_TSSOP5

+VCC_CORE
+1.35V_MEM
@EMC@CC23
22U_0603_6.3V6M

+1.05V_RUN
+VCC_CORE
@EMC@CC79
22U_0603_6.3V6M
@EMC@CC84
22U_0603_6.3V6M

+1.05V_RUN
+3.3V_RUN
@EMC@CC85
22U_0603_6.3V6M

H_VCCST_PWRGD
@EMC@
CC24
100P_0402_50V8J

+1.35V_MEM
VDDQ DECOUPLING
2.2U_0402_6.3V6M @CC25
2.2U_0402_6.3V6M @CC26
2.2U_0402_6.3V6M CC27
2.2U_0402_6.3V6M CC28
10U_0603_6.3V6M CC29
10U_0603_6.3V6M @CC30
10U_0603_6.3V6M CC31
10U_0603_6.3V6M CC32
10U_0603_6.3V6M @CC33
10U_0603_6.3V6M CC34

SVID ALERT

+1.05V_VCCST
75_0402_1% RC204
CAD Note: Place the PU resistors close to CPU RC204 close to CPU 300 - 1500mils
<45> VIDALERT_N
43_0402_5%
H_CPU_SVIDALRT#
RC207

SVID DATA

+1.05V_VCCST
110_0402_1% RC208
CAD Note: Place the PU resistors close to CPU RC208close to CPU 300 - 1500mils
<45> VIDSOUT
VIDSOUT

VCC_SENSE

+VCC_CORE
100_0402_1% RC209
<45> VCCSENSE
VCCSENSE
CAD Note: RC209 SHOULD BE PLACED CLOSE TO CPU

@UC1L
BDW_ULT_DDR3L
+1.35V_MEM
+VCC_CORE
+VCCIO_OUT
+VCCIOA_OUT
VCCSENSE
H_CPU_SVIDALRT#
<45> VIDSCLK
<9> H_VCCST_PWRGD
<45> H_VR_EN
<45> H_VR_READY
<9> CPU_PWR_DEBUG#
@T74 PAD-D
@T75 PAD-D
@T76 PAD-D
@T77 PAD-D
+1.05V_VCCST
+VCC_CORE
HSW ULT POWER
BDW-ULT-DDR3L_BGA1168
12 OF 19

+1.05V_RUN
PJP23
PAD-OPEN1x1m
+1.05V_VCCST
CC36 22U_0603_6.3V6M
@CC37 1U_0402_6.3V6K

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Title: CPU (10/12)

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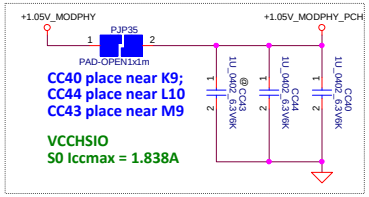

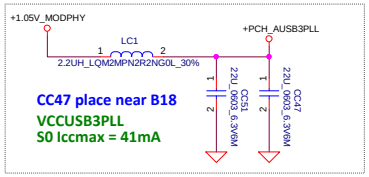

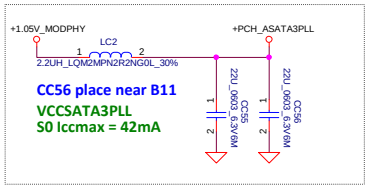

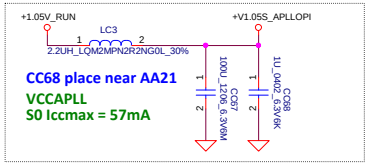

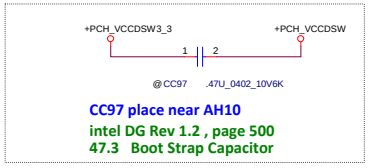

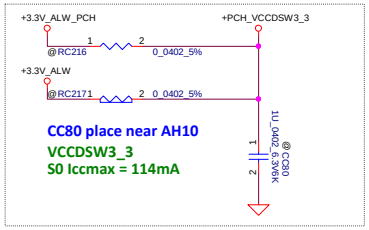

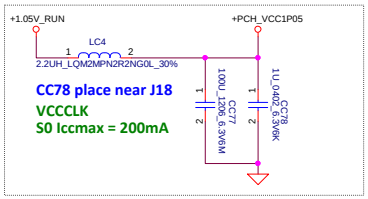

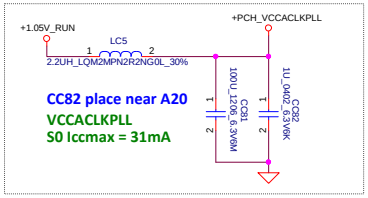

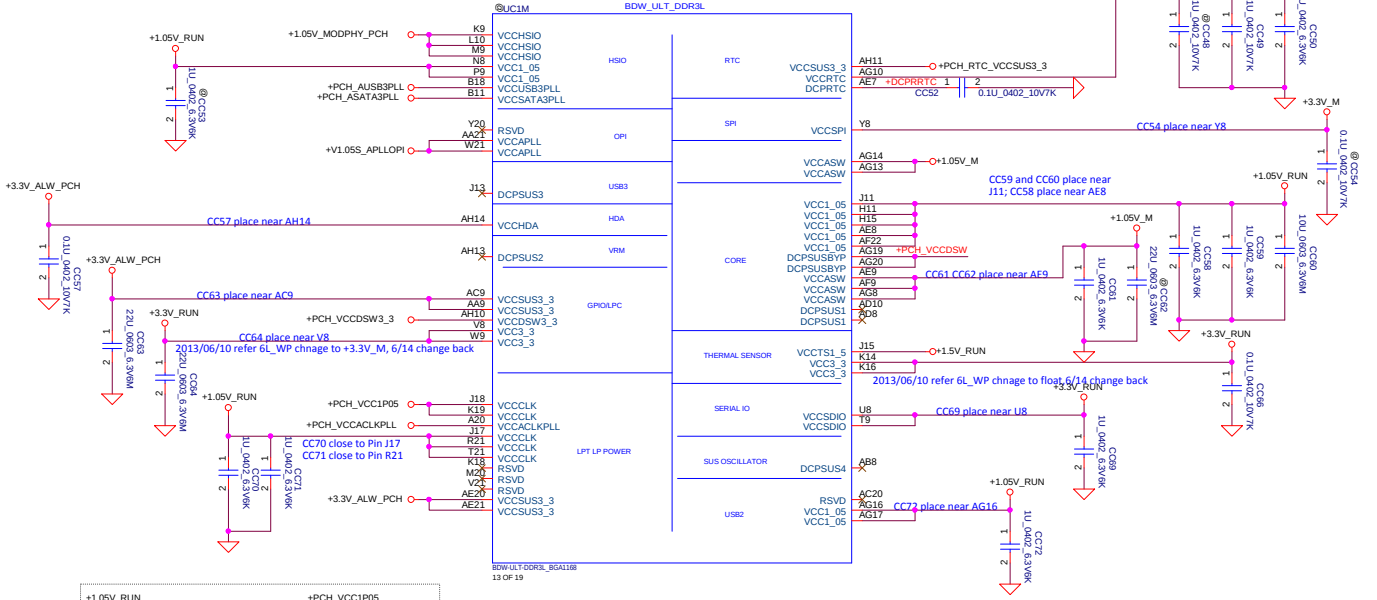

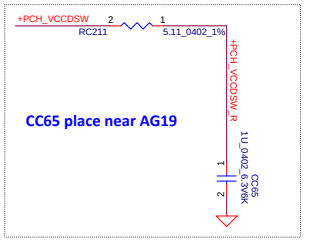

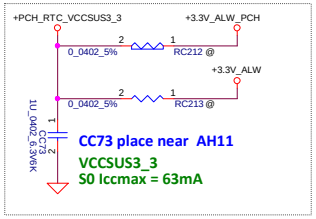

Voltage Rail	Voltage (V)	S0 Iccmax Current (A)[3]	Sx Iccmax Current (A)[3]	Deep Sx Iccmax (A)[3]	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.632	0	0	
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.838	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCASW	1.05	0.658	0	0	0
VCCSPI	3.3	0.018	0	0	0
VCCHDA	3.3	0.011	<1 mA	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCCSUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.005	0	0
DcpSus1[4]	1.05	0.109	0.014	0	0
DcpSus2[4]	1.05	0.025	0.001	0	0
DcpSus3[4]	1.05	0.010	0.003	0	0
DcpSus4[4]	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	6 µA See notes 1, 2

Reminder below power rail need isolation for layout refer attach file for more detail that from Intel review feedback.

Power Rail Isolation

Voltage Supply	Interface: (power rail isolation required)	PCH Pins sharing power rail
V1.05S	Core	J11, H11, H15, AE8, AF22
	OPI	AA21, W21
	HSIO	K9, L10, N8, P9, B18, B11, M9
	USB2	AG16, AG17
	CLKPLL	A20
	CLK(A)	R21, T21
	CLK(B)	J18, K19
	CLK(C)	J17
V3.3A	GPIO	AC9, AA9, AE20, AE21
	RTC	AH11
	HDA	AH14
V3.3S	GPIO	V8, W9
	SDIO	U8, T9
	Thermal Sensor	K14, K16

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Title: CPU (11/12)

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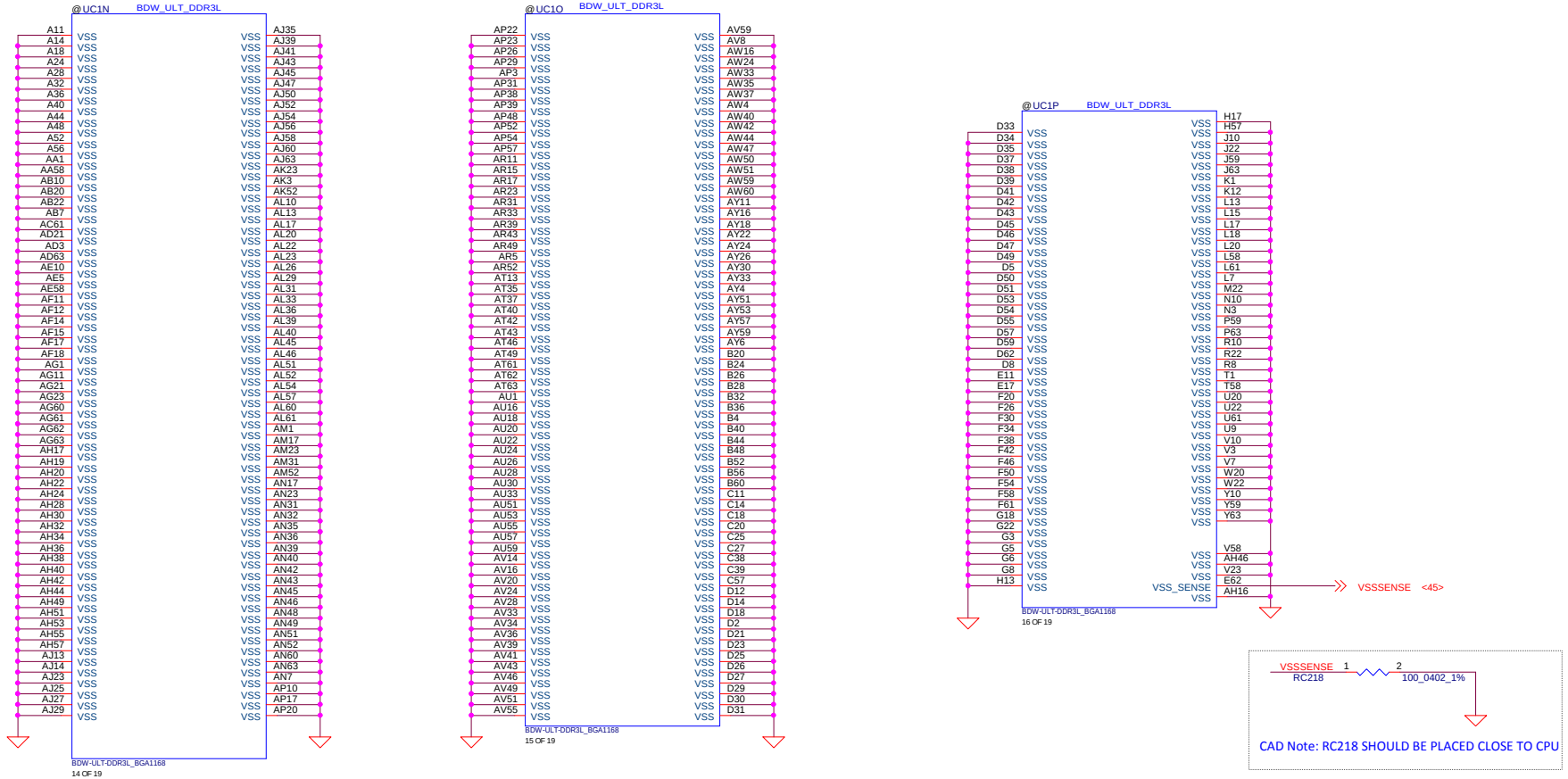

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Title: CPU (12/12)

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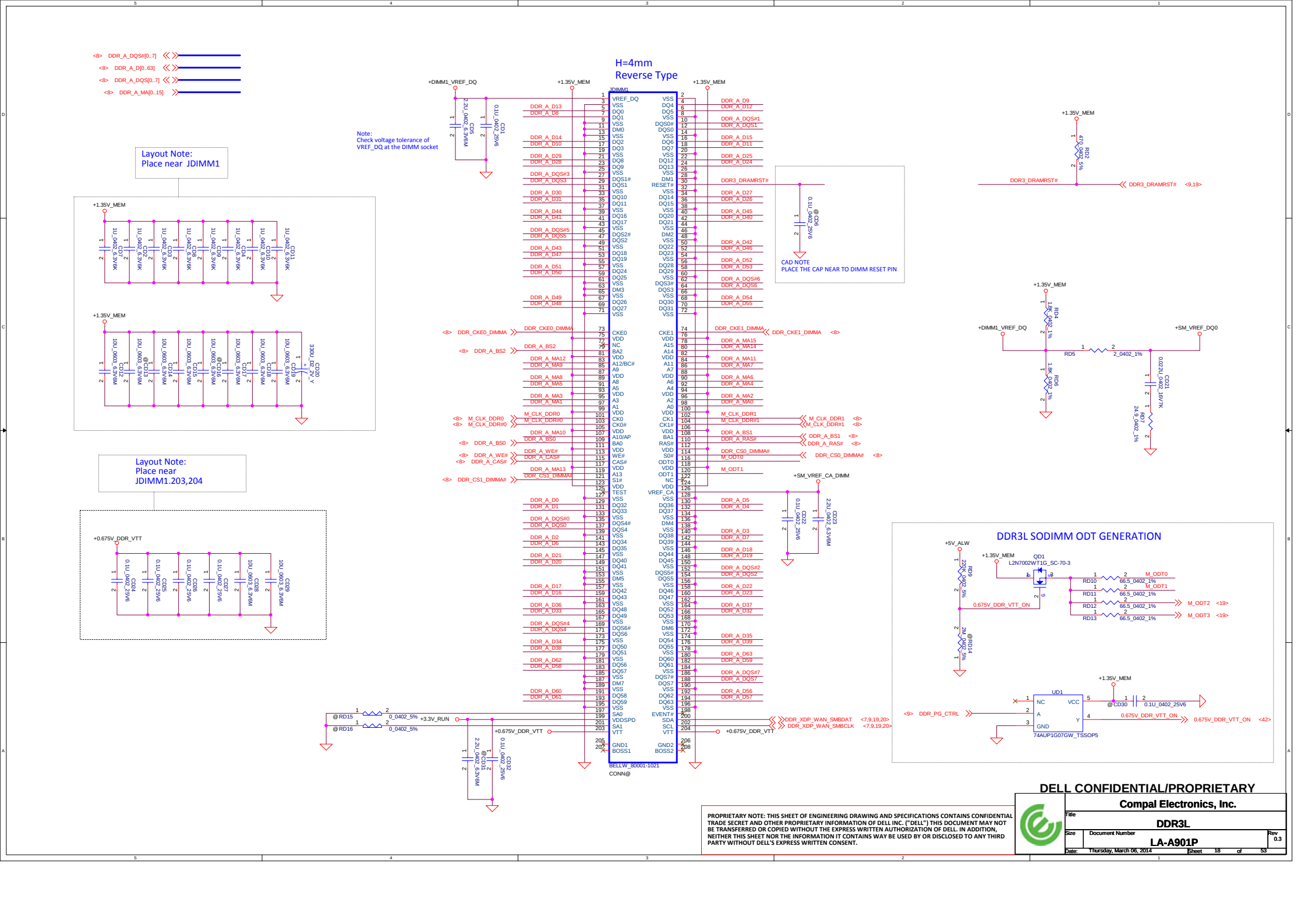
H=4mm
Reverse Type
JDIMM1
BELLW_80001-1021
CONN@
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket
Layout Note:
Place near JDIMM1
Layout Note:
Place near
JDIMM1.203,204
CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN
DDR3L SODIMM ODT GENERATION
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DDR3L
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H=4mm
Reverse Type

<8> DDR_B_DQS#[0..7]
<8> DDR_B_D[0..63]
<8> DDR_B_DQS[0..7]
<8> DDR_B_MA[0..15]

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMM2

Layout Note:
Place near
JDIMM2.203,204

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

JDIMM2
BELLW_80001-1021
CONN@

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Title: DDR3L

Size: | Document Number: LA-A901P | Rev: 0.3

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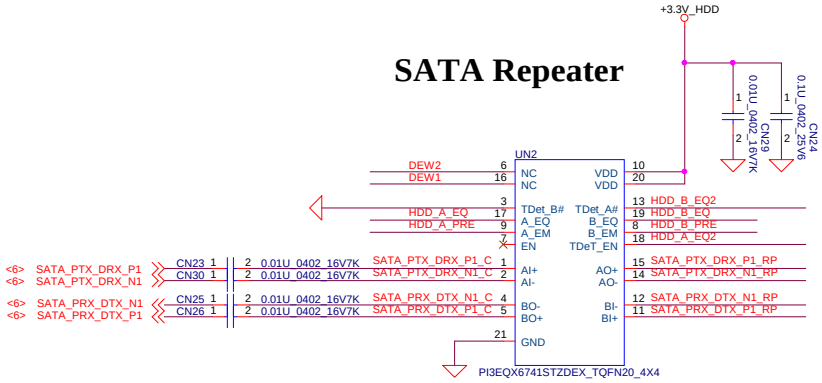
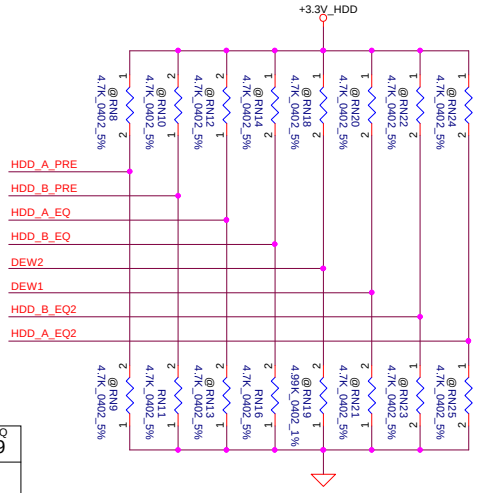
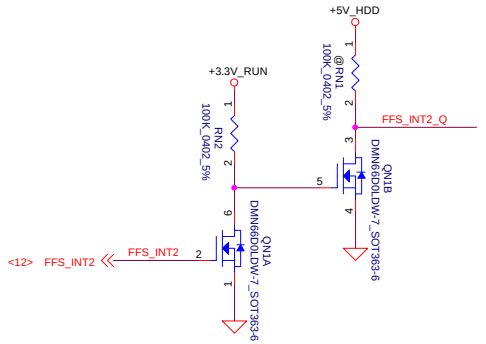
SATA Repeater



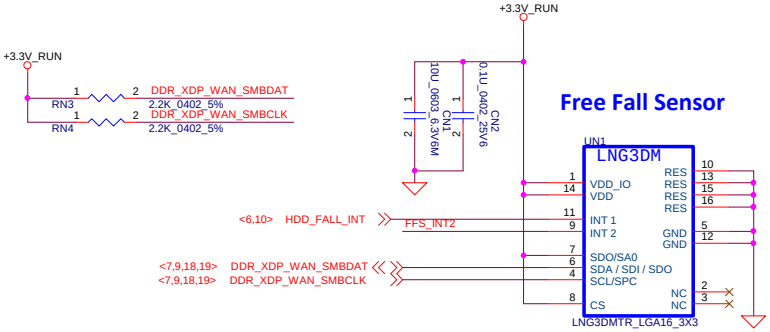


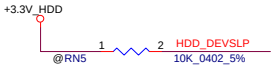


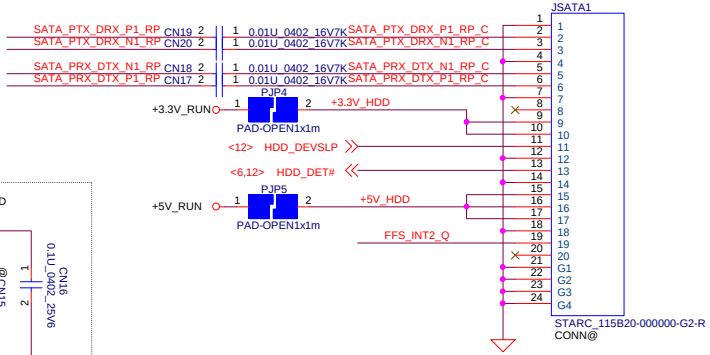
	DEW2 PIN6	HDD_B_PRE PIN8	HDD_A_PRE PIN9	HDD_B_EQ2 PIN13	DEW1 PIN16	HDD_A_EQ PIN17	HDD_A_EQ2 PIN18	HDD_B_EQ PIN19
Pericom PI3EQX6741ST	NC	PD (RN11)	NC (IPU)	PD (RN25)	NC	NC	PH (RN22)	PD (RN16)
TI SN75LVCP601	NC (IPU)	PD (RN11)	PD (RN9)	PD (RN25)	NC (IPU)	PD (RN13)	PD (RN23)	NC
Parade PS8527C	PD (RN19)	PD (RN11)	PH (RN8)	PD (RN25)	NC	NC	PH (RN22)	NC

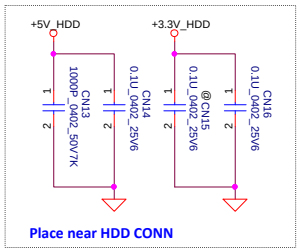
			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0	3dB	3dB	0	0dB	0dB
		NC	6dB	6dB	NC		
		1	9dB	9dB	1	1.5dB	1.5dB
2nd	TI	0	7dB	7dB	0	0dB	0dB
		NC	0dB	0dB	NC	-6dB	-6dB
		1	14dB	14dB	1	-3dB	-3dB
3rd	Parade	EQ2 EQ1	A_EQ	B_EQ		A_EM	B_EM
		(M = VDD/2)					
		0 M	2.4dB	2.4dB			
		0 0	7.4dB	7.4dB			
		0 1	14.4dB	14.4dB	0	0dB	0dB
		M M	12.2dB	12.2dB	M	-3.5dB	-3.5dB
		M 0	9.4dB	9.4dB	1	-1.5dB	-1.5dB
		M 1	13.3dB	13.3dB			
		1 M	6.2dB	6.2dB			
		1 0	11.2dB	11.2dB			
		1 1	5dB	5dB			

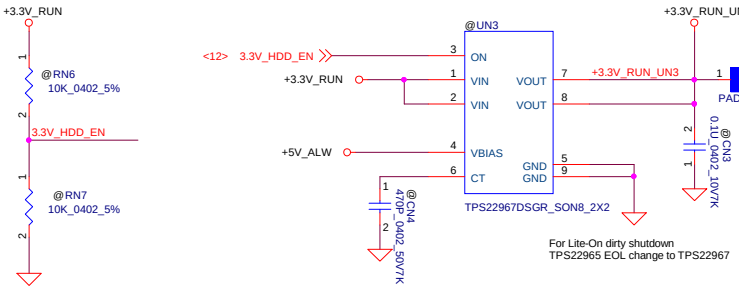
* red color is current setting











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Title: HDD CONN

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1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

CONN@ JSPK1 — ACES_50279-0040N-001

Close to UA1

Close to UA1 pin6

Verb table configures as 1 JD mode with internal 47K pull high to save external rBOM.

Place closely to Pin 13.

Add for solve pop noise and detect issue

Place closely to Pin 14 for DOCK only

Digital Mic

BCLK: Audio serial data bus bit clock input/output
LRCK: Audio serial data bus word clock input/output

Place RA9 close to codec

Place RA32 close to codec

Place CA29 close to Codec

place at AGND and DGND plane

Realtek feedback
Prevent the Noise from Combo Jack while system entry into S3 / S4 /S5

HP-Out-Right
HP-Out-Left
Nokia-MIC
iPhone-MIC

Global Headset
Universal Jack

Normal Open

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Title	Codec _ALC3226
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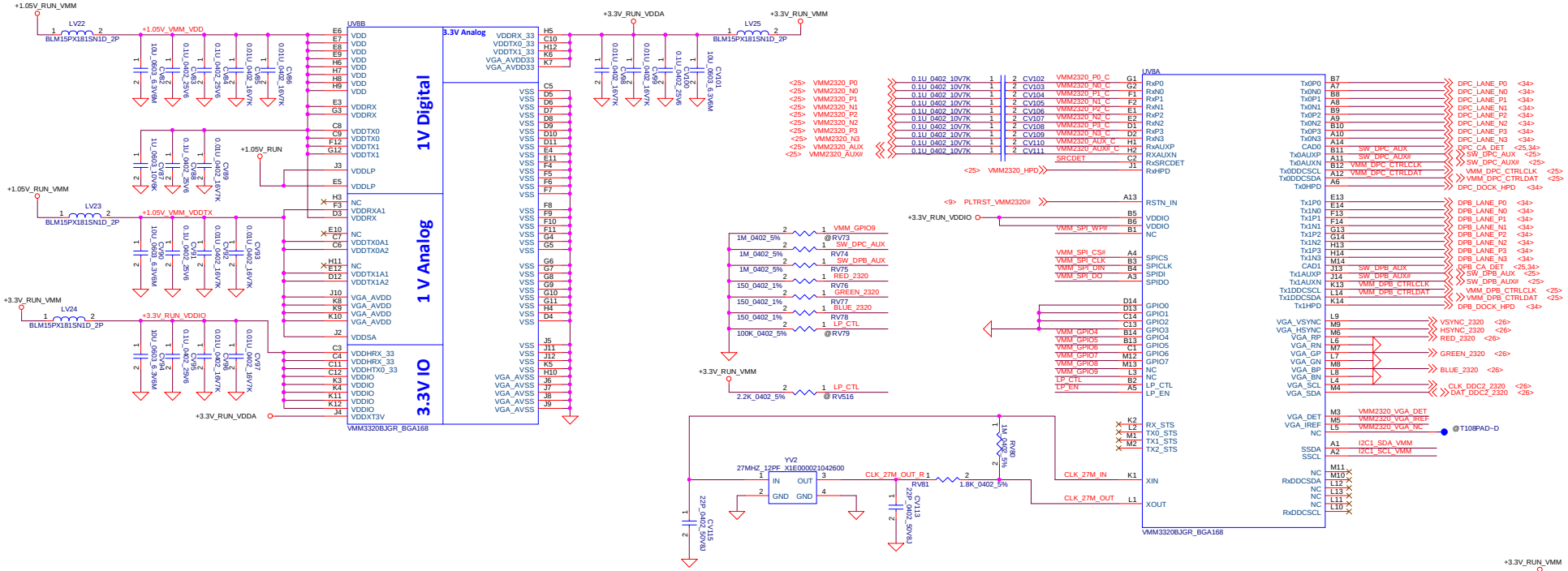
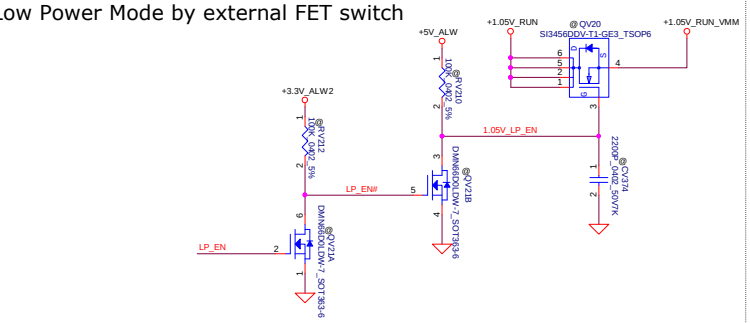
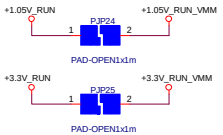


	TYP. Current (mA)			Max Current (mA)			TYP.Watt	MAX.Watt
Cond./Voltage	1.0V	1.0 LP	3.3	1.13	1.13 LP	3.63	1.0/3.3	1.13/3.63
ROOM (40)	711	4.42	72	786	5.29	74	0.95302	1.1627777

Low Power Mode by external FET switch

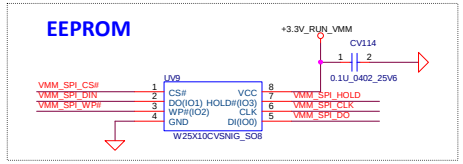


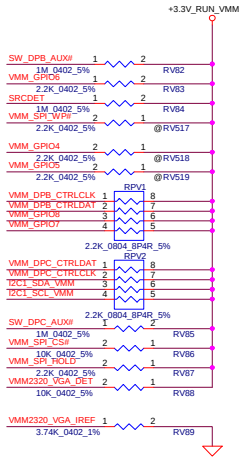
VMM2320 Operation power consumption for 1.0V=1.464A (Max)



PRODUCT SUMMARY (SI3456DDV)

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[d]	Q_g (Typ.)
30	0.040 at V_{GS} = 10 V	6.3	2.8 nC
	0.050 at V_{GS} = 4.5 V	5.7	





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Title: DP 1.2 MST HUB

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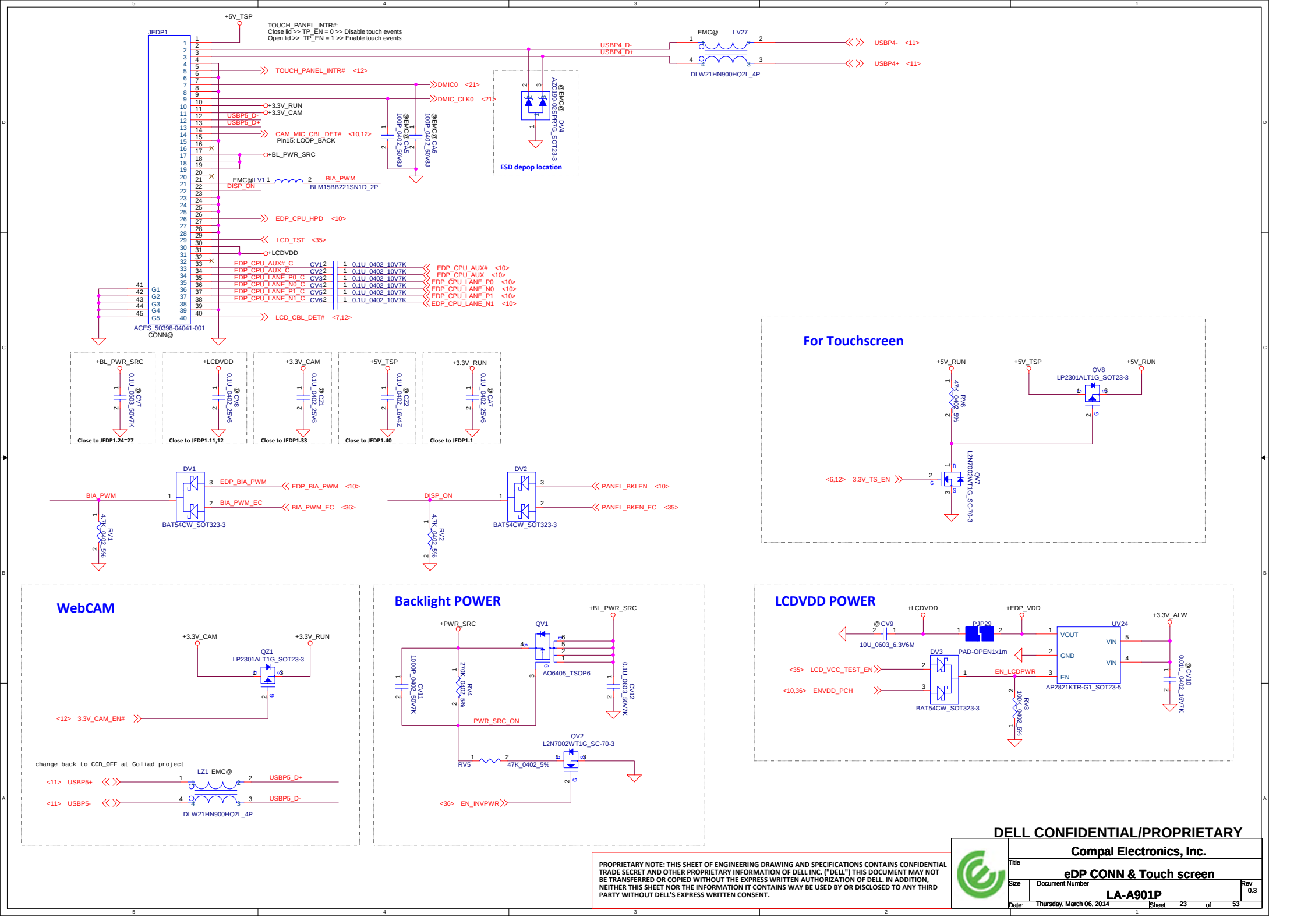

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Title	eDP CONN & Touch screen
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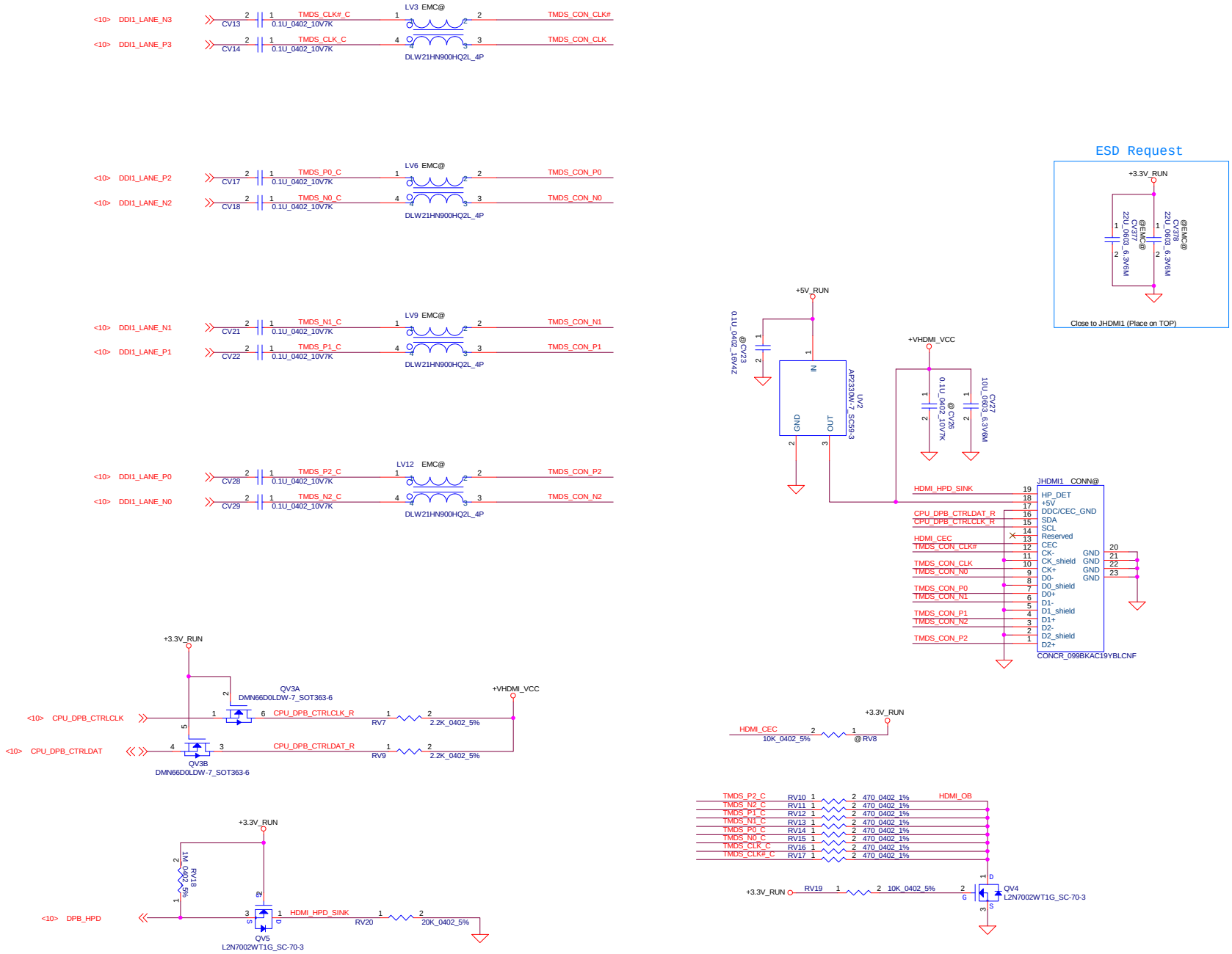

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Title: HDMI CONN

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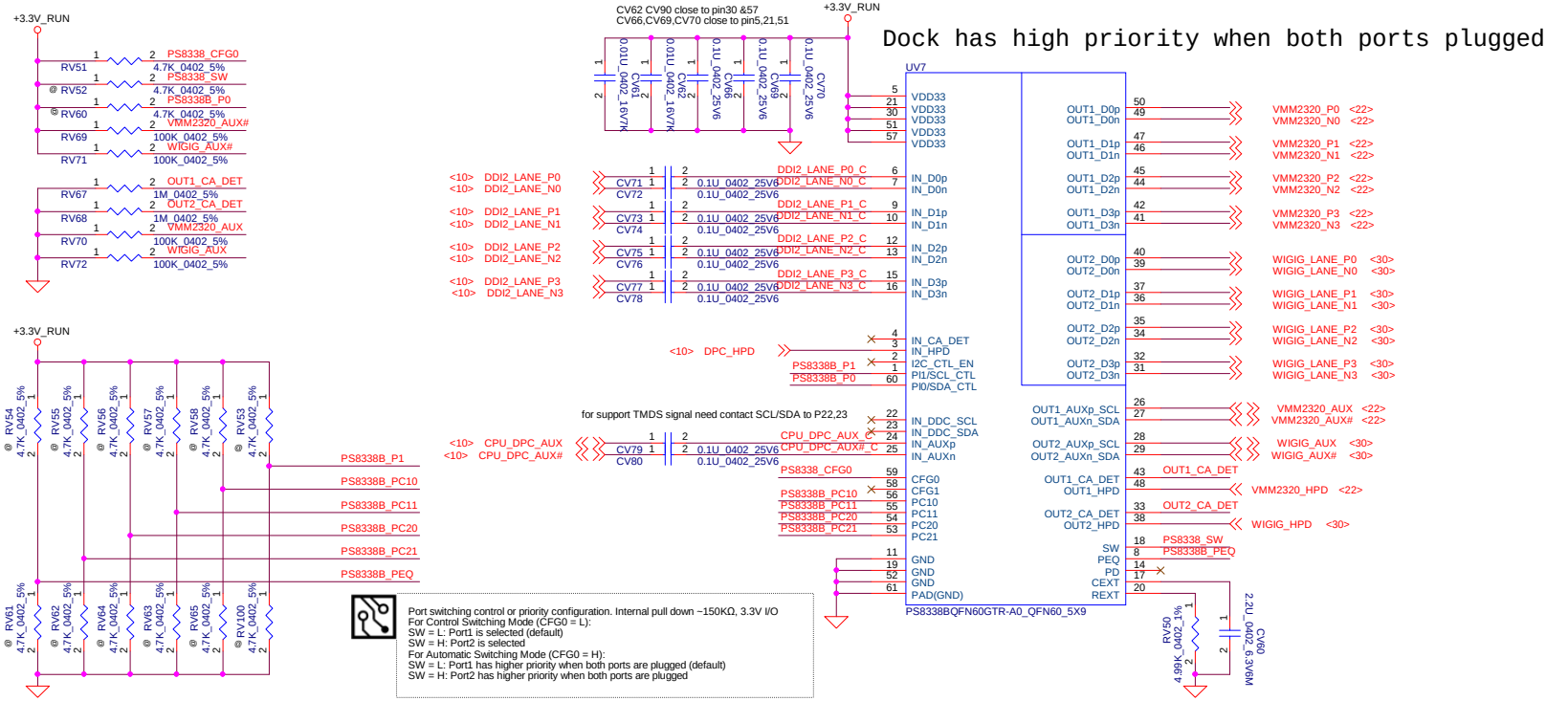
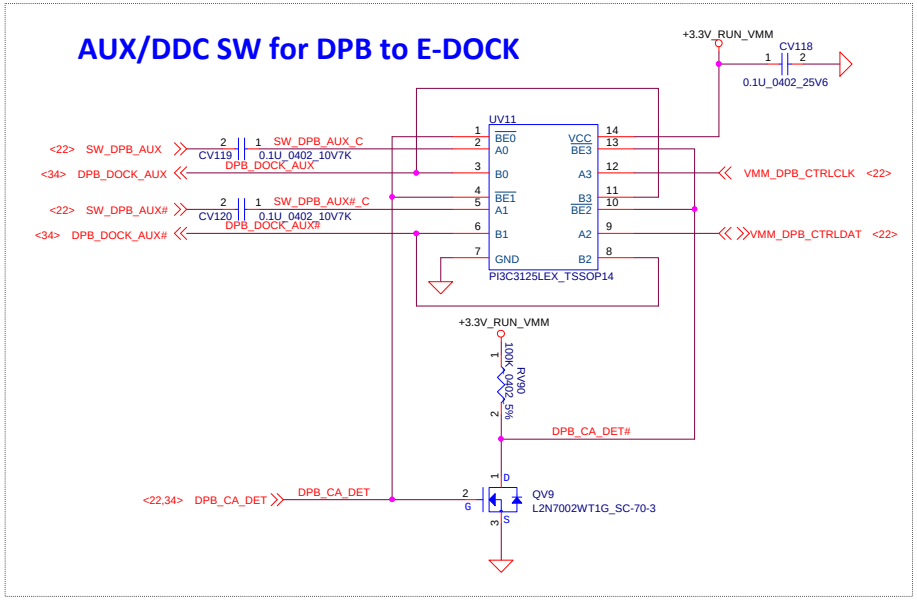
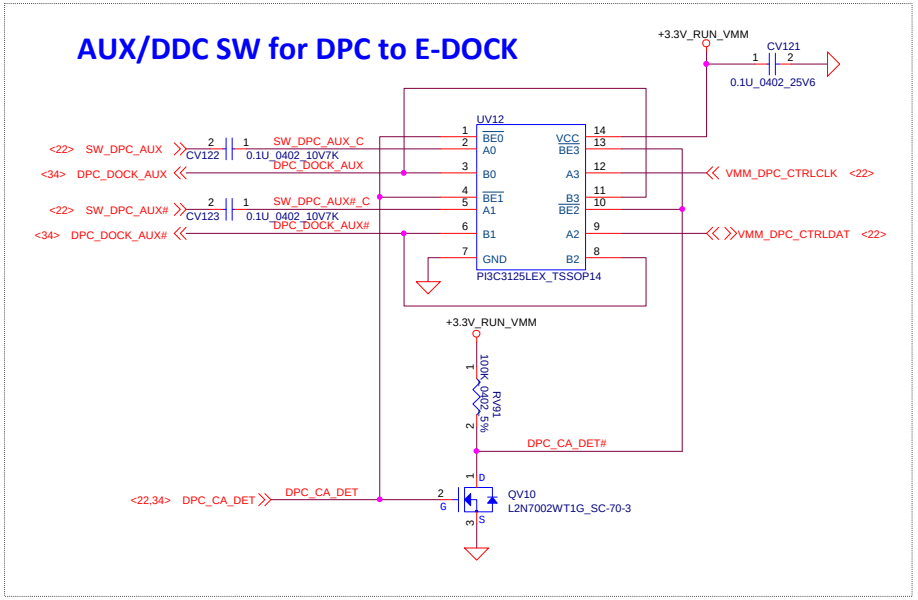
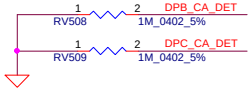
PCB	DP SWITCH
H12 UMA	PS8338+PS8339
H12 Entry	PS8339
H14 DSC	PS8338
H14 UMA	PS8338
H14D_En	PS8338
H14U_En	PS8338
H15 DSC	PS8338
H15 UMA	PS8338
H15D_En	PS8338
H15U_En	PS8338









	DP	HDMI
DPB_CA_DET	0	1
DPC_CA_DET	0	1

Compal Electronics, Inc.

Title: DP SW

Size | Document Number: LA-A901P | Rev: 0.3

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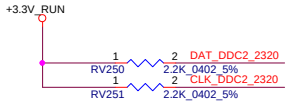
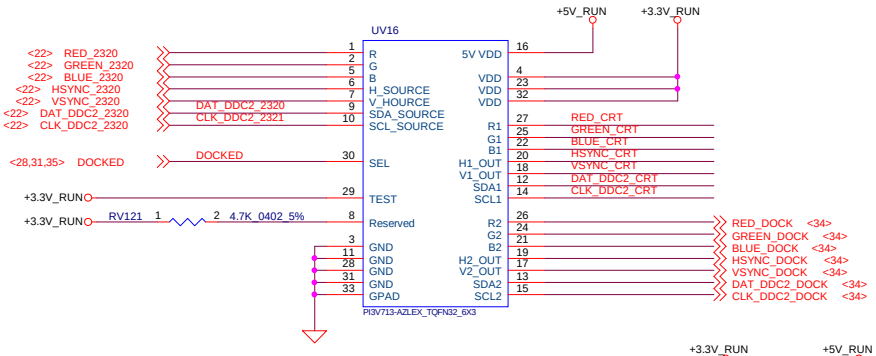
VGA SW for MB/DOCK

VGA SW

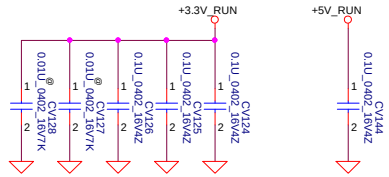
PCB	VGA SWITCH
H12 UMA	NA
H12 Entry	NA
H14 DSC	PI3V713
H14 UMA	PI3V713
H14D_En	NA
H14U_En	NA
H15 DSC	PI3V713
H15 UMA	PI3V713
H15D_En	NA
H15U_En	NA

source from VMM2320

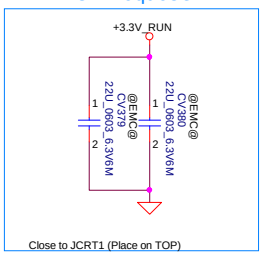


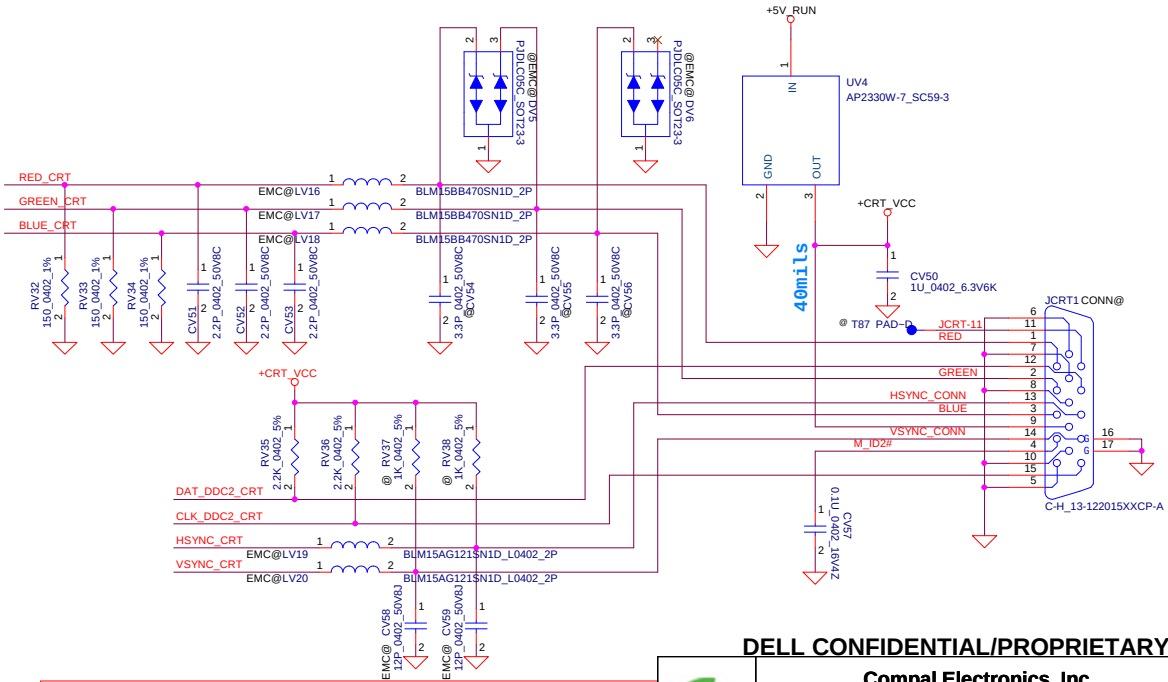


SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR



ESD Request





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Title: VGA SW & VGA Conn

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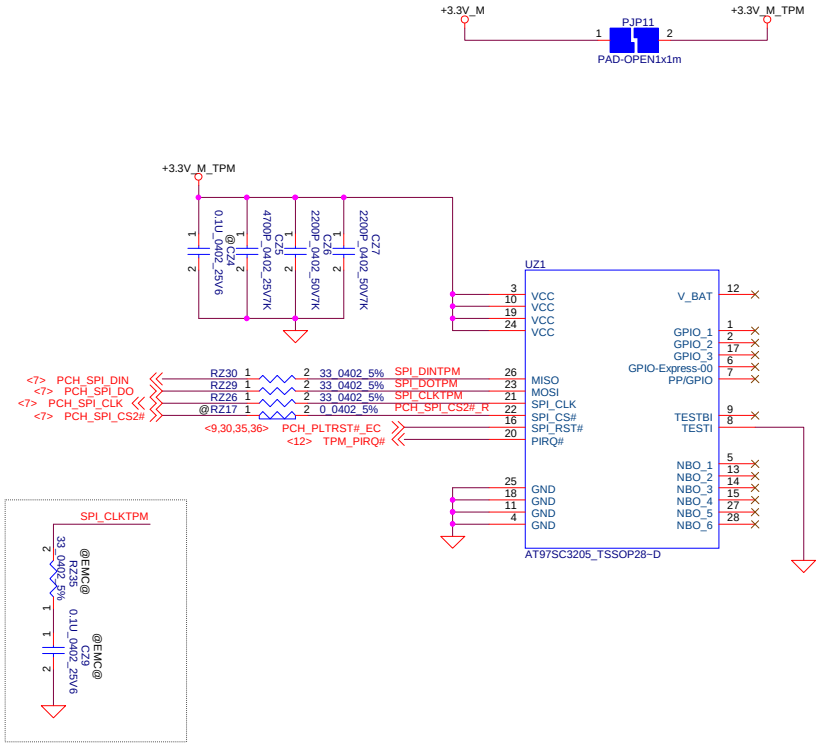

Compal Electronics, Inc.

Title: USH & TPM

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LAN ANALOG SWITCH

DOCKED	1: TO DOCK
	0: TO RJ45

PI3L720ZHEX_TQFN42_9X3P5

RJ45 LOM circuit

+3.3V_LAN:20mils

SANTA_130456-511

Layout Notice : Place bead as close UL4 as possible

Note: +1.0V_LAN will work at 0.95V to 1.15V

Place CL3, CL4 and LL1 close to UL1

SMBus Device Address 0xC8

WGI218LM-QQ89-B0_QFN48_6X6~D

APE8990GN3B_SON14_2X3

MHPC_NS692417

GND CHASSIS

use 40mil trace if necessary

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Compal Electronics, Inc.		
Title: LAN		
Size	Document Number: LA-A901P	Rev: 0.3
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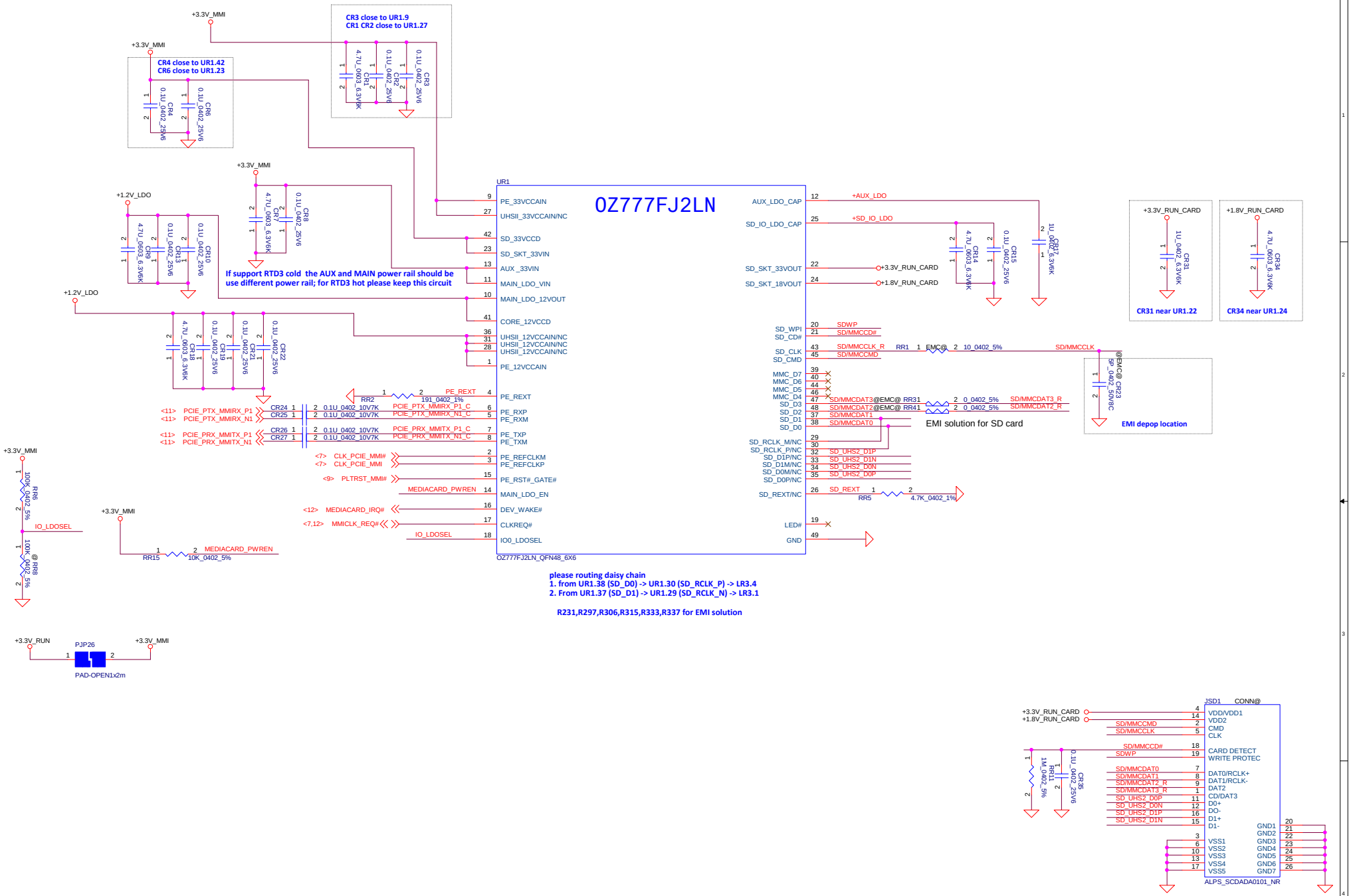

Compal Electronics, Inc.

Title: Card Reader

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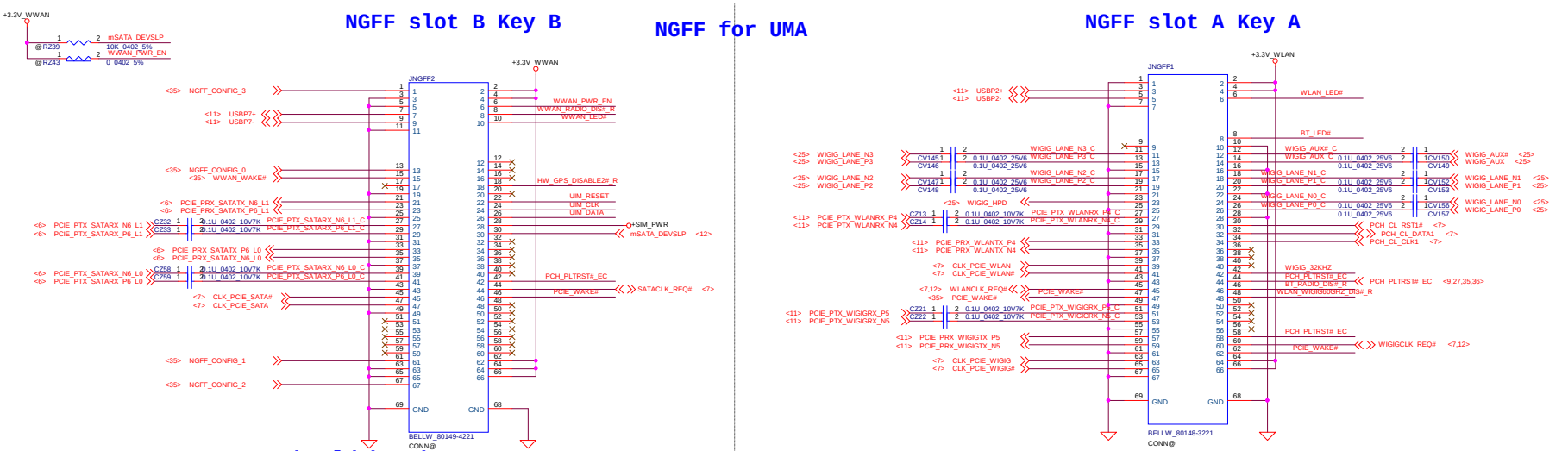
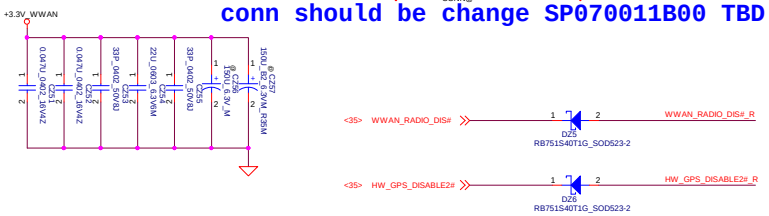
NGFF slot B Key B

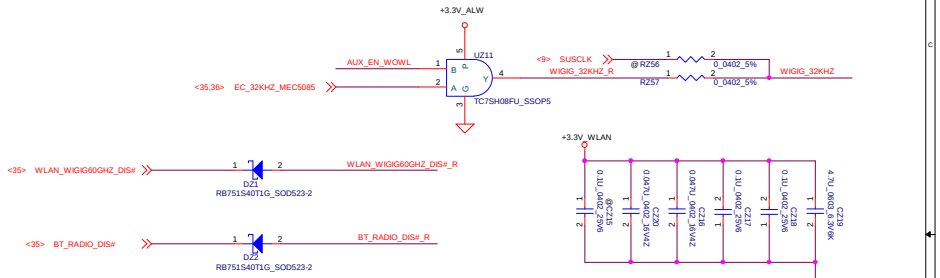
NGFF for UMA

NGFF slot A Key A



conn should be change SP070011B00 TBD



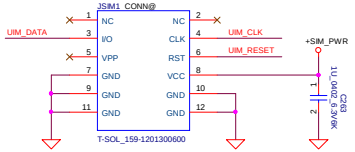


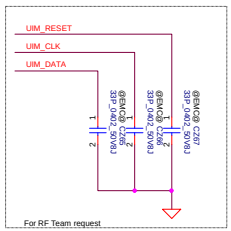
STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIE
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE
15	HIGH	HIGH	HIGH	HIGH	NA

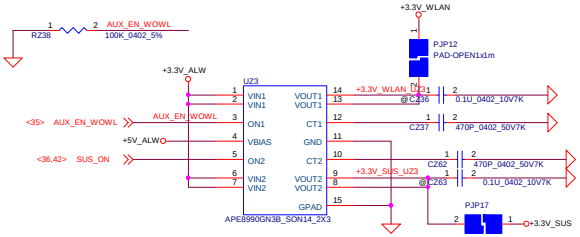
Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

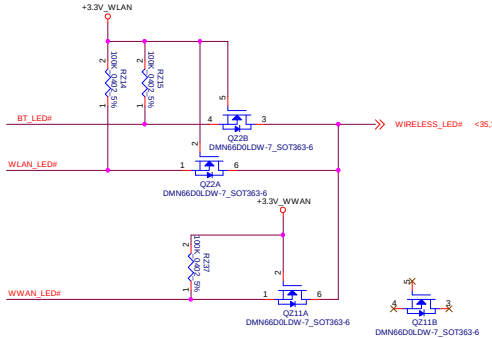
SIM Card







LED control circuit



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Title: NGFF Card

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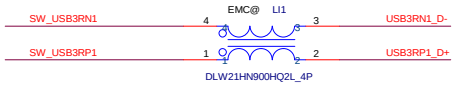
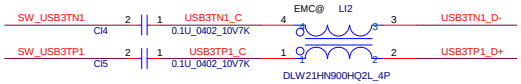
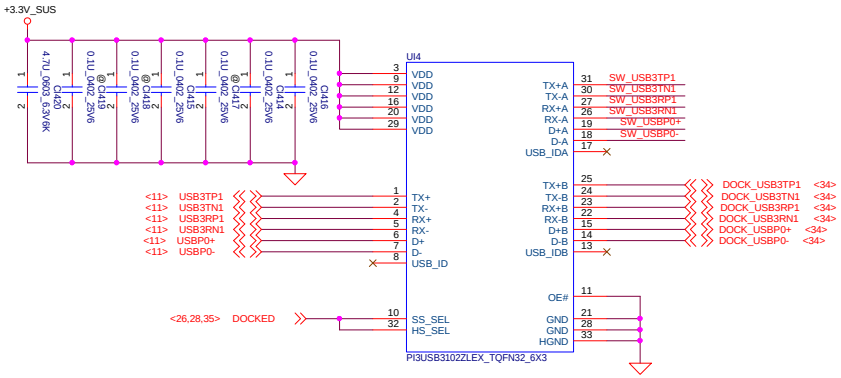
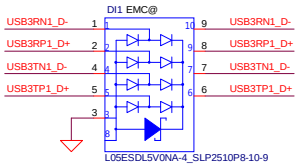


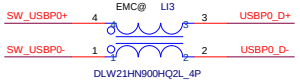




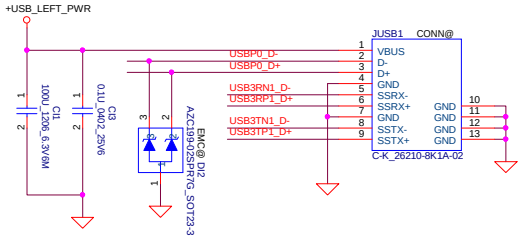
check port mapping

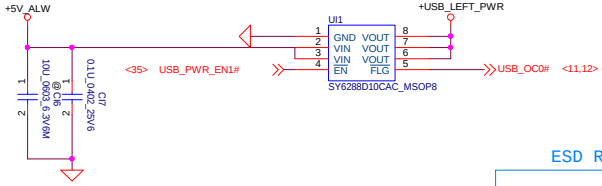
DOCKED	function
1	Dock
0	M/B



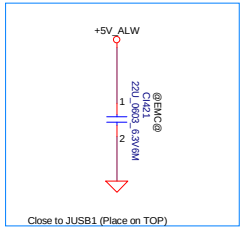


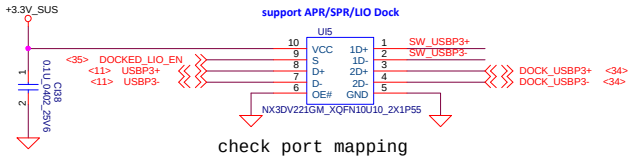
PCB	USB2 0	USB2 3
H12 UMA	USB3102	NX3DV221
H12 Entry	NA	NA
H14 DSC	USB3102	NX3DV221
H14 UMA	USB3102	NX3DV221
H14D_En	NA	NA
H14U_En	NA	NA
H15 DSC	USB3102	NX3DV221
H15 UMA	USB3102	NX3DV221
H15D_En	NA	NA
H15U_En	NA	NA





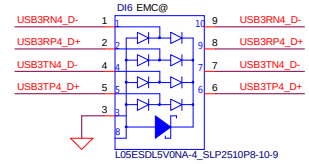
ESD Request

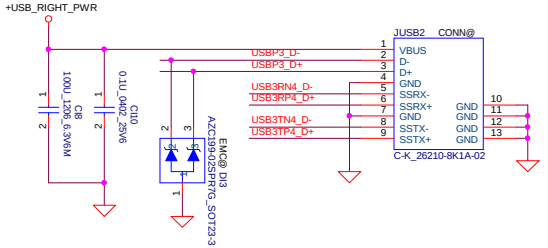


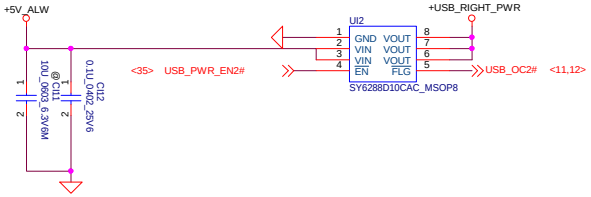


check port mapping

DOCKED_LIO_EN	function
1	Dock
0	M/B







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Title: USB3.0

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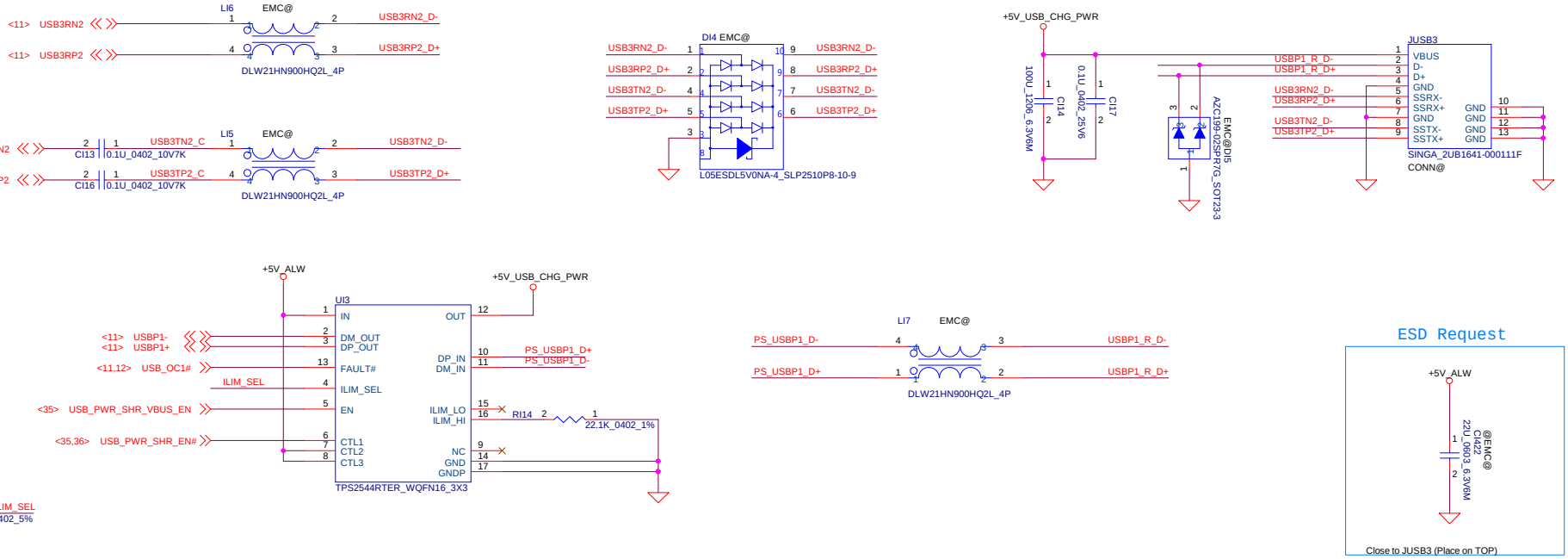

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Title: USB SW		
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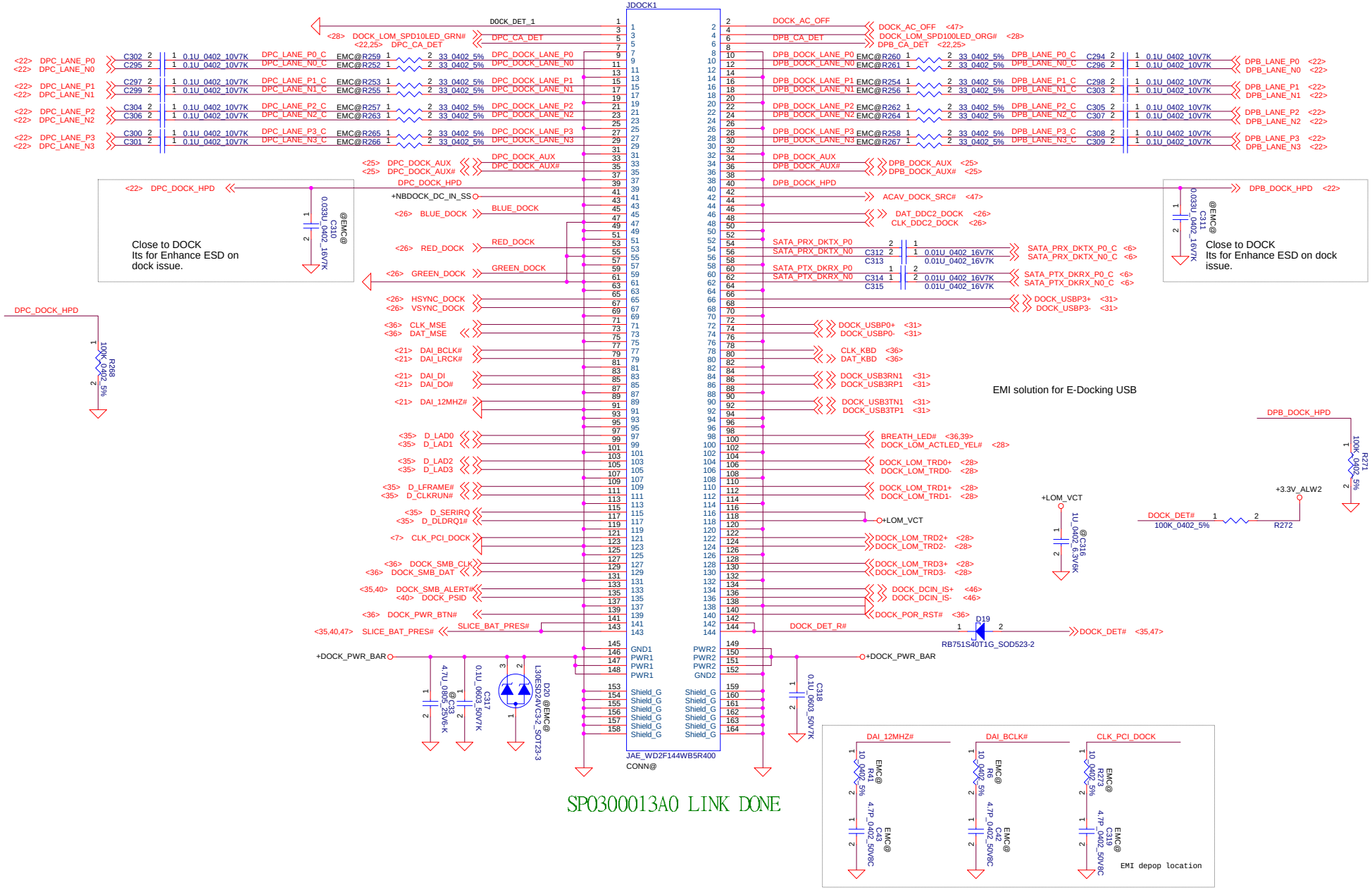
Houston 14 support NFC on USH



Compal Electronics, Inc.

Title: E-Dock

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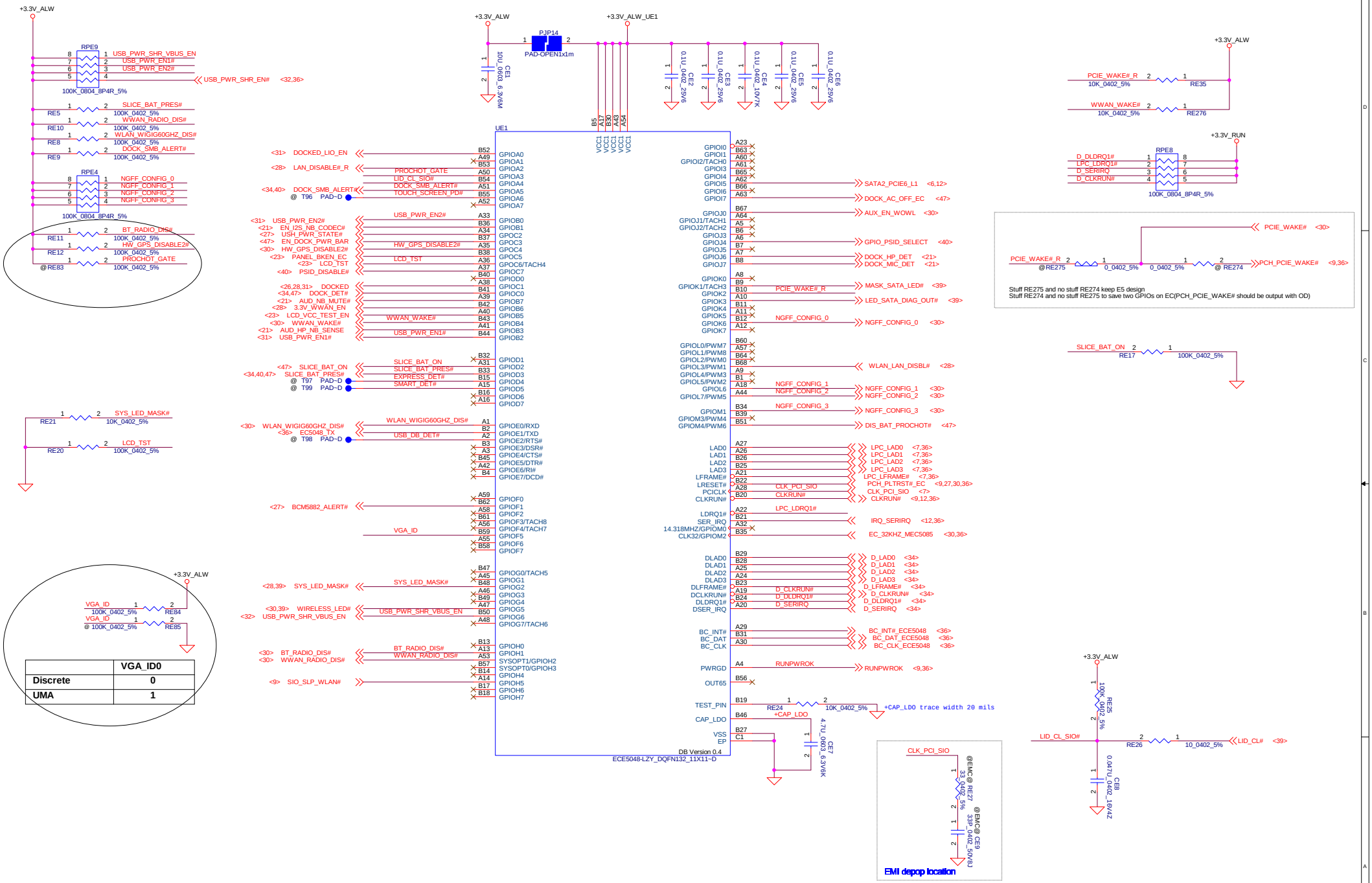

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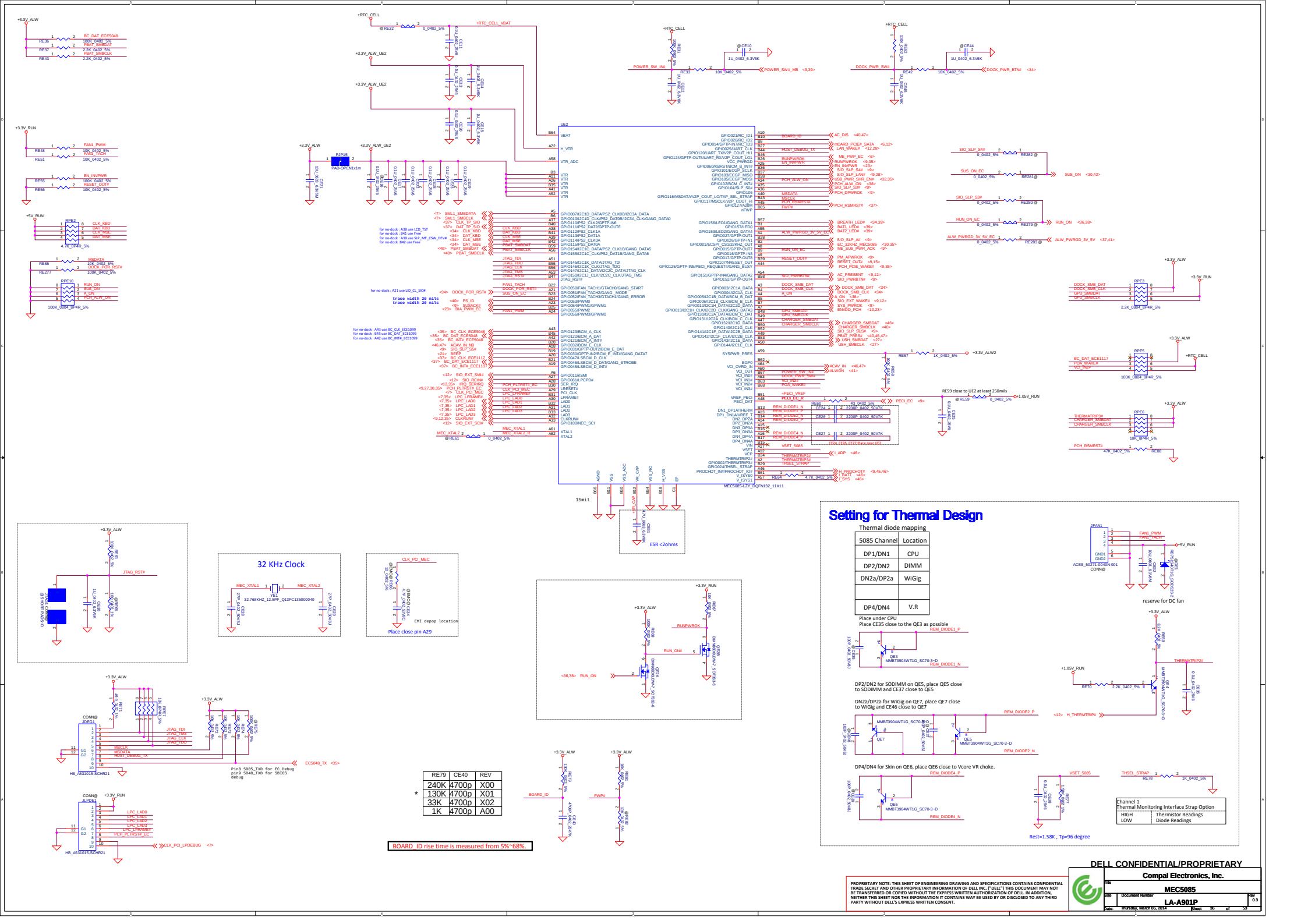
Setting for Thermal Design
Thermal diode mapping
5085 Channel | Location
DP1/DN1 | CPU
DP2/DN2 | DIMM
DN2a/DP2a | WiGig
DP4/DN4 | V.R
Place under CPU
Place CE35 close to the QE3 as possible
DP2/DN2 for SODIMM on QE5, place QE5 close to SODIMM and CE37 close to QE5
DN2a/DP2a for WiGig on QE7, place QE7 close to WiGig and CE46 close to QE7
DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.
reserve for DC fan
Rest=1.58K , Tp=96 degree
Channel 1
Thermal Monitoring Interface Strap Option
HIGH | Thermistor Readings
LOW | Diode Readings
32 KHz Clock
32.768KHZ_12.5PF_Q13FC1350000040
EMI depop location
Place close pin A29
ESR <2ohms
15mil
BOARD_ID rise time is measured from 5%~68%.
RE79 | CE40 | REV
240K | 4700p | X00
130K | 4700p | X01
33K | 4700p | X02
1K | 4700p | A00
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MEC5085
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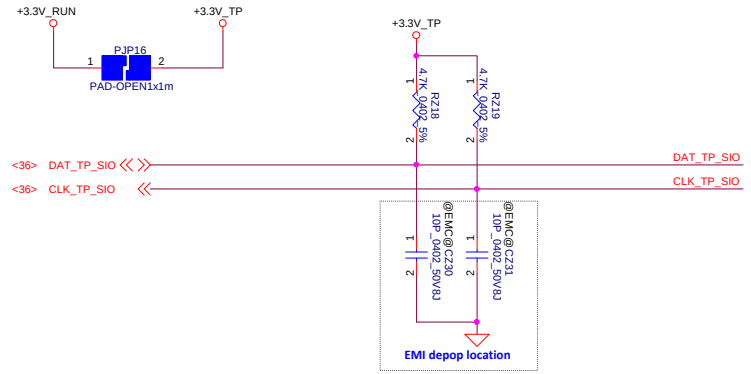
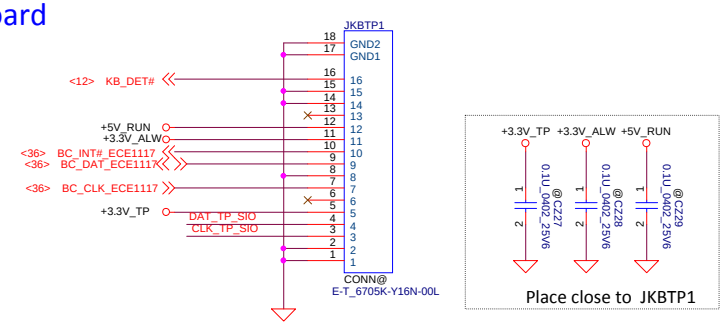
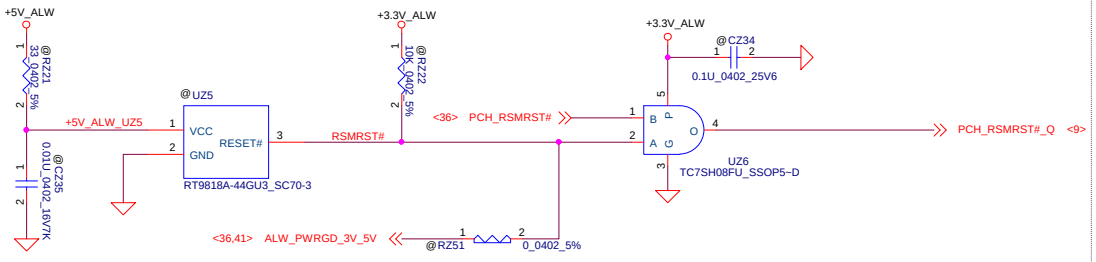
Touch Pad



Keyboard



RSMRST circuit



@eDP Cable W CAM

Part Number	Description
DC02C007600	H-CONN SET 13D MB-EDP-CAMERA

@eDP TS Cable W CAM

Part Number	Description
DC02C007C00	H-CONN SET 13D MB-EDP-CAMERA-TS

@eDP Cable W/O CAM

Part Number	Description
DC02C007D00	H-CONN SET 13D MB-EDP

@SATA SPINDLE Cable

Part Number	Description
DC02C007500	H-CONN SET 13D MB-SPINDLE HDD

@SATA Cable

Part Number	Description
DC02C007400	H-CONN SET 13D MB-MSATA HDD

@DC-IN Cable

Part Number	Description
DC30100Q100	CONN SET 13F DCJACK-MB 2DW1003-041110F

@BATT Cable

Part Number	Description
DC02001X800	H-CONN SET 13D MB-BATT CABLE

@LED FFC

Part Number	Description
NBX0001JG00	FFC 10P F P0.5 PAD0.3 172MM MB-LED/B 13D

@FP FFC

Part Number	Description
NBX0001JK00	FFC 8P F P0.5 PAD.3 123MM MB-FP VALIDITY

@TP FFC

Part Number	Description
NBX0001JI00	FFC 16P F P0.5 PAD=0.3 119MM MB-TP 13D

@USH Board FFC

Part Number	Description
NBX0001JJ00	FFC 26P G P0.5 PAD.3 88MM MB-USH/B 13D

@RTC BATT

Part Number	Description
GC02001DS00	BATT CR2032 3V 225MAH PA 5 W/C 30MM

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

Compal Electronics, Inc.

Title: Keyboard

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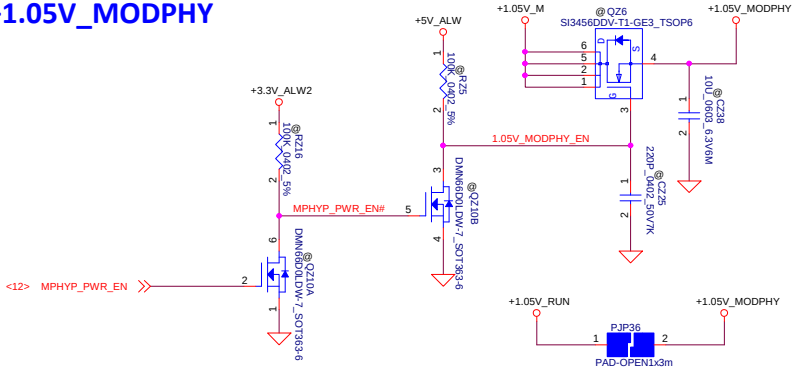
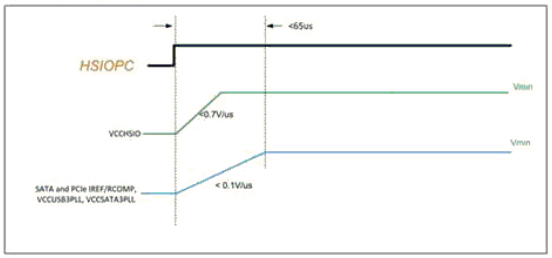
+1.05V_MODPHY

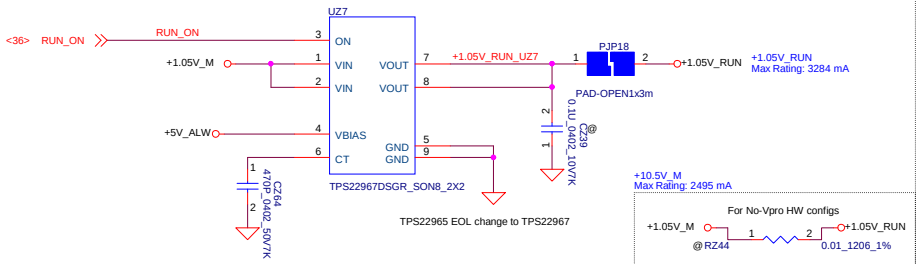


if support MODPHY off keep DSC solution
MODPHY timing spec 0.7V/us and <65us

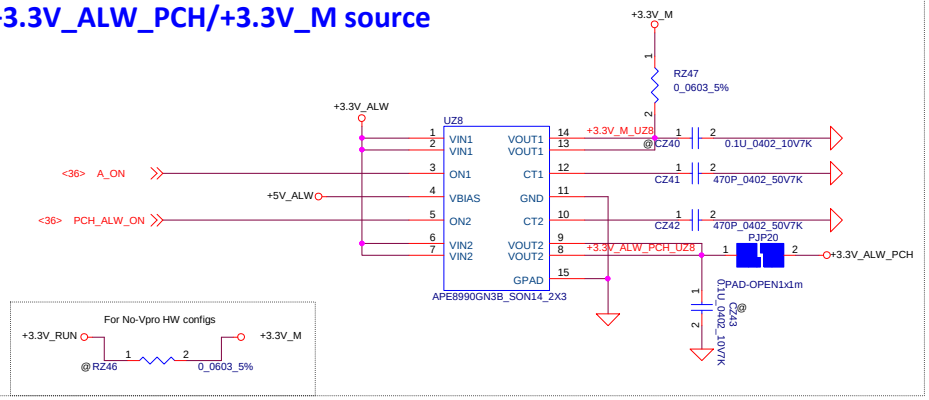
Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



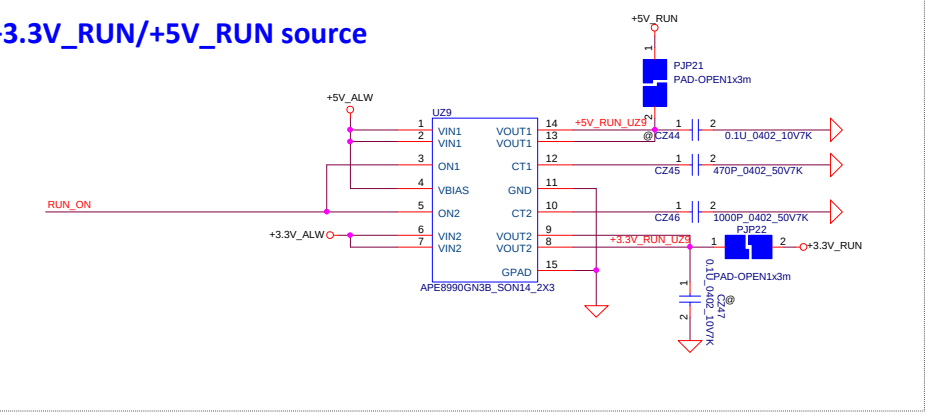
+1.05V_RUN source



+3.3V_ALW_PCH/+3.3V_M source



+3.3V_RUN/+5V_RUN source



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Compal Electronics, Inc.

Title: Power control

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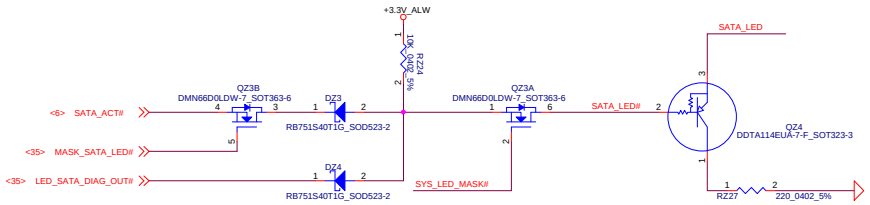
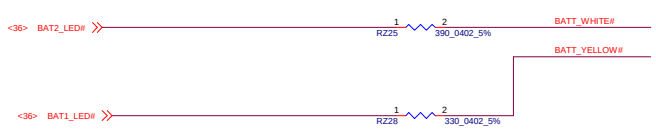
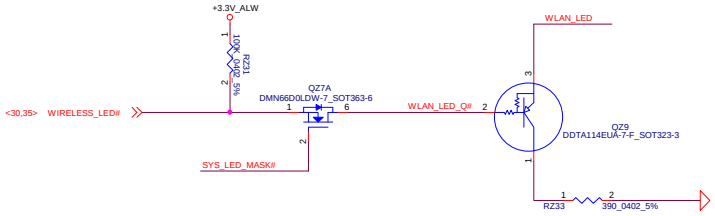
HDD LED solution for White LED



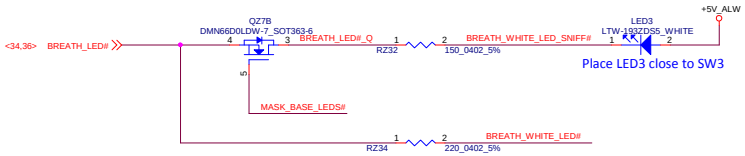
Battery LED

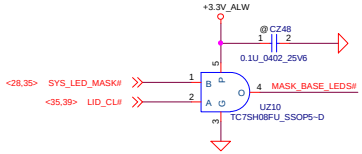


WLAN LED solution for White LED

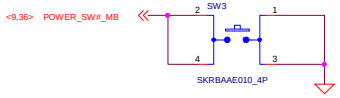


Breath LED

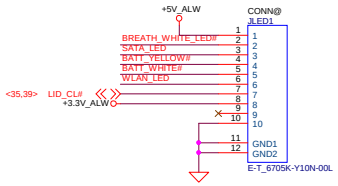




POWER & INSTANT ON SWITCH



LED board CONN



Fiducial Mark

@FD1 FIDUCIAL MARK~D
@FD2 FIDUCIAL MARK~D
@FD3 FIDUCIAL MARK~D
@FD4 FIDUCIAL MARK~D

LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

@H1 H_2P8 @H2 H_2P4 @H3 H_2P8 @H4 H_4P0 @H6 H_2P8 @H7 H_2P8 @H8 H_2P8 @H9 H_2P8 @H10 H_3P8 @H11 H_3P8 @H12 H_3P8 @H13 H_3P8 @H15 H_3P2 @H17 H_3P2 @H18 H_2P4 @H19 H_4P0 @H20 H_2P5N @H22 H_2P8 @H24 H_3P3

Compal Electronics, Inc.

Title: PAD, LED

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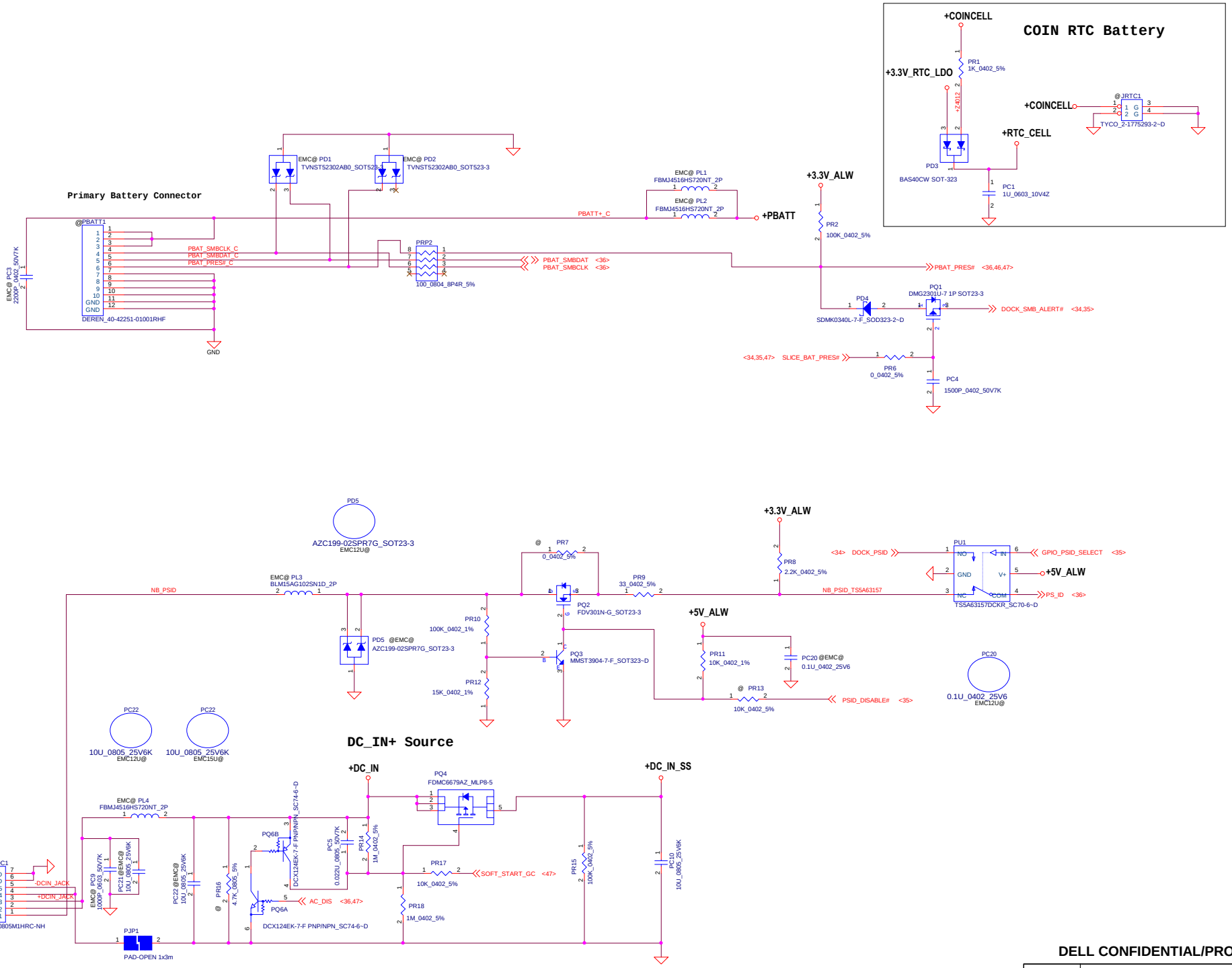

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Compal Electronics, Inc.			
Title: +DCIN			
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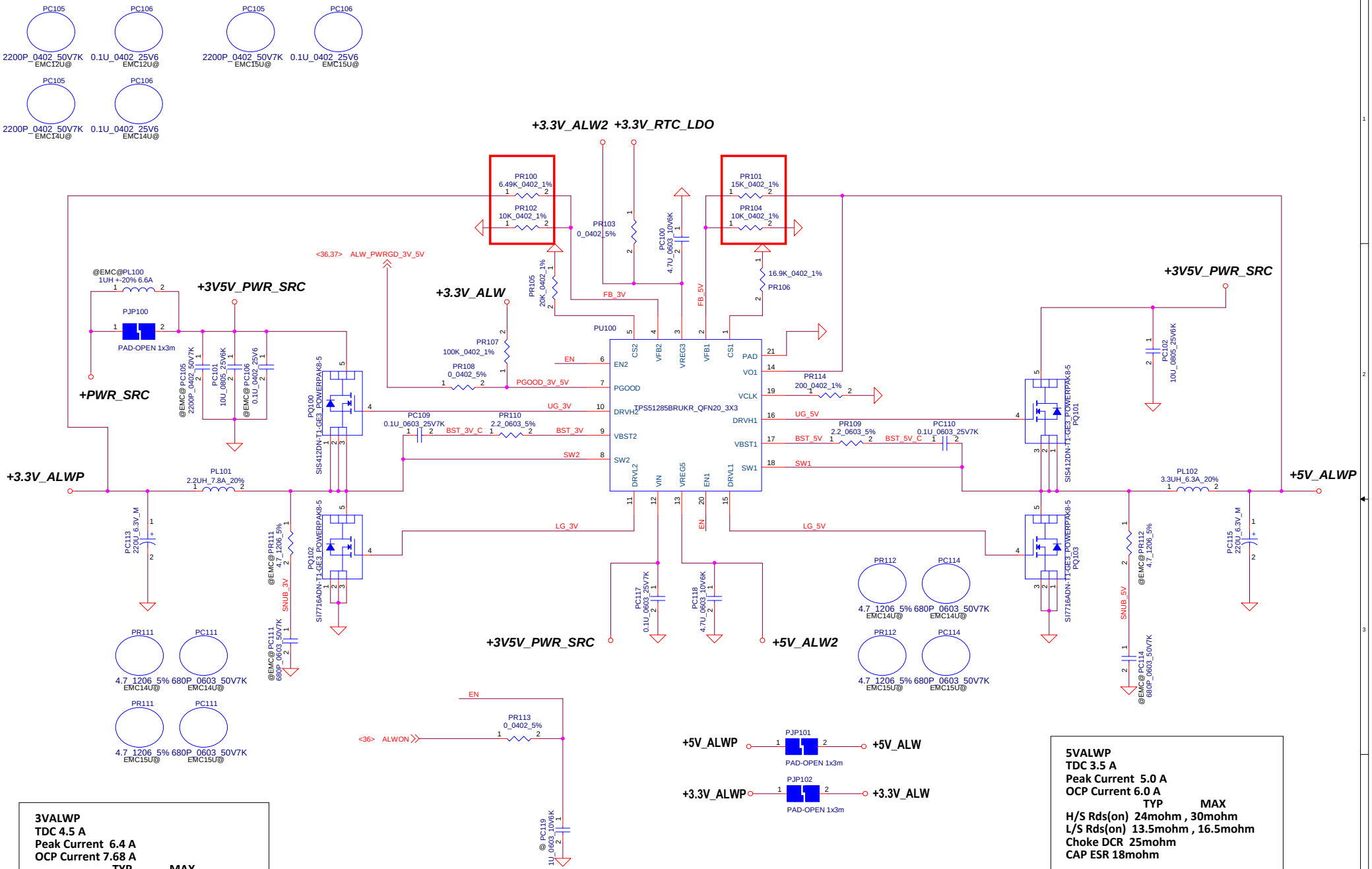

3VALWP
TDC 4.5 A
Peak Current 6.4 A
OCP Current 7.68 A

	TYP	MAX
H/S Rds(on)	24mohm	30mohm
L/S Rds(on)	13.5mohm	16.5mohm
Choke DCR	15.5mohm	
CAP ESR	18mohm	

5VALWP
TDC 3.5 A
Peak Current 5.0 A
OCP Current 6.0 A

	TYP	MAX
H/S Rds(on)	24mohm	30mohm
L/S Rds(on)	13.5mohm	16.5mohm
Choke DCR	25mohm	
CAP ESR	18mohm	

Compal Electronics, Inc.

Title: +5V_ALW/3.3V_ALW

Size: | Document Number: LA-A901P | Rev: 0.3

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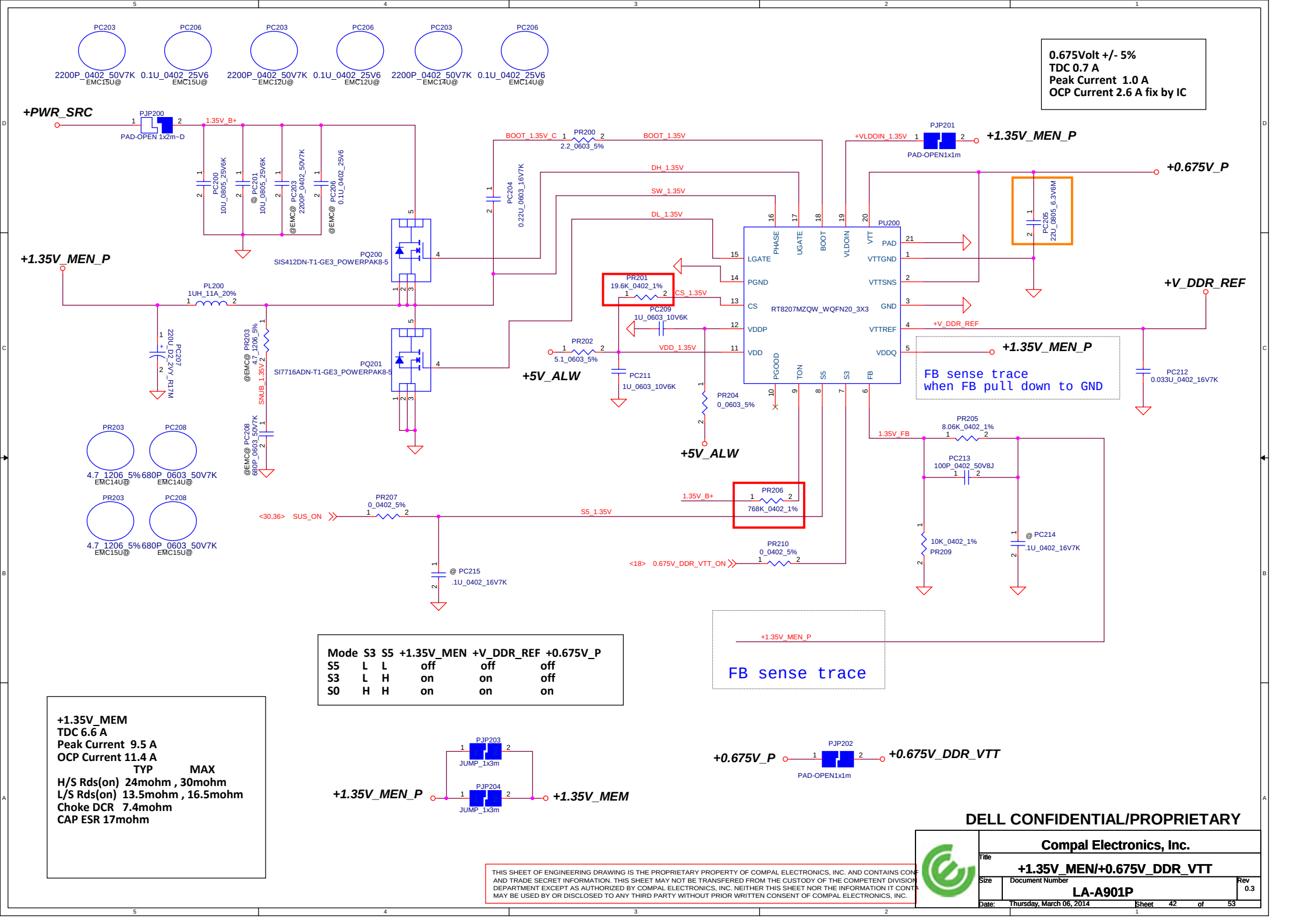

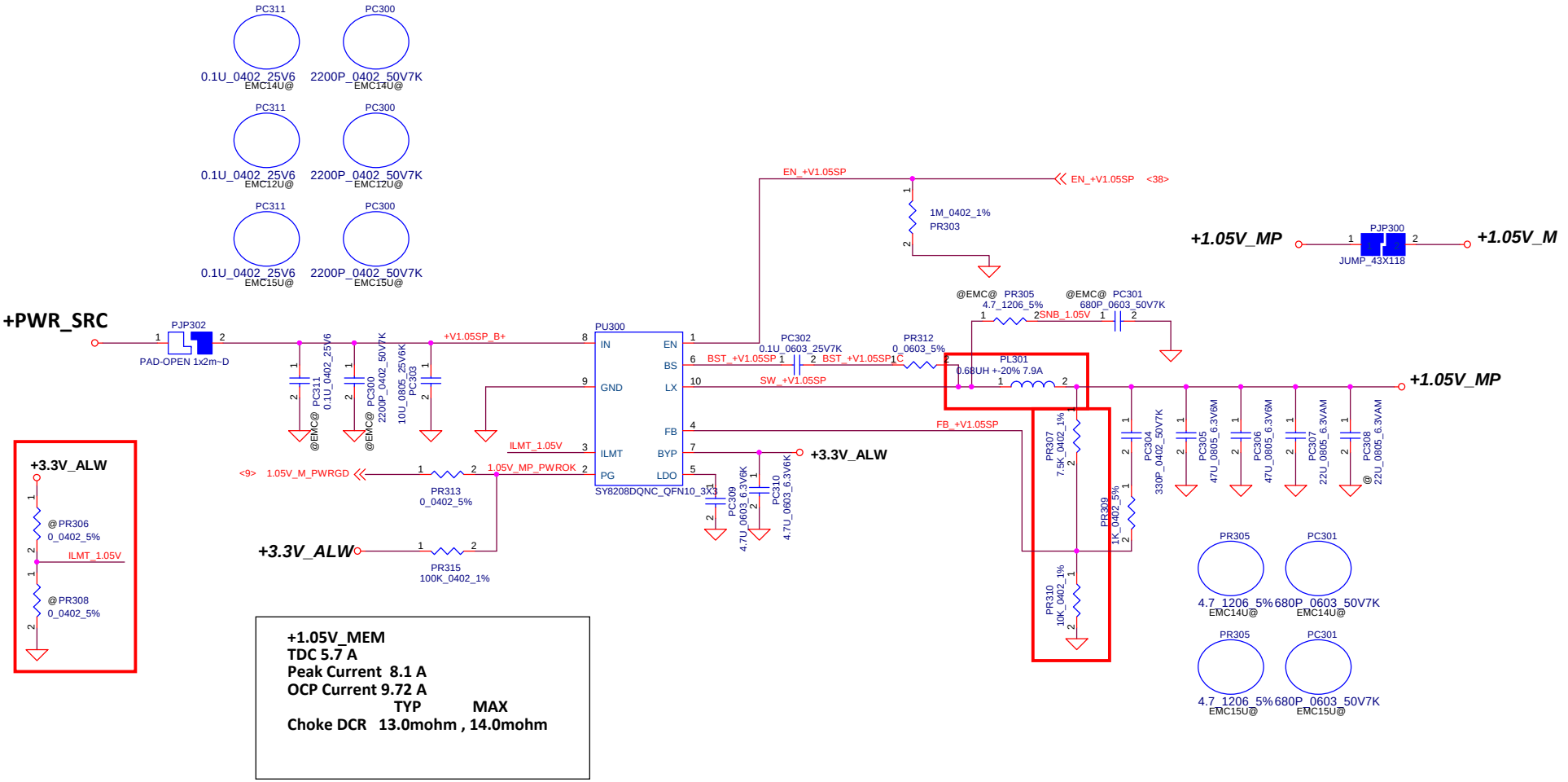

+1.05V_MEM
TDC 5.7 A
Peak Current 8.1 A
OCP Current 9.72 A

	TYP	MAX
Choke DCR	13.0mohm ,	14.0mohm

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Compal Electronics, Inc.	
Title	+1.05V_M
Size	Document Number: LA-A901P
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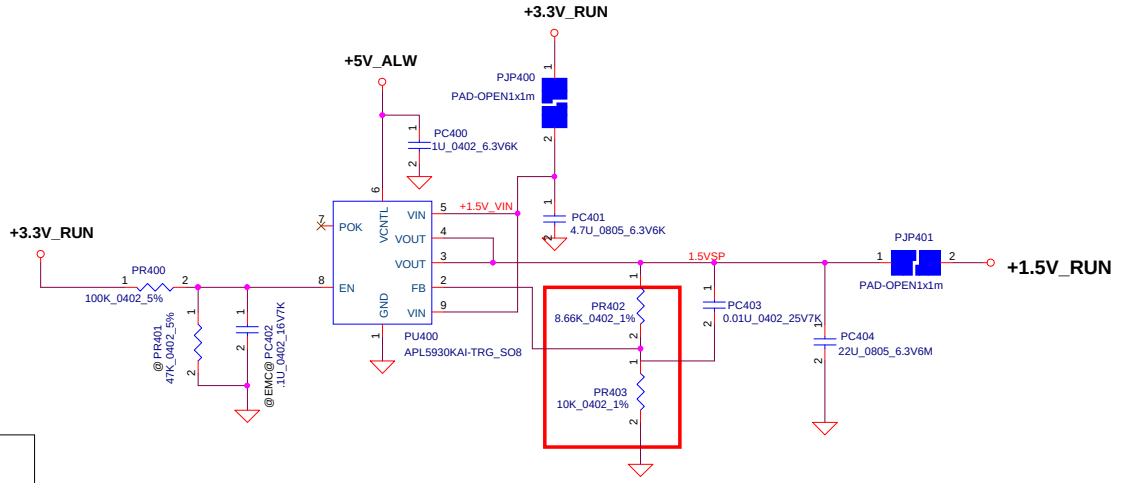

+1.5V_RUN
TDC 0.47 A
Peak Current 0.67 A

Compal Electronics, Inc.		
Title: +1.5V_RUN		
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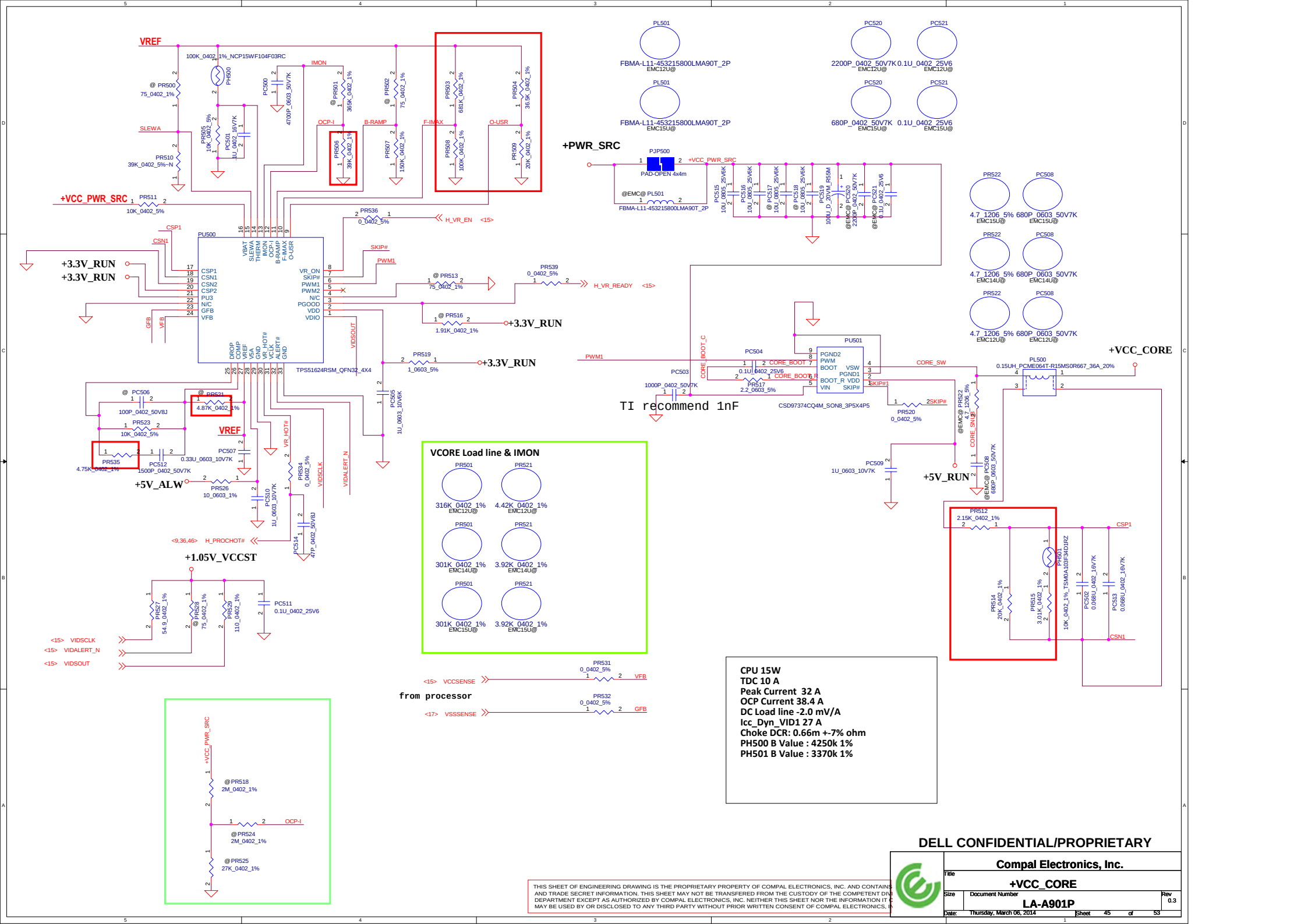

CPU 15W
TDC 10 A
Peak Current 32 A
OCP Current 38.4 A
DC Load line -2.0 mV/A
Icc_Dyn_VID1 27 A
Choke DCR: 0.66m +-7% ohm
PH500 B Value : 4250k 1%
PH501 B Value : 3370k 1%

Compal Electronics, Inc.

Title: +VCC_CORE

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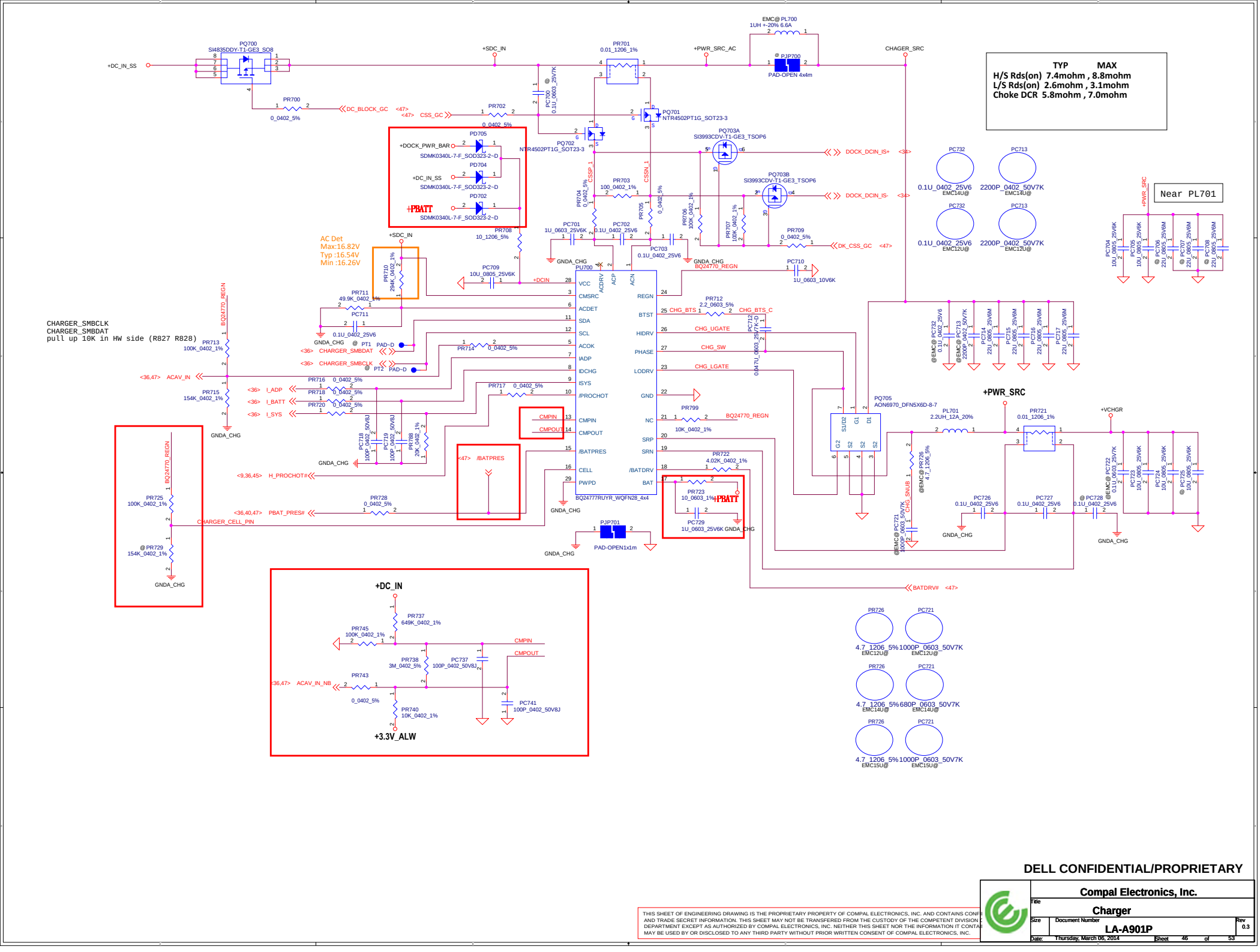
TYP MAX
H/S Rds(on) 7.4mohm , 8.8mohm
L/S Rds(on) 2.6mohm , 3.1mohm
Choke DCR 5.8mohm , 7.0mohm
Near PL701
AC Det
Max:16.82V
Typ :16.54V
Min :16.26V
CHARGER_SMBCLK
CHARGER_SMBDAT
pull up 10K in HW side (R827 R828)
+PWR_SRC
+DC_IN
+3.3V_ALW
BQ24777RUYR_WQFN28_4x4
SI4835DDY-T1-GE3_SO8
SI3993CDV-T1-GE3_TSOP6
NTR4502PT1G_SOT23-3
SDMK0340L-7-F_SOD323-2~D
AON6970_DFN5X6D-8-7
PAD-OPEN 4x4m
PAD-OPEN1x1m
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MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
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Compal Electronics, Inc.
Charger
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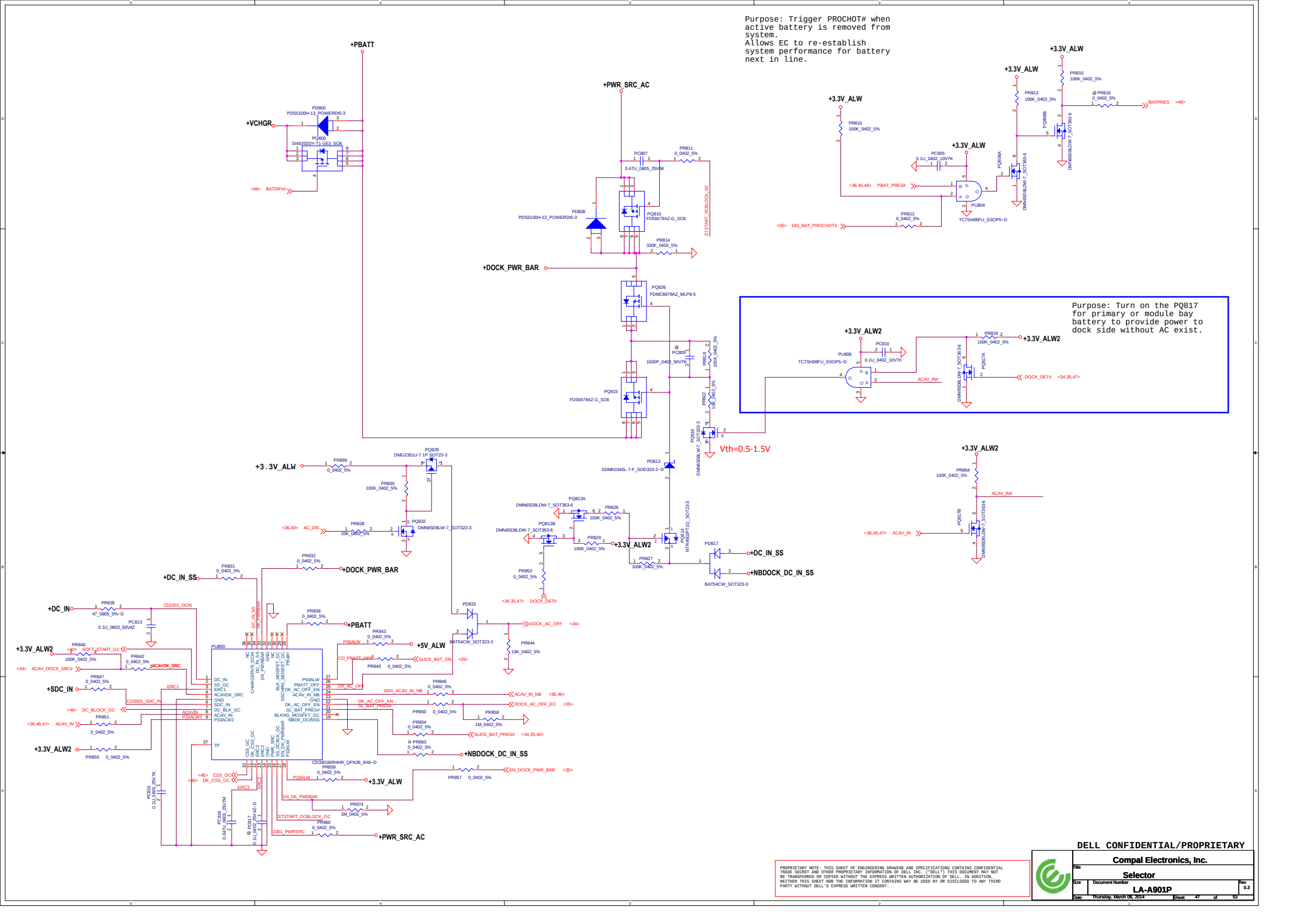
Purpose: Trigger PROCHOT# when active battery is removed from system.
Allows EC to re-establish system performance for battery next in line.

Purpose: Turn on the PQ817 for primary or module bay battery to provide power to dock side without AC exist.



DELL CONFIDENTIAL/PROPRIETARY

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Compal Electronics, Inc.		
Title: Selector		
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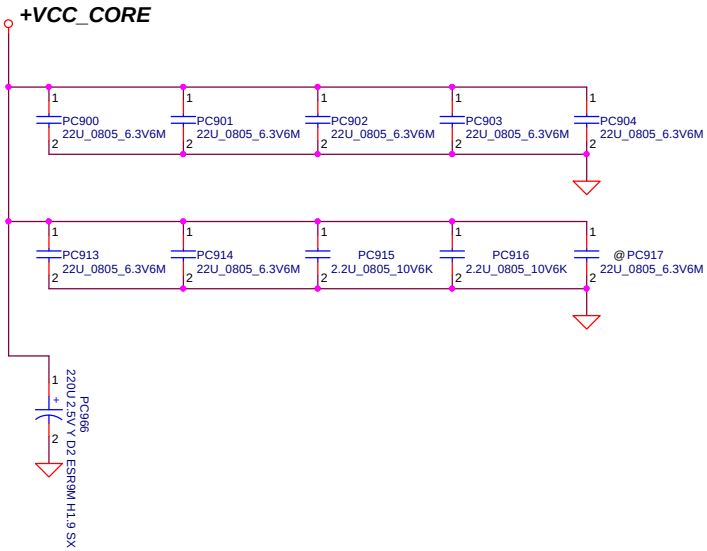

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	Selector	10/8	Compal	Remove slice battery support circuit	Remove PC808, PC811, PC812 , PC814, PD806, PD807, PD811, PD814, PD819, PD821, PQ801, PQ807, PQ809, PQ811, PQ812, PQ818, PQ821, PQ828, PQ830, PQ831, PR802, PR804, PR808, PR813, PR815, PR816, PR817, PR821, PR823, PR825, PR834, PR836, PR837, PR839, PR849, PR852, PR861, PU805, PU807, PU808	X01
2	45	VCC_CORE	10/8	Compal	To prevent acoustic noise issue	Remove PC923, PC924, PC925, PC926, PC927, PC928, PC929, PC930, PC931, PC940, PC941, PC943, PC946, PC947, PC948 Add PC966	X01
3	42	1.35V_MEN	10/8	RICHTEK	To prevent IC damage	Add PR204	X01
4	46	Charger	10/8	Compal	Fine tune divider voltage	Change PR713, PR725 to 100k Change PR715, PR729 to 154k	X01
5	41,43,44	+1.05V_M +1.5V_RUN +3V/+5V	10/22	Compal	To improve the ability of anti-noise	Change PR307 to 7.5k Change PR310, PR102, PR104, PR403 to 10k Change PR100 to 6.49k Change PR101 to 15k Change PR402 to 8.66k	X01
6	46	Charger	10/25	Compal	Change /BATPRES pin control net from /BATPRES to PBAT_PRES#	Pop PR728 Depop PR816	X01
7	45	VCC_CORE	10/31	Compal	Fine tune IMON	Add PR518, PR524, PR525	X01
8	ALL	ALL	10/31	Compal	RF request	Add PC521, PC206, PC106, PC311, PC732 (0.1uF)	X01
9	ALL	ALL	10/31	Compal	RF request	Pop PR111,PC111,PR112,PC114,PR203,PC208,PR305,PC301,PR522,PC508, (4.7ohm, 680pF)	X01
10	46	Charger	10/31	Compal	To prevent VCP trigger PROCHOT#	PR703 change to 100ohm	X01

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	HW	2013/10/8	COMPAL	Follow intel reference circuit.	Add CC100, RC300 on CPU pin AC4, net name is PM_TEST_RST	0.2(X01)
2	27	HW	2013/10/8	COMPAL	Dell drop POA function.	Change JUSH1 from 26 pin to 20 pin, pin define follow E5	0.2(X01)
3	36	HW	2013/10/8	COMPAL	Dell drop POA function.	remove POA_WAKE# off page symbol remove POA_ON/OFF#,make UE2.B62 to be NC pin	0.2(X01)
4	22	HW	2013/10/9	COMPAL	IC version changed.	VMM2320 circuit change: 1. UV8 from VMM2320 change to VMM 2330 (SA00007G800) 2. UV8 pin J3, E5 to +1.05V_RUN 3. VMM_SPI_WP# reserved RV517, 2.2K resistor PU to +3.3V_RUN_VMM 4. VMM_GPIO4,reserved RV518, 2.2K resistor PU to +3.3V_RUN_VMM 5. VMM_GPIO5 reserved RV519, 2.2K resistor PU to +3.3V_RUN_VMM 6. add QV20,CZ69,RV210,RV212,QV21 external FET switch circuit 7. UV8 pin B5, B6 change to +3.3V_RUN_VMM 8. LP_CTL add RV516, 2.2K resistor PU to +3.3V_RUN_VMM 9. Depop RV73 10. add LP_EN on UV8.A5 (10/18) 11. depop QV20,CZ69,RV210,RV212, QV21 external FET switch circuit (10/24) 12.RPV2 pin1 & pin2 NC (11/4)	0.2(X01)
5	23	HW	2013/10/9	COMPAL	Follow EMC suggestion	Change LI1,LI2,LI3,LI4,LI5,LI6,LI7,LI8,LI9,LV3,LV6,LV10,LV12,LV27 From SM070003K00 (S COM FI_ CHILISIN CMMI21T-900Y-N) To SM070003Y00 (S COM FI_ MURATA DLW21HN900HQ2L)	0.2(X01)
6	9	HW	2013/10/9	COMPAL	reserved for S3 within 2s , system shutdown issue debug.	add RC26, , reserved RC27.	0.2(X01)
7	36	HW	2013/10/9	COMPAL	board ID change.	RE79 change to 130K	0.2(X01)
8	36	HW	2013/10/14	COMPAL	follow intel latest design guide.	pop RE56 and change from 8.2K to 10K , it's RESET_OUT# pull down resistor	0.2(X01)
9	7	HW	2013/10/16	COMPAL	RF requirement.	add CC14, CC15 and move CC12, CC13 to behind the resistor (RC72)	0.2(X01)
10	20,23,31,32	HW	2013/10/17	COMPAL	follow ESD recommend list.	change all ESD diode CPN change DI2, DI3, DI5, DV4 from SCA00001100(S ZEN ROW PJDLC05C 3P C/A SOT23) to SC600001600(S DIO ROW AZC199-02S.R7G C/C SOT23 ESD) change DI1,DI6,DI4 from SC300002800(S DIO(BR) TVWDF1004AD0 DFN ESD) to SC300002C00(S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD) change DA1,DA2,DA3,DA6,DA7 from SCA00001L00(S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD) to SCA00002900(S ZEN ROW L03ESDL5V0CC3-2 C/A SOT-23 ESD)	0.2(X01)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
11	7,38	HW	2013/10/17	COMPAL	for UMA DOCK configure, it support has non-VPRO configure.	add PJP33, PJP34 UC3, CC7, RC50, RC55, RPC12, UZ7, CZ64 change to VPRO@	0.2(X01)
12	38	HW	2013/10/17	COMPAL	power doesn't split VPRO & NPRO BOM.	add RZ41, RZ42, reserve it for VPRO & NVPRO option.	0.2(X01)
13	39	HW	2013/10/17	COMPAL	SSI design will cause LED behavior error.	remove QZ5, QZ7.2 & QZ3.2 change to SYS_LED_MASK#	0.2(X01)
14	20	HW	2013/10/17	COMPAL	To solve Line-on HDD dirty shut down issue.	add UN3, CN3, CN4, PJP7 and reserved it.	0.2(X01)
15	30,36	HW	2013/10/17	COMPAL	follow Dell requirement.	add back SUS_ON, change +3.3V_SUS control pin to SIO_SLP_S4# 1. UL3.3 from SIO_SLP_S4# to SUS_ON 2. UE2.B23 → SUS_ON_EC , RPE10.2 → SUS_ON 3. add RE282(Pop), RE281(depop) 4. add RE279, RE280 (dock only) 5. UE2.B9 → RUN_ON_EC	0.2(X01)
16	23	HW	2013/10/18	COMPAL	follow ESD recommend.	LZ1 change from SM070001N00 to SM070003Y00	0.2(X01)
17	12	HW	2013/10/24	COMPAL	add GPIO pin for DIMM quantity detection.	add DIMM_DET on UC1.U4 to replace PCH_GPIO48, remove	0.2(X01)
18	6	HW	2013/10/24	COMPAL	debug usage.	add RC301	0.2(X01)
19	9	HW	2013/10/28	COMPAL	reserve it to prevent PCH_PLTRST# floating when power on	add RC304, 100K pull down, on PCH_PLTRST#_EC	0.2(X01)
20	30	HW	2013/10/29	COMPAL	New SIM connector has no this pin.	remove UIM_DET on JNGFF2 pin58	0.2(X01)
21	23	HW	2013/10/29	COMPAL	it's designed for Goliad, Houston doesn't need.	remove RZ1	0.2(X01)
22	30	HW	2013/10/29	COMPAL	To solve WWAN can not detec issue.	Add RZ43, 100k pull up for WWAN_PWR_EN	0.2(X01)
23	38	HW	2013/10/29	COMPAL	for support VPRO & NVPRO BOM option.	remove PJP33, PJP34, PJP19 add RZ44, RZ46, RZ47	0.2(X01)
24	12	HW	2013/10/29	COMPAL	To solve backdrive issue.	Change TPM_PIRQ# pull up (RC247) to +3.3V_RUN from +3.3V_ALW_PCH	0.2(X01)
25	37	HW	2013/10/29	COMPAL	Dell request.	add RZ48, RZ49, QZ12 depop UZ5, UZ6, RZ21, RZ22, CZ35,RC91 (11/4) add RZ51, change QZ12 from 3904 to 3906. make RPE6 to be NC pin, add RE88 (11/4)	0.2(X01)

Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
26	30	HW	2013/10/30	COMPAL	Dell doesn't support MODPHY.	add PJP36, depop QZ6, QZ10, RZ16, RZ5, CZ25, CZ38	0.2(X01)
27	28	HW	2013/11/04	COMPAL	SSI design will cause LED behavior error.	Change QL1, QL2 contorl pin from MASK_BASE_LEDS# to SYS_LED_MASK#	0.2(X01)
28	21	HW	2013/11/04	COMPAL	EMC request.	Add RA42, RA43.	0.2(X01)
29	21	HW	2013/11/05	COMPAL	follow vender suggestion. It's for 15KV ESD fail issue.	add CA12, CA13 change DA1, DA2, DA3, DA4 from GNDA to GND	0.2(X01)
30	12	HW	2013/11/05	COMPAL	GPIO 14 is sus power well, it has risk to cause back drive.	move TPM_PIRQ# from PCH_GPIO14 to PCH_GPIO17, add T21 on PCH_GPIO14	0.2(X01)
31	30	HW	2013/11/05	COMPAL	follow vender request.	RZ43 from 100K change to 0 ohm	0.2(X01)
32	20	HW	2013/11/06	COMPAL	For SATA repeater setting	RN11,RN16 pop 0ohm	0.2(X01)
33	28	HW	2013/11/06	COMPAL	For EMI request	RL21~ RL28 change to 2.2 ohm	0.2(X01)
41	20	HW	2013/11/06	COMPAL	For SATA repeater setting	RN11,RN16 pop 0ohm	0.2(X01)
42	30	HW	2013/11/05	COMPAL	follow vender request.	RZ43 from 100K change to 0 ohm	0.2(X01)
43	9,11,27, 35,36	HW	2013/11/20	COMPAL	follow vender suggest to solve "Bo" noise issue	1.UA1 pin22 add RA45 0 ohm PU to +3.3V_RUN_AUDIO 2.UA1 pin21 add RA44 100k ohm to GND	0.2(X01)
44	12,22	HW	2013/11/20	COMPAL	follow vender suggest	1.RPC8 change from 2.2k to 10k 2.UC1.F2 &RPC8.3 change name from I2C0_SDA to PCH_GPIO4 3.UC1.F3 &RPC8.4 change name from I2C0_SCL to PCH_GPIO5 4.UC1.G4 &RPC8.1 change name from I2C1_SDA_VMM to PCH_GPIO6 5.UC1.F1 &RPC8.2 change name from I2C1_SCL_VMM to PCH_GPIO7 6.RPV2.1 connect to I2C1_SDA_VMM 8.RPV2.2 connect to I2C1_SCL_VMM	0.2(X01)
45	22	HW	2013/11/27	COMPAL	To solve CRT display jitter issue	LV23,LV25 change from BLM15AX102SN1D to BLM15PX181SN1D	0.2(X01)
46	36,37	HW	2013/11/27	COMPAL	Base on Pre-PT RSMRST EA result	1.POP RE88,UZ6,RE51 2.remove QZ12,RZ48,RZ49,RZ50	0.2(X01)
47	6	HW	2013/11/29	COMPAL	follow intel DG, ESR MAX=50 ohm	Change YC1 from SJ100001K00(S CRYSTAL 32.768KHZ Q13FC1350000400) to SJ10000LD00(S CRYSTAL 32.768KHZ 12.5PF 9H03220008)	0.2(X01)
48	22	HW	2013/12/10	COMPAL	follow vender suggestion	1. change LV22,LV24 from SM01000N400(S SUPPRE_ MURATA BLM15AX102SN1D 0402) to SM01000NO00(S SUPPRE_MURATA BLM15PX181SN1D 0402) 2. change CV82, CV94 from 1uF to 10uF 3. UV8 pin D3 from +1.05V_VMM_VDDTX to+1.05V_VMM_VDD. 4. UV8 Pin H3, E10, H11 change to NC 5. Change UV8 pin B5, B6 from +3.3V_RUN_VMM to +3.3V_RUN_VDDIO	0.2(X01)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
49	34	HW	2013/12/18	COMPAL	To solve Power leakage issue.	Change R272 from 10K to 100K, and pull up to +3.3V_ALW2	0.2(X01)
50	21	HW	2013/11/05	COMPAL	follow ESD/vender request	1. change RA42, RA43 to LA10, LA1 SM01000NA00(S SUPPRE_ MURATA BLM15PX330SN1D 0402) 2. change RA7, RA8 from 16 to 24.9 ohm 3. DA1 &DA3 change from SCA00002900 to SCA00001B00(S ZEN ROW AZ5123-02S.R7G 3P C/A SOT23) 4.CA4&CA1 change from 220pF(@EMC@) to 680pF(EMC@)	0.2(X01)
51	26	HW	2013/12/18	COMPAL	Base on CRT EA result	change CV51, CV52, CV53 from 12pF to 2.2pF	0.2(X01)
52	20	HW	2013/12/18	COMPAL	For SATA repeater setting	De-pop RN9,RN13	0.2(X01)
53	38	HW	2014/02/06	COMPAL	For MODPHY power rail contril by JUMP directly	1.change PJP36 pin1 from +1.05V_M to +1.05V_RUN 2.depop QZ6, QZ10, RZ16, RZ5, CZ25, CZ38	0.3(X01)
54	25	HW	2014/02/06	COMPAL	Base on PS8338 datasheet, PI0 have 2 level, PI1 have 3 level	For PI0, delete RV66 For PI1, add RV100 PD to GND	0.3(X01)
55	36	HW	2014/02/10	COMPAL	EC request, for Delray common code reserved.	add RE283(@)	0.3(X01)
56	29	HW	2014/02/27	COMPAL	EMI test fail , back to SSI SD card connector.	change JSD1 from TAITW_PSDCT6-20GLBS1NN4H_19P-T to ALPS_SCDADA0101_19P_NR	0.3(X01)
57	9,16	HW	2014/03/03	COMPAL	follow intel DG 1.2	1.reserved 0.47uF for +PCH_VCCDSW3_3 , near CPU AH10 pin 2.add 10K pull high to +PCH_VCCDSW3_3 for PM_LANPHY_ENABLE, leave RPC19. pin 3 NC	0.3(X01)
58	30	HW	2014/03/05	COMPAL	intel Wigig need 32K clock when DSx	1.Add UZ11&RZ56(@)&RZ57 2.JNGFF1 change to WIGIG_32KHZ from SUSCLK 3.JNGFF2.60 change to NC from SUSCLK	0.3(X01)
59	27	HW	2014/03/05	COMPAL	EMC team Solution	1. reserved CZ68 47nF on pltrst_ush# to GND. 2. Pop R6,R41,R273 to 10 ohm 3. Pop C42,C43,C319 to 4.7pF	0.3(X01)