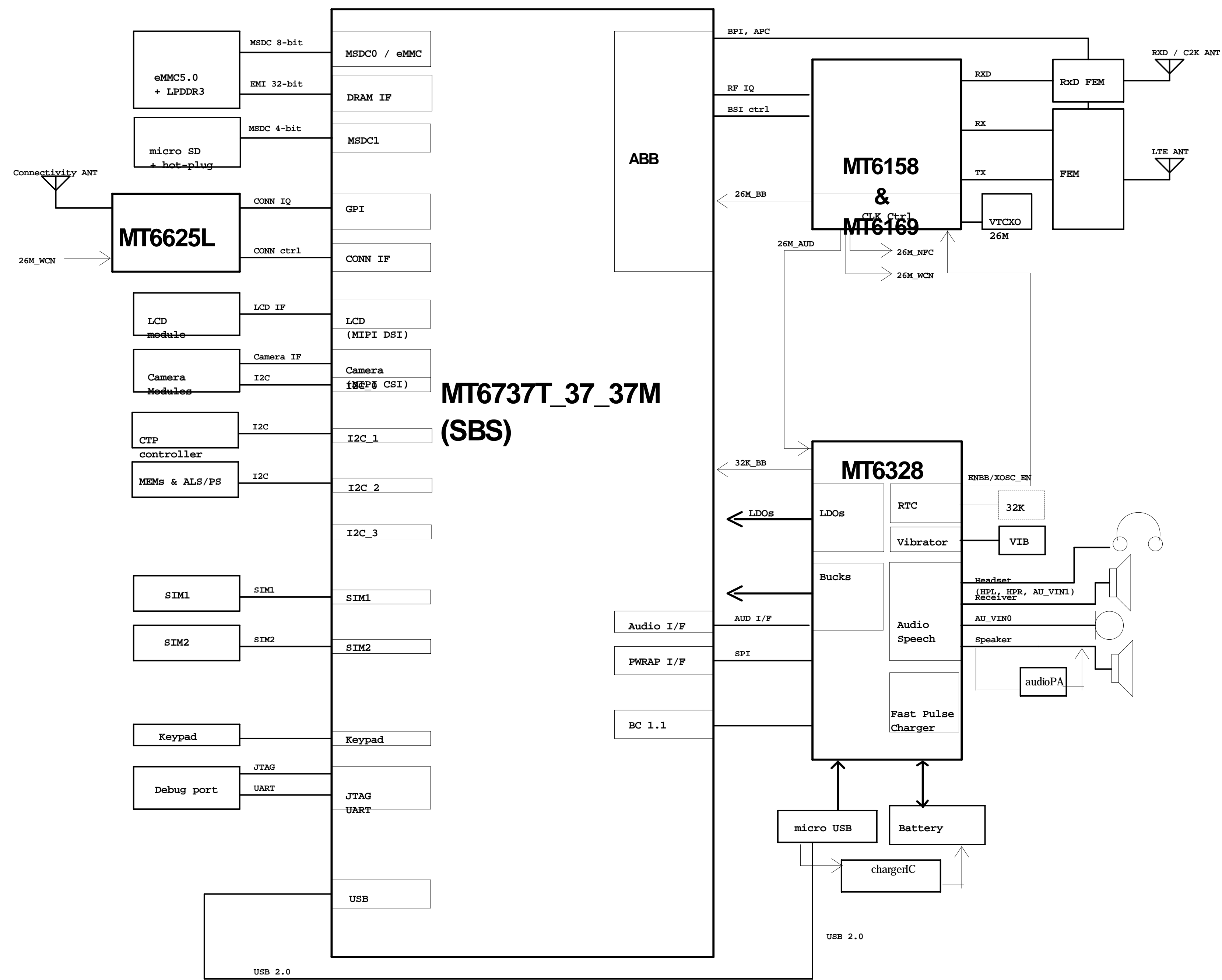
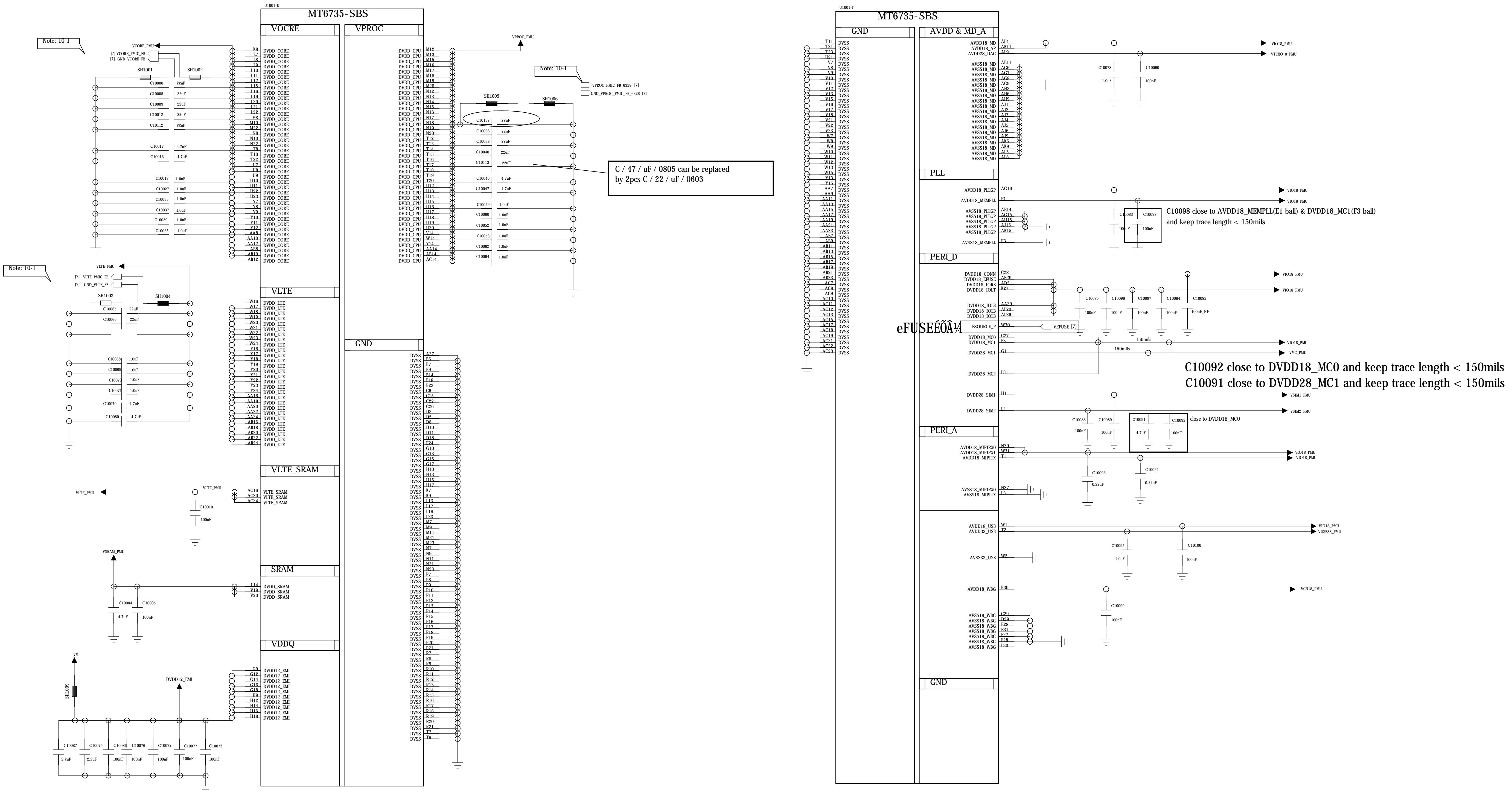


Project : MT6737T\_37\_37M REF\_SCH TOP LEVEL



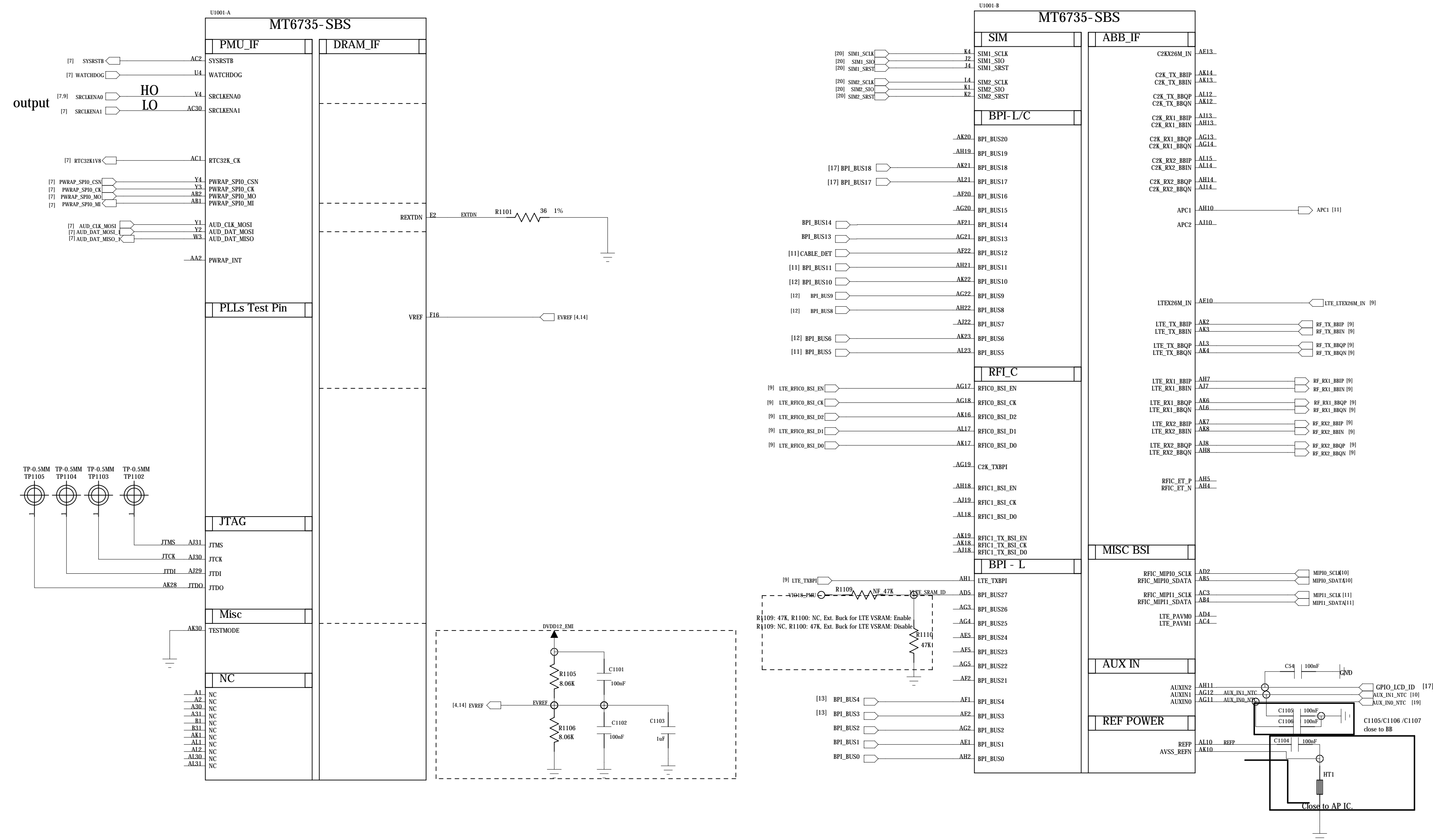
I2C	Function	I2C Spec.	Budget Timing	I2C Slave Address (7-bit mode)
I2C-0	Rear Camera - 8M	400 Kbps	Yes.	Rear camera (IMX135) I2C address: 0X10 (Write:0x20, Read:0x21) AF driver (DW9714A) I2C address: 0x0C (Write:0x18 , Read:0x19)
	Front Camera-2M	400 Kbps	Yes.	Front camera (GC2355) I2C address: 0x3C (Write:0x78, Read:0x79)
	charger IC			charger IC ( FAN54015) I2C address: 0x6A ( Write:0xD4, Read:0xD5)
I2C-1	CTP	400 Kbps	Yes.	GT1151 / CTP I2C address: 0X5D (Write:0xBA, Read:0xBB) or 0x14 (Write:0x28, Read:0x29)
I2C-2	LCD_DC-DC			DC-DC( KTD2151EU0-TR) I2C Address: 0x3E ( Write:0x7C, Read:0x7D)
	G-Sensor	400 Kbps	Yes.	G-Sensor( BMA253) I2C Address: 0x18 ( Write:0x30, Read:0x31)
I2C-3				
Note : I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)				

MT6737M

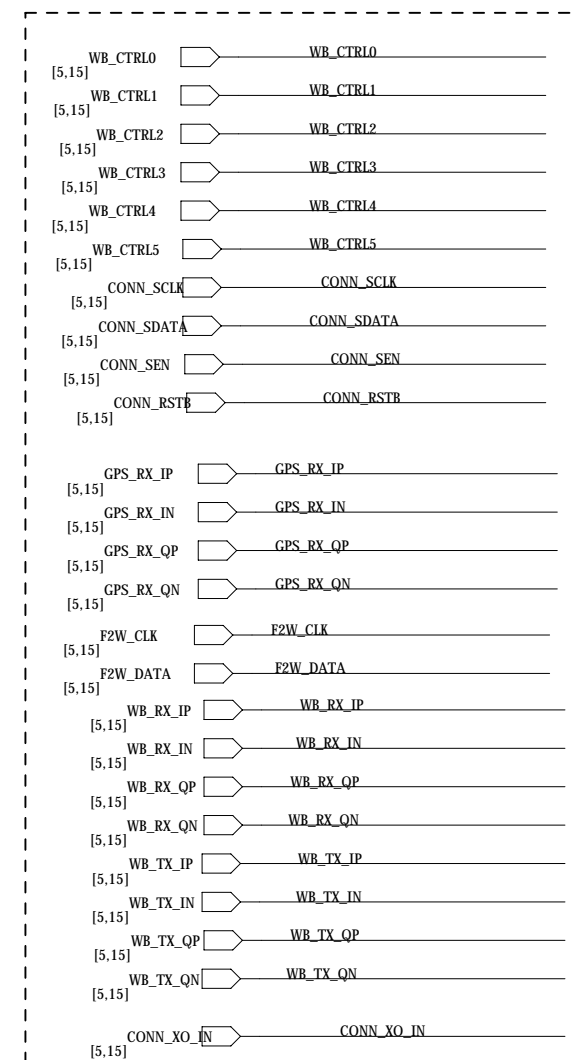
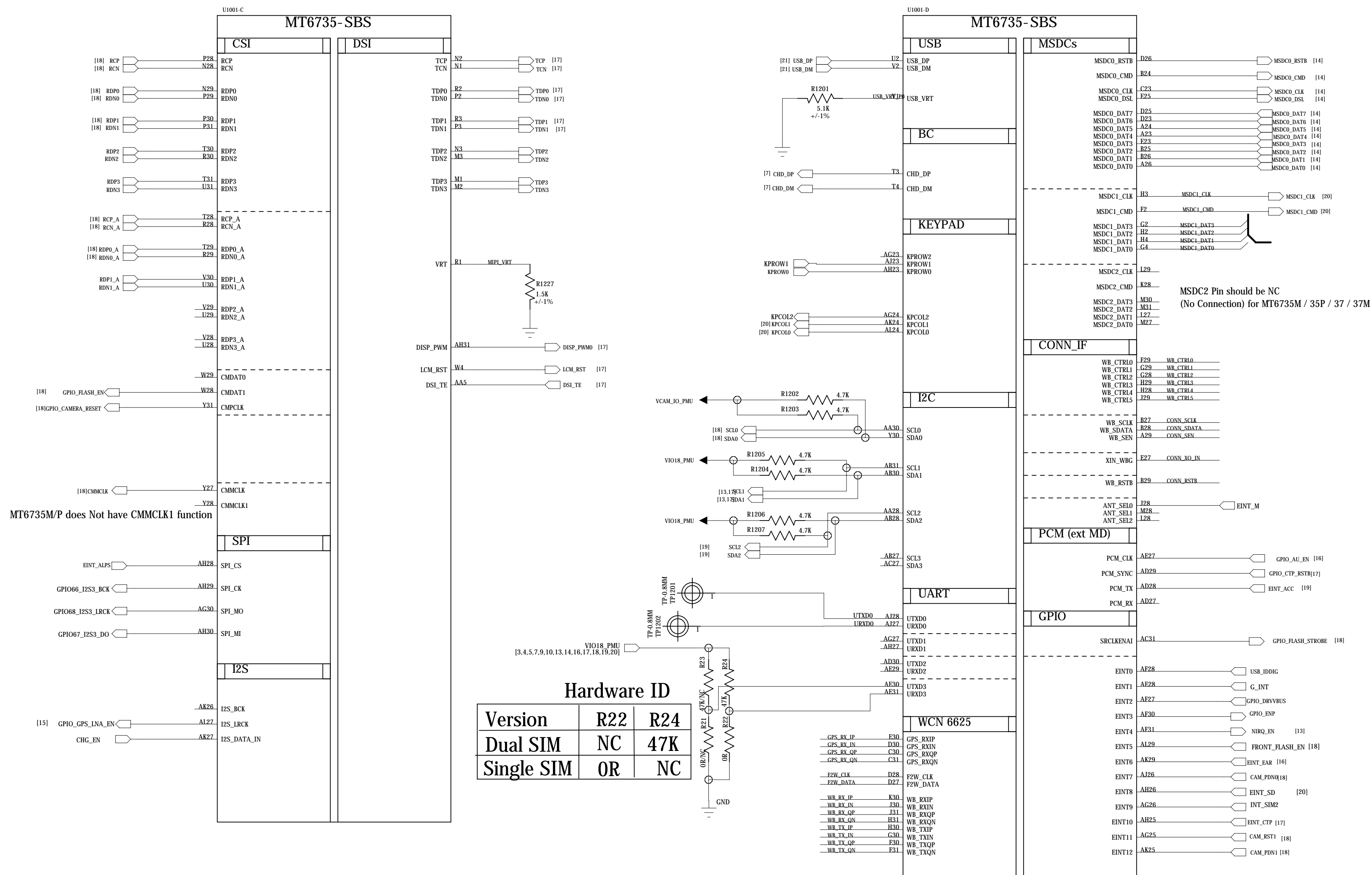


- Schematic design notice of "10\_BB\_POWER" page.
- Note 10-1: 4 mil GND trace with good shielding to PMIC (Differential)
- Note 10-3: FSOURCE\_P(EFUSE)  
(1)FSOURCE\_P EFUSE power(VEFUSE) should be only for EFUSE usage(not share with other application)  
(2)W/I EFUSE program, VEFUSE need 1uF bypass cap (pls refer to iSLDO output voltage/current table;)"  
(3)W/O EFUSE program, VEFUSE bypass cap should be NC.

## MT6737M

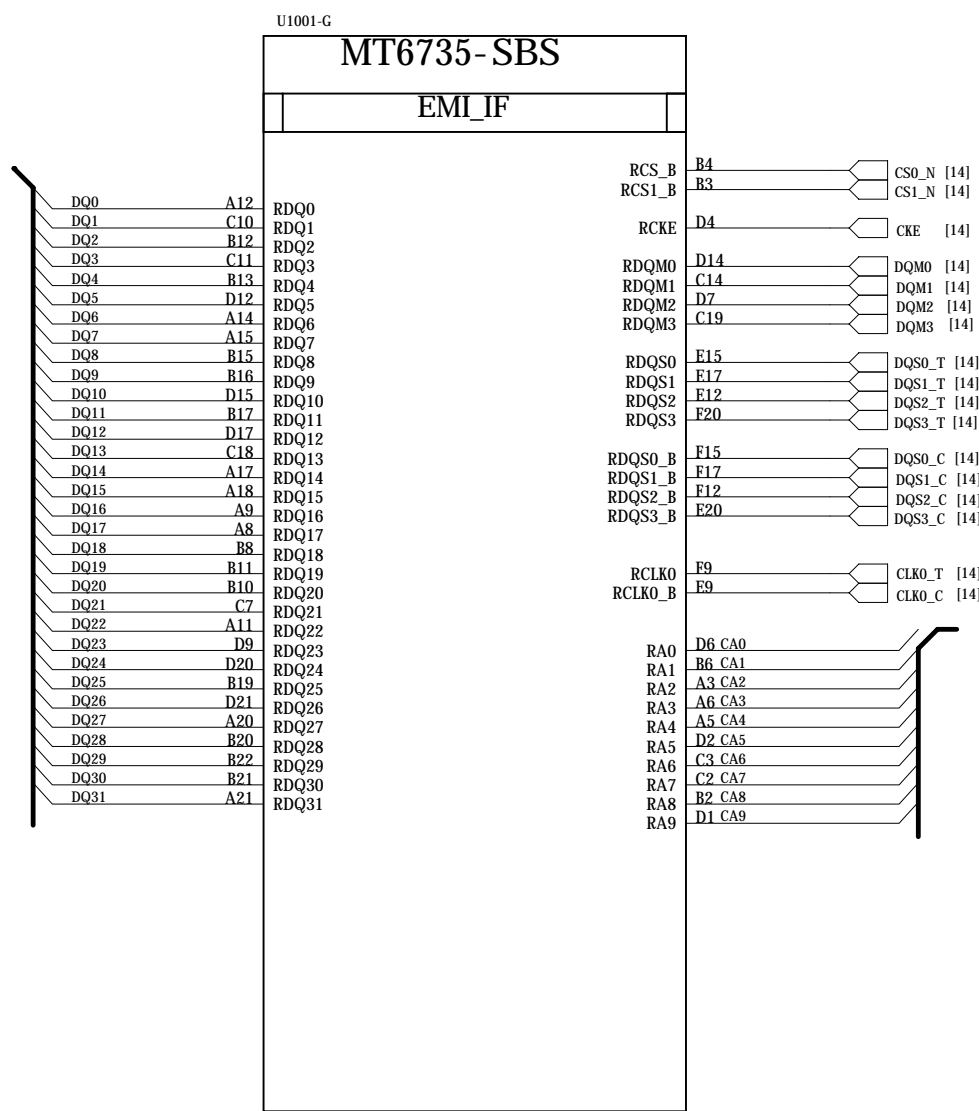


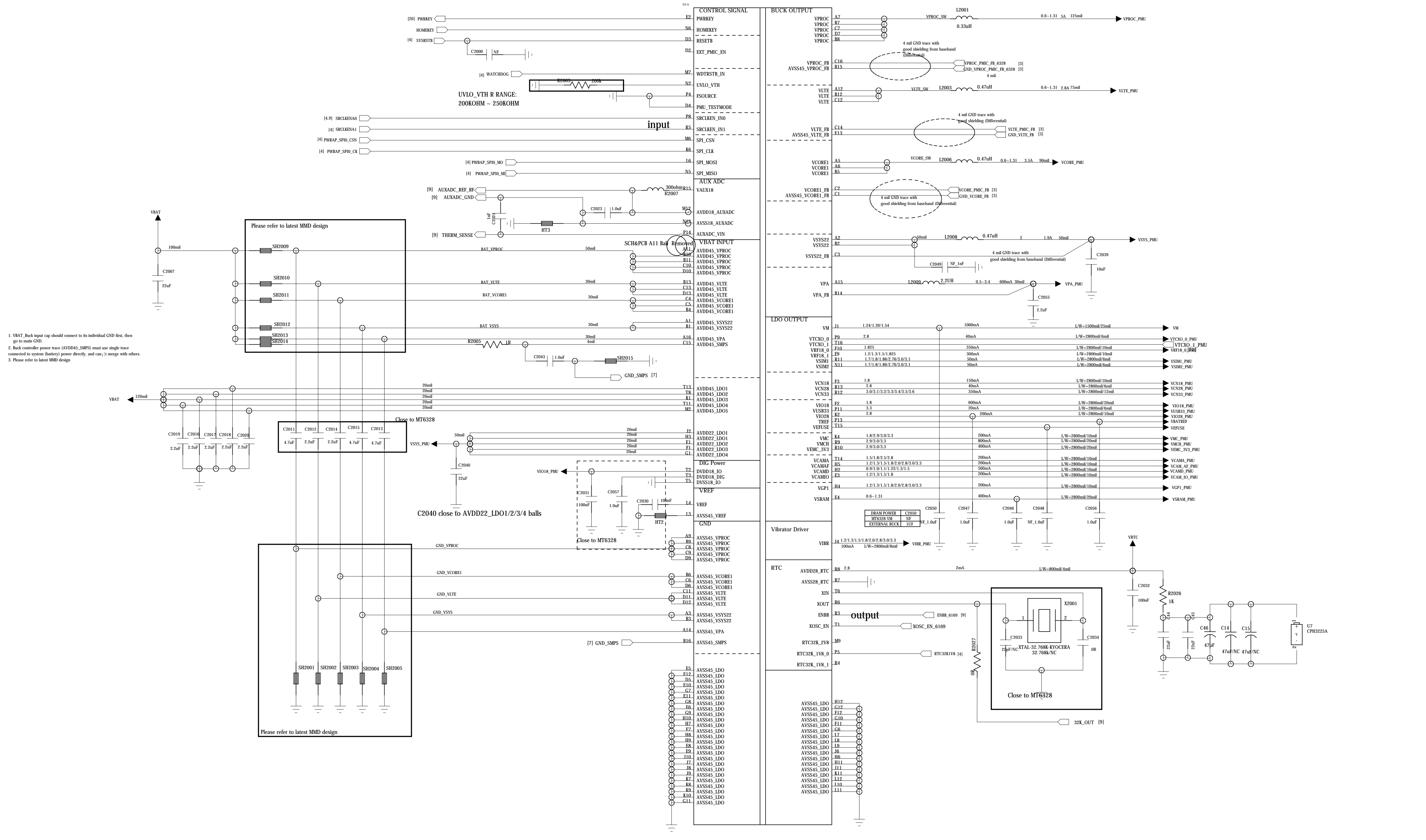
## MT6737M



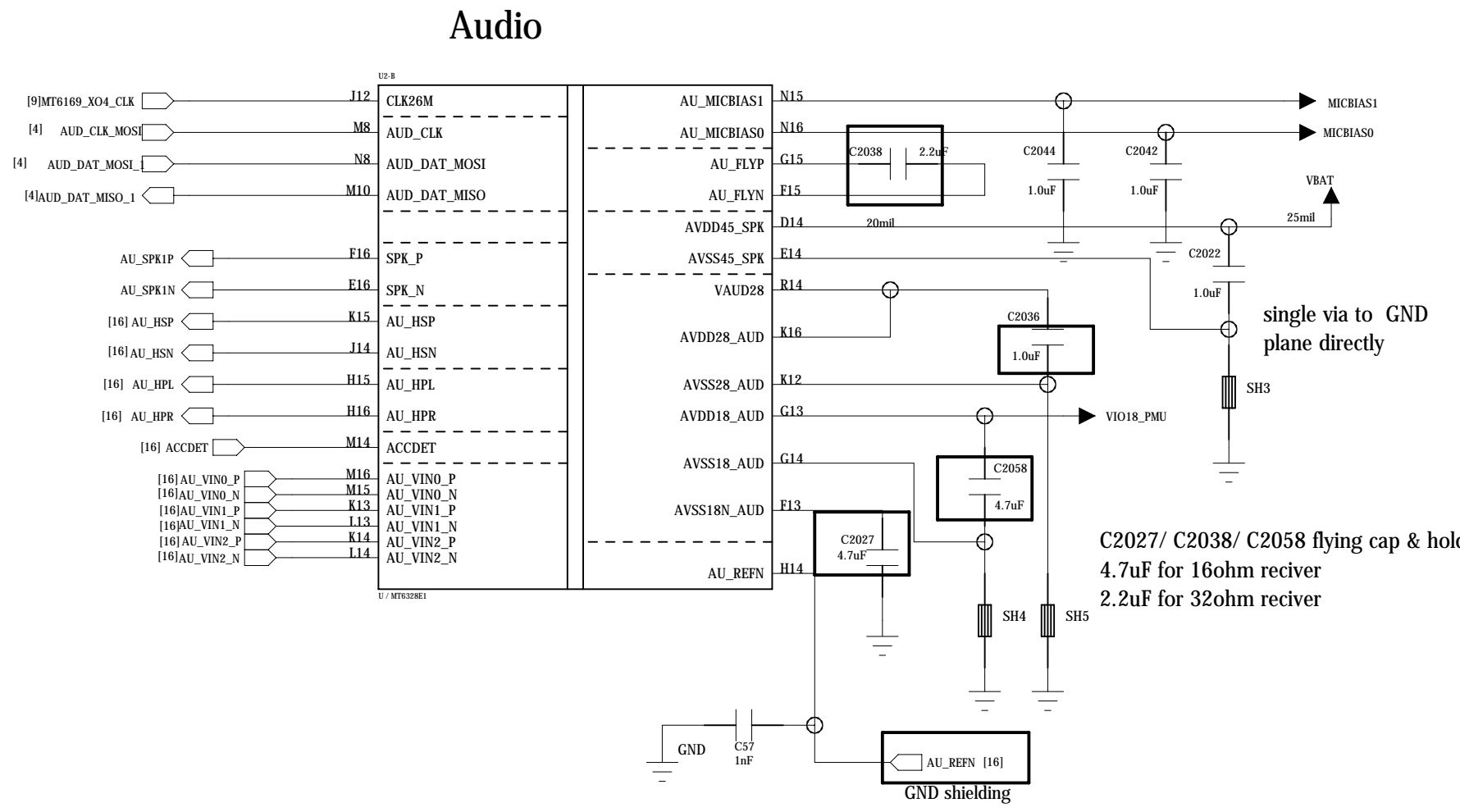
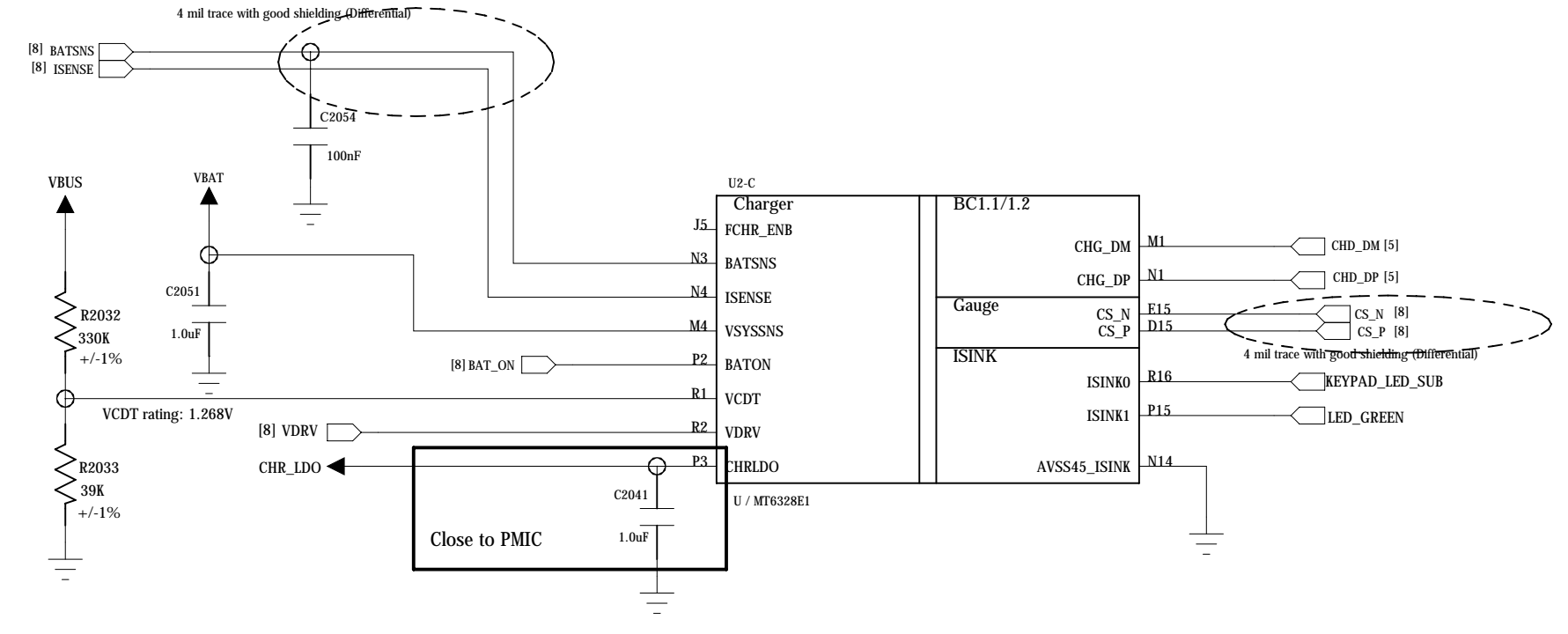
Hardware ID		
Version	R22	R24
Dual SIM	NC	47K
Single SIM	0R	NC

MT6737M





- 1. VBAT Buck input cap should connect to its individual GND first, then go to main GND.
- 2. Buck controller power trace (AVSS43\_SMP5) must use single trace connected to system (battery) power directly, and can't merge with others.
- 3. Please refer to latest MMD design.

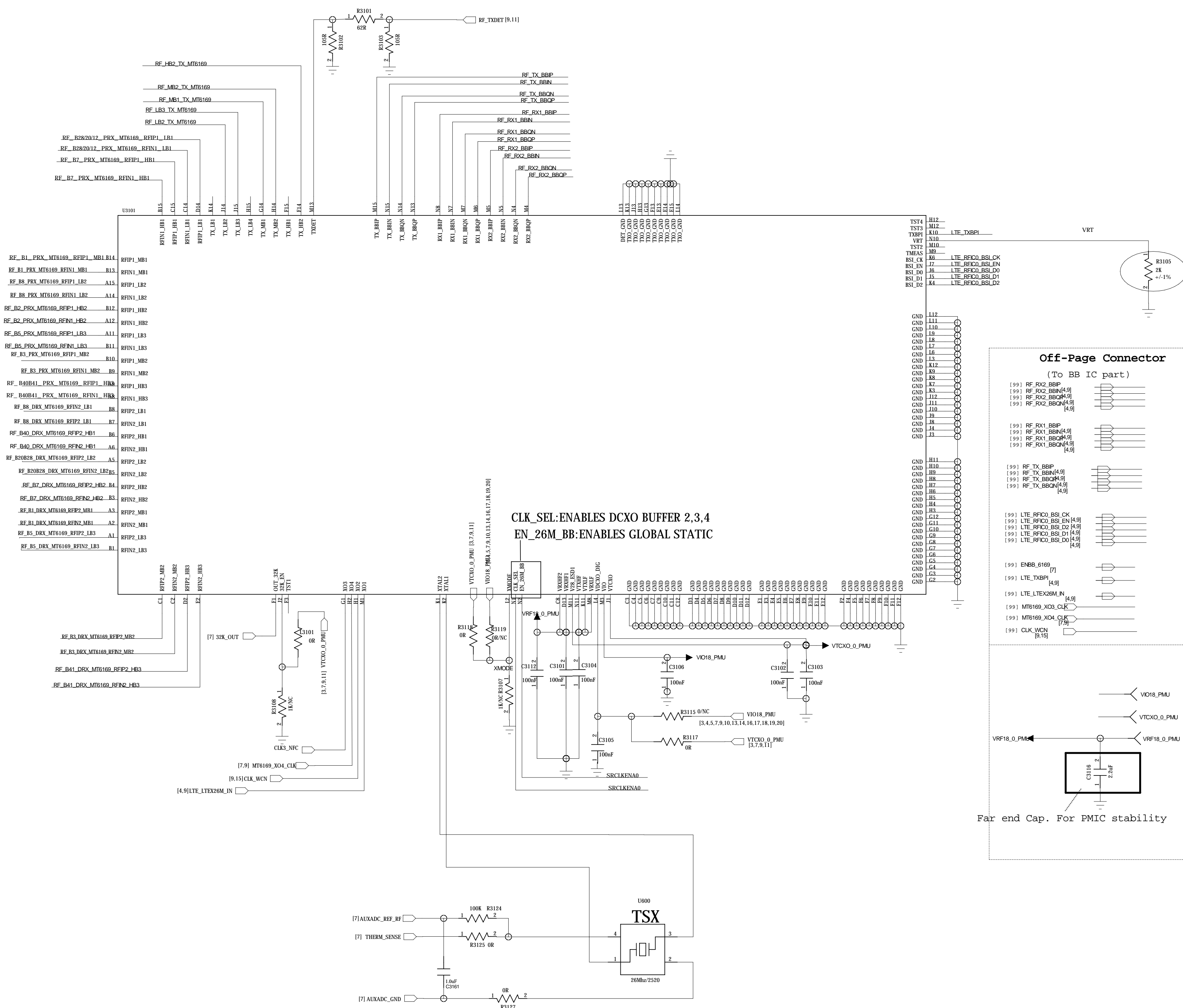


To improve noise level, connect to audio jack first, and then connect to GND

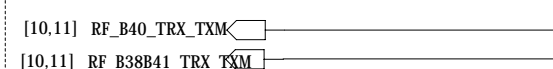
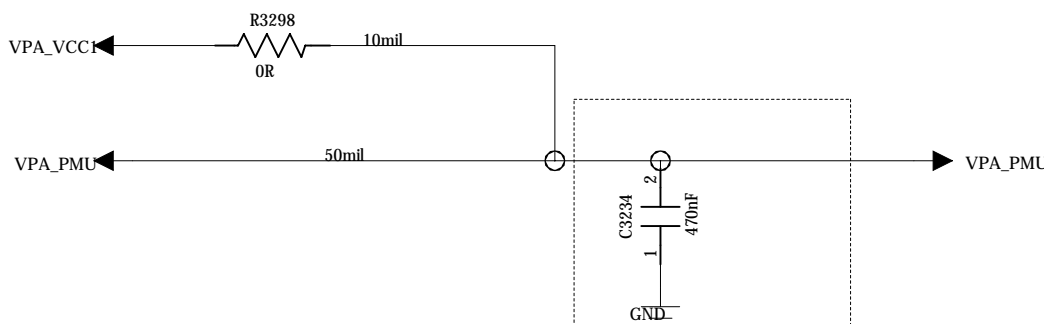
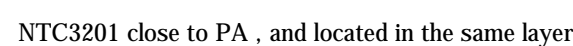
TITLE	<TITLE>	REV	<REV>
DOCUMENT NO.	20_POWER_MT6328	SIZED	A1
DEPARTMENT	Hardware DEPT.		
COMPANY	WINGTEC		
DESIGNER	<DESIGNER>	Last Saved Date	2017/1/16/PC
SHEET	7	OF	21



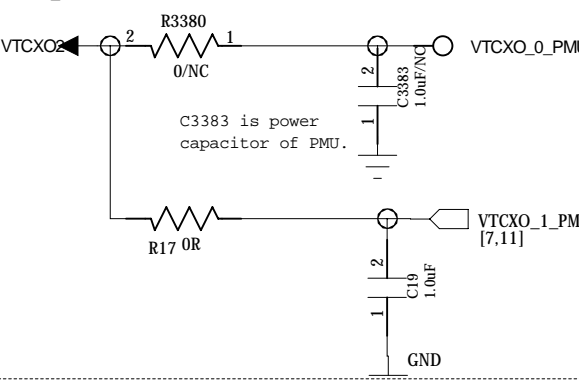
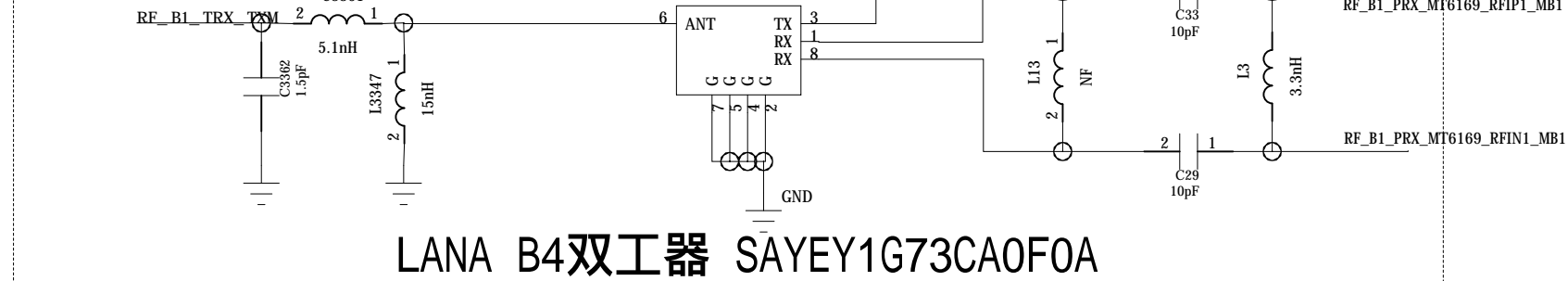
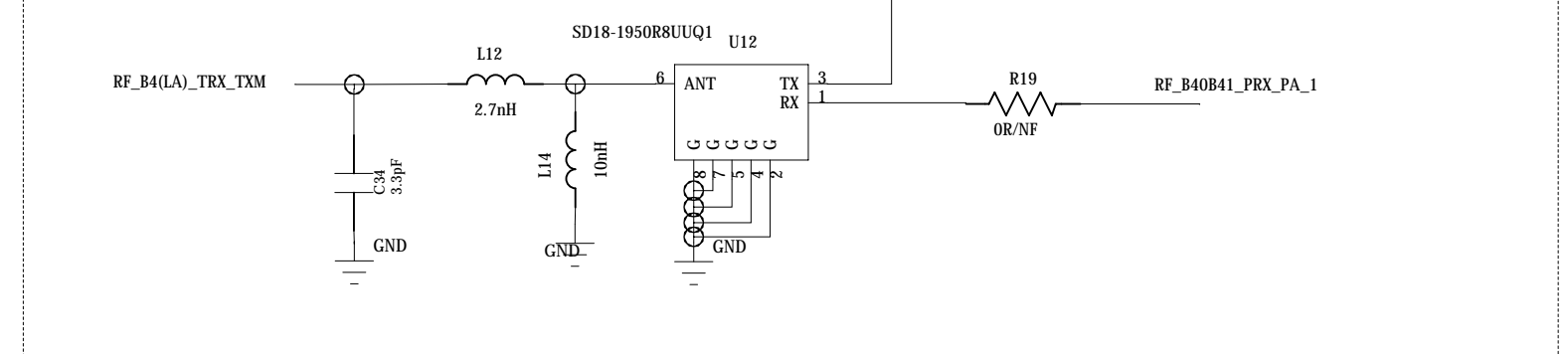
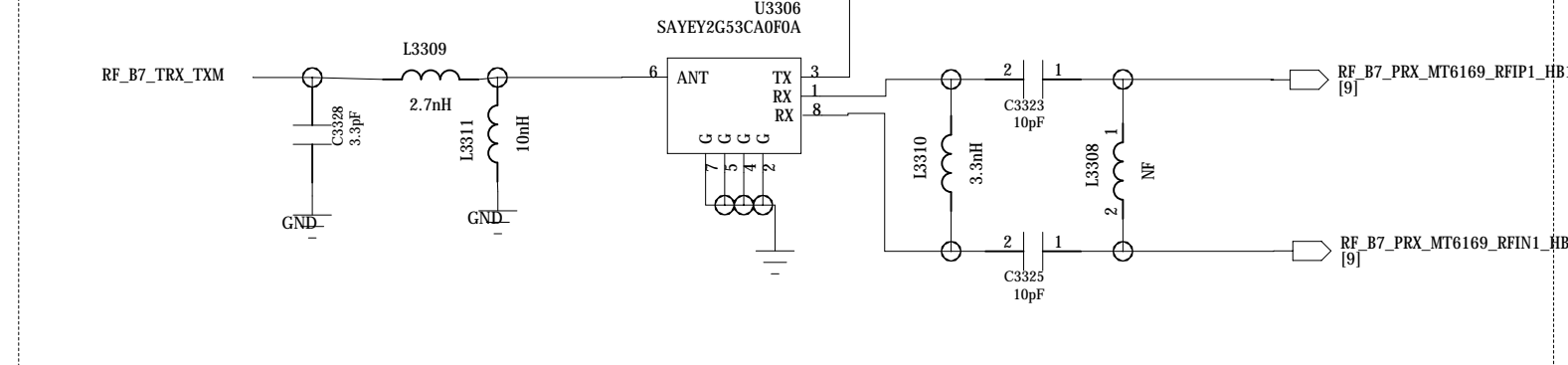
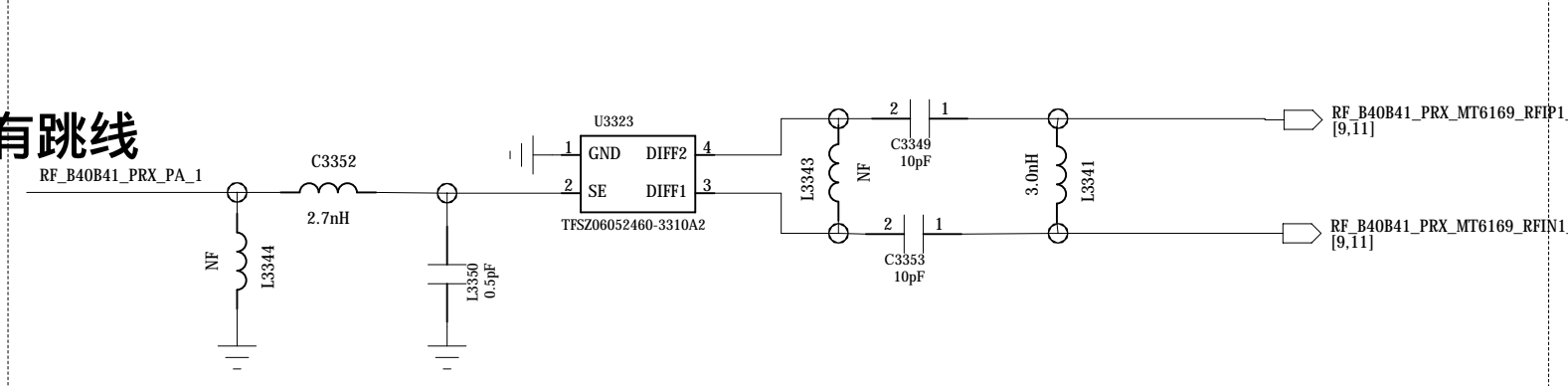
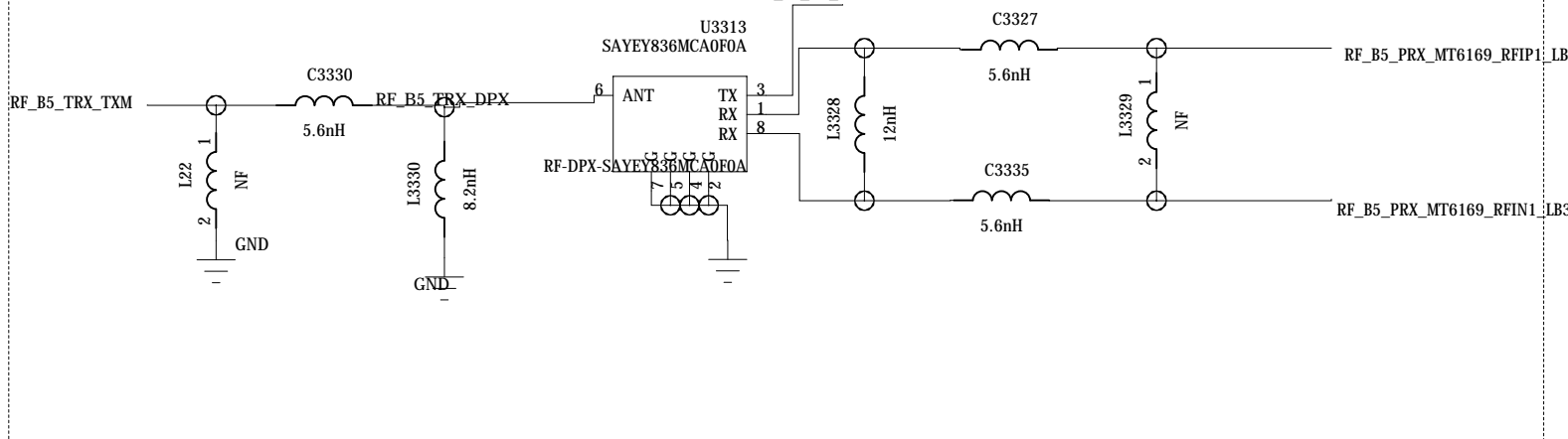
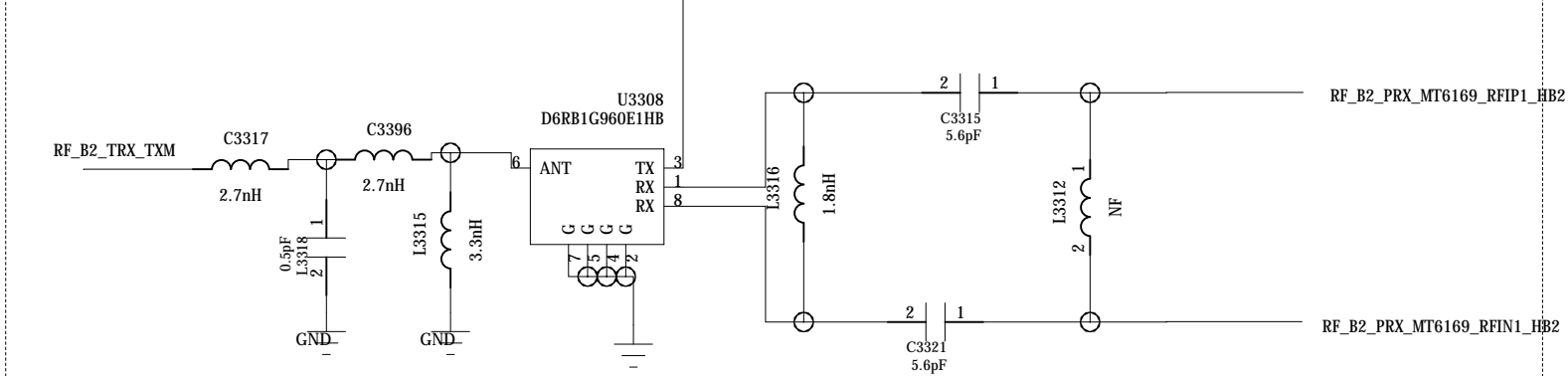
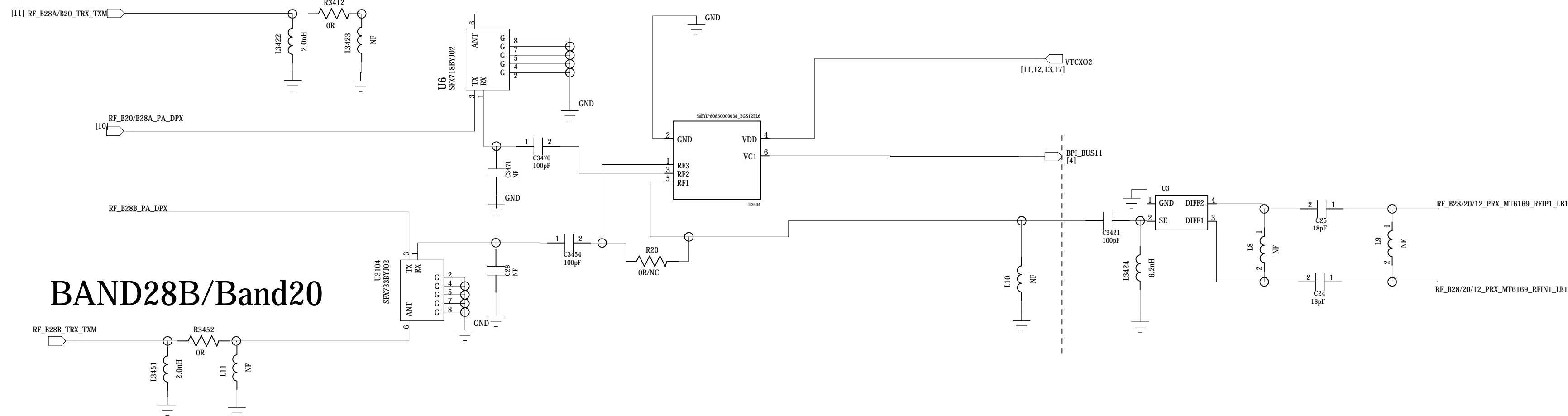
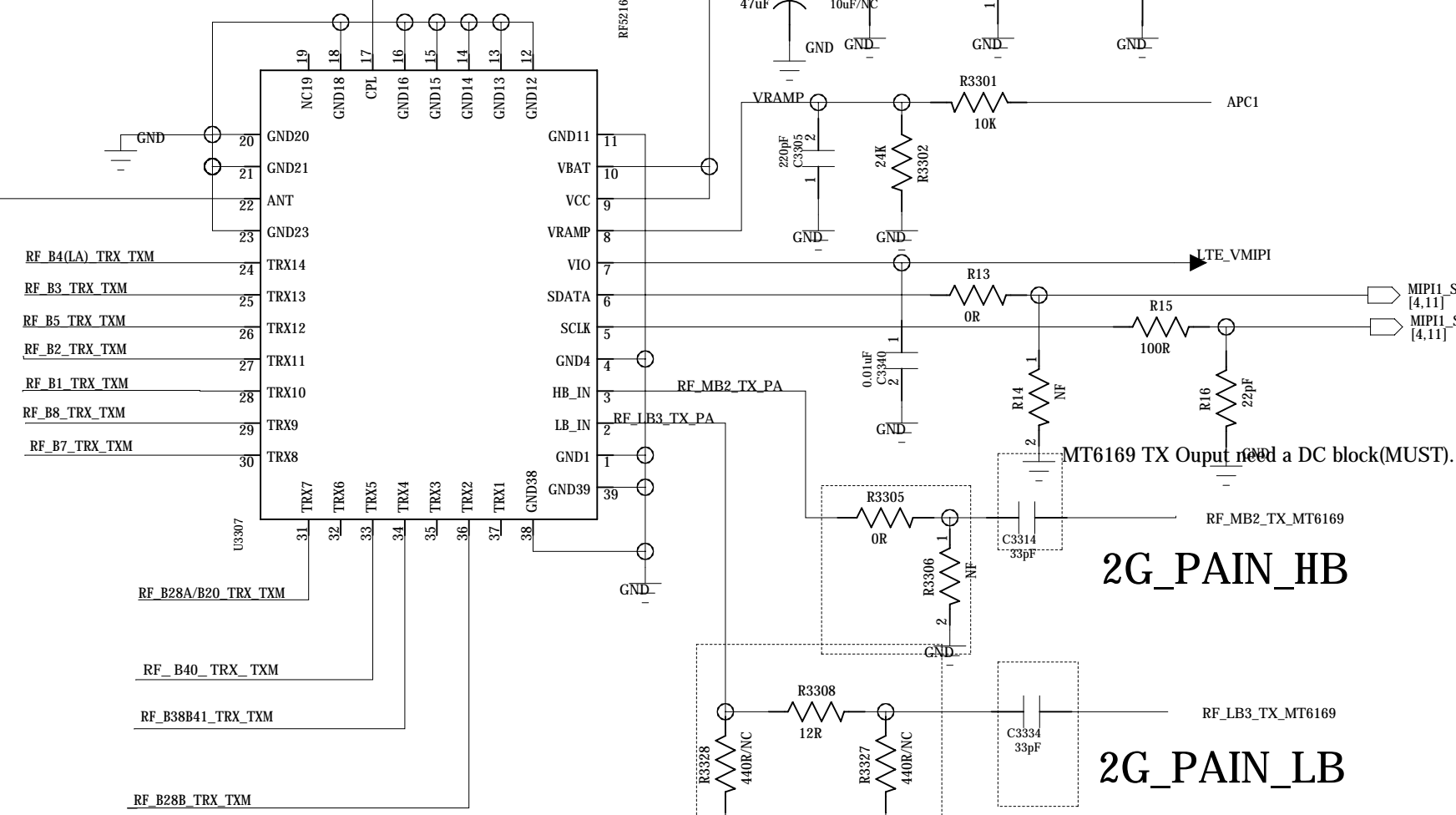
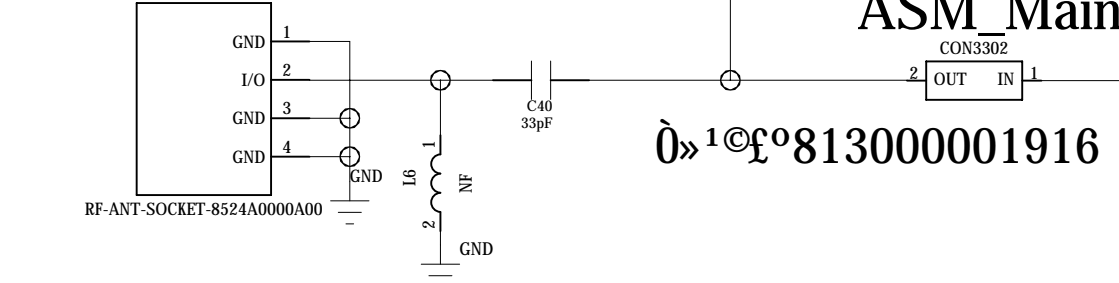




Clock Scheme	32K Crystal Component				32K_EN			XMODE			VDDCO_DIG			VCTCXO / TSX Component								MT6328_AuxADC			VCTXO2 Power			
	R2027	C2033	C2034	X2001	R3116	L3101	R3108	R3119	R3118	R3107	R3115	R3117	R3114	R3126	R3124	R3125	R3127	X3102	U3103	C3113	C3114	C3115	C3161	C2024	C2023	R2007	VCTXO2 Power Connection	
VCTXO + 32K Exis1	NC	22pF	22pF	32K X'tal	NC	NC	1K	NC	NC	1K	0R	NC	0R	0R	NC	NC	NC	NC	VCTXO	100nF	100nF	NC	NC	NC	0R	1uF	0R	Connect to VCTXO_0_PMU
TSX + 32K Exis1	NC	22pF	22pF	32K X'tal	NC	NC	1K	0R	NC	NC	0R	NC	NC	NC	100K	0R	0R	TSX	NC	NC	NC	NC	NC	1nF	1uF	Bead	Connect to VCTXO_0_PMU	
TSX + 32K Less	0R	NC	NC	NC	NC	0R	NC	NC	0R	NC	0R	NC	NC	NC	100K	0R	0R	TSX	NC	NC	NC	NC	NC	1nF	1uF	Bead	Connect to VCTXO_1_PMU	



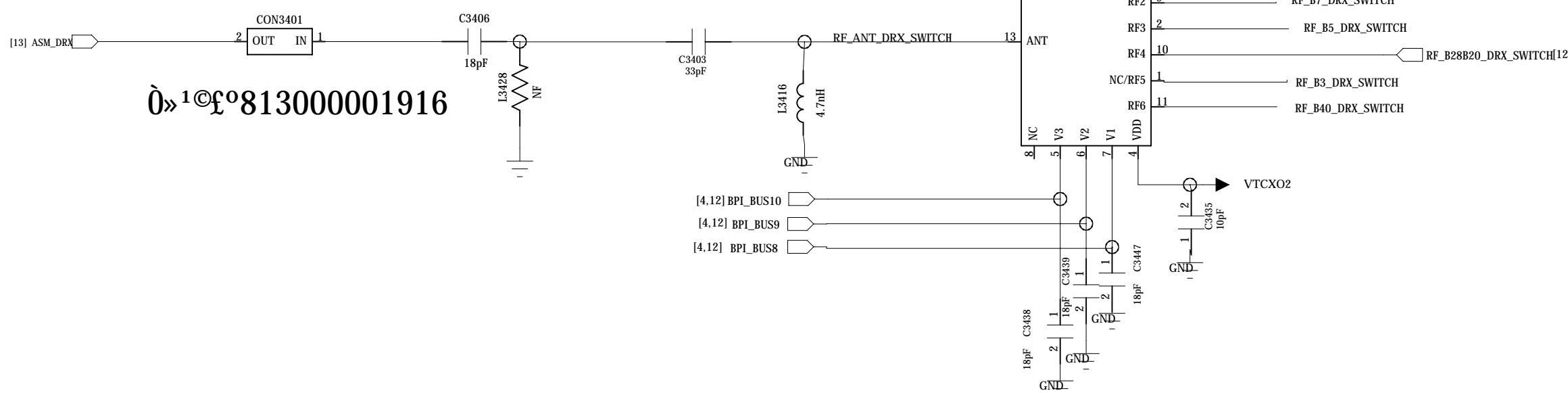
TITLE:	<TITLE>		REV:	<REV>
DOCUMENT NO.:	32_RF_MT6169_RF_TX		SIZED:	A1
DEPARTMENT:	Hardware DEPT.			
COMPANY:				
DESIGNER:	<DESIGNER>	Last Saved Date:	2017/1/16/RC/RD	SHEET: 10 OF 21



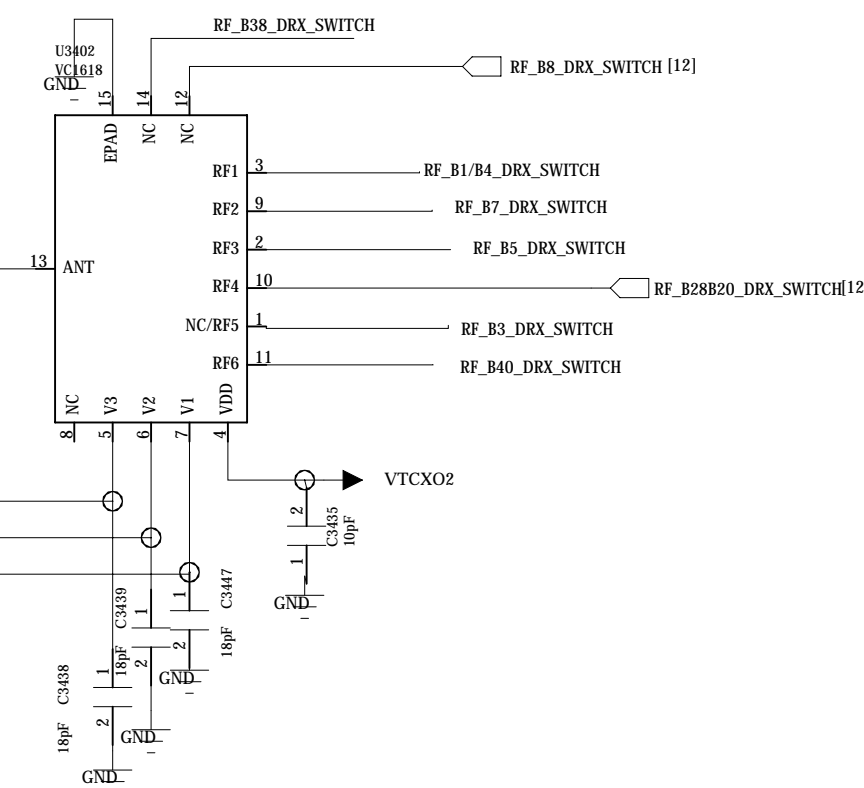
TITLE:	<TITLE>		REV:	<REV>
DOCUMENT NO.:	33_RF_MT6169_RF_PRX		SIZED:	A1
DEPARTMENT:	Hardware DEPT.			
COMPANY:				
DESIGNER:	<DESIGNER>	Last Saved Date:	2017/1/16/RC/RO	
			SHEET:	11 OF 21

DRX ANT: 704~2690MHz

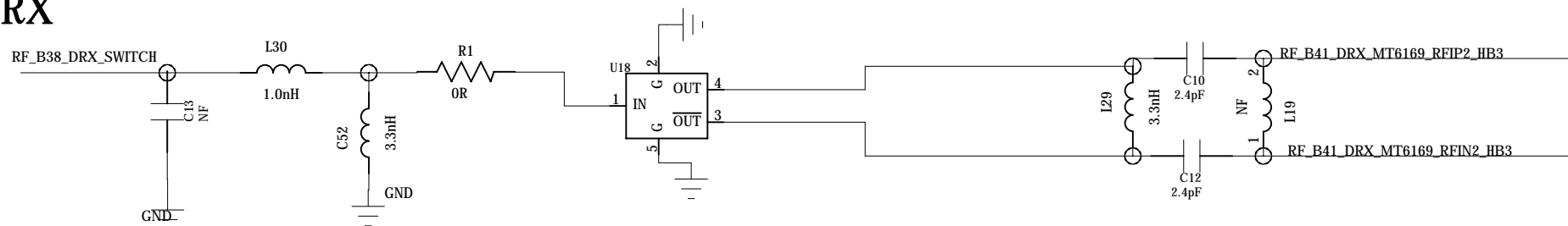
## DRX Car Kit



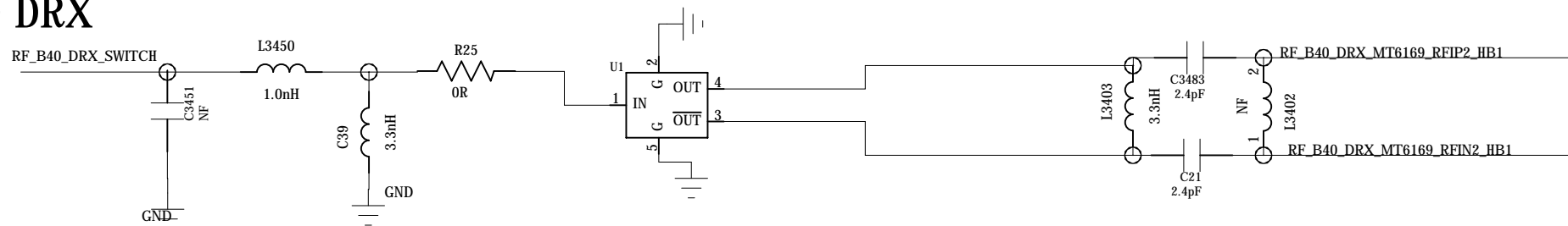
## SP8T



## B38 DRX

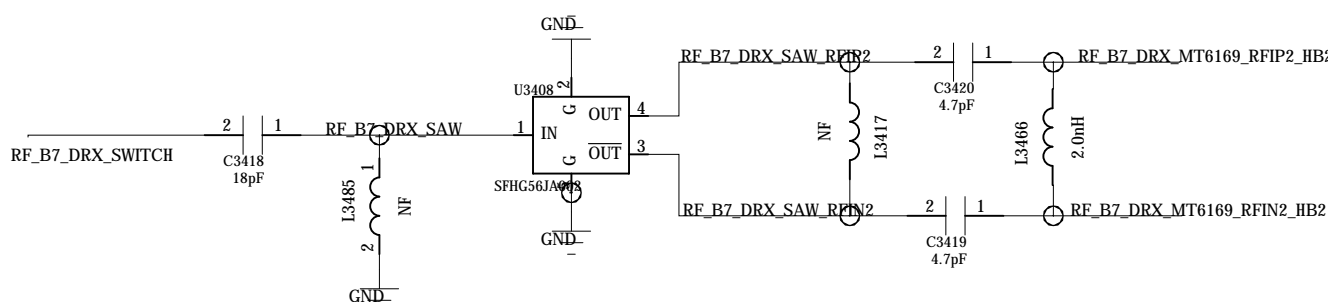


## B40 DRX

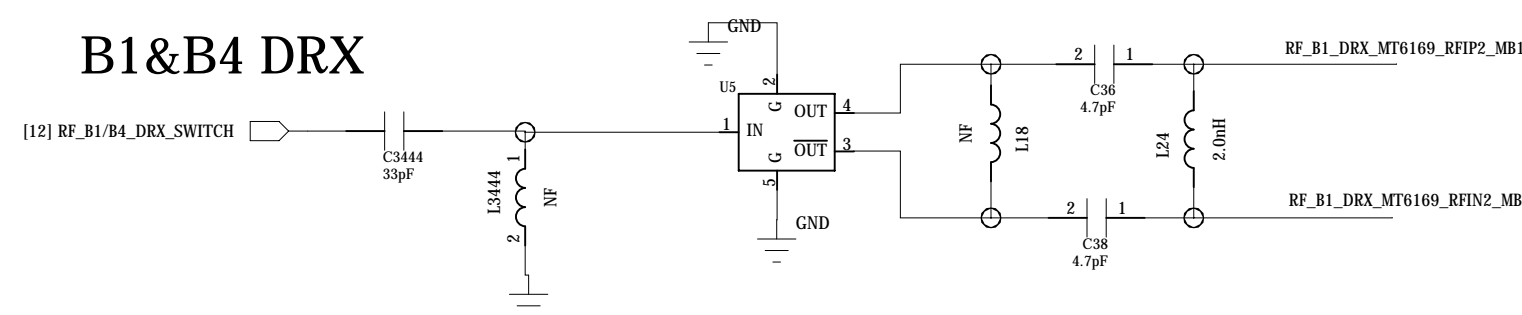


B40 for india B2 for LA DRX

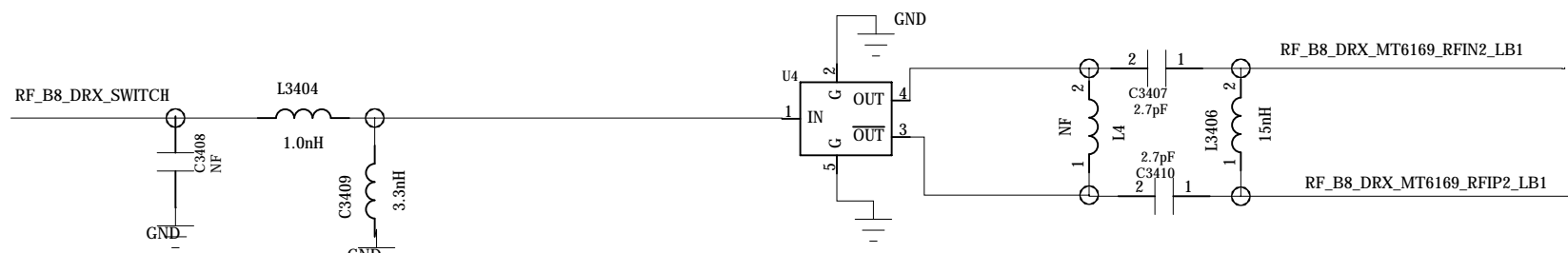
## B7 DRX



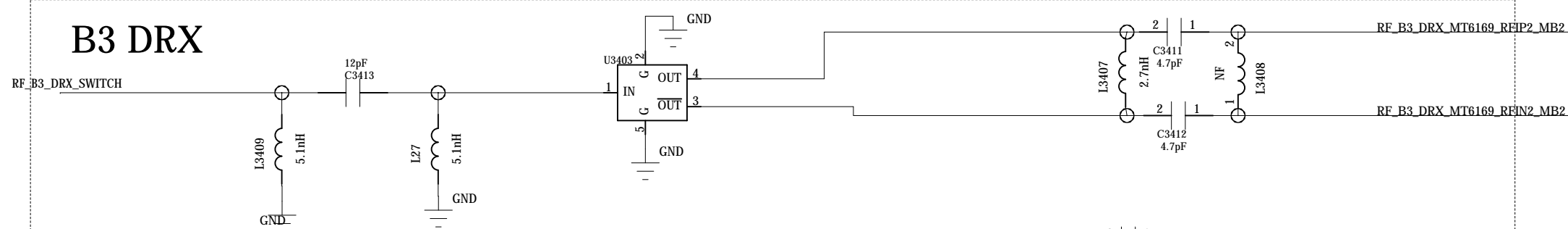
## B1&amp;B4 DRX



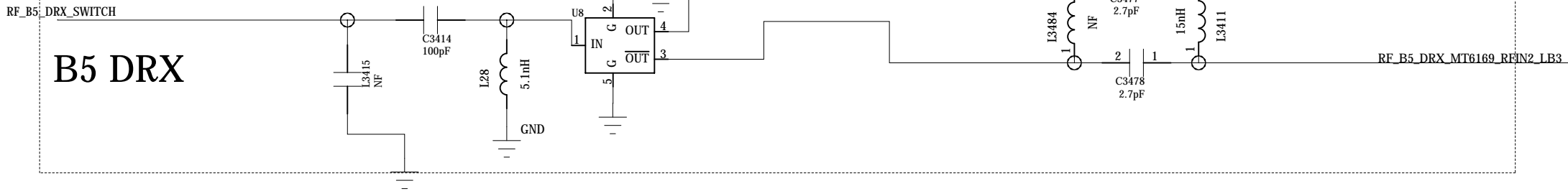
## B8 DRX



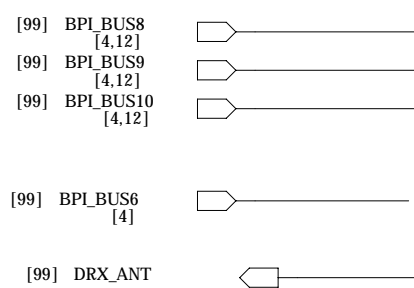
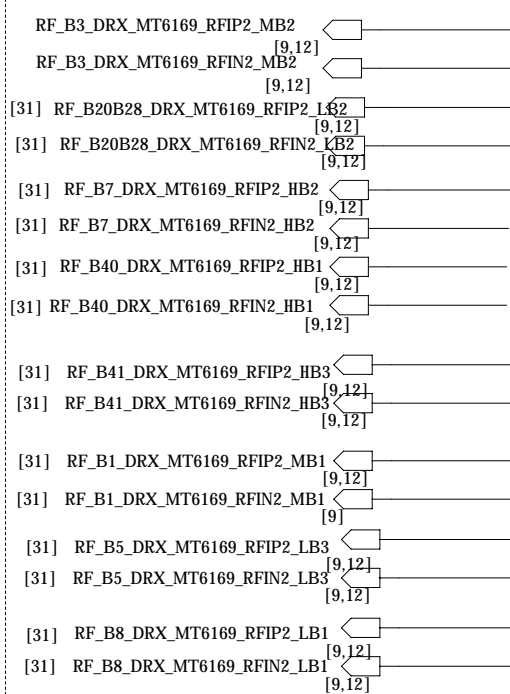
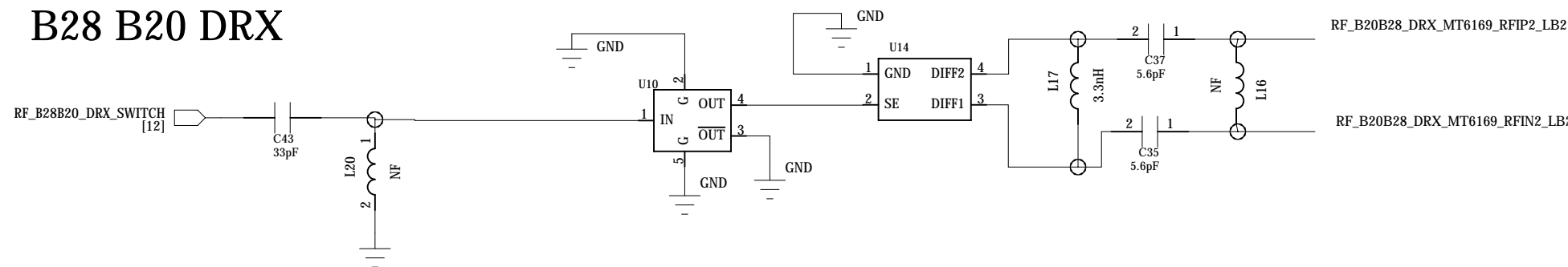
## B3 DRX



## B5 DRX

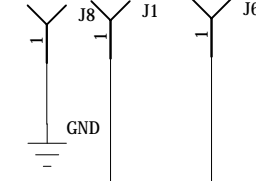


## B28 B20 DRX



Eç<sup>1</sup>ûDRX0»0Đ, ßÆ£-´E13489;E00<sup>2</sup>»0A0ꝞAô;

DRX ANT: 734~960MHz + 1805~2690MHz





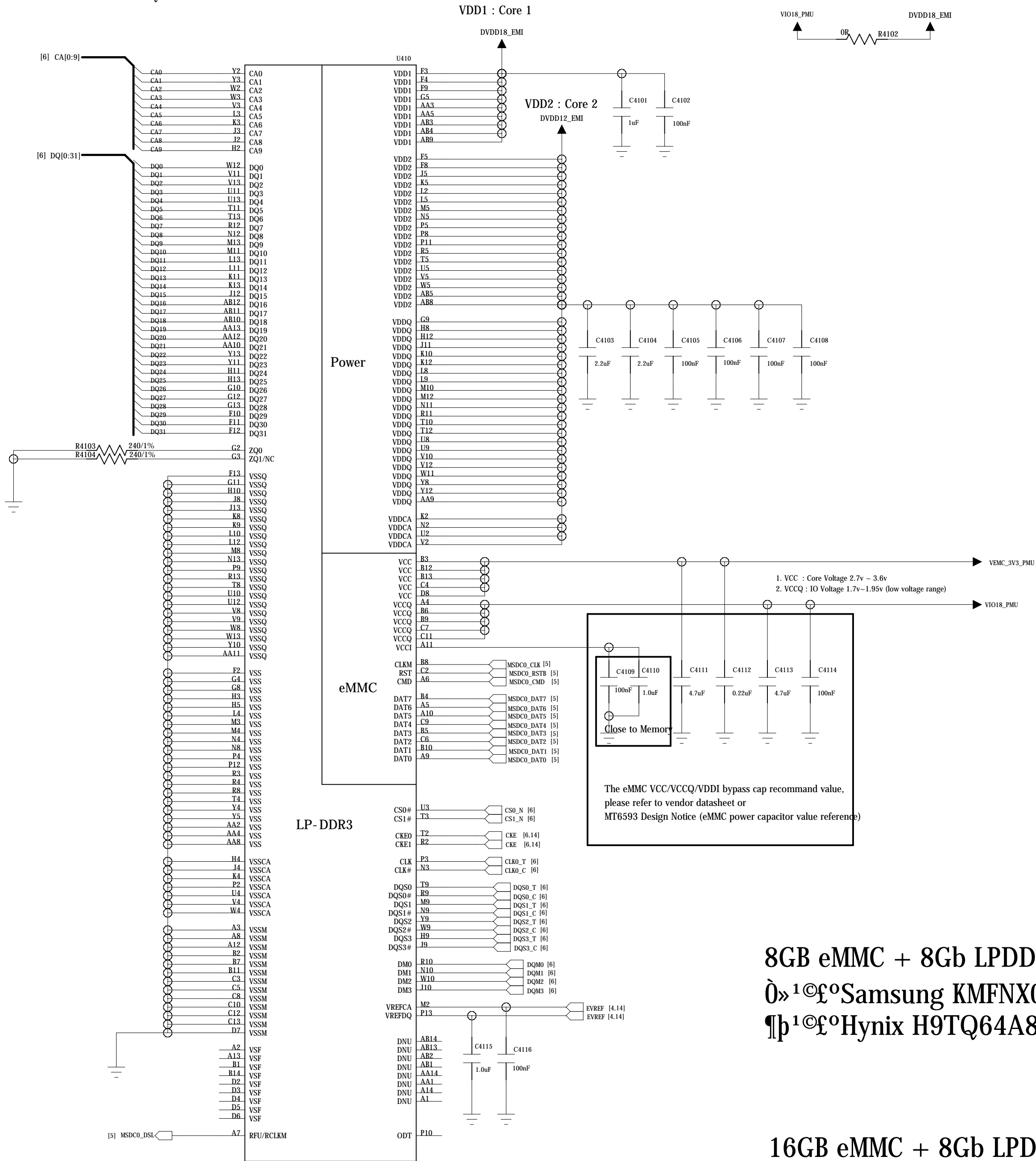
Connect to AP			
DQ[0..31]		DQ[0..31]	
CA[0..9]		CA[0..9]	
CS0_N		CS0_N	
CS1_N		CS1_N	
CKE		CKE	
DQM0		DQM0	
DQM1		DQM1	
DQM2		DQM2	
DQM3		DQM3	
DQS0_C		DQS0_C	
DQS1_C		DQS1_C	
DQS2_C		DQS2_C	
DQS3_C		DQS3_C	
DQS0_T		DQS0_T	
DQS1_T		DQS1_T	
DQS2_T		DQS2_T	
DQS3_T		DQS3_T	
CLK0_T		CLK0_T	
CLK0_C		CLK0_C	
VREF_CA		VREF_CA	
VREF_DQ		VREF_DQ	
MSDC0_RSTB		MSDC0_RSTB	
MSDC0_CMD		MSDC0_CMD	
MSDC0_CLK		MSDC0_CLK	
MSDC0_DSL		MSDC0_DSL	
MSDC0_DAT0		MSDC0_DAT0	
MSDC0_DAT1		MSDC0_DAT1	
MSDC0_DAT2		MSDC0_DAT2	
MSDC0_DAT3		MSDC0_DAT3	
MSDC0_DAT4		MSDC0_DAT4	
MSDC0_DAT5		MSDC0_DAT5	
MSDC0_DAT6		MSDC0_DAT6	
MSDC0_DAT7		MSDC0_DAT7	

Power I/F			
VIO18_PMU		VIO18_PMU	
VEMC_3V3_PMU		VEMC_3V3_PMU	
DVDD12_EMI		DVDD12_EMI	

eMMC+LPDDR3

221 Ball, 0.5mm pitch

VDD1=1.8V  
VDD2=1.20V  
VDDCA=1.2V  
VDDQ= 1.20V



8GB eMMC + 8Gb LPDDR3

0»¹©ƒ°Samsung KMFNX0012M-B214 806700000431

¶p¹©ƒ°Hynix H9TQ64A8GTBCUR-KUM

16GB eMMC + 8Gb LPDDR3

0»¹©ƒ°Samsung KMFE10012M-B214 806700000291

¶p¹©ƒ°Hynix H9TQ17A8GTACUR-KUM

TITLE:	<TITLE>	REV:	<REV>
DOCUMENT NO.:	41_MEMORY_EMMC_LPDDR3	SIZED:	A1
DEPARTMENT:	Hardware DEPT.		
COMPANY:			
DESIGNER:	<DESIGNER>	Last Saved Date:	2017/1/16/PC/ED
SHEET:	14	OF	21



[illegible]

# Earphone Audio

**MAIN MIC**

Handset Microphone 1

Close to MIC

Close to BB

please change cap

**MIC**

Reserved for ACC mode

together then single via to main GND

### Earphone MICPHONE

Reserved for ACC mode

Close to BB

Close to MIC

Close to CON6001

GND of C6018(4.7uF) and headset should tie together and single via to GND plane

For multi-key accuracy @ Low cost mode

	ACC mode	Low cost mode
C6017	1uF	0 ohm
C6022	1uF	0 ohm
R6009	1K	NC
R6010	1.5K	NC
R6019	NC	2.5K
C6018	4.7uF	0 ohm

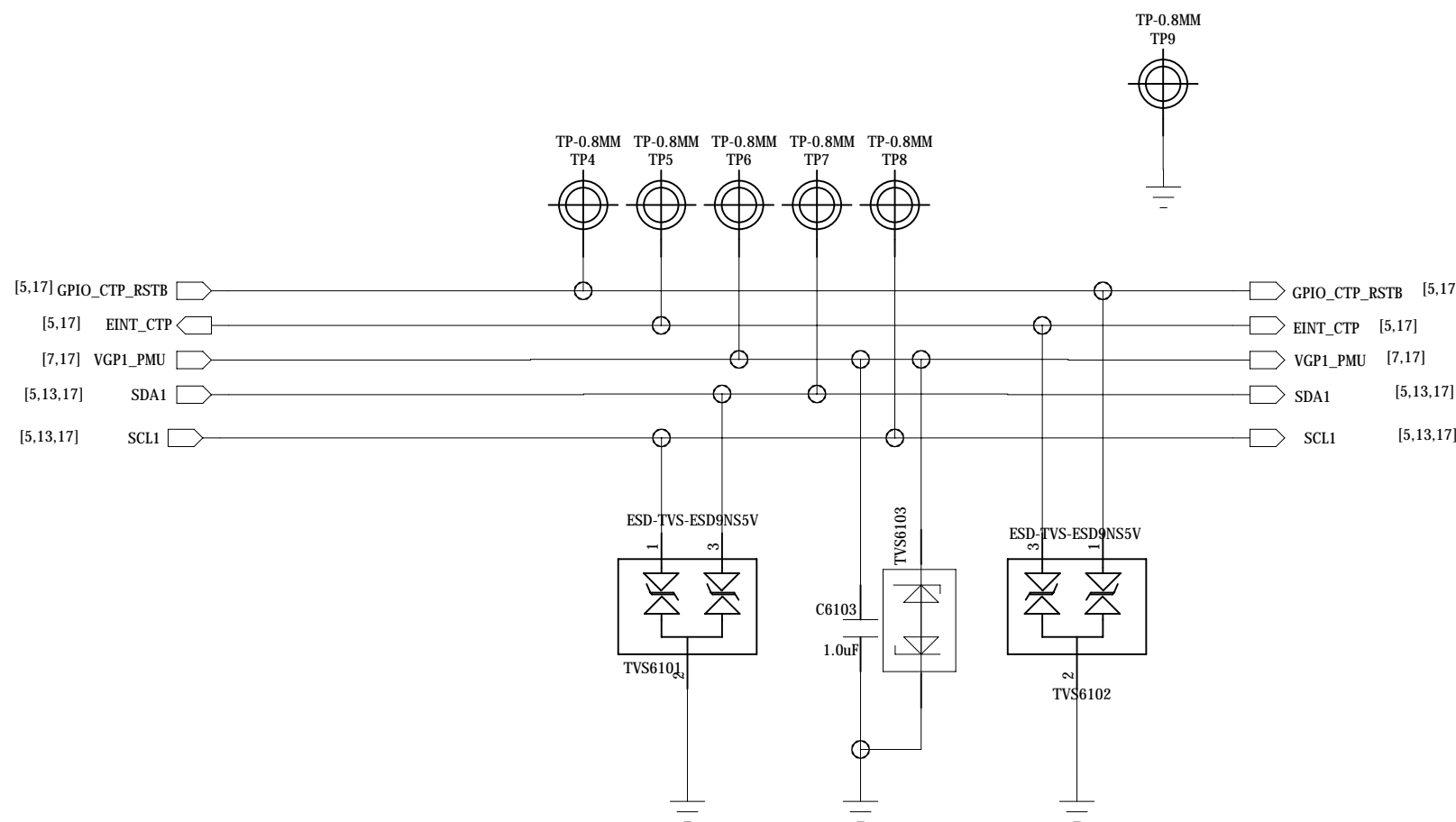
# Audio PA

Schematic design notice of "60_PERL_AUDIO_IO" page.	
Note 60-1:	The equivalent capacitance of audio and speech ESD protection device must be $\leq 330\text{pF}$ . choose bi-directional device only
Note 60-2:	The equivalent capacitance of FM ANT. ESD protection device must be $\leq 1\text{pF}$ .

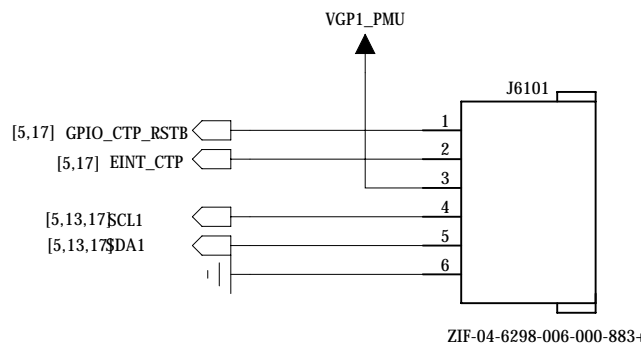
TITLE: <TITLE>		REV: <REV>
DOCUMENT NO.: 60_PERI_AUDIO	SIZED: A1	
DEPARTMENT: Hardware DEPT.		
COMPANY: 		
DESIGNER: <DESIGNER>	Last Saved Date: 2017/1/16/00:00	SHEET: 16 OF 21



CTP



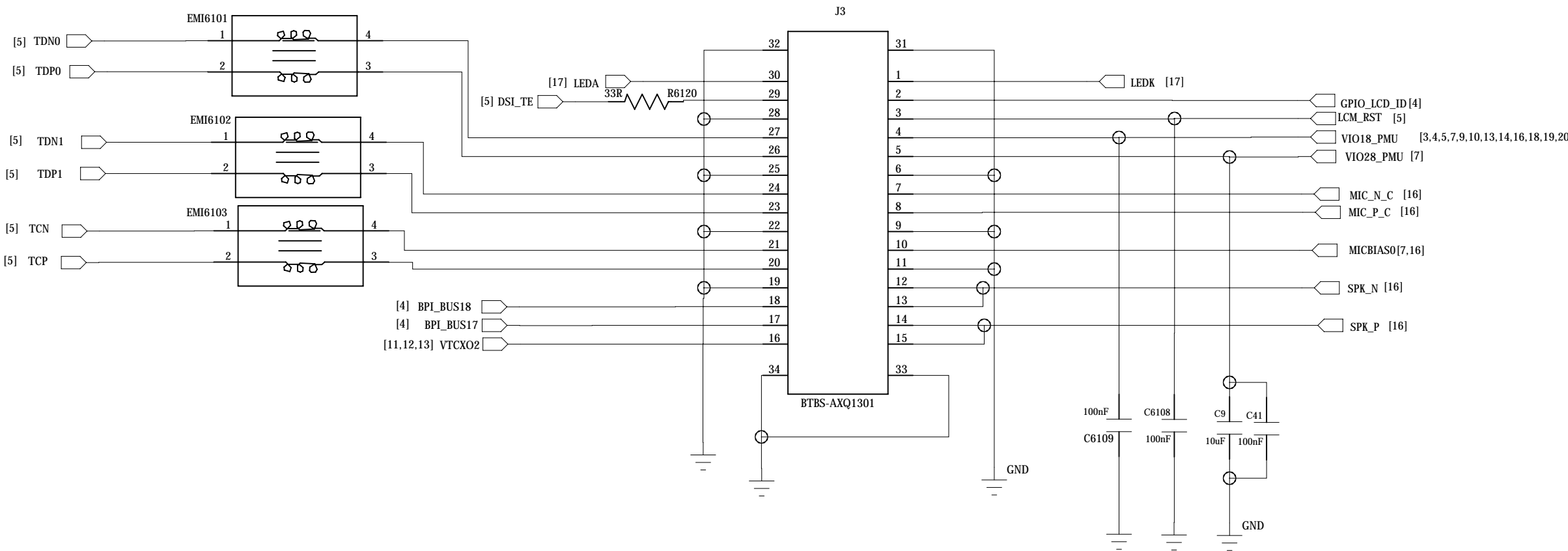
CTP Connector



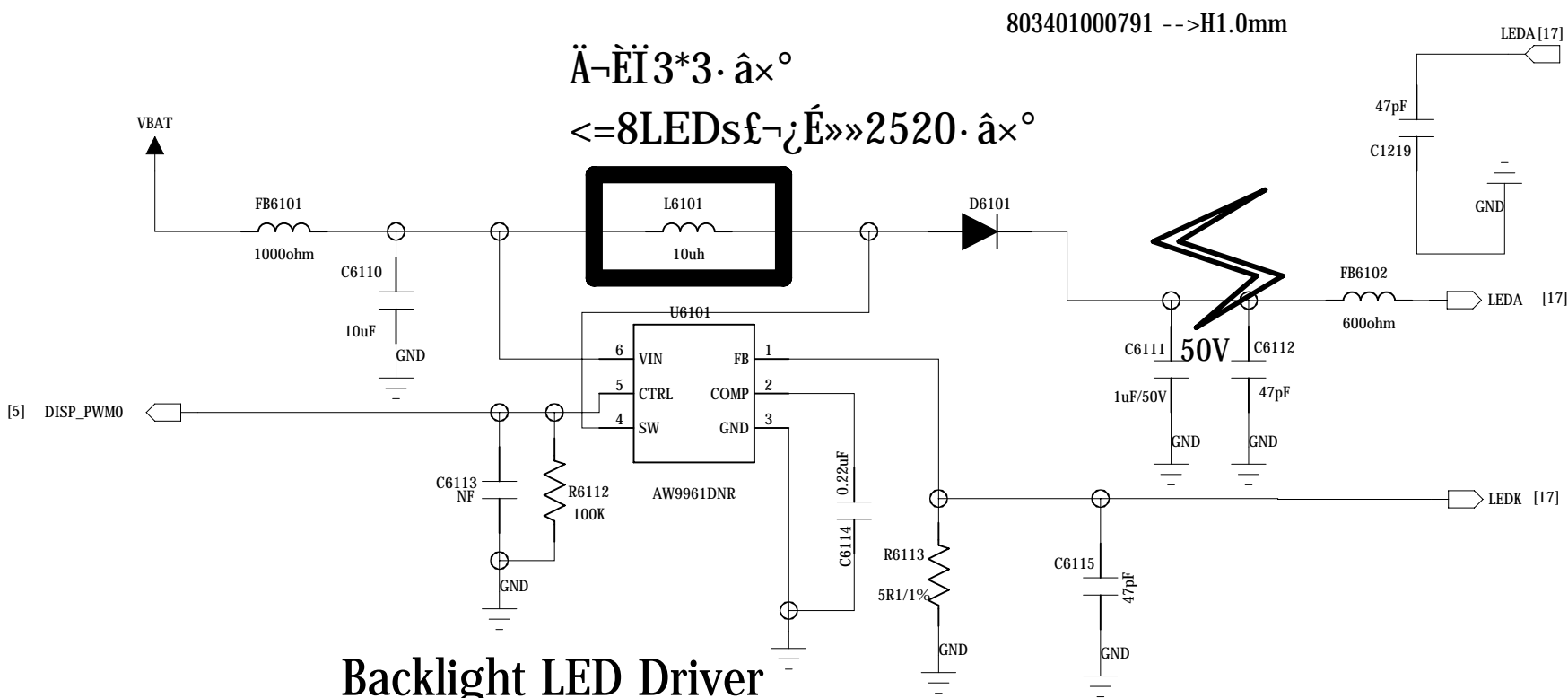
0»¹©£°813200000193

¶p¹©£°813200000192

Main LCM



Backlight LED Driver



0»¹©£°AW9961DNR 807300000551

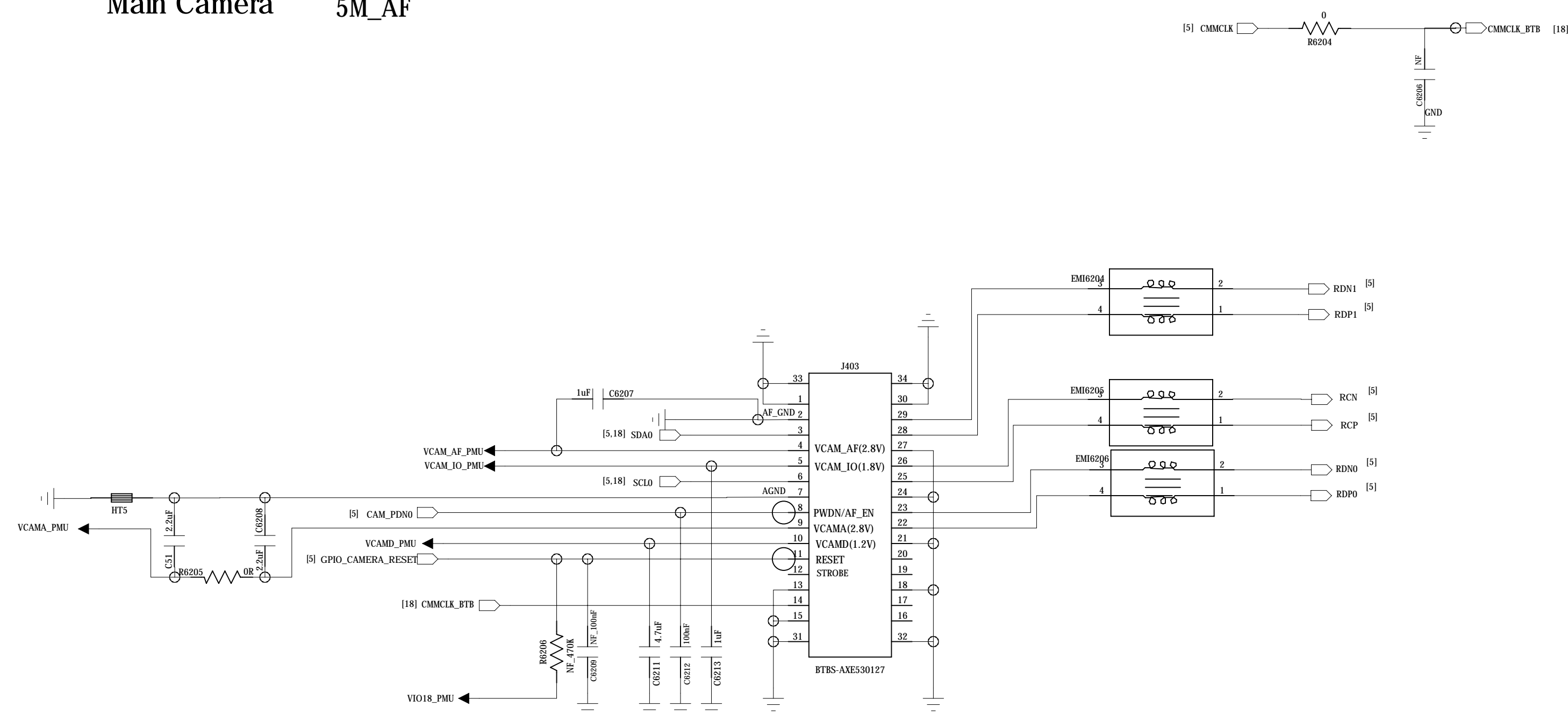
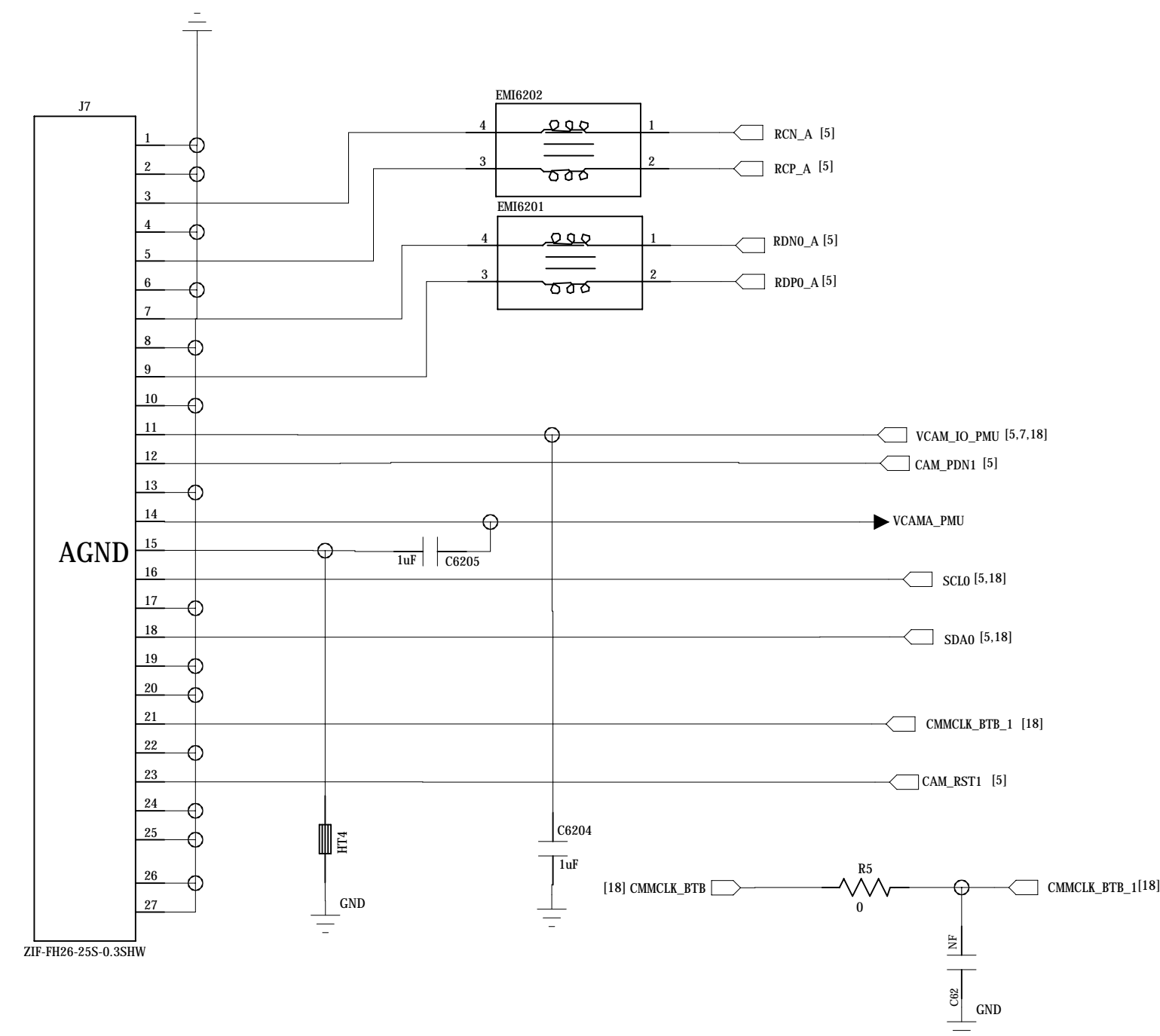
¶p¹©£°SGM3756YTDI6G/TR 807300000651

Schematic design notice of "61\_PERI\_LCD\_CTP" page.

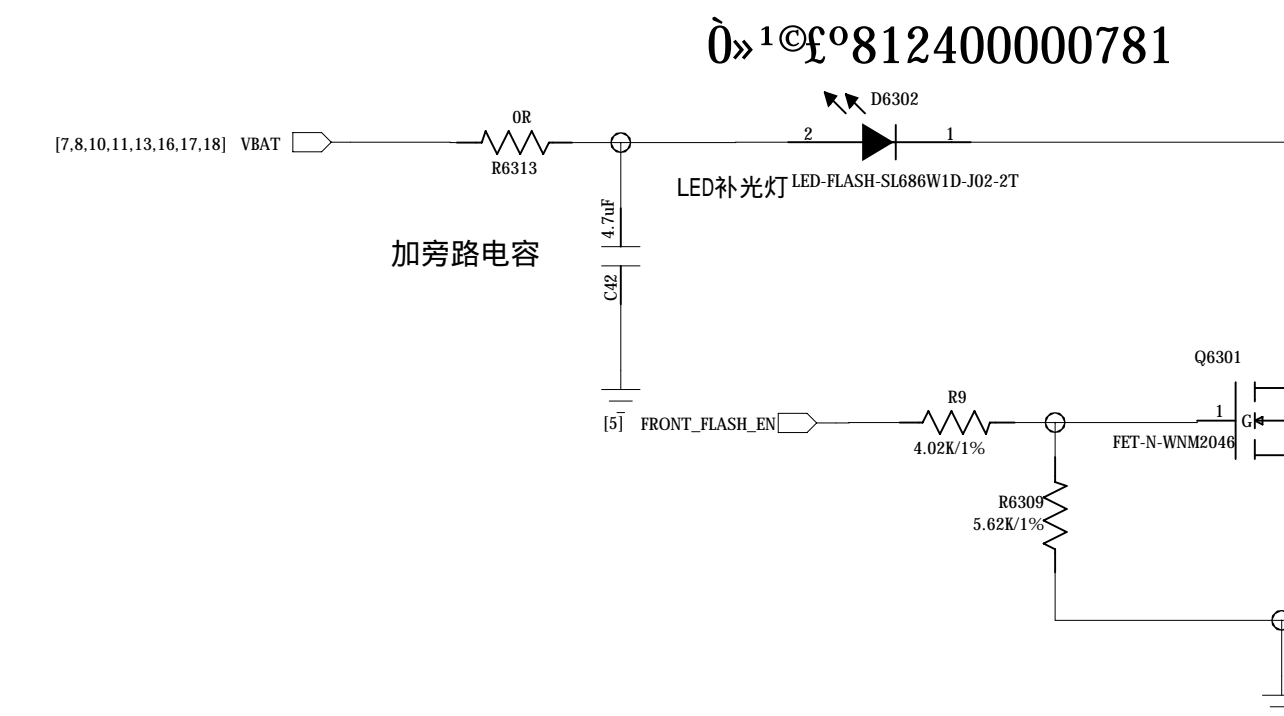
Note 61-1: GT1151 I2C address: 0X5D (Write:0xBA, Read:0xBB) or 0x14 (Write:0x28, Read:0x29)

TITLE:	<TITLE>	REV:	<REV>
DOCUMENT NO.:	61_PERI_LCD/CTP	SIZED:	A1
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINGTEC		
DESIGNER:	<DESIGNER>	Last Saved Date:	2017/1/16/PC
SHEET:	17	OF	21

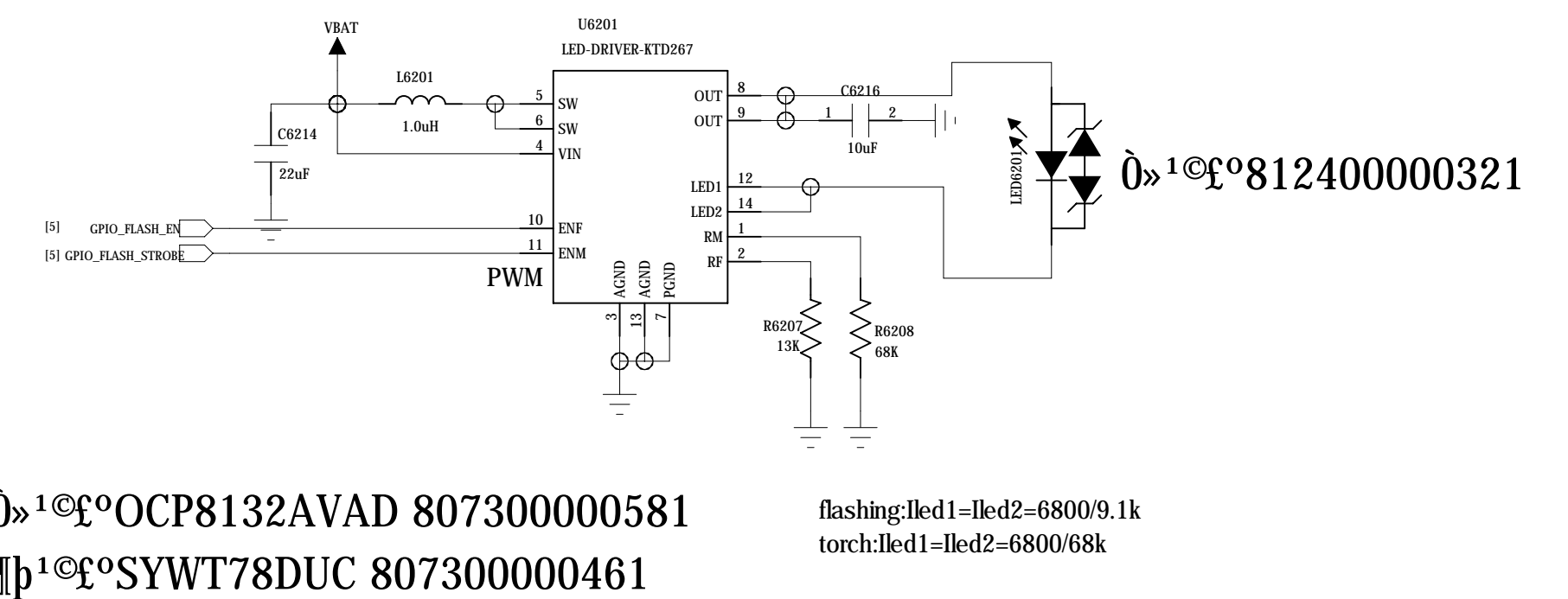
DOVDD=1.8V  
AVDD=2.8V



Front



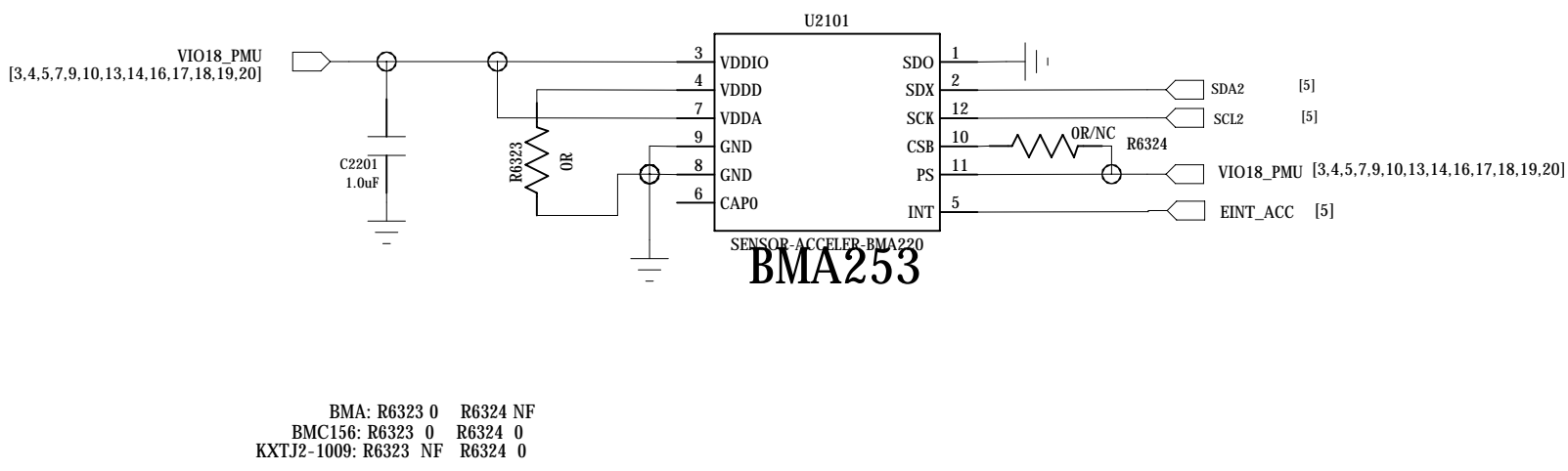
## Back



TITLE: <TITLE>		REV: <REV>	
DOCUMENT NO.: 62_PERI_CAMERA		SIZED: A1	
DEPARTMENT: Hardware DEPT.			
COMPANY: 			
DESIGNER: <DESIGNER>	Last Saved Date: 2017/1/16 06:00		SHEET: 18 OF 21

M-Sensor

G-Sensor

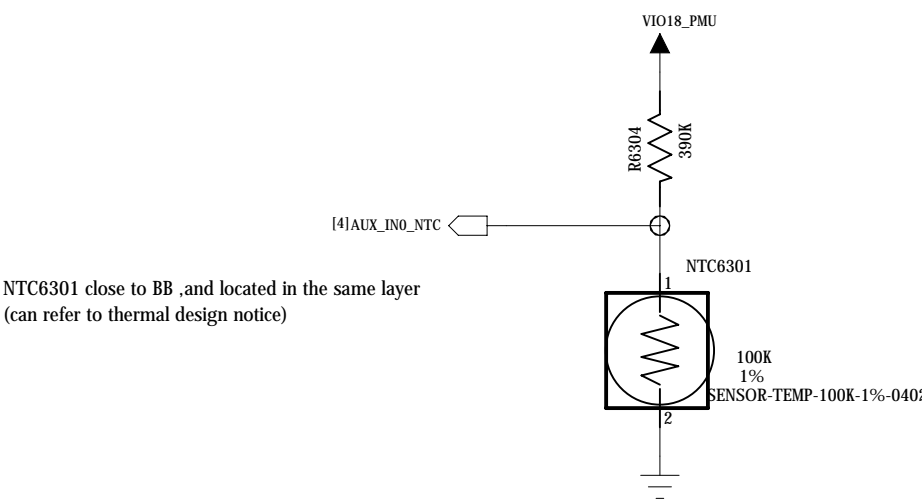


0»¹@£°821100000031  
¶p¹@£°821100000041

Accerometer

ALS+PS+IR

Thermistor



Thermistor / To sense board level temperature

TITLE:	<TITLE>	REV:	<REV>
DOCUMENT NO.:	\ 63_PERI_SENSORS	SIZED:	A1
DEPARTMENT:	Hardware DEPT.		
COMPANY:			
DESIGNER:	<DESIGNER>	Last Saved Date:	2017/1/16/PC.HU>
SHEET:	19	OF	21

0»<sup>1</sup>©£°813200000193

¶b<sup>1</sup>©£°813200000192

0»¹©£°813320000041

¶p<sup>1</sup>©£°813320000042

# SIM2

# SIM1

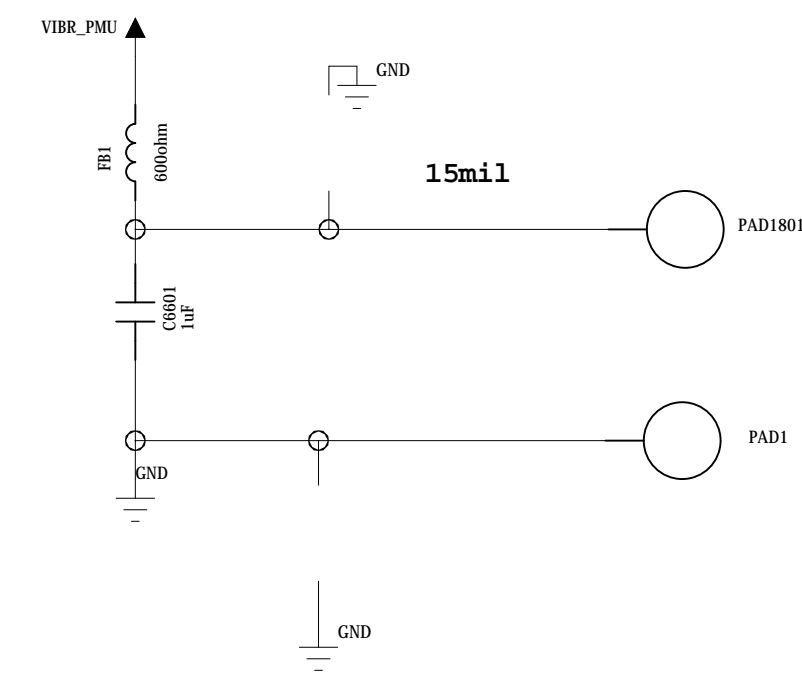
Note: 40-1

Based on your system level design , if better ESD/desense performance is needed on your system.

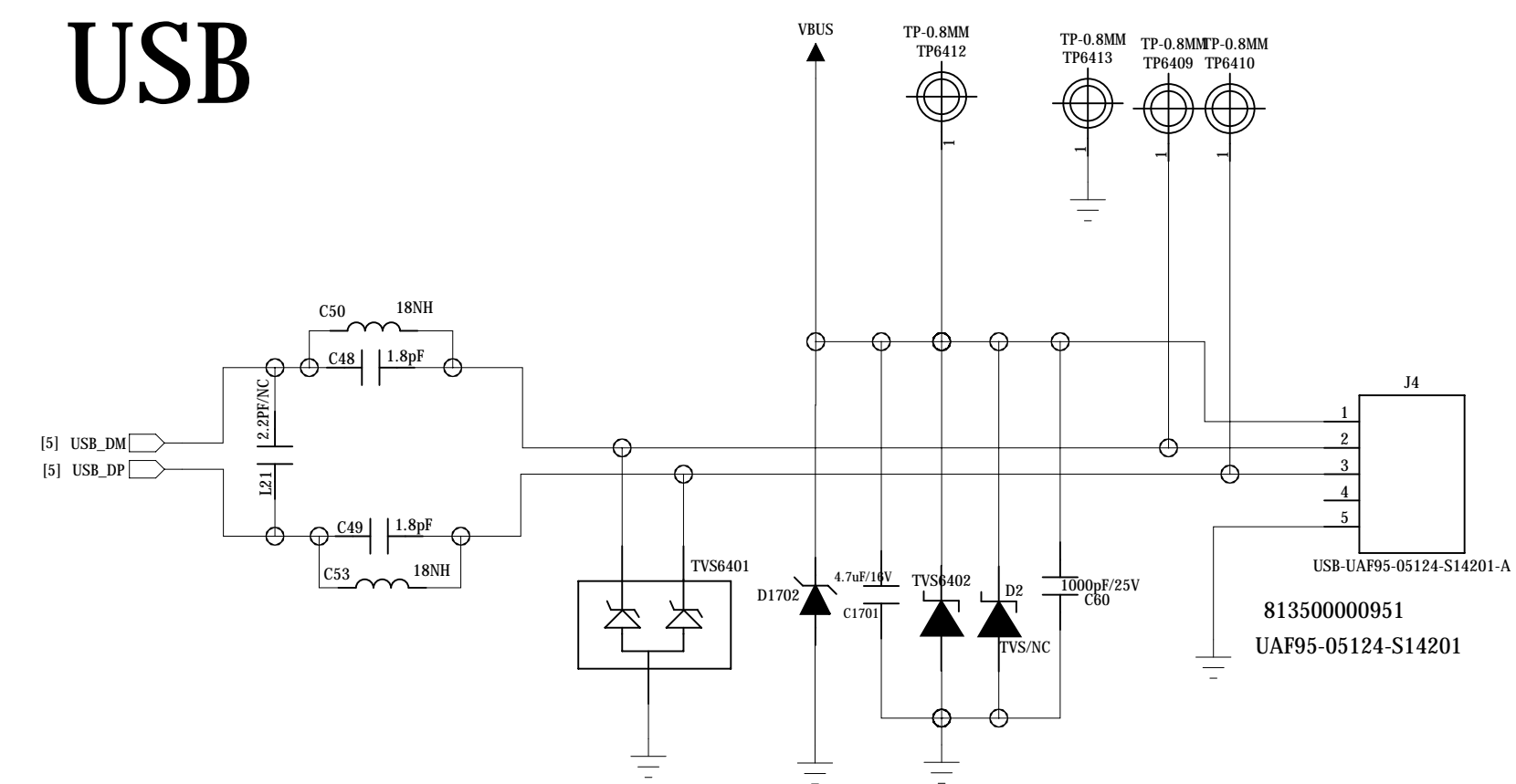
Schematic design notice of "40\_MEMORY\_SD Card" page.

Note 40-1: The equivalent capacitance of MSDC ESD protection device must be  $\leq 10\text{pF}$ .  
But for NFC app. equivalent capacitance of MSDC\_NFC\_SWPIO and MSDC\_NFC\_VCCSWP should  $\leq 0.5\text{pF}$ .

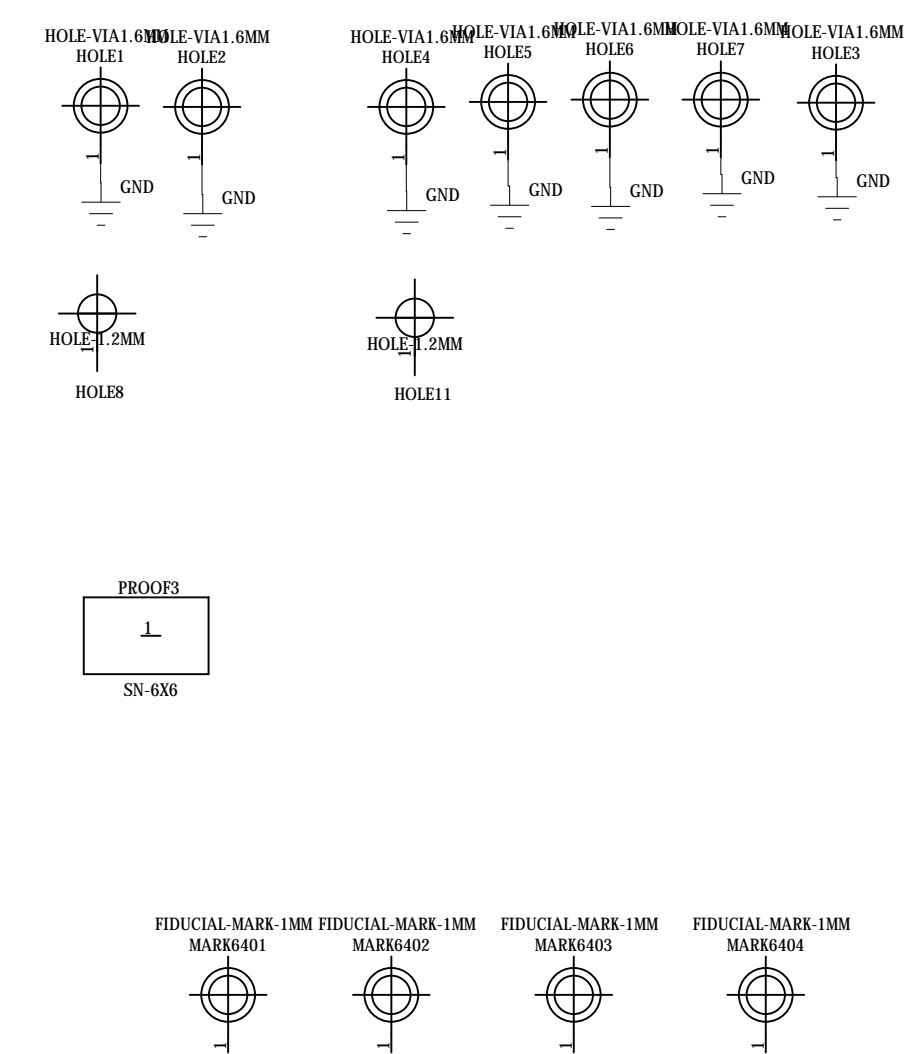
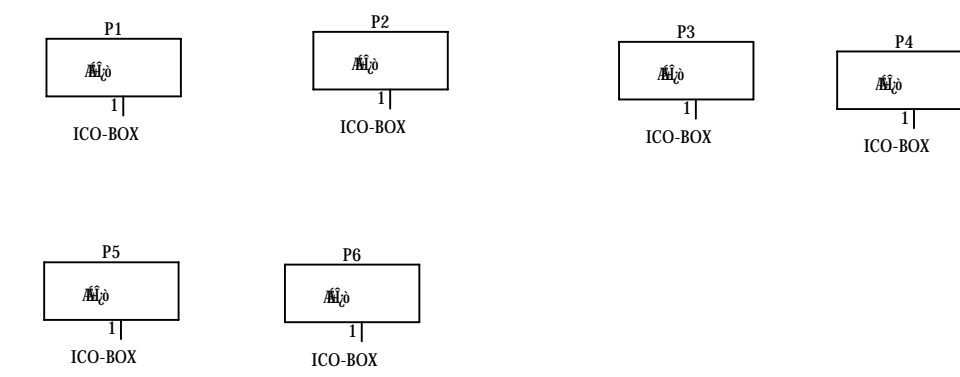
## MOTO



# USB



sheildings



TITLE: <TITLE>		REV: <REV>
DOCUMENT NO.: 65_PERI_USB/VIBRATOR/OTHER		SIZED: A1
DEPARTMENT: Hardware DEPT.		
COMPANY: 		
DESIGNER: <DESIGNER>	Last Saved Date: 2017/1/16 09:00	SHEET: 21 OF 21