



# ST7567A

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**132X65 Dot Matrix LCD Controller/Driver**

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## **Datasheet**

**Version 1.2a**

**2016/12**

**Sitronix Technology Corporation**

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## 1 INTRODUCTION

ST7567A is a single-chip dot matrix LCD driver which incorporates LCD controller and common/segment drivers. ST7567A can be connected directly to a microprocessor with 8-bit parallel interface, 4-line serial interface (SPI-4), 3-line serial interface (SPI-3) or I2C serial interface. Display data sent from MPU is stored in the internal Display Data RAM (DDRAM) of 132x65 bits. The display data bits which are stored in DDRAM are directly related to the pixels of LCD panel. ST7567A contains 132 segment-outputs, 64 common-outputs and 1 icon-common-output. With built-in oscillation circuit and low power consumption power circuit, ST7567A generates LCD driving signal without external clock or power, so that it is possible to make a display system with the fewest components and minimal power consumption.

## 2 FEATURES

### Single-chip LCD Controller & Driver

#### On-chip Display Data RAM (DDRAM)

- Capacity: 132x65=8580 bits
- Directly display RAM pattern from DDRAM

#### Selectable Display Duty

- 1/65 duty : 132 segment x 65 common
- 1/55 duty : 132 segment x 55 common
- 1/49 duty : 132 segment x 49 common
- 1/33 duty : 132 segment x 33 common
- 1/17 duty : 132 segment x 17 common
- 1/9 duty : 132 segment x 9 common

#### Microprocessor Interface

- Bidirectional 8-bit parallel interface supports:  
8080-series and 6800-series MPU
- 4-line SPI (SPI-4)
- 3-line SPI (SPI-3)
- I2C

#### Abundant Functions

- Display ON/OFF, Normal/Reverse Display Mode, Set Display Start Line, Read IC Status, Set all

Display Points ON, Set LCD Bias, Electronic Volume Control, Read-modify-Write, Select Segment Driver Direction, Power Saving Mode, Select Common Driver Direction, Select Voltage Regulator Resistor Ratio (for V0).

#### External Hardware Reset Pin (RSTB)

#### Built-in Oscillation Circuit

- No external component required

#### Low Power Consumption Analog Circuit



- Voltage Booster (4X, 5X)
- High-accuracy Voltage Regulator for LCD Vop (Thermal Gradient: -0.05%/°C)
- Voltage Follower for LCD Bias Voltage

#### Wide Operation Voltage Range

- VDD1-VSS1=1.8V~3.3V (TYP.)
- VDD2-VSS2=2.2V~3.3V (TYP.)
- VDD3-VSS3=2.2V~3.3V (TYP.)

#### Temperature Range: -30~85°C

#### Package Type: COG

|                 |                                   |   |
|-----------------|-----------------------------------|---|
| <b>ST7567A</b>  | <b>6800, 8080, 4-Line, 3-Line</b> |  |
| <b>ST7567Ai</b> | <b>I<sup>2</sup>C Interface</b>   |  |

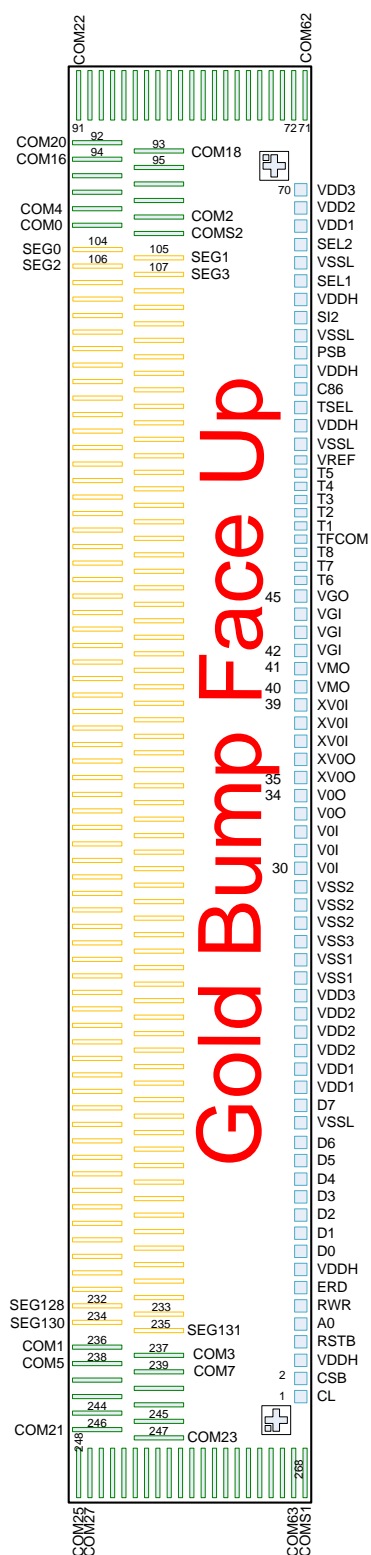
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### 3-1 PAD ARRANGEMENT

| Part Number   |                 |
|---|-----------------|
| ST7567A   |                 |
| Chip Size   | 4214 x 624 ± 40 |
| Chip Thickness  | 300             |
| Bump Height   | 10              |
| Bump Size   |                 |
| PAD No.   | Size            |
| 71~91,248~268   | 115X12          |
| 92~103,104~235, 236~247   | 12X115          |
| 3,8,16,55~70  | 30X45           |
| 46~54   | 25X45           |
| 1~2,4~7,9~15,17~45  | 40x45           |
| Bump Space  |                 |
| PAD No.   | Length          |
| 1~70  | 15              |
| 71~91,248~268   | 14              |
| 92~103,104~235, 236~247   | 36              |
| * Unit: um<br>* Refer to section “PAD CENTER COORDINATES” for ITO layout. |                 |

### Figure 1 Chip Outline

### 3-2 PAD CENTER COORDINATES



| PAD NO. | PIN Name | X     | Y      |
|---------|----------|-------|--------|
| 1       | CL       | -1735 | -254.5 |
| 2       | CSB      | -1680 | -254.5 |
| 3       | VDDH     | -1630 | -254.5 |
| 4       | RSTB     | -1580 | -254.5 |
| 5       | A0       | -1525 | -254.5 |
| 6       | RWR      | -1470 | -254.5 |
| 7       | ERD      | -1415 | -254.5 |
| 8       | VDDH     | -1365 | -254.5 |
| 9       | D0       | -1315 | -254.5 |
| 10      | D1       | -1260 | -254.5 |
| 11      | D2       | -1205 | -254.5 |
| 12      | D3       | -1150 | -254.5 |
| 13      | D4       | -1095 | -254.5 |
| 14      | D5       | -1040 | -254.5 |
| 15      | D6       | -985  | -254.5 |
| 16      | VSSL     | -935  | -254.5 |
| 17      | D7       | -885  | -254.5 |
| 18      | VDD1     | -830  | -254.5 |
| 19      | VDD1     | -775  | -254.5 |
| 20      | VDD2     | -720  | -254.5 |
| 21      | VDD2     | -665  | -254.5 |
| 22      | VDD2     | -610  | -254.5 |
| 23      | VDD3     | -555  | -254.5 |
| 24      | VSS1     | -500  | -254.5 |
| 25      | VSS1     | -445  | -254.5 |
| 26      | VSS3     | -390  | -254.5 |
| 27      | VSS2     | -335  | -254.5 |
| 28      | VSS2     | -280  | -254.5 |
| 29      | VSS2     | -225  | -254.5 |
| 30      | V0I      | -170  | -254.5 |
| 31      | V0I      | -115  | -254.5 |
| 32      | V0I      | -60   | -254.5 |
| 33      | V0O      | -5    | -254.5 |
| 34      | V0O      | 50    | -254.5 |
| 35      | XV0O     | 105   | -254.5 |
| 36      | XV0O     | 160   | -254.5 |
| 37      | XV0I     | 215   | -254.5 |
| 38      | XV0I     | 270   | -254.5 |
| 39      | XV0I     | 325   | -254.5 |
| 40      | VMO      | 380   | -254.5 |

Figure 2 PAD Location



| PAD NO. | PIN Name | X      | Y      |
|---------|----------|--------|--------|
| 41      | VMO      | 435    | -254.5 |
| 42      | VGI      | 490    | -254.5 |
| 43      | VGI      | 545    | -254.5 |
| 44      | VGI      | 600    | -254.5 |
| 45      | VGO      | 655    | -254.5 |
| 46      | T6       | 702.5  | -254.5 |
| 47      | T7       | 742.5  | -254.5 |
| 48      | T8       | 782.5  | -254.5 |
| 49      | TFCOM    | 822.5  | -254.5 |
| 50      | T1       | 862.5  | -254.5 |
| 51      | T2       | 902.5  | -254.5 |
| 52      | T3       | 942.5  | -254.5 |
| 53      | T4       | 982.5  | -254.5 |
| 54      | T5       | 1022.5 | -254.5 |
| 55      | VREF     | 1065   | -254.5 |
| 56      | VSSL     | 1110   | -254.5 |
| 57      | VDDH     | 1155   | -254.5 |
| 58      | TSEL     | 1200   | -254.5 |
| 59      | C86      | 1245   | -254.5 |
| 60      | VDDH     | 1290   | -254.5 |
| 61      | PSB      | 1335   | -254.5 |
| 62      | VSSL     | 1380   | -254.5 |
| 63      | SI2      | 1425   | -254.5 |
| 64      | VDDH     | 1470   | -254.5 |
| 65      | SEL1     | 1515   | -254.5 |
| 66      | VSSL     | 1560   | -254.5 |
| 67      | SEL2     | 1605   | -254.5 |
| 68      | VDD1     | 1650   | -254.5 |
| 69      | VDD2     | 1695   | -254.5 |
| 70      | VDD3     | 1740   | -254.5 |
| 71      | COM62    | 2009.5 | -257.5 |
| 72      | COM60    | 2009.5 | -231.5 |
| 73      | COM58    | 2009.5 | -205.5 |
| 74      | COM56    | 2009.5 | -179.5 |
| 75      | COM54    | 2009.5 | -153.5 |
| 76      | COM52    | 2009.5 | -127.5 |
| 77      | COM50    | 2009.5 | -101.5 |
| 78      | COM48    | 2009.5 | -75.5  |
| 79      | COM46    | 2009.5 | -49.5  |
| 80      | COM44    | 2009.5 | -23.5  |

| PAD NO. | PIN Name | X      | Y     |
|---------|----------|--------|-------|
| 81      | COM42    | 2009.5 | 2.5   |
| 82      | COM40    | 2009.5 | 28.5  |
| 83      | COM38    | 2009.5 | 54.5  |
| 84      | COM36    | 2009.5 | 80.5  |
| 85      | COM34    | 2009.5 | 106.5 |
| 86      | COM32    | 2009.5 | 132.5 |
| 87      | COM30    | 2009.5 | 158.5 |
| 88      | COM28    | 2009.5 | 184.5 |
| 89      | COM26    | 2009.5 | 210.5 |
| 90      | COM24    | 2009.5 | 236.5 |
| 91      | COM22    | 2009.5 | 262.5 |
| 92      | COM20    | 1880   | 219.5 |
| 93      | COM18    | 1856   | 89.5  |
| 94      | COM16    | 1832   | 219.5 |
| 95      | COM14    | 1808   | 89.5  |
| 96      | COM12    | 1784   | 219.5 |
| 97      | COM10    | 1760   | 89.5  |
| 98      | COM8     | 1736   | 219.5 |
| 99      | COM6     | 1712   | 89.5  |
| 100     | COM4     | 1688   | 219.5 |
| 101     | COM2     | 1664   | 89.5  |
| 102     | COM0     | 1640   | 219.5 |
| 103     | COMS2    | 1616   | 89.5  |
| 104     | SEG0     | 1572   | 219.5 |
| 105     | SEG1     | 1548   | 89.5  |
| 106     | SEG2     | 1524   | 219.5 |
| 107     | SEG3     | 1500   | 89.5  |
| 108     | SEG4     | 1476   | 219.5 |
| 109     | SEG5     | 1452   | 89.5  |
| 110     | SEG6     | 1428   | 219.5 |
| 111     | SEG7     | 1404   | 89.5  |
| 112     | SEG8     | 1380   | 219.5 |
| 113     | SEG9     | 1356   | 89.5  |
| 114     | SEG10    | 1332   | 219.5 |
| 115     | SEG11    | 1308   | 89.5  |
| 116     | SEG12    | 1284   | 219.5 |
| 117     | SEG13    | 1260   | 89.5  |
| 118     | SEG14    | 1236   | 219.5 |
| 119     | SEG15    | 1212   | 89.5  |
| 120     | SEG16    | 1188   | 219.5 |

| PAD NO. | PIN Name | X    | Y     |
|---------|----------|------|-------|
| 121     | SEG17    | 1164 | 89.5  |
| 122     | SEG18    | 1140 | 219.5 |
| 123     | SEG19    | 1116 | 89.5  |
| 124     | SEG20    | 1092 | 219.5 |
| 125     | SEG21    | 1068 | 89.5  |
| 126     | SEG22    | 1044 | 219.5 |
| 127     | SEG23    | 1020 | 89.5  |
| 128     | SEG24    | 996  | 219.5 |
| 129     | SEG25    | 972  | 89.5  |
| 130     | SEG26    | 948  | 219.5 |
| 131     | SEG27    | 924  | 89.5  |
| 132     | SEG28    | 900  | 219.5 |
| 133     | SEG29    | 876  | 89.5  |
| 134     | SEG30    | 852  | 219.5 |
| 135     | SEG31    | 828  | 89.5  |
| 136     | SEG32    | 804  | 219.5 |
| 137     | SEG33    | 780  | 89.5  |
| 138     | SEG34    | 756  | 219.5 |
| 139     | SEG35    | 732  | 89.5  |
| 140     | SEG36    | 708  | 219.5 |
| 141     | SEG37    | 684  | 89.5  |
| 142     | SEG38    | 660  | 219.5 |
| 143     | SEG39    | 636  | 89.5  |
| 144     | SEG40    | 612  | 219.5 |
| 145     | SEG41    | 588  | 89.5  |
| 146     | SEG42    | 564  | 219.5 |
| 147     | SEG43    | 540  | 89.5  |
| 148     | SEG44    | 516  | 219.5 |
| 149     | SEG45    | 492  | 89.5  |
| 150     | SEG46    | 468  | 219.5 |
| 151     | SEG47    | 444  | 89.5  |
| 152     | SEG48    | 420  | 219.5 |
| 153     | SEG49    | 396  | 89.5  |
| 154     | SEG50    | 372  | 219.5 |
| 155     | SEG51    | 348  | 89.5  |
| 156     | SEG52    | 324  | 219.5 |
| 157     | SEG53    | 300  | 89.5  |
| 158     | SEG54    | 276  | 219.5 |
| 159     | SEG55    | 252  | 89.5  |
| 160     | SEG56    | 228  | 219.5 |

| PAD NO. | PIN Name | X    | Y     |
|---------|----------|------|-------|
| 161     | SEG57    | 204  | 89.5  |
| 162     | SEG58    | 180  | 219.5 |
| 163     | SEG59    | 156  | 89.5  |
| 164     | SEG60    | 132  | 219.5 |
| 165     | SEG61    | 108  | 89.5  |
| 166     | SEG62    | 84   | 219.5 |
| 167     | SEG63    | 60   | 89.5  |
| 168     | SEG64    | 36   | 219.5 |
| 169     | SEG65    | 12   | 89.5  |
| 170     | SEG66    | -12  | 219.5 |
| 171     | SEG67    | -36  | 89.5  |
| 172     | SEG68    | -60  | 219.5 |
| 173     | SEG69    | -84  | 89.5  |
| 174     | SEG70    | -108 | 219.5 |
| 175     | SEG71    | -132 | 89.5  |
| 176     | SEG72    | -156 | 219.5 |
| 177     | SEG73    | -180 | 89.5  |
| 178     | SEG74    | -204 | 219.5 |
| 179     | SEG75    | -228 | 89.5  |
| 180     | SEG76    | -252 | 219.5 |
| 181     | SEG77    | -276 | 89.5  |
| 182     | SEG78    | -300 | 219.5 |
| 183     | SEG79    | -324 | 89.5  |
| 184     | SEG80    | -348 | 219.5 |
| 185     | SEG81    | -372 | 89.5  |
| 186     | SEG82    | -396 | 219.5 |
| 187     | SEG83    | -420 | 89.5  |
| 188     | SEG84    | -444 | 219.5 |
| 189     | SEG85    | -468 | 89.5  |
| 190     | SEG86    | -492 | 219.5 |
| 191     | SEG87    | -516 | 89.5  |
| 192     | SEG88    | -540 | 219.5 |
| 193     | SEG89    | -564 | 89.5  |
| 194     | SEG90    | -588 | 219.5 |
| 195     | SEG91    | -612 | 89.5  |
| 196     | SEG92    | -636 | 219.5 |
| 197     | SEG93    | -660 | 89.5  |
| 198     | SEG94    | -684 | 219.5 |
| 199     | SEG95    | -708 | 89.5  |
| 200     | SEG96    | -732 | 219.5 |

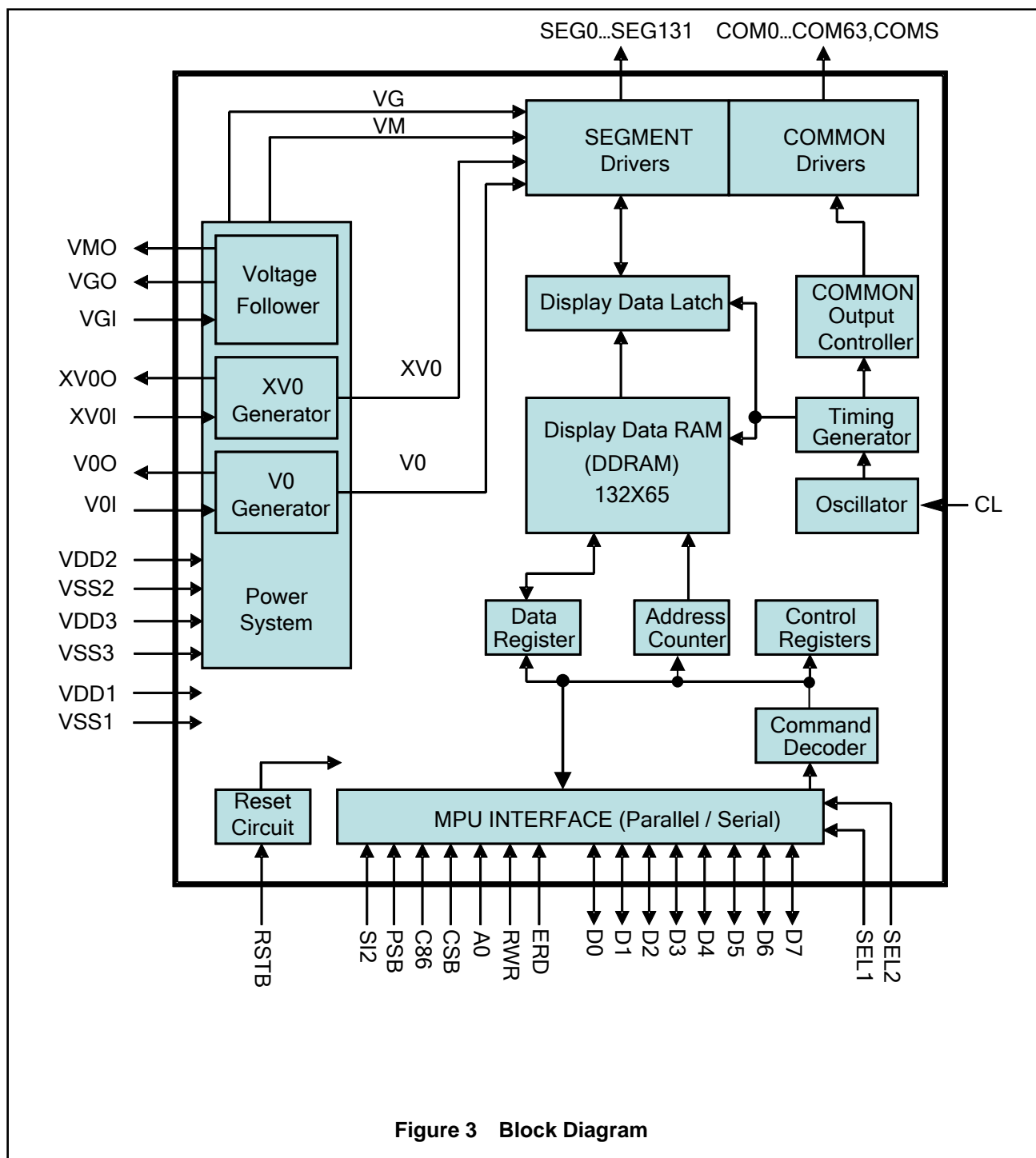
| PAD NO. | PIN Name | X     | Y     |
|---------|----------|-------|-------|
| 201     | SEG97    | -756  | 89.5  |
| 202     | SEG98    | -780  | 219.5 |
| 203     | SEG99    | -804  | 89.5  |
| 204     | SEG100   | -828  | 219.5 |
| 205     | SEG101   | -852  | 89.5  |
| 206     | SEG102   | -876  | 219.5 |
| 207     | SEG103   | -900  | 89.5  |
| 208     | SEG104   | -924  | 219.5 |
| 209     | SEG105   | -948  | 89.5  |
| 210     | SEG106   | -972  | 219.5 |
| 211     | SEG107   | -996  | 89.5  |
| 212     | SEG108   | -1020 | 219.5 |
| 213     | SEG109   | -1044 | 89.5  |
| 214     | SEG110   | -1068 | 219.5 |
| 215     | SEG111   | -1092 | 89.5  |
| 216     | SEG112   | -1116 | 219.5 |
| 217     | SEG113   | -1140 | 89.5  |
| 218     | SEG114   | -1164 | 219.5 |
| 219     | SEG115   | -1188 | 89.5  |
| 220     | SEG116   | -1212 | 219.5 |
| 221     | SEG117   | -1236 | 89.5  |
| 222     | SEG118   | -1260 | 219.5 |
| 223     | SEG119   | -1284 | 89.5  |
| 224     | SEG120   | -1308 | 219.5 |
| 225     | SEG121   | -1332 | 89.5  |
| 226     | SEG122   | -1356 | 219.5 |
| 227     | SEG123   | -1380 | 89.5  |
| 228     | SEG124   | -1404 | 219.5 |
| 229     | SEG125   | -1428 | 89.5  |
| 230     | SEG126   | -1452 | 219.5 |
| 231     | SEG127   | -1476 | 89.5  |
| 232     | SEG128   | -1500 | 219.5 |
| 233     | SEG129   | -1524 | 89.5  |
| 234     | SEG130   | -1548 | 219.5 |
| 235     | SEG131   | -1572 | 89.5  |
| 236     | COM1     | -1616 | 219.5 |
| 237     | COM3     | -1640 | 89.5  |
| 238     | COM5     | -1664 | 219.5 |
| 239     | COM7     | -1688 | 89.5  |
| 240     | COM9     | -1712 | 219.5 |

| PAD NO. | PIN Name | X       | Y      |
|---------|----------|---------|--------|
| 241     | COM11    | -1736   | 89.5   |
| 242     | COM13    | -1760   | 219.5  |
| 243     | COM15    | -1784   | 89.5   |
| 244     | COM17    | -1808   | 219.5  |
| 245     | COM19    | -1832   | 89.5   |
| 246     | COM21    | -1856   | 219.5  |
| 247     | COM23    | -1880   | 89.5   |
| 248     | COM25    | -2009.5 | 262.5  |
| 249     | COM27    | -2009.5 | 236.5  |
| 250     | COM29    | -2009.5 | 210.5  |
| 251     | COM31    | -2009.5 | 184.5  |
| 252     | COM33    | -2009.5 | 158.5  |
| 253     | COM35    | -2009.5 | 132.5  |
| 254     | COM37    | -2009.5 | 106.5  |
| 255     | COM39    | -2009.5 | 80.5   |
| 256     | COM41    | -2009.5 | 54.5   |
| 257     | COM43    | -2009.5 | 28.5   |
| 258     | COM45    | -2009.5 | 2.5    |
| 259     | COM47    | -2009.5 | -23.5  |
| 260     | COM49    | -2009.5 | -49.5  |
| 261     | COM51    | -2009.5 | -75.5  |
| 262     | COM53    | -2009.5 | -101.5 |
| 263     | COM55    | -2009.5 | -127.5 |
| 264     | COM57    | -2009.5 | -153.5 |
| 265     | COM59    | -2009.5 | -179.5 |
| 266     | COM61    | -2009.5 | -205.5 |
| 267     | COM63    | -2009.5 | -231.5 |
| 268     | COMS1    | -2009.5 | -257.5 |

Note:

1. Unit:  $\mu\text{m}$
2. This is the default PAD Center Coordinate Table with 1/65 Duty. Other duty output mapping can be found in Section 6 FUNCTION DESCRIPTION.
3. Tolerance:  $\pm 0.05 \mu\text{m}$ .
4. **The definition of pin name is in full duty (65 duty).**
5. **The definition of output pin in different duty (55 Duty, 49 Duty and 33 Duty) please refers Figure 15~17.**

# 4 BLOCK DIAGRAM



## 5 HARDWARE PIN DESCRIPTION

### 5-1 LCD Driver Output Pins

| Pin Name                | Type  | Description  | Pins            |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
|-------------------------|-------|--|-----------------|-------|-------------------------------|--|----------------|-----------------|---|---|-----|-----|---|---|-----|----|---|---|-----|----|---|---|----|-----|-------------------------|--|-----|-----|-----|
| SEG0 to SEG131          | O     | <p>LCD segment driver outputs.</p> <p>The display data and the frame control the output voltage.</p> <table> <tr> <th rowspan="2">Display data</th><th rowspan="2">Frame</th><th colspan="2">Segment Driver Output Voltage</th></tr> <tr> <th>Normal Display</th><th>Inverse Display</th></tr> <tr> <td>H</td><td>+</td><td>VG</td><td>VSS</td></tr> <tr> <td>H</td><td>-</td><td>VSS</td><td>VG</td></tr> <tr> <td>L</td><td>+</td><td>VSS</td><td>VG</td></tr> <tr> <td>L</td><td>-</td><td>VG</td><td>VSS</td></tr> <tr> <td colspan="2">Display OFF, Power Save</td><td>VSS</td><td>VSS</td></tr> </table>           | Display data    | Frame | Segment Driver Output Voltage |  | Normal Display | Inverse Display | H | + | VG  | VSS | H | - | VSS | VG | L | + | VSS | VG | L | - | VG | VSS | Display OFF, Power Save |  | VSS | VSS | 132 |
| Display data            | Frame | Segment Driver Output Voltage  |                 |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
|                         |       | Normal Display   | Inverse Display |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| H                       | +     | VG   | VSS             |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| H                       | -     | VSS  | VG              |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| L                       | +     | VSS  | VG              |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| L                       | -     | VG   | VSS             |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| Display OFF, Power Save |       | VSS  | VSS             |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| COM0 to COM63           | O     | <p>LCD common driver outputs.</p> <p>The internal scanning signal and the frame control the output voltage.</p> <table> <tr> <th rowspan="2">Scan signal</th><th rowspan="2">Frame</th><th colspan="2">Common Driver Output Voltage</th></tr> <tr> <th>Normal Display</th><th>Inverse Display</th></tr> <tr> <td>H</td><td>+</td><td colspan="2">XV0</td></tr> <tr> <td>H</td><td>-</td><td colspan="2">V0</td></tr> <tr> <td>L</td><td>+</td><td colspan="2">VM</td></tr> <tr> <td>L</td><td>-</td><td colspan="2">VM</td></tr> <tr> <td colspan="2">Display OFF, Power Save</td><td colspan="2">VSS</td></tr> </table> | Scan signal     | Frame | Common Driver Output Voltage  |  | Normal Display | Inverse Display | H | + | XV0 |     | H | - | V0  |    | L | + | VM  |    | L | - | VM |     | Display OFF, Power Save |  | VSS |     | 64  |
| Scan signal             | Frame | Common Driver Output Voltage   |                 |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
|                         |       | Normal Display   | Inverse Display |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| H                       | +     | XV0  |                 |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| H                       | -     | V0   |                 |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| L                       | +     | VM   |                 |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| L                       | -     | VM   |                 |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| Display OFF, Power Save |       | VSS  |                 |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |
| COMS1, COMS2 (COMS)     | O     | <p>LCD common driver outputs for icons.</p> <p>The output signals of these two pins are the same.</p> <p>When icon feature is not used, these pins should be left open.</p>  | 2               |       |                               |  |                |                 |   |   |     |     |   |   |     |    |   |   |     |    |   |   |    |     |                         |  |     |     |     |

### 5-2 Microprocessor Interface Pins

| Pin Name | Type | Description   | Pins |
|----------|------|---|------|
| RSTB     | I    | Hardware reset input pin. When RSTB is "L", internal initialization is executed and the internal registers will be initialized.   | 1    |
| CSB      | I    | Chip select input pin. Interface access is enabled when CSB is "L". When CSB is non-active (CSB="H"), D[7:0] pins are high impedance.   | 1    |
| A0       | I    | <p>It determines whether the access is related to data or command.</p> <p>A0="H" : Indicates that signals on D[7:0] are display data.</p> <p>A0="L" : Indicates that signals on D[7:0] are command.</p> | 1    |

| Pin Name | Type | Description  |             |     |  | Pins |
|----------|------|--|-------------|-----|--|------|
| RWR      | I    | Read/Write execution control pin. When PSB is “H”,   |             |     |  | 1    |
|          |      | C86  | MPU Type    | RWR | Description  |      |
|          |      | H  | 6800 series | R/W | Read/Write control input pin.<br>R/W=“H”: read.<br>R/W=“L”: write.   |      |
|          |      | L  | 8080 series | /WR | Write enable input pin.<br>Signals on D[7:0] will be latched at the rising edge of /WR signal.   |      |
|          |      | RWR is used to decide slave address (SA1) in I2C serial interface.<br>RWR is not used in 3-line and 4-line SPI interface and should fix to “H” by VDD1 or VDDH.  |             |     |  |      |
| ERD      | I    | Read/Write execution control pin. When PSB is “H”,   |             |     |  | 1    |
|          |      | C86  | MPU Type    | ERD | Description  |      |
|          |      | H  | 6800 series | E   | Read/Write control input pin.<br>R/W=“H”: When E is “H”, D[7:0] are in output mode.<br>R/W=“L”: Signals on D[7:0] are latched at the falling edge of E signal. |      |
|          |      | L  | 8080 series | /RD | Read enable input pin.<br>When /RD is “L”, D[7:0] are in output mode.  |      |
|          |      | ERD is used to decide slave address (SA0) in I2C serial interface.<br>ERD is not used in 3-Line and 4-Line SPI interface and should fix to “H” by VDD1 or VDDH.  |             |     |  |      |
| D[7:0]   | I/O  | <b>When using 8-bit parallel interface: (6800 or 8080 mode)</b><br>8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.<br>When CSB is non-active (CSB=“H”), D[7:0] pins are high impedance.  |             |     |  | 8    |
|          | I/O  | <b>When using serial interface: 4-line SPI, 3-line SPI or I2C serial interface</b><br>D[0]=SCL: Serial clock input.<br>D[1]=SDA_IN: Serial data input.<br>D[2:3]=SDA_OUT: Serial data output.<br><b>D[1:3] must be connected together as SDA.</b><br>D[4:7]=(1,1,1,1): ID Pin. D[4:7] should fix to “H” or “L” by VDDH or VSSL.<br>ID[0:3] can be read 4-bit ID only for serial interface from D[4:7]. |             |     |  |      |

**Note:**

1. After VDD1 is turned ON, any MPU interface pins cannot be left floating.

**5-3 Configuration Pins**

| Pin Name | Type | Description   | Pins                               |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
|----------|------|---|------------------------------------|------|------|--------------------|-----|-----|------|-----------------------------|-----|-----|------|-----------------------------|-----|-----|------|------------------------------------|-----|-----|------|------------------------------------|-----|-----|-----|----------------------|---|
| VDDH     | O    | Logic "1" level for option pins which should connected to "H".  | 2                                  |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
| VSSL     | O    | Logic "0" level for option pins which should connected to "L".  | 2                                  |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
| PSB      | I    | PSB selects the interface type: Serial or Parallel.   | 1                                  |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
| C86      | I    | C86 selects the microprocessor type in parallel interface mode.   | 1                                  |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
| SI2      | I    | <p>SI2 selects the interface type: I2C serial interface or not</p> <table border="1"> <thead> <tr> <th>SI2</th><th>PSB</th><th>C86</th><th>Selected Interface</th></tr> </thead> <tbody> <tr> <td>"L"</td><td>"L"</td><td>"L"</td><td>Serial 3-Line SPI Interface</td></tr> <tr> <td>"L"</td><td>"L"</td><td>"H"</td><td>Serial 4-Line SPI Interface</td></tr> <tr> <td>"L"</td><td>"H"</td><td>"L"</td><td>Parallel 8080 Series MPU Interface</td></tr> <tr> <td>"L"</td><td>"H"</td><td>"H"</td><td>Parallel 6800 Series MPU Interface</td></tr> <tr> <td>"H"</td><td>"L"</td><td>"X"</td><td>I2C Serial Interface</td></tr> </tbody> </table> <p>Please refer to "APPLICATION NOTES" and "Microprocessor Interface" (Section 6) for detailed connection of the selected interface.</p> | SI2                                | PSB  | C86  | Selected Interface | "L" | "L" | "L"  | Serial 3-Line SPI Interface | "L" | "L" | "H"  | Serial 4-Line SPI Interface | "L" | "H" | "L"  | Parallel 8080 Series MPU Interface | "L" | "H" | "H"  | Parallel 6800 Series MPU Interface | "H" | "L" | "X" | I2C Serial Interface | 1 |
| SI2      | PSB  | C86   | Selected Interface                 |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
| "L"      | "L"  | "L"   | Serial 3-Line SPI Interface        |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
| "L"      | "L"  | "H"   | Serial 4-Line SPI Interface        |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
| "L"      | "H"  | "L"   | Parallel 8080 Series MPU Interface |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
| "L"      | "H"  | "H"   | Parallel 6800 Series MPU Interface |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
| "H"      | "L"  | "X"   | I2C Serial Interface               |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
| SEL[2:1] | I    | <p>These pins select the display duty and bias of ST7567A.</p> <table border="1"> <thead> <tr> <th>SEL2</th><th>SEL1</th><th>Duty</th><th>Bias</th></tr> </thead> <tbody> <tr> <td>"L"</td><td>"L"</td><td>1/65</td><td>1/9 or 1/7</td></tr> <tr> <td>"L"</td><td>"H"</td><td>1/49</td><td>1/8 or 1/6</td></tr> <tr> <td>"H"</td><td>"L"</td><td>1/33</td><td>1/6 or 1/5</td></tr> <tr> <td>"H"</td><td>"H"</td><td>1/55</td><td>1/8 or 1/6</td></tr> </tbody> </table> <p><b>Note:</b><br/>The detailed definition of output pin name can be found in Fig. 14~17.<br/>The setting of 1/17 duty and 1/9 duty can be found in command "Display Setting Mode"</p>   | SEL2                               | SEL1 | Duty | Bias               | "L" | "L" | 1/65 | 1/9 or 1/7                  | "L" | "H" | 1/49 | 1/8 or 1/6                  | "H" | "L" | 1/33 | 1/6 or 1/5                         | "H" | "H" | 1/55 | 1/8 or 1/6                         | 2   |     |     |                      |   |
| SEL2     | SEL1 | Duty  | Bias                               |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
| "L"      | "L"  | 1/65  | 1/9 or 1/7                         |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
| "L"      | "H"  | 1/49  | 1/8 or 1/6                         |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
| "H"      | "L"  | 1/33  | 1/6 or 1/5                         |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
| "H"      | "H"  | 1/55  | 1/8 or 1/6                         |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |
| TSEL     | I    | <p>TSEL is high power mode function.<br/>TSEL="L", Off mode (<math>1.6V \leq V_G &lt; V_{DD2}-0.2V</math>, for general use).<br/>TSEL="H", On mode (<math>V_{DD2}-0.2V \leq V_G &lt; 3.8V</math>).<br/>Note: <math>V_G = (V_{op}/bias) * 2</math></p>   | 1                                  |      |      |                    |     |     |      |                             |     |     |      |                             |     |     |      |                                    |     |     |      |                                    |     |     |     |                      |   |

**5-4 Power System Pins**

| Pin Name     | Type  | Description  | Pins   |
|--------------|-------|--|--------|
| VDD1         | Power | Digital power. If VDD1=VDD2, connect to VDD2 externally.   | 3      |
| VDD2         | Power | Analog power. If VDD1=VDD2, connect to VDD1 externally.  | 4      |
| VDD3         | Power | Power for reference voltage circuit.   | 2      |
| VSS1         | Power | Digital ground. Connect to VSS2 externally.  | 2      |
| VSS2         | Power | Analog ground. Connect to VSS1 externally.   | 3      |
| VSS3         | Power | Ground for reference voltage circuit.  | 1      |
| V0O<br>V0I   | Power | V0 is the LCD driving voltage for common circuits at negative frame.<br>V0O is the output of V0 regulator.<br>V0I is the V0 input of common circuits.<br>Be sure that: $V0 \geq VG > VM > VSS \geq XV0$ (under operation).<br>V0O, V0I should be connected together in ITO layout. | 2<br>3 |
| XV0O<br>XV0I | Power | XV0 is the LCD driving voltage for common circuits at positive frame.<br>XV0O is the output of XV0 regulator.<br>XV0I is the XV0 input of common circuits.<br>XV0O, XV0I should be connected together in ITO layout.   | 2<br>3 |
| VGO<br>VGI   | Power | VG is the LCD driving voltage for segment circuits.<br>VGO is the output of VG regulator.<br>VGI is the VG input of segment circuits.<br>VGO, VGI should be connected together in ITO layout.<br>$1.6V \leq VG < VDD2-0.2V$ , TSEL=L.<br>$VDD2-0.2V \leq VG < 3.8V$ , TSEL=H.      | 1<br>3 |
| VMO          | Power | VM is the LCD driving voltage for common circuits.<br>$0.8V \leq VM < VG$ .  | 2      |

**5-5 Test Pins**

| Pin Name | Type | Description   | Pins |
|----------|------|---|------|
| VREF     | T    | Test pin for power system.<br>This pin must be left open (without any kinds of connection). | 1    |
| TFCOM    | T    | Do NOT use. Reserved for testing.<br>Must be floating.                                      | 1    |
| T1~T8    | T    | Do NOT use. Reserved for testing.<br>Must be floating.                                      | 8    |
| CL       | T    | Do not use. Reserved for testing.<br>Must be floating.                                      | 1    |



**5-6 Recommend ITO Resistance**

| Pin Name  | ITO Resistance |
|---|----------------|
| T[8:1], TFCOM, CL, VREF, VMO  | Floating       |
| VDD1, VDD2, VDD3  | < 100Ω         |
| VSS1, VSS2, VSS3  | < 70Ω          |
| V0(V0I,V0O), XV0(XVI,XV0O), VG(VGI,VGO)                             | < 200 Ω        |
| A0, RWR, ERD, CSB, D[7:0]   | < 700Ω         |
| PSB, C86, SEL[2:1],SI2,TSEL   | < 5KΩ          |
| D[0](I2C - SCL),D[3:1](I2C - SDA)                                   | <100Ω          |
| D[0](3-line or 4-line SPI - SCL),D[3:1](3-line or 4-line SPI - SDA) | <300Ω          |
| RSTB *1   | 2~3KΩ          |

Note:

1. To prevent the ESD pulse resetting the internal register, applications should increase the resistance of RSTB signal (add a series resistor or increase ITO resistance). The value is different from modules.
2. The option setting to be "H" should connect to VDD1 or VDDH.
3. The option setting to be "L" should connect to VSS1 or VSSL.

## 6 FUNCTION DESCRIPTION

### 6-1 Microprocessor Interface

#### 6-1-1 Chip Select Input

CSB pin is used for chip selection. When CSB is “L”, the microprocessor interface is enabled and ST7567A can interface with an MPU. When CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In the serial interface (3-Line, 4-Line SPI and I2C), the internal shift register and serial counter are reset when CSB is “H”.

#### 6-1-2 Interface Selection

The interface selection is controlled by C86, PSB and SI2 pins. The selection for parallel or serial interface is shown in Table 1.

**Table 1. Parallel/Serial Interface Mode**

| SI2 | PSB | C86 | CSB | A0  | ERD | RWR | D[7:0]                     | MPU Interface                  |
|-----|-----|-----|-----|-----|-----|-----|----------------------------|--------------------------------|
| “L” | “L” | “L” | CSB | --- | --- | --- | Refer to serial interface. | 3-Line SPI interface           |
| “L” | “L” | “H” |     | --- | --- | --- |                            | 4-Line SPI interface           |
| “L” | “H” | “L” |     | A0  | /RD | /WR | D[7:0]                     | 8080-series parallel interface |
| “L” | “H” | “H” |     |     | E   | R/W |                            | 6800-series parallel interface |
| “H” | “L” | “X” | --- | --- | SA0 | SA1 | Refer to serial interface. | I2C serial interface           |

⇒ The un-used pins are marked as “---” and should be fixed to “H” by VDD1 or VDDH.

#### 6-1-3 Parallel Interface

When PSB= “H”, the 8-bit bi-directional parallel interface is enabled and the type of MPU is selected by “C86” pin as shown in Table 2. The data transfer type is determined by signals on A0, ERD and RWR as shown in Table 3.

**Table 2. Microprocessor Selection for Parallel Interface**

| PSB | C86 | CSB | A0 | ERD | RWR | D[7:0] | MPU Interface                  |
|-----|-----|-----|----|-----|-----|--------|--------------------------------|
| “H” | “L” | CSB | A0 | /RD | /WR | D[7:0] | 8080-series parallel interface |
| “H” | “H” |     |    | E   | R/W |        | 6800-series parallel interface |

**Table 3. Parallel Data Transfer Type**

| Common Pins |     | 6800-Series |           | 8080-Series |           | Description                               |
|-------------|-----|-------------|-----------|-------------|-----------|---|
| CSB         | A0  | E (ERD)     | R/W (RWR) | /RD (ERD)   | /WR (RWR) |   |
| “L”         | “H” | “H”         | “H”       | “L”         | “H”       | Display data read out                     |
|             | “H” | “H”         | “L”       | “H”         | “L”       | Display data write                        |
|             | “L” | “H”         | “H”       | “L”         | “H”       | Internal status read                      |
|             | “L” | “H”         | “L”       | “H”         | “L”       | Writes to internal register (instruction) |

#### 6-1-4 Setting Serial Interface

| Serial Mode          | SI2 | PSB | C86 | CSB | A0  | ERD | RWR | D[7:0]                          |
|----------------------|-----|-----|-----|-----|-----|-----|-----|---------------------------------|
| 3-Line SPI interface | "L" | "L" | "L" | CSB | --- | --- | --- | ID3,ID2,ID1,ID0,SDA,SDA,SDA,SCL |
| 4-Line SPI interface | "L" | "L" | "H" | CSB | A0  | --- | --- | ID3,ID2,ID1,ID0,SDA,SDA,SDA,SCL |
| I2C serial interface | "H" | "L" | "X" | --- | --- | SA0 | SA1 | ID3,ID2,ID1,ID0,SDA,SDA,SDA,SCL |

\* The un-used pins are marked as "---" and should be fixed to "H" by VDD1 or VDDH.

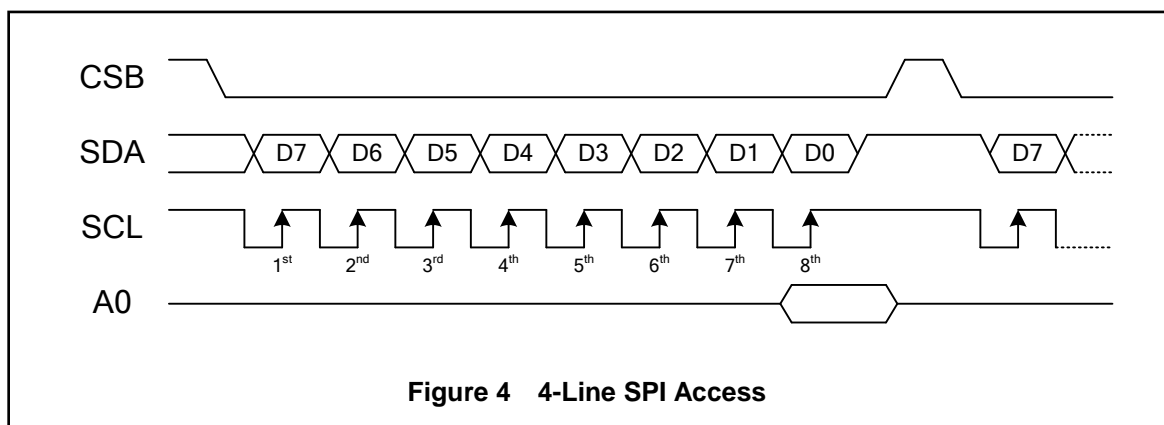
\* C86 is marked as "X" and can be fixed to "H" or "L".

Note:

1. The option setting to be "H" should connect to VDD1 or VDDH.
2. The option setting to be "L" should connect to VSS1 or VSSL.

#### 6-2 4-line SPI interface (SI2="L", PSB="L" and C86="H")

When ST7567A is active (CSB="L"), serial data (SDA) and serial clock (SCL) inputs are enabled. When ST7567A is not active (CSB="H"), the internal 8-bit shift register and 3-bit counter are reset. Serial data on SDA is latched at the rising edge of serial clock on SCL. After the 8<sup>th</sup> serial clock, the serial data will be processed to be 8-bit parallel data. The address selection pin (A0), which is latched at the 8<sup>th</sup> clock, indicates the 8-bit parallel data is display data or instruction. The 8-bit parallel data will be display data when A0 is "H" and will be instruction when A0 is "L". The read feature is not available in this mode. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access. Please note that the SCL signal quality is very important and external noise maybe causes unexpected data/instruction latch.



Note:

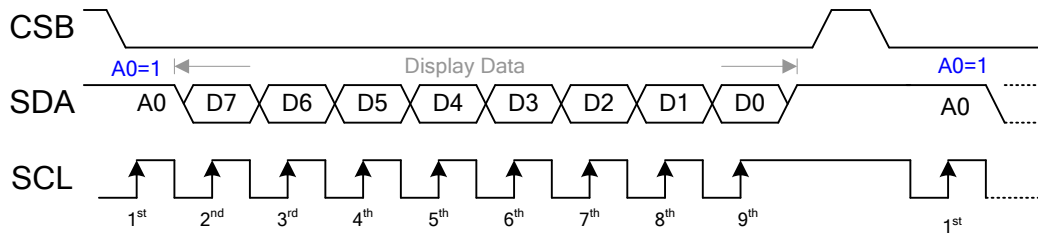
Some MPU will set the interface to be Hi-Z (high impedance) mode when power saving mode or after hardware reset. This is not allowed when the VDD1 of ST7567A is turned ON. Because the floating input (especially for those control pins such as CSB, RSTB, RWR or ERD...) maybe cause abnormal latch and cause abnormal display.

### 6-3 3-line SPI interface (SI2="L", PSB="L" and C86="L")

The 3-Line SPI (9-bit) uses 3 pins (CSB, SDA & SCL) to communicate with MPU. When CSB is "L", IC is active and the SDA and SCL pins are enabled. Serial data is latched at the rising edge of serial clock. The internal shift register collects serial bits and reformat them into 8-bit data after the last (9<sup>th</sup>) clock. After CSB returns to "H", IC is inactive and the internal shift register and counter are reset. The parameter/command indicator is the "A0" bit at the 1<sup>st</sup> bit of each 9-bit serial data.

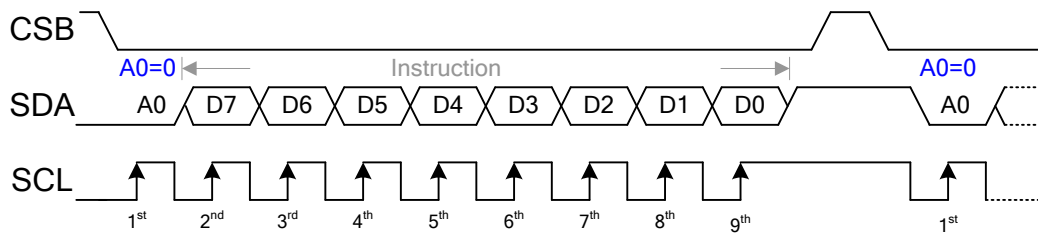
#### Write Parameter by 3-Line SPI (A0=1)

When A0 is "1", the transferred 8-bit is parameter.



#### Write Instruction by 3-Line SPI (A0=0)

When A0 is "0", the transferred 8-bit is instruction.

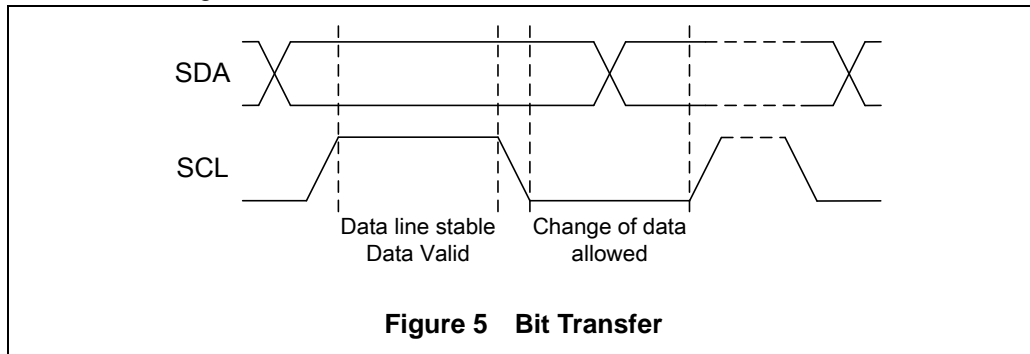


#### 6-4 I2C serial interface (SI2="H, "PSB="L" and C86="X")

The I2C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected with a pull-up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

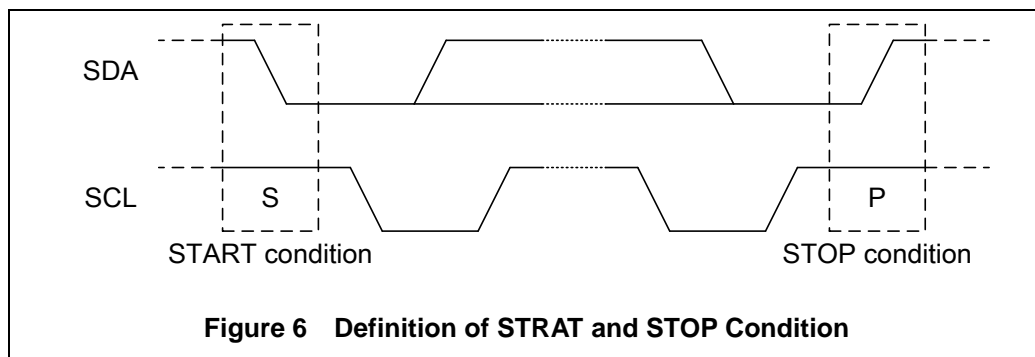
##### 6-4-1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in Fig 5.



##### 6-4-2 Start and Stop Conditions

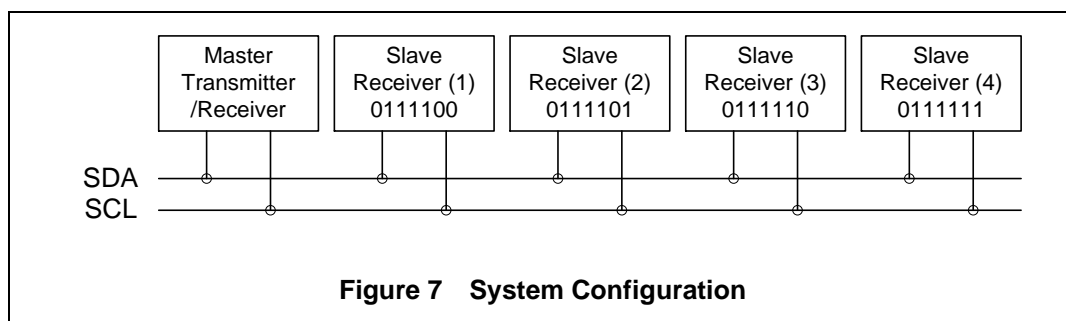
Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig 6.



### 6-4-3 System Configuration

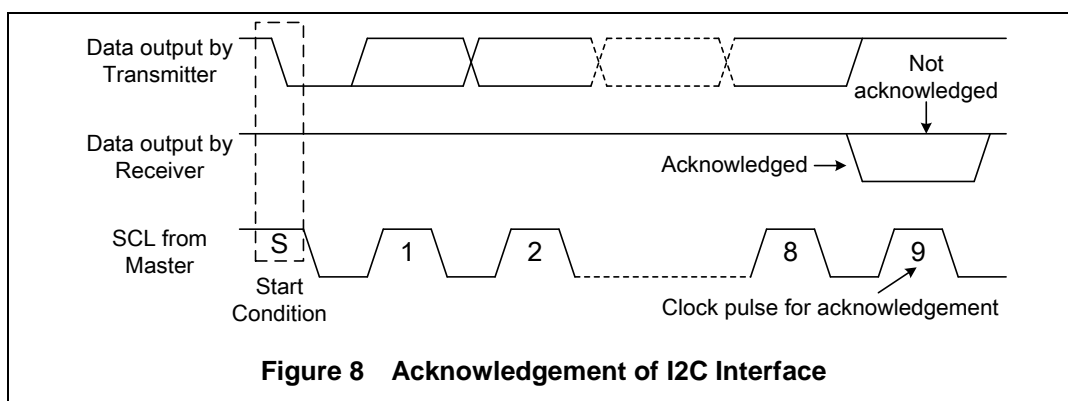
The system configuration is illustrated in Fig. 7 and some word-definitions are explained below:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device which initiates a transfer generates clock signals and terminates a transfer.
- Slave: the device which is addressed by a master.
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.



### 6-4-4 Acknowledgement

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). Acknowledgement on the I2C Interface is illustrated in Fig 8.



#### 6-4-5 I2C Interface Protocol

ST7567A supports command/data write to addressed slaves on the bus.

Before any data is transmitted on the I2C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for ST7567A. The least significant 2 bits of the slave address is set by connecting SA0 and SA1 to either logic 0 (VSSL) or logic 1 (VDDH). The I2C Interface protocol is illustrated in Fig 9.

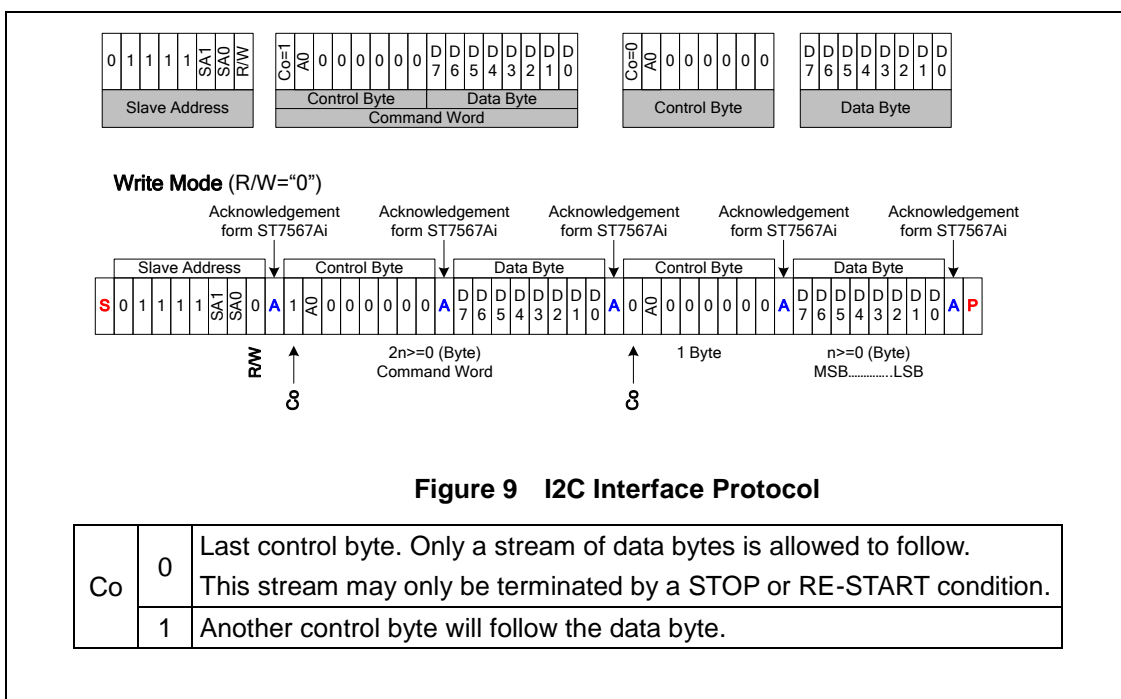
The sequence is initiated with a START condition (S) from the I2C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I2C Interface transfer. After acknowledgement, one or more command words are followed and define the status of the addressed slaves. A command word consists of a control byte, which defines Co and A0, and a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data byte(s) will follow. The state of the A0 bit defines whether the following data bytes are interpreted as commands or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte either a series of display data bytes or command data bytes may follow (depending on the A0 bit setting).

If the A0 bit of the last control byte is set to logic 1, these data bytes (display data bytes) will be stored in the display RAM at the address specified by the internal data pointer. The data pointer is automatically updated and the data is directed to the intended ST7567A device.

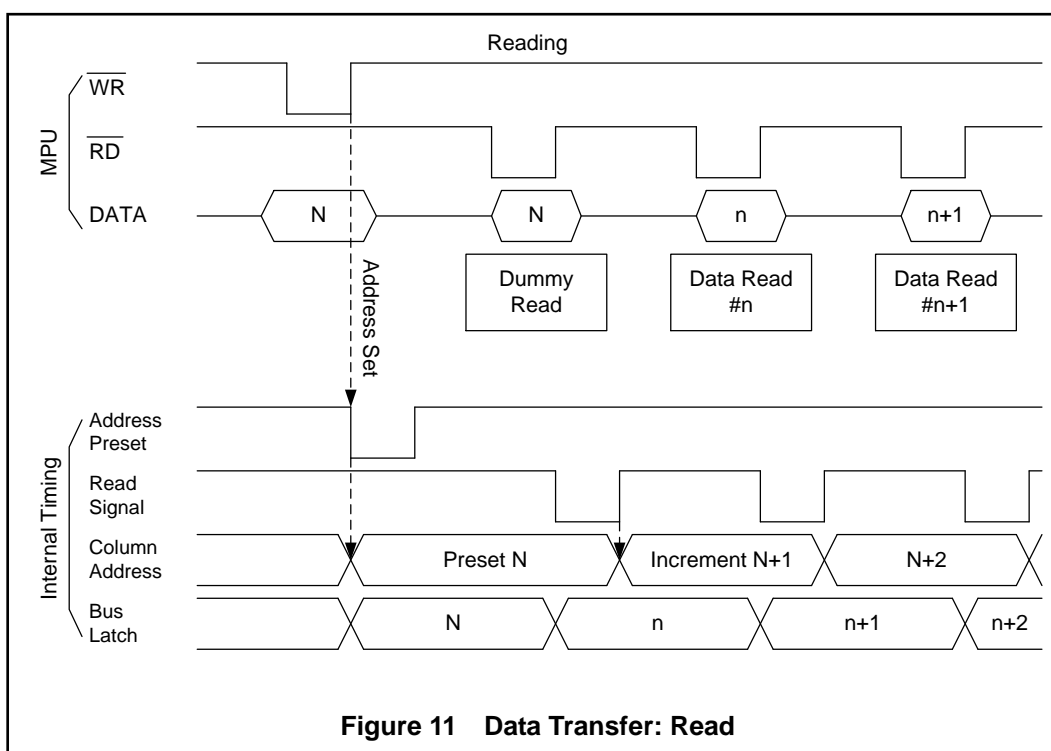
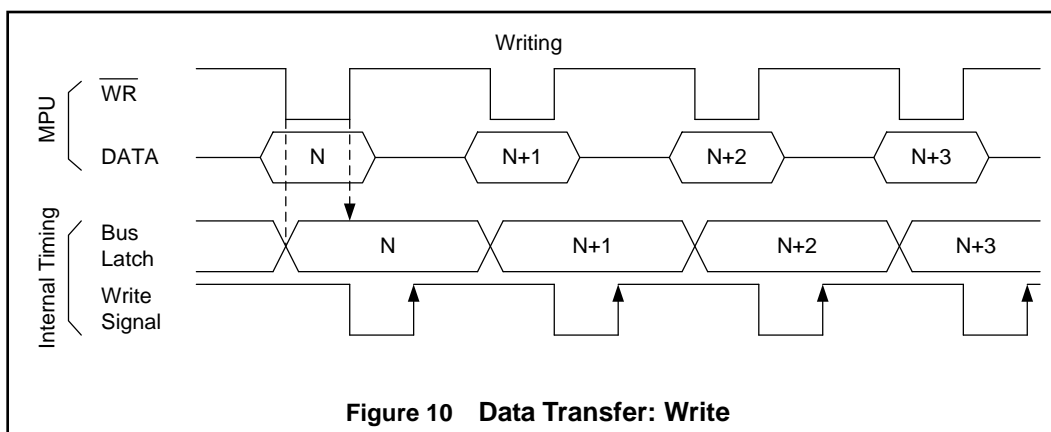
If the A0 bit of the last control byte is set to logic 0, these data bytes (command data byte) will be decoded and the setting of ST7567A will be changed according to the received commands.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.



## 6-5 Data Transfer

ST7567A uses bus latch and internal data bus for parallel interface data transfer. When writing data from MPU to the DDRAM, data is automatically transferred from the bus latch to the DDRAM as shown in Fig.10. When reading data from the on-chip DDRAM to MPU, the first read cycle reads the content in bus latch (dummy read) and the data that MPU should read will be output at the next read cycle as shown in Fig. 11. That means: after setting the target address, a dummy read cycle is required before the following read-operation. Therefore, the data of the specified address cannot be read at the first read of display data right after setting the address, but can be read at the second read of display data.



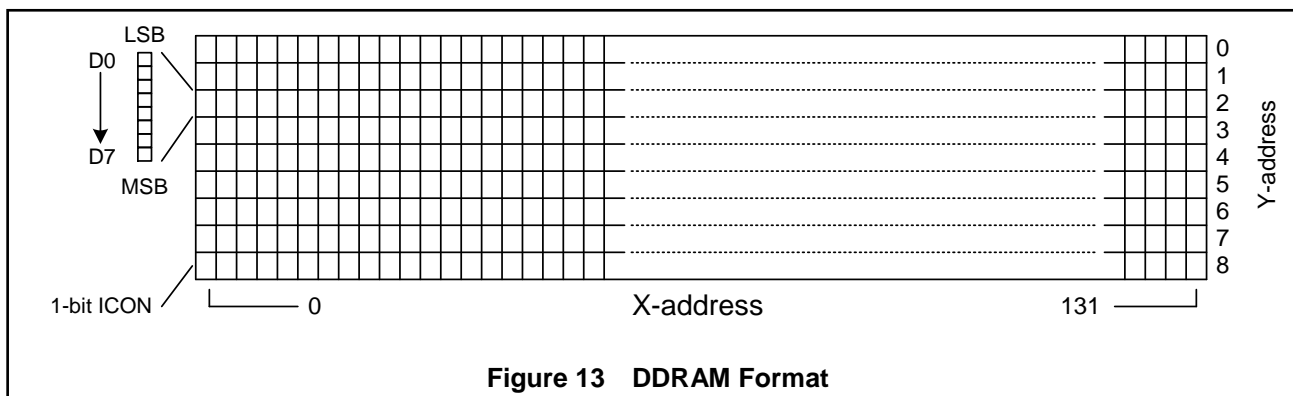
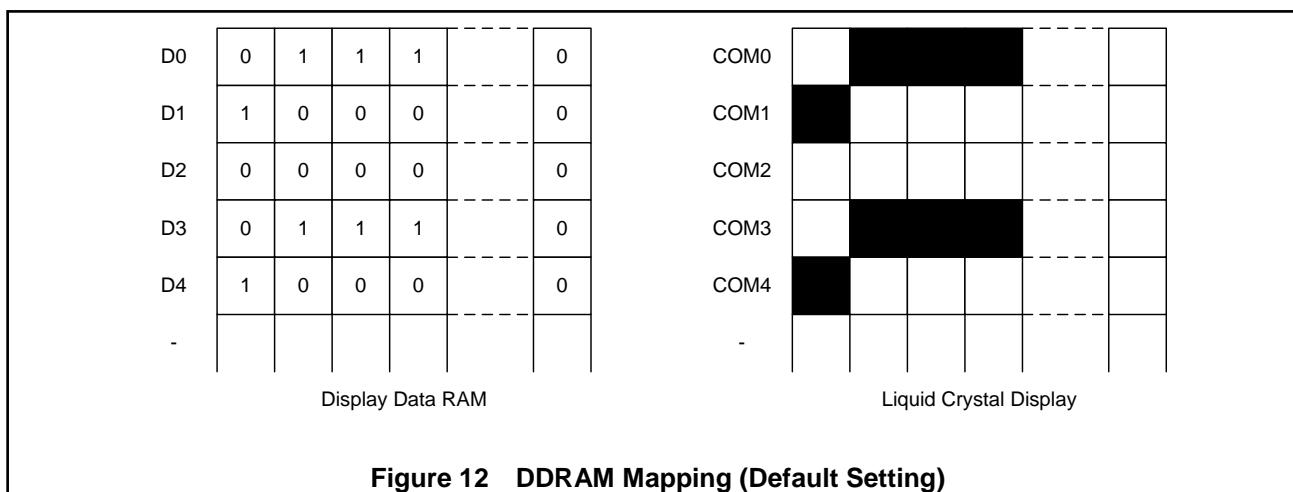
Note: Dummy bit description (Read RAM Mode)

- 8080 interface: 8-bit
- 6800 interface: 8-bit
- 3-Line interface: 1-bit
- 4-Line interface: 1-bit
- I2C interface: 8-bit



## 7 DISPLAY DATA RAM (DDRAM)

ST7567A is built-in a RAM with 132X65 bit capacity which stores the display data. The display data RAM (DDRAM) store the dot data of the LCD. It is an addressable array with 132 columns by 65 rows (8-page with 8-bit and 1-page with 1-bit). The X-address is directly related to the column output number. Each pixel can be selected when the page and column addresses are specified (please refer to Fig.12 detailed illustration). The rows are divided into: 8 pages (Page-0 ~ Page-7) each with 8 lines (for COM0~63) and Page-8 with only 1 line (COMS, for icon). The display data (D7~D0) corresponds to the LCD common-line direction and D0 is on top. All pages can be accessed through D[7:0] directly except icon page. Icon RAM uses only 1-bit of data bus (D0). Refer to Fig. 13 for detailed illustration. The microprocessor can write to and read from DDRAM by the I/O buffer. Since the LCD controller operates independently, data can be written into DDRAM at the same time as data is being displayed without causing the LCD flicker or data-conflict.



### **7-1 Addressing**

Data is downloaded into the Display Data RAM matrix in ST7567A as byte-format. The Display Data RAM has a matrix of 132 by 65 bits. The address ranges are: X=0~131 (column address), Y=0~8 (page address). Addresses outside these ranges are not allowed.

### **7-2 Page Address Circuit**

This circuit provides the page address of DDRAM. It incorporates 4-bit Page Address Register which can be modified by the "Page Address Set" instruction only. The Page Address must be set before accessing DDRAM content. Page Address "8" is a special RAM area for the icons with only one valid bit: D0.

### **7-3 Column Address Circuit**

The column address of DDRAM is specified by the Column Address Set command. Column Address Circuit has 8-bit preset counter that provides Column Address to the Display Data RAM (DDRAM). This allows MPU accessing DDRAM content continuously. The column address is automatically incremented from the start up to the end column. During auto-increment, the column address returns to the start address as the end column (counter value) is reached.

Furthermore, Register MX and MY makes it possible to invert the relationship between the DDRAM and the outputs (COM/SEG). It is necessary to rewrite the display data into DDRAM after changing MX setting.

2016/12/06



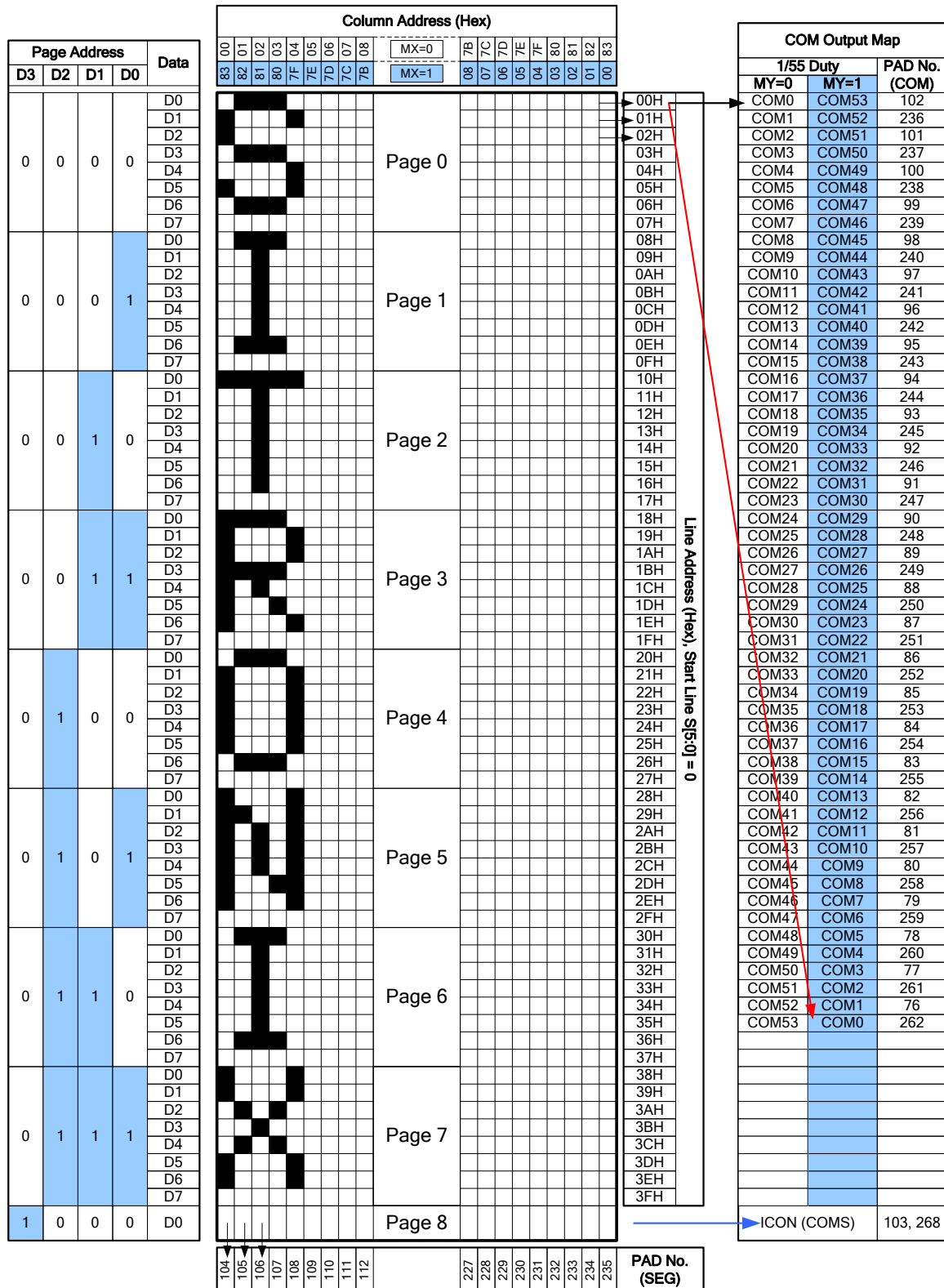


Figure 15 DDRAM and Output Map (COM/SEG) 1/55 Duty

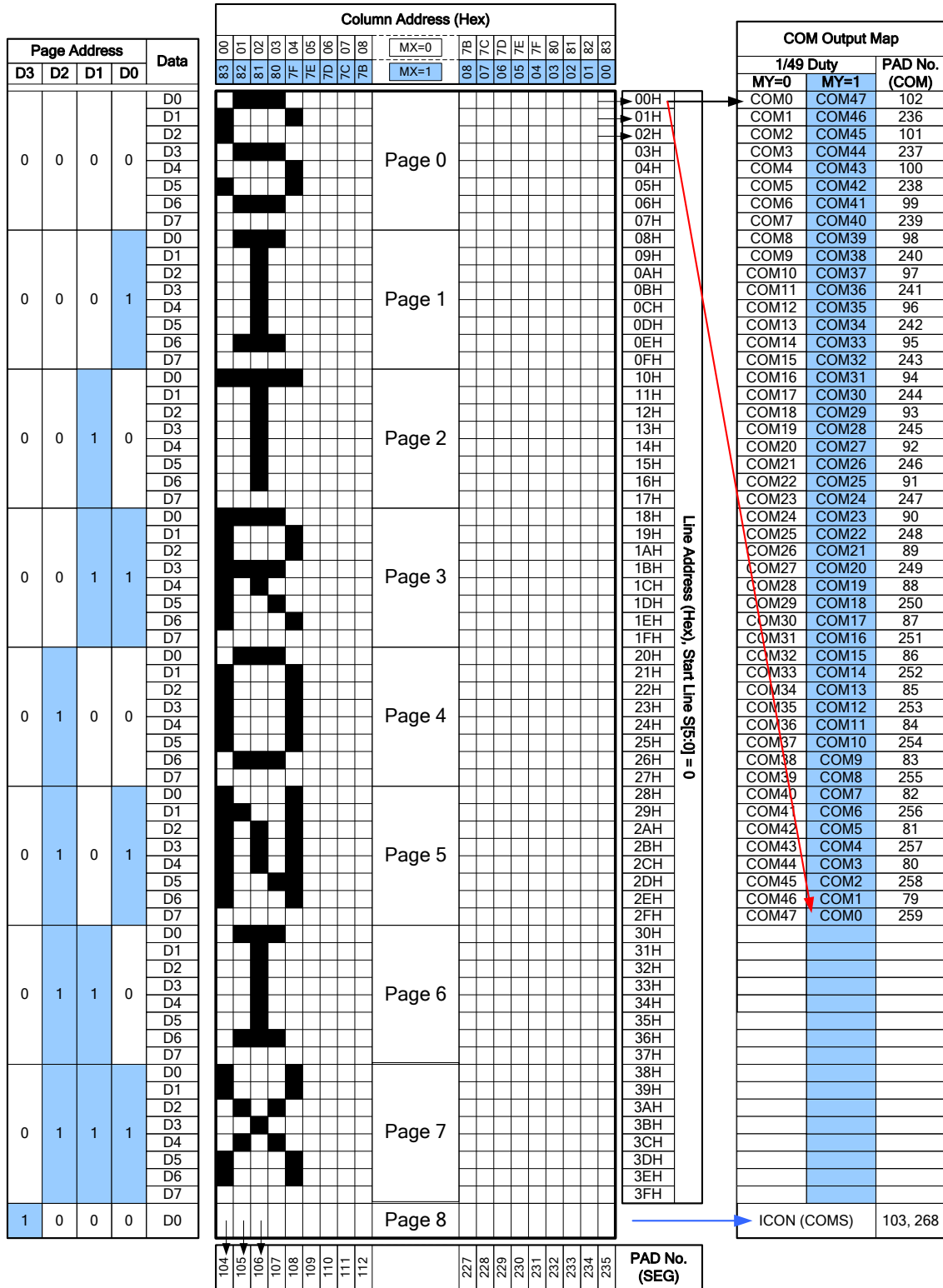


Figure 16 DDRAM and Output Map (COM/SEG) 1/49 Duty

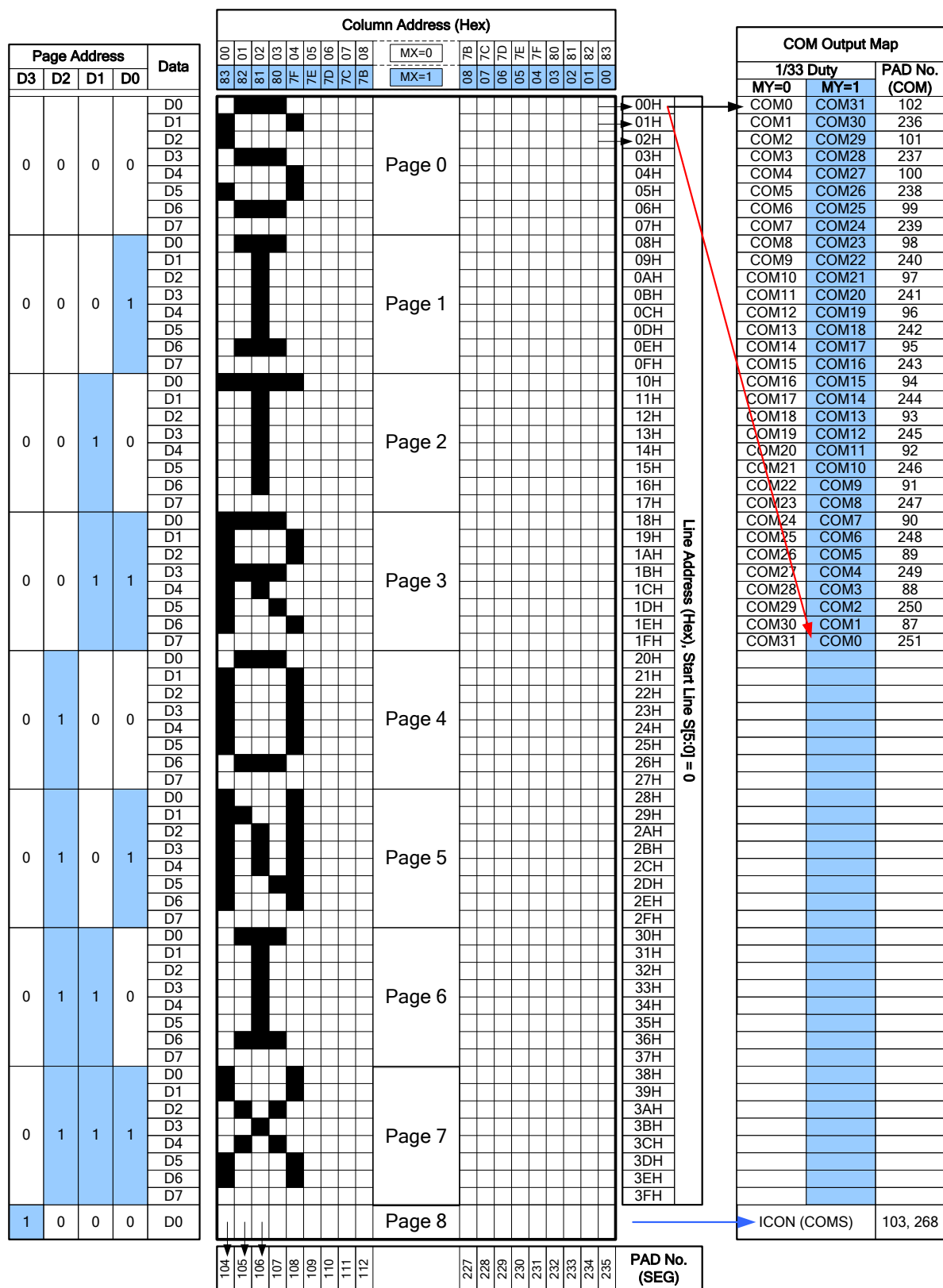
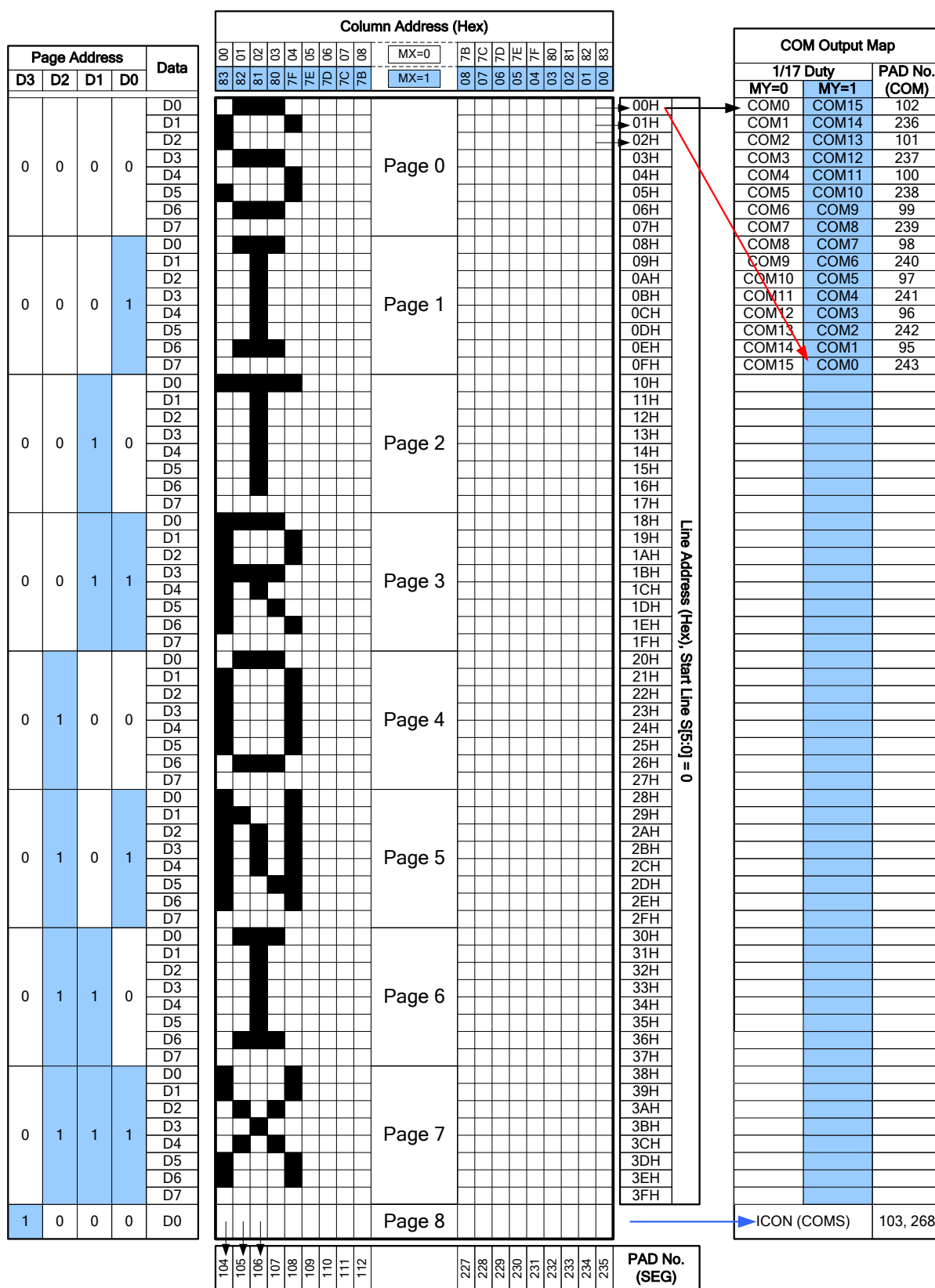


Figure 17 DDRAM and Output Map (COM/SEG) 1/33 Duty



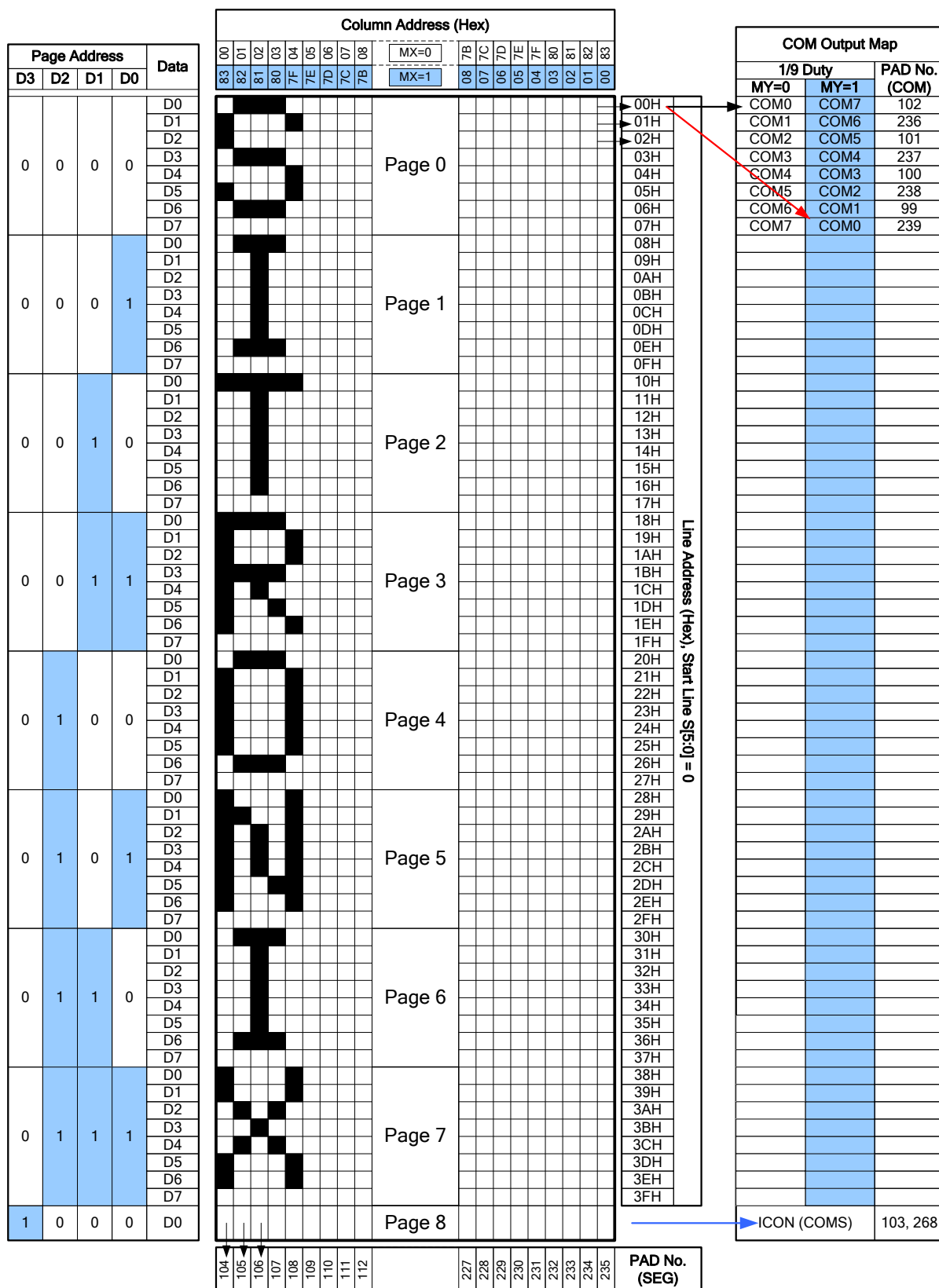


Figure 19 DDRAM and Output Map (COM/SEG) 1/9 Duty





### 7-5 Display Data Latch Circuit

The display data latch circuit latches temporarily display data of each segment output which will be output at the next clock. The special functions such as reverse display, display OFF and display all points ON only change the data in the latch and the content in the Display Data RAM is not changed.

### 7-6 Oscillation Circuit

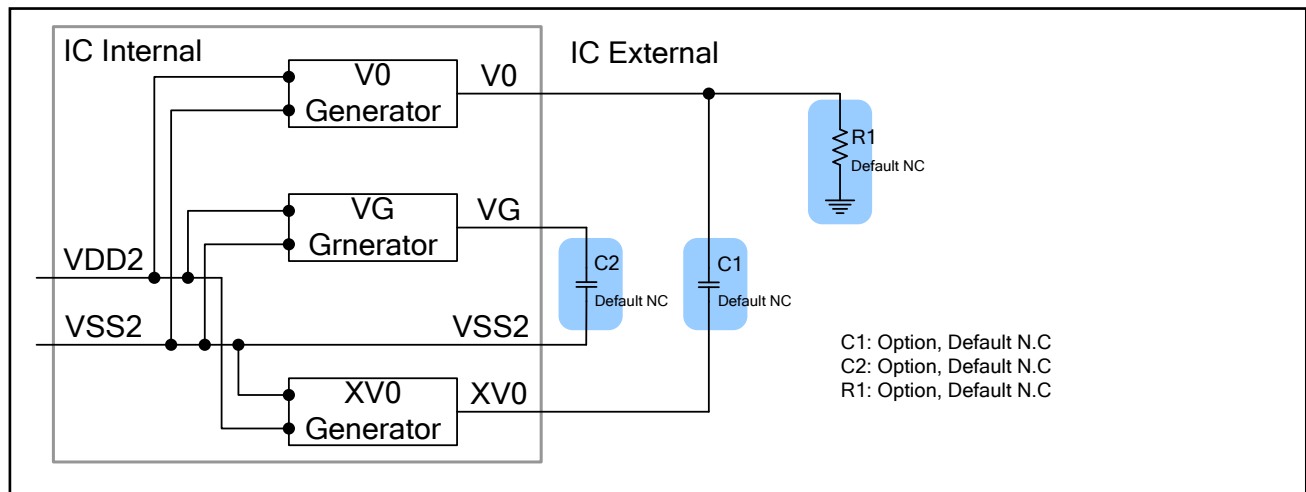
The built-in oscillation circuit generates the system clock for the liquid crystal driving circuit. The oscillation circuit is enabled after initializing ST7567A. The clock will not be output to reduce the power consumption.

### 7-7 Liquid Crystal Driver Power Circuit

The built-in power circuits generate the voltage levels which are necessary to drive the liquid crystal. It consumes low power with the fewest external components. The built-in power system has voltage booster, voltage regulator and voltage follower circuits. Before power ST7567A OFF, a Power OFF procedure is needed (please refer to the OPERATION FLOW section).

### 7-8 External Components of Power Circuit

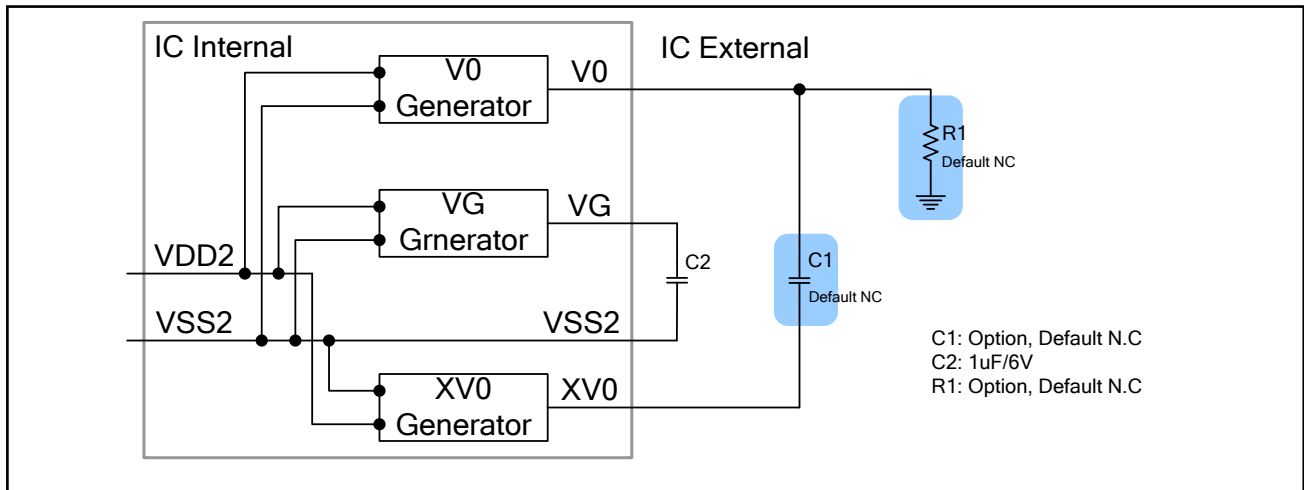
#### Normal Mode



Components selection notes:

- If the panel size is larger than 2" or heavy loading, the capacitor C1 and C2 must be added.
- If the icon is used, the capacitor C1 and C2 must be added.
- If the module is abnormal power down or do not follow the power off sequence, the resistor R1 can be added according to the display performance on LCD panel.
- The referential external component value:  
C1=0.1uF~1.0uF (Non-Polar/25V, default N.C.)  
C2=0.1uF~1.0uF (Non-Polar/6V, default N.C.)  
R1=500KΩ~1MΩ (default N.C.)  
Higher capacitor values are recommended for ripple reduction.
- In order to avoid the characteristic differences of the LCD panel. The capacitor values should be verified according to the display performance on LCD panel.

### High Power Mode



#### Components selection notes:

- If High Power Mode is enabled, the capacitor C2 must be added.
- If the panel size is larger than 2" or heavy loading, the capacitor C1 and C2 must be added.
- If the icon is used, the capacitor C1 and C2 must be added.
- If the module is abnormal power down or do not follow the power off sequence, the resistor R1 can be added according to the display performance on LCD panel.
- The referential external component value:  
C1=0.1uF~1.0uF (Non-Polar/25V, default N.C.)  
C2=0.1uF~1.0uF (Non-Polar/6V, default N.C.)  
R1=500KΩ~1MΩ (default N.C.)  
Higher capacitor values are recommended for ripple reduction.
- In order to avoid the characteristic differences of the LCD panel. The capacitor values should be verified according to the display performance on LCD panel.

### Regulator Circuit

The built-in high accuracy regulation circuit has 8 regulation ratios and each one has 64 EV-levels for voltage adjustment. Without additional external component, the output voltage can be changed by instructions such as "Regulation Ratio" and "Set EV". The detailed setting method can be found in the INSTRUCTION DESCRIPTION section.

## 8 RESET CIRCUIT

Setting RSTB to “L” can initialize internal function. While RSTB is “L”, no instruction except read status can be accepted. RSTB pin must connect to the reset pin of MPU and initialization by RSTB pin is essential before operating. Please note the hardware reset is not same as the software reset. When RSTB becomes “L”, the hardware reset procedure will start. When RESET instruction is executed, the software reset procedure will start. The procedure is listed below:

| Procedure   | Hardware Reset | Software Reset |
|---|----------------|----------------|
| Display OFF: D=0, all SEGs/COMs output at VSS                       | V              | X              |
| Normal Display: INV=0, AP=0   | V              | X              |
| SEG Normal Direction: MX=0  | V              | X              |
| Clear Serial Counter and Shift Register (if using Serial Interface) | V              | X              |
| Bias Selection: BS=0  | V              | X              |
| Booster Level BL=0  | V              | X              |
| Exit Power Saving Mode  | V              | X              |
| Power Control OFF: VB=0, VR=0, VF=0                                 | V              | X              |
| N-Line Inversion NL[4:0] = (0, 1, 1, 0, 0)                          | V              | X              |
| Extension Command Set: Mode=0                                       | V              | X              |
| Display Setting Mode: DSM=0   | V              | X              |
| Duty: DT[3:0]=(0,0,0,0)   | V              | X              |
| Set Bias: BA[2:0]=(0,0,0)   | V              | X              |
| Frame Rate: FR[2:0]=(0,0,0)   | V              | X              |
| Exit Read-modify-Write mode   | V              | V              |
| Start Line S[5:0]=0   | V              | V              |
| Column Address X[7:0]=0   | V              | V              |
| Page Address Y[3:0]=0   | V              | V              |
| COM Normal Direction: MY=0  | V              | V              |
| V0 Regulation Ratio RR[2:0]=(1,0,0)                                 | V              | V              |
| EV[5:0]=(1,0,0,0,0,0)   | V              | V              |

After power-on, RAM data are undefined and the display status is “Display OFF”. It’s better to initialize whole DDRAM (ex: fill all 00h or write the display pattern) before turning the Display ON. Besides, the power is not stable at the time that the power is just turned ON. A hardware reset is needed to initialize those internal registers after the power is stable.

## 9 INSTRUCTION

### 9-1 INSTRUCTION TABLE

| INSTRUCTION            | A0 | R/W<br>(RWR) | COMMAND BYTE     |    |     |     |     |     |     |     | DESCRIPTION  |
|------------------------|----|--------------|------------------|----|-----|-----|-----|-----|-----|-----|--|
|                        |    |              | D7               | D6 | D5  | D4  | D3  | D2  | D1  | D0  |  |
| (1) Display ON/OFF     | 0  | 0            | 1                | 0  | 1   | 0   | 1   | 1   | 1   | D   | D=1, display ON<br>D=0, display OFF  |
| (2) Set Start Line     | 0  | 0            | 0                | 1  | S5  | S4  | S3  | S2  | S1  | S0  | Set display start line   |
| (3) Set Page Address   | 0  | 0            | 1                | 0  | 1   | 1   | Y3  | Y2  | Y1  | Y0  | Set page address   |
| (4) Set Column Address | 0  | 0            | 0                | 0  | 0   | 1   | X7  | X6  | X5  | X4  | Set column address (MSB)   |
|                        | 0  | 0            | 0                | 0  | 0   | 0   | X3  | X2  | X1  | X0  | Set column address (LSB)   |
| (5) Read Status        | 0  | 1            | 0                | MX | D   | RST | 0   | 0   | 0   | 0   | Read IC Status   |
| (6) Write Data         | 1  | 0            | D7               | D6 | D5  | D4  | D3  | D2  | D1  | D0  | Write display data to RAM  |
| (7) Read Data          | 1  | 1            | D7               | D6 | D5  | D4  | D3  | D2  | D1  | D0  | Read display data from RAM   |
| (8) SEG Direction      | 0  | 0            | 1                | 0  | 1   | 0   | 0   | 0   | 0   | MX  | Set scan direction of SEG<br>MX=1, reverse direction<br>MX=0, normal direction   |
| (9) Inverse Display    | 0  | 0            | 1                | 0  | 1   | 0   | 0   | 1   | 1   | INV | INV =1, inverse display<br>INV =0, normal display                                |
| (10) All Pixel ON      | 0  | 0            | 1                | 0  | 1   | 0   | 0   | 1   | 0   | AP  | AP=1, set all pixel ON<br>AP=0, normal display                                   |
| (11) Bias Select       | 0  | 0            | 1                | 0  | 1   | 0   | 0   | 0   | 1   | BS  | Select bias setting<br>0=1/9; 1=1/7 (at 1/65 duty)                               |
| (12) Read-modify-Write | 0  | 0            | 1                | 1  | 1   | 0   | 0   | 0   | 0   | 0   | Column address increment:<br>Read:+0 , Write:+1                                  |
| (13) END               | 0  | 0            | 1                | 1  | 1   | 0   | 1   | 1   | 1   | 0   | Exit Read-modify-Write mode  |
| (14) RESET             | 0  | 0            | 1                | 1  | 1   | 0   | 0   | 0   | 1   | 0   | Software reset   |
| (15) COM Direction     | 0  | 0            | 1                | 1  | 0   | 0   | MY  | -   | -   | -   | Set output direction of COM<br>MY=1, reverse direction<br>MY=0, normal direction |
| (16) Power Control     | 0  | 0            | 0                | 0  | 1   | 0   | 1   | VB  | VR  | VF  | Control built-in power circuit<br>ON/OFF   |
| (17) Regulation Ratio  | 0  | 0            | 0                | 0  | 1   | 0   | 0   | RR2 | RR1 | RR0 | Select regulation resistor ratio   |
| (18) Set EV            | 0  | 0            | 1                | 0  | 0   | 0   | 0   | 0   | 0   | 1   | Double command!! Set<br>electronic volume (EV) level                             |
|                        | 0  | 0            | 0                | 0  | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 |  |
| (19) Set Booster       | 0  | 0            | 1                | 1  | 1   | 1   | 1   | 0   | 0   | 0   | Double command!!<br>Set booster level:<br>BL=0: 4X<br>BL=1: 5X                   |
|                        | 0  | 0            | 0                | 0  | 0   | 0   | 0   | 0   | 0   | BL  |  |
| (20) Power Save        | 0  | 0            | Compound Command |    |     |     |     |     |     |     | Display OFF + All Pixel ON   |
| (21) NOP               | 0  | 0            | 1                | 1  | 1   | 0   | 0   | 0   | 1   | 1   | No operation   |
| (22) Set N-Line        | 0  | 0            | 1                | 0  | 0   | 0   | 0   | 1   | 0   | 1   | Set N-Line inversion   |
|                        | 0  | 0            | 0                | 0  | 0   | NL4 | NL3 | NL2 | NL1 | NL0 |  |
| (23) Release N-Line    | 0  | 0            | 1                | 0  | 0   | 0   | 0   | 1   | 0   | 0   | Exit N-Line inversion  |
| (24) SPI Read Status   | 0  | 1            | 1                | 1  | 1   | 1   | 1   | 1   | 0   | 0   | SPI read status command  |
|                        | 0  | 1            | 0                | MX | D   | RST | ID3 | ID2 | ID1 | ID0 |  |
| (25) SPI Read DDRAM    | 0  | 1            | 1                | 1  | 1   | 1   | 1   | 1   | 0   | 1   | SPI read DDRAM command   |
|                        | 1  | 1            | D7               | D6 | D5  | D4  | D3  | D2  | D1  | D0  |  |

| INSTRUCTION              | A0 | R/W<br>(RWR) | COMMAND BYTE |    |    |    |     |     |     |      | DESCRIPTION   |
|--------------------------|----|--------------|--------------|----|----|----|-----|-----|-----|------|---|
|                          |    |              | D7           | D6 | D5 | D4 | D3  | D2  | D1  | D0   |   |
| EXTENSION COMMAND SET    |    |              |              |    |    |    |     |     |     |      |   |
| Extension Command Set    | 0  | 0            | 1            | 1  | 1  | 1  | 1   | 1   | 1   | Mode | Mode=1: Enter extension command table<br>Mode=0: Exit extension command table |
| (1) High Power Mode ON   | 0  | 0            | 0            | 1  | 1  | 0  | 1   | 0   | 1   | 1    | Enter high power mode   |
| (2) High Power Mode OFF  | 0  | 0            | 0            | 1  | 1  | 0  | 0   | 1   | 0   | 0    | Exit high power mode  |
| (3) Display Setting Mode | 0  | 0            | 0            | 1  | 1  | 1  | -   | -   | DSM | 0    | Complex command   |
|                          | 0  | 0            | 1            | 1  | 0  | 1  | DT3 | DT2 | DT1 | DT0  | DSM=1: Enter display setting  |
|                          | 0  | 0            | 1            | 0  | 0  | 1  | 0   | BA2 | BA1 | BA0  | DSM=0: Exit display setting   |
|                          | 0  | 0            | 1            | 0  | 0  | 1  | 1   | FR2 | FR1 | FR0  | When DSM=1, Set duty(DT[3:0]), bias(BA[2:0]), frame rate(FR[2:0])             |

Note: 1. Symbol “-” means this bit can be “H” or “L”.

2. Do not use instructions not listed in these tables.

## 9-2 INSTRUCTION DESCRIPTION

### 9-2-1 Display ON/OFF

The D flag selects the display mode.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 0  | 1  | 0  | 1  | 1  | 1  | D  |

D=1: Normal Display Mode.

D=0: Display OFF. All SEGs/COMs output with VSS.

### 9-2-2 Set Start Line

This instruction sets the line address of the Display Data RAM to determine the initial display line. The display data of the specified line address is displayed at the top row (COM0) of the LCD panel.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 0  | 1  | S5 | S4 | S3 | S2 | S1 | S0 |

| S5 | S4 | S3 | S2 | S1 | S0 | Line address |
|----|----|----|----|----|----|--------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0            |
| 0  | 0  | 0  | 0  | 0  | 1  | 1            |
| 0  | 0  | 0  | 0  | 1  | 0  | 2            |
| 0  | 0  | 0  | 0  | 1  | 1  | 3            |
| :  | :  | :  | :  | :  | :  | :            |
| 1  | 1  | 1  | 1  | 0  | 1  | 61           |
| 1  | 1  | 1  | 1  | 1  | 0  | 62           |
| 1  | 1  | 1  | 1  | 1  | 1  | 63           |

### 9-2-3 Set Page Address

Y [3:0] defines the Y address vector address of the display RAM.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 0  | 1  | 1  | Y3 | Y2 | Y1 | Y0 |

| Y3 | Y2 | Y1 | Y0 | Page Address      | Valid Bit |
|----|----|----|----|-------------------|-----------|
| 0  | 0  | 0  | 0  | Page0             | D0~ D7    |
| 0  | 0  | 0  | 1  | Page1             | D0~ D7    |
| 0  | 0  | 1  | 0  | Page2             | D0~ D7    |
| :  | :  | :  | :  | :                 | :         |
| 0  | 1  | 1  | 0  | Page6             | D0~ D7    |
| 0  | 1  | 1  | 1  | Page7             | D0~ D7    |
| 1  | 0  | 0  | 0  | Page8 (icon page) | D0        |

## 9-2-4 Set Column Address

This instruction is used to define area of DDRAM where MCU can access. The column address is automatically increased by one after each byte of display data access (read/write). The X[7:0] setting that must be less than or equal to "83h". If X[7:0] setting is great than 83h, out of DDRAM range will be ignored.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 0  | 0  | 0  | 1  | X7 | X6 | X5 | X4 |

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 0  | 0  | 0  | 0  | X3 | X2 | X1 | X0 |

| X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 | Column Address |
|----|----|----|----|----|----|----|----|----------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0              |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1              |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 2              |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 3              |
| :  | :  | :  | :  | :  | :  | :  | :  | :              |
| 1  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 129            |
| 1  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 120            |
| 1  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 131            |

## 9-2-5 Read Status

Read the internal status of ST7567A. The read function is not available in serial interface mode.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4  | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|-----|----|----|----|----|
| 0  | 1        | 0  | MX | D  | RST | 0  | 0  | 0  | 0  |

| Flag | Description   |
|------|---|
| MX   | MX=0: Normal direction (SEG0->SEG131)<br>MX=1: Reverse direction (SEG131->SEG0) |
| D    | D=0: Display ON<br>D=1: Display OFF   |
| RST  | RST=1: During reset (hardware or software reset)<br>RST=0: Normal operation     |

## 9-2-6 Write Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

| A0 | R/W(RWR) | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|------------|----|----|----|----|----|----|----|
| 1  | 0        | Write Data |    |    |    |    |    |    |    |

## 9-2-7 Read Data

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor.

| A0 | R/W(RWR) | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|-----------|----|----|----|----|----|----|----|
| 1  | 1        | Read Data |    |    |    |    |    |    |    |



#### 9-2-8 SEG Direction

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 0  | 1  | 0  | 0  | 0  | 0  | MX |

| Flag | Description   |
|------|---|
| MX   | MX=0: Normal direction (SEG0->SEG131)<br>MX=1: Reverse direction (SEG131->SEG0) |

#### 9-2-9 Inverse Display

This instruction changes the selected and non-selected voltage of SEG. The display will be inversed (White -> Black, Black -> White) while the display data in the Display Data RAM is never changed.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0  |
|----|----------|----|----|----|----|----|----|----|-----|
| 0  | 0        | 1  | 0  | 1  | 0  | 0  | 1  | 1  | INV |

| Flag | Description                                     |
|------|---|
| INV  | INV=0: Normal display<br>INV=1: Inverse display |

#### 9-2-10 All Pixel ON

This instruction will let all segments output the selected voltage and make all pixels turned ON.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 0  | 1  | 0  | 0  | 1  | 0  | AP |

| Flag | Description                                 |
|------|---|
| AP   | AP=0: Normal display<br>AP=1: All pixels ON |

#### 9-2-11 Bias Select

Select LCD bias ratio of the voltage required for driving the LCD.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 0  | 1  | 0  | 0  | 0  | 1  | BS |

| Duty | Bias |      |
|------|------|------|
|      | BS=0 | BS=1 |
| 1/65 | 1/9  | 1/7  |
| 1/49 | 1/8  | 1/6  |
| 1/33 | 1/6  | 1/5  |
| 1/55 | 1/8  | 1/6  |

Reference LCD Bias Voltage (1/65 Duty with 1/9 Bias)

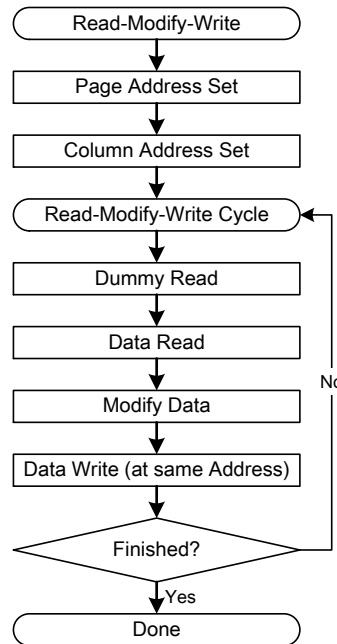
| Symbol | Bias Voltage |
|--------|--------------|
| V0     | V0           |
| VG     | 2/9 x V0     |
| VM     | 1/9 x V0     |
| VSS    | VSS          |

### 9-2-12 Read-modify-Write

This command is used paired with the “END” instruction. Once this command has been input, the display data read operation will not change the column address, but only the display data write operation will increase the column address ( $X[7:0]+1$ ). This mode is maintained until the END command is input. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as a blanking cursor.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 0  |

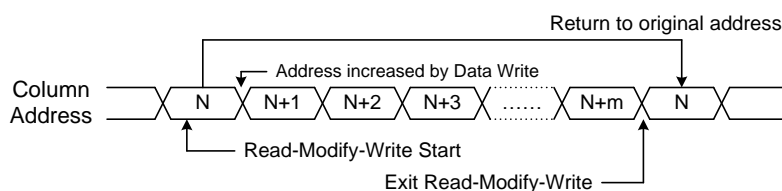
⇒ In Read-modify-Write mode, other instructions aside from display data read/write commands can also be used.



### 9-2-13 END

When the END command is input, the Read-modify-Write mode is released and the column address returns to the address it was when the Read-modify-Write instruction was entered.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 0  |



### 9-2-14 RESET

This instruction resets Start Line ( $S[5:0]$ ), Column Address ( $X[7:0]$ ), Page Address ( $Y[3:0]$ ) and COM Direction (MY) to their default setting. Please note this instruction is not complete same as hardware reset ( $RSTB=L$ ) and cannot initialize the built-in power circuit which is initialized by the RSTB pin. The detailed information is in “Section 8 Reset Circuit”.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 1  | 1  | 0  | 0  | 0  | 1  | 0  |

### 9-2-15 COM Direction

This instruction controls the common output status which changes the vertical display direction. The detailed information can be found in Fig 14~17.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 1  | 0  | 0  | MY | -  | -  | -  |

| Flag | Description   |
|------|---|
| MY   | MY=0: Normal direction (COM0->COM63)<br>MY=1: Reverse direction (COM63->COM0) |

### 9-2-16 Power Control

This instruction controls the built-in power circuits. Typically, these 3 flags are turned ON at the same time.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 0  | 0  | 1  | 0  | 1  | VB | VR | VF |

| Flag | Description   |
|------|---|
| VB   | VB=0: Built-in Booster OFF<br>VB=1: Built-in Booster ON     |
| VR   | VR=0: Built-in Regulator OFF<br>VR=1: Built-in Regulator ON |
| VF   | VF=0: Built-in Follower OFF<br>VF=1: Built-in Follower ON   |

### 9-2-17 Regulation Ratio

This instruction controls the regulation ratio of the built-in regulator.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2  | D1  | D0  |
|----|----------|----|----|----|----|----|-----|-----|-----|
| 0  | 0        | 0  | 0  | 1  | 0  | 0  | RR2 | RR1 | RR0 |

| RR2 | RR1 | RR0 | Regulation Ratio (RR) |
|-----|-----|-----|-----------------------|
| 0   | 0   | 0   | 3.0                   |
| 0   | 0   | 1   | 3.5                   |
| 0   | 1   | 0   | 4.0                   |
| 0   | 1   | 1   | 4.5                   |
| 1   | 0   | 0   | 5.0                   |
| 1   | 0   | 1   | 5.5                   |
| 1   | 1   | 0   | 6.0                   |
| 1   | 1   | 1   | 6.5                   |

The operation voltage (V0) calculation formula is shown below: (RR comes from Regulation Ratio, EV comes from EV[5:0])

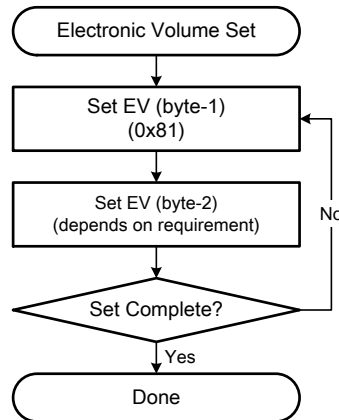
$V0 = RR \times [1 - (63 - EV) / 162] \times 2.1$ , or  $V0 = RR \times [(99 + EV) / 162] \times 2.1$

| SYMBOL | REGISTER | VALUE                                     |
|--------|----------|---|
| RR     | RR[2:0]  | 3.0, 3.5, 4.0, 4.5, 5.0, 5.5, 6.0 and 6.5 |
| EV     | EV[5:0]  | 0~63                                      |

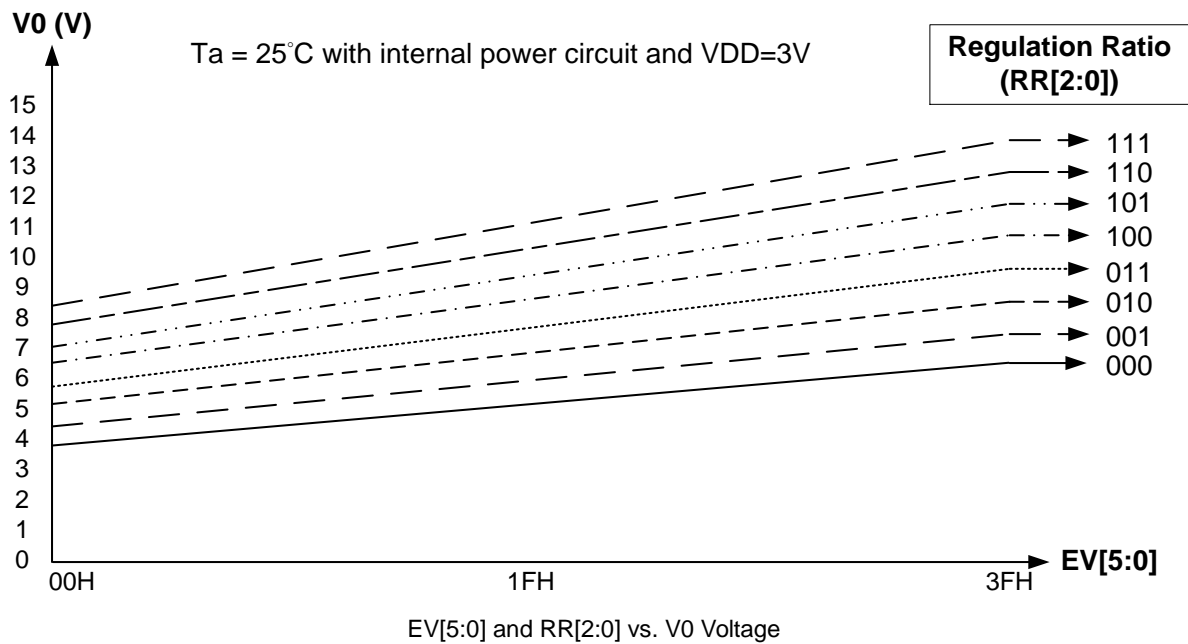
### 9-2-18 Set EV

This is double byte instruction. The first byte set ST7567A into EV adjust mode and the following instruction will change the EV setting. That means these 2 bytes must be used together. They control the electronic volume to adjust a suitable V0 voltage for the LCD.

| A0 | R/W(RWR) | D7 | D6 | D5  | D4  | D3  | D2  | D1  | D0  |
|----|----------|----|----|-----|-----|-----|-----|-----|-----|
| 0  | 0        | 1  | 0  | 0   | 0   | 0   | 0   | 0   | 1   |
| 0  | 0        | 0  | 0  | EV5 | EV4 | EV3 | EV2 | EV1 | EV0 |



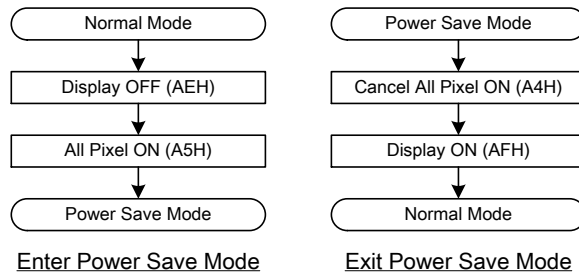
The maximum voltage that can be generated is dependent on the VDD2 voltage and the loading of LCD module. There are 8 V0 voltage curve can be selected. It is recommended the EV should be close to the center (1FH) for easy contrast adjustment.



### 9-2-19 Power Save (Compound Instruction)

This is compound instruction. The 1<sup>st</sup> instruction is Display OFF (D=0) and the 2<sup>nd</sup> instruction is All Pixel ON (AP=1). The Power Save mode starts the following procedure: (the display data and register settings are still kept except D-Flag and AP-Flag)

1. Stops internal oscillation circuit;
2. Stops the built-in power circuits;
3. Stops the LCD driving circuits and keeps the common and segment outputs at VSS.



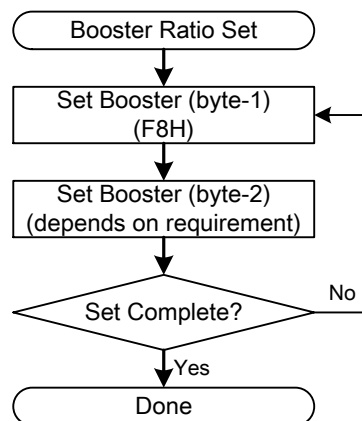
After exiting Power Save mode, the settings will return to be as they were before.

### 9-2-20 Set Booster

This is double byte instruction. The first byte set ST7567A into booster configuration mode and the following instruction will change the booster setting. That means these 2 bytes must be used together. They control the built-in booster circuit to provide the power source of the built-in regulator. ST7567A booster is built-in booster capacitors. Booster level can be changed with instruction only without changing hardware connection.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 1  | 1  | 1  | 1  | 0  | 0  | 0  |
| 0  | 0        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | BL |

| BL | Boost Level |
|----|-------------|
| 0  | X4          |
| 1  | X5          |



### 9-2-21 NOP

"No Operation" instruction. ST7567A will do nothing when receiving this instruction.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 1  | 1  | 0  | 0  | 0  | 1  | 1  |

### 9-2-22 Set N-Line

This 2-byte instruction sets the inverted line number within range of 1 to 32 to improve the display quality by controlling the phase of the internal frame signal. The DC bias maybe occurred if the N-line is not set well. Be sure to confirm this factor after choosing a value of N.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4  | D3  | D2  | D1  | D0  |
|----|----------|----|----|----|-----|-----|-----|-----|-----|
| 0  | 0        | 1  | 0  | 0  | 0   | 0   | 1   | 0   | 1   |
| 0  | 0        | 0  | 0  | 0  | NL4 | NL3 | NL2 | NL1 | NL0 |

| NL4 | NL3 | NL2 | NL1 | NL0 | Selected N-Line Inversion |
|-----|-----|-----|-----|-----|---------------------------|
| 0   | 0   | 0   | 0   | 0   | 1-line inversion          |
| 0   | 0   | 0   | 0   | 1   | 2-line inversion          |
| 0   | 0   | 0   | 1   | 0   | 3-line inversion          |
| :   | :   | :   | :   | :   | :                         |
| 1   | 1   | 1   | 0   | 1   | 30-line inversion         |
| 1   | 1   | 1   | 1   | 0   | 31-line inversion         |
| 1   | 1   | 1   | 1   | 1   | 32-line inversion         |

### 9-2-23 Release N-Line

This instruction makes the inversion mode back to the frame inversion from the N-Line inversion.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 1  | 0  | 0  | 0  | 0  | 1  | 0  | 0  |

### 9-2-24 SPI Read Status

Indicate the status of read by 3-Line and 4-Line SPI

| A0 | R/W(RWR) | D7 | D6 | D5 | D4  | D3  | D2  | D1  | D0  |
|----|----------|----|----|----|-----|-----|-----|-----|-----|
| 0  | 1        | 1  | 1  | 1  | 1   | 1   | 1   | 0   | 0   |
| 0  | 1        | 0  | MX | D  | RST | ID3 | ID2 | ID1 | ID0 |

### 9-2-25 SPI Read DDRAM

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 1        | 1  | 1  | 1  | 1  | 1  | 1  | 0  | 1  |
| 1  | 1        | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

### 9-2-26 Extension Command Set

This instruction enables the extension command set.

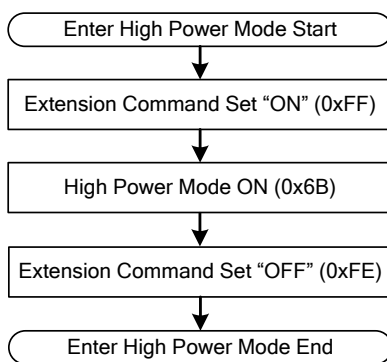
| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0   |
|----|----------|----|----|----|----|----|----|----|------|
| 0  | 0        | 1  | 1  | 1  | 1  | 1  | 1  | 1  | Mode |

| Flag | Description   |
|------|---|
| Mode | Mode=0: Exit extension command set<br>Mode=1: Enter extension command set |

### 9-2-27 High Power Mode ON

This instruction makes the High Power Mode turn on. This feature should be turned on when the VG exceed VDD.

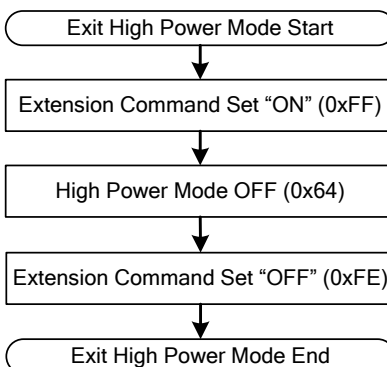
| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 0  | 1  | 1  | 0  | 1  | 0  | 1  | 1  |



### 9-2-28 High Power Mode OFF

This instruction makes the High Power Mode turn off.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----------|----|----|----|----|----|----|----|----|
| 0  | 0        | 0  | 1  | 1  | 0  | 0  | 1  | 0  | 0  |



### 9-2-29 Display Setting Mode

This instruction enables Display Setting Mode. The duty, bias, and frame rate must be initialized by command when display setting mode is enabled.

| A0 | R/W(RWR) | D7 | D6 | D5 | D4 | D3  | D2  | D1  | D0  |
|----|----------|----|----|----|----|-----|-----|-----|-----|
| 0  | 0        | 0  | 1  | 1  | 1  | -   | -   | DSM | 0   |
| 0  | 0        | 1  | 1  | 0  | 1  | DT3 | DT2 | DT1 | DT0 |
| 0  | 0        | 1  | 0  | 0  | 1  | 0   | BA2 | BA1 | BA0 |
| 0  | 0        | 1  | 0  | 0  | 1  | 1   | FR2 | FR1 | FR0 |

| Flag | Description   |
|------|---|
| DSM  | DSM=0: Exit display setting mode<br>DSM=1: Enter display setting mode |

DT[3:0] sets the display duty and has priority over the SEL[2:1].

| DT3 | DT2 | DT1 | DT0 | Selected Duty Ratio |
|-----|-----|-----|-----|---------------------|
| 0   | 1   | 0   | 0   | 65 (1/64+1 icon)    |
| 0   | 1   | 1   | 1   | 55 (1/54+1 icon)    |
| 0   | 1   | 0   | 1   | 49 (1/48+1 icon)    |
| 0   | 1   | 1   | 0   | 33 (1/32+1 icon)    |
| 1   | 1   | 1   | 0   | 17 (1/16+1 icon)    |
| 1   | 0   | 1   | 0   | 9 (1/8+1 icon)      |

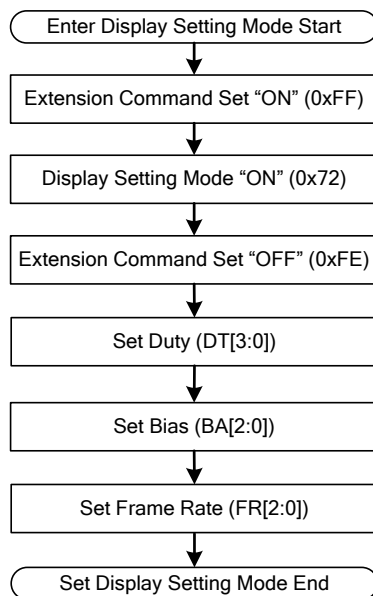
BA[2:0] selects LCD bias ratio for the internal voltage follower to drive the LCD. This command has priority over the Bias Select (BS).

| BA2 | BA1 | BA0 | Bias |
|-----|-----|-----|------|
| 0   | 0   | 0   | 1/9  |
| 1   | 0   | 0   | 1/8  |
| 0   | 0   | 1   | 1/7  |
| 1   | 0   | 1   | 1/6  |
| 0   | 1   | 1   | 1/5  |
| 1   | 1   | 0   | 1/4  |

FR[2:0] specifies the frame rate for different duty.

| FR2 | FR1 | FR0 | Frame Rate(Hz)   |                   |
|-----|-----|-----|------------------|-------------------|
|     |     |     | 9 duty ~ 17 duty | 33 duty ~ 65 duty |
| 0   | 0   | 0   | 70               | 75                |
| 0   | 0   | 1   | 105              | 110               |
| 0   | 1   | 0   | 140              | 150               |
| 0   | 1   | 1   | 175              | 190               |
| 1   | 0   | 0   | 195              | 220               |
| 1   | 0   | 1   | 230              | 250               |
| 1   | 1   | 0   | 275              | 300               |

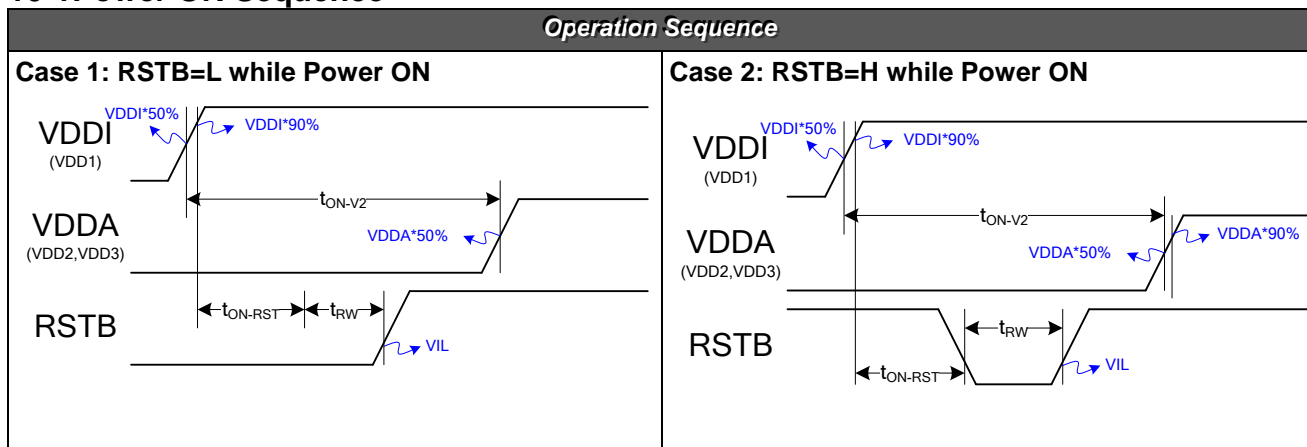




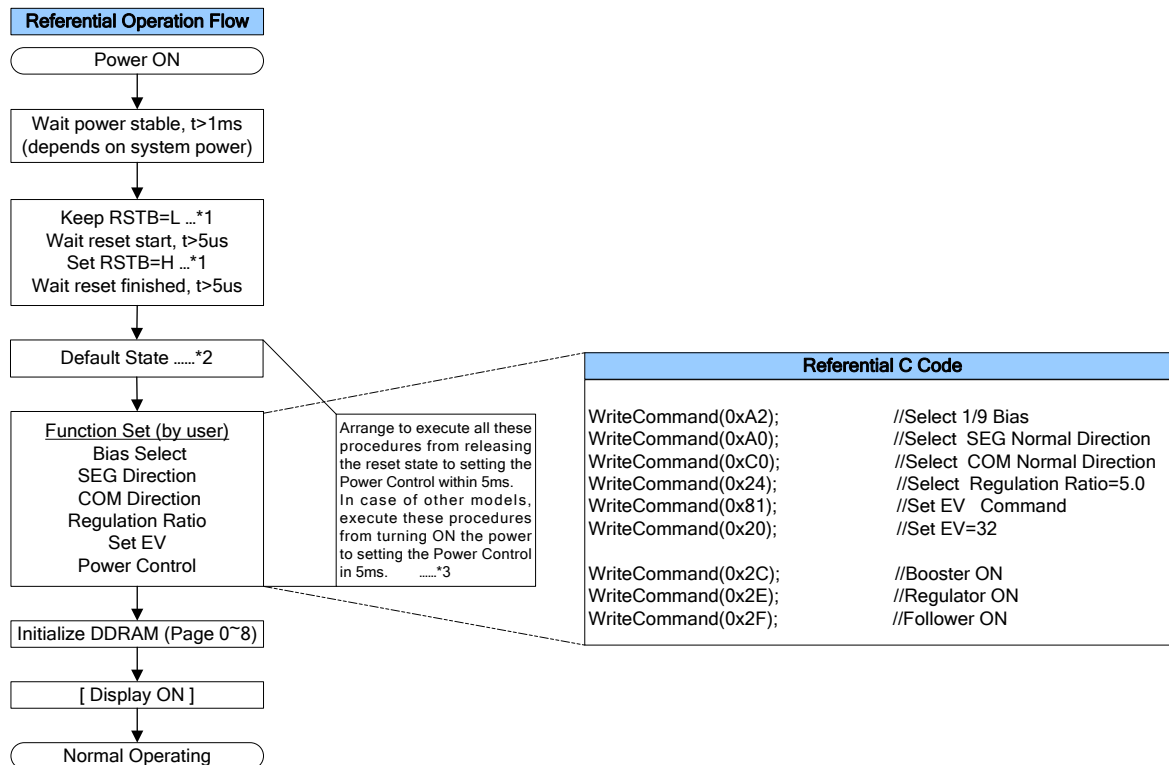
## 10. OPERATION FLOW

This section introduces some reference operation flows.

### 10-1 Power ON Sequence



### Power ON Operation Flow



Note: The detailed description can be found in the respective sections listed below.

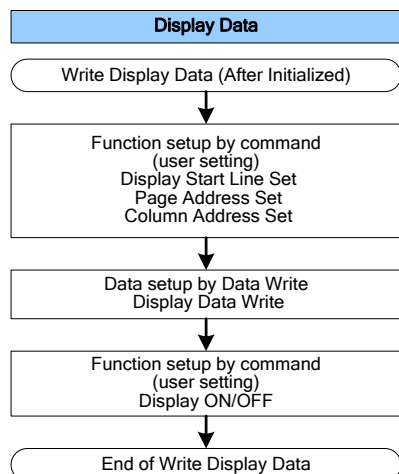
1. Please refer to the timing specification of  $t_{RW}$  and  $t_R$ .
2. Refer to Section 8 Reset Circuit.
3. The 5ms requirement depends on the characteristics of LCD panel and the external component of the power circuit. It is recommended to check with the real products with external component.
4. The detailed instruction functionality is described in Section 9-2 INSTRUCTION INTRODUCTION;
5. Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage.

**Timing Requirement:**

| Item             | Symbol       | Requirement        | Note  |
|------------------|--------------|--------------------|---|
| VDDA power delay | $t_{ON-V2}$  | $0 \leq t_{ON-V2}$ | <ul style="list-style-type: none"> <li>Applying VDDI and VDDA in any order will not damage IC.</li> </ul>   |
| RSTB input time  | $t_{ON-RST}$ | No Limitation      | <ul style="list-style-type: none"> <li>If RSTB is Low, High or unstable during power ON, a successful hardware reset by RSTB is required after VDDI is stable.</li> <li>RSTB=L can be input at any time after power is stable.</li> <li><math>t_{RW}</math> &amp; <math>t_R</math> should match the timing specification of RSTB.</li> <li>To prevent abnormal display, the recommended timing is: <math>1ms \leq t_{ON-RST} \leq 30\ ms</math>.</li> </ul> |

- The requirement listed here is to prevent abnormal display on LCD module.

## 10-2 Display Data



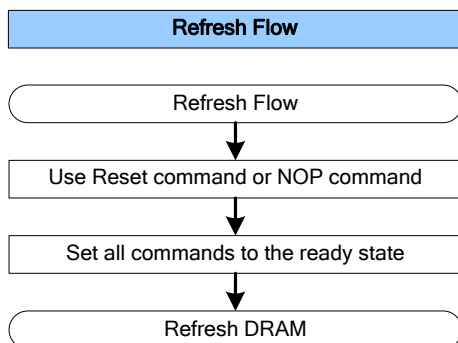
| Reference C Code                      |                               |
|---------------------------------------|-------------------------------|
| Extern unsigned char picture[8][132]; | //Picture must be set         |
| Void WriteDisplayData(void)           |                               |
| {                                     |                               |
| int page=0; column=0;                 | //Picture data                |
| int pageAddr=0xB0;                    | //Set page=page0              |
| WriteCommand(0x40);                   | //Set start line address=0x00 |
| for( page=0; page<9; page++)          | //Send picture data           |
| {                                     | //From page 0 to page 8       |
| WriteCommand(pageAddr);               | //Set Page                    |
| WriteCommand(0x10);                   | //Set MSB Column address      |
| WriteCommand(0x00);                   | //Set LSB Column address      |
| for( column=0; column<132; column++)  | //Send picture data           |
| {                                     | //From column 0 to column 132 |
| WriteData(picture[page][column]);     | //Write picture data          |
| }  pageAddr++;                        | //Set page= next page         |
| }                                     |                               |
| WriteCommand(0xAF);                   | //Display ON(0xAF)            |
| }                                     |                               |

Notes: Reference items

1. The detailed instruction functionality is described in Section
2. It is recommended to write display data (initialize DDRAM) before Display ON.

## 10-3 Refresh

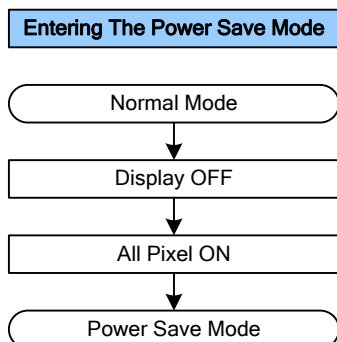
It is recommended to use the refresh sequence regularly in a specified interval.



| Use Reset command or NOP command |                               |
|----------------------------------|-------------------------------|
| WriteCommand(0xE2);              | //SoftwareReset               |
| or                               |                               |
| WriteCommand(0xE3);              | //NOP                         |
| WriteCommand(0xA2);              | //Select 1/9Bias              |
| WriteCommand(0xA0);              | //Select SEG Normal Direction |
| WriteCommand(0xC0);              | //Select COM Normal Direction |
| WriteCommand(0x24);              | //Select Regulation Ratio=5.0 |
| WriteCommand(0x81);              | //Set EV Command              |
| WriteCommand(0x20);              | //Set EV=32                   |
| WriteCommand(0x2C);              | //Booster ON                  |
| WriteCommand(0x2E);              | //Regulator ON                |
| WriteCommand(0x2F);              | //Follower ON                 |
| WriteDisplayData();              | //WriteDisplayData            |

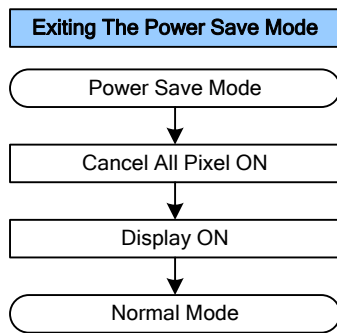
## 10-4 Power-Save Flow and Sequence

Entering the Power Save Mode:



| Reference C Code     |                |
|----------------------|----------------|
| WriteCommand (0xAE); | //Display OFF  |
| WriteCommand (0xA5); | //All Pixel ON |

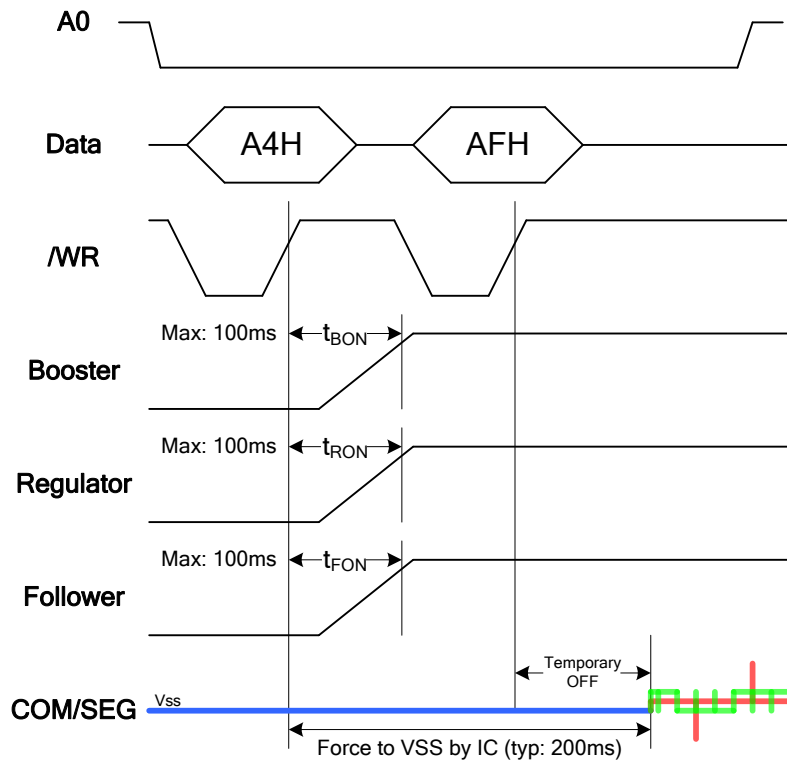
Exiting the Power Save Mode:



| Reference C Code    |                       |
|---------------------|-----------------------|
| WriteCommand(0xA4); | //Cancel All Pixel ON |
| WriteCommand(0xAF); | //Display ON          |

INTERNAL SEQUENCE of EXIT POWER SAVE MODE

After receiving power save instruction, the internal circuits (Power) will starts the following procedure.

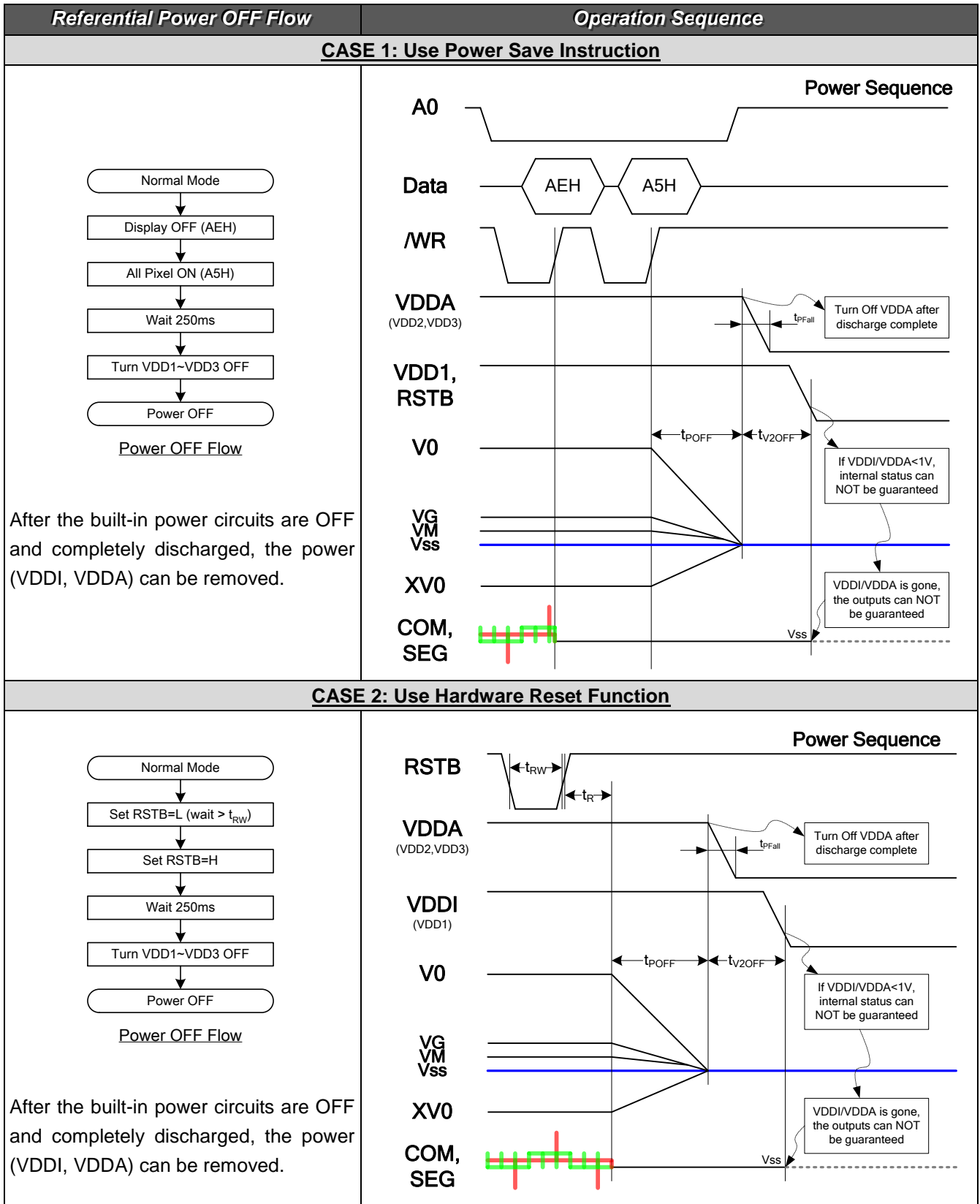


Note:

1. The power stable time is determined by LCD panel loading.
2. The power stable time in this figure is base on: LCD Panel Size = 1.4" without capacitor ( $\text{VDD}=2.7\text{V}$ ,  $\text{Vop}=9\text{V}$ ).

# 10-5 Power OFF Flow and Sequence

In power save mode, LCD outputs are fixed to VSS and all analog outputs are discharged. The power can be turned OFF after ST7567A is in the power save mode. The power save mode can be triggered by the following two methods.



**Note:**

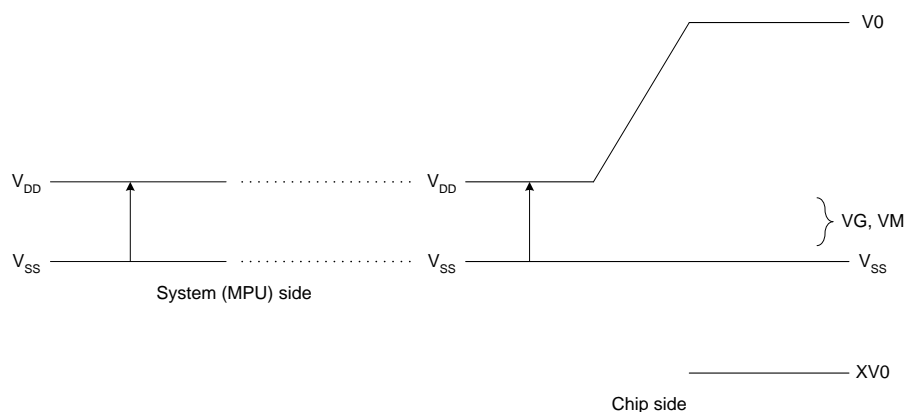
1.  $t_{POFF}$ : Internal Power discharge time.  $\Rightarrow$  250ms (max).
2.  $t_{V2OFF}$ : Period between VDDI and VDDA OFF time.  $\Rightarrow$  0 ms (min).
3. It is NOT recommended to turn VDDI OFF before VDDA. Without VDDI, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe flows into COM/SEG output(s) and the liquid crystal in panel maybe polarized.
4. IC will NOT be damaged if either VDDI or VDDA is OFF while another is ON.
5. The timing is dependent on panel loading and the external capacitor(s).
6. The timing in these figures is base on the condition that: LCD Panel Size = 1.4" without capacitor.
7. When turning VDDA OFF, the falling time should follow the specification:  $20\text{ms} \leq t_{Pfall} \leq 0.2\text{sec}$



# 11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System; please refer to notes 1 and 2.

| Parameter                    | Symbol     | Conditions      | Unit |
|------------------------------|------------|-----------------|------|
| Digital Power Supply Voltage | VDD1       | -0.3 ~ 4.0      | V    |
| Analog Power supply voltage  | VDD2, VDD3 | -0.3 ~ 4.0      | V    |
| Input Voltage                | VIN        | -0.3 ~ VDD1+0.3 | V    |
| Operating temperature        | TOPR       | -30 to +85      | °C   |
| Storage temperature          | TSTR       | -55 to +125     | °C   |
| LCD power supply voltage     | V0-XV0     | -0.3 ~ 18       | V    |



## Notes

- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
- That the stress exceeds the Limiting Value listed above it may cause the driver IC permanent damage. These values are for stress only. IC should be operated under the DC/Timing Characteristic conditions for normal operation. If these conditions are not met, IC operation may be error and the reliability may be deteriorated.
- Insure the voltage levels of V0, VDD2, VG, VM, VSS and XV0 always match the correct relation:  
 $V0 \geq VDD2 > VG > VM > VSS \geq XV0$
- VIN should be less than or equal to 3.6V. ( $VIN \leq 3.6V$ )

## 12 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

## 13 DC CHARACTERISTICS

VSS=0V; Temp=-30°C to +85°C; unless otherwise specified.

| Item                                | Symbol           | Condition                                    | Rating     |      |            | Unit | Applicable Pin |
|-------------------------------------|------------------|--|------------|------|------------|------|----------------|
|                                     |                  |  | Min.       | Typ. | Max.       |      |                |
| Operating Voltage (1)               | VDD1             |  | 1.7        | —    | 3.6        | V    | VDD1           |
| Operating Voltage (2)               | VDD2             |  | 2.0        | —    | 3.6        | V    | VDD2           |
| Operating Voltage (3)               | VDD3             |  | 2.0        | —    | 3.6        | V    | VDD3           |
| Input High-level Voltage            | V <sub>IHC</sub> |  | 0.7 x VDD1 | —    | VDD1       | V    | MPU Interface  |
| Input Low-level Voltage             | V <sub>ILC</sub> |  | VSS1       | —    | 0.3 x VDD1 | V    | MPU Interface  |
| Output High-level Voltage           | V <sub>OHC</sub> | I <sub>OUT</sub> =1mA, VDD1=1.8V             | 0.8 x VDD1 | —    | VDD1       | V    | D[7:0]         |
| Output Low-level Voltage            | V <sub>OLC</sub> | I <sub>OUT</sub> =-1mA, VDD1=1.8V            | VSS1       | —    | 0.2 x VDD1 | V    | D[7:0]         |
| Input Leakage Current               | I <sub>LI</sub>  |  | -1.0       | —    | 1.0        | μA   | MPU Interface  |
| Output Leakage Current              | I <sub>LO</sub>  |  | -3.0       | —    | 3.0        | μA   | MPU Interface  |
| Liquid Crystal Driver ON Resistance | R <sub>ON</sub>  | Ta=25°C                                      | —          | 0.6  | 0.8        | KΩ   | COMx           |
|                                     |                  | Vop=8.5V,<br>ΔV=0.85V<br>VG=1.9V<br>ΔV=0.19V |            | 1.3  | 1.5        | KΩ   | SEGx           |
| Frame Frequency                     | FR               | Duty=1/65, Vop=8.5V<br>Ta = 25°C             | 70         | 75   | 80         | Hz   |                |
| LCD Power Supply Voltage            | VLCD             | Ta = 25°C                                    | 4.0        | —    | 13.65      | V    | V0-XV0         |

Current consumption: During Display, with internal power system, current consumed by whole IC (bare die), Temp=-20°C to +70°C.

| Test Pattern                    | Symbol | Condition  | Rating |      |      | Unit | Note |
|---------------------------------|--------|--|--------|------|------|------|------|
|                                 |        |  | Min.   | Typ. | Max. |      |      |
| Display Pattern: Black (Static) | ISS    | VDD1=VDD2=VDD3=3.3V,<br>Booster X5<br>V <sub>OP</sub> = 8.5V, Bias = 1/9 | —      | 80   | 130  | μA   |      |
| Display OFF                     | ISS    | VDD1=VDD2=VDD3=3.3V,<br>Booster X5<br>V <sub>OP</sub> = 8.5V, Bias = 1/9 | —      | 70   | 110  | uA   |      |
| Power Down                      | ISS    | VDD1=VDD2=VDD3=3.3V  | —      | 1.0  | 3.0  | μA   |      |

Note:

*The Current Consumption is DC characteristics*

## Selection of Application Voltage

- Positive Booster:  $(VDD2 \times BL \times BE) \geq V0$  or  $(VDD2 \times BL \times BE) \geq Vop$ .
- Negative Booster:  $[-VDD2 \times (BL - 1) \times BE] \leq XV0$  or  $[VDD2 \times (BL - 1) \times BE] \geq (Vop - VG)$ , where  $VG = Vop \times 2 / N$ .
- If  $VG \geq VDD2 - 0.2V$ , please enable high power mode.
- $Vop$  requirement:  $[VDD2 \times (BL - 1) \times BE] \geq [Vop \times (N - 2) / N]$  or  $[Vop \leq VDD2 \times (BL - 1) \times BE \times N / (N - 2)]$ .
- $BL$  is the booster stage and  $BE$  is the booster efficiency. Actual  $BE$  should be determined by module loading and ITO resistance value.
- The worse condition should be considered. Furthermore, it should reserve some range for the temperature compensation and the contrast control (for end-customer).

For quickly reference, the following table lists the EV setting range for  $Vop$ .

$VDD1=2.8V$ ,  $VDD2=VDD3=2.8V$ , bare dice,  $Ta=25^{\circ}C$

| Bias | Booster | Vop                 |                    |
|------|---------|---------------------|--------------------|
|      |         | High Power Mode OFF | High Power Mode ON |
| 1/9  | X5      | 8.5 ~ 11.5          | 8.5 ~ 13.5         |
| 1/8  | X5      | 7.5 ~ 10.0          | 7.5 ~ 13.5         |
| 1/7  | X5      | 6.5 ~ 9.0           | 6.5 ~ 13.0         |
| 1/6  | X5      | 5.5 ~ 7.5           | 5.5 ~ 11.0         |
| 1/5  | X5      | 4.5 ~ 6.5           | 4.5 ~ 9.0          |
| 1/4  | X5      | 4.0 ~ 5.0           | 4.0 ~ 7.0          |

$VDD1=3.3V$ ,  $VDD2=VDD3=3.3V$ , bare dice,  $Ta=25^{\circ}C$

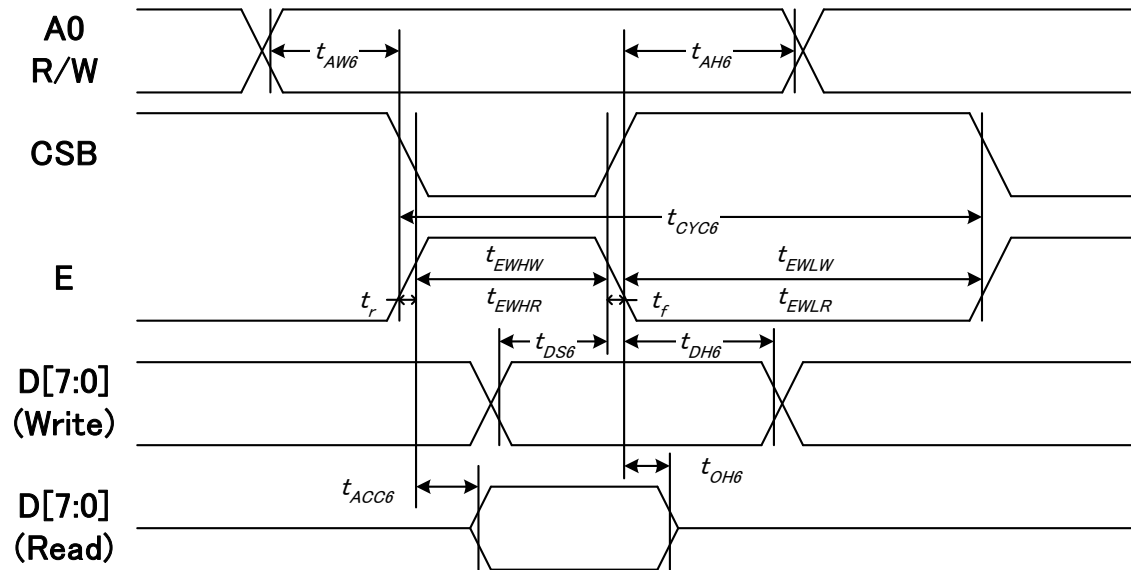
| Bias | Booster | Vop                 |                    |
|------|---------|---------------------|--------------------|
|      |         | High Power Mode OFF | High Power Mode ON |
| 1/9  | X5      | 8.5 ~ 13.5          | 8.5 ~ 13.5         |
| 1/8  | X5      | 7.5 ~ 12.0          | 7.5 ~ 13.5         |
| 1/7  | X5      | 6.5 ~ 10.5          | 6.5 ~ 13.0         |
| 1/6  | X5      | 5.5 ~ 9.0           | 5.5 ~ 11.0         |
| 1/5  | X5      | 4.5 ~ 7.5           | 4.5 ~ 9.0          |
| 1/4  | X5      | 4.0 ~ 6.0           | 4.0 ~ 7.0          |

Note:

1. In order to avoid ITO designed to affect the power efficiency, please refer to the ITO Layout Reference in section 15-1.
2. The power consumption of High Power Mode ON is higher than that of High Power Mode OFF.

# 14 TIMING CHARACTERISTICS

## 14-1 System Bus Timing for 6800 Series MPU



(VDD1 = 3.3V , Ta =25°C)

| Item                          | Signal | Symbol | Condition  | Min. | Max. | Unit |
|-------------------------------|--------|--------|------------|------|------|------|
| Address setup time            | A0     | tAW6   |            | 0    | —    | ns   |
| Address hold time             |        | tAH6   |            | 10   | —    |      |
| System cycle time             | E      | tCYC6  |            | 240  | —    |      |
| Enable L pulse width (WRITE)  |        | tEHLW  |            | 80   | —    |      |
| Enable H pulse width (WRITE)  |        | tEHWLW |            | 80   | —    |      |
| Enable L pulse width (READ)   |        | tEHLR  |            | 80   | —    |      |
| Enable H pulse width (READ)   |        | tEHWLR |            | 140  | —    |      |
| Write data setup time         | D[7:0] | tDS6   |            | 40   | —    |      |
| Write data hold time          |        | tDH6   |            | 10   | —    |      |
| Read data access time         |        | tACC6  | CL = 16 pF | —    | 70   |      |
| Read data output disable time |        | tOH6   | CL = 16 pF | 5    | 50   |      |

(VDD1 = 2.8V , Ta =25°C)

| Item                          | Signal | Symbol | Condition  | Min. | Max. | Unit |
|-------------------------------|--------|--------|------------|------|------|------|
| Address setup time            | A0     | tAW6   |            | 0    | —    | ns   |
| Address hold time             |        | tAH6   |            | 0    | —    |      |
| System cycle time             | E      | tCYC6  |            | 400  | —    |      |
| Enable L pulse width (WRITE)  |        | tEHLW  |            | 220  | —    |      |
| Enable H pulse width (WRITE)  |        | tEHWLW |            | 180  | —    |      |
| Enable L pulse width (READ)   |        | tEHLR  |            | 220  | —    |      |
| Enable H pulse width (READ)   |        | tEHWLR |            | 180  | —    |      |
| Write data setup time         | D[7:0] | tDS6   |            | 40   | —    |      |
| Write data hold time          |        | tDH6   |            | 20   | —    |      |
| Read data access time         |        | tACC6  | CL = 16 pF | —    | 140  |      |
| Read data output disable time |        | tOH6   | CL = 16 pF | 10   | 100  |      |

(VDD1 = 1.8V , Ta =25°C)

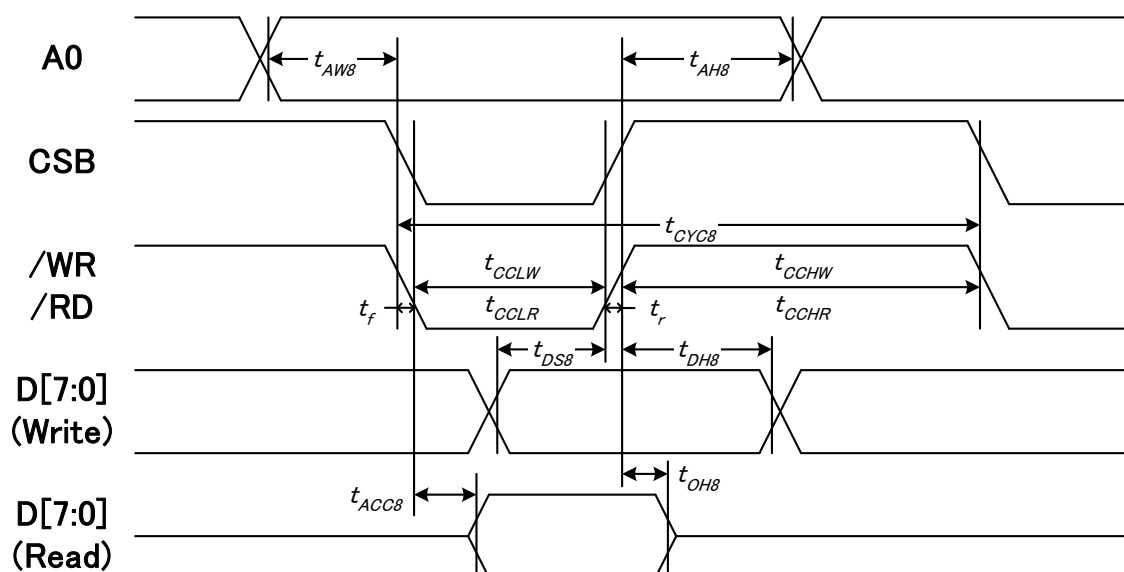
| Item                          | Signal | Symbol | Condition  | Min. | Max. | Unit |
|-------------------------------|--------|--------|------------|------|------|------|
| Address setup time            | A0     | tAW6   |            | 0    | —    | ns   |
| Address hold time             |        | tAH6   |            | 0    | —    |      |
| System cycle time             | E      | tCYC6  |            | 640  | —    |      |
| Enable L pulse width (WRITE)  |        | tEWLW  |            | 360  | —    |      |
| Enable H pulse width (WRITE)  |        | tEWHW  |            | 280  | —    |      |
| Enable L pulse width (READ)   |        | tEWLR  |            | 360  | —    |      |
| Enable H pulse width (READ)   |        | tEWHR  |            | 280  | —    |      |
| Write data setup time         | D[7:0] | tDS6   |            | 80   | —    |      |
| Write data hold time          |        | tDH6   |            | 20   | —    |      |
| Read data access time         |        | tACC6  | CL = 16 pF | —    | 240  |      |
| Read data output disable time |        | tOH6   | CL = 16 pF | 10   | 200  |      |

\*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast,  $(tr + tf) \leq (tCYC6 - tEWLW - tEWHW)$  for  $(tr + tf) \leq (tCYC6 - tEWLR - tEWHR)$  are specified.

\*2 All timing is specified using 20% and 80% of VDD1 as the reference.

\*3 tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.

# 14-2 System Bus Timing for 8080 Series MPU



(VDD1 = 3.3V , Ta =25°C)

| Item                      | Signal | Symbol | Condition  | Min. | Max. | Unit |
|---------------------------|--------|--------|------------|------|------|------|
| Address setup time        | A0     | tAW8   |            | 0    | —    | ns   |
| Address hold time         |        | tAH8   |            | 10   | —    |      |
| System cycle time         | /WR    | tCYC8  |            | 240  | —    |      |
| /WR L pulse width (WRITE) |        | tCCLW  |            | 80   | —    |      |
| /WR H pulse width (WRITE) | RD     | tCCHW  |            | 80   | —    |      |
| /RD L pulse width (READ)  |        | tCCLR  |            | 140  | —    |      |
| /RD H pulse width (READ)  |        | tCCHR  |            | 80   | —    |      |
| WRITE Data setup time     | D[7:0] | tDS8   |            | 40   | —    |      |
| WRITE Data hold time      |        | tDH8   |            | 20   | —    |      |
| READ access time          |        | tACC8  | CL = 16 pF | —    | 70   |      |
| READ Output disable time  |        | tOH8   | CL = 16 pF | 5    | 50   |      |

(VDD1 = 2.8V , Ta =25°C)

| Item                      | Signal | Symbol | Condition  | Min. | Max. | Unit |
|---------------------------|--------|--------|------------|------|------|------|
| Address setup time        | A0     | tAW8   |            | 0    | —    | ns   |
| Address hold time         |        | tAH8   |            | 0    | —    |      |
| System cycle time         | /WR    | tCYC8  |            | 400  | —    |      |
| /WR L pulse width (WRITE) |        | tCCLW  |            | 220  | —    |      |
| /WR H pulse width (WRITE) | RD     | tCCHW  |            | 180  | —    |      |
| /RD L pulse width (READ)  |        | tCCLR  |            | 220  | —    |      |
| /RD H pulse width (READ)  |        | tCCHR  |            | 180  | —    |      |
| WRITE Data setup time     | D[7:0] | tDS8   |            | 40   | —    |      |
| WRITE Data hold time      |        | tDH8   |            | 20   | —    |      |
| READ access time          |        | tACC8  | CL = 16 pF | —    | 140  |      |
| READ Output disable time  |        | tOH8   | CL = 16 pF | 10   | 100  |      |

(VDD1 = 1.8V , Ta =25°C)

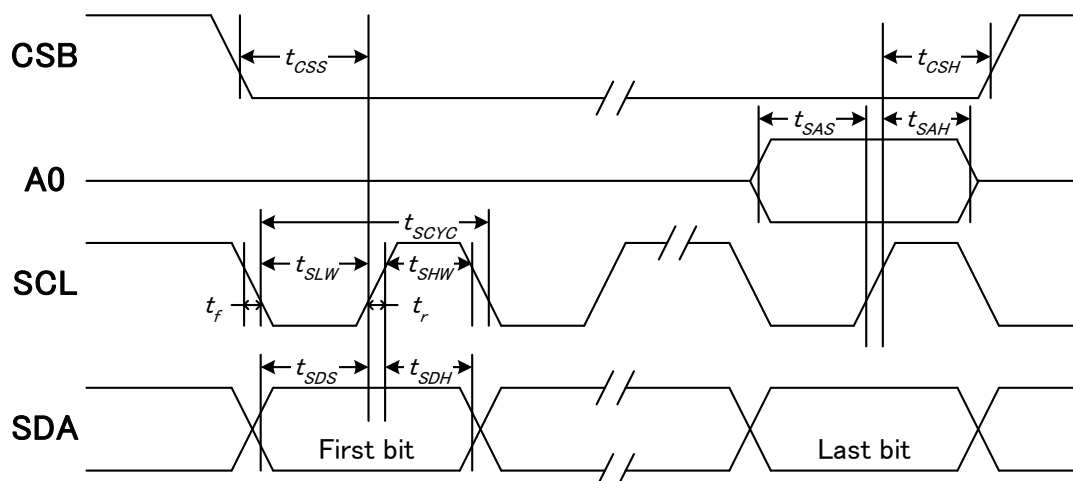
| Item                      | Signal | Symbol | Condition  | Min. | Max. | Unit |
|---------------------------|--------|--------|------------|------|------|------|
| Address setup time        | A0     | tAW8   |            | 0    | —    | ns   |
| Address hold time         |        | tAH8   |            | 0    | —    |      |
| System cycle time         | /WR    | tCYC8  |            | 640  | —    |      |
| /WR L pulse width (WRITE) |        | tCCLW  |            | 360  | —    |      |
| /WR H pulse width (WRITE) |        | tCCHW  |            | 280  | —    |      |
| /RD L pulse width (READ)  | RD     | tCCLR  |            | 360  | —    |      |
| /RD H pulse width (READ)  |        | tCCHR  |            | 280  |      |      |
| WRITE Data setup time     | D[7:0] | tDS8   |            | 80   | —    |      |
| WRITE Data hold time      |        | tDH8   |            | 20   | —    |      |
| READ access time          |        | tACC8  | CL = 16 pF | —    | 240  |      |
| READ Output disable time  |        | tOH8   | CL = 16 pF | 10   | 200  |      |

\*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast,  $(tr + tf) \leq (tCYC8 - tCCLW - tCCHW)$  for  $(tr + tf) \leq (tCYC8 - tCCLR - tCCHR)$  are specified.

\*2 All timing is specified using 20% and 80% of VDD1 as the reference.

\*3 tCCLW and tCCLR are specified as the overlap between CSB being “L” and WR and RD being at the “L” level.

### 14-3 System Bus Timing for 4-Line Serial Interface



(VDD1 = 3.3V , Ta =25°C)

| Item                | Signal | Symbol | Condition | Min. | Max. | Unit |
|---------------------|--------|--------|-----------|------|------|------|
| Serial clock period | SCL    | tSCYC  |           | 50   | —    | ns   |
| SCL "H" pulse width |        | tSHW   |           | 25   | —    |      |
| SCL "L" pulse width |        | tSLW   |           | 25   | —    |      |
| Address setup time  | A0     | tSAS   |           | 20   | —    |      |
| Address hold time   |        | tSAH   |           | 10   | —    |      |
| Data setup time     | SDA    | tSDS   |           | 20   | —    |      |
| Data hold time      |        | tSDH   |           | 10   | —    |      |
| CSB-SCL time        | CSB    | tCSS   |           | 20   | —    |      |
| CSB-SCL time        |        | tCSH   |           | 40   | —    |      |

(VDD1 = 2.8V , Ta =25°C)

| Item                | Signal | Symbol | Condition | Min. | Max. | Unit |
|---------------------|--------|--------|-----------|------|------|------|
| Serial clock period | SCL    | tSCYC  |           | 100  | —    | ns   |
| SCL "H" pulse width |        | tSHW   |           | 50   | —    |      |
| SCL "L" pulse width |        | tSLW   |           | 50   | —    |      |
| Address setup time  | A0     | tSAS   |           | 30   | —    |      |
| Address hold time   |        | tSAH   |           | 20   | —    |      |
| Data setup time     | SDA    | tSDS   |           | 30   | —    |      |
| Data hold time      |        | tSDH   |           | 20   | —    |      |
| CSB-SCL time        | CSB    | tCSS   |           | 30   | —    |      |
| CSB-SCL time        |        | tCSH   |           | 60   | —    |      |



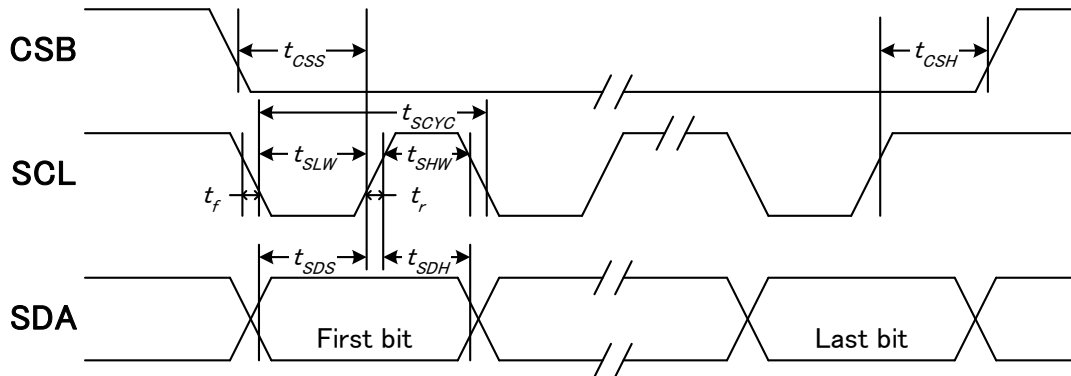
(VDD1 = 1.8V , Ta =25°C)

| Item                | Signal | Symbol | Condition | Min. | Max. | Unit |
|---------------------|--------|--------|-----------|------|------|------|
| Serial clock period | SCL    | tSCYC  |           | 200  | —    | ns   |
| SCL “H” pulse width |        | tSHW   |           | 80   | —    |      |
| SCL “L” pulse width |        | tSLW   |           | 80   | —    |      |
| Address setup time  | A0     | tSAS   |           | 60   | —    |      |
| Address hold time   |        | tSAH   |           | 30   | —    |      |
| Data setup time     | SDA    | tSDS   |           | 60   | —    |      |
| Data hold time      |        | tSDH   |           | 30   | —    |      |
| CSB-SCL time        | CSB    | tCSS   |           | 40   | —    |      |
| CSB-SCL time        |        | tCSH   |           | 100  | —    |      |

\*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

\*2 All timing is specified using 20% and 80% of VDD1 as the standard.

# 14-4 SERIAL INTERFACE (3Line-SPI Interface)



(VDD1 = 3.3V , Ta =25°C)

| Item                | Signal | Symbol | Condition | Min. | Max. | Unit |
|---------------------|--------|--------|-----------|------|------|------|
| Serial clock period | SCL    | tSCYC  |           | 50   | —    | ns   |
| SCL "H" pulse width |        | tSHW   |           | 25   | —    |      |
| SCL "L" pulse width |        | tSLW   |           | 25   | —    |      |
| Data setup time     | SDA    | tSDS   |           | 20   | —    |      |
| Data hold time      |        | tSDH   |           | 10   | —    |      |
| CSB-SCL time        | CSB    | tCSS   |           | 20   | —    |      |
| CSB-SCL time        |        | tCSH   |           | 40   | —    |      |

(VDD1=2.8V Ta=25°C)

| Item                   | Signal | Symbol | Condition | Min. | Max. | Unit |
|------------------------|--------|--------|-----------|------|------|------|
| Serial clock period    | SCL    | tSCYC  |           | 100  | —    | ns   |
| SCL "H" pulse width    |        | tSHW   |           | 50   | —    |      |
| SCL "L" pulse width    |        | tSLW   |           | 50   | —    |      |
| Data setup time        | SDA    | tSDS   |           | 30   | —    |      |
| Data hold time         |        | tSDH   |           | 20   | —    |      |
| Chip select setup time | CSB    | tCSS   |           | 30   | —    |      |
| Chip select hold time  |        | tCSH   |           | 60   | —    |      |

(VDD1 = 1.8V , Ta =25°C)

| Item                | Signal | Symbol | Condition | Min. | Max. | Unit |
|---------------------|--------|--------|-----------|------|------|------|
| Serial clock period | SCL    | tSCYC  |           | 200  | —    | ns   |
| SCL "H" pulse width |        | tSHW   |           | 80   | —    |      |
| SCL "L" pulse width |        | tSLW   |           | 80   | —    |      |
| Data setup time     | SDA    | tSDS   |           | 60   | —    |      |
| Data hold time      |        | tSDH   |           | 30   | —    |      |
| CSB-SCL time        | CSB    | tCSS   |           | 40   | —    |      |
| CSB-SCL time        |        | tCSH   |           | 100  | —    |      |

\*1 The rise and fall time (tr, tf) of the input signal are specified at 15 ns or less.

\*2 All timings take 20% and 80% of VDD1 as standard.

The diagram illustrates the timing relationships for an I2C bus. It shows three signals: SDA (Serial Data), SCL (Serial Clock), and SDA (Serial Data) again. The timing parameters are defined as follows:

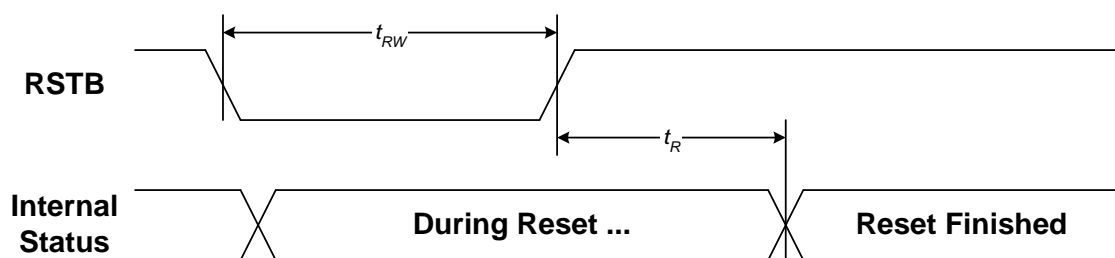
- $t_{BUF}$ : Buffer time, the time between the start of a data transfer and the start of the clock signal.
- $t_{HD,STA}$ : Hold time, the time between the start of a data transfer and the start of the clock signal.
- $t_{LOW}$ : Low time, the time the SCL signal is held low.
- $t_{HIGH}$ : High time, the time the SCL signal is held high.
- $t_f$ : Fall time, the time the SCL signal takes to fall from high to low.
- $t_r$ : Rise time, the time the SCL signal takes to rise from low to high.
- $t_{HD,DAT}$ : Hold time, the time between the end of a data transfer and the end of the clock signal.
- $t_{SU,DAT}$ : Setup time, the time between the end of a data transfer and the end of the clock signal.
- $t_{SU,STA}$ : Setup time, the time between the start of a data transfer and the start of the clock signal.
- $t_{SU,STO}$ : Setup time, the time between the end of a data transfer and the end of the clock signal.

| Item                                      | Signal | Symbol   | Condition | Min. | Max. | Unit |
|---|--------|----------|-----------|------|------|------|
| SCL clock frequency                       | SCL    | fSCL     |           | -    | 400  | kHz  |
| SCL clock low period                      |        | tLOW     |           | 160  | -    |      |
| SCL clock high period                     |        | tHIGH    |           | 60   | -    |      |
| Data set-up time                          | SDA    | tSU;Data |           | 80   | -    |      |
| Data hold time                            |        | tHD;Data |           | 40   | -    |      |
| Setup time for a repeated START condition | SDA    | tSU;STA  |           | 90   | -    |      |
| Start condition hold time                 |        | tHD;STA  |           | 220  | -    |      |
| Setup time for STOP condition             |        | tSU;STO  |           | 110  | -    |      |
| Bus free time between a STOP and START    |        | tBUF     |           | 150  | -    |      |

| Item                                      | Signal | Symbol   | Condition | Min. | Max. | Unit |
|---|--------|----------|-----------|------|------|------|
| SCL clock frequency                       | SCL    | fSCL     |           | -    | 400  | ns   |
| SCL clock low period                      |        | tLOW     |           | 160  | -    |      |
| SCL clock high period                     |        | tHIGH    |           | 60   | -    |      |
| Data set-up time                          | SDA    | tSU;Data |           | 80   | -    |      |
| Data hold time                            |        | tHD;Data |           | 40   | -    |      |
| Setup time for a repeated START condition | SDA    | tSU;STA  |           | 90   | -    |      |
| Start condition hold time                 |        | tHD;STA  |           | 220  | -    |      |
| Setup time for STOP condition             |        | tSU;STO  |           | 110  | -    |      |
| Bus free time between a STOP and START    |        | tBUF     |           | 150  | -    |      |

\*2 All timings take 20% and 80% of VDD1 as standard.

## 14-6 Hardware Reset Timing



(VDD1 = 3.3V , Ta =25°C)

| Item                  | Symbol | Condition | Min. | Max. | Unit |
|-----------------------|--------|-----------|------|------|------|
| Reset time            | tR     |           | —    | 1.0  | us   |
| Reset “L” pulse width | tRW    |           | 1.0  | —    |      |

(VDD1 = 2.8V , Ta =25°C)

| Item                  | Symbol | Condition | Min. | Max. | Unit |
|-----------------------|--------|-----------|------|------|------|
| Reset time            | tR     |           | —    | 2.0  | us   |
| Reset “L” pulse width | tRW    |           | 2.0  | —    |      |

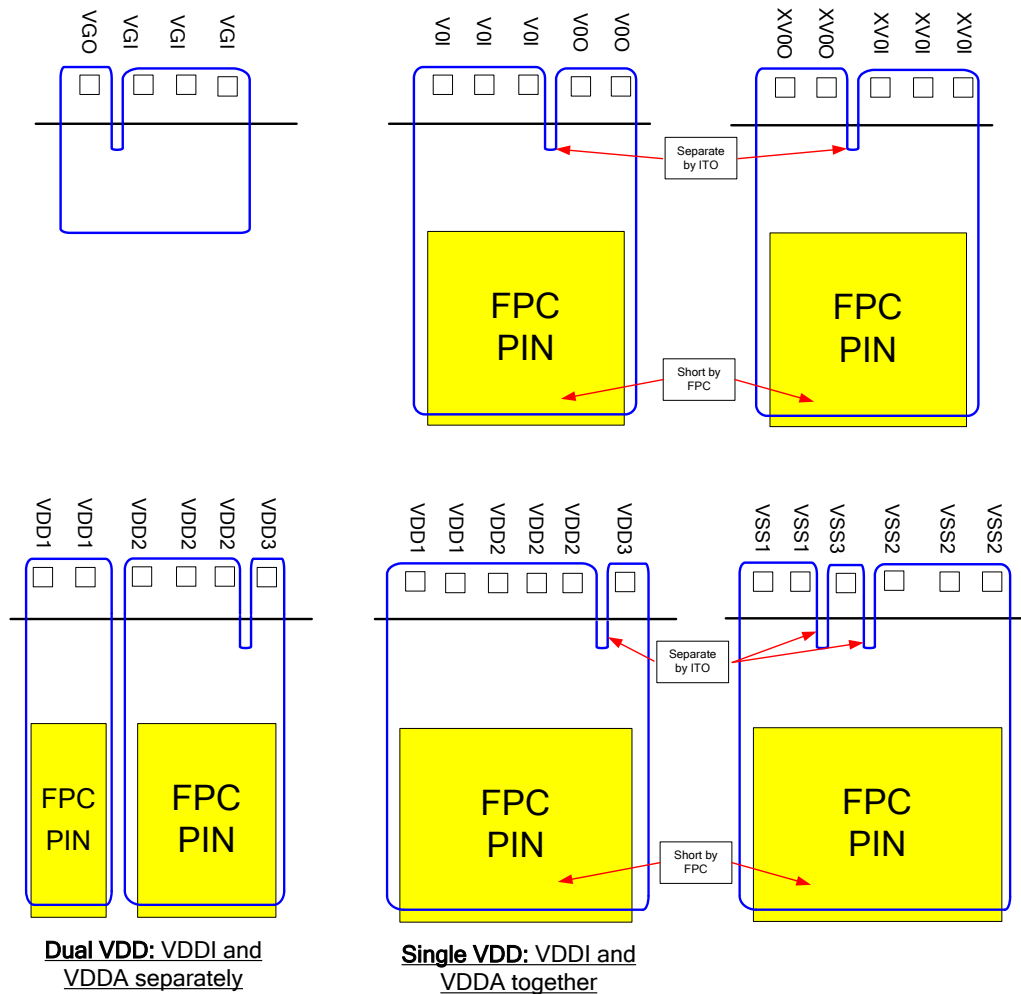
(VDD1 = 1.8V , Ta =25°C)

| Item                  | Symbol | Condition | Min. | Max. | Unit |
|-----------------------|--------|-----------|------|------|------|
| Reset time            | tR     |           | —    | 3.0  | us   |
| Reset “L” pulse width | tRW    |           | 3.0  | —    |      |

# 15 APPLICATION NOTE

## 15-1 ITO Layout Reference

The reference ITO layout is shown below:



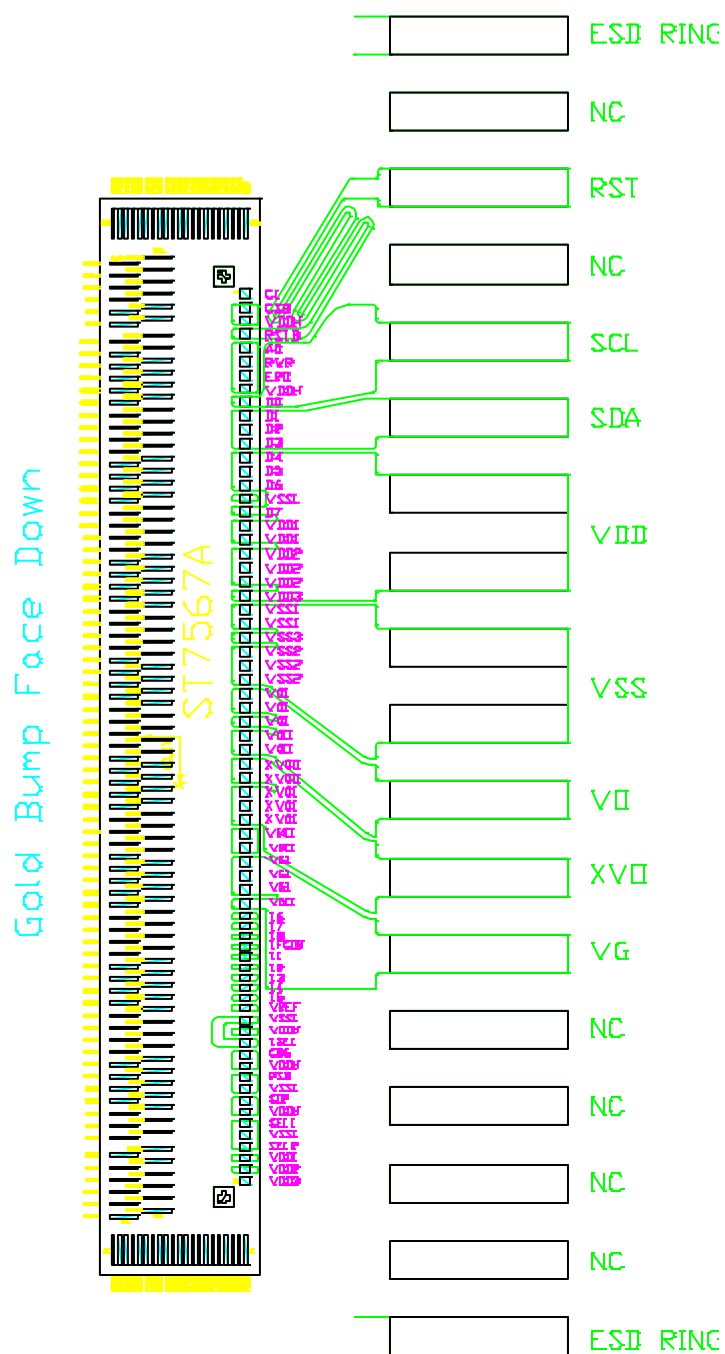
The equivalent circuit is shown below:

| $V_0, XV_0$ & $V_G$  | $V_{SS}$   | Dual VDD<br>(VDDI & VDDA separately)   | Single VDD<br>(VDDI & VDDA together)   |
|--|--|--|--|
|  |  |  |  |
| <p><b>Ideal Layout:</b></p> <p>=&gt; <math>R_3=0</math> Ohm. <math>R_1 \geq R_2</math>.</p> <p><b>Acceptable Layout:</b></p> <p>=&gt; <math>R_3 \neq 0</math>. <math>R_1 &gt; R_2 &gt; R_3</math>.</p> <p><b>Not Acceptable:</b></p> <p>=&gt; <math>R_3 \geq (R_1 \text{ or } R_2)</math>.</p> <p><math>XV_0</math> and <math>V_G</math> are the same as <math>V_0</math>.</p> | <p><b>Ideal Layout:</b></p> <p>=&gt; <math>R_4=0</math> Ohm. <math>R_2 &gt; R_1 &gt; R_3</math>.</p> <p><b>Acceptable Layout:</b></p> <p>=&gt; <math>R_4 \neq 0</math>. <math>R_2 &gt; R_1 &gt; R_3 &gt; R_4</math>.</p> <p><b>Not Acceptable:</b></p> <p>=&gt; <math>R_4 \geq (R_1 \text{ or } R_2)</math>.</p> | <p><b>Ideal Layout:</b></p> <p>=&gt; <math>R_4=0</math> &amp; <math>R_5=0</math> Ohm.</p> <p>=&gt; <math>R_3 \geq R_1 &gt; R_2</math>.</p> <p><b>Acceptable Layout:</b></p> <p>=&gt; <math>R_4 \neq 0</math> &amp; <math>R_5 \neq 0</math>.</p> <p>=&gt; <math>R_3 \geq R_1 &gt; R_2 &gt; R_5 &gt; R_4</math></p> <p><b>Not Acceptable:</b></p> <p>=&gt; <math>R_4</math> &amp; <math>R_5 \geq (R_1 \text{ or } R_2 \text{ or } R_3)</math>.</p> | <p><b>Ideal Layout:</b></p> <p>=&gt; <math>R_3=0</math> Ohm. <math>R_2 \geq R_1</math>.</p> <p><b>Acceptable Layout:</b></p> <p>=&gt; <math>R_3 \neq 0</math>. <math>R_2 \geq R_1 &gt; R_3</math>.</p> <p><b>Not Acceptable:</b></p> <p>=&gt; <math>R_3 \geq (R_1 \text{ or } R_2)</math>.</p> |

## Ver 1.2a



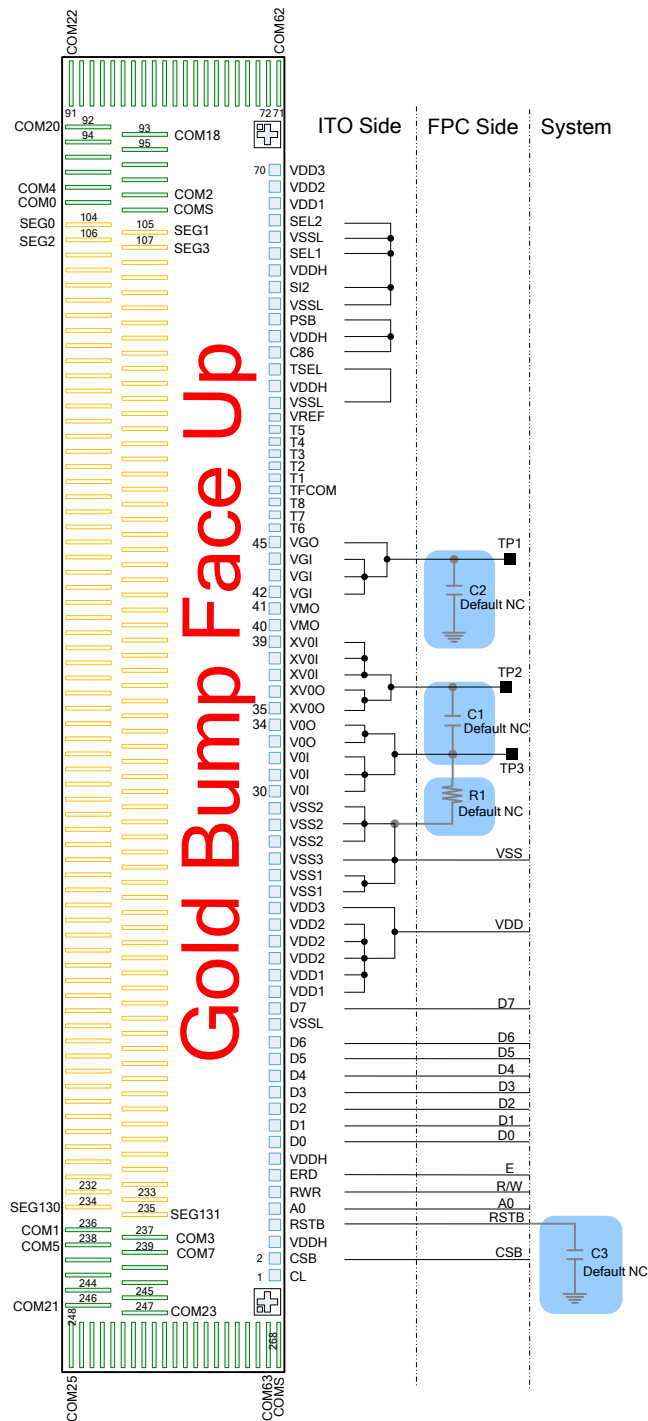
15-3 Layout Design Reference (65 Duty, I2C)



## 15-4 Application Circuit

If the panel size is larger than 2" or use the icon, must be added the capacitor C1 and C2, please refer to Section 7-8 External Components of Power Circuit.

### ● 6800 Interface



Interface: 6800

High Power Mode OFF

Duty: 1/65

Bias: 1/9

TSEL = L

C1: 0.1uF~1uF/ 25V

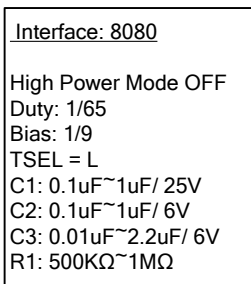
C2: 0.1uF~1uF/ 6V

C3: 0.01uF~2.2uF/ 6V

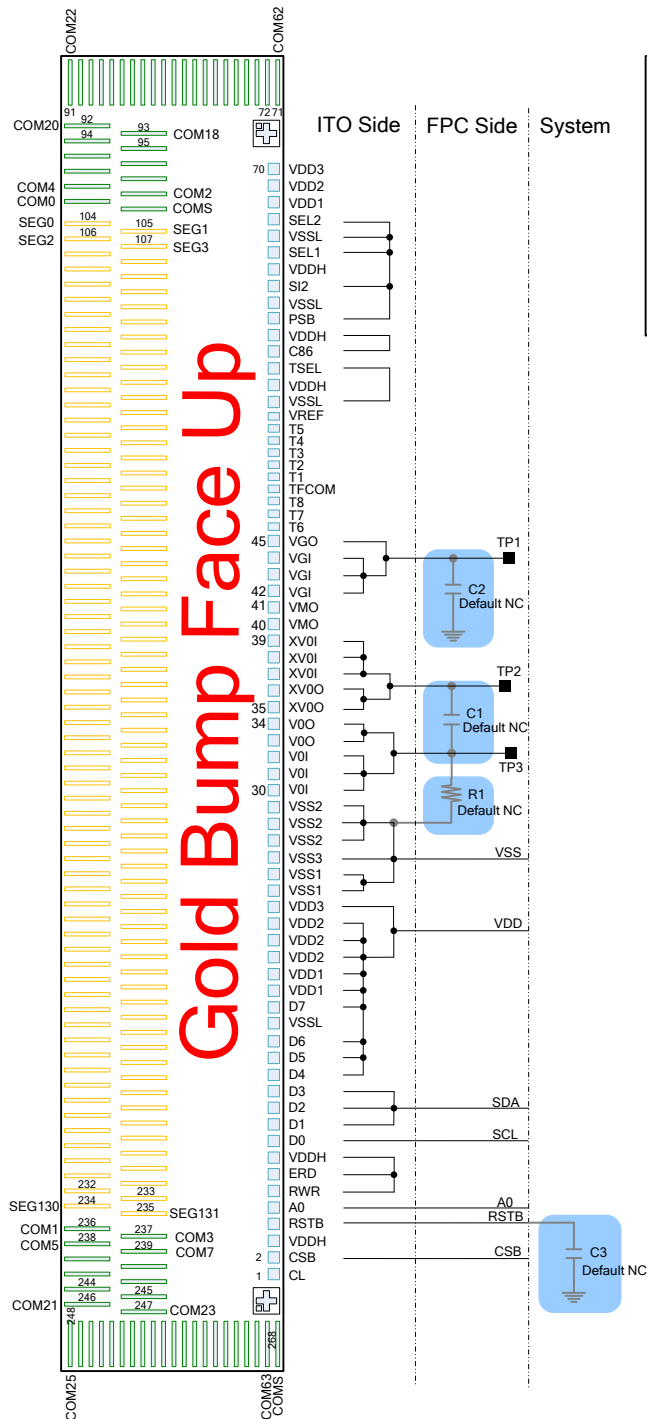
R1: 500KΩ~1MΩ



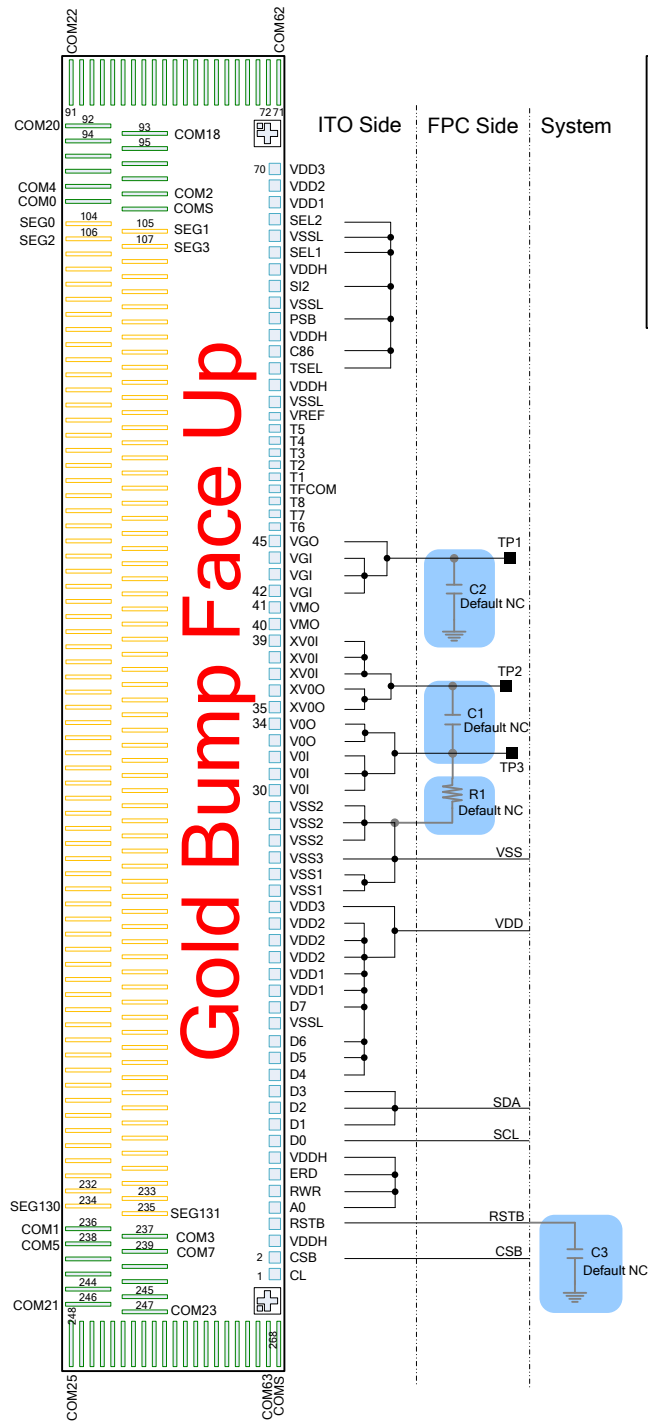
- **8080 Interface**



● 4Line-SPI Interface

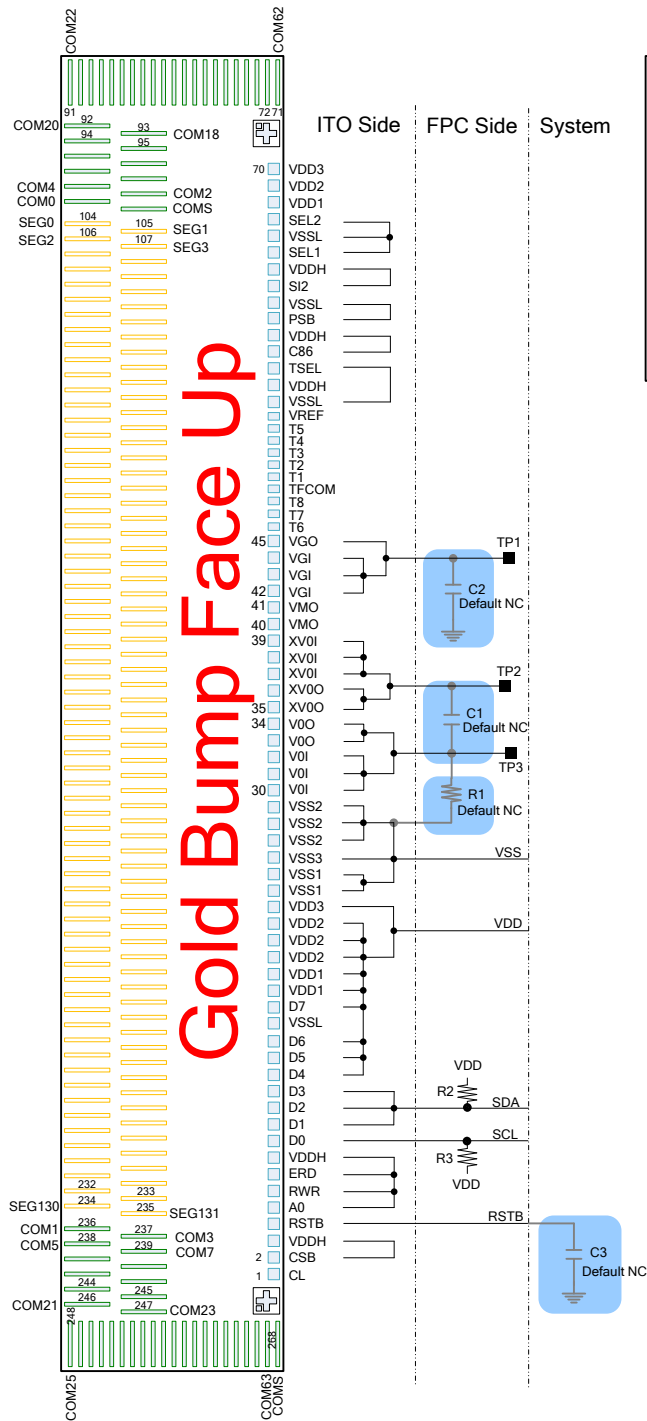


● 3Line-SPI Interface



Interface: 3SPI  
 High Power Mode OFF  
 Duty: 1/65  
 Bias: 1/9  
 TSEL = L  
 C1: 0.1uF~1uF/ 25V  
 C2: 0.1uF~1uF/ 6V  
 C3: 0.01uF~2.2uF/ 6V  
 R1: 500KΩ~1MΩ

● I2C-Interface



Interface: I2C

High Power Mode OFF

Duty: 1/65

Bias: 1/9

TSEL = L

C1: 0.1uF~1uF/ 25V

C2: 0.1uF~1uF/ 6V

C3: 0.01uF~2.2uF/ 6V

R1: 500KΩ~1MΩ

R2: 3KΩ~5KΩ

R3: 3KΩ~5KΩ

## 16 REVERSION HISTORY

| Version | Date       | Description   |
|---------|------------|---|
| 1.0     | 2015/08/21 | Remove Preliminary.   |
| 1.1     | 2015/09/15 | 1. Add Extension Command Table<br>2. Modify Bump Height<br>3. Add Vop reference Table   |
| 1.1a    | 2015/12/09 | Add Description of 17 Duty and 9 Duty   |
| 1.2     | 2016/07/13 | Modify Column Address Instructions  |
| 1.2a    | 2016/12/06 | 1. Modify Minimum Voltage of VDDA<br>2. Modify Temperature Range of Current Consumption |