ELC 2137 Lab #4: Subtractor

Sebastian Lopez and Megan Gordon

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Summary

In this lab we described the operation of a two-bit adder/subtractor. We developed a moderately complex circuit on a breadboard using standard electrical parts, as well as our own test procedure and verification operation of the circuit. Then, we recognized that the digital circuits quickly become complex and difficult to implement in hardware.

Q&A

1. Why did we use two full adders instead of a half adder and a full adder?
2. How many input combinations would it take to exhaustively test the adder/subtractor? It would take six input combinations to exhaustively test the adder/subtractor.
3. Why were the combinations given in the truth table chosen? The reason why these specific combinations were given is due to the fact that it gives the proper values to effectively run and test the adder/subtractor.
4. Do the results from your adder/subtractor match what you would expect from theory? Explain any discrepancies.

Results

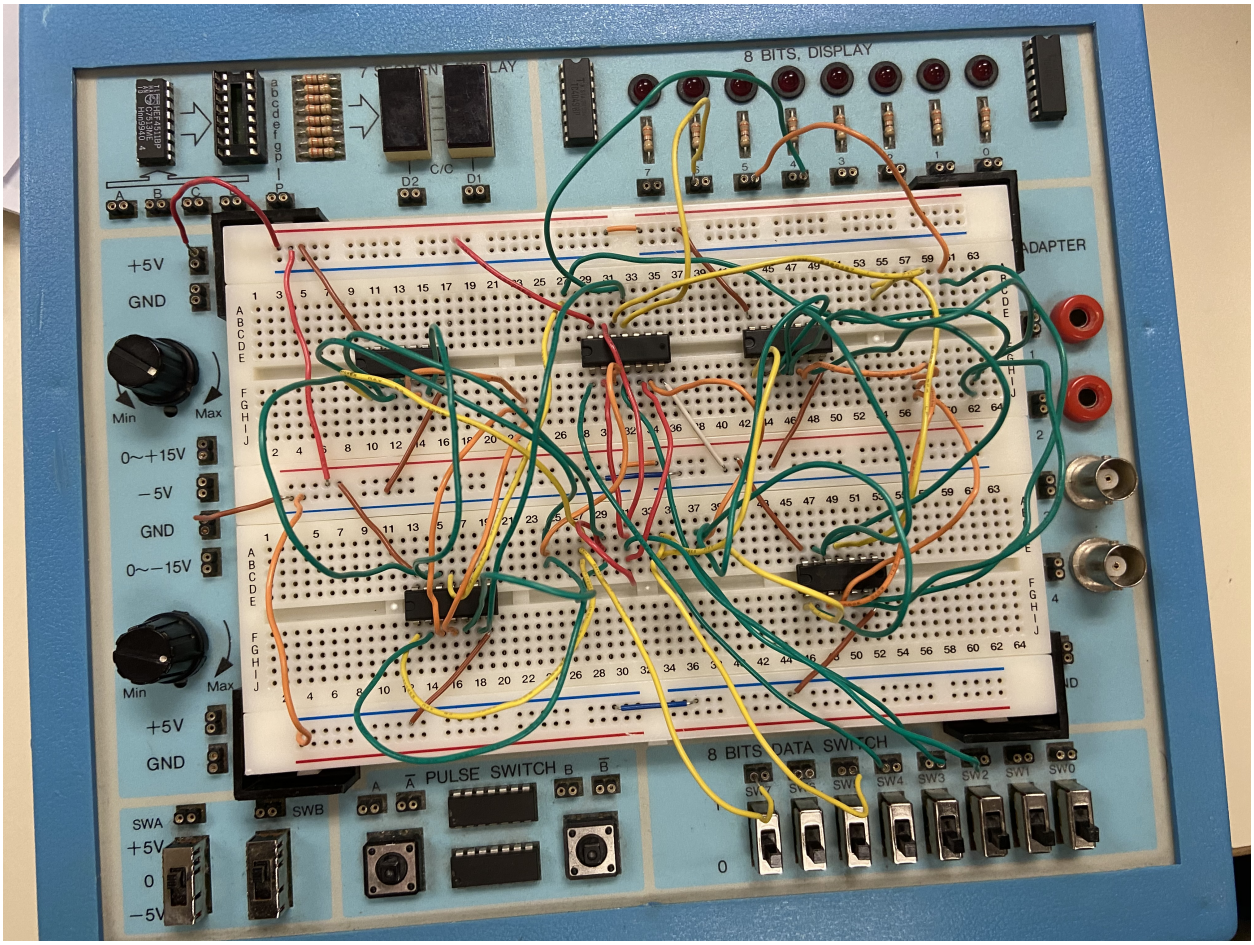


Figure 1: This is the assembled circuit.

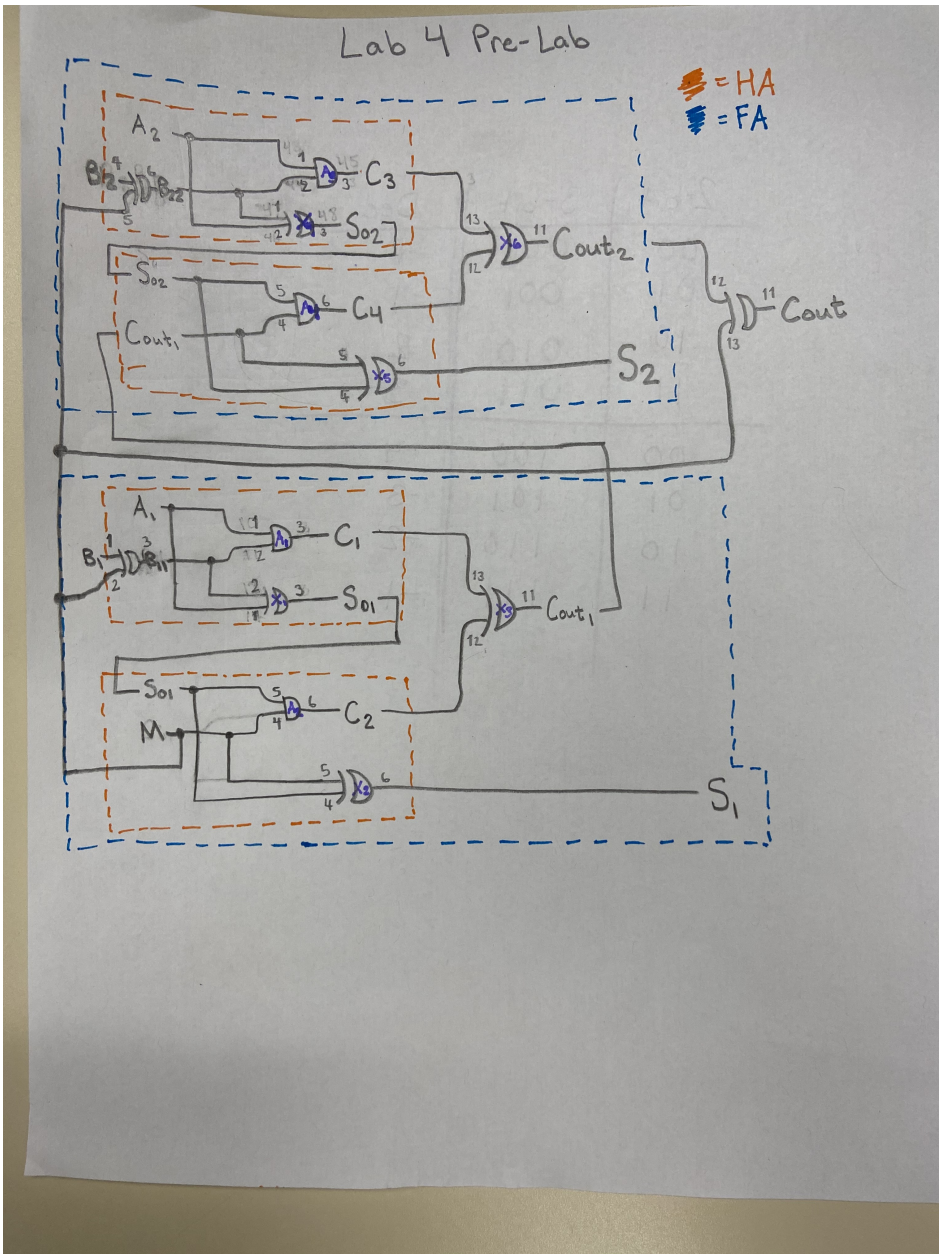
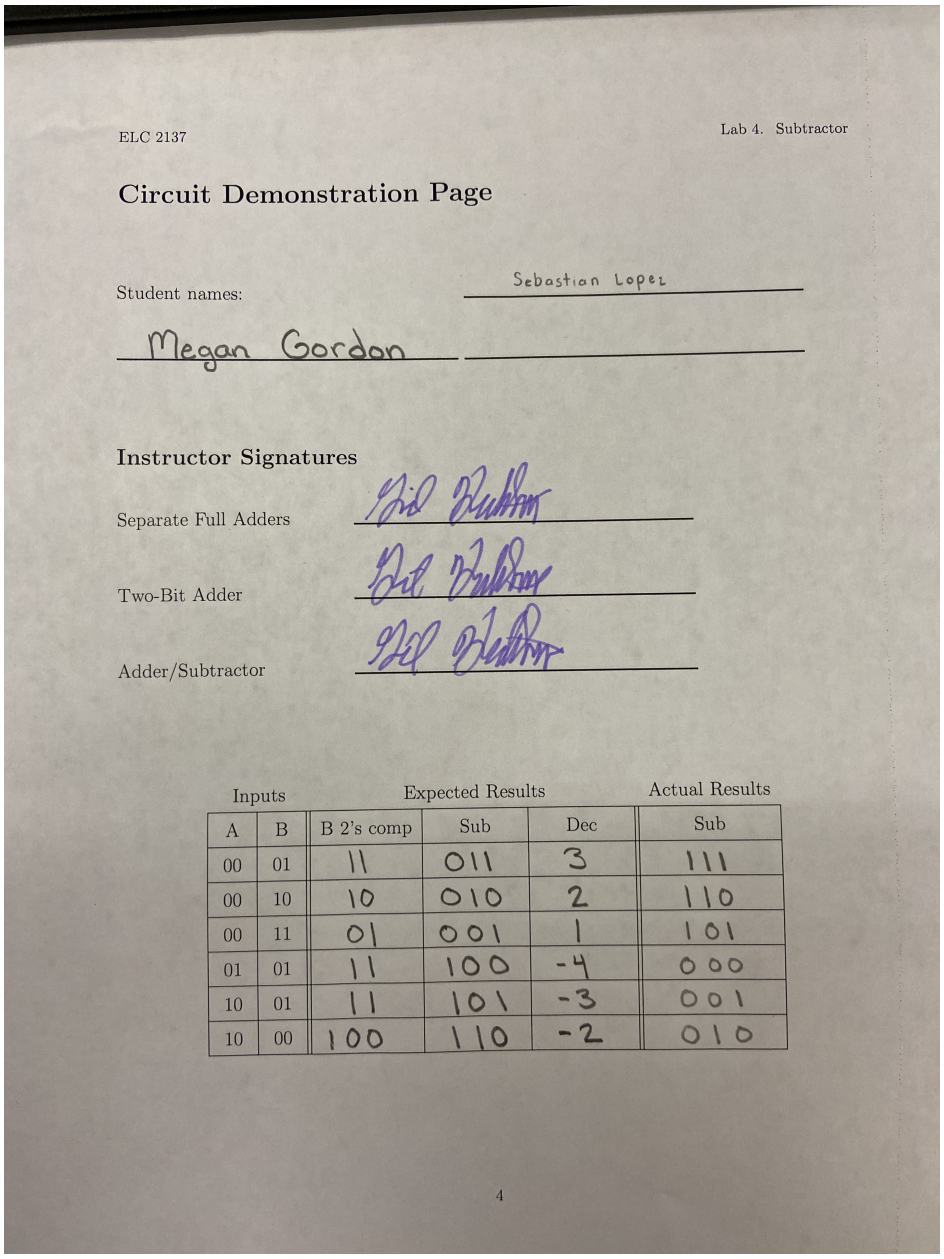


Figure 2: This is the two bit adder/subtractor schematic.



ELC 2137 Lab 4. Subtractor

Circuit Demonstration Page

Student names: Sebastian Lopez

Megan Gordon

Instructor Signatures

Separate Full Adders

Two-Bit Adder

Adder/Subtractor

Inputs		Expected Results			Actual Results
A	B	B 2's comp	Sub	Dec	Sub
00	01	11	011	3	111
00	10	10	010	2	110
00	11	01	001	1	101
01	01	11	100	-4	000
10	01	11	101	-3	001
10	00	100	110	-2	010

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Figure 3: This is the circuit demonstration page.