LTC3786 Supply Design Summary Report

Vin: 10V (min.), 12V (nom.), 14V (max.)

Output Rails : Vout1 = 34,91V / 12A (max.)

Project Name: Demo Board DC1641A

Project Date: 9/2014

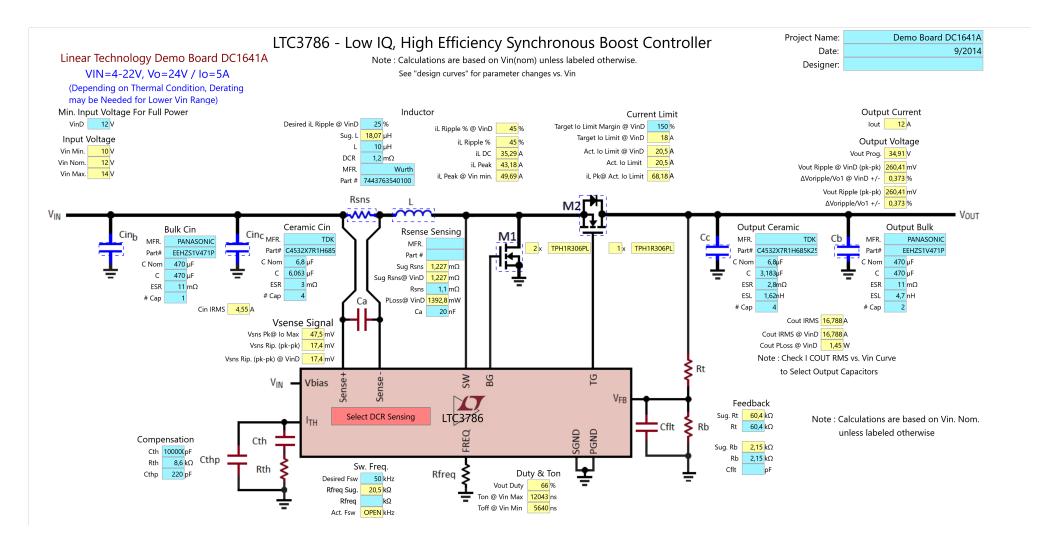
Designer:





LTC3786 Solution - Simplified Schematic

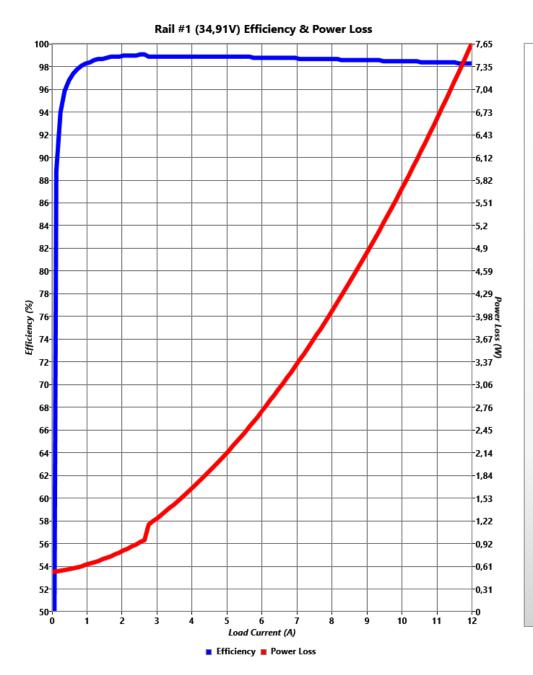
Vin: 10V (min.), 12V (nom.), 14V (max.) Output Rails: Vout1 = 34,91V / 12A (max.)



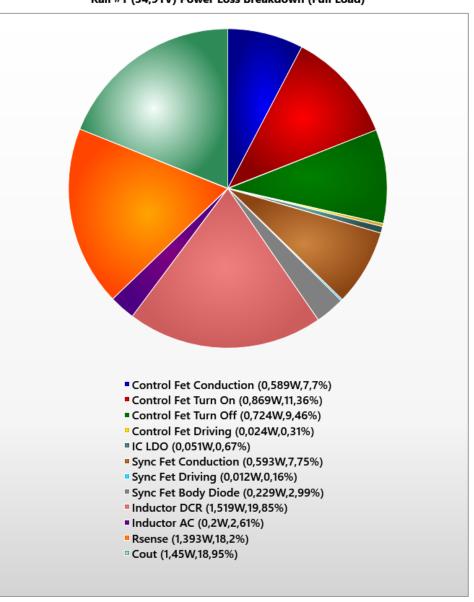
LTC3786 Solution - Efficiency & Loss Estimations

Rail # 1 : Vin = 12V, Vout1 = 34,91V

* Estimations For CCM Mode Only. Inductor AC Losses Entered by User



Rail #1 (34,91V) Power Loss Breakdown (Full Load)



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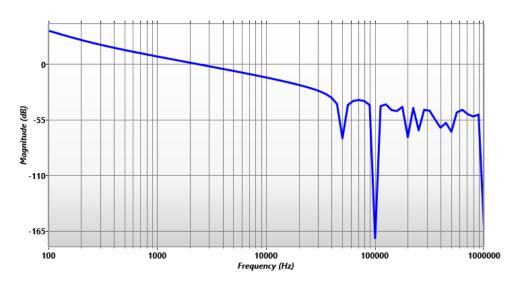
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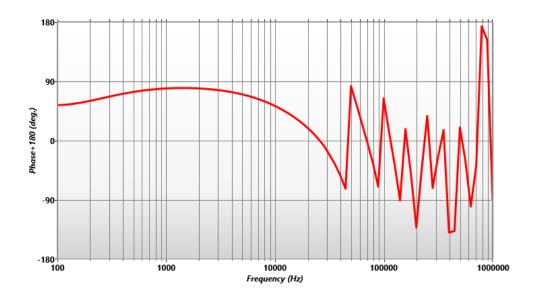
LTC3786 Solution - Loop Gain & Load Transient Estimations

Rail # 1 : Vin = 12V, Vout1 = 34,91V, Iout1 = 1A

* Estimations For CCM Mode Only. Estimations Based On Small Signal Avg. Model

Rail #1 (34,91V) Loop Gain



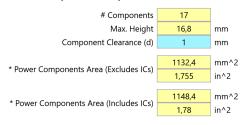


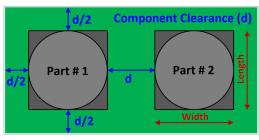
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LTC3786 Solution - Summary

LTC3786 Supply Design Summary **Project Info:** Demo Board DC1641A, 9/2014 **Design Specifications** Steady State: Rail # Vin Min. Vin Max. ΔVο ΔVo% lo Max iLpk Toff min. Vin Nom. Fsw Vo ∆iLp-p ΔiL% **Duty Max** Ton min. 10 V 12 V 14 V 50 kHz 34,91 V 260,41 mV 0,4 % 12 A 45 % 43,18 A 15,77 A 71,8 % 12043 ns 5640 ns **Efficiency and Loop:** Rail # Vo Eff.@lomax PLoss@lomax Loop BW Loop PM Iomax 12 A 98.21 % 77,74 deg 34,91 V 7,653 W 2,24 kHz **Recommendations and Warnings:** Message **Power Components Power Components Bill Of Materials:** Export BOM Mfr. Name Mfr. Part # Ref. Des. Value Quantity Description Pkg. (Imperial) L(mm) W(mm) H(mm) User Note U1 LINEAR TECH LTC3786 0,8 IND Wurth 7443763540100 19,81 19,56 7,4 Lo1 10μΗ 16,8 470µF CAP **PANASONIC** EEHZS1V471P 10 10 Cinb1 C4532X7R1H685K250KB 2,8 Cinc1 Cinc2 Cinc3 Cinc4 6,8µF CAP TDK 4,5 3,2 16,8 CAP **PANASONIC** EEHZS1V471P 10 Cob1 Cob2 470µF 10 CAP TDK C4532X7R1H685K250KB 3,2 2.8 Coc1 Coc2 Coc3 Coc4 6,8µF 4.5 2,5 0,74 RES Rsense1 $1,1m\Omega$ Mctrl1 Mctrl2 60V FET TOSHIBA TPH1R306PL 5,2 6,3 TPH1R306PL 60V FET TOSHIBA 5.2 6,3 Msync1

Power Components Footprint:





* Notes:

- 1. The calculated power component area is only the simple sum of component footprint areas with given clearance, assuming all power components are on the same side of PCB. It is NOT the final PCB size with layout design.
- 2. Component count should change with the number of paralleled phases.

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