FPGA Based Flight Controller

Project Guide:
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College

Team members:

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Medha Lakshman Rao	36
Omar Bin Shafi	45
Sebastian James	55

CONTENTS

Detailed Analysis and Modelling

Objectives

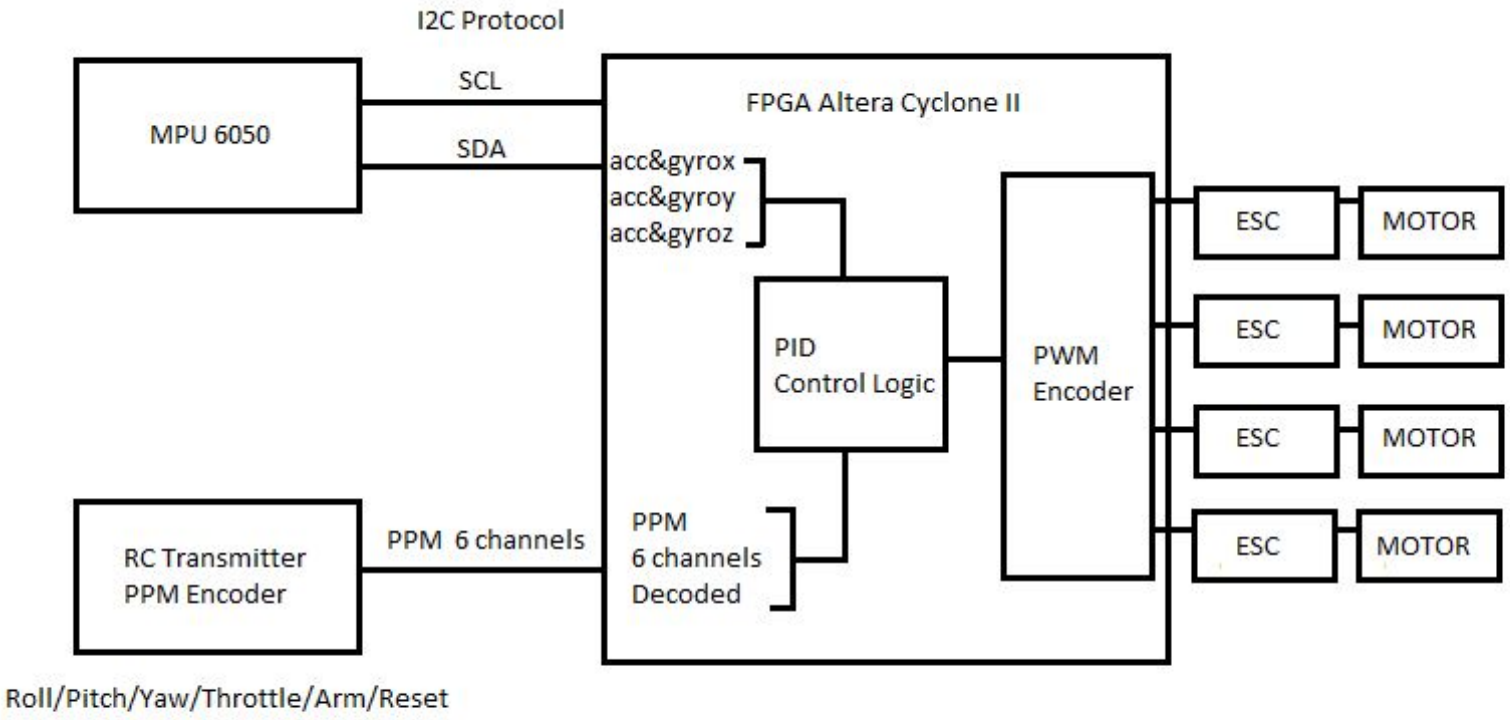
- To design a flight controller (FC) system on an FPGA board using System Verilog to program the FPGA.
- To deploy the code in Altera Cyclone II FPGA development board to tune the flight parameters to achieve stable flight using a radio transmitter/similar manual input.
- Testing and interfacing MPU-6050 (I2C) with FPGA board.
- Implementing PID loop and PWM encoder in the FPGA.
- Direct the input of ESC to control RPM of each motor in response to input into PID from MPU and RC transmitter

Detailed Analysis and Modelling

Novelty

- Implementations in Finite State Machine (FSM) approach.
- Convert to a minimum viable product (MVP).
- Integration of more sensors like barometer, ultrasonic to improve stability.

Detailed Analysis and Modelling - Overview



Detailed Analysis and Modelling

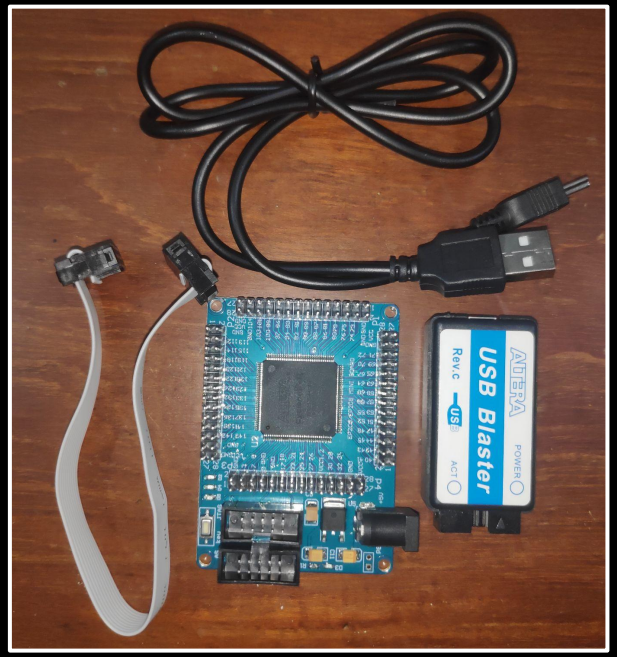
Work done – Previous presentation

- Familiarised with Vivado ISE and Quartus II, implemented gates, adders, clocks.
- Learned basics of PID, learned PPM decoding.
- Completed PPM decoding in Verilog, hardware implementation in progress.
- Learned basics of PWM and implemented PWM encoding.
- Learned filter design, started to implement filter.
- Implemented I2C protocol.
- Learned the basics of FPGA from Coursera; familiarized with Quartus Prime.
- Read the reference papers and various standard texts.

Detailed Analysis and Modelling

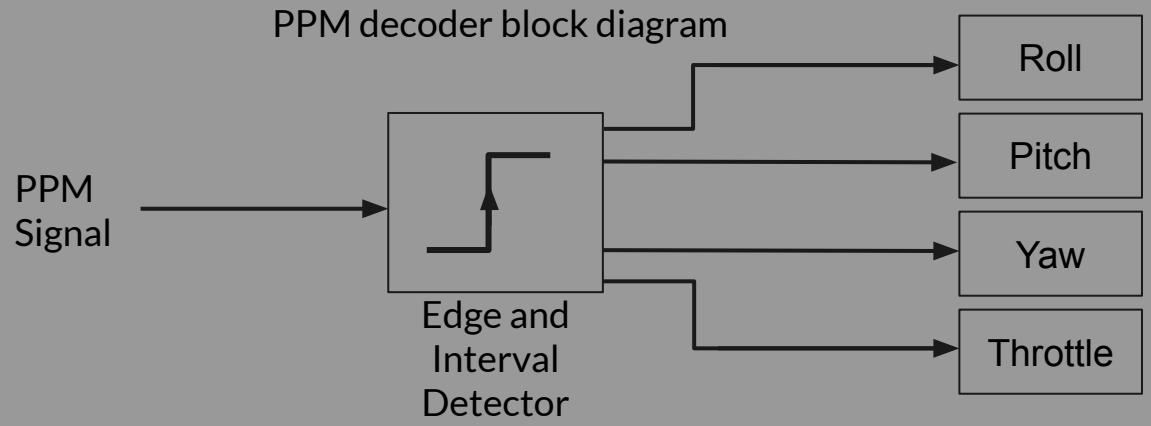
Plan of implementation and demonstration

- Purchased FPGA - Altera Cyclone II
- Shifted to Altera Quartus II
- Familiarization of FPGA
- PPM decoding and testing
- I2C master interfacing with MPU-6050
- MPU-6050 driver testing
- PID implementation
- PWM encoder testing

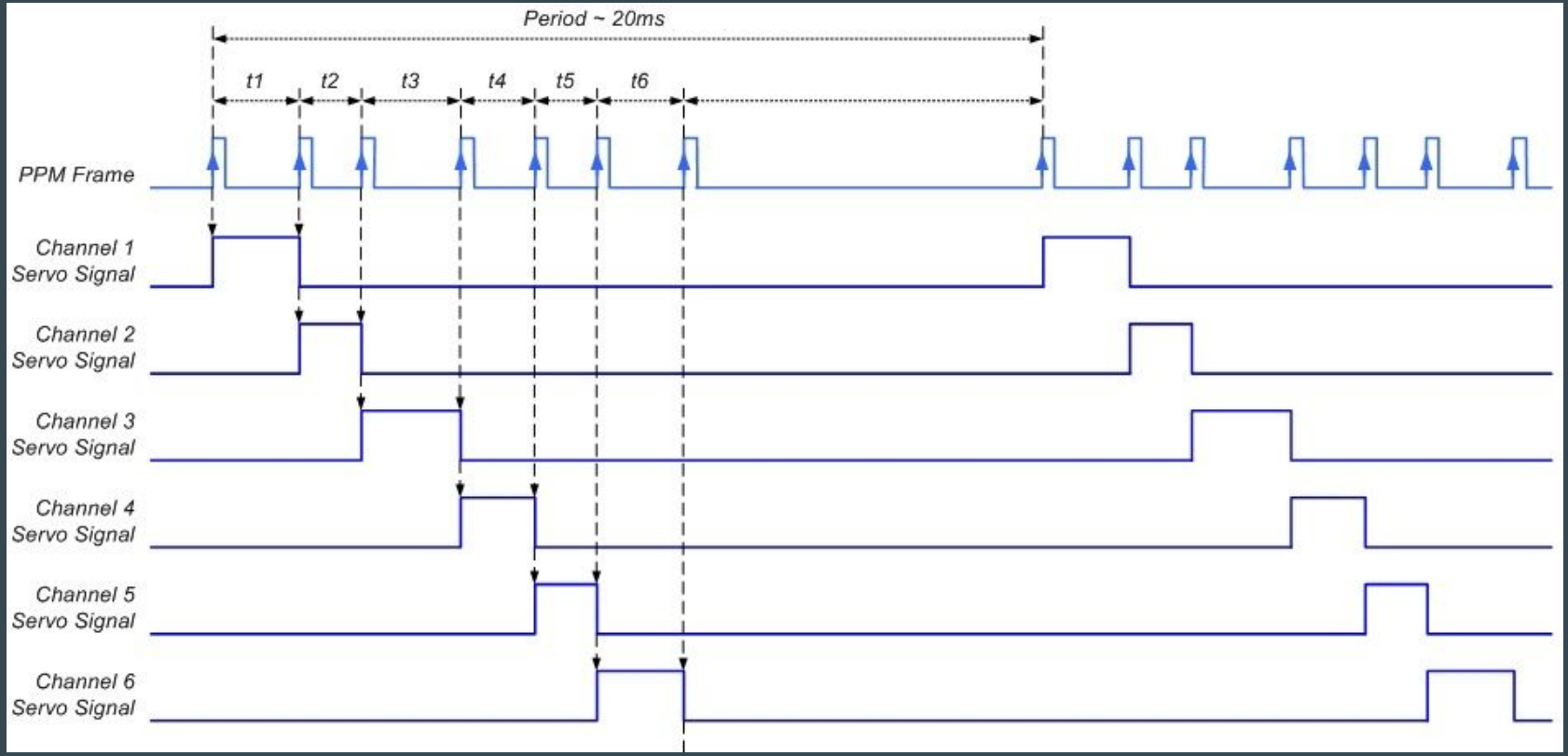


Modelling (HARDWARE) - PPM decoder

OBJECTIVES	COMPONENTS	TESTING STATUS
Generation of 6 ppm channels	Arduino / MSP for PPM generation	Ongoing
Decoding separate channels	FPGA (decoder)	Ongoing



PPM ENCODING DATAFLOW



Modelling - SOFTWARE

PPM decoder

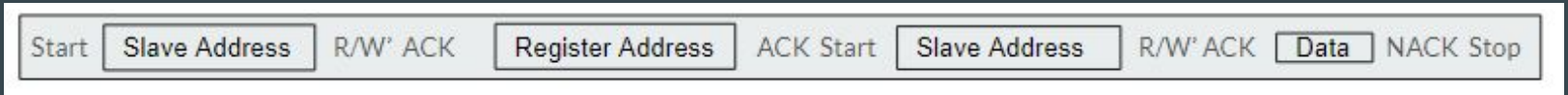
OBJECTIVES	SOFTWARE USED	TESTING STATUS
Create main code for PPM decoding	Quartus II	Completed
Create testbench for PPM decoder	Quartus II	Completed

Modelling - HARDWARE

I2C

OBJECTIVES	COMPONENTS	TESTING STATUS
Implement I2C interface in FPGA	FPGA	Ongoing
Drive MPU-6050 using I2C	FPGA, MPU-6050	Ongoing

- I2C - master reading from slave using SDA and SCL pins



I2C data flow

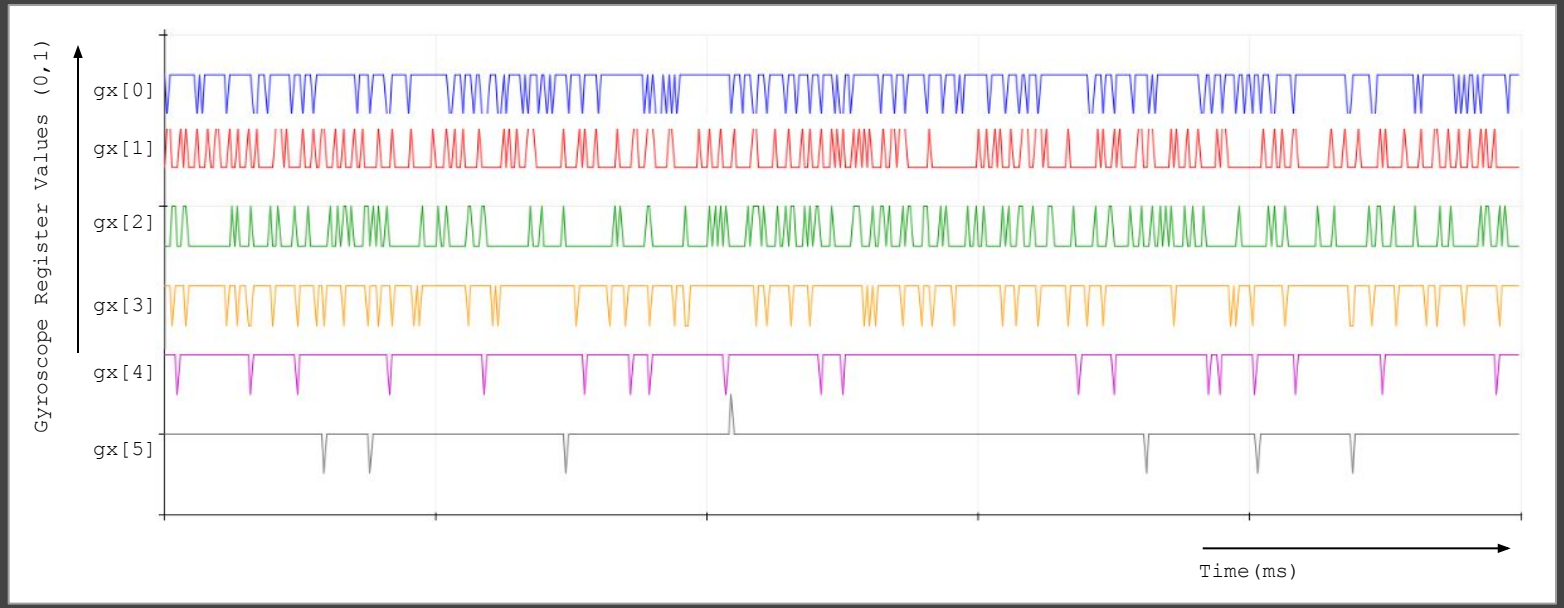
Modelling - SOFTWARE

I2C

OBJECTIVES	SOFTWARE USED	TESTING STATUS
Create master code for I2C interface	Quartus II	Completed
Interface MPU-6050 with I2C master code	Quartus II	Completed

WORK DONE - SOFTWARE

I2C Interface with MPU-6050 on FPGA



Gyroscope registers - gx[15:0], gy[15:0], gz[15:0]

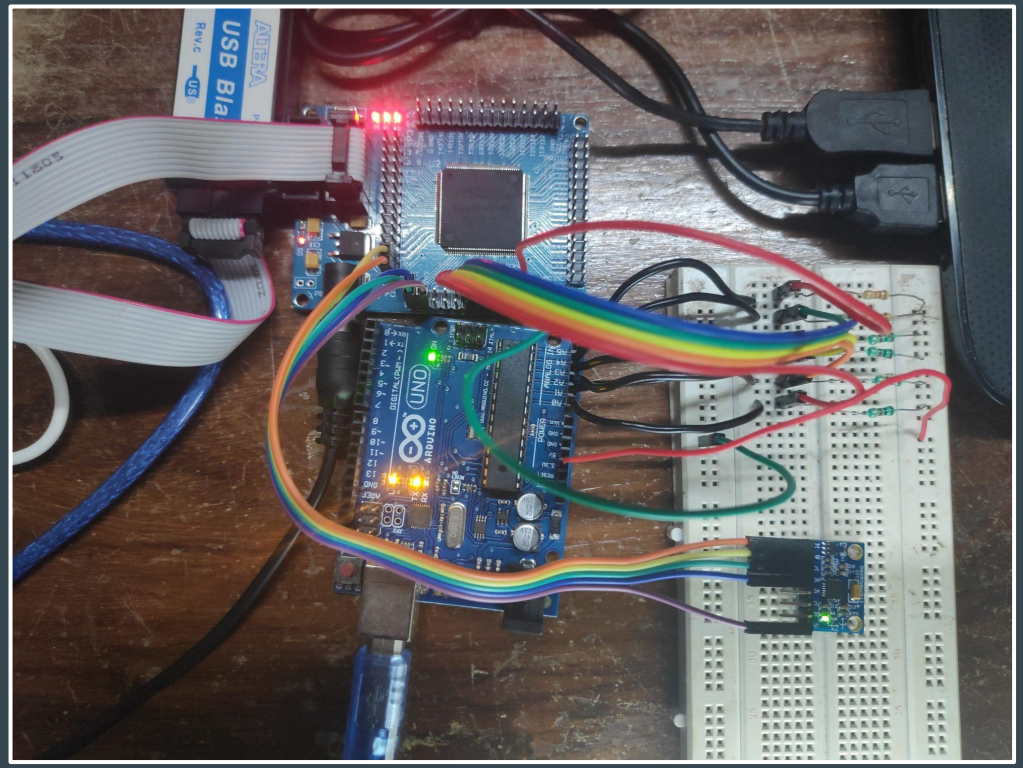
Modelling - SOFTWARE

PWM

OBJECTIVES	SOFTWARE USED	TESTING STATUS
PWM simulation and testbench	Vivado	Completed

WORK DONE - HARDWARE

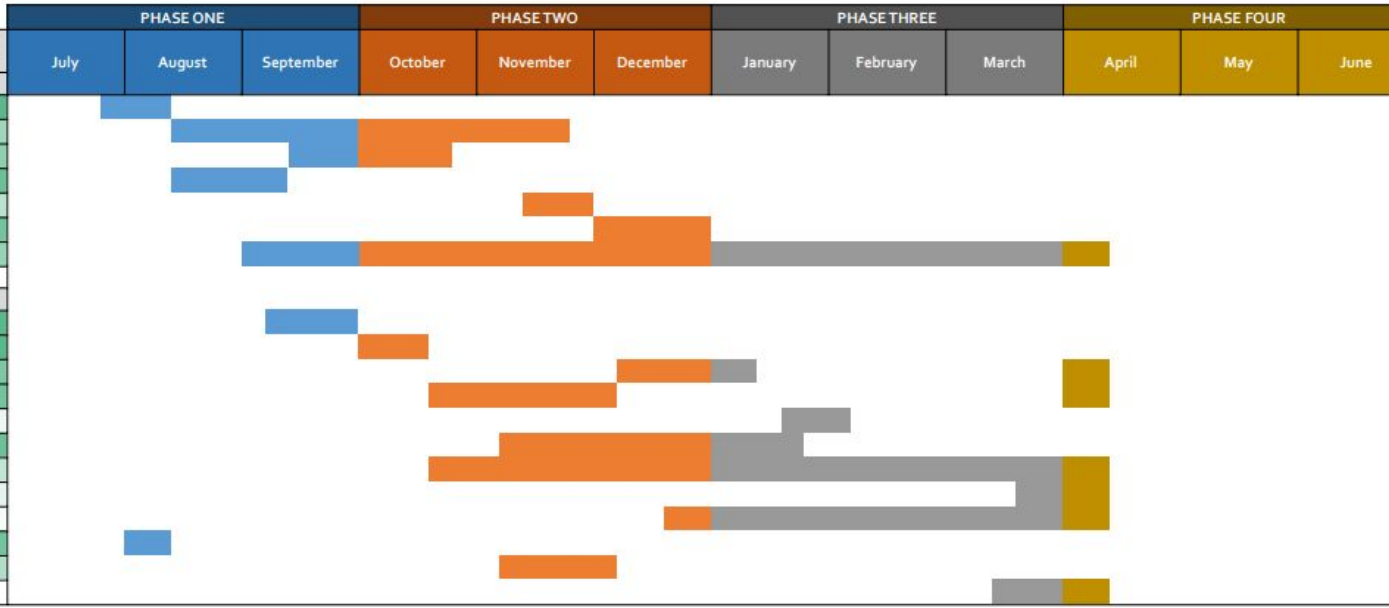
- Used 6 I/O pins of FPGA to assign first 6 bits of the x-axis gyroscope register (gx)
- Used Arduino to read the signals using analog inputs
- Pull up resistors are used for the FPGA I/O pins
- USB Blaster is used to program the FPGA using JTAG interface
- MPU-6050 is the IMU used



GANTT CHART

PROJECT TITLE	FPGA FLIGHT CONTROLLER
PROJECT GUIDE	Mr. Jagadeesh Kumar P
GROUP MEMBERS	Athul John Kurian (AJK), Medha Lakshman Rao(MLR), Omar Bin Shafi(OBS), Sebastian James (SJ)
DATE	14th April 2021

SL. NO.	TASK TITLE	TASK OWNER	PCT OF TASK COMPLETE
1	Project Conception and Initiation		
1.1	Topic Selection	OBS, AJK,SJ, MLR	100%
1.2	Literature Review	OBS, AJK,SJ	60%
1.3	Feasibility Study	MLR,OBS,SJ	70%
1.4	Project Planning	OBS, AJK,SJ,MLR	90%
1.5	Project Initiation	OBS, AJK, MLR	45%
1.6	Scope & Goal Setting	SJ,AJK,MLR	85%
1.7	Background study	SJ	65%
2	Tasks		
2.1	Software installations	OBS, MLR, AJK, SJ	100%
2.2	Getting to know the software	OBS, MLR, AJK, SJ	100%
2.3	PPM Decoder	AJK	80%
2.4	I2C Communication, filter	OBS, SJ	85%
2.5	PID Loop	OBS, AJK	15%
2.6	PWM Encoder	MLR	90%
2.7	Simulation	AJK, MLR, OBS	40%
2.8	Component Testing	AJK, OBS	20%
2. 10	Debugging	AJK, OBS	10%
2.11	Finalising the project	SJ, AJK	85%
2.12	Novelty	SJ, AJK	50%
2.13	Conference Paper Presentation	MLR, SJ	5%



Status of Paper preparation

Selection of Conference / Journal

IEEE Conference

Progress

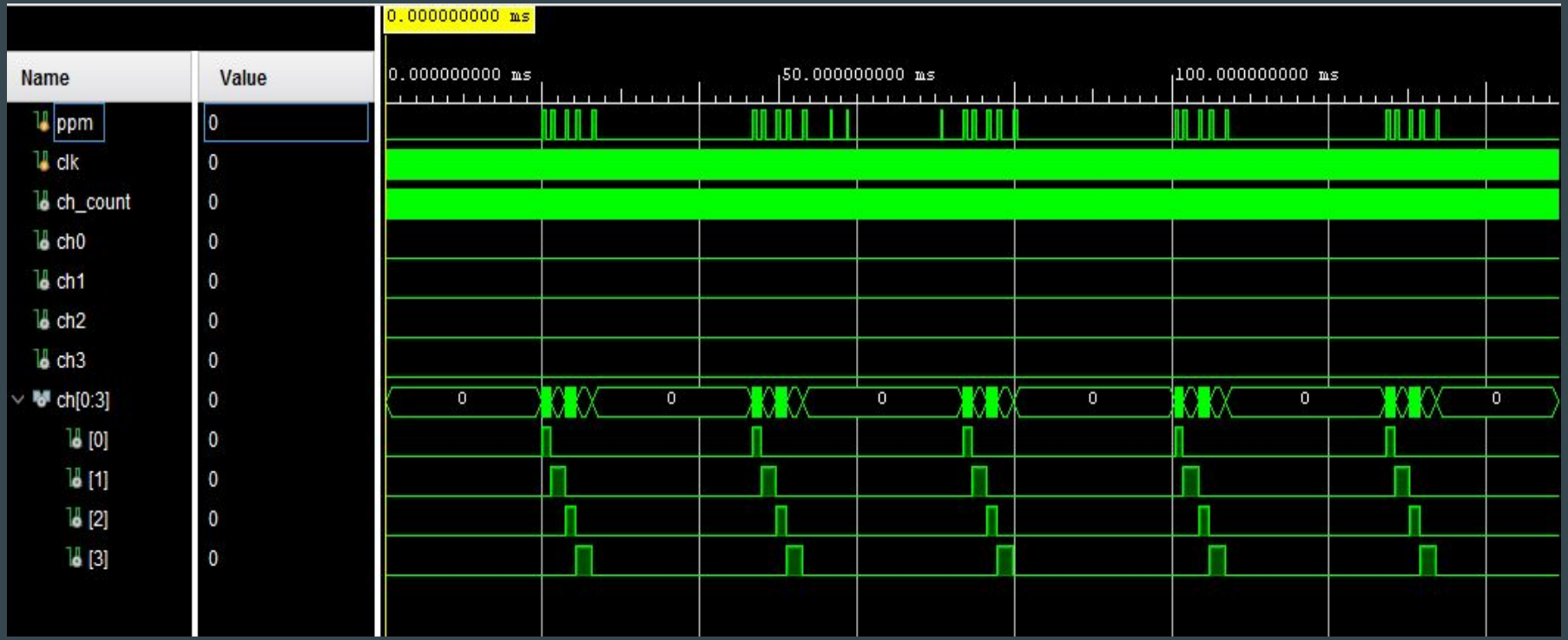
Introduction
Methodology
Simulations

WORK SCHEDULE

Deadlines	April	May
20th	Implementation of MPU code	Combining individual components
25th	Implementation of I2C	Debugging
30th	Implementation of PID	Documentation and Report

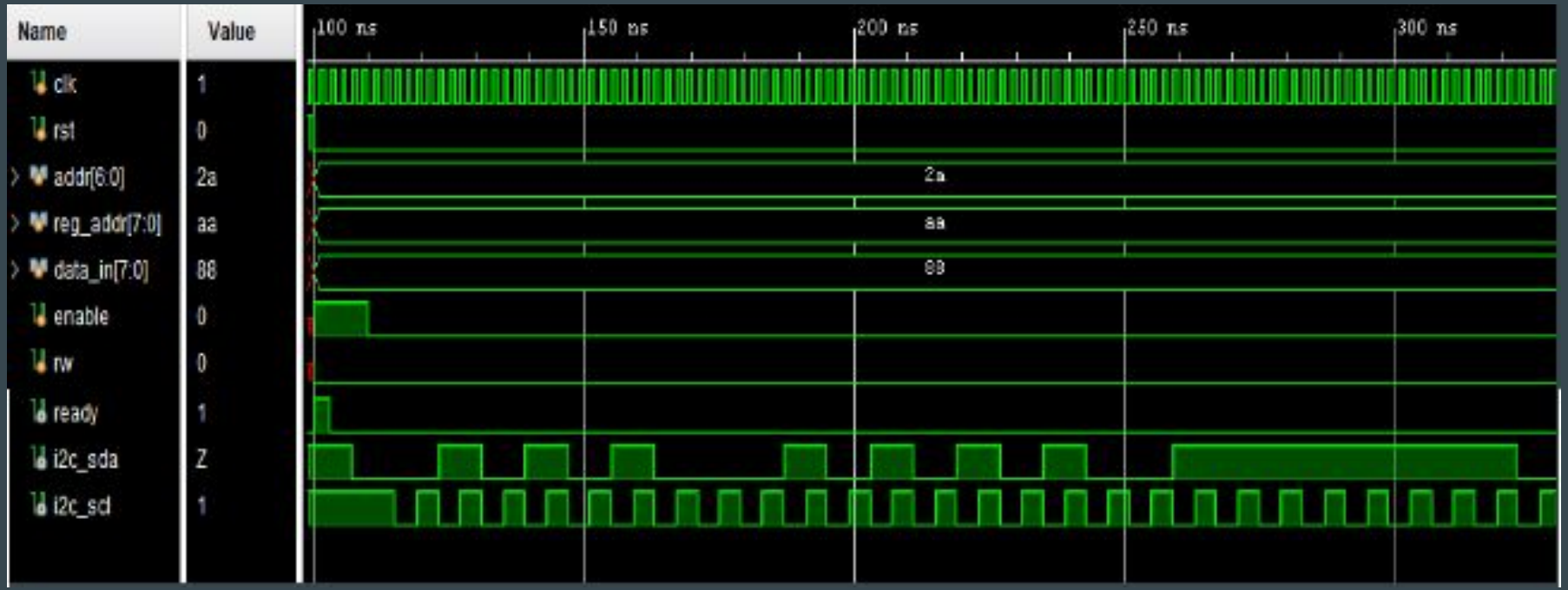
Simulation

PPM decoder



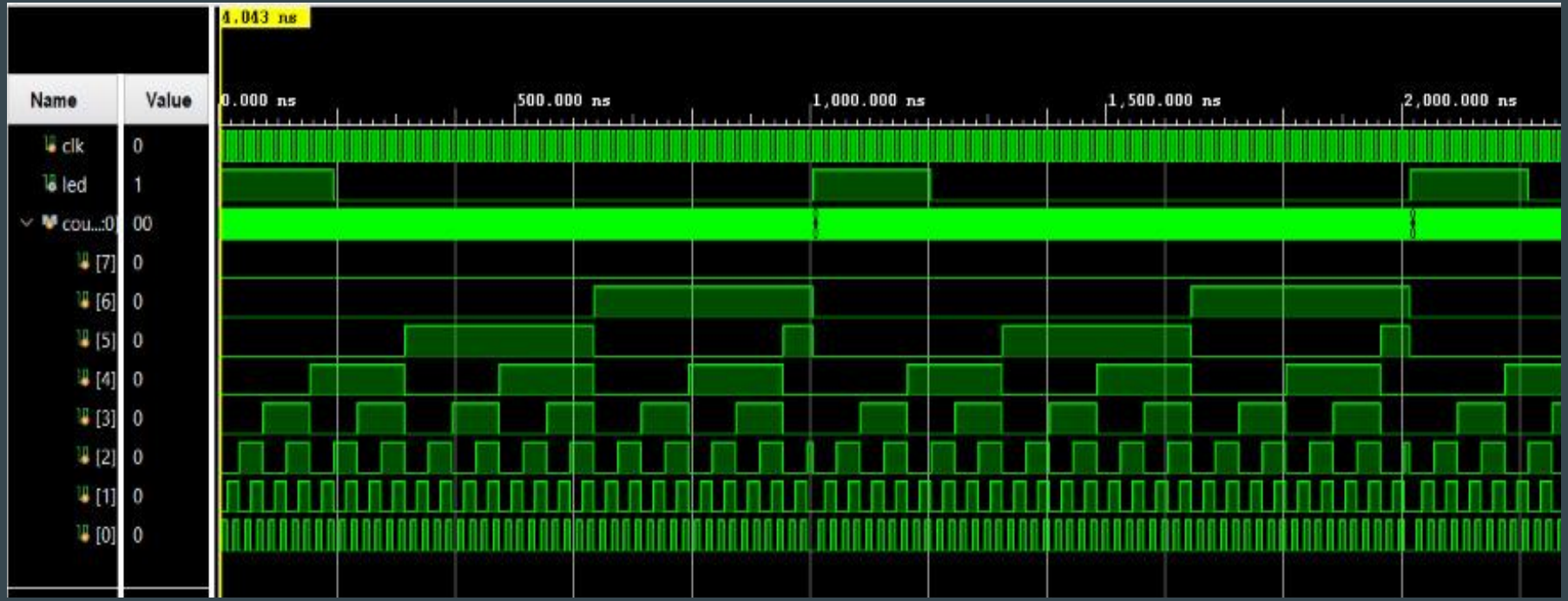
Simulation

I2C



Simulation

PWM encoder



INDIVIDUAL CONTRIBUTIONS

- Athul
  - Familiarised with Vivado ISE and Quartus II
  - Learned basics of PID.
  - Completed PPM decoding in Verilog, hardware implementation pending.
  - I2C implementation - ongoing.
- Medha
  - Familiarised with Vivado ISE and Quartus II.
  - Implementation of PWM encoding.
- Omar
  - Familiarised with Vivado ISE and Quartus II.
  - Learned filter design, started to implement filter.
- Sebastian
  - Learned the basics of FPGA from Coursera; familiarized with Quartus Prime.
  - Read the reference papers & texts, learning verilog.
  - Learned I2C implementation in detail.

CONCLUSION

- Developed firmware of PPM decoding and hardware testing in progress.
- Developed I2C communication protocol to interface with MPU 6050 module.
- Developed firmware for PWM encoding.

REFERENCES

[1] N. Monterrosa, J. Montoya, F. Jarquín and C. Bran, "Design, development and implementation of a UAV flight controller based on a state machine approach using a FPGA embedded system," 2016 IEEE/AIAA 35th Digital Avionics Systems Conference (DASC), Sacramento, CA, 2016, pp. 1-8, doi: 10.1109/DASC.2016.7778069.

[2] B. L. Sharma, N. Khatri and A. Sharma, "An analytical review on FPGA based autonomous flight control system for small UAVs," 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), Chennai, 2016, pp. 1369-1372, doi: 10.1109/ICEEOT.2016.7754907.

[3] Gadde, Premkumar & Rajmohan, Jayalakshmi. (2018). “Design and Implementation of FPGA Based Quadcopter”, International Journal of Engineering Technology Science and Research, ISSN 2394 – 3386., 2018, Volume 5, Issue 3.

Thank You!