

# FPGA Based Flight Controller

## Project Guide:

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# INTRODUCTION

## Motivation

- Faster response provided by parallelism, more capacity for FPGA are key motivations.

## Objectives

- To design a flight controller (FC) system on an FPGA board.
- Achieve stable flight using PID controller.

## Scope & Relevance

- FC is the brain of the drone and is critical in maneuvering the drone. Drones have wide range of applications from agriculture to military.

# LITERATURE REVIEW

SL NO	YEAR	TITLE & SOURCE	OBJECTIVES	METHODOLOGY	RESULT	LIMITATIONS
1	2019	<b>TITLE</b> Designing multiple pid controllers based on an fpga for controlling the temperature of tem-cell surfaces [1] <b>SOURCE</b> SIBIRCON	Computing PID controllers with different sets of parameters.	Verilog HDL in Quartus, PID controller, I2C protocol.	Processing speed of PWM algo is important.	RAM, ROM are required.

# LITERATURE REVIEW

SL NO	YEAR	TITLE & SOURCE	OBJECTIVES	METHODOLOGY	RESULT	LIMITATIONS
2	2019	<b>TITLE</b> An Implementation of the System on Chip Control System for a FPGA-Based Computer Vision Accelerator [2] <b>SOURCE</b> ISOCC	To build a high efficiency and compact system, which also provides flexibility and convenience for machine control.	Made use of FPGA and tested on a drone. Programmable logic is used for sensor interfaces such as motor drivers.	Real time control was feasible. Parallel processing, power efficient and advantageous for miniaturization.	Heavy, high cost, high end FPGA has been used.

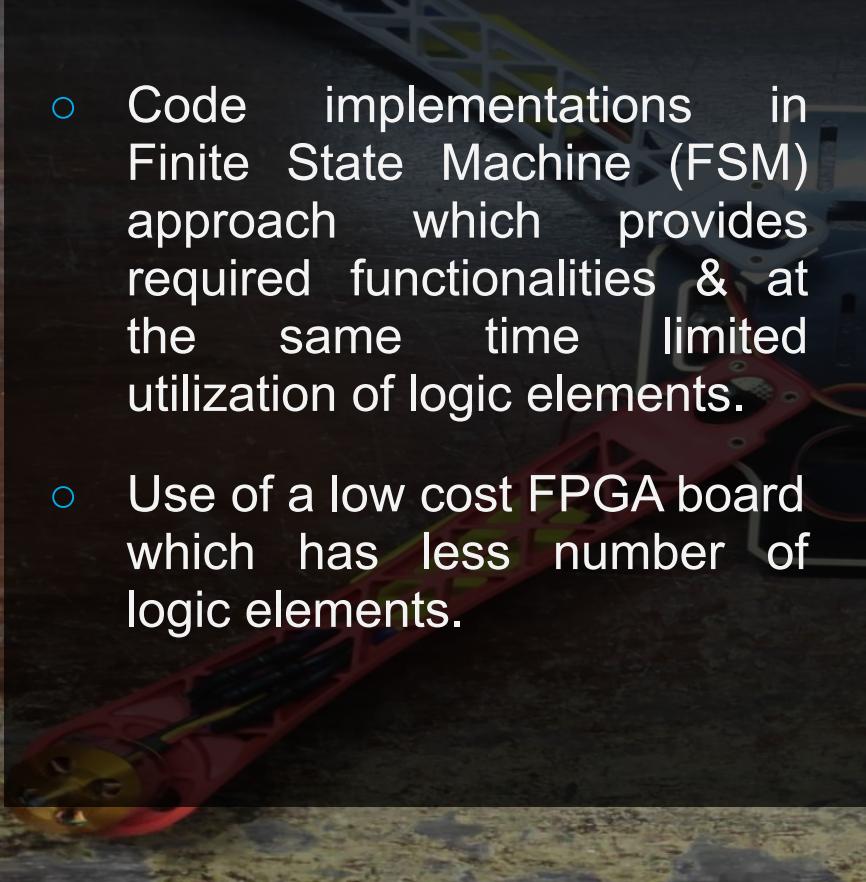
# LITERATURE REVIEW

SL NO	YEAR	TITLE & SOURCE	OBJECTIVES	METHODOLOGY	RESULT	LIMITATIONS
3	2018	<b>TITLE</b> Design and Implementation of FPGA Based Quadcopter [3]  <b>SOURCE</b> IJETSR	PWM encoder/decoder Design  Study Basic Block diagram of the FC  Mapping unit to produce output for motors from roll, pitch, yaw, throttle	FPGA Block Diagram PWM encoder  PWM signal generator PWM decoder  Mapping unit	Relation between the Motor output - Throttle, Roll, pitch and yaw required.	No PPM encoder/decoder is implemented.

Table 1. Summary of Literature Review

# NOVELTY

- Code implementations in Finite State Machine (FSM) approach which provides required functionalities & at the same time limited utilization of logic elements.
- Use of a low cost FPGA board which has less number of logic elements.



# PROJECT DESCRIPTION

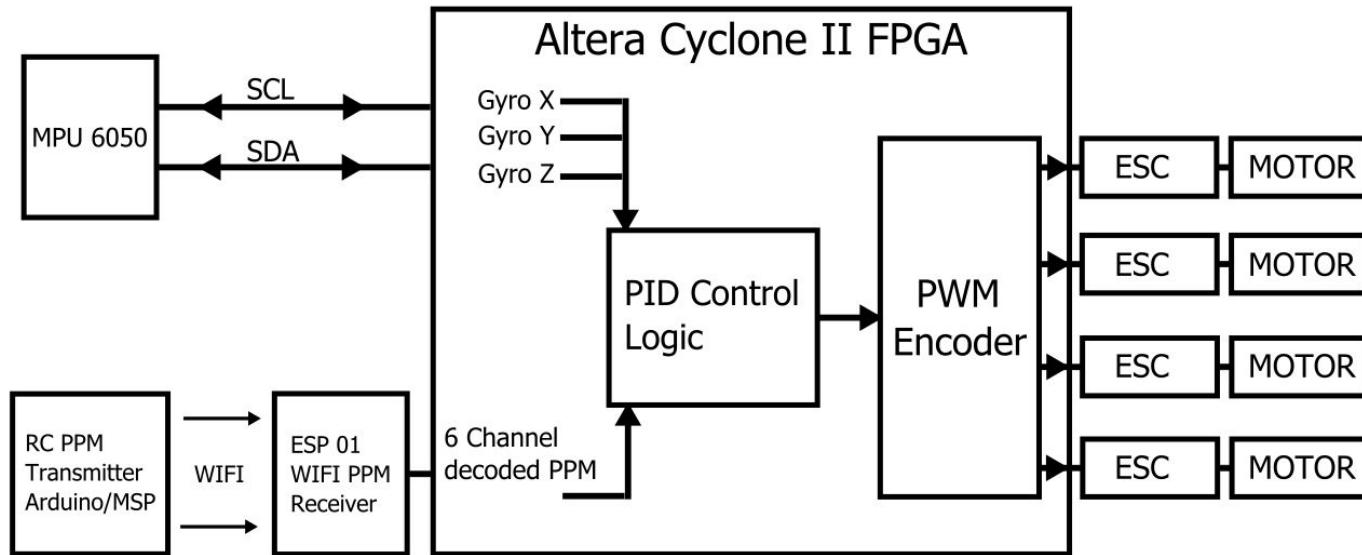


Figure 1. FPGA Based FC Block Diagram

# HARDWARE

	OBJECTIVES	COMPONENTS	PURPOSE
PPM	Generation of 6 ppm channels	Arduino/MSP/E SP01 for PPM generation	For encoding before transmission of RC inputs.
	Decoding separate channels	FPGA (decoder)	For decoding the received values.
I2C	Implement I2C interface in FPGA	FPGA	To interface with MPU 6050
	Drive MPU-6050 using I2C	FPGA, MPU-6050	To get real time gyro values

Table 2. Details of Hardware

# SOFTWARE

	OBJECTIVES	SOFTWARE USED	PURPOSE
PPM	Create main code & testbench for PPM decoding		Code editor, Altera-modelsim simulator, timing analyzer, synthesizer, Logic Analyzer
I2C	Create master code for I2C interface	Quartus II	Code editor, Altera-modelsim simulator, timing analyzer, synthesizer, Logic Analyzer
	Interface MPU-6050 with I2C master code		
PWM	PWM simulation and testbench		

Table 3. Details of Software

# METHODOLOGY

PPM DECODER

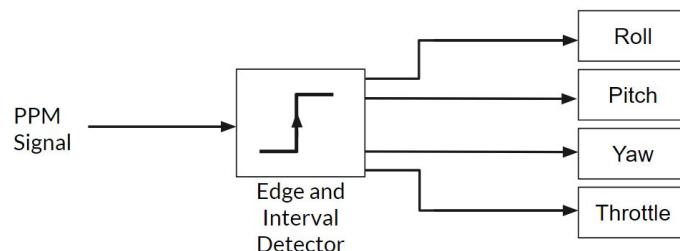


Figure 2. PPM decoder logic

PWM ENCODER

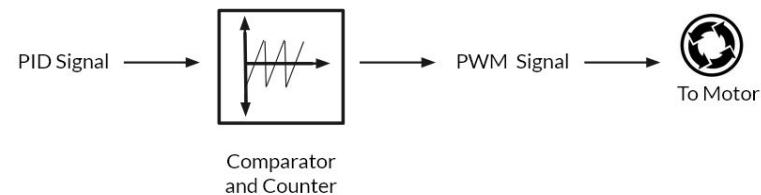


Figure 4. PWM encoder logic

I2C FRAME  
STRUCTURE

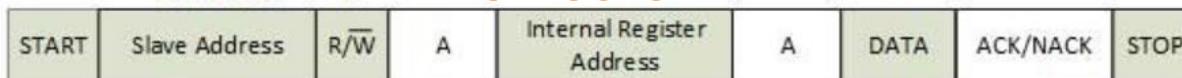


Figure 3. I2C data flow

# FLOW CHART

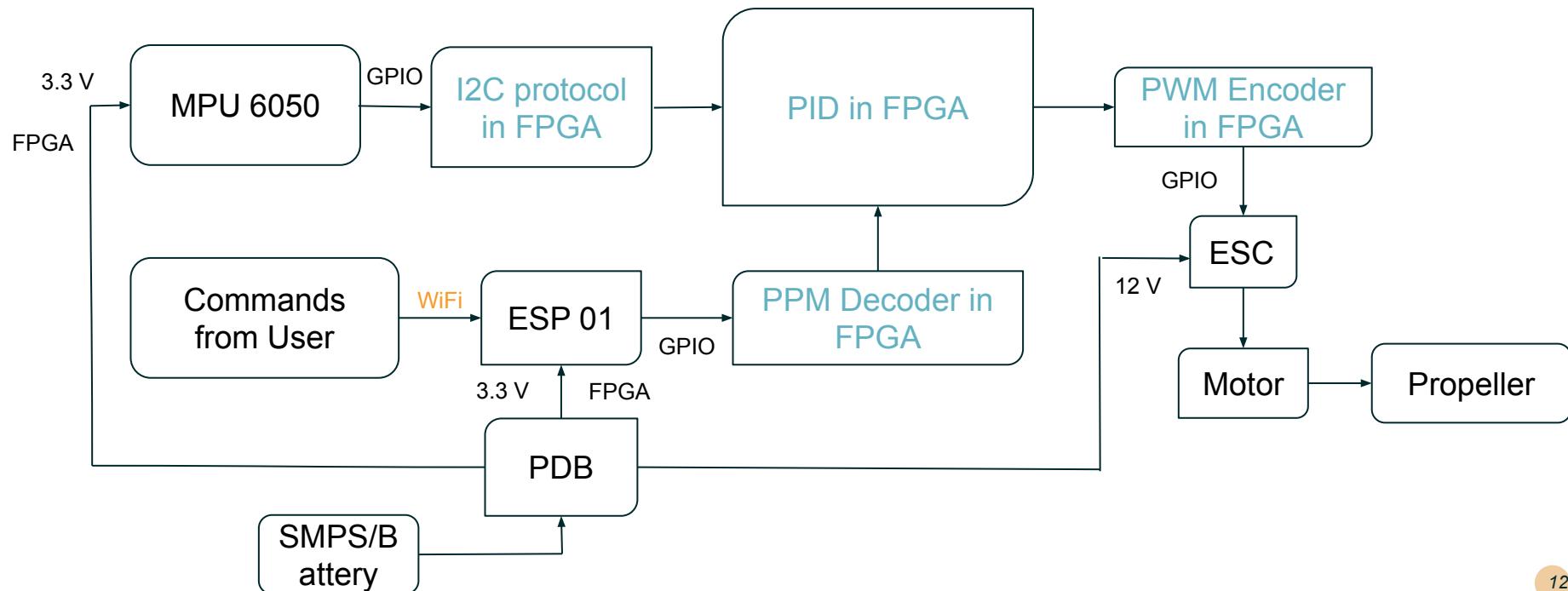


Figure 5. Flow Chart of the Project

# Total Cost

Sl. No.	Component Name	Cost
1	POWER DISTRIBUTION BOARD WITH XT60 connector	453
2	F450 Quadcopter Kit with 4 Pcs. A2212 KV1000 Brushless Motor and 4 Pcs. 30A ESC and 4 Pair 1045 Propeller	3090
3	ALTERA FPGA Cyclone II EP2C5T144 System Development Board	1624
4	USB Blaster ALTERA CPLD/FPGA Programmer	699
5	ESP-01 ESP8266 Serial WIFI Wireless Transceiver Module	208
6	Male To Female Jumper Wires 40 Pcs 10cm	55

**Total Cost:** 6129

Table 4. Cost distribution of components used

# RESULT: SIMULATIONS

## PPM Decoder

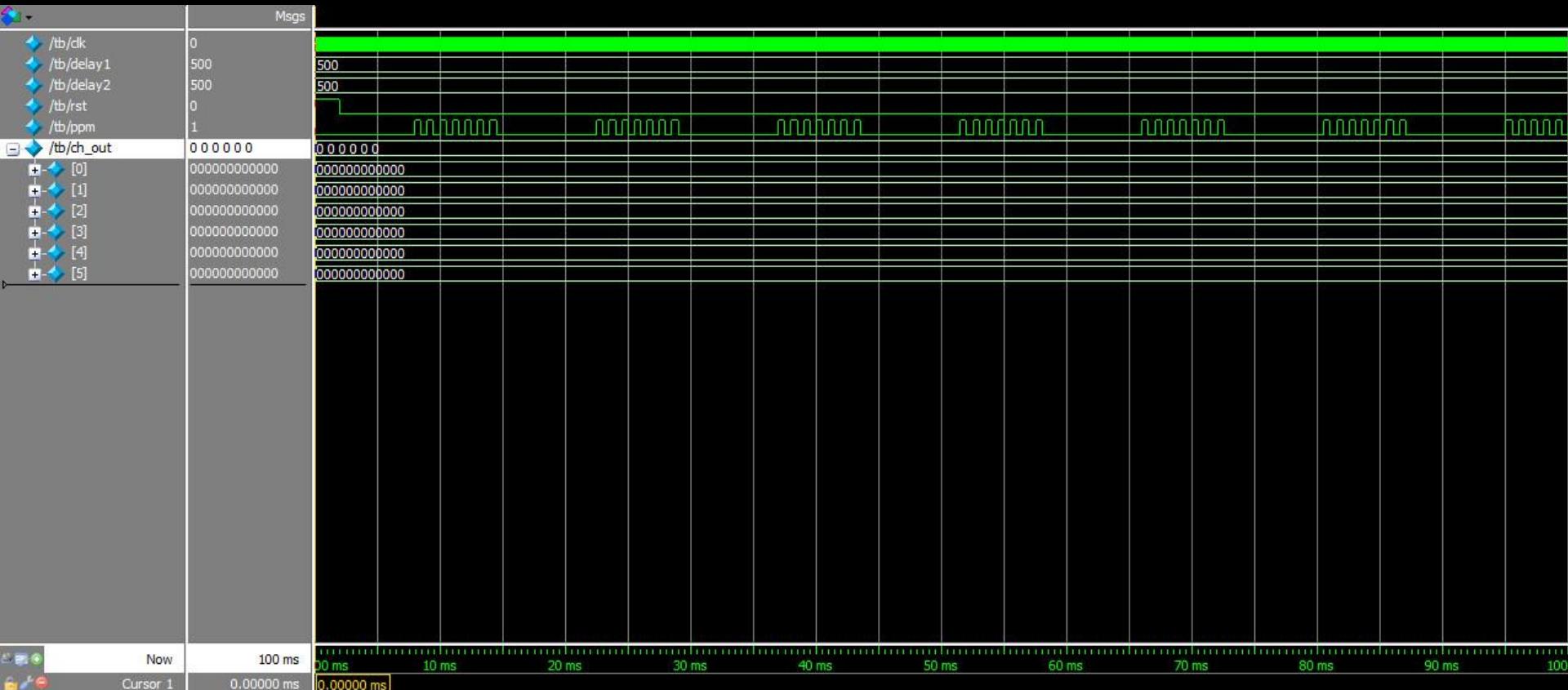


Figure 6-1. PPM decoder Simulation in Quartus II

# RESULT: SIMULATIONS

## PPM Decoder

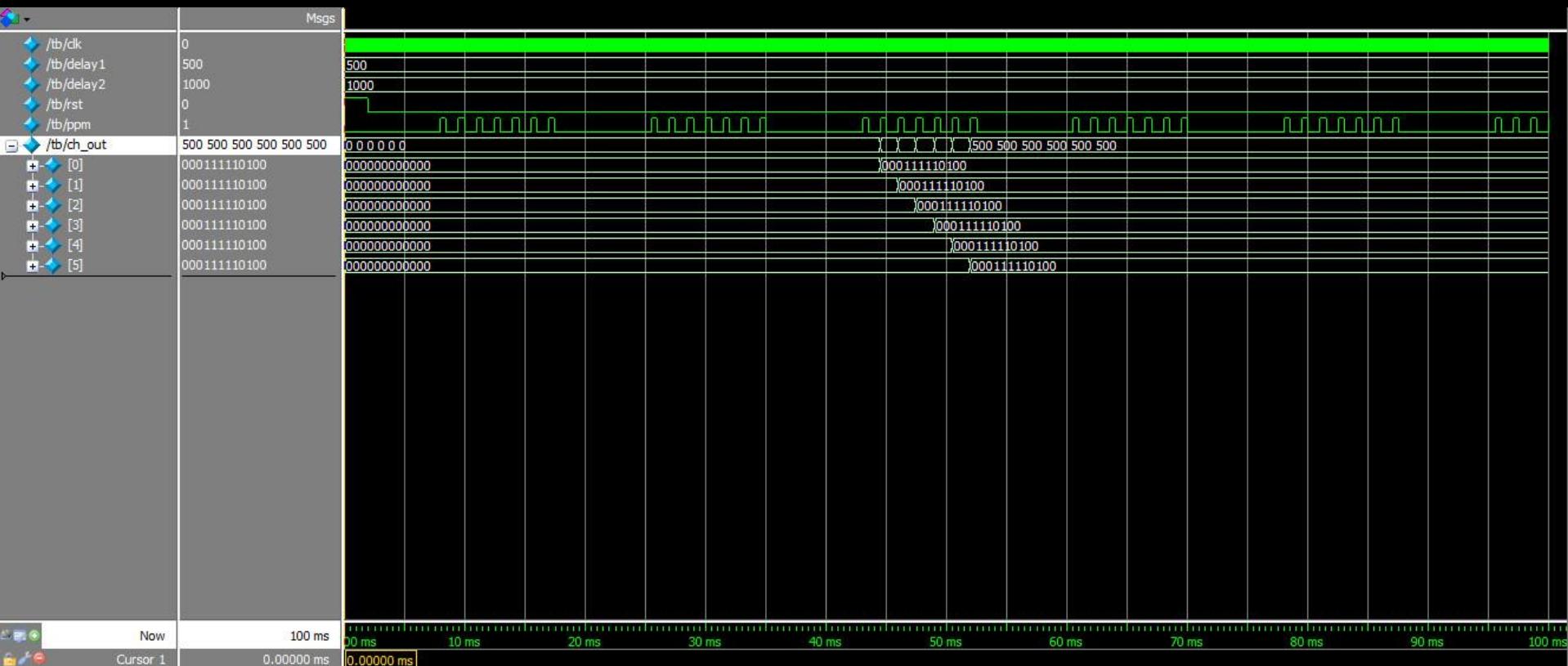


Figure 6-2. PPM decoder Simulation in Quartus II

# RESULT: SIMULATIONS

## PPM Decoder



Figure 6-3. PPM decoder Simulation in Quartus II

## RESULT: SIMULATIONS

### I2C

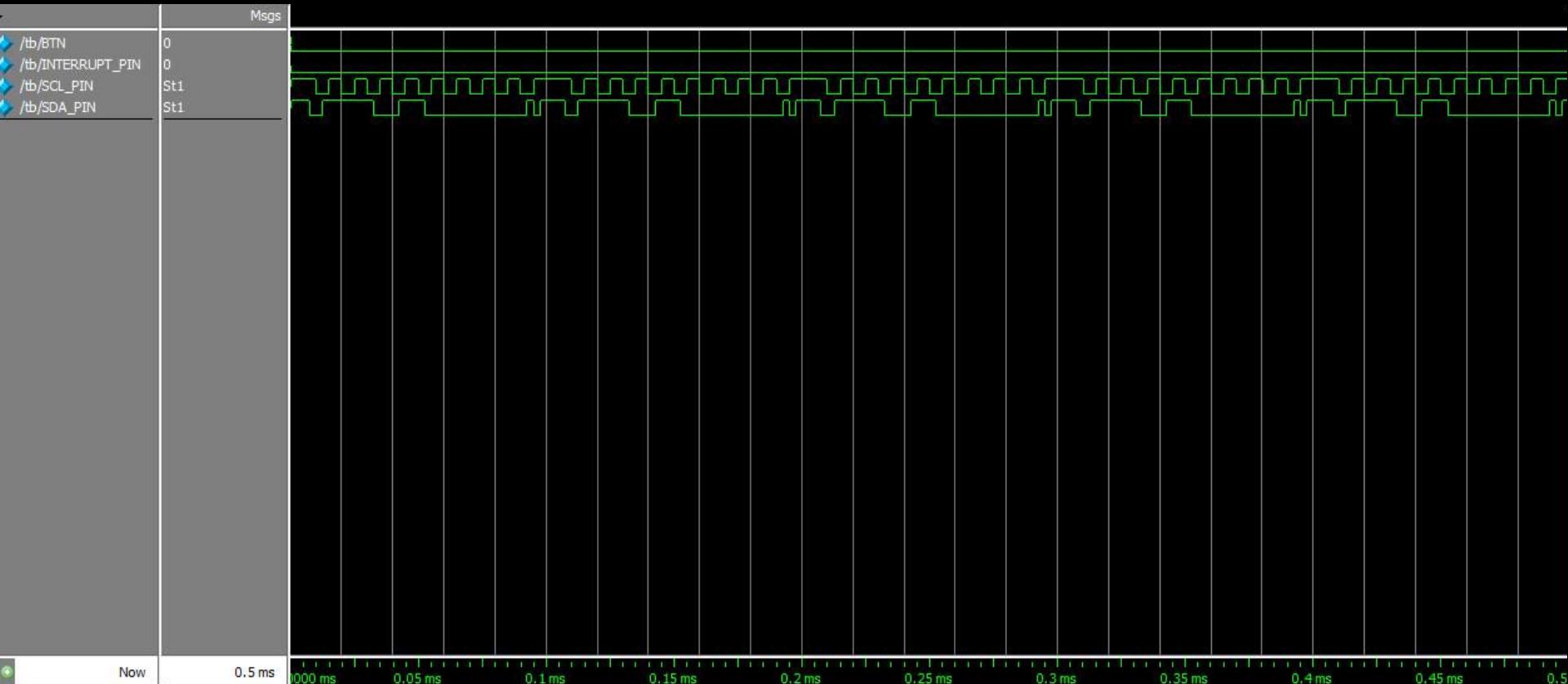


Figure 7. I2C Simulation in Quartus II

# RESULT: SIMULATIONS

## PWM encoder

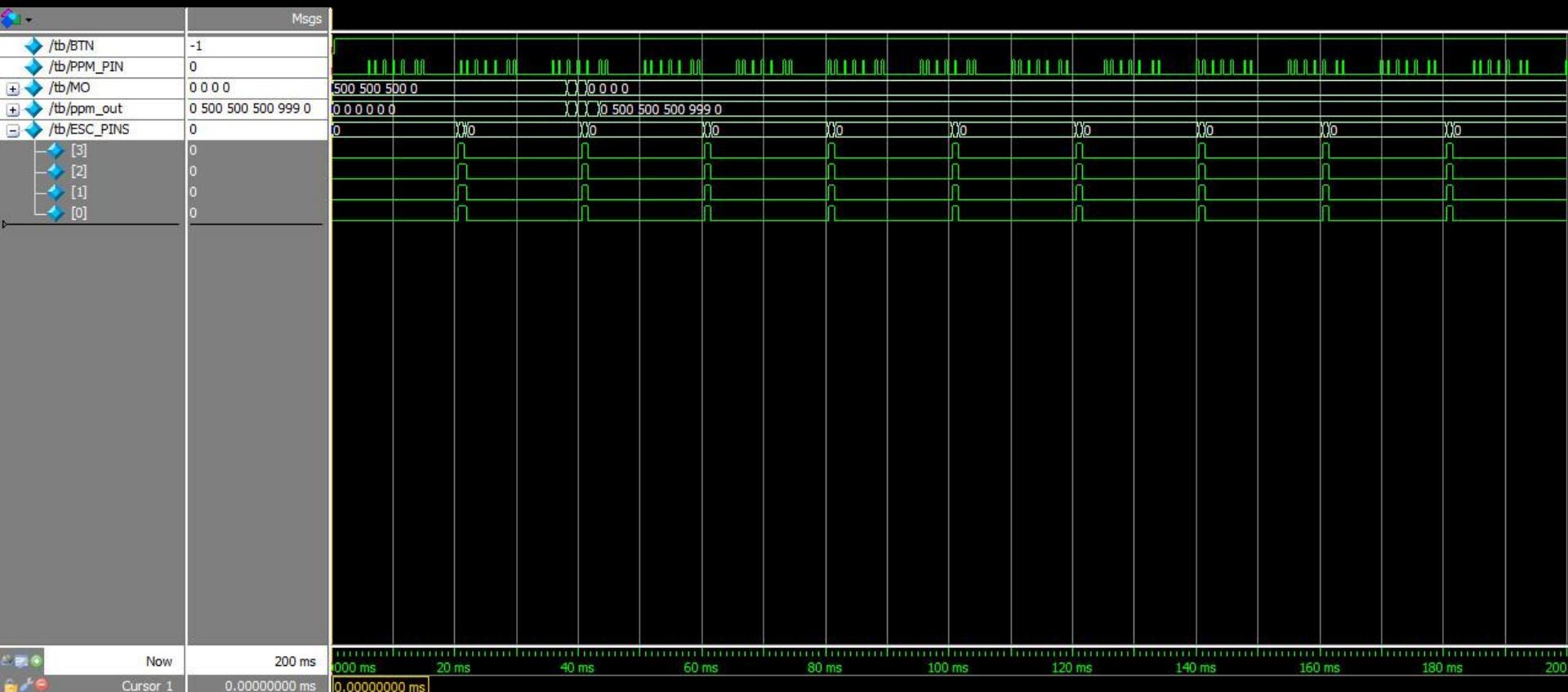


Figure 8-1. PWM encoder Simulation in Quartus II

## RESULT: SIMULATIONS

# PWM encoder

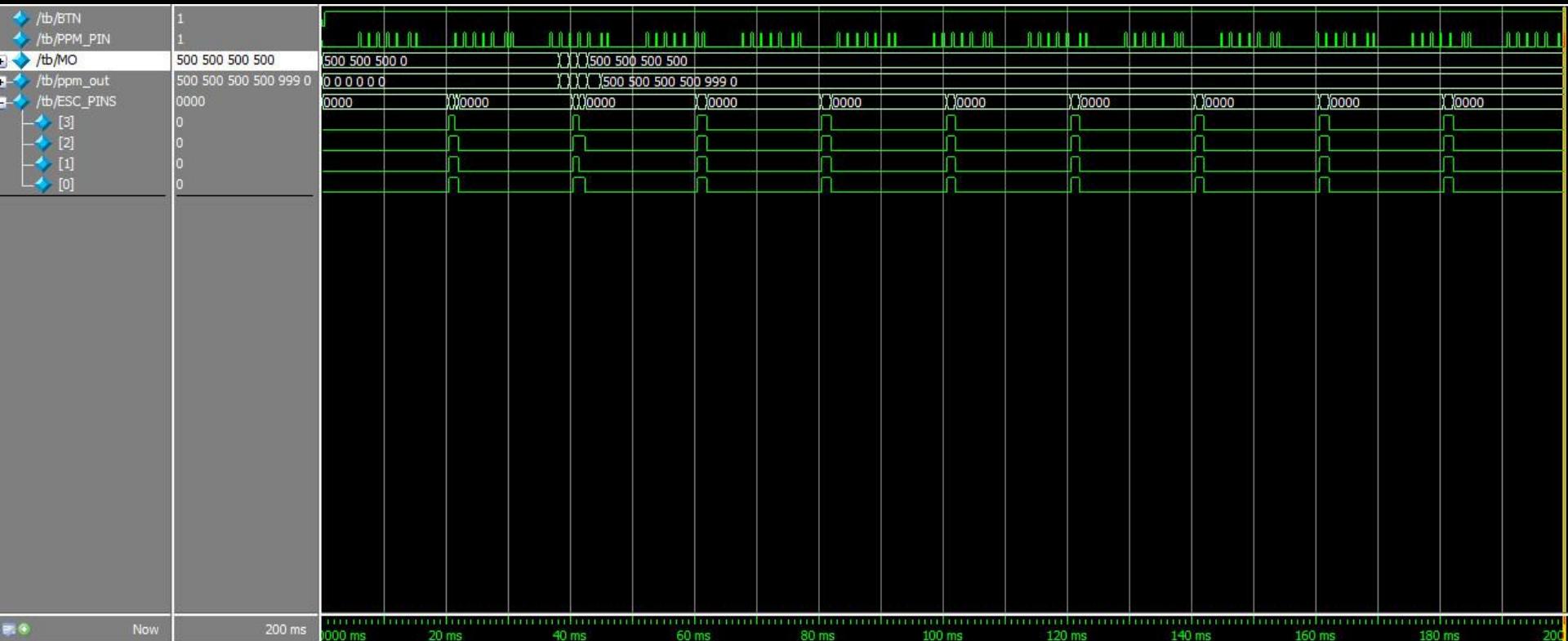


Figure 8-2. PWM encoder Simulation in Quartus II

# RESULT: SIMULATIONS

## PWM encoder

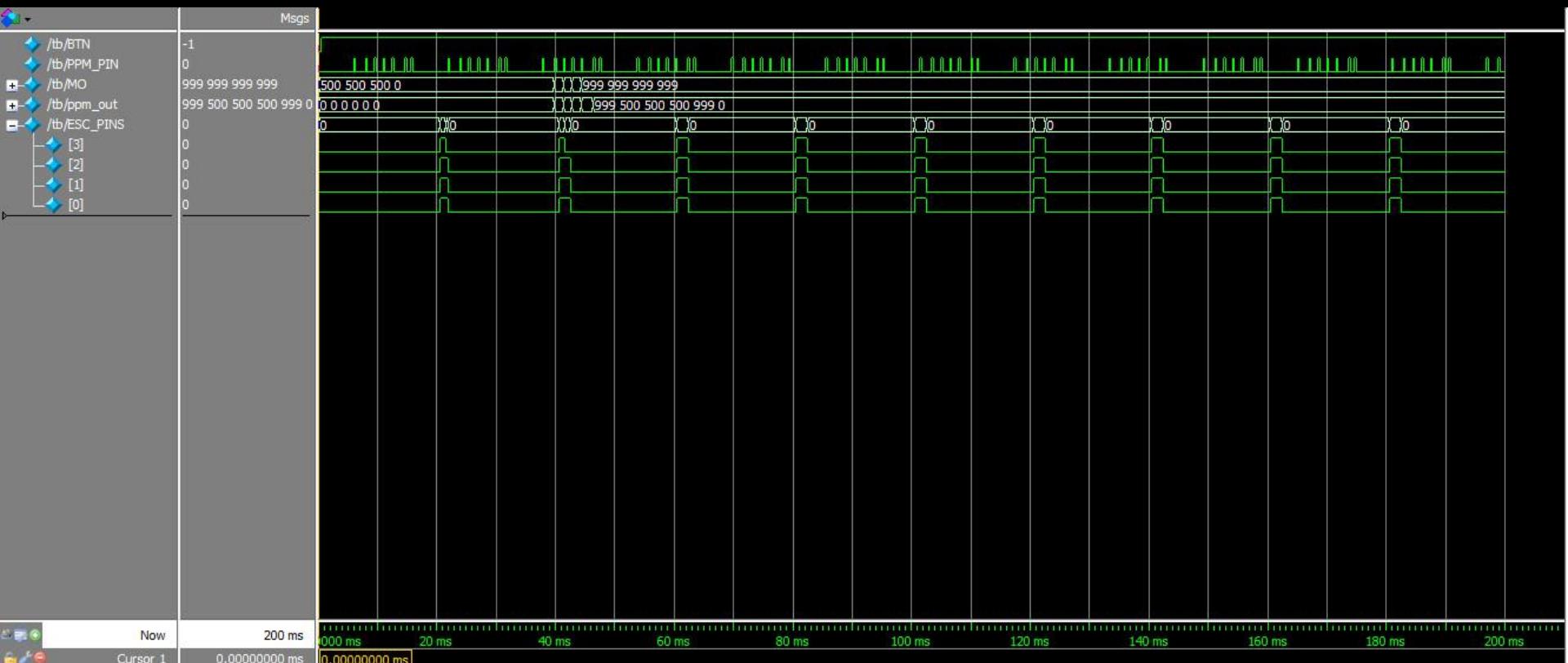


Figure 8-3. PWM encoder Simulation in Quartus II

# RESULT: SIMULATIONS

## PWM encoder Roll

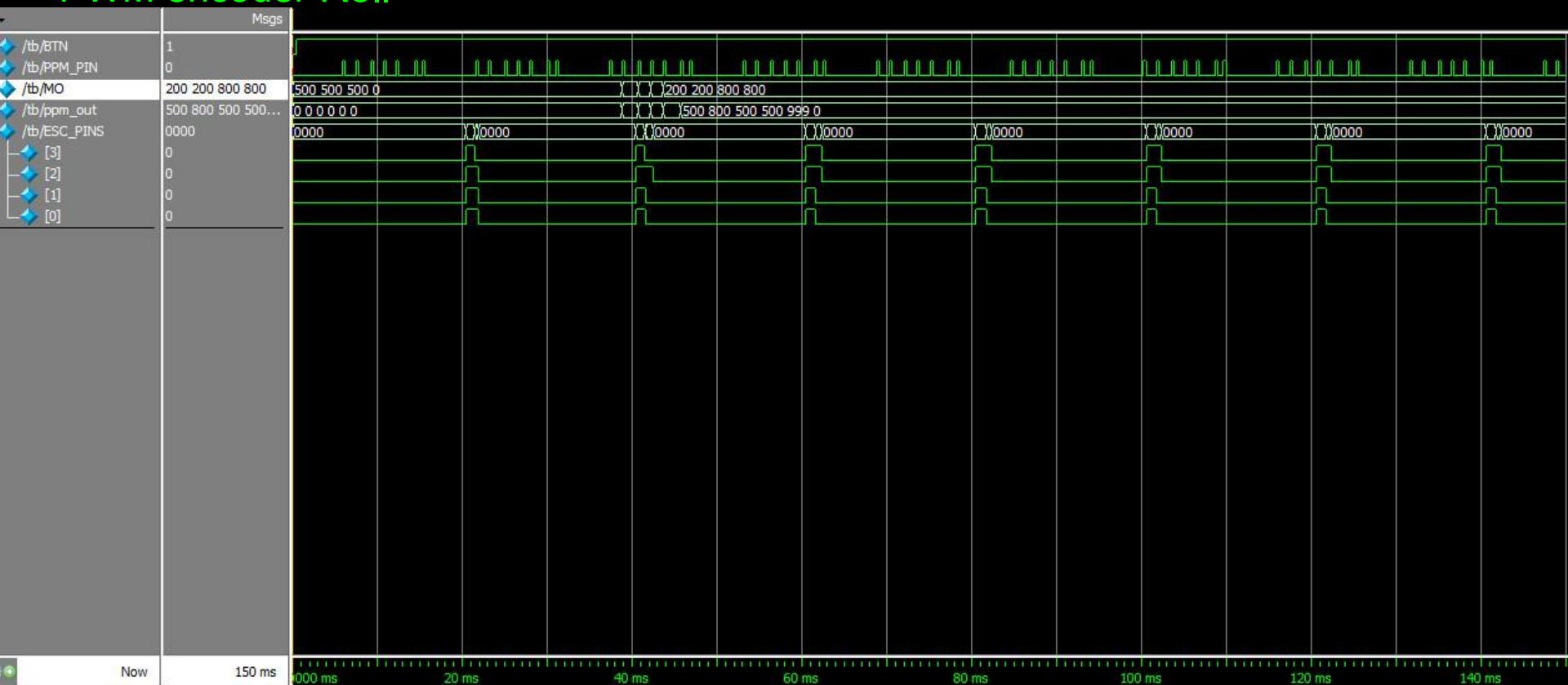


Figure 8-4. PWM encoder Simulation in Quartus II

# RESULT: SIMULATIONS

## PWM encoder Pitch

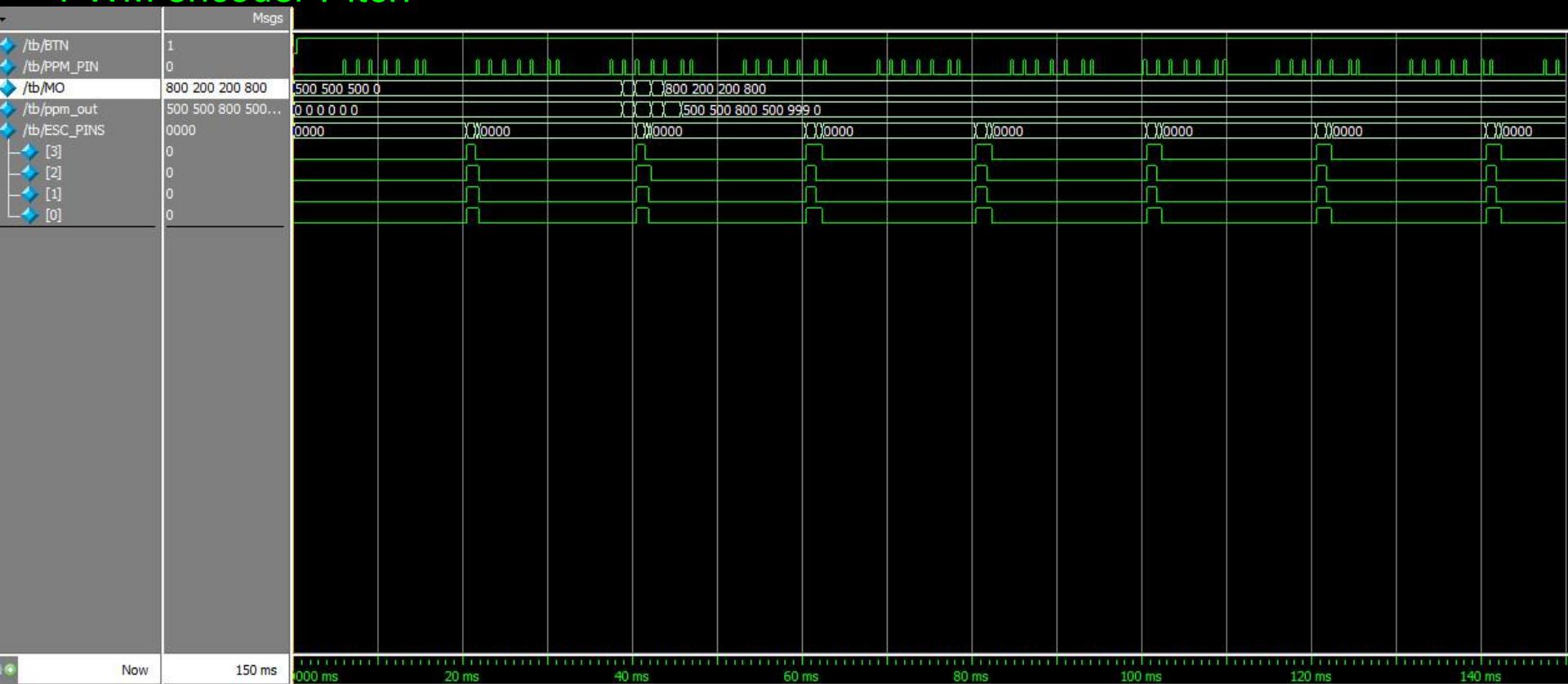


Figure 8-5. PWM encoder Simulation in Quartus II

# VALIDATION OF RESULTS

Flow Status	Successful - Wed May 19 18:19:45 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	ppm_decoder
Top-level Entity Name	main
Family	Cyclone II
Device	EP2C5T144C8
Timing Models	Final
Total logic elements	3,715 / 4,608 ( 81 % )
Total combinational functions	3,475 / 4,608 ( 75 % )
Dedicated logic registers	1,373 / 4,608 ( 30 % )
Total registers	1373
Total pins	10 / 89 ( 11 % )
Total virtual pins	0
Total memory bits	0 / 119,808 ( 0 % )
Embedded Multiplier 9-bit elements	26 / 26 ( 100 % )
Total PLLs	0 / 2 ( 0 % )

Table 5. Synthesis Result

Type	Alias	Name	0	Value	1
in		BTN		1	
in		PPM_PIN		0	
R		+ ... r:decoder ch[0][11..0]		500	
R		+ ... r:decoder ch[1][11..0]		707	
R		+ ... r:decoder ch[2][11..0]		400	
R		+ ... r:decoder ch[3][11..0]		506	
R		+ ... r:decoder ch[4][11..0]		0	
R		+ ... r:decoder ch[5][11..0]		999	
io		SCL_PIN		1	
io		SDA_PIN		0	
out		+ gyro_xout		14515	
out		+ gyro_yout		1666	
out		+ gyro_zout		-3602	
C		+ ... ncoder:encoder val[0]		555	
C		+ ... ncoder:encoder val[1]		190	
C		+ ... ncoder:encoder val[2]		190	
C		+ ... ncoder:encoder val[3]		567	
out		+ b_right		555	
out		+ f_right		153	
out		+ f_left		141	
out		+ b_left		567	

Table 6. Logic Analyzer Output

# VALIDATION OF RESULTS

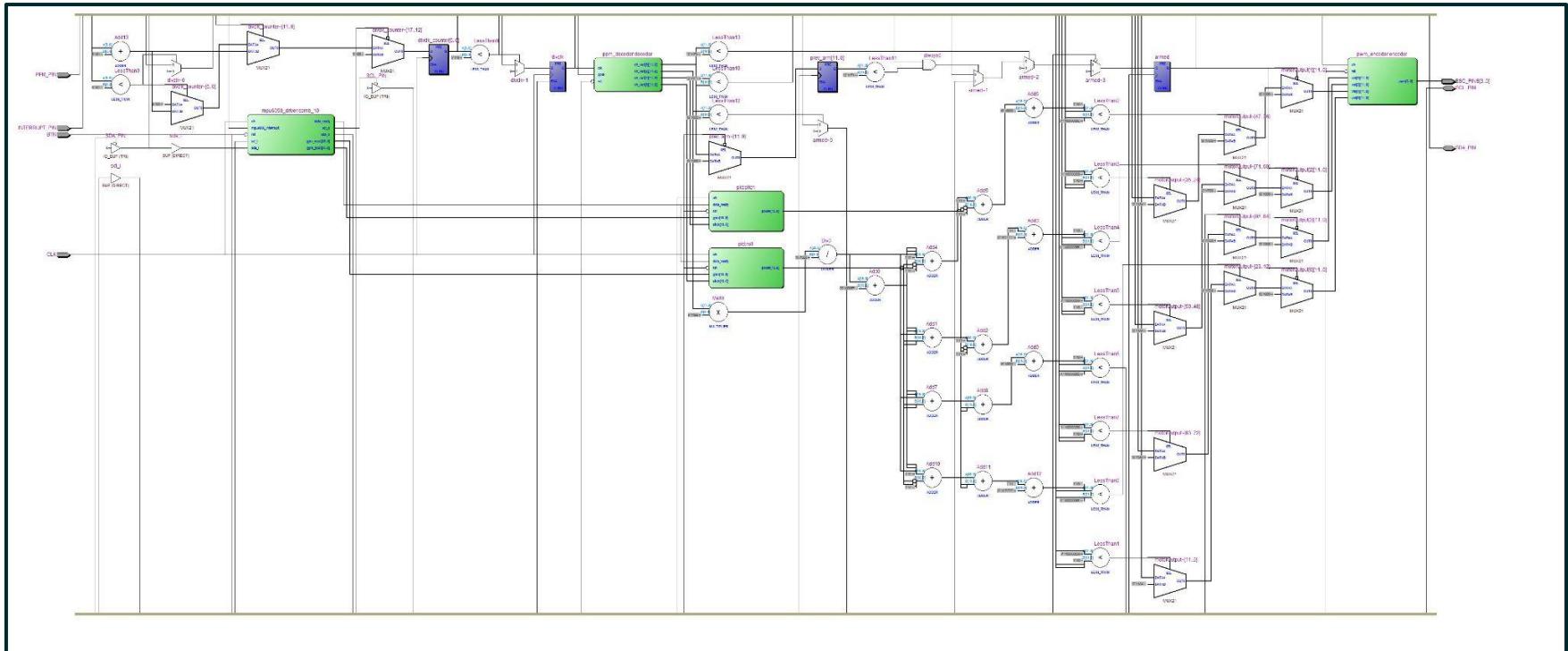


Figure 9. RTL Synthesis Block Diagram

# PHOTOS

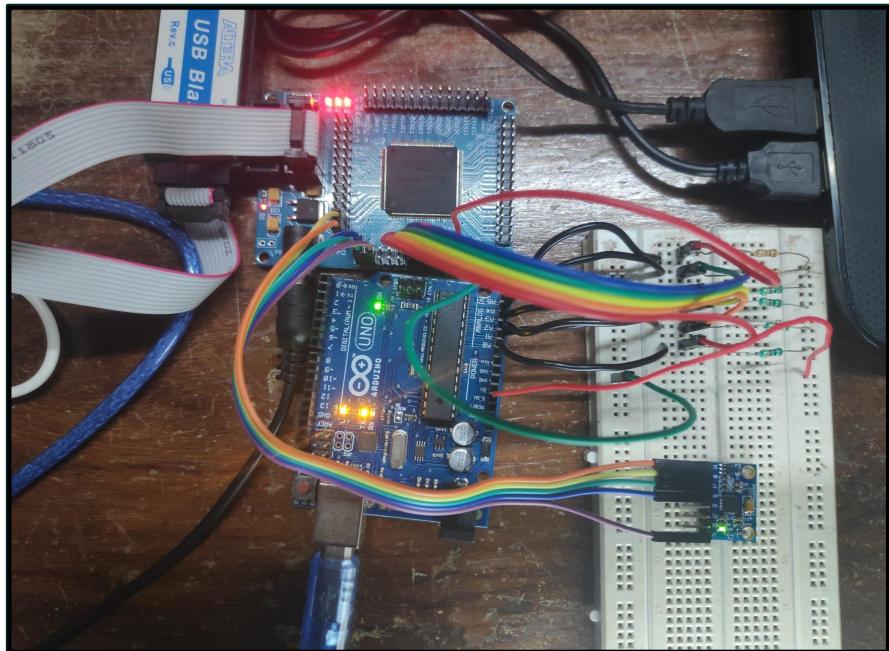


Figure 10. PPM from Arduino, Interfacing of MPU

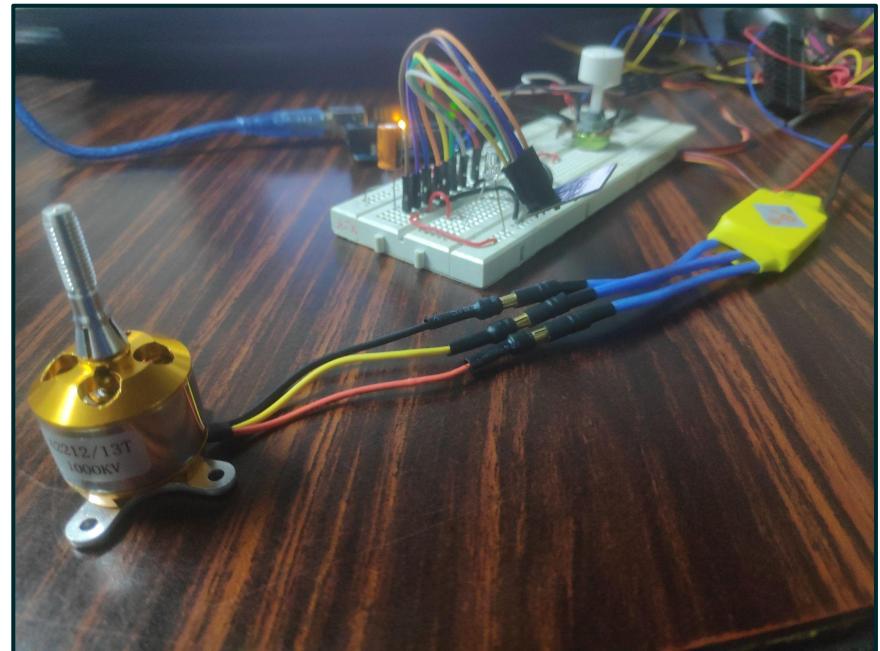


Figure 11. ESP-01 Programming and  
ESC/Motor testing

# PHOTOS

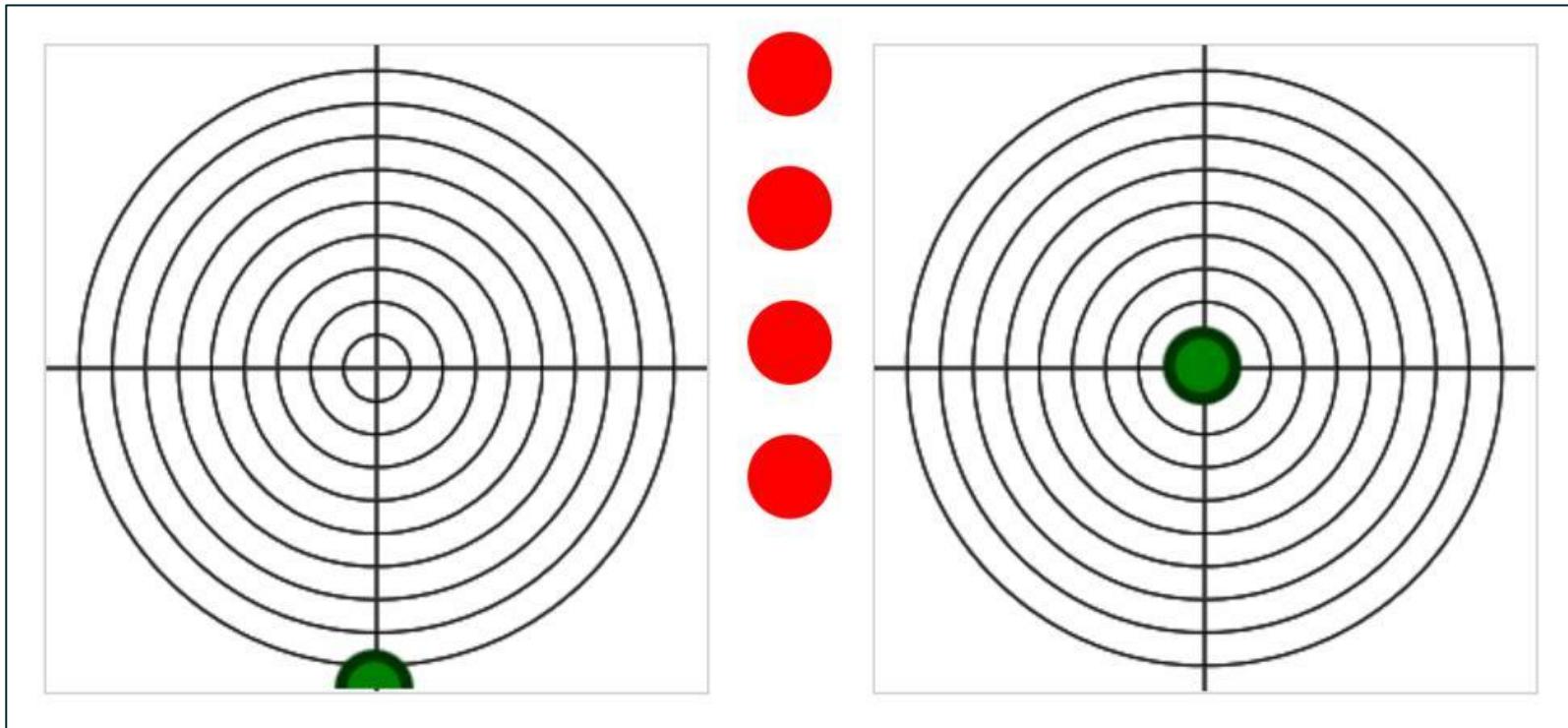


Figure 12. Wifi PPM Controls

# PHOTOS

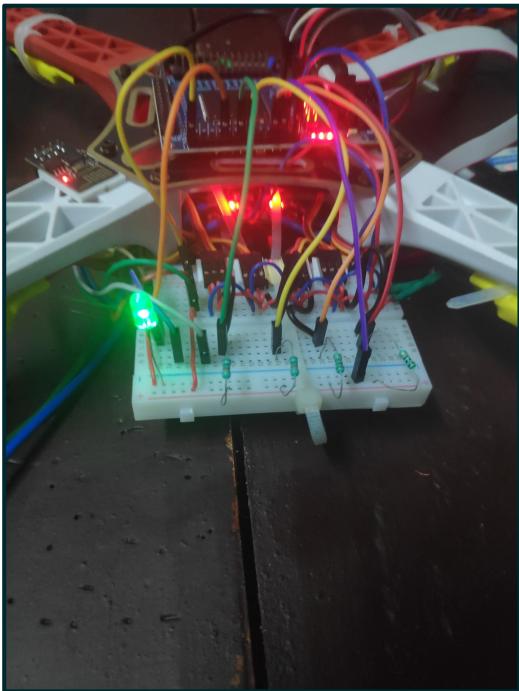


Figure 13. Drone Circuitry

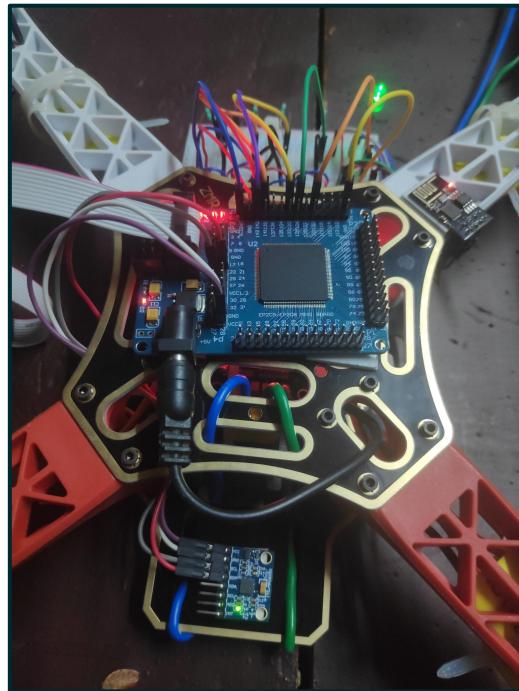


Figure 14. FPGA and MPU-6050 on Drone

# PHOTOS

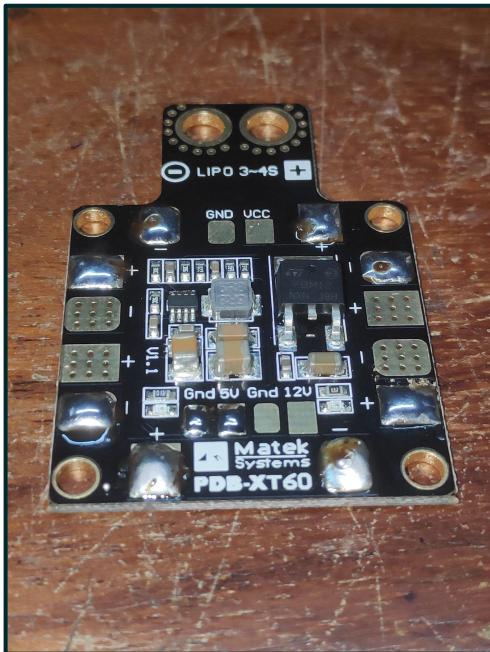


Figure 15. Power Distribution Board

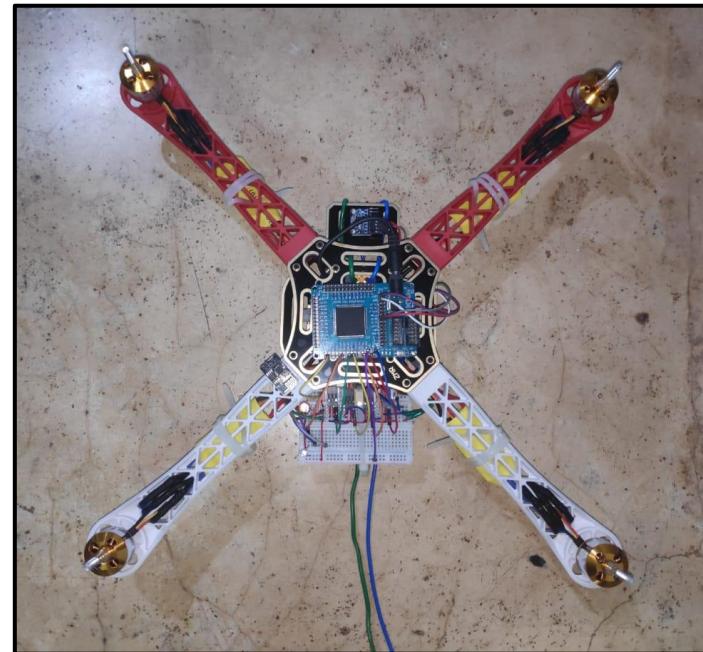


Figure 16. Drone Structure

# FPGA FC on Drone

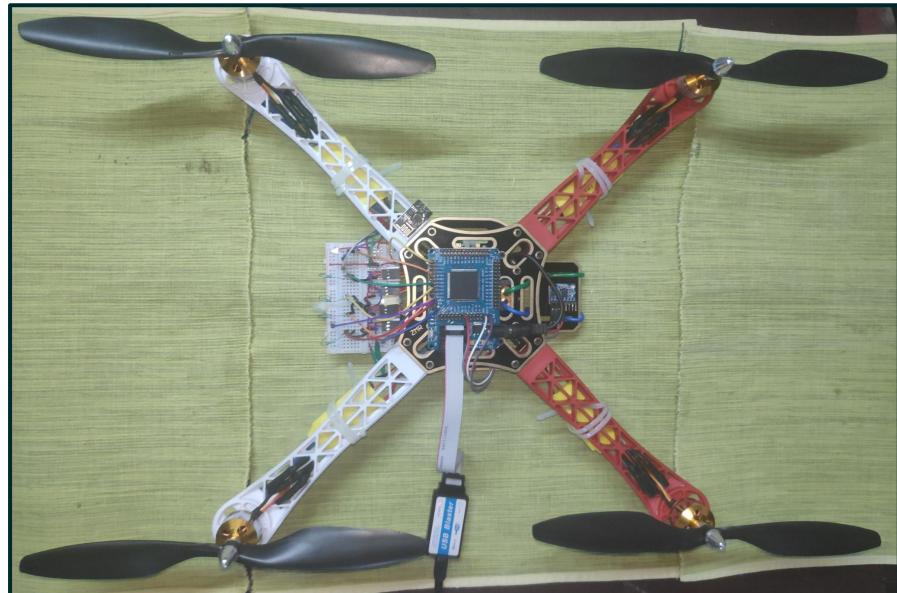


Figure 17. Top View

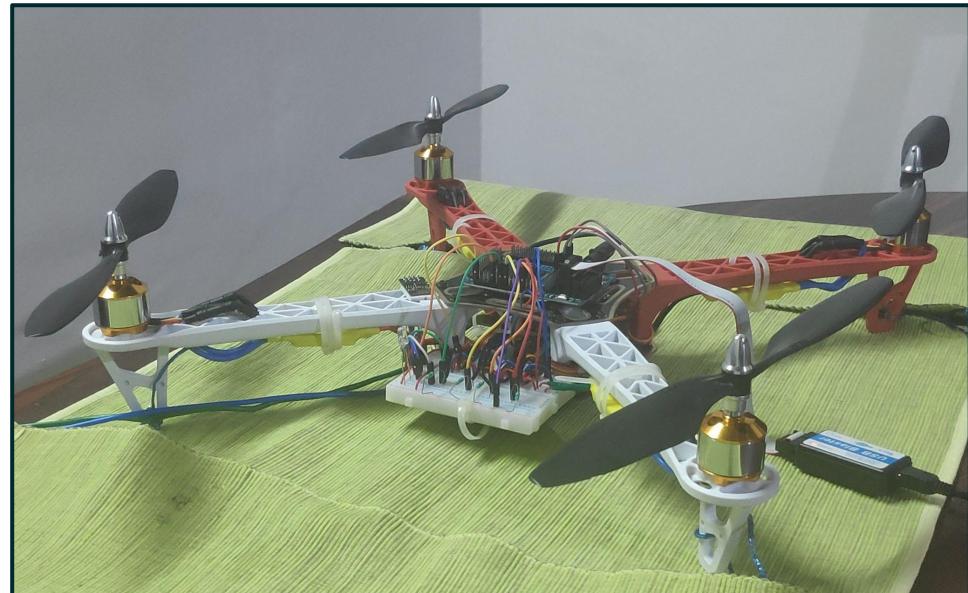
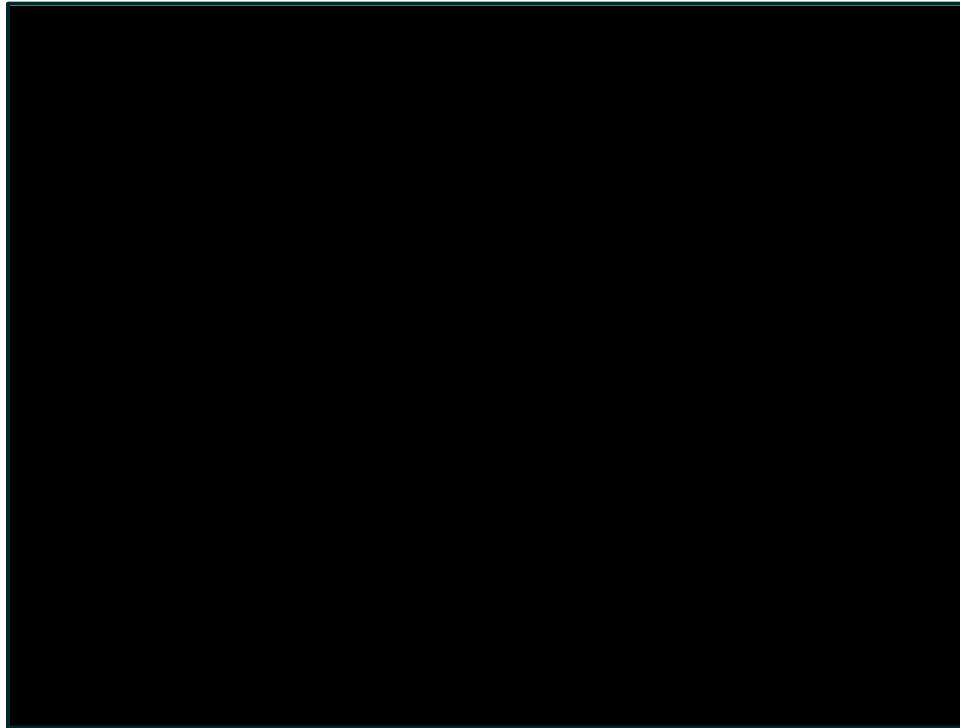


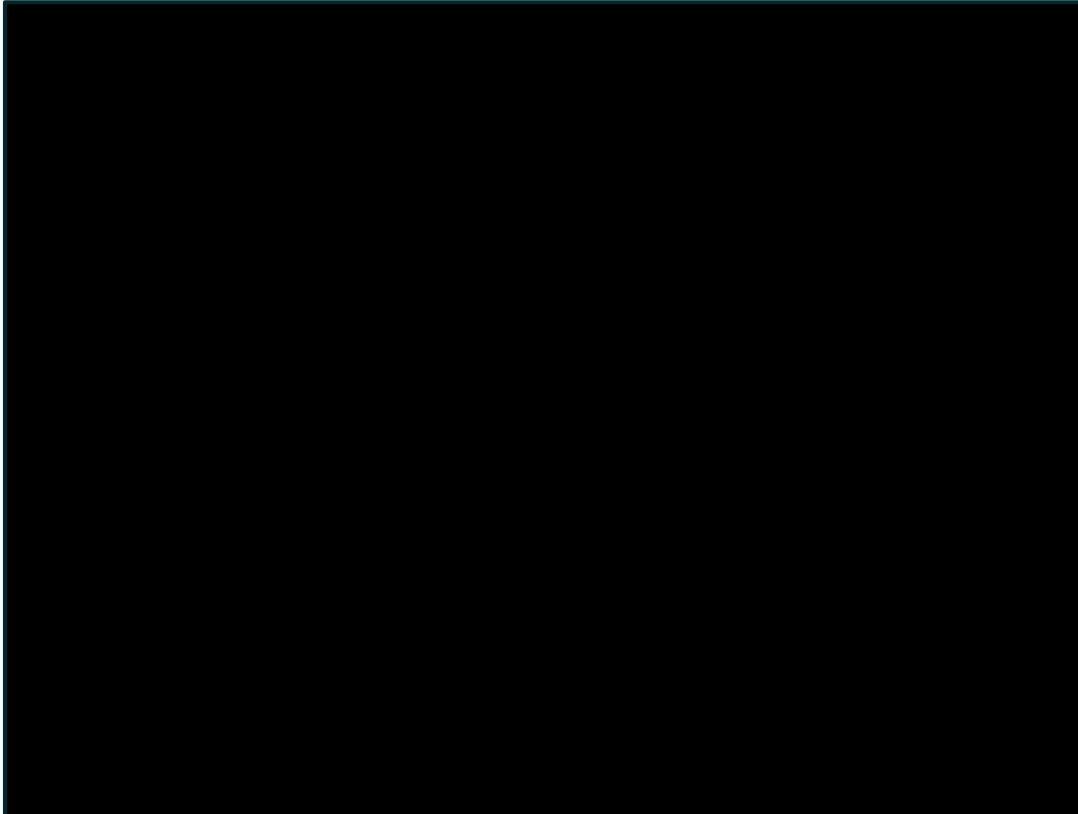
Figure 18. Side View

# VIDEOS



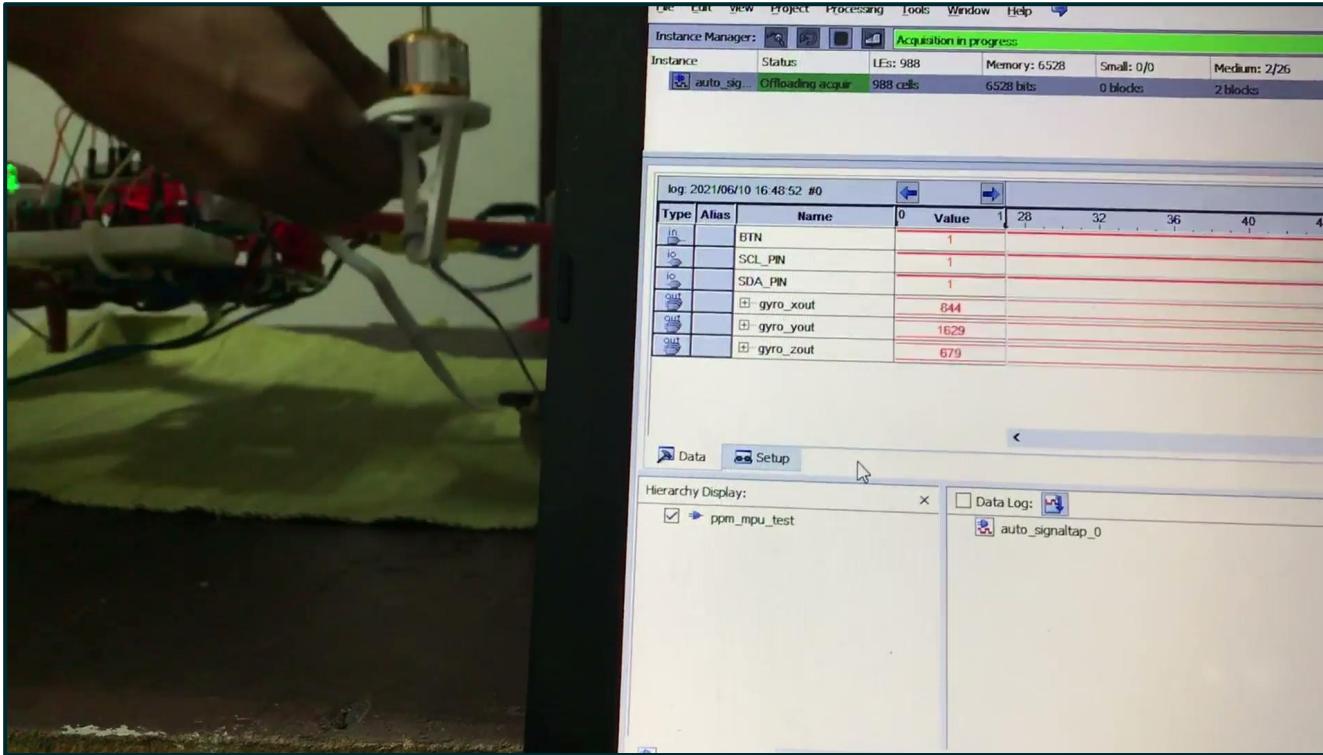
Video 1. Servo Motor response to RC

# VIDEOS



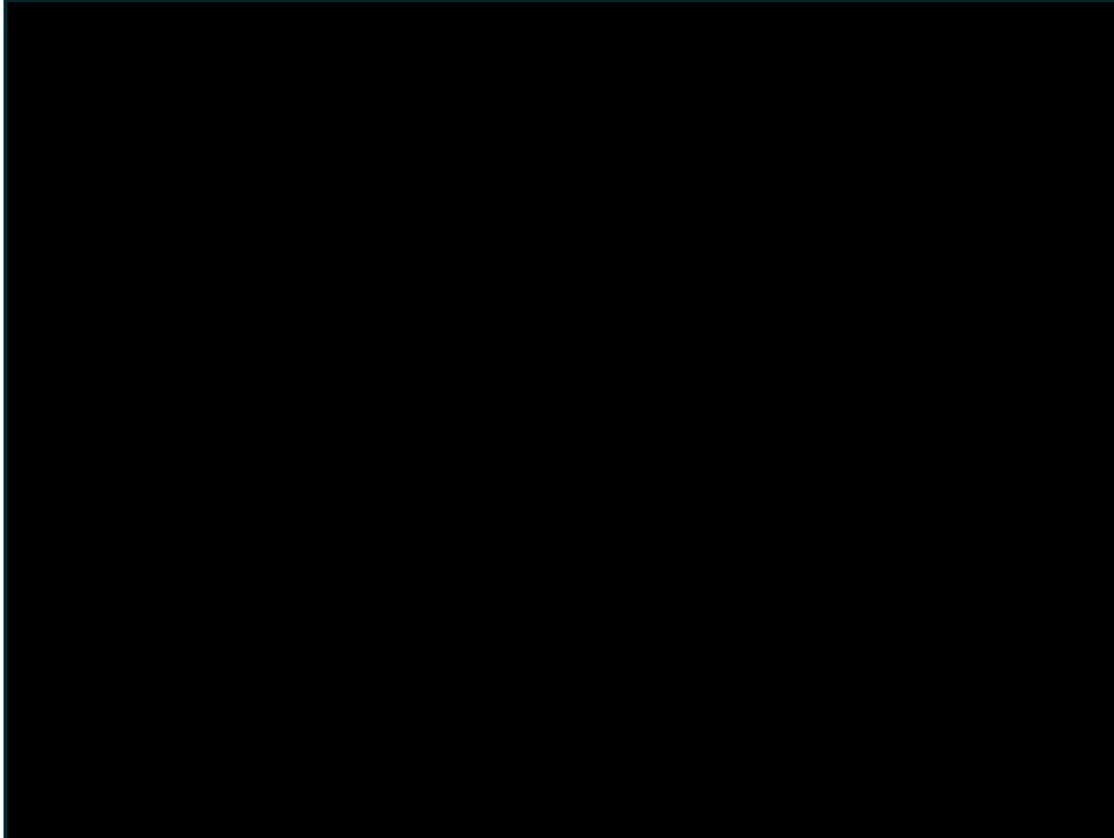
Video 2. PPM Decoding

# VIDEOS



Video 3. MPU-6050 Gyroscope Interface

# VIDEOS



Video 4. PWM Encoding with PPM signal

# VIDEOS



Video 5. PID tuning

# VIDEOS



Video 6. FPGA FC Drone in flight

# LEVEL OF COMPLETION

Objectives	Novelty	Results Obtained	Level Of Completion (%)
PPM Decoder	FSM approach	PPM decoded	100
MPU Driver		Data transmitted	100
I2C Protocol		Data transferred	100
PID	Nil	Tuned parameters	In progress
PWM Encoder		PWM encoded	100
FPGA as FC	Low cost	Stable Drone	In progress

Table 7. Level of Completion

# STATUS OF PAPER PRESENTATION

- A. J. Kurian, M. L. Rao, O. B. Shafi and S. James, “FPGA based Flight Controller,” in 2021 International Conference on Emerging Trends in Signals, Systems & Information (ICETSSI), 2021.
  - Hosted by Nehru College of Engineering and Research Centre (NAAC Accredited, Approved by AICTE, Affiliated to APJ Abdul Kalam Technological University, Kerala).
  - Conference Proceedings Reference number not ready.

# CERTIFICATES



## Future Scope

- Integration of more sensors like barometer, ultrasonic to improve stability.
- Conversion to a minimum viable product (MVP).
- Implementation of the project in VHDL / Verilog as well, apart from SystemVerilog, to portray the benefits.
- Implement Fuzzy based controller to improve response.

# CONCLUSION

- All the functionalities of the proposed logic:
  - The logics of PPM decoding
  - MPU interface via I2C
  - PWM encoding making use of motor mixing algorithms

were successfully implemented on a Cyclone II FPGA development board by making use of **parallelism** and is sufficient for a flight controller to **provide stability** to a quadcopter.

- Demonstrated that it is possible to implement the proposed functionality on a **low cost FPGA with lesser number of logic elements** like Cyclone II FPGA development board, hence can be made into a Minimum Viable Product.
- Total **utilization is just 81%** of the logic elements.

# REFERENCES

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- [3] Gadde, Premkumar & Rajmohan, Jayalakshmi. (2018). "Design and Implementation of FPGA Based Quadcopter", International Journal of Engineering Technology Science and Research, ISSN 2394 – 3386., 2018, Volume 5, Issue 3.
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- [8] S James, "fpga-flight-controller," <https://github.com/SebastianJames55/fpga-flightcontroller>, last accessed on 9 June, 2021.
- [9] N. Monterrosa, J. Montoya, F. Jarquín and C. Bran, "Design, development and implementation of a UAV flight controller based on a state machine approach using a FPGA embedded system," 2016 IEEE/AIAA 35th Digital Avionics Systems Conference (DASC), Sacramento, CA, 2016, pp. 1-8, doi: 10.1109/DASC.2016.7778069.

# Thank You!