FPGA-BASED FLIGHT CONTROLLER

Project Guide
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Group 8
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Sebastian James (55)

CONTENTS

INTRODUCTION

AIM

- **Main idea**: To design a flight controller (FC) system on an FPGA board using **Verilog** to program the FPGA.
  - **Further extension**: implement machine learning for stability.
  - To deploy the code in **Xilinx Virtex - 6** FPGA development board to tune the flight parameters to achieve stable flight using a radio transmitter/similar manual input.
  - To convert this project into a product.

INTRODUCTION

SCOPE & RELEVANCE

- Can be used for UAV flight stability.
- Faster response of flight controller - parallel processing capability of FPGA.
- From entertainment to military purposes, drones are used in various applications and the scope of drone technology is limitless.
- Lots of scope for FPGA-based flight controllers considering the innumerable application of the drones.

LITERATURE REVIEW

SL NO	YEAR	TITLE & SOURCE	OBJECTIVES	METHODOLOGY	RESULT	LIMITATIONS
1	2016	**TITLE** Design, development and implementation of a UAV flight controller based on a state machine approach using a FPGA embedded system. **SOURCE** DASC	Fast Real time processing of inputs Sensor Interfacing With FPGA Combining Various Sensor inputs	Parallel processing and having large numbers of gates on a single chip And also provides a cost saving platform. Sensors measure the air vehicle's altitude and other functions and compare it to the desired states and the error signal is eliminated	Parallel Processing	Noise From Sensors Affect stability

LITERATURE REVIEW

SL NO	YEAR	TITLE & SOURCE	OBJECTIVES	METHODOLOGY	RESULT	LIMITATIONS
2	2016	**TITLE** An analytical review on FPGA based autonomous flight control system for small UAVs **SOURCE** ICEEOT	To smoothen out MPU 6050 Output using filters. To generate PWM motor Signals corresponding to roll and pitch from the sensors	Kalman Filter and PID Controller offers short transition, good stability, anti-disturbance, good control and fulfills the requirement of real-time and accurate control. FCS The goal of the FCS is to help the user with automatic compensation in all the maneuvers of the aircraft in case of any disturbance.	Timing and Control of FPGA input signals from sensors. Synchronization of signals. Generation of output PWM signals for controlling the motors	PID - limited stability

LITERATURE REVIEW

SL NO	YEAR	TITLE & SOURCE	OBJECTIVES	METHODOLOGY	RESULT	LIMITATIONS
3	2018	**TITLE** Design and Implementation of FPGA Based Quadcopter **SOURCE** IJETSR	PWM encoder/decoder Design Study Basic Block diagram of the FC Mapping unit to produce output for motors from roll,pitch,yaw,throttle	FPGA Block Diagram PWM encoder PWM signal generator PWM decoder Mapping unit	Relation between the Motor output, Throttle Roll, pitch and yaw required.	No PPM encoder/decoder is implemented.

MOTIVATION & OBJECTIVES

- UAVs have become very popular in recent years and can be used for several applications.
- A flight controller is the core of any UAV and its feasibility depends on the efficiency of the flight controller.
- The motive is to build a well effective and efficient flight controller system.

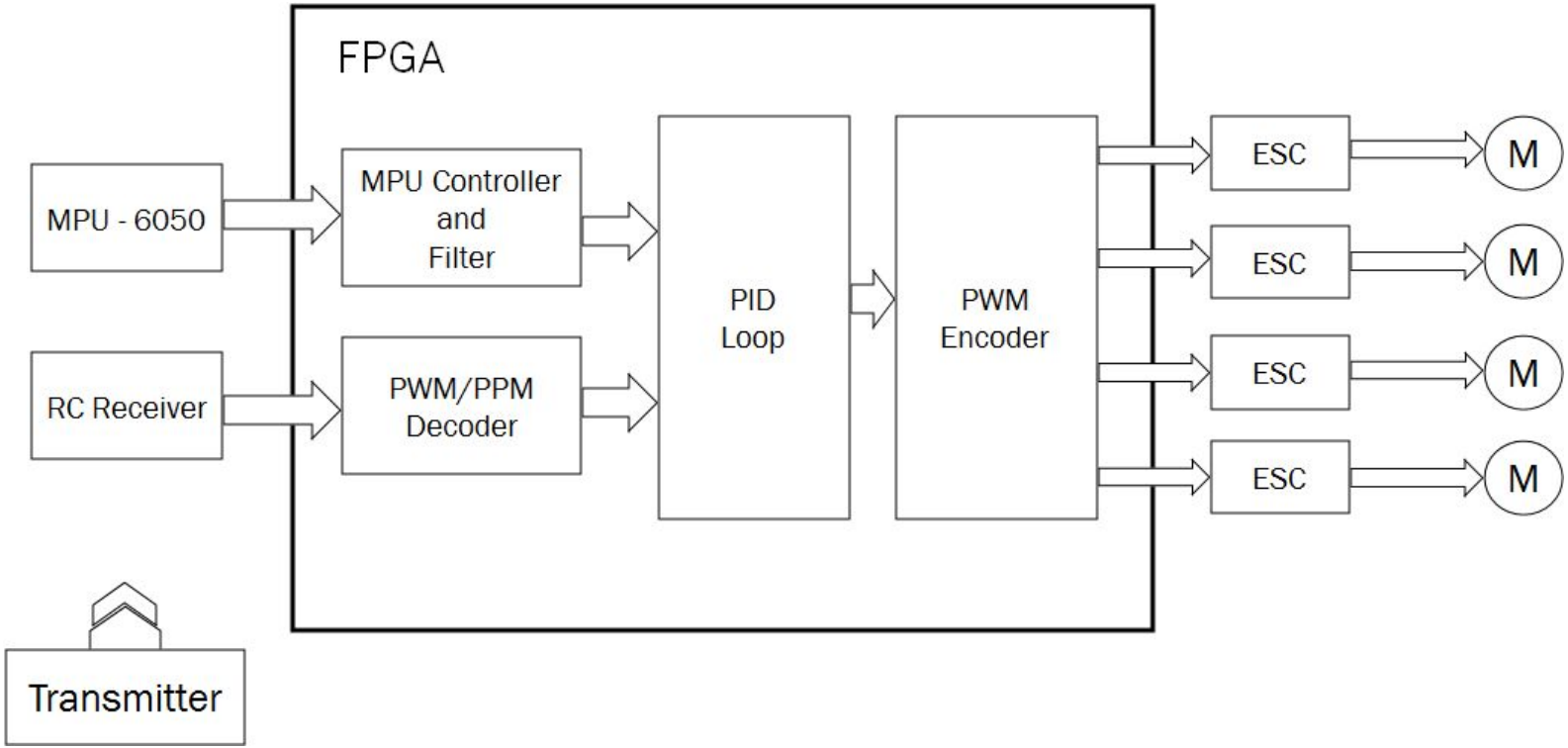
The main objectives are:

- Testing and interfacing MPU-6050 (I2C) with FPGA board.
- Implementing PID loop and PWM encoder in the FPGA.
- Direct the input of ESC to control RPM of each motor in response to input into PID from MPU and RC transmitter

NOVELTY

- Different implementations other than PID
  - Kalman filter
  - Finite State Machine
  - Fuzzy based
- Convert to a minimum viable product (MVP).
- Integration of more sensors like barometer, ultrasonic to improve stability.
- Implementation of the project in VHDL / SystemVerilog as well, apart from Verilog, to portrait the benefits.

BLOCK DIAGRAM

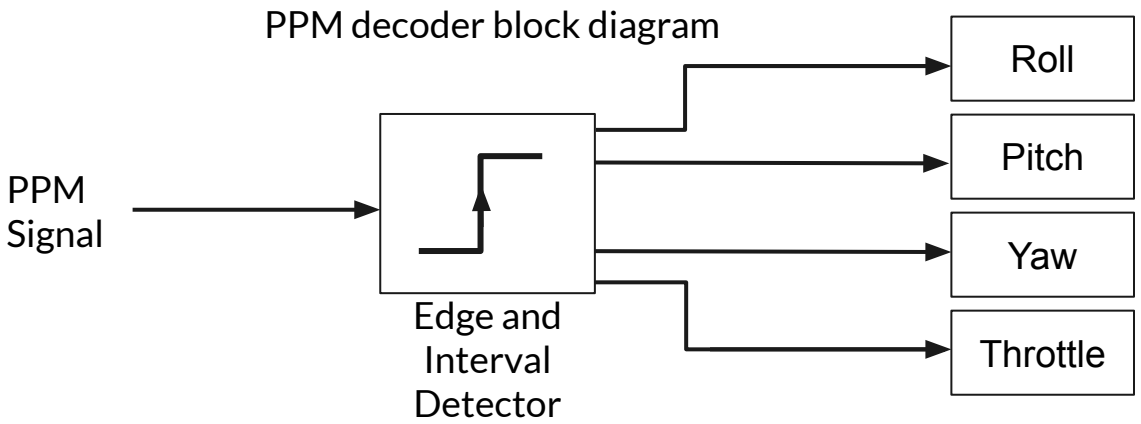


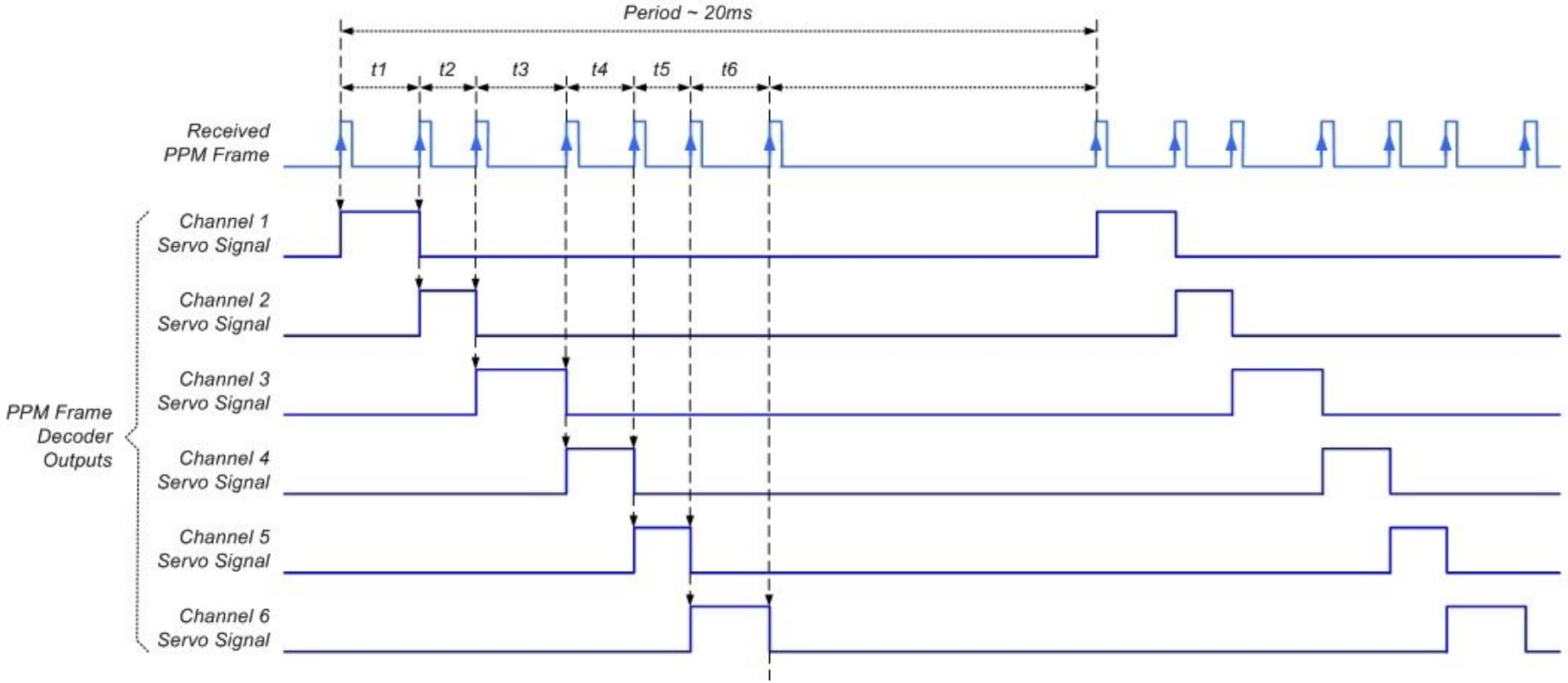
Flight Controller on FPGA

METHODOLOGY

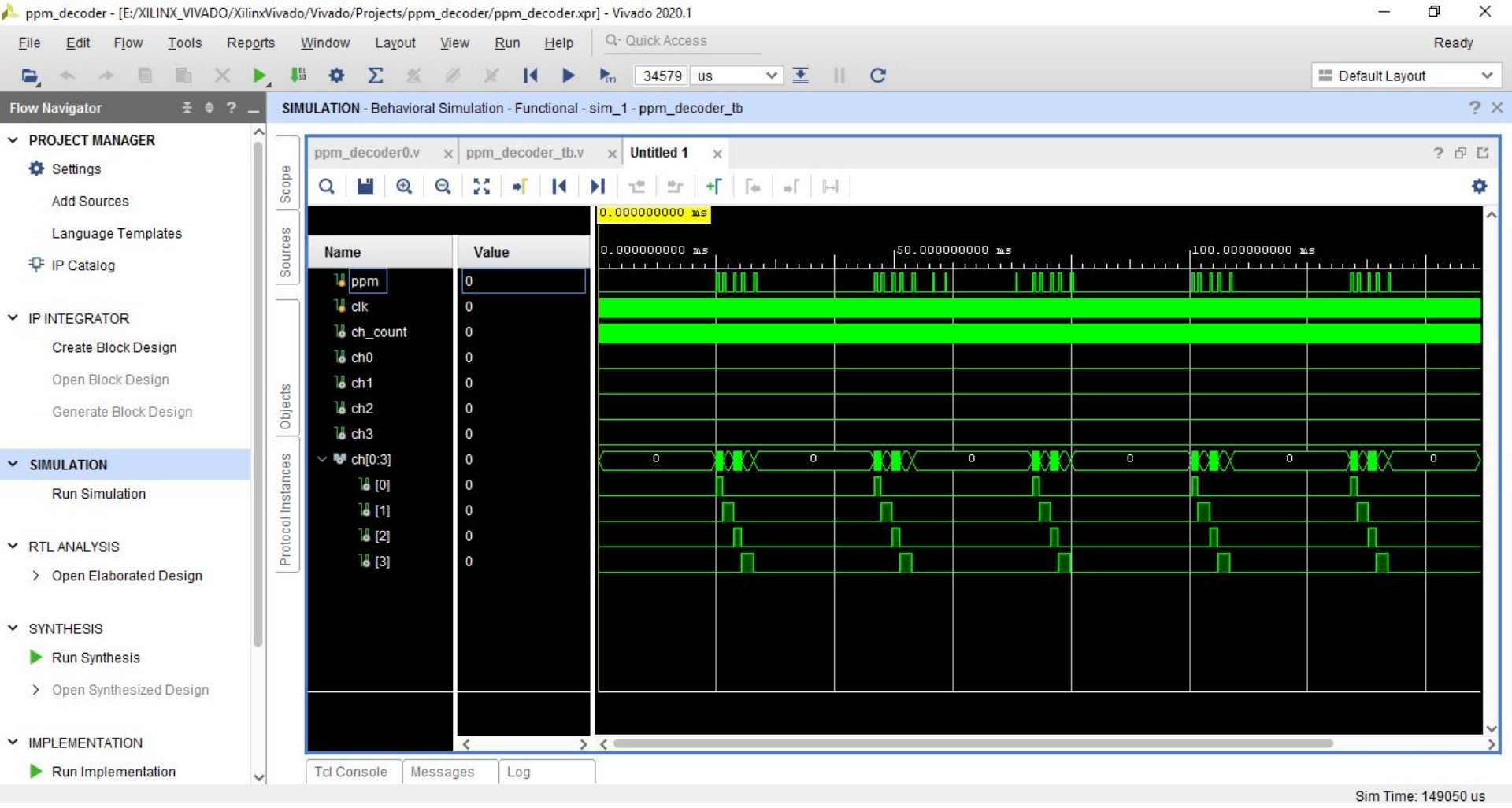
PPM DECODER

- Each pulse signifies each channel from the RC
- Time interval between each pulse is measured
- This is manipulated to the appropriate channels in the output





PPM decoder data flow



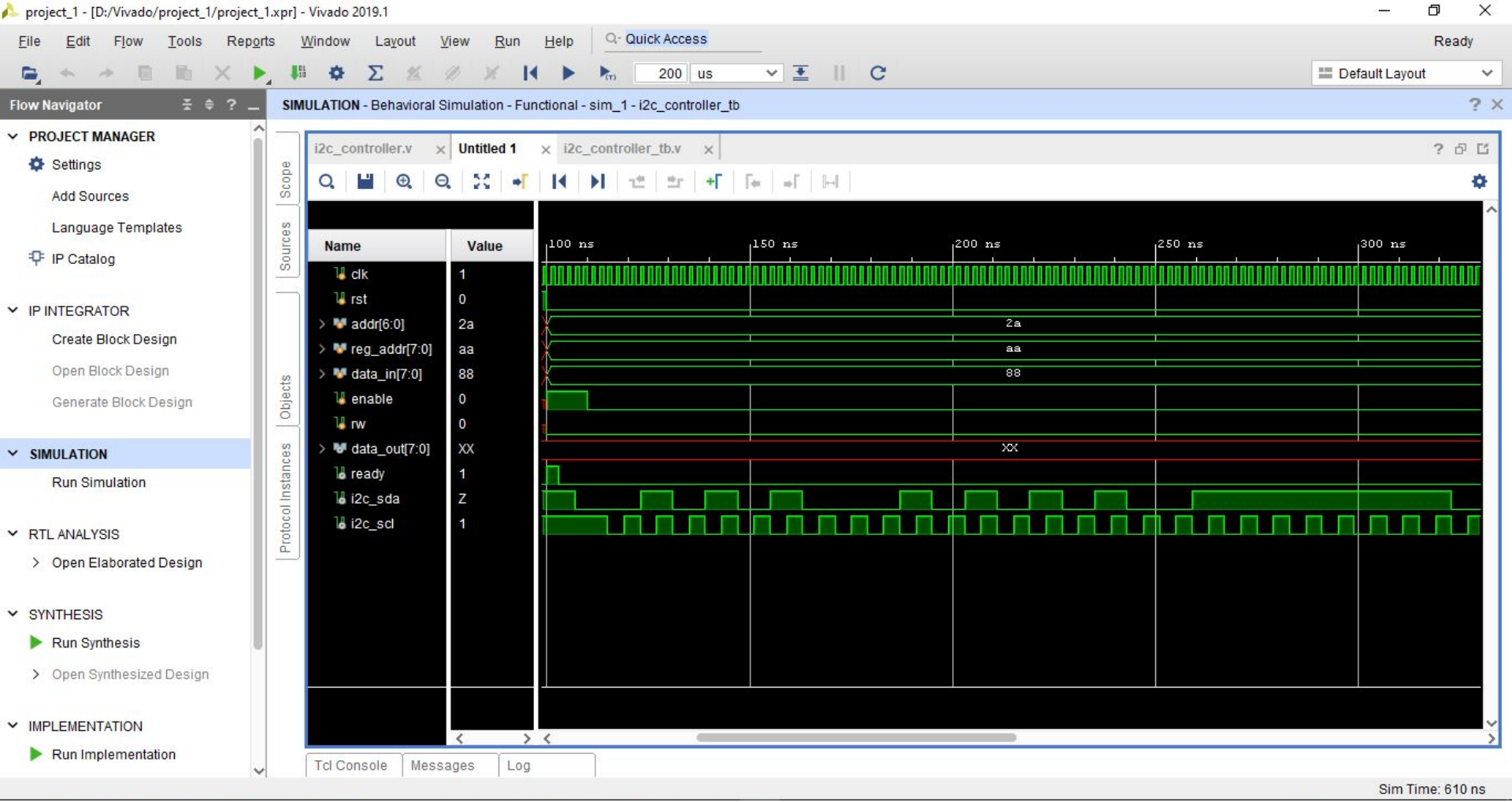
PPM Decoder Simulation

I2C COMMUNICATION

- I2C - master reading from slave using SDA and SCL pins

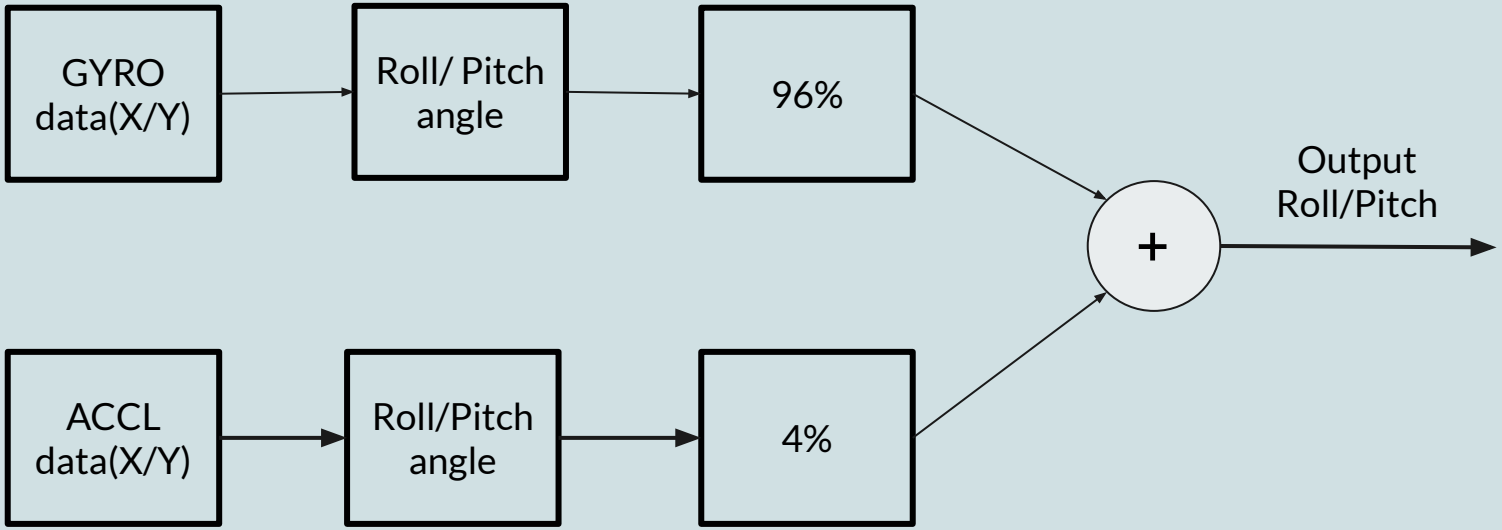
I2C data flow

- Filter design for gyro and accelero data from MPU-6050 [Complementary Filter]
  - The Gyro drifts off over the course of time not suitable for long term measurements.
  - Accelerometer is more susceptible to vibrations so values over short time are not suitable
  - A Combination of both filters are used.

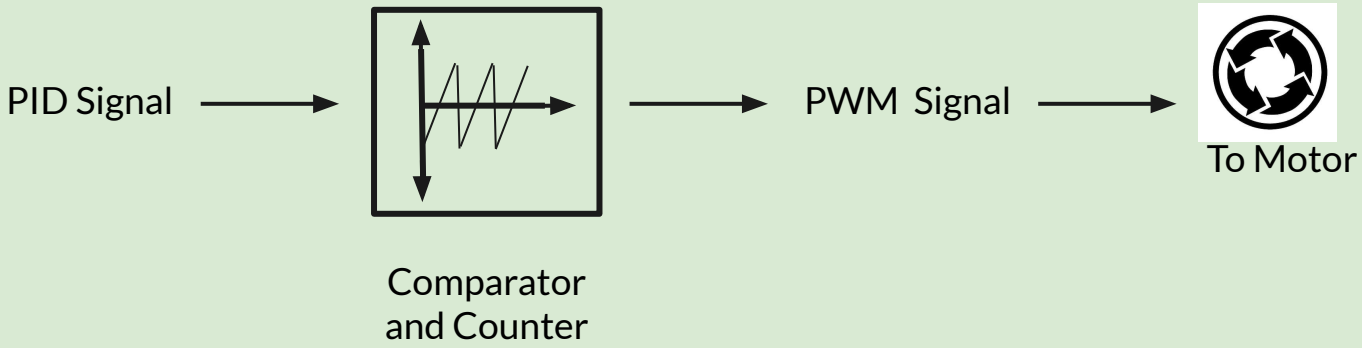


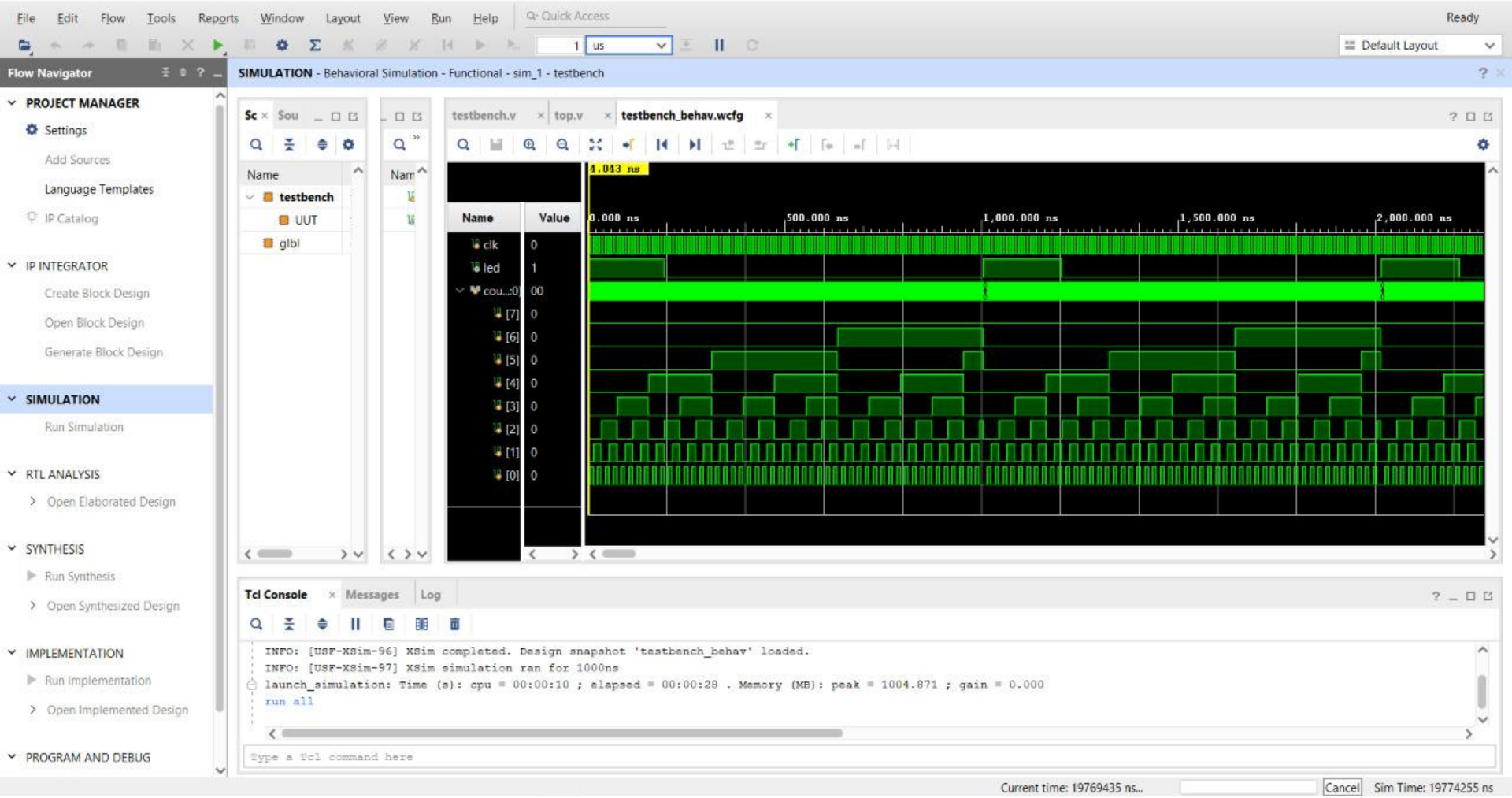
I2C Simulation

FILTER DATAFLOW



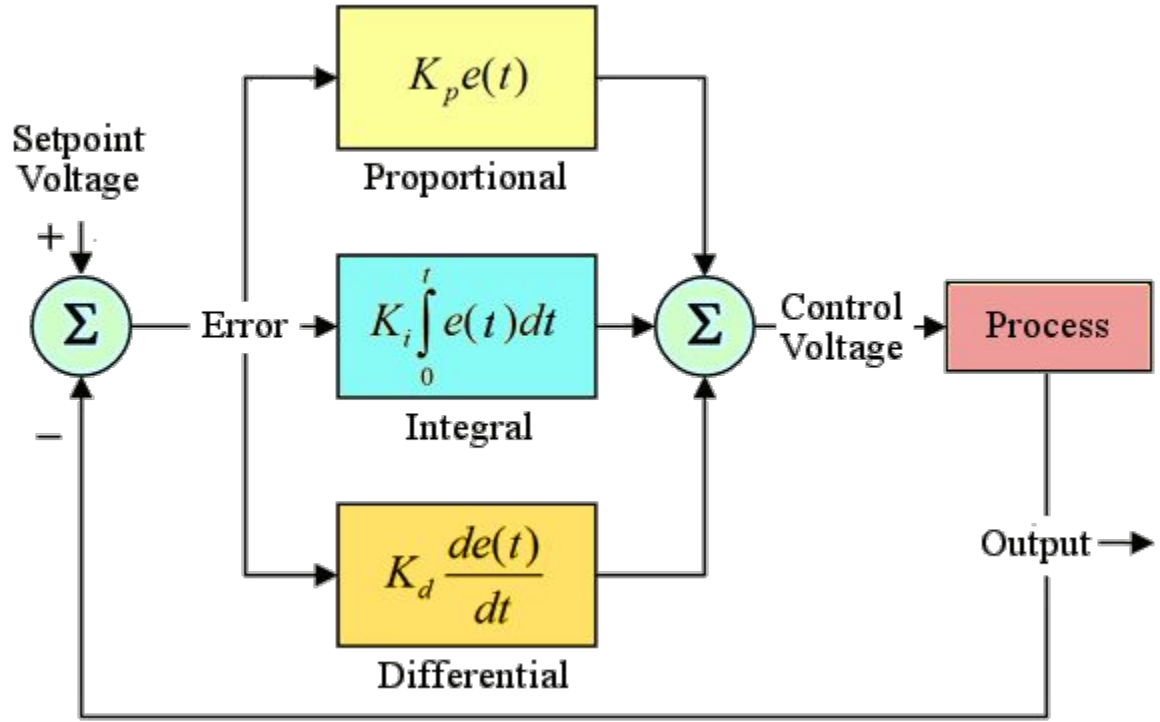
PWM DATAFLOW





PWM Encoder Simulation

PID CONTROLLER LOOP



Feasibility Study

Sl. No	Requirement in the project	Hardware/Software available			Hardware/Software selection		
		Name	Features relevant to the project	Cost (₹) / License	Name	Reason	Cost (₹)
1	FPGA Development board	Xilinx Virtex - 6	Performance, Scalability	20000	Virtex - 6	.Cost .Optimal	20000
		Xilinx Zynq 7000	SoC, High Scalability	80000			
		Altera Cyclone V	SoC	25000			
2	IMU	MPU-6050	6-axis IMU, I2C	100	MPU - 6050	.Optimal	100
		MPU-6500	6-axis IMU, DMP, I2C	200			
3	IDE	Xilinx Vivado	For Xilinx boards	Free	Xilinx Vivado	.Virtex - 6	Free
		Quartus Prime	For Altera boards	Free			

Feasibility Study

Sl. No	Requirement in the project	Hardware/Software available			Hardware/Software selection		
		Name	Features relevant to the project	Cost (₹) / License	Name	Reason	Cost (₹)
4	Language	VHDL	Non-C Syntax, HDL	-	Verilog	.Feasible	-
		Verilog	C Syntax, Compact, HDL	-			
		SystemVerilog	C++ Syntax, HDL, HVL	-			
5	Control System	PID	Basic control system	-	PID	.Viability	-
		ML	Complex	-			
6	Motor (4)	Coreless	Low cost, compact	500	BLDC	.Efficiency .Durability	2000
		BLDC	Efficiency, Large torque	2000			

Work Schedule

- Athul - Integrate PPM into PID
- Medha - Integrate PWM into PID
- Omar - Filter for MPU6050 and I2C protocol for MPU6050
- Sebastian - Implement Kalman filter
- Integrate the above into the PID together

Work Done and Schedule

PROJECT TITLE	FPGA FLIGHT CONTROLLER
PROJECT GUIDE	Mr. Jagadeesh Kumar P
GROUP MEMBERS	Athul John Kurian (AJK),Medha Lakshman Rao(MLR),Omar Bin Shafi(OBS),Sebastian James (SJ)
DATE	7th Jan 2021

SL. NUMBER	TASK TITLE	TASK OWNER	START DATE	DUE DATE	DURATION	PCT OF TASK COMPLETE
1	Project Conception and Initiation					
1.1	Topic Selection	OBS, AJK, SJ, MLR	30th July			100%
1.2	Literature Review	OBS, AJK, SJ	25th Aug			60%
1.3	Feasibility Study	MLR,OBS,SJ	3rd Nov			70%
1.4	Project Planning	OBS, AJK, SJ,MLR	12th Aug			90%
1.5	Project Initiation	OBS, AJK, MLR	14th Nov			45%
1.6	Scope & Goal Setting	SJ,AJK,MLR	1st Nov			85%
1.7	Budget	MLR, AJK	30th Nov			40%
1.8	Background study	SJ	7th Sept			65%
2	Work Schedule					
2.1	Software installations	OBS, MLR, AJK, SJ	24th Sept			100%
2.2	Getting to know the software	OBS, MLR, AJK, SJ	5th Oct			100%
2.3	PPM Decoder	AJK	30th Nov			80%
2.4	I2C Communication, filter	OBS, SJ	27th Oct			85%
2.5	PID Loop	OBS, AJK	28th Sept			
2.6	PWM Encoder	MLR	22th Nov			90%
2.7	Simulation	AJK, MLR, OBS		15th Mar		
2.8	Component Testing			10th Apr		
2. 10	Debugging			20th Apr		
2.11	Finalising the project	SJ, AJK				
2.12	Novelty	SJ, AJK	30th Nov			90%

Work done

- Athul
  - Familiarised with Vivado ISE; implemented gates, adders, clocks.
  - Learned basics of PID, learned PPM decoding.
  - Completed PPM decoding in Verilog, hardware implementation pending.
- Medha
  - Familiarised with Vivado ISE; implemented gates, adders.
  - Learned basics of PWM and implemented PWM encoding.
- Omar
  - Familiarised with Vivado ISE; implemented gates, adders, clocks.
  - Learned filter design, started to implement filter.
  - Implemented I2C protocol.
- Sebastian
  - Learned the basics of FPGA from Coursera; familiarized with Quartus Prime.
  - Read the reference papers; 5 chapters from 3 texts.
  - Learned I2C implementation in detail.

Conclusion

- Implement FC on FPGA
- PID to provide stability
- Integrate various sensors and Kalman filter to improve stability
- Incorporate ML/FSM
- Develop an MVP from the project

References

[1] N. Monterrosa, J. Montoya, F. Jarquín and C. Bran, "**Design, development and implementation of a UAV flight controller based on a state machine approach using a FPGA embedded system,**" 2016 IEEE/AIAA 35th Digital Avionics Systems Conference (DASC), Sacramento, CA, 2016, pp. 1-8, doi: 10.1109/DASC.2016.7778069.

[2] B. L. Sharma, N. Khatri and A. Sharma, "**An analytical review on FPGA based autonomous flight control system for small UAVs**," 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), Chennai, 2016, pp. 1369-1372, doi: 10.1109/ICEEOT.2016.7754907.

[3] Gadde, Premkumar & Rajmohan, Jayalakshmi. (2018). "**Design and Implementation of FPGA Based Quadcopter**", International Journal of Engineering Technology Science and Research, ISSN 2394 – 3386., 2018, Volume 5, Issue 3.

Thank You :)