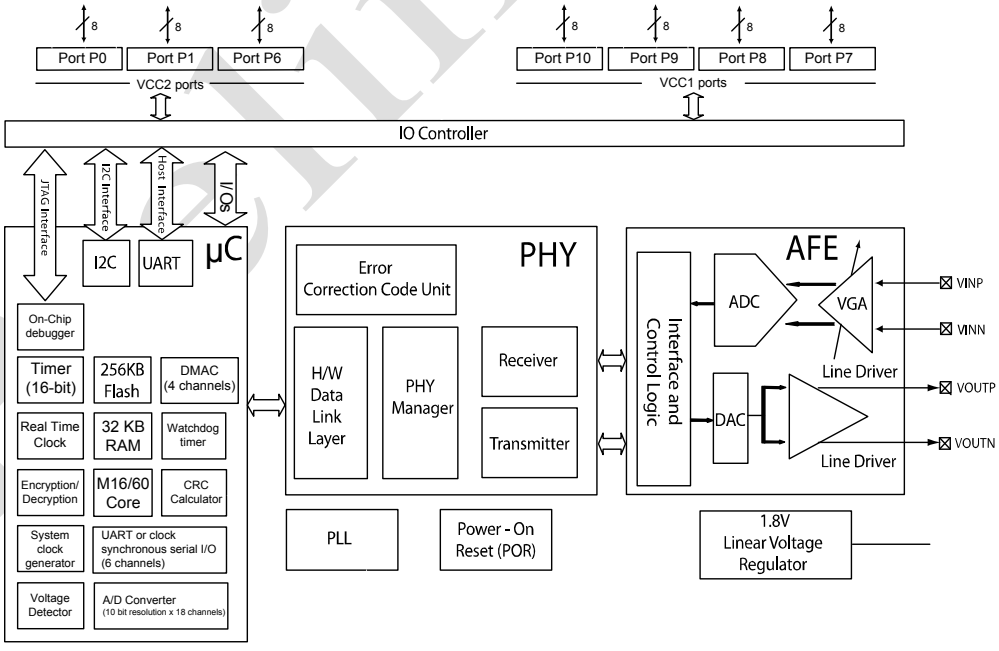
IT900 MAIN FEATURES

- Low-cost Powerline Communication (PLC) modem and application solution in a single chip
- Data rates up to 500 Kbps FCC and ARIB, 150 Kbps in CENELEC-A band
- HomePlug® Command and Control ready
- Transparent interface for IPv6, IPv4, 6lowpan; support for SE 2.0
- Implements DCSK and DCKS Turbo Modulation
- Incorporates Yitran's high performance Data Link Layer (DLL), Network Protocol (Y-Net) and extremely robust Physical Layer (PHY)
- M16C/60 microcontroller with 256KB Flash for protocol stack and application code.
- Chip Architecture options:
  - **Protocol Controller Architecture:** IT900 is accompanied by communication stack firmware
  - **Open Solution Architecture:** allows user to program application code together with the communication stack
- Full coverage even under adverse line conditions
- Fully backward compatible with IT700 and IT800 Series

APPLICATIONS

- Smart Grid Applications:
  - Automated Meter Reading (AMR)
  - Advanced Meter Management (AMM)
  - Demand Response & Real-Time pricing
- Smart Home & Energy Management:
  - Home & Building Automation
  - Home Appliance Control & Diagnostics
  - Security and Access Control
  - Environmental Control
- Commercial Applications:
  - Street Light Control
  - Vending Machine Control
  - Signage Control



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1 IT900 GENERAL DESCRIPTION

The IT900 is a highly integrated System-on-a-Chip (SoC) Powerline Communication (PLC) modem. It incorporates Yitran's extremely reliable Physical Layer (PHY), high-performance Data Link Layer (DLL) and Network (Y-Net) protocol.

An integrated microcontroller with M16C/60 core, 256KB Flash memory, 3KB RAM and 7 eight bit ports implement the protocol stack and offers the required flexibility to implement various protocols and applications. The microcontroller's UART interface provides the connection to an external Host and application controller. The I^2C interface connects an optional external EEPROM for stack parameter storage.

The IT900 PLC modem core uses Yitran's patented DCSK and DCSK Turbo implementing advanced coherent spread spectrum modulation techniques for high speed and extremely robust communication with data rates up to 500 Kbps FCC and ARIB, 150 Kbps in CENELEC-A band. In addition to the inherent interference immunity provided by DCSK modulation, DCSK Turbo utilizes several mechanisms for enhanced communication speed such as adaptive symbol overlapping and Decision Feedback Equalization.

The integrated Analog Frontend provides differential inputs and line driver outputs to connect via an external line filter and coupler to the power transmission lines. An integrated Phase Locked Loop Circuit allows the operation of the IT900 with a choice of different crystal oscillators. An integrated Power-On-Reset (POR) circuit eliminates the need for any external reset components and provides an autonomous, safe power-up and power-down reset to the chip. The integrated 1.8V voltage regulator allows the IT900 to operate from a single 3.3V supply.

The IT900 complies with worldwide regulations (FCC part 15, ARIB and CENELEC bands) and is an ideal solution for a variety of command and control PLC applications.

The IT900 is available in two versions:

> The **Protocol Controller Architecture** version is accompanied by Yitran's Y-Net network protocol firmware. A UART interface and simple command language provide seamless connection to an external Host controller and simplify application development. In this version, no access to the microcontroller's resources is provided.
>
> The **Open Solution Architecture** version allows utilization of the IT900 microcontroller's peripheral functions such as timers, interrupts, communication interfaces, A/D, spare memory resources and general-purpose I/Os to implement the application code, thereby eliminating the requirement for an external host controller. An Application Programming Interface (API) enables easy integration of the application code with Yitran's code.

This Datasheet covers the Protocol Controller Architecture version only.
Material related to Open Solution Architecture version is documented separately

2 PIN DIAGRAM AND PIN DESCRIPTION

2.1 PIN DIAGRAM

The following figure shows the IT900 HTQFP100 lead-free package pinout:

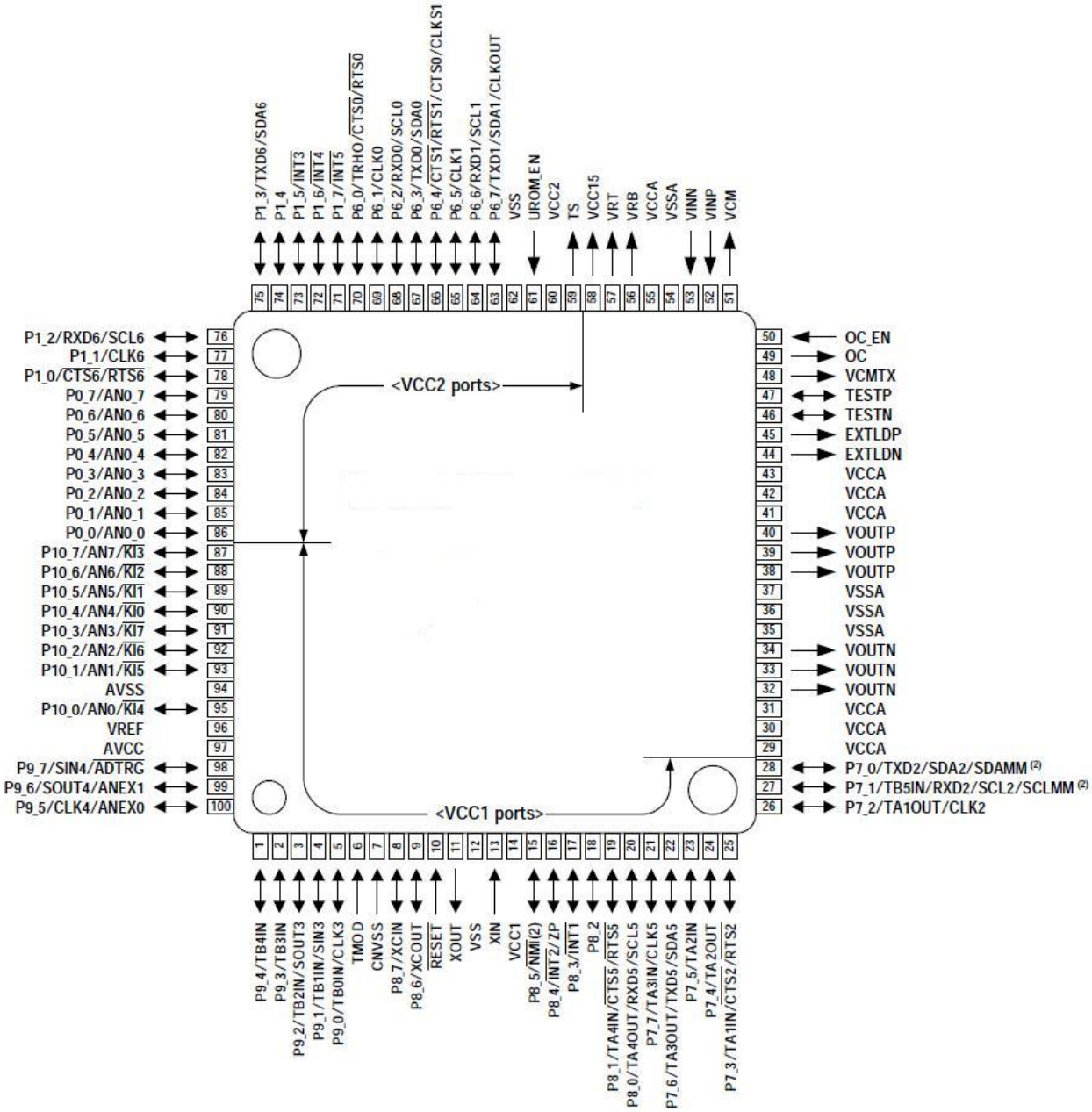


Figure 2: IT900 HTQFP100 Package Pinout

2.2 PIN DESCRIPTION

The functionality of the IT900 pins is described in Table 2.1, Table 2.2 and Table 2.3

Table 2.1: IT900 Pin Names

Pin No.	Power	Clock	Control Pin	Port	I/O Pin for Peripheral Function				
					Interrupt	Timer	Serial Interface	PLC	ADC
1				P9_4		TB4IN			
2				P9_3		TB3IN			
3				P9_2		TB2IN	SOUT3		
4				P9_1		TB1IN	SIN3		
5				P9_0		TB0IN	CLK3		
6			TMOD						
7			CNVSS						
8		XCIN		P8_7					
9		XCOUT		P8_6					
10			RESET						
11		XOUT							
12	VSS								
13		XIN							
14	VCC1								
15				P8_5	NMI				
16				P8_4	INT2	ZP			
17				P8_3	INT1				
18				P8_2					
19				P8_1		TA4IN	CTS5/RTS5		
20				P8_0		TA4OUT	RXD5/SCL5		
21				P7_7		TA3IN	CLK5		
22				P7_6		TA3OUT	TXD5/SDA5		
23				P7_5		TA2IN			
24				P7_4		TA2OUT			
25				P7_3		TA1IN	CTS2/RTS2		
26				P7_2		TA1OUT	CLK2		
27				P7_1		TB5IN	RXD2/SCL2SCLMM		
28				P7_0			TXD2/SDA2/SDAMM		
29	VCCA								
30	VCCA								
31	VCCA								
32								VOUTN	
33								VOUTN	
34								VOUTN	
35	VSSA								
36	VSSA								
37	VSSA								
38								VOUTP	
39								VOUTP	
40								VOUTP	
41	VCCA								
42	VCCA								
43	VCCA								
44								EXTLDN	
45								EXTLDP	
46								TESTN	
47								TESTP	

Pin No.	Power	Clock	Control Pin	Port	I/O Pin for Peripheral Function				
					Interrupt	Timer	Serial Interface	PLC	ADC
48								VCMTX	
49								OC	
50								OC_EN	
51								VCM	
52								VINN	
53									
54	VSSA								
55	VCCA								
56								VRB	
57								VRT	
58								VCC15	
59								TS	
60	VCC2								
61			UROM_EN						
62	VSS								
63		CLKOUT		P6_7			TXD1/SDA1		
64				P6_6			RXD1/SCL1		
65				P6_5			CLK1		
66				P6_4			CTS1/RTS1/CTS0/CLKS1		
67				P6_3			TXD0/SDA0		
68				P6_2			RXD0/SCL0		
69				P6_1			CLK0		
70				P6_0		TRHO	CTS0/RTS0		
71				P1_7	INT5				
72				P1_6	INT4				
73				P1_5	INT3				
74				P1_4					
75				P1_3			TXD6/SDA6		
76				P1_2			RXD6/SCL6		
77				P1_1			CLK6		
78				P1_0			CTS6/RTS6		
79				P0_7					AN0_7
80				P0_6					AN0_6
81				P0_5					AN0_5
82				P0_4					AN0_4
83				P0_3					AN0_3
84				P0_2					AN0_2
85				P0_1					AN0_1
86				P0_0					AN0_0
87				P10_7	KI3				AN7
88				P10_6	KI2				AN6
89				P10_5	KI1				AN5
90				P10_4	KI0				AN4
91				P10_3	KI7				AN3
92				P10_2	KI6				AN2
93				P10_1	KI5				AN1
94	AVSS								
95				P10_0	KI4				AN0
96									VREF
97	AVCC								
98				P9_7			SIN4		ADTRG
99				P9_6			SOUT4		ANEX1
100				P9_5			CLK4		ANEX0

Table 2.2 Pin Functions

Pin Numbers	Signal Name	Pin Name	I/O	Power Supply	Description
14, 60, 62	Digital power supply input	VCC1, VCC2, VSS	I	-	Apply 2.7 V to 3.6 V to pins VCC1 and NCC2, and 0 V to the VSS pin under the condition VCC1 = VCC2
97, 94	MCU ADC power supply input	AVCC, AVSS	I	VCC1	Power supply input for A/D converter. Connect AVCC pin to VCC1 and the AVSS pin to VSS.
29-31, 41-43, 35-37	PLC analog power supply input	VCCA, VSSA	I	-	Power supply input for AFE. Connect VCCA pin to VCC1 and VSSA pin to VSS.
10	Reset input	RESET	I	VCC1	Driving this pin Low resets the MCU.
7, 6	Mode setting input	CNVSS, TMOD	I	VCC1	Pins to set an operating mode. Connect both CNVSS and TMOD pins to VSS via resistors.
61		UROM_EN	I	VCC2	Connect to VSS via a resistor.
13	Main clock input	XIN	I	VCC1	I/O for the main clock oscillation circuit. Connect crystal oscillator between pins XIN and XOUT.
11	Main clock output	XOUT	O	VCC1	
8	Sub clock input	XCIN	I	VCC1	I/O for the sub clock oscillation circuit. Connect crystal oscillator between pins XCIN and XOUT.
9	Sub clock output	XCOUT	O	VCC1	
63	Clock output	CLKOUT	O	VCC2	This pin outputs the clock having the same frequency as fC, f1, f8 or f32.
17, 16 71-73	INT interrupt input	INT1, INT2	I	VCC1	Input for the INT interrupt.
		INT3 to INT5	I	VCC2	
15	NMI interrupt input	NMI	I	VCC1	Input for the NMI interrupt.
87-93, 95	Key input interrupt input	KI0 to KI7	I	VCC1	Input for the key input interrupt.
26, 24, 22, 20 25, 23, 21, 19 16	Timer A	TA1OUT to TA4OUT	I/O	VCC1	I/O for timers A1 to A4.
		TA1IN to TA4IN	I	VCC1	Input for timers A1 to A4.
		ZP	I	VCC1	Input for Z-phase.
1-5, 27	Timer B	TB0IN to TB5INT	I	VCC1	Input for timers B0 to B5.
70	Real-time clock output	TRHO	O	VCC2	Output for the real-time clock.
25, 19 66, 78	Serial interface UART0 to UART2, UART5 to UART 6	CTS2, CTS5	I	VCC1	Input to control data transmission
		CTS0, CTS1, CTS6	I	VCC2	
25, 19 70, 66, 78		RTS2, RTS5	O	VCC1	Output to control data reception.
		RTS0, RTS1, RTS6	O	VCC2	
26, 21 69, 65, 77		CLK2, CLK5	I/O	VCC1	Transmit/receive clock I/O.
		CLK0, CLK1, CLK6	I/O	VCC2	
27, 20 68, 64, 76		RXD2, RXD5	I	VCC1	Serial data input.
		RXD0, RXD1, RXD6	I	VCC2	
28, 22 67, 63, 75		TXD2*, TXD5	O	VCC1	Serial data output.
66		TXD0, TXD1, TXD6	O	VCC2	
		CLKS1	O	VCC1	Output for transmit/receive clock multiple-pin output function.
28, 22	UART0 to UART2,	SDA2†, SDA5	I/O	VCC1	Serial data I/O for I²C mode.

* TXD2 is an N-channel open drain output pin. TXDi (i=0, 1, 5, 6) can be selected as a CMOS output pin or N-channel open drain output pin by a program.

Pin Numbers	Signal Name	Pin Name	I/O	Power Supply	Description
67, 63, 75 27, 20 68, 64, 76	UART5, UART6 I²C mode	SDA0, SDA1, SDA6	I/O	VCC2	
		SCL2, SCL5	I/O	VCC1	Transmit/receive clock I/O for I²C mode.
		SCL0, SCL1, SCL6	I/O	VCC2	
5, 100 4, 98 3, 99	Serial interface SI/O3, SI/O4	CLK3, CLK4	I/O	VCC1	Transmit/receive clock I/O.
		SIN3, SIN4	I	VCC1	Serial data input
		SOUT3, SOUT4	O	VCC1	Serial data output.
28 27	Multi-master I²C-bus interface	SDAMM	I/O	VCC1	Serial data I/O. (Output is N-channel open drain)
		SCLMM	I/O	VCC1	Transmit/receive clock I/O. (Output is N-channel open drain)
96	Reference voltage input	VREF	I	VCC1	Reference voltage input for the A/D converter.
79-86	A/D converter	AN0 to AN7	I	VCC1	Analog input for the A/D converter.
		AN0_0 TO AN0_7	I	VCC2	
98		ADTRG	I	VCC2	External activation source input.
99, 100		ANEX0, ANEX1	I	VCC1	Extended analog input for the AD converter.
79-86 71-78 63-70	I/O ports	P0_0 to P0_7, P1_0 to P1_7, P6_0 to P6_7	I/O	VCC2	8-bit CMOS I/O ports. Each port has a direction register, allowing each pin in the port to be directed for input or output individually. A pull-up resistor may be enabled or disabled for input ports in 4-bit units.
21-28 15-20, 8-9 1-5, 98-100 87-93, 95		P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7	I/O	VCC1	8-bit I/O ports having equivalent functions to P0. However, P7_0, P7_1 and P8_5 are N-channel open drain output ports. No Pull-up resistor is provided. P8_5 is an input port for verifying the NMI pin level and shares a pin with NMI.

† YXD2, SDA2, SCL2, SDAMM and SCLMM are N-channel open drain output pins. TXDi, SDAi and SCLi (all where i = 0, 1, 5, 6) can be selected as CMOS output pins or N-channel open drain output pins by a program.

Table 2.3 Internal Pin Function for PLC Modem[‡]

Signal Name	Pin Name	I/O	Description
Internal interrupt input	INT0, INT6, INT7	I	INT interrupt input from PLC modem.
Internal timer A connection	TA0OUT	I/O	Timer A0 I/O form/to PLC modem.
	TA0IN	I	Timer A0 input from PLC modem.
Internal serial connection	TXD7	O	Serial data output to PLC modem.
	RXD7	I	Serial data input from PLC modem.
	CLK7	I/O	Transmit/receive clock I/O from/to PLC modem.
Internal ports	P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7	I/O	Ports to connect PLC modem. Used as addresses, data, control signals, and status signals to access registers of PLC modem and AFE.
RX signal	VINP	Analog input	Input pins for differential reception signals.
	VINN		
TX signal	VOUTP	Analog output	Output pins for differential transmission signals.
	VOUTN		
Analog pin	EXTLDP EXTLDN	Analog output	Differential transmission output pins for the external line driver as optional specifications.
	VCMTX	Analog output	Reference voltage output pin for the analog circuit of the transmitter block. Connect to a bypass capacitor for VSSA.
	VRT	Analog output	Reference voltage output pins for ADC of PLC block. Connect to a bypass capacitor for VSSA.
	VRB		
	VCM	Analog output	Reference voltage output pin for the analog circuit of receiver block. Connect to a bypass capacitor for VSSA.
Testing Pins	TESTP	Analog I/O	I/O for testing. Leave open.
	TESTN		
Digital Pins	OC_EN	I	Connect to VCCA via a register when using internal line driver for enabling over current protection. Connect VSSA via register when using external line driver for disabling over current protection.
	OC	O	Status output pin for the over current protection circuit.
	TS	O	Pin to turn off/on the external line driver.
Regulator Output	VCC15	Analog output	Regulator output pin (1.5 V) for the digital circuit of PLC block. Connect only to a bypass capacitor for VSSA. Do not use this pin to provide power to other circuits.

[‡] On-chip PLC modem should be controlled by DLL software released by Yitran. Do no access the PLC control registers directly by any user program.

3 IT900 FUNCTIONAL DESCRIPTION

The following chapters describe the different functional blocks shown in the IT900 block diagram in more detail. Functional blocks are described starting with the Analog Front End (AFE) from the right side of the block diagram, followed by the PHY and microcontroller.

3.1 ANALOG FRONT END (AFE)

The IT900 interfaces to the power line medium via an integrated Analog Front End (AFE). The AFE consists of the following main building blocks as shown in Figure 3:

1. Digital-to-Analog Converter (DAC) that converts the digital transmit-data from the PHY into an analog waveform to be transmitted over the power line.
2. Line Driver to amplify the analog signal provided by the DAC before it is coupled onto the power line.
3. Variable Gain Amplifier (VGA) to amplify the analog receive-data waveform coming from the power line coupler, thereby better utilizing the full dynamic range of the ADC.
4. Analog-to-Digital Converter (ADC) that converts the analog receive-data waveform, which is amplified by the VGA, into digital data that are then sent to the PHY.
5. Digital interface to and from the PHY transmitter and receiver blocks.

Analog front end (AFE) is the circuit located between PLC PHY and a power line. There are the following two signal paths in the AFE.

- Transmitting path: Consists of a DAC driven by the internal port, a low-pass filter (LPF), a differential Line Driver amplifier and a line coupling circuit which drives the power line.
- Receiving path: Consists of a line coupling circuit, an input filter, a differential VGA amplifier, a LPF)and an ADC. The line coupling circuit is common to both transmission and reception.

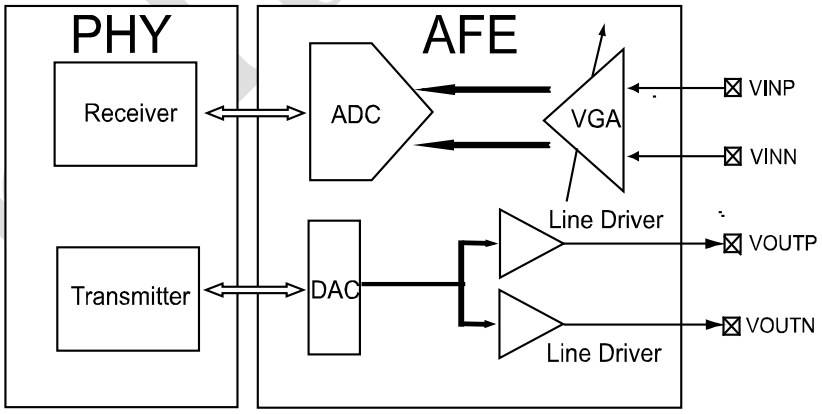


Figure 3: AFE Block Diagram

3.1.1 Transmit Path

The IT900 transmit path is shown in Figure 4.

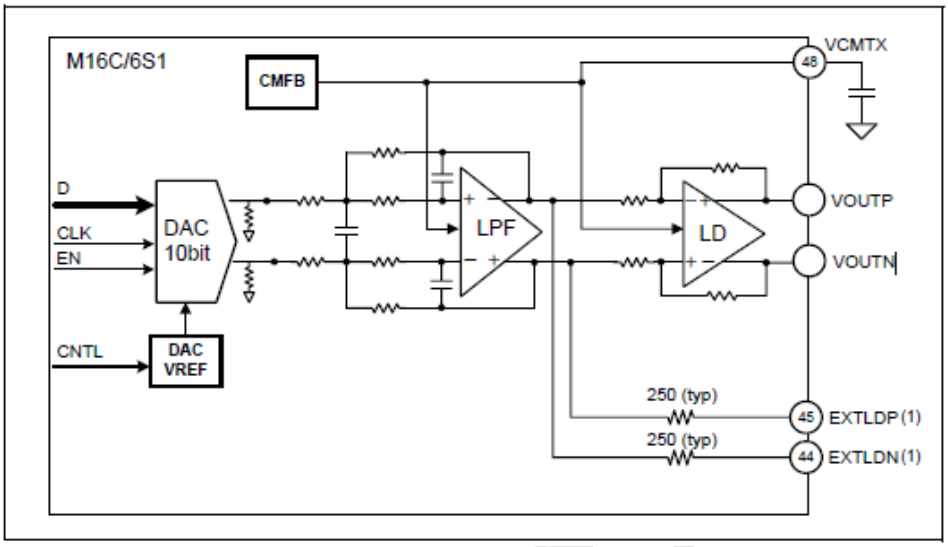


Figure 4: AFE Transmitter Circuit

Notes:

*When not using an external line drive amplifier, leave EXTLP and EXTLDN open.
*At AFE default register settings, the Line Driver (LD) is turned off if the internal temperature exceeds 125 °C.

3.1.1.1 Digital-to-Analog Converter (DAC)

The 10-bit DAC features a 16MS/s conversion speed and a Signal-to-Noise Ratio (SNR) of better than 70dB. It is used to convert the digital transmit-data from the PHY transmitter into an analog waveform, which is then amplified by the differential Line Driver before it is transmitted over the power line.

3.1.1.1.1 Adjustment of Output Amplitude

Transmission output amplitude can be changed by changing the VREF setting of the DAC. The relation between DACVREF code (4 bits) and amplitude is shown in Figure 5.

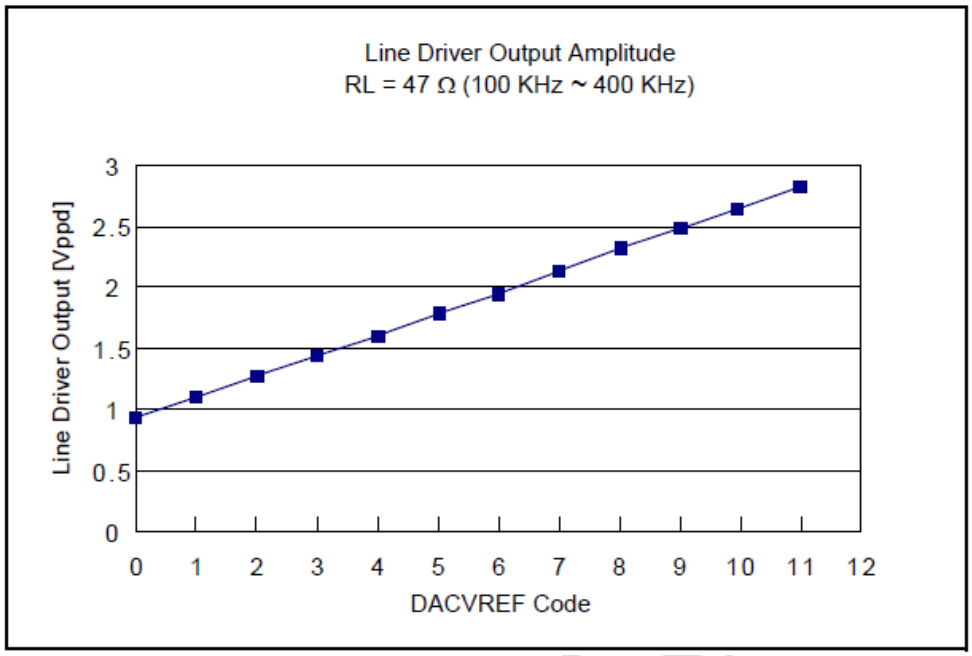


Figure 5: Line Driver Amplitude

DACVREF is the part of AFE75 register which is inside the AFE block. The relation between Load Resistance and Transformer output Amplitude is shown below.

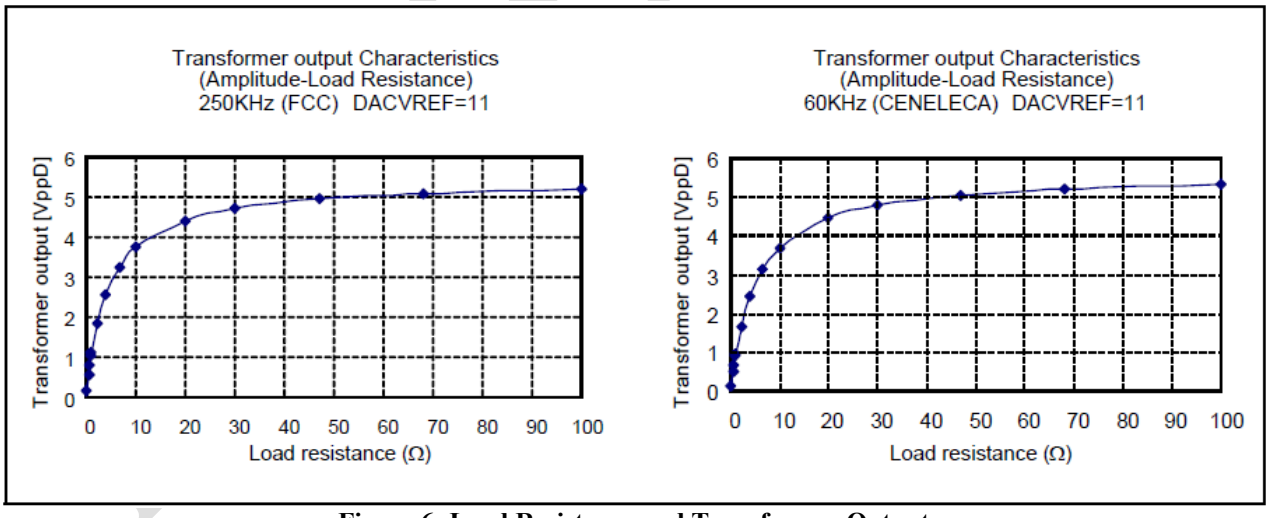


Figure 6: Load Resistance and Transformer Output

3.1.1.2 Line Driver

The Output Line Driver is a fully integrated class AB driver with differential outputs that is capable of driving a wide range of loads and delivering $1A_{peak\text{-}peak}$ of output current.

3.1.1.2.1 Short-circuit Protection (Over current Protection Circuit)

If DC over current flows due to a short across pins on the IT900, the on-chip protection circuit stops the line drive output. Once the over current protection circuit operates, no transmission can be performed until the over current protection circuit is reset.

This circuit is reset by setting the OC_EN pin to low, or setting bit 5 to "1" in the AFE71 register which is inside the AFE block, or an MCU reset. To resume the over current protection states, setting the OC_EN pin to high and setting the bit 5 to "0" in the AFE71 register.

OC_EN pin enable/disable the over current protection circuit. Set the OC_EN to "H" for enabling the over current protection circuit. When you use external line drive you need to disable over current protection circuit by setting OCLEN to "L".

* Note: The AFE registers should be written in 8-bit units. Write the same value not to change the value of bits other than the corresponding bit.

3.1.1.2.2 Peripheral Circuit When Using External Line Driver

When using a driver circuit which is located externally, connect pins EXTLDP and EXTLDN to the external driver input. To turn off the internal line driver, set bits 3 and 4 in the AFE72 register to "1" and bits 5 and 6 to "0". The EXTLDP and EXTLDP pin has an internal resistor for protection. Please add the internal resistor value, when calculating an external driver amplifier gain.

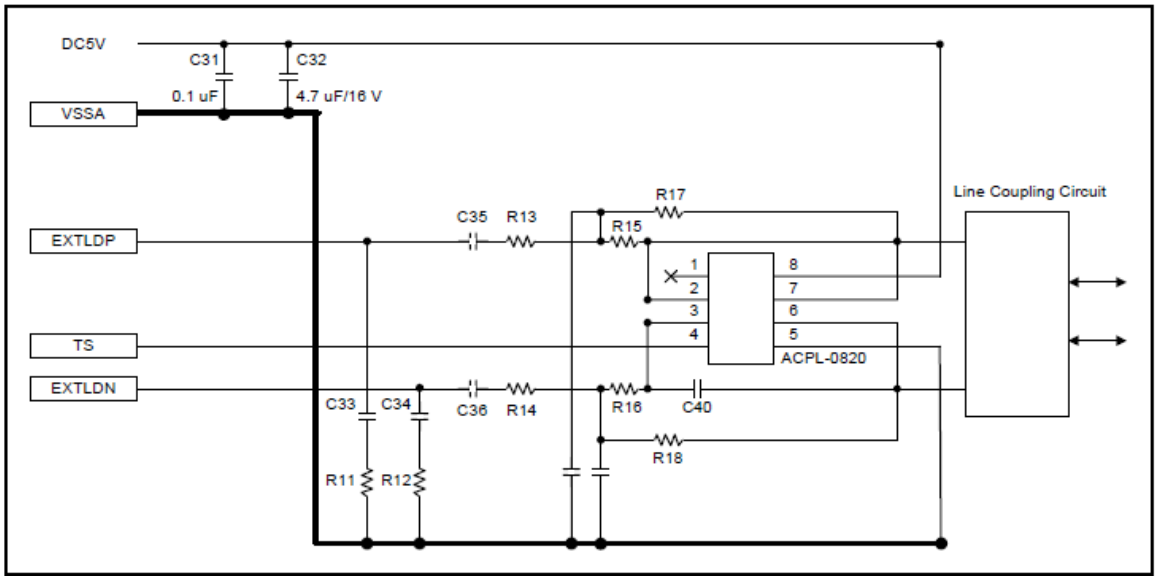


Figure 7: External Line Driver Example

The external line driver LSI of this circuit is ACPL-0820 (by AVAGO Technologies).
Internal resistance: 250 Ω (typ).

3.1.1.2.3 Short-circuit Protection (Over current Protection Circuit)

If DC over current flows due to a short across pins on the IT900, the on-chip protection circuit stops the line drive output. Once the over current protection circuit operates, no transmission can be performed until the over current protection circuit is reset.

This circuit is reset by setting the OC_EN pin to low, or setting bit 5 to "1" in the AFE71 register which is inside the AFE block, or an MCU reset. To resume the over current protection states, setting the OC_EN pin to high and setting the bit 5 to "0" in the AFE71 register.

OC_EN pin enable/disable the over current protection circuit. Set the OC_EN to "H" for enabling the over current protection circuit. When you use external line drive you need to disable over current protection circuit by setting OCLEN to "L".

* Note: The AFE registers should be written in 8-bit units. Write the same value not to change the value of bits other than the corresponding bit.

3.1.1.2.4 High-temperature Protection (Temperature Sensor Circuit)

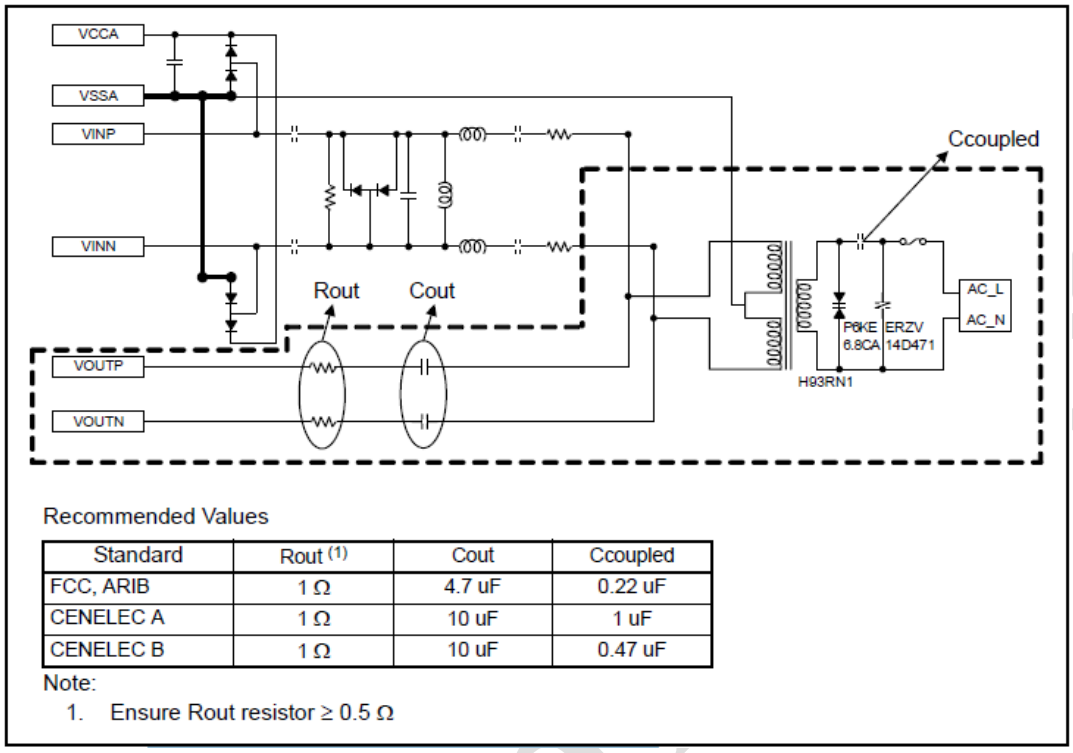
To set the temperature sensor circuit for high-temperature protection, use the following steps:

1. Set the value of TSDUREF_CNTL of AFE76 register to the required temperature.
2. Set INT7 mode to rising edge.

The maximum temperature is indicated by interrupt INT7.

Once an interrupt was generated by either the over current detector or temperature sensor, the other interrupt source for interrupts cannot generate an additional interrupt because both interrupt factor share the same interrupt vector.

A recommended peripheral circuit of the transmitter is shown in Figure 8.



Recommended Values

Standard	Rout (1)	Cout	Ccoupled
FCC, ARIB	1 Ω	4.7 uF	0.22 uF
CENELEC A	1 Ω	10 uF	1 uF
CENELEC B	1 Ω	10 uF	0.47 uF

Note:
1. Ensure Rout resistor ≥ 0.5 Ω

Figure 8: Recommended Peripheral Circuit of Transmitter

3.1.1.2.5 Notes on Mounting

IT900 has an embedded power line driver that can generate a large amount of heat when operating at a heavy load. If the chip will be mounted on the PCB, the thermally enhanced design of the footprint is needed. An example of the thermally enhanced footprint is provided in the IT900 Layout Designs document. The IT900 thermal pad located at the bottom of the IT900 package should be soldered to the thermal pad on the PCB. To improve the heat spreading of the IT900 package it is strongly recommended to use a PCB with at least four layers fabricated with FR4 material.

The printed wires supplying power to the IT900 line driver must have calculated width and thickness according to the current specifications provided in electrical characteristic section. Failure to follow this requirement can cause the line driver output signal degradation in terms of its amplitude and distortions. Use of PCB polygons is recommended for power supply connections.

Pins of the line driver power supply and outputs must be grouped together according to their functions and connected together using short and wide wires. No pins can be left open.

Line driver output VOUTN – pins 32, 33, 34
Line driver output VOUTP – pins 38, 39, 49
+3.3V power VCCA – pins 29, 30, 31 (Group 1), 41, 42, 43 (Group 2)
GND potential VSSA – pins 35, 36, 37

When using power and ground PCB polygons, each power and ground pin can be connected to their respective polygons, independently.

Use a transformer whose transfer ratio is 1:1.

3.1.2 Receive path

The IT900 receiver path is shown in Figure 9. A recommended input filter is shown in Figure 10.

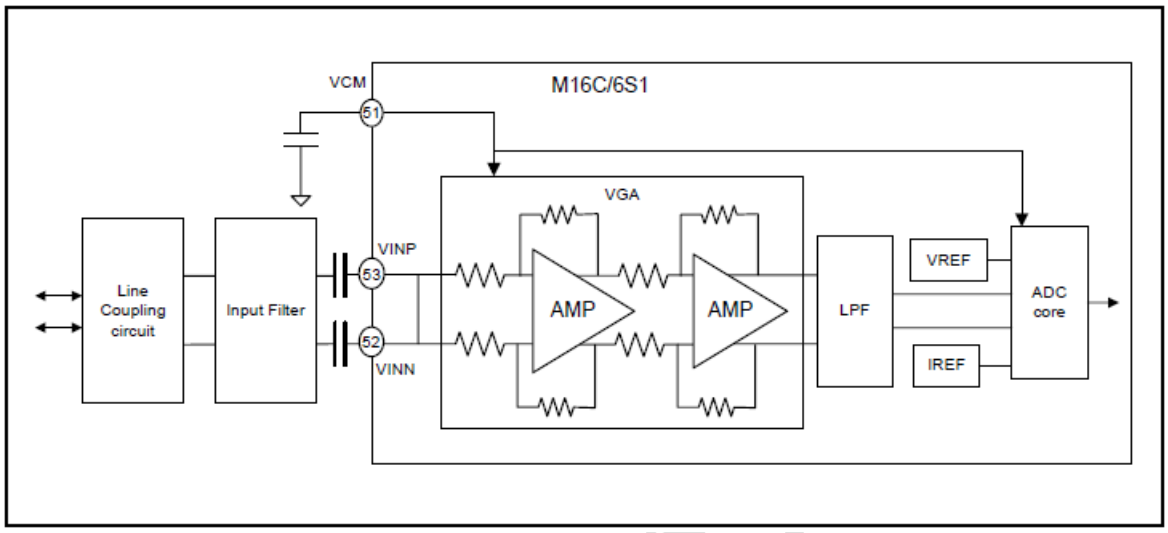


Figure 9: AFE Receiver Analog Circuit

	CA	CA2	CB	ARIB	FCC
C24, C25	100 nF	15 nF	10 nF	18 nF	18 nF
C26	16 nF	39 nF	27 nF	3.9 nF	3.9 nF
L1, L2	150 uH	270 uH	220 uH	33 uH	33 uH
L3	1.2 mH	100 uH	82 uH	150 uH	150 uH

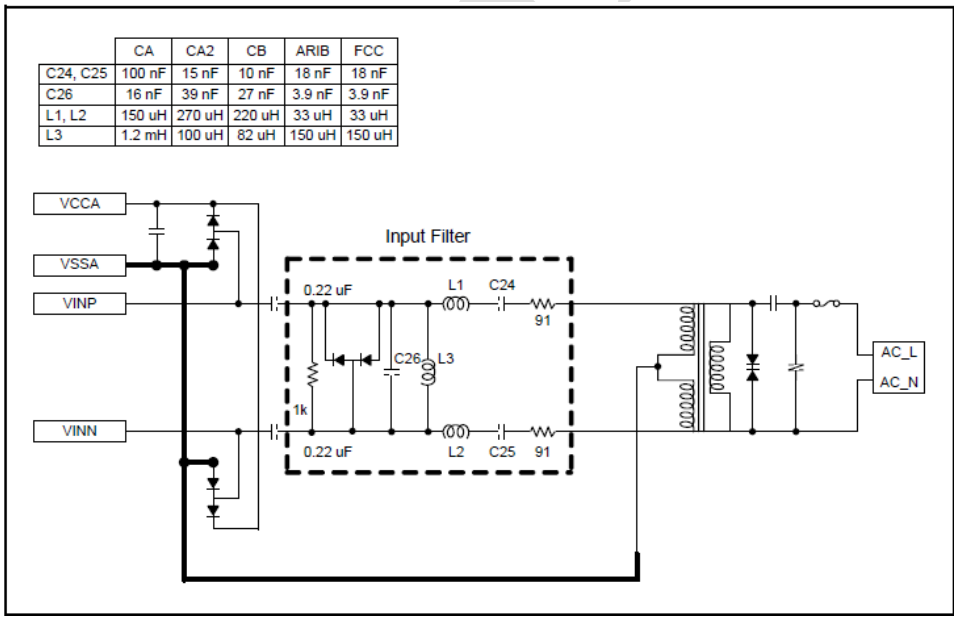


Figure 10: Recommended Input Filter

3.1.2.1 Variable Gain Amplifier (VGA)

The VGA is a switched-capacitor, fully differential amplifier with digitally controlled variable gain. The gain is variable in 6dB steps from −6dB to 42dB. Gain is automatically controlled by the IT900 to scale the incoming power line signal amplitude to the Analog-to-Digital Converter's available resolution. Total harmonic distortion is better than 70dB and the input referred noise is $<15\mu V_{RMS}$ at maximum gain.

3.1.2.2 Analog-to-Digital Converter (ADC)

The ADC is a high resolution, 13-bit, 2.56MS/s successive approximation Analog-to-Digital Converter with a typical integrated and differential non linearity of ±0.5LSb each. The ADC converts the received analog data waveform, which is amplified by the VGA, into a digital stream that is transferred to the PHY receiver.

3.2 PHYSICAL LAYER (PHY)

3.2.1 Overview

The PHY layer is a communication transceiver that is optimized for the power line medium. The PHY layer employs the DCSK (Differential Code Shift Keying) and DCSK turbo modulation techniques.

The PHY Layer consists of four major functional blocks:

1. **Transmitter** – Manages all aspects of physical transmission: encoding, interleaving, data modulation, spectrum shaping and power leveling.
2. **Receiver** – Manages all aspects of physical reception: packet synchronization, data demodulation, de-interleaving and decoding.
3. **PHY Manager** – A packet management unit and state machine that, together with the **Error Correction Code Unit**, manages all aspects of logic packet transmission and reception such as cyclic redundancy check, header decoding, etc.
4. **Hardware Data Link Layer** – Provides and manages the interface from the PHY block to the Software Data Link Layer that is implemented in the microcontroller firmware.

The block diagram of the PHY transmit and receive paths is shown in Figure 11.

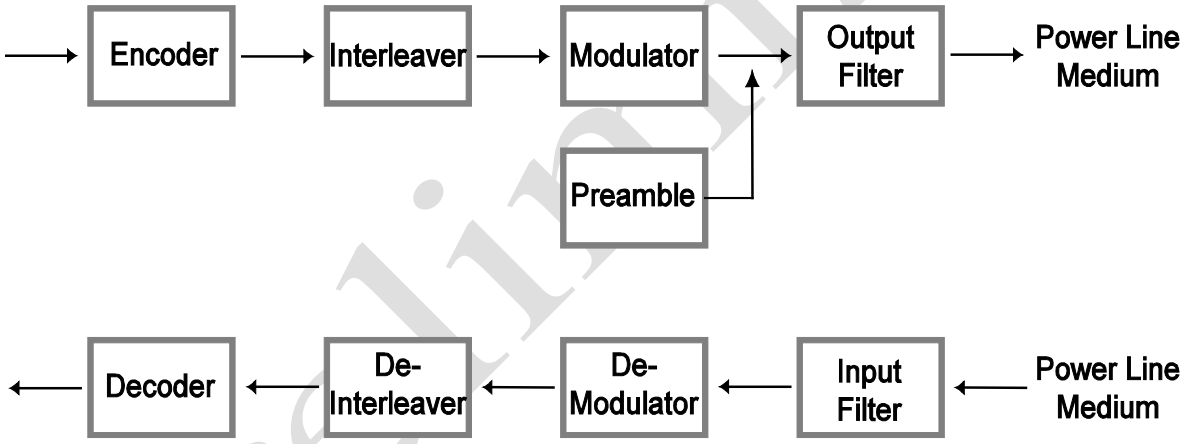


Figure 11: PHY Transceiver Block Diagram

3.2.2 PHY Transmitter

The transmitter block diagram is shown at the top of Figure 11. The transmitter is composed of the following main modules:

- **Encoder** – Receives data bits from the PHY Manager, encodes them and sends the encoded data to the Interleaver.
- **Interleaver** – Receives the code words from the encoder module, mixes them and sends the interleaved code words to the modulator.
- **Modulator** – Receives the interleaved code words from the interleaver, modulates them and sends the modulated symbols to the output shaping filter.
- **Output Filter** – Receives the modulated symbols from the modulator and filter the modulated symbol.
- **Preamble** – Generates the synchronization sequence that precedes the PHY packet.

3.2.3 PHY Receiver

The receiver block diagram is shown at the bottom of Figure 11. The receiver is composed of the following main modules:

- **Decoder** – Receives the data bits from the de-interleaver, decodes them and sends the decoded data to the PHY Manager.
- **De-Interleaver** – Receives the interleaved code words from the demodulator module, extracts the code blocks and sends the de-interleaved code blocks to the decoder.
- **Demodulator** – Receives the code blocks from the input filter, demodulates them and sends the demodulated symbols to the de-interleaver.
- **Input Filter** – Receives the modulated data symbols from the power line, filters the modulated symbol and sends the resulting code blocks to the demodulator.

A physical carrier sense is provided by the receiver to the higher layer. The following carrier sense features are supported:

- **Carrier Detect (CD)** – indicates detection of a symbol on the channel.
- **Sync** – indicates detection of a valid preamble sequence.

3.2.4 PHY Operating Modes

The following table details PHY operating modes:

Item		Specification
Modulation technique		DCSK, DCSK Turbo (DSCKT)
Error correction		Short-block error correction, CRC-16
Compliant worldwide regulations		FCC, ARIB, EN50065-1-CENELEC
Maximum Data rate	FCC and ARIB	120kHz to 400kHz • Up to 500 kbps in DCSK Turbo Modulation • Up to 7.5 kbps in DCSK Modulation
	CENELEC	A Band: 9 kHz to 95 kHz • Up to 150 kbps in DCSK Turbo Modulation • Up to 2.5 kbps DCSK Modulation
		A2 Band: 71 kHz to 94 kHz • Up to 37.5 kbps in DCSK Turbo Modulation • Up to 1.88 kbps DCSK Modulation
		A4 Band: 45 kHz to 95 kHz • Up to 150 kbps in DCSK Turbo Modulation
		B Band: 95 kHz to 125 kHz • Up to 50 kbps in DCSK Turbo Modulation • Up to 2.5 kbps DCSK Modulation

Each signal band requires suitable configuration of the PLC modem, adjusting the input filter to a signal band and output amplitude, setting.

Refer to the following standards about the regulation of a signal level outside the band.

- U.S.: FCC standard, part 15
- Europe: CENELEC standard, EN 50065-1
- Japan: ARIB, STD-T84

The PHY layer supports the following basic transmission modes:

- DSCK Modes
- DCSK Turbo Modes

The transmission mode determines the encoding scheme, interleaving scheme and modulation scheme as detailed in Table 3.1.

Table 3.1: DCSK Transmission Modes

Mode	Encoding	Modulation	Symbol Rate[§]	Supported Band
DCSKT 0	(26,32)	QAM	1	FCC, ARIB, CA
DCSKT 1	(11,16)	QAM	1	FCC, ARIB, CA
DCSKT 2	(26,32)	QAM	2	FCC, ARIB, CA, CB
DCSKT 3	(11,16)	QAM	2	FCC, ARIB, CA, CB
DCSKT 4	(11,16)	QPSK	1	FCC, ARIB, CA, CB
DCSKT 5	(11,16)	QPSK	2	FCC, ARIB, CA, CB
DCSKT 6	(11,16)	QPSK	3	FCC, ARIB, CA, CB
DCSKT 7	(11,16)	BPSK	3	FCC, ARIB, CA, CB
DCSKT 8	(11,16)	QPSK	4	FCC, ARIB, CA, CB
DCSKT 9	(11,16)	BPSK	4	FCC, ARIB, CA, CB
DCSKT 10	(11,16)	QPSK	5	FCC, ARIB
DCSKT 11	(4,8)	BPSK	4	FCC, ARIB, CA, CB
DCSKT 12	(4,8)	BPSK	5	FCC, ARIB
DCSKT_TD [**]1	(11,16) with ×2 repetition	QAM	2	FCC, ARIB, CA, CB
DCSKT_TD 2	(11,16) with ×2 repetition	QPSK	1	FCC, ARIB, CA, CB
DCSKT_TD 3	(11,16) with ×2 repetition	QPSK	2	FCC, ARIB, CA, CB
DCSKT_TD 4	(11,16) with ×2 repetition	QPSK	3	FCC, ARIB, CA, CB
DCSKT_TD 5	(11,16) with ×2 repetition	BPSK	3	FCC, ARIB, CA, CB
DCSKT_TD 6	(11,16) with ×2 repetition	QPSK	4	FCC, ARIB, CA, CB
DCSKT_TD 7	(11,16) with ×2 repetition	BPSK	4	FCC, ARIB, CA, CB
DCSKT_TD 8	(11,16) with ×2 repetition	QPSK	5	FCC, ARIB
DCSKT_TD 9	(4,8) with ×2 repetition	BPSK	4	FCC, ARIB, CA, CB
DCSKT_TD 10	(4,8) with ×2 repetition	BPSK	5	FCC, ARIB
DCSK[*] - ERM	(5,7) with ×4 repetition	DCSK4	-	FCC, ARIB, CA, CB
DCSK[*] - RM	(5,7)	DCSK4	-	FCC, ARIB, CA, CB
DCSK[*] - SM	(7,9)	DCSK6	-	FCC, ARIB

***The DCSK transmission modes are fully back compatible with Yitran's IT800 and IT700 series.**

[§] Symbol Rate indicates the rate of the DCSKT symbols where 1 is highest rate, and 5 is lowest rate.
[**] TD (Time Diversity) is a mode is used when there is strong periodic noise on the channel

The following table details the IT900 PHY Payload Rates for the different Transmission bands per Tx mode:

Table 3.2: Effective PHY Rate

TX Mode	Effective PHY Rate [kbps]		
	FCC	CENELEC-A	CENELEC-B
DCSKT 0	346	104	N/A
DCSKT 1	293	88	N/A
DCSKT 2	260	65	32.5
DCSKT 3	220	55	27.5
DCSKT 4	146	44	27.5
DCSKT 5	110	27.5	13.75
DCSKT 6	55	13.75	6.88
DCSKT 7	28	6.88	3.44
DCSKT 8	28	6.88	3.44
DCSKT 9	14	3.44	1.72
DCSKT 10	14	2.5	1.25
DCSKT 11	10	N/A	-
DCSKT 12	5	N/A	-
DCSKT _TD 0	109	27.14	13.57
DCSKT_TD 1	72	21.58	13.49
DCSKT_TD 2	54	13.57	6.79
DCSKT_TD 3	27	6.71	3.36
DCSKT_TD 4	14	3.36	1.68
DCSKT_TD 5	13	3.15	1.57
DCSKT_TD 6	7	1.57	0.79
DCSKT_TD 7	6	1.14	0.57
DCSKT_TD 8	5	N/A	N/A
DCSKT_TD 9	2	N/A	N/A
DCSK - SM	5.83	N/A	N/A
DCSK - RM	3.57	1.8	1.8
DCSK - ERM	0.9	0.45	0.45

3.3 Enhanced M16/C60 Microcontroller

The IT900 features an integrated, enhanced M16/C60 microcontroller, running at a system clock frequency of 46.08 MHz with 256KBytes of Flash program memory and 31KBytes RAM data memory.

Table 3.3: Microcontroller Functions

Item	Function	Description
CPU	Central processing unit	M16C/60 Series core (multiplier: 16-bit × 16-bit = 32-bit, multiply and accumulate instruction: 16-bit × 16-bit + 32-bit = 32-bit) • Number of basic instructions: 91 • Minimum instruction execution time: 32.6 ns (f(BCLK) = 30.72 MHz, VCC1 = VCC2 = 3.0 to 3.6 V) 41.7 ns (f(BCLK) = 24 MHz, VCC1 = VCC2 = 2.7 to 3.0 V)
Memory	ROM, RAM, data flash	
Clock	Clock generator	• 4 circuits: Main clock, sub clock, low-speed on-chip oscillator (125 kHz), PLL frequency synthesizer • Oscillation stop detection: Main clock oscillation stop/re-oscillation detection • Frequency divider circuit: Divide ratio selectable from 1, 2, 4, 8, 16 • Power saving features: Wait mode, stop mode • Real-time clock
I/O Ports	Programmable I/O ports	• CMOS I/O ports: 53 (selectable pull-up resistors) • N-channel open drain ports: 3
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 14 (NMI, INT × 5, key input × 8) • Interrupt priority levels: 7
Watchdog Timer		15-bit timer × 1 (with prescaler) Automatic reset start function selectable
DMA	DMAC	• 4 channels, cycle steal mode • Trigger sources: 43 • Transfer modes: 2 (single transfer, repeat transfer)
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse width modulation (PWM) mode, Event counter two-phase pulse signal processing (two-phase encoder input) × 3, programmable output mode × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse period measurement mode, pulse width measurement mode
	Real-time clock	Count: seconds, minutes, hours, days of the week, months, years
Serial Interface	UART0 to UART2, UART 5 to UART7	Clock synchronous/asynchronous × 5 channels, PLC connection × 1 channel, Special mode emulation for I2C-bus, IEBus, SIM, and multi device communication
	SI/O3, SI/O4	Clock synchronization only × 2 channels
Multi-master I²C-bus interface		1 channel
A/D Converter		10-bit resolution × 18 channels, including sample and hold function Conversion time: 1.4 µs
CRC Calculator		CRC-CCITT (X16 + X12 + X5 + 1), CRC-16 (X16 + X15 + X2 + 1) compliant
Encryption	AES	AES Encryption (Key length: 128 bits)
Flash Memory		• Erase/write power supply voltage: 2.7 to 3.6 V • Erase/write cycles: 1,000 times (program ROM 1, program ROM 2), 10,000 times (data flash) • Program security: ROM code protect, ID code check

3.3.1 Firmware Activity Monitoring

It is recommended to implemented firmware activity monitoring logic by periodically polling the External Host Interface, and verifying correct response from the IT900. If no response is received from the IT900, the Host should issue a reset sequence.

For devices that require very high reliability, the IT900 provides an "activity monitor" Pin (P1_0), that may be used by an external circuitry to monitor correct operation. This pin generates pulse (1 mS width - active high) every 0.8 ± 0.1 seconds for all bands, except for CA2 that generates pulse every 1.2 ± 0.1 seconds.

If the pulse is not generated for more than 1.7 sec, then the IC should get a reset sequence. The monitoring circuitry may be implemented by watchdog element.

3.3.2 Safe Mode

As part of the startup sequence after reset, IT900 loads parameters stored in the non-volatile memory. The host application may inadvertently set the values of the parameters such as to cause bad startup sequence of IT900, which may result in repeated resets. Safe mode allows IT900 to startup using the default parameter values stored in the firmware, thus guaranteeing successful completion of the startup sequence. The host application may then read and correct corrupt values stored in the non-volatile memory.

The procedure for recovery from parameters corruption in IT900 is as follows:

- To enter Safe Mode, set IT900 pin P1_4 to logical "0".
- Resetting IT900 will cause it to wake up with default parameters.
- Set pin P1_4 to logical "1" (P1_4 as an internal pull-up).
- Apply proper configuration to IT900 and save settings to NVM.

3.4 Y-NET PROTOCOL

In the Protocol Architecture version, the IT900 is accompanied by Yitran's Y-Net protocol firmware. The Y-Net protocol stack firmware implements Media Access Control (MAC) and Network Layer (NL), which are layers 2 and 3 of the seven-layer OSI model highlighted in grey in Figure 12. The following sections provide an overview of the Y-Net protocol stack features and capabilities.

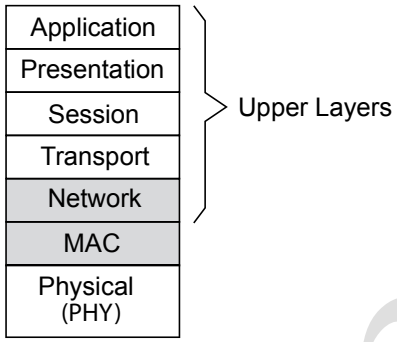


Figure 12: OSI Network Layer Model

3.4.1 Media Access Control (MAC)

3.4.1.1 Introduction

The MAC layer implements a highly efficient channel access management function, which enables occupation of the channel by a single node at a given time, while providing fair Quality of Service (QoS) among nodes and at the same time maintaining high overall network throughput.

In addition, the MAC layer supports low-level services as detailed below:

- Packet Transmission Services
- Addressing and Logical Networks
- Virtual Jamming
- Coexistence with CEBus and X-10 Nodes
- Statistics and Diagnostics

3.4.1.2 Channel Access Method

The MAC uses a Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA) protocol with an adaptive back-off scheme and channel access prioritization to manage channel access in such a way that only a single sending node occupies the communication channel at any given time. The channel access method is optimized for the power line medium. It provides optimal performance for network sizes ranging from a few nodes to thousands of nodes.

The media access control is based on:

- Super-Frame Time Intervals
- Carrier Sense Mechanism
- Packet Prioritization and Quality of Service (QoS)
- Adaptive Back-off Algorithm

3.4.1.2.1 Super-Frame Time Intervals

A super-frame is the time between the end of packet transmission (EOP) and the start of the next packet transmission. The super frame is sub-divided into time intervals for signaling MAC events, a back-off period and/or message transmission period.

3.4.1.2.2 Carrier Sense Mechanism

The PHY layer provides Carrier Detection (CD) indication to the MAC. The output of the PHY CD signal to the MAC indicates an ongoing transmission on the line.

3.4.1.2.3 Packet Prioritization and Quality of Service (QoS)

The upper layer can assign priorities to packets as follows:

- Emergency
- High
- Normal

The MAC signals the priority of packets to be transmitted as part of the super frame (no signal for normal priority packets). The MAC ensures that only transmitters that have packets with the highest priority will contend for channel access in each super-frame.

3.4.1.2.4 Adaptive Back-off Algorithm

The adaptive back-off algorithm manages the contention for the channel by multiple transmitters. The MAC continuously updates the size of the back-off randomization range. The back-off range is optimally set for maximizing the throughput as a function of the number of simultaneous nodes contending for channel access.

If the MAC is unable to transmit the packet within a timeout period set by the upper layer, it discards the packet as blocked and informs the upper layer.

3.4.1.3 MAC Packet Transmission Services

The MAC layer encapsulates the payload received from the Upper Layer and provides various types of packet transmission services to and from the Upper Layer.

The MAC protocol supports the packet delivery services detailed in Table 3.4.

Table 3.4: Packet Delivery Services

Service	Description
Unicast with Acknowledgment	Intranetworking Unicast transmission in which the receiving node sends an acknowledgment to the transmitting node to indicate the successful reception or a lack of resources to receive the packet.
Unicast Repetitive Un-acknowledgment	Intranetworking Unicast transmission service in which the packet is retransmitted a specified number of times, regardless of its successful or unsuccessful delivery. The receiving node does not send a packet reception acknowledgment.
Broadcast	The MAC provides two types of broadcast services: (1) **Intranetworking Broadcast** – The packet is transmitted to all nodes in the same logical network. (2) **Internetworking Broadcast** – The packet is transmitted to all nodes regardless of their logical network. Broadcast packets may also be retransmitted repetitively, using the repetitive un-acknowledgment service.

3.4.1.4 IT900 Transmission Rate Modes

The IT900 supports multiple transmission rate modes which are dynamically selected by the IT900 MAC layer according to channel quality and statistics. In addition, the IT900 supports Yitran's IT700/IT800 modulation (DCSK) and rates which will be activated automatically when target device is IT800/IT700 or when channel conditions require.

The table below details the range of transmission rates supported by the IT900 for each operation band:

Table 3.5: IT900 Transmission Rates

TX Mode	Data Rate [kbps]		
	FCC	CENELEC-A	CENELEC-B
DCSKT Turbo (DCSKT)	Up to 500	Up to 150	Up to 50
DCSK	7.5 (SM), 5(RM), 1.25(ERM)	2.5(RM), 0.625(ERM)	2.5(RM), 0.625(ERM)

3.4.1.5 MAC Addressing and Logical Networks

The IT900 MAC layer uses a 16-byte Serial Number (S/N), which is unique among all IT900 devices. The S/N is used by Internetworking broadcast transmissions to identify the transmitter.

In addition, the IT900 MAC layer defines an 11-bit logical node address (Node ID) and a 10-bit logical network address (Network ID). The logical node and network addresses are local to the specific logical network. The network address must be unique between different logical networks on the same physical network and the node address must be unique within the same logical network. A node can only use a single logical address. The network and node addresses can be configured by the Upper Layer. Communication services within the same logical network use logical addressing.

3.4.1.6 Security: Encryption and Virtual Jamming

The MAC layer provides security services, including 128-bit AES encryption operating in CTR mode[††], CBC-MAC 32 message authentication, as well as message and encryption counters for message uniqueness.

These security services allow the implementation of a secured platform that provides a high level of confidentiality for the information transmitted over the power line medium.

Virtual jamming can be used to identify an impostor node attempting to infiltrate the network using the logical address of a valid network node. The node whose logical address is spoofed by another node sends an impostor packet to inform the network of the impostor, thus preventing the execution of commands that the impostor has issued.

3.4.1.7 Coexistence with CEBus and X10 Nodes

The IT900 PHY detects CEBus and X10 packets on the medium. The MAC layer defers transmission if the PHY indicates that such transmission is ongoing.

3.4.1.8 Statistics and Diagnostics

The PHY and MAC layers collect and provide channel quality information and statistics to the Upper Layer.

[††] Encryption is not currently supported, but will be available in future versions of the Y-Net stack.

3.4.2 Network Layer (NL)

3.4.2.1 Introduction

The NL transparently creates and maintains a tree-type topology network and releases the Upper Layer from the responsibility of handling the constantly changing conditions of the power line medium.

The logical network contains a Network Coordinator (NC) node responsible for network formation activities. The NC is expected to remain online for proper operation of the network. All other nodes in the logical network are Remote Stations (RS). RS may serve as a router that routes packets to or from the NC and may also implement remote application functionality. RS-to-RS communication is supported as long as there is physical connectivity between the two nodes and no need for routing the packets.

The NL provides the following networking services:

- **Data Services** – Provides advanced intranetworking and internetworking transmission services.
- Management Services, as follows:
    - **Network Formation Services** – Enable users without any prior networking or protocol knowledge to easily install, create and maintain logical networks.
    - **Dynamic Routing Service** – The NL creates a tree topology, enabling the NC to communicate with all nodes in the same logical network and vice versa (via intermediate nodes if required). This service provides complete transparency of the communication between all the devices and the NC, and makes them appear like standard peer-to-peer. Peer-to-peer communication between any two devices is also supported, as long as they have direct physical connectivity.

3.4.2.2 Data Services

Data services are responsible for transmission and reception of upper layer payload. The data services used by the NL are as follows:

- Internetworking: Transmission of data between nodes in any logical network.
- Intranetworking: Transmission of data (may be over multiple hops) between nodes in the same network.

3.4.2.2.1 Internetworking Services

Internetworking Unicast Service

The Internetworking Unicast Service allows a source node from one logical network to transmit packets to an individual destination node in any logical network. The figure below shows an internetworking Unicast transmission where filtering is performed by the receiver according to the S/N.

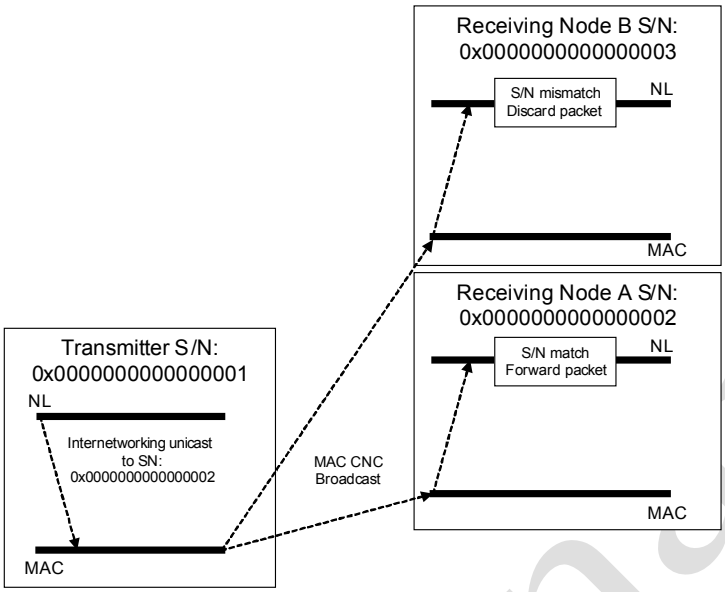


Figure 13: Internetworking Unicast Message Flow

Internetworking Broadcast Service

The Internetworking Broadcast Service allows a source node to transmit packets to all surrounding nodes in any logical network. The figure below shows an internetworking broadcast transmission where all nodes receive the packet.

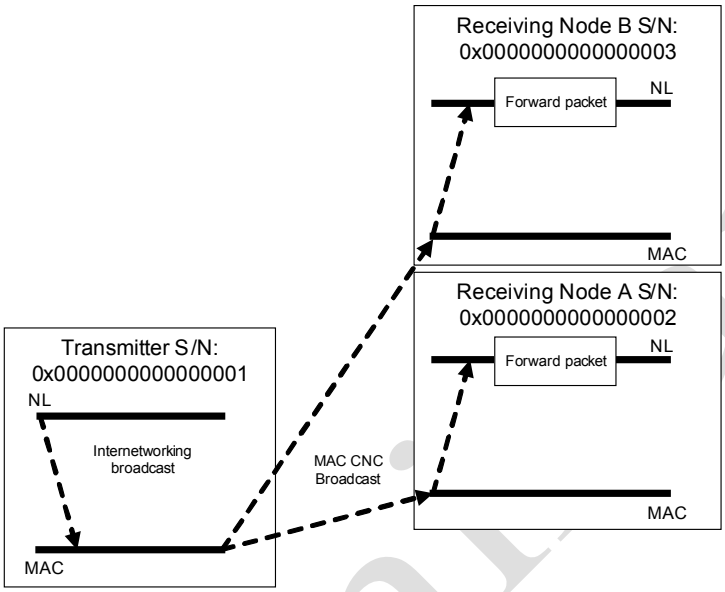


Figure 14: Internetworking Broadcast Message Flow

Internetworking Security[‡‡]

Internetworking messages can be secured through encryption of the payload on the transmitter side and decryption on the receiver side.

Internetworking Authorization[§§]

The Upper Layer can configure internetworking data services authorization for received packets that are marked as destined for the Upper Layer to one of the following:

- **All** – Authorize all internetworking data packets to the Upper Layer to be forwarded.
- **Encrypted Only** – Authorize only encrypted internetworking data packets to the Upper Layer to be forwarded. Unencrypted internetworking data packets to the Upper Layer are discarded.
- **None** – No internetworking data are allowed to be forwarded to the Upper Layer. All internetworking data packets to the Upper Layer are discarded.

[‡‡] Security is currently not supported, but will be available in future versions of the Y-Net stack.
[§§] Authorization is currently not supported, but will be available in future versions of the Y-Net stack.

3.4.2.2.2 Intranetworking Services

Direct Intranetworking Unicast

The Direct Intranetworking Unicast service allows a source node to transmit packets to an individual destination node in the same logical network if they can communicate directly. The figure below shows Direct Intranetworking Unicast transmission where filtering of the packet is performed by the receiver according to the logical address.

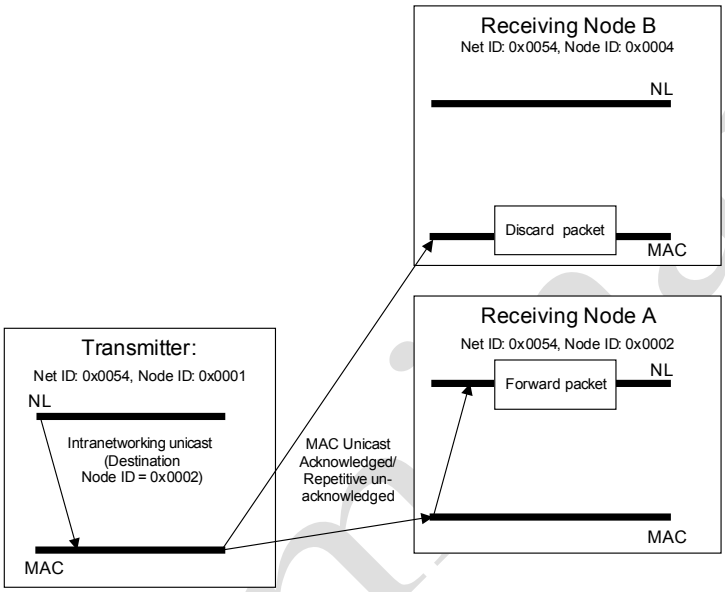


Figure 15: Direct Intranetworking Unicast Message Flow

Routed Intranetworking Unicast

The NL routing capabilities extend the MAC transmission service to allow nodes from the same logical network, which have no direct connection, to communicate via intermediate nodes.

In the routing process each node along the route, from the originating node to the final destination node, retransmits the packet using one of the MAC Unicast transmission services (acknowledged or repetitive un-acknowledged). The originating node defines which MAC transmission service to use. All intermediate nodes use the same MAC service to retransmit the packet to the next node along that route.

The source node can encrypt the message prior to transmission and only the final destination node will decrypt it.

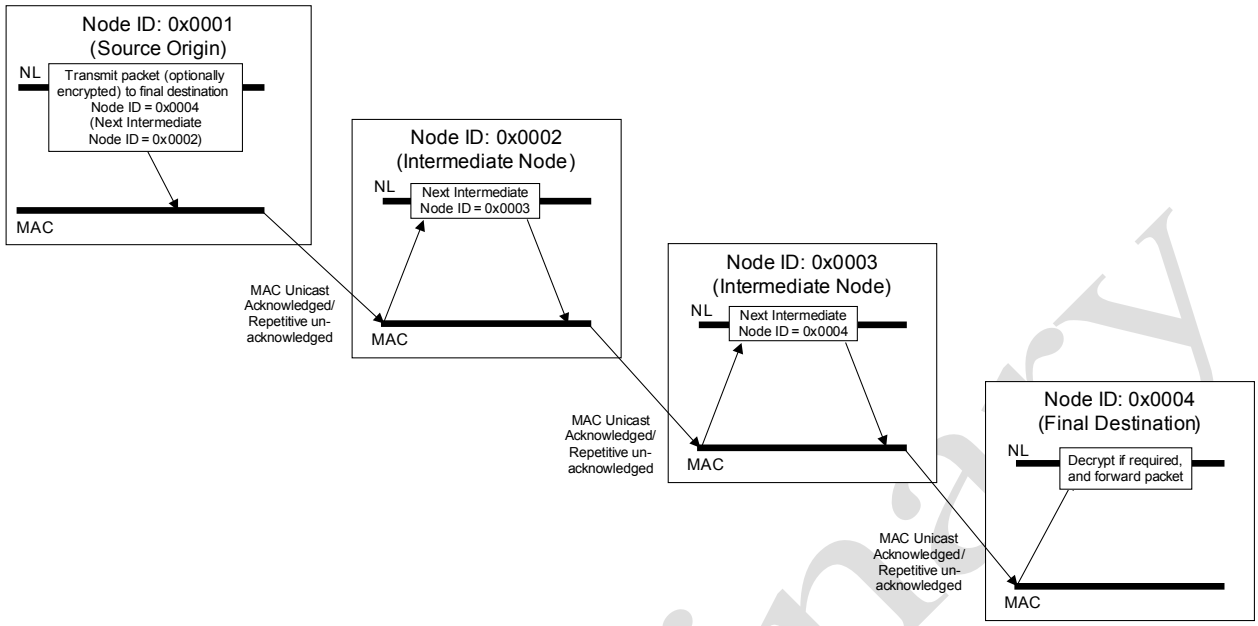


Figure 16: Routed Intranetworking Unicast Message Flow

The NL routing function selects the next node along the route to the final destination and retransmits the packet to that node as shown in
Figure 16.

Intranet Broadcast Service

The Intranetworking Broadcast service allows a source node to transmit packets to all nodes in the same the same logical network.

Intranetworking Security[***]

Intranetworking messages can be secured by the NL through encryption of the payload on the transmitter side and decryption on the receiver side. The security services include 128-bit AES encryption operating in CTR mode, CBC-MAC 32 message authentication and message and encryption counters for message uniqueness.

Intranetworking Authorization[†††]

The Intranetworking packets authorization applies to all intranetworking packets. The following authorization modes are available:

[***] Security is currently not supported, but will be available in future versions of the Y-Net stack.
[†††] Authorization is currently not supported, but will be available in future versions of the Y-Net stack.

- **None** – Only unencrypted intranetworking packets are received. Encrypted packets are discarded.
- **Secure –** Only encrypted intranetworking packets are received. Unencrypted packets are discarded.

Maximum Payload Size per NL Data Service

The maximum payload size supported per NL data service is as follows:

Table 3.6: Maximum Payload Size per NL Data Service

#	Service	Max Payload Size – DCSK Turbo rates	Max Payload Size – DCSK rates	
		Encrypted/Non Encrypted	*Encrypted*	*Non Encrypted*
1	Internetworking Unicast	Up to 1522 bytes (Enc' is N/A)	N/A	87 bytes
2	Internetworking Broadcast	Up to 1522 bytes (Enc' is N/A)	N/A	103 bytes
3	Intranetworking source routing service	Up to 1522 bytes	67 bytes	76 bytes
4	Intranetworking table routing service	Up to 1522 bytes	97 bytes	106 bytes
5	Intranetworking direct Unicast service	Up to 1522 bytes	100 bytes	109 bytes
6	Intranetworking Broadcast service	Up to 1522 bytes	100 bytes	109 bytes
7	Fragmented Intranetworking services	1522 bytes		

*Note: the payload size allows for full Ethernet/IPv6 packets.

The actual size of single fragment varies according to the transmission rate mode and regulation.
When the payload size exceeds the actual single fragment size the Y-Net splits the transmission into multiple fragments that are then reassembled in the receiving node. This mechanism is called **fragmentation** at the transmitting node and **reassembly** at the receiving node.

3.4.2.3 NL Management Services

The NL management module provides two primary services:

- Network Formation Services
- Dynamic Routing Service

3.4.2.3.1 Network Formation Services

The NL network formation services consist of the following:

- Logical network creation
- Network admission control
- Logical addressing management
- Networking indications to host

Logical Network Creation

The logical network creation service enables an NC to select a unique Network ID (automatically or manually by configuration) and create a logical network, thereby enabling RS nodes to join the logical network of the NC.

Network Admission Control

The network admission control services enable and assist the end user to (automatically or in conjunction with the application):

- Associate nodes that should belong to the same logical network together.
- Prevent hostile or incorrect nodes from joining a logical network.
- Prevent nodes from joining a hostile or incorrect logical network.

Two services enable the above to be performed in a simple and quick manner:

- **Admission Process (in NC)** – The NC admits only allowed nodes to its network based on its admission mode configuration (i.e. only nodes that should belong to the logical network are admitted and potentially hostile or incorrect nodes are rejected). The admission modes are described in Table 3.7.

- **Approval Process (in RS)** – The RS needs to approve the NC's decision to admit it to its logical network thereby preventing it from joining a hostile or incorrect logical network. When the NC admits a new node to the network, it attaches an 8-byte Node Key field to the admission approval packet sent to the RS. The Node Key can be set per RS by the NC application in "Application Mode" admission mode or by default using the Node Key configured to the NC. If the Node Key configured in the RS matches the one received from the NC, the RS approves the admission of the NC to its logical network. Otherwise, the RS rejects the admission of the NC and does not join the network. The Node Key mechanism can be used for auto-segmentation of overlapping logical networks by configuring the same Node Key to an NC and all RS that should be associated with the

logical network of that NC. The RS optionally can disable the use of the Node Key mechanism, thereby accepting admission of any admitting NC by setting all the bytes of its configured Node Key to 0x00.

Table 3.7: NC Admission Modes

Admission Mode	Description
Auto Mode	When an admission request arrives to the NC from any RS, the NC immediately admits the RS to its network. There is no admission restrictions or host application involvement.
S/N Range Mode	When an admission request arrives to the NC from an RS, the NC admits only RS whose MSB of their S/N are within the S/N range configured in the NC (number of MSB to use is configurable in the NC). The host application is responsible to configure the S/N range, and the number of MSB to be used prior to the admission process.
Application Mode	When an admission request arrives to the NC from an RS, the NL sends an indication to the host application. The host application is responsible to decide whether to admit the RS based on the S/N of the RS provided by the NL of the NC. Note that in this mode, if the application recognizes the RS and admits the RS, the application may also provide the Node Key of the RS to the NL of the NC (otherwise, the default Node Key configured in the NC will be used).
S/N Range or Application Mode	When an admission request arrives to the NL of the NC from an RS, the NC attempts to admit the RS using the S/N Range mode. If the RS is rejected at the S/N Range mode, the NC uses the Application Mode admission mode to admit the RS.

Logical Addressing Management

The logical addressing management services are responsible for ensuring that each node is assigned with a unique logical address. The logical addressing management services consist of:

- Allocating logical addresses to nodes that guarantee unique logical address within a physical network (where are a logical address is the combination of Network ID and Node ID).
- Maintaining logical addressing uniqueness and resolving conflicts (both Network ID and Node ID).

3.4.2.3.2 Dynamic Routing

The NL creates a tree topology in which RS and NC maintain an optimal symmetric bi-directional route between them (in terms of number of hops from NC).

The NL dynamic routing services are:

- **Route Discovery**: Each RS discovers its route to the NC and vice versa.
- **Route Maintenance**: Each RS maintains the integrity of its route to the NC and vice versa.
- **Route Optimization**: The route to the NC is continuously optimized, by searching and selecting shorter routes to the NC.
- **NC Reset Recovery**: When powered up, the NC retrieves the last known topology from its non-volatile memory.

3.5 HOST INTERFACE

The IT900 Protocol Controller Architecture version is accompanied by Yitran's Y-Net protocol stack pre-firmware. In this mode, the device operates as a PLC modem chip with interface to an external host application. The external host application is required to implement the application layer functionality. The host controller connects to the IT900 through a full-duplex UART physical interface. A command set provides the logical interface from the host application to the IT900 network layer.

The following sections detail the physical host connection and provide an overview of the command set and logical interface, which are described further in the IT900 Host Interface Command Set User Guide (IT900-UM-001-R1.0).

3.5.1 Application Host Connection

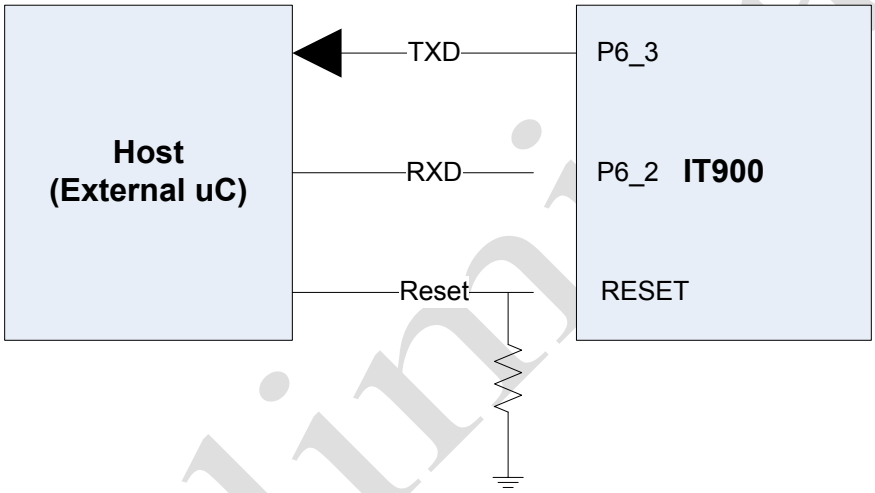


Figure 17: Host Connection

Table 3.8: Host Interface Pins

Pin Name	Pin Number	Interface Function	Description
P6_3	67	TXD	UART data output (IT900 → Host)
P6_2	68	RXD	UART data input (Host → IT900)
RESET	10	RESET	RESET (active low)

The communication parameters of the UART Host interface are set to the values listed in the table below:

Table 3.9: Host Interface Parameters

Parameter	Value
Communication Rate [bps]	960000 or 38400
Data [bits]	8
Parity [bits]	0
Stop [bits]	1
Flow Control	Off

Fast/Slow baud rate select:
uC which don't support fast UART baud rates may use P6_0 to select slow baud rate mode.
P6_0 selects the fast/slow UART baud rate:
P6_0 = '1': Fast baud rate (default value is 960000)
P6_0 = '0': Slow baud rate (default value is 38400)

3.5.2 Communication Guidelines

The host software should follow the implementation guidelines described below.

- **Full-Duplex Operation:** Communication over the UART interface is full duplex. While the host transfers data to the IT900, the IT900 may at the same time transfer data to the host. Therefore the host software should be designed to handle full-duplex communication.

- **Command Response:** The IT900 transmits a response to each received host command. While waiting for a command response, the host software should still be able to handle data packets received from the IT900.

- **Unique Task:** The host may only issue a single task to the IT900 at a time. This means that the host should not issue a new command until the command response of the previous command has been received from the IT900.

3.5.3 IT900 Initialization – First Power-On

Upon the **very first power-on**, the default values stored in the IT900 code are loaded and stored in both the on-chip RAM and the non-volatile (NV) memory storage.

The Host controller may change these values using the proper commands. The Host uses the "Set Device Parameters" command to change parameter values in the on-chip RAM and the "Save Device Parameters" command to store them in the NV memory. The new values override those previously stored in the NV

memory and will be loaded after subsequent RESET or power-on events. Values that were changed only in the RAM will not be retained after RESET.

3.5.4 Host Initial Actions

The host is required to implement the actions described in this section in order to properly communicate over the power line. For further details, see the IT900-V1 Host Interface Command Set User Guide (IT900-UM-001-R1.0).

1. **Device Reset:** A RESET indication is issued to the host upon every reset of the IT900, including Power-On. The Host should detect this indication to validate proper wake-up of the device.
2. **Parameter Configuration:** The initialization process of the IT900 includes configuration of parameters for all nodes type and a separate configuration for the BST and for RMT.
3. **Save Parameters to NV Memory:** Save parameter settings by sending the "Save Device Parameters" command. Once the parameters are stored, the IT900 will retrieve the required settings from the NV memory storage on each subsequent power-on or reset.
4. **Online Mode:** Set the device to an online mode by sending the "Go Online" command. Once the device is online, the NL processes will begin.

3.5.5 Command Set General Description

The Host interface supports three packet types:

- **Request:** A Request packet is sent from an Upper Layer application to the NL to request a service be initiated.
- **Response:** A Response packet is sent from the NL to the Upper Layer application in response to the Request.
- **Indication:** An Indication packet is sent by the NL when it has to inform the Upper Layer of significant NL events (for example, admission result).

The Interface Commands are seperated into a number of groups:

- **Embedded Services Commands:** These commands provide interface to cross-layer and general services, such as Free Memory, Write/Read from NV Memory, Get Version, etc.
- **Stack Services Commands:** These commands provide interface to cross-layer services required by the Y-NET stack, such as Reset, Go Online, etc.
- **Configuration and Monitoring Commands:** These commands set, get or save parameters from one of the IT900 configuration tables.
- **NL Management Commands and Indications:** These commands monitor the NL Management Database, interface to NL Management services that require information from upper layers (set Private Key, Admission Response, etc.) and report significant NL Management events (Admission Result, Connected to NC, and Disconnected from NC).
- **NL Data Commands and Indications:** These commands handle transmission and reception of data packets. They also provide access to the routing tables.

4 CLOCK CONFIGURATION

4.1 CLOCK CIRCUIT

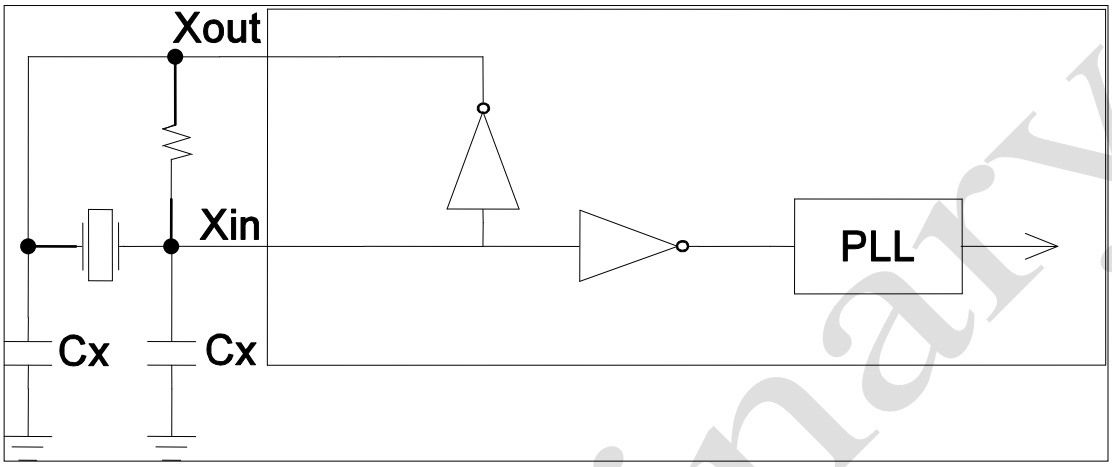


Figure 18: Clock Circuit

Notes:

1. The recommended value for Cx should be taken from the IT900 reference design.
2. The crystal should be located as close as possible to the Xin and Xout pins.

5 RESET CONFIGURATION

5.1 INTRODUCTION

The following resets can be used to reset the MCU: hardware reset, power-on reset, voltage monitor 0 reset, oscillator stop detect reset, watchdog timer reset, and software reset.

Table 5.1 lists the Types of Resets; Figure 6.1 shows the Reset Circuit Block Diagram, and Table 6.2 lists the I/O Pins.

Table 5.1: Types of Resets

Reset Name	Trigger
Hardware reset	A low-level signal is applied to the RESET pin.
Power-on reset	The rise in voltage on VCC1.
Voltage monitor 0 Reset	The drop in voltage on VCC1 (reference voltage: Vdet0).
Oscillator stop detect reset	A stop in the main clock oscillator is detected.
Watchdog timer reset	The watchdog timer underflows.
Software reset	Setting the PM03 bit in the PM0 register to 1.

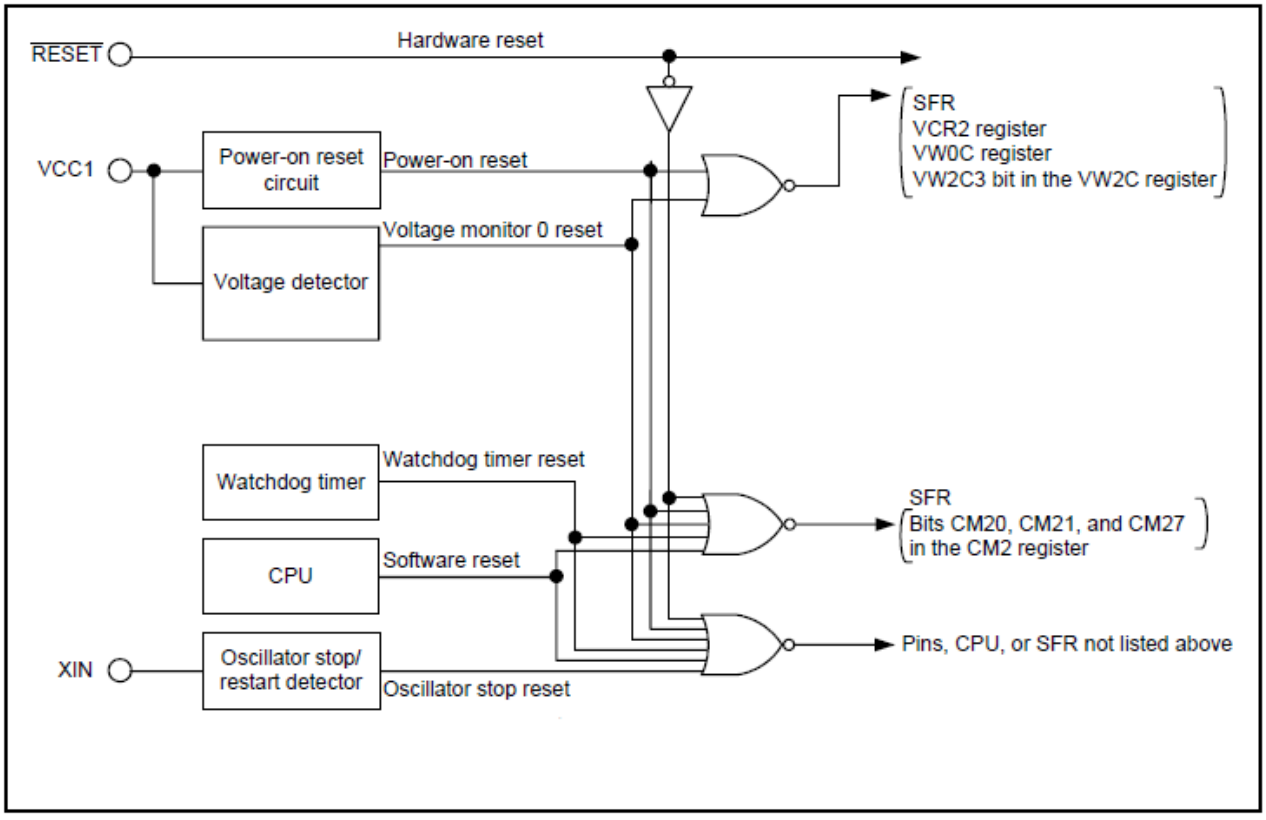


Figure 19: Reset Circuit Block Diagram

Table 5.2: I/O Pins

Pin	I/O	Function
RESET	Input	Hardware reset input.
VCC1	Input	Power input. The power-on reset and voltage monitor 0 reset are generated by monitoring VCC1.
XIN	Input	Main clock input. The oscillator stop detect reset is generated by monitoring the main clock.

5.1.1 Hardware Reset

This reset is triggered by the RESET pin. When the power supply voltage meets the recommended operating conditions, the MCU resets the pins, CPU, and SFRs when a low-level signal is applied to the RESET pin.

When changing the signal applied to the RESET pin from low to high, the MCU executes the program at the address indicated by the reset vector. fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The HWR bit in the RSTFR register becomes 1 (hardware reset detected) after hardware reset.
"Special Function Registers (SFRs)" for the rest of the SFR states after reset.

The internal RAM is not reset. When a low-level signal is applied to the RESET pin while writing data to the internal RAM, the internal RAM becomes undefined.

The procedures for generating a hardware reset are as follows:

When the power supply is stable
(1) Apply a low-level signal to the RESET pin.
(2) Wait for tw(RSTL).
(3) Apply a high-level signal to the RESET pin.

When the power is turned on
(1) Apply a low-level signal to the RESET pin.
(2) Raise the power supply voltage to the recommended operating level.
(3) Wait for td (P-R) until the internal voltage stabilizes.
(4) Wait for $\frac{1}{fOCO\text{–}S}$ × 20 cycles.
(5) Apply a high-level signal to the RESET pin.

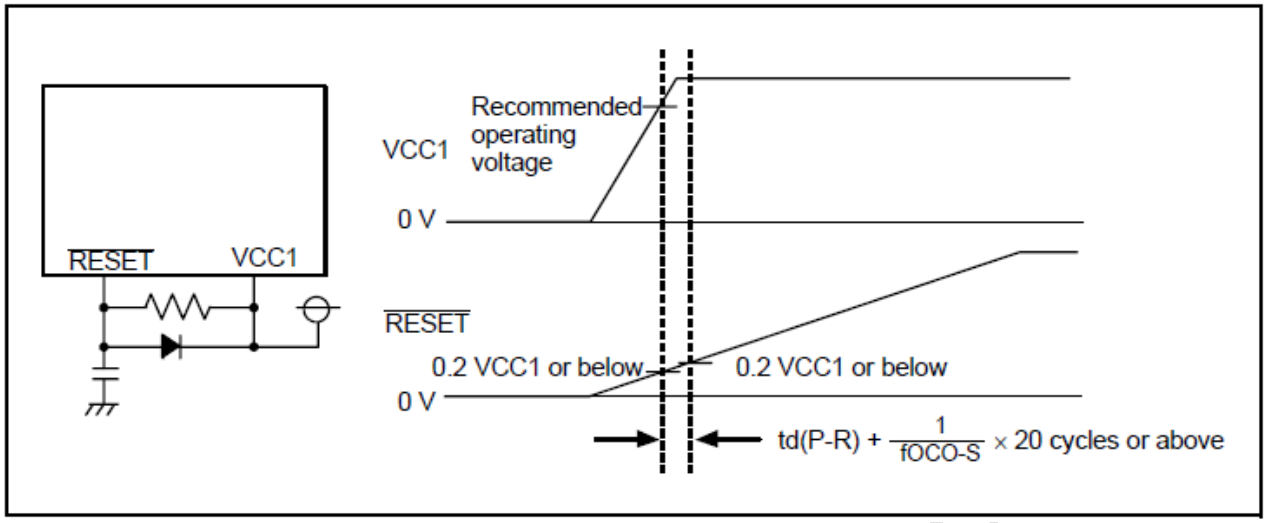


Figure 20: Reset Circuit Example

5.1.2 Power-On Reset Function

The power-on reset function can be used on the system in which VCC1 is Vdet0 or higher. When the RESET pin is connected to VCC1 via a pull-up resistor and the VCC1 voltage level rises while the rise gradient is trth or more, the power-on reset function is enabled and the MCU resets the pins, CPU, and SFRs.

When the input voltage to the VCC1 pin reaches Vdet0 or above, the fOCO-S count starts. When the fOCO-S count reaches 32, the internal reset signal becomes high and the MCU executes the program at the address indicated by the reset vector. fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The CWR bit in the RSTFR register becomes 0 (cold start) after power-on reset. Refer to 4. “Special Function Registers (SFRs)” for the remaining SFR states after reset.
The internal RAM is not reset.

Use the voltage monitor 0 reset together with the power-on reset. Set the LVDAS bit in the OFS1 address to 0 (voltage monitor 0 reset enabled after hardware reset) to use the power-on reset. In this case, the voltage monitor 0 reset is enabled (the VW0C0 bit and bit 6 in the VW0C register are 1 and the VC25 bit in the VCR2 register is 1). Do not set these bits to 0.

Figure 21 shows Power-On Reset Circuit and Operation Example. When a capacitor is connected to the RESET pin, always keep voltage to the RESET pin at 0.8 VCC1 or more.

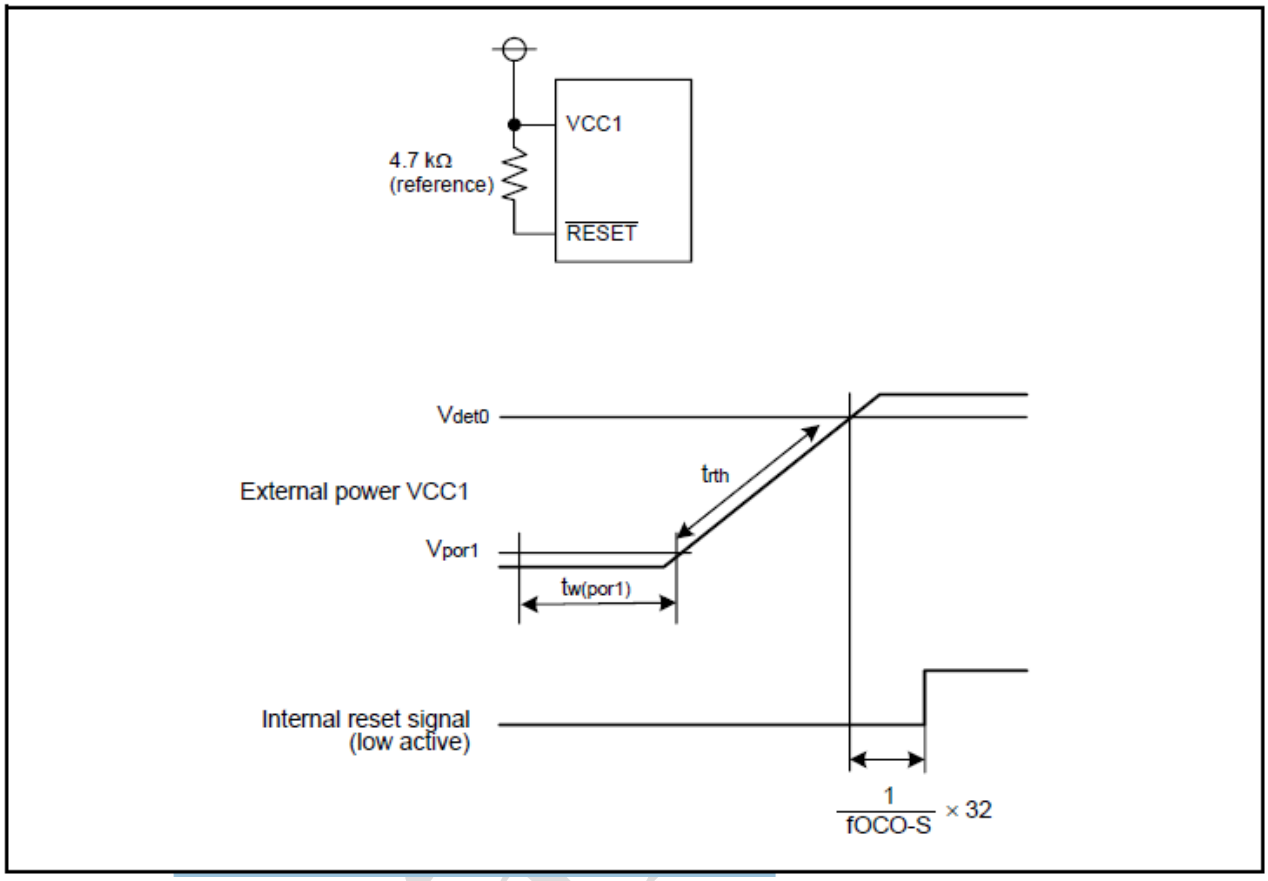


Figure 21: Power-On Reset Circuit and Operation Example

5.1.3 Voltage Monitor 0 Reset

This reset is triggered by the MCU's on-chip voltage detector 0. The voltage detector 0 monitors the voltage applied to the VCC1 pin (Vdet0). The MCU resets the pins, CPU, and SFRs when the voltage applied to the VCC1 pin drops to Vdet0 or below.

The fOCO-S count starts when the voltage applied to the VCC1 pin rises to Vdet0 or above. The internal reset signal becomes high after 32 cycles of fOCO-S, and then the MCU executes the program at the address indicated by the reset vector. fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The CWR bit in the RSTFR register becomes 0 (cold start) after voltage monitor 0 reset. The internal RAM is not reset. When the voltage applied to the VCC1 pin drops to Vdet0 or below while writing data to the internal RAM, the internal RAM becomes undefined.

5.1.4 Oscillator Stop Detect Reset

The MCU resets and stops the pins, CPU, and SFRs when the CM27 bit in the CM2 register is 0 (reset when oscillator stop detected), if it detects that the main clock oscillator has stopped.

The OSDR bit in the RSTFR register becomes 1 (oscillator stop detect reset detected) after oscillator stop detect reset. Some SFRs are not reset at oscillator stop detect reset.

The internal RAM is not reset. When the main clock oscillator stop is detected while writing data to the internal RAM, the internal RAM becomes undefined.

Oscillator stop detect reset is canceled by hardware reset or voltage monitor 0 reset.

5.1.5 Watchdog Timer Reset

The MCU resets the pins, CPU, and SFRs when the PM12 bit in the PM1 register is 1 (reset when watchdog timer underflows) and the watchdog timer underflows. Then the MCU executes the program at the address determined by the reset vector. fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The WDR bit in the RSTFR register becomes 1 (watchdog timer reset detected) after watchdog timer reset. Some SFRs are not reset at watchdog timer reset.
The internal RAM is not reset. When the watchdog timer underflows while writing data to the internal RAM, the internal RAM becomes undefined.

5.1.6 Software Reset

The MCU resets the pins, CPU, and SFRs when the PM03 bit in the PM0 register is 1 (MCU reset). Then the MCU executes the program at the address determined by the reset vector. fOCO-S divided by 8 is automatically selected as the CPU clock after reset.

The SWR bit in the RSTFR register becomes 1 (software reset detected) after software reset. Some SFRs are not reset at software reset.

The internal RAM is not reset.

5.1.7 Cold/Warm Start Discrimination

The cold/warm start discrimination detects whether or not voltage applied to the VCC1 pin drops to the RAM hold voltage or below. The reference voltage is Vdet0. Therefore, the voltage monitor 0 reset is used for cold/warm start discrimination.

The CWR bit in the RSTFR register is 0 (cold start) when power is turned on. The CWR bit also becomes 0 after power-on reset or voltage monitor 0 reset. The CWR bit becomes 1 (warm start) by writing 1, and remains unchanged at hardware reset, oscillator stop detect reset, watchdog timer reset, or software reset.

In the cold/warm start discrimination, the Vdet0 level can be selected by setting the VDSEL1 bit in the OFS1 address.

- When power-on reset or voltage monitor 0 reset is used, set the VDSEL1 bit to 0 (Vdet0 = 2.85 V (Vdet0_2)).
- When neither power-on reset nor voltage monitor 0 reset is used as the user system, set the VDSEL1 bit to 1 (Vdet0 = 1.90 V (Vdet0_0)). In this case, voltage monitor 0 reset and its cancellation are based on Vdet0_0. Therefore, execute hardware reset after cancelling the voltage monitor 0 reset.

Figure 22 shows the Cold/Warm Start Discrimination example.

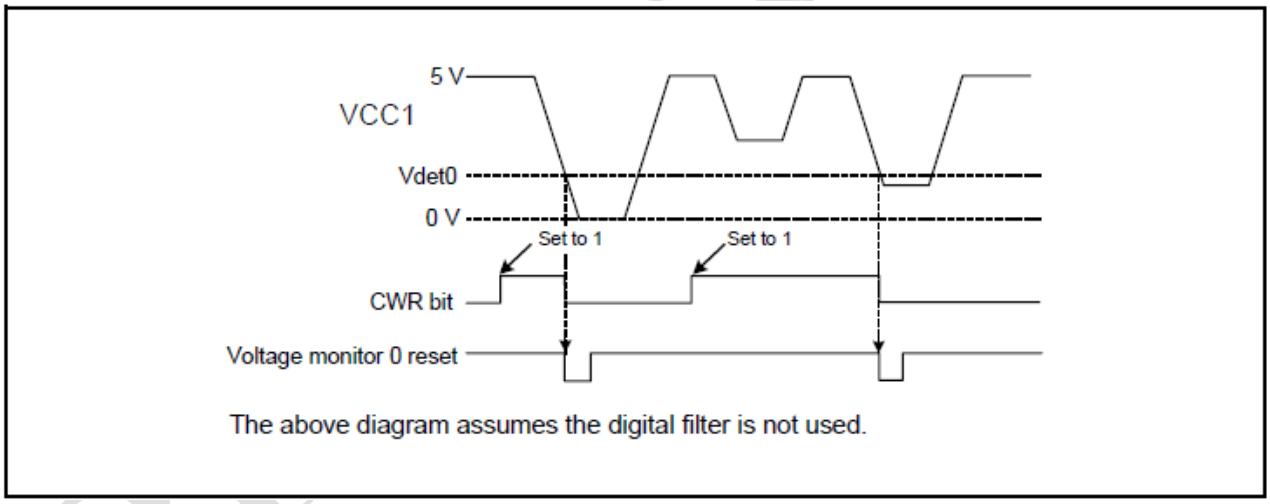


Figure 22: Cold/Warm Start Discrimination

5.2 NOTES ON RESETS

5.2.1 Power Supply Rising Gradient

When supplying power to the MCU, make sure that the power supply voltage applied to the VCC1 pin meets the SVCC conditions.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
SVCC	Power supply VCC1 rising gradient (Voltage range: 0 V to 2.0 V)	0.05			V/ms

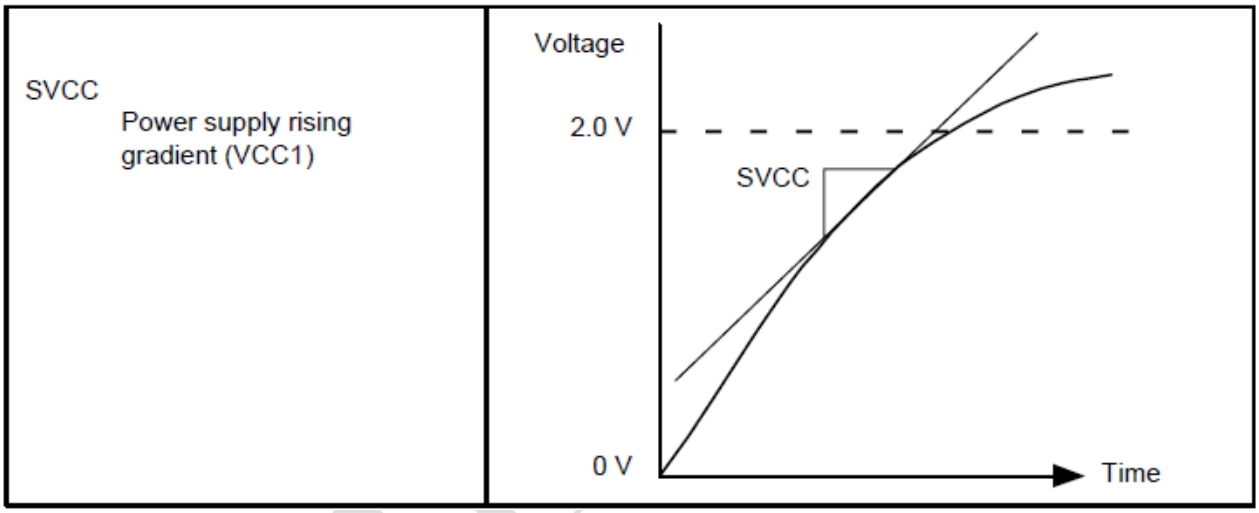


Figure 23: SVCC Timing

5.2.2 Power-On Reset

Use the voltage monitor 0 reset together with the power-on reset. To use the power-on reset, set the LVDAS bit in the OFS1 address to 0 (voltage monitor 0 reset enabled after hardware reset). In this case, the voltage monitor 0 reset is enabled (the VW0C0 bit and bit 6 in the VW0C register are 1, and the VC25 bit in the VCR2 register is 1) after power-on reset. Do not disable these bits.

5.2.3 OSDR Bit (Oscillation Stop Detect Reset Detection Flag)

When an oscillation stop detect reset is generated, the MCU is reset and then stopped. This state is canceled by hardware reset or voltage monitor 0 reset.

Note that the OSDR bit in the RSTFR register value is not affected by a hardware reset, but becomes 0 (not detected) from a voltage monitor 0 reset.

5.3 NON VOLATILE MEMORY

5.3.1 Overview

The Non-Volatile Memory holds all the IT900's configurable parameters and sustainable data. There are two options for Non-Volatile storage: Internal Flash and External EEPROM. Internal Flash is a lower-cost option, but has the disadvantage of limited memory space and number of erase cycles. The use of the internal Flash is most appropriate for RMT devices, while the use of external EEPROM is advised for BST devices.

5.4 EEPROM APPLICATION CIRCUIT

The EEPROM is mandatory for IT900 NC and for any application that requires Remote Version Download support (firmware upgrade through power line).
For a RS or for any application which does not rely on IT900 YNET Network Layer, the EEPROM is optional.
When using an EEPROM, a 24Cxx serial EEPROM is recommended. The required EEPROM connection to the IT900 is shown in the following figure:

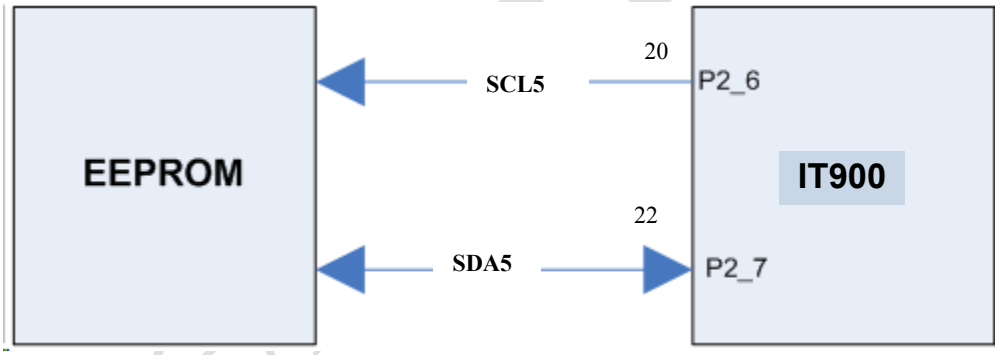


Figure 24: IT900 to EEPROM Connection

Note: The EEPROM device used must have a 64-Byte page write mode.

5.5 APPLICATION CIRCUIT

Figure 25 below shows a typical schematic connections for the IT900 application circuit (the EEPROM is optional – see section 5.4).

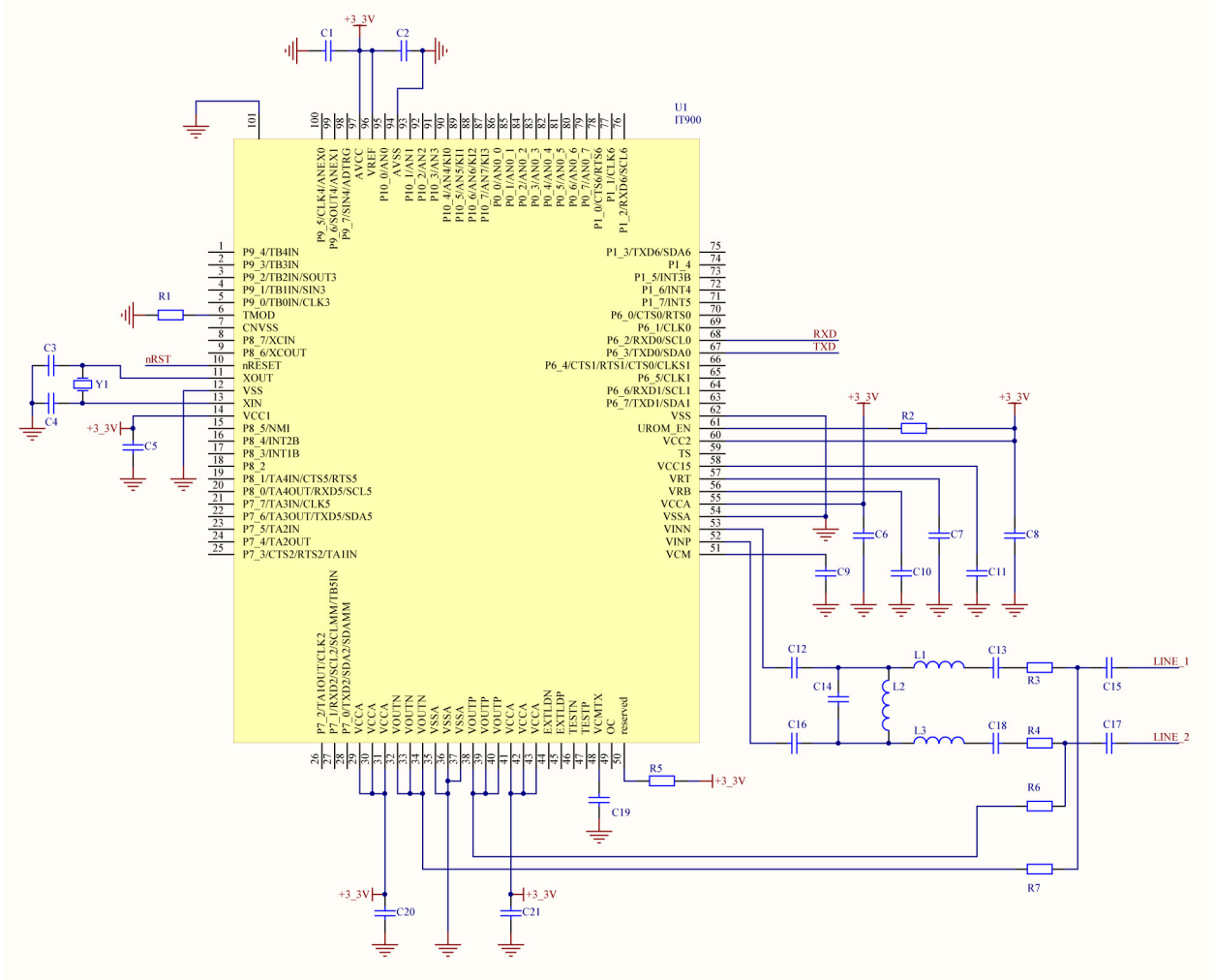


Figure 25: IT900 Typical Application Circuit

6 ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM OPERATING CONDITIONS

Table 6.1: Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
VCC1	Supply voltage		VCC1= AVCC	-0.3 to 4.6	V
VCC2	Supply voltage		VCC1= AVCC	-0.3 to VCC1 + 0.1 (*)	V
VCCA	Supply voltage			-0.3 to 4.6	V
AVCC	Analog supply voltage		VCC1= AVCC	-0.3 to 4.6	V
VREF	Analog supply voltage		VCC1= AVCC	-0.3 to VCC1 + 0.1 (*)	V
VI	Input voltage	RESET, CNVSS, TMOD P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN		-0.3 to VCC1 + 0.3 (*)	V
		P0_0 to P0_7, P1_0 to P1_7, P6_0 to P6_7, UROM_EN		-0.3 to VCC2 + 0.3 (*)	V
		P7_0, P7_1, P8_5		-0.3 to 4.6	V
		VINP, VINN, TESTP, TESTN, OC_EN		-0.3 to VCCA + 0.3(*)	V
VO	Output voltage	P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, XOUT		-0.3 to VCC1 + 0.3 (*)	V
		P0_0 to P0_7, P1_0 to P1_7, P6_0 to P6_7, TS		-0.3 to VCC2 + 0.3 (*)	V
		P7_0, P7_1, P8_5		-0.3 to 4.6	V
		VOUTP, VOUTN, EXTLDP, EXTLDN, VCM, VCMTX, VRT, VRB, TESTP, TESTN, OC		-0.3 to VCCA + 0.3(*)	V
		VCC15		-0.3 to 2.0	V
Pd	Power consumption		−40°C ≤ Topr ≤ 85°C	1000	V
Topr	Operating temperature	When MCU is operating		-40 to 85	mW
		Flash program erase		-40 to 85	ºC
Tstg	Storage temperature			-65 to 150	ºC

* Maximum value is 4.6 V.

6.2 RECOMMENDED OPERATING CONDITIONS

Table 6.2: Recommended Operating Conditions (1/4)

VCC1 = VCC2 = 2.7 to 3.6 V at Topr = -40 to 85°C unless otherwise specified.

Symbol	Parameter			Standard			Unit
				Min	Type	Max	
VCC1	Supply voltage	PLC operation	VCC1 = VCC2 = VCCA	3.0		3.6	V
		No PLC operation	VCC1 = VCC2 = VCCA	2.7		3.6	
VCC2	Supply voltage		VCC1 = VCC2 = VCCA		VCC1		V
VCCA	Supply voltage		VCC1 = VCC2 = VCCA		VCC1		V
AVCC	Analog supply voltage				VCC1		V
VSS	Supply voltage						
VSSA	Supply voltage				0		
AVSS	Analog supply voltage				0		V
VIH	High input voltage	P0_0 to P0_7, P1_0 to P1_7, P6_0 to P6_7, UROM_EN		0.8 VCC2	0	VCC2	V
		P7_2 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, TMOD		0.8 VCC1		VCC1	V
		P7_0, P7_1, P8_5		0.8 VCC1		4.6	V
		OC_EN		0.8VCCA		VCCA	V
VIL	Low input voltage	P0_0 to P0_7, P1_0 to P1_7, P6_0 to P6_7, UROM_EN		0		0.2 VCC2	V
		P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, XIN, RESET, CNVSS, TMOD		0		0.2 VCC1	V
		OC_EN		0		0.2 VCCA	V

Table 6.3: Recommended Operating Conditions (2/4)

VCC1 = VCC2 = 2.7 to 3.6 V at Topr = -40 to 85°C unless otherwise specified.

Symbol	Parameter		Standard			Unit
			Min	Type	Max	
IOH(sum)	High peak sum output current	Sum of IOH(peak) at P0_0 to P0_7, P1_0 to P1_7, P6_0 to P6_7			-40.0	mA
		Sum of IOH(peak) at P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			-40.0	mA
IOH(peak)	High peak output current	P0_0 to P0_7, P1_0 to P1_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			-10.0	mA
IOH(avg)	High average output current (*)	P0_0 to P0_7, P1_0 to P1_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7			-5.0	mA
IOL(sum)	Low peak sum output current	Sum of IOL(peak) at P0_0 to P0_7, P1_0 to P1_7, P6_0 to P6_7			80.0	mA
		Sum of IOL(peak) at P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7			80.0	mA
IOL(peak)	Low peak output current	P0_0 to P0_7, P1_0 to P1_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7			10.0	mA
IOL(avg)	Low average output current (*)	P0_0 to P0_7, P1_0 to P1_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7			5.0	mA

*The average output current is the mean value within 100 ms.

Table 6.4: Recommended Operating Conditions (3/4)

VCC1 = VCC2 = 2.7 to 3.6 V at Topr = -40 to 85°C unless otherwise specified.

Symbol	Parameter		Standard			Unit
			Min	Type	Max	
f(XIN)	Main clock oscillation frequency			15.36		MHz
f(XCIN)	Sub clock oscillation frequency		30	32.768	35	kHz
f(PLL)	PLL clock oscillation frequency	VCC = 2.7 to 2.6 V	11.52		30.72	MHz
f(BCLK)	CPU operation clock		2		32	MHz
fsu(PLL)	PLL frequency synthesizer stabilization wait time	VCC1 = 3.0 V			3	ms

Table 6.5: Recommended Operating Conditions (4/4)*

VCC1 = VCC2 = 2.7 to 3.6 V, Vss = 0 V, and Topr = -40 to 85°C unless otherwise specified.
The ripple voltage must not exceed Vr(VCC1) and/or dVr(VCC1)/dt.

Symbol	Parameter	Standard			Unit
		Min	Type	Max	
Vr(VCC1)	Allowable ripple voltage			0.3	Vp-p
dVr(VCC1)/dt	Ripple voltage failing gradient			0.3	V/ms

*The device is operationally guaranteed under these operating conditions.

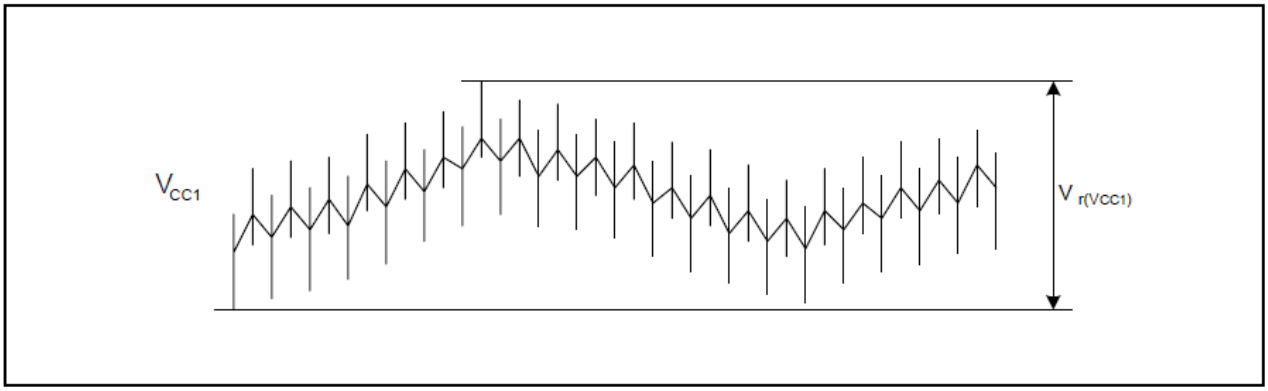


Figure 26: Ripple Waveform

6.3 A/D Conversion Characteristics

Table 6.6: A/D Conversion Characteristics (1/2)*

AVCC = VCC1 = VCC2 = 2.7 to 3.6 V ≥ VREF, VSS = AVSS = 0 V at Topr = -40 to 85°C unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min	Type	Max	
-	Resolution		AVCC = VCC1 = VCC2 ≥ VREF			10	Bits
INL	Integral non-linearity error	10 bit	AN0 to AN7 input, AN0_0 to AN0_7 input, ANEX0, ANEX1 input**			±3	LSB
-	Absolute accuracy	10 bit	AN0 to AN7 input, AN0_0 to AN0_7 input, ANEX0, ANEX1 input**			±3	LSB

*Use when AVCC = VCC1.
**Flash memory rewrite disabled. Except for the analog input pin, set pins to be measured as input ports and connect them to VSS. See Figure 27.

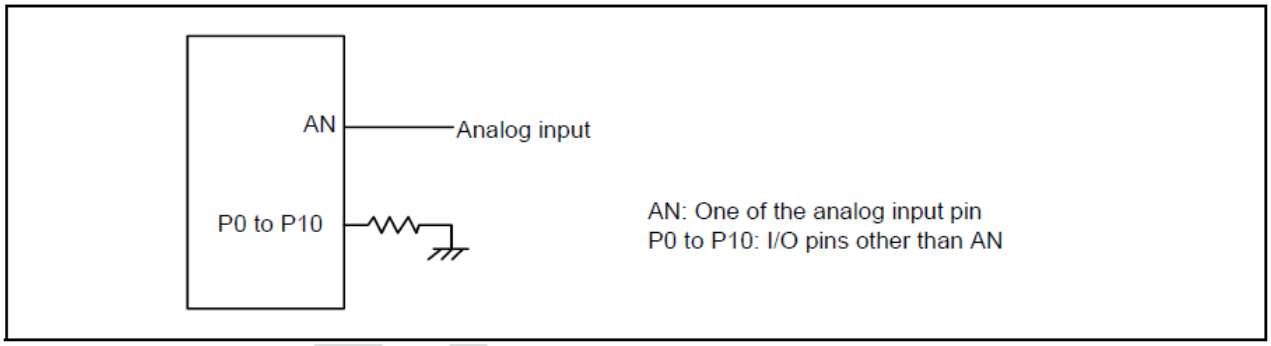


Figure 27: A/D Accuracy Measure Circuit

Table 6.7: A/D Conversion Characteristics (2/2)*

AVCC = VCC1 = VCC2 = 2.7 to 3.6 V ≥ VREF, VSS = AVSS = 0 V at Topr = -40 to 85°C unless otherwise specified.

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min	Type	Max	
ϕ AD	A/D operating clock frequency	3.2 V ≤ VREF ≤ AVCC ≤ 3.6 V	2		15.36	MHz
		3.0 V ≤ VREF ≤ AVCC ≤ 3.6 V	2		11.52	MHz
		2.7 V ≤ VREF ≤ AVCC ≤ 3.6 V	2		5.72	MHz
-	Tolerance level impedance			3		kΩ
DNL	Differential non-linearity error	***			±1	LSB
-	Offset error	***			±3	LSB
-	Gain error	***			±3	LSB
tCONV	10-bit conversion time	VCC1 = 3.3 V, φAD = 15.36 MHz	2.8			µs
tSAMP	Sampling time		0.98			µs
VREF	Reference voltage		2.7		VCC1	V
VIA	Analog input voltage**		0		VREF	V

*Use when AVCC = VCC1=VCC2.
** When analog input voltage is over reference voltage, the result of A/D conversion is 3FFh.
***Flash memory rewrite disabled. Except for the analog input pin, set pins to be measured as input ports and connect them to VSS. See Figure 27

6.4 FLASH MEMORY ELECTRICAL CHARACTERISTICS

Table 6.8: CPU Clock When Operating Flash Memory

VCC1 = 2.7 to 3.6 V, Topr = -40 to 85°C unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min	Type	Max	
-	CPU rewrite mode				10*	MHz
f(SLOW_R)	Slow read mode				5	MHz
-	Low current consumption read mode			fC(32.768)	35	kHz
-	Data flash read	3.0 V < VCC1 < 3.6 V			20**	MHz
		2.7 V ≤ VCC1 ≤ 3.0 V			16**	MHz

* Set the PM17 bit in the PM1 register to 1 (one wait).
** When the frequency is over this value, set FMR17 bit in the FMR1 register to 0 (one wait) or the PM17 bit in the PM1 register to 1 (one wait).

Table 6.9: Flash Memory (Program ROM 1, 2) Electrical Characteristics

VCC1 = 2.7 to 3.6 V, Topr = -40 to 85°C unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min	Type	Max	
-	Program and erase cycles (1, 3, 4)	VCC1 = 3.3 V, Topr = 25°C	1,000 (2)			times
-	Two words program time	VCC1 = 3.3 V, Topr = 25°C		150	4000	µs
-	Lock but program time	VCC1 = 3.3 V, Topr = 25°C		70	3000	µs
-	Block erase time	VCC1 = 3.3 V, Topr = 25°C		0.2	3.0	s
td(SR-SUS)	Time delay from suspend request until suspend				5 + CPU clock × 3 cycles	ms
-	Interval from erase start/restart until following suspend request		0			µs
-	Suspend interval necessary for auto-erasure to complete (7)		20			Ms
-	Time from suspend until erase restart				30 + CPU clock × 1 cycle	µs
-	Program, erase voltage		2.7		3.6	V

-	Read voltage		2.7		3.6	V
-	Program, erase temperature		0		60	°C
tPS	Flash Memory Circuit Stabilization Wait Time				50	µs
-	Data hold time (6)	Ambient temperature = 55 °C	20			year

Notes:
1. Definition of program and erase cycles: The program and erase cycles refer to the number of per-block erasures. If the program and erase cycles are n (n = 1,000), each block can be erased n times. For example, if a 64 Kbyte block is erased after writing two word data 16,384 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. It is advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, and then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas Electronics support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

Table 6.10: Flash Memory (Data Flash) Electrical Characteristics

VCC1 = 2.7 to 3.6 V, Topr = -40 to 85°C unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min	Type	Max	
-	Program and erase cycles (1, 3, 4)	VCC1 = 3.3 V, Topr = 25°C	10,000 (2)			times
-	Two words program time	VCC1 = 3.3 V, Topr = 25°C		300	4000	µs
-	Lock but program time	VCC1 = 3.3 V, Topr = 25°C		140	3000	µs
-	Block erase time	VCC1 = 3.3 V, Topr = 25°C		0.2	3.0	s
td(SR-SUS)	Time delay from suspend request until suspend				5 + CPU clock × 3 cycles	ms
-	Interval from erase start/restart until following suspend request		0			µs
-	Suspend interval necessary for auto-erase to complete (7)		20			Ms
-	Time from suspend until erase restart				30 + CPU clock × 1 cycle	µs
-	Program, erase voltage		2.7		3.6	V
-	Read voltage		2.7		3.6	V
-	Program, erase temperature		-20/-40		85	°C
tPS	Flash Memory Circuit Stabilization Wait Time				50	µs
-	Data hold time (6)	Ambient temperature = 55 °C	20			year

Notes:
1. Definition of program and erase cycles. The program and erase cycles refer to the number of per-block erasures. If the program and erase cycles are n (n = 10,000), each block can be erased n times. For example, if a 4 Kbyte block is erased after writing two word data 1,024 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 256 groups before erasing them all in one operation. In addition, averaging the erasure cycles between blocks A and B can further reduce the actual erasure cycles. It is also advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

6.5 VOLTAGE DETECTOR AND POWER SUPPLY CIRCUIT ELECTRICAL CHARACTERISTICS

Table 6.11: Voltage Detector 0 Electrical Characteristics

The measurement condition is VCC1 = 2.7 to 3.6 V, Topr = -40 to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min	Type	Max	
Vdet0	Voltage detection level Vdet0_0 (1)	When VCC1 is falling.	1.80	1.90	2.10	V
	Voltage detection level Vdet0_2 (1)	When VCC1 is falling.	2.70	2.85	3.00	V
-	Voltage detector 0 response time (3)	When VCC1 falls from 3.6 V to (Vdet0_0 - 0.1) V			200	µs
-	Voltage detector self power consumption	VC25 = 1, VCC1 = 3.3 V		1.5		µA
td(E-A)	Waiting time until voltage detector operation starts (2)				100	µs

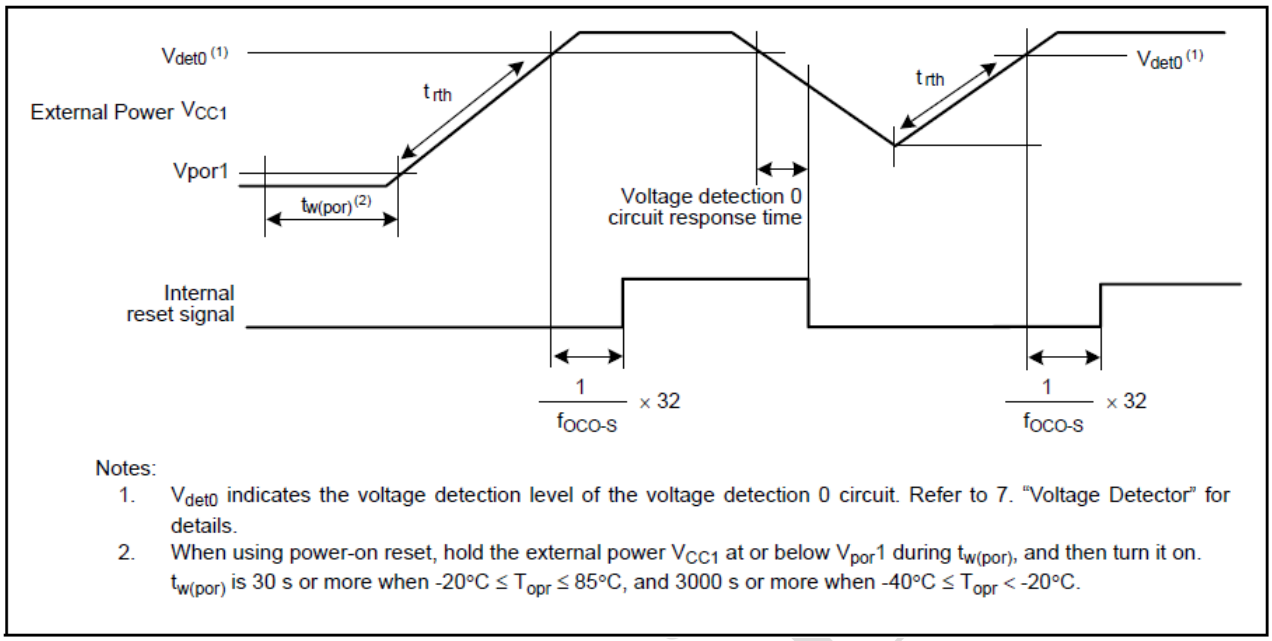
Notes:
1. Select the voltage detection level with the VDSEL1 bit in the OFS1 address.
2. Necessary time until the voltage detector operates when setting to 1 again after setting the VC25 bit in the VCR2 register to 0.
3. Time from when passing the Vdet0 until when a voltage monitor 0 reset is generated.

Table 6.12: Power-On Reset Circuit

The measurement condition is VCC1 = 2.7 to 3.6 V, Topr = -40 to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min	Type	Max	
Vpor1	Voltage at which power-on reset enables*				0.1	V
Trth	External power VCC1 rise gradient		2.0	1.5	50000	mV/ms

* To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS but in the OFS1 address to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to 7. "Voltage Detector" for details.
2. When using power-on reset, hold the external power V_{CC1} at or below $V_{por}1$ during $t_{w(por)}$, and then turn it on. $t_{w(por)}$ is 30 s or more when $-20°C \le T_{opr} \le 85°C$, and 3000 s or more when $-40°C \le T_{opr} < -20°C$.

Figure 28: Power-On Reset Circuit Electric Characteristics

Table 6.13: Power Supply Circuit Timing Characteristics

The measurement condition is VCC1 = 2.7 to 3.6 V and Topr = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min	Type	Max	
td(P-R)	Internal power supply stability time when power is on*				5	Ms
td(R-S)	STOP release time				150	µs
td(W-S)	Low power mode wait mode release time				150	µs

* Waiting time until the internal power supply generator stabilizes when power is on

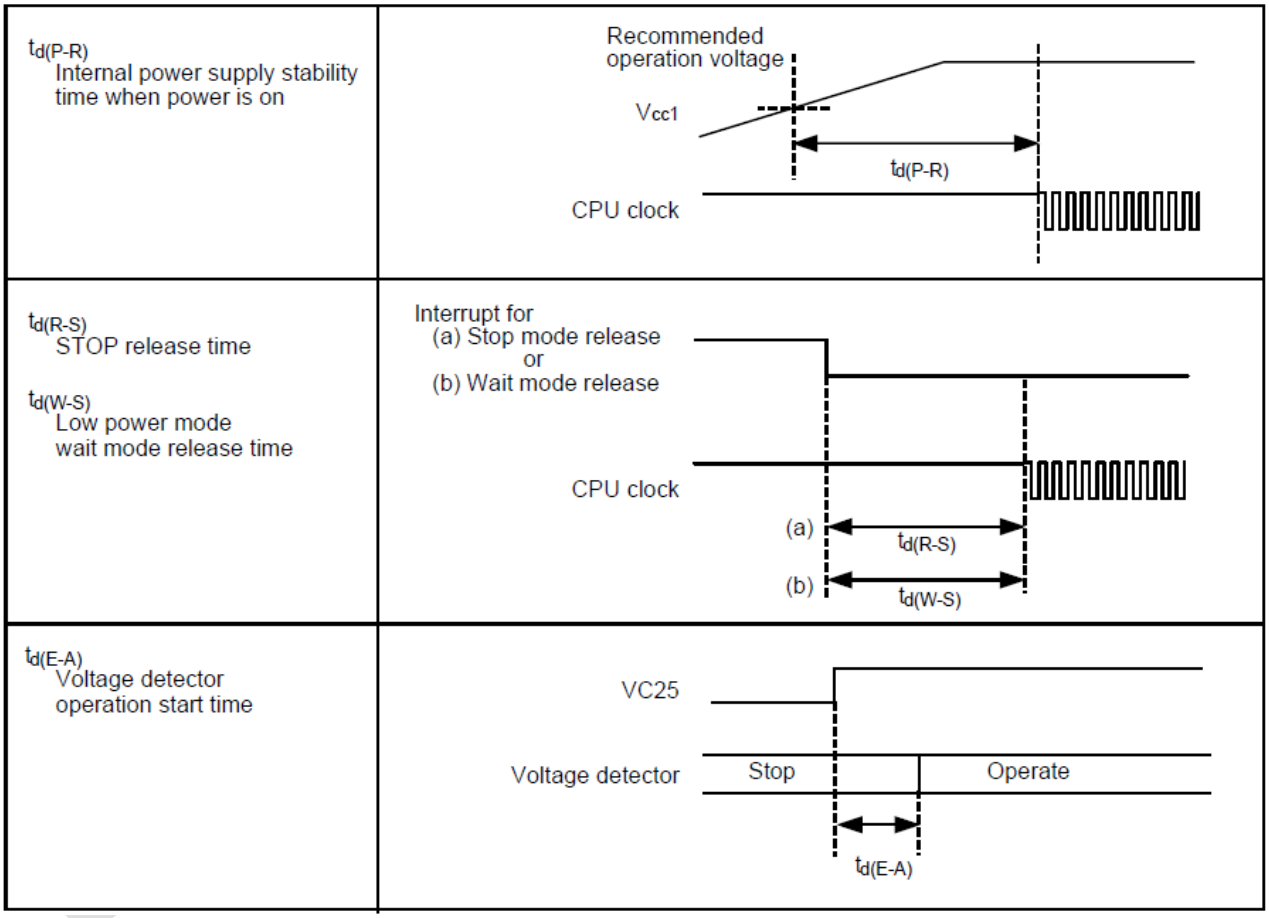


Figure 29: Power Supply Circuit Timing Diagram.

6.6 Oscillation Circuit Electrical Characteristics

Table 6.14: 125 kHz On-Chip Oscillator Circuit Electrical Characteristics

VCC1 = 2.7 to 3.6 V, Topr = -40 to 85°C unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min	Type	Max	
tOCO-S	125 kHz on-chip oscillator frequency	Average frequency in a 10 ms period	100	125	150	kHz
tsu(fOCO-S)	Wait time until 125 kHz on-chip oscillator stabilizes				20	µs

6.7 Analog Front End Electrical Characteristics

Table 6.15: AFE Electrical Characteristics

VCCA = 3.3 V, VSSA = 0 V, Topr = 25°C unless otherwise specified.

Symbol	Condition/Comments	Standard			Unit
		Min	Type	Max	
Analog supply voltage	VCCA	3.0	3.3	3.6	V
Digital supply voltage (internal output regulator supply)	VCCA		1.5	1.65	V
DC reference voltage	VCMTX	1.5	1.65	1.8	V
	VCM		1.5		V
Analog power supply current	VCCA = 3.3 V Load resistance = 1 Ω			700	mARMS
Cutoff frequency			1		MHz
Maximum output amplitude	Load resistance = 50 Ω DACVREF = 11			5*	Vpp
SFDR (Spurious Free Dynamic Range)	Load resistance = 50 Ω f = 100 KHz RBW = 9 kHz			TBD*	dBc
Output impedance	During transmission		TBD		Ω
	While transmission is stopped		TBD		Ω
Operation stop temperature	Internal silicon junction		125**		°C
Input impedance	DC		1		Kohms
Input amplitude	VINP, VINN			2	Vpp
AGC gain range	CGA	-6		42	dB
AGC gain step	VGA		6		dB

*These values are defined at M16C/6S1 Group output pin. Output amplitude and SFDR vary depending on the following conditions:
(1) Value of DACVREF.
(2) Condition of the transmission line and parameter of the coupling circuit.
**As the AFE registers are set to default. The line driver turns off at the operation stop temperature. Ensure that temperature does not exceed 125°C during operation.

6.8 Electrical Characteristics

Table 6.16: Electrical Characteristics (1)

VCC1 = VCC2 = 2.7 to 3.6 V, VSS = 0 V at Topr = -40 to 85°C, f(BCLK) = 30.72 MHz unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min	Type	Max	
VOH	High output voltage	P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	IOH = −1 mA	VCC1 − 0.5		VCC1	V
		P0_0 to P0_7, P1_0 to P1_7, P6_0 to P6_7	IOH = −1 mA	VCC2 − 0.5		VCC2	
VOH	High output voltage XOUT	High drive	IOH = −0.1 mA	VCC1 − 0.5		VCC1	V
	High output voltage XCOUT	Low drive	IOH = −50 µA	VCC1 − 0.5		VCC1	
VOL	Low output voltage	P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7	IOL = 1 mA			0.5	V
		P0_0 to P0_7, P1_0 to P1_7, P6_0 to P6_7	IOL = 1 mA			0.5	
VOL	Low output voltage XOUT	High drive	IOL = 0.1 mA			0.5	V
	Low output voltage XCOUNT	Low drive	IOL = 50 µA			0.5	
VT+-VT-	Hysteresis	TA1IN to TA4IN, TB0IN to TB5IN, INT1 to INT5, NMI, ADTRG, CTS0 to CTS2, CTS5 to CTS6, SCL0 to SCL2, SCL5 to SCL6, SDA0 to SDA2, SDA5 to SDA6, CLK0 to CLK6, TA1OUT to TA4OUT, KI0 to KI7, RXD0 to RXD2, RXD5 to RXD6, SIN3, SIN4, SCLMM, SDAMM		0.2		1.0	V

VT+-VT-	Hysteresis	RESET		0.2		1.8	V
IIH	High input current	P0_0 to P0_7, P1_0 to P1_7	VI = VCC1			4.0	µA
		P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS, TS, OC_EN	VI = VCC1			4.0	µA
IIL	Low input current	P0_0 to P0_7, P1_0 to P1_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7 XIN, RESET, CNVSS, TS, OC_EN	VI = 0 V			-4.0	µA
RPULLUP	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P6_0 to P6_7, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7	VI = 0 V			500	kΩ
RfXIN	Feedback resistance XIN						MΩ
RfXCIN	Feedback resistance XCIN						MΩ
VRAM	RAM retention voltage		In stop mode				V

Table 6.17: Electrical Characteristics (3)

VCC1 = VCC2 = 2.7 to 3.6 V, VSS = 0 V at Topr = -40 to 85°C, f(BCLK) = 30.72 MHz unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min	Type	Max	
ICC	Power supply current PLL no operation, the output pin is open and other pins are VSS	High-speed mode	f(BCLK) = 30.72 MHz XIN = 15.36 MHz, PLL operates 125 kHz on-chip oscillator stop		TBD		mA
			f(BCLK) = 15.36 MHz XIN = 15.36 MHz 125 kHz on-chip oscillator stop PLL stops		7.2		mA
		125 kHz on-chip oscillator mode	Main clock stop Sub clock stop 125 kHz on-chip oscillator on, no division FMR22 = 1 (slow read mode)		300		µA
		Low-power mode	f(BCLK) = 32 kHz FMR 22 = FMR23 = 1 (in low-current consumption read mode) On flash memory*		80.0		µA
			f(BCLK) = 30.72 kHz XIN = 15.36 MHz, PLL operates 125 kHz on-chip oscillator stop Topr = 25°C				
		Wait mode	f(BCLK) = 32 kHz, Xein = 32 kHz Main clock stop 125 kHz on-chip oscillator on PM25 = 1 (peripheral function clock fC operating) Topr = 25°C Real-time clock operating		TBD		µA
			f(BCLK) = 32 kHz Main clock stop 125 kHz on-chip oscillator stop		8		µA

			PM25 = 0 (peripheral function clock fC stop) Topr = 25°C				
		Stop mode	Main clock stop Sub clock stop 125 kHz on-chip oscillator on, no division peripheral function clock fC stop		TBD		µA
		During flash memory program	f(BCLK) = 7.68 MHz, PM17 = 1 (one wait) VCC1 = 3.3 V		20.0		mA
		During flash memory erase	f(BCLK) = 7.68 MHz, PM17 = 1 (one wait) VCC1 = 3.3 V		30.0		mA

* This indicates the memory in which the program to be executed exists.

6.9 Timing Requirements (Peripheral Functions and Others)

(VCC1 = VCC2 = 2.7~3.6 V, VSS = 0 V, at Topr = -40 to 85°C unless otherwise specified)

6.9.1 Reset Input (RESET Input)

Table 6.18: Reset Input (RESET Input)

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(RSTL)	RESET input low pulse width	10		µs

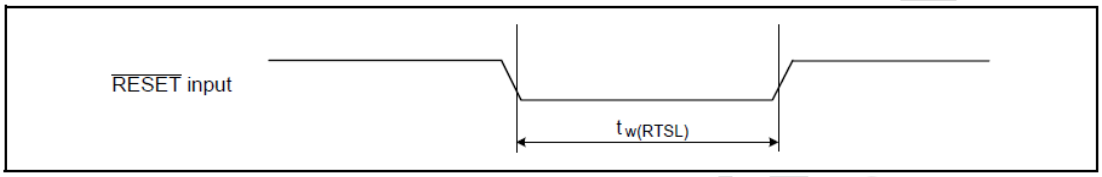


Figure 30: Reset Input (RESET Input)

6.9.2 Timer A Input

Table 6.19: Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAiIN input cycle time	150		ns
tw(TAH)	TAiIN input high pulse width	60		ns
tw(TAL)	TAiIN input low pulse width	60		ns

Table 6.20: Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAiIN input cycle time	600		ns
tw(TAH)	TAiIN input high pulse width	300		ns
tw(TAL)	TAiIN input low pulse width	300		ns

Table 6.21: Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAiIN input cycle time	300		ns
tw(TAH)	TAiIN input high pulse width	150		ns
tw(TAL)	TAiIN input low pulse width	150		ns

Table 6.22: Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(TAH)	TAiIN input high pulse width	150		ns
tw(TAL)	TAiIN input low pulse width	150		ns

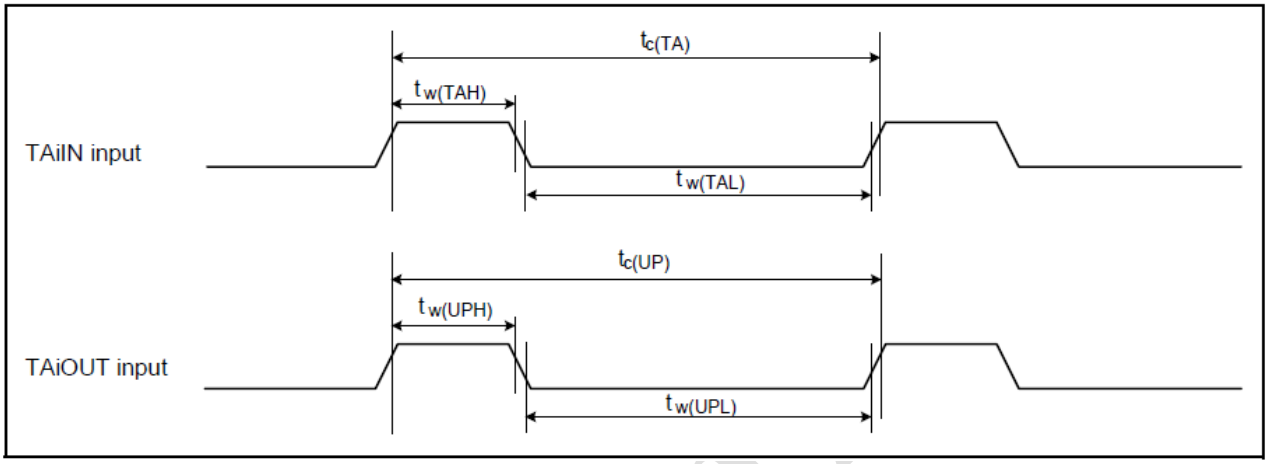


Figure 31: Timer A Input

Table 6.23: TableTitleTimer A Input (Two-Phase Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAiIN input cycle time	2		µs
tsu(TAIN-TAOUT)	TAiOUT input setup time	500		µs
tsu(TAOUT-TAIN)	TAiIN input setup time	500		µs

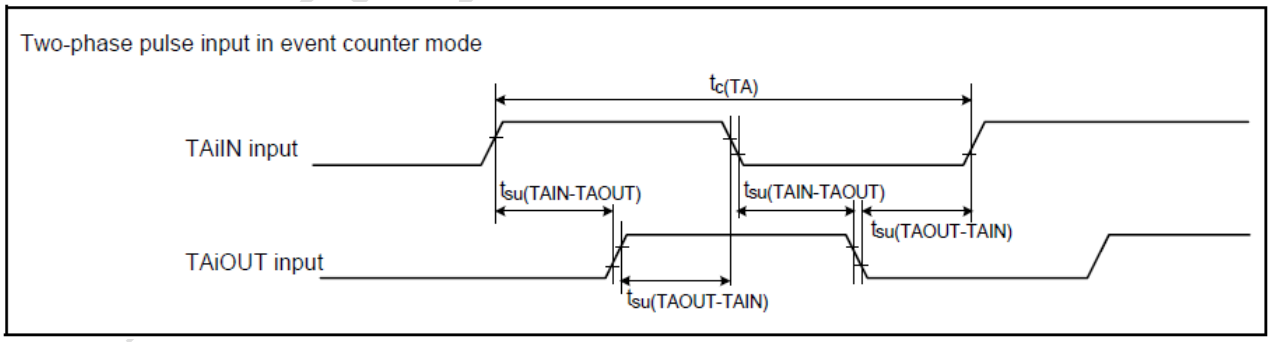


Figure 32: Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

6.9.3 Timer B Input

Table 6.24: Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBiIN input cycle timer (counted on one edge)	150		ns
tw(TBH)	TBiIN input high pulse width (counted on one edge)	60		ns
tw(TBL)	TBiIN input low pulse width (counted on one edge)	60		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	300		ns
tw(TBH)	TBiIN input pulse width (counted on both edges)	120		ns
tw(TBL)	TBiIN input low pulse width (counted on both edges)	120		ns

Table 6.25: Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBiIN input cycle time	600		ns
tw(TBH)	TBiIN input high pulse width	300		ns
tw(TBL)	TBiIN input low pulse width	300		ns

Table 6.26: Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBiIN input cycle time	600		ns
tw(TBH)	TBiIN input high pulse width	300		ns
tw(TBL)	TBiIN input low pulse width	300		ns

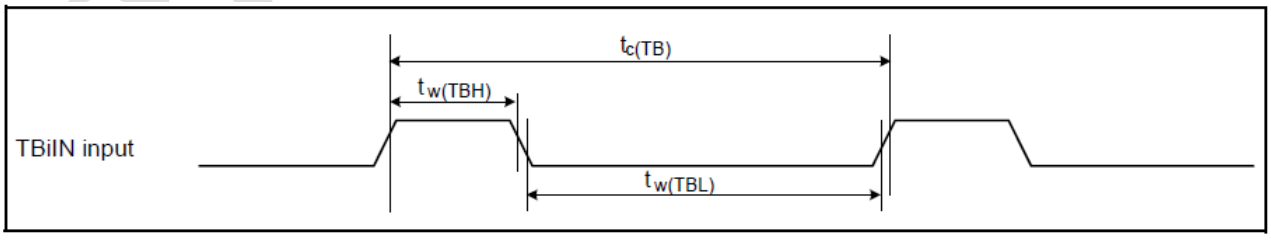


Figure 33: Timer B Input

6.9.4 Serial Interface

Table 6.27: Serial Interface

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(CK)	CLKi input cycle time	300		ns
tw(CKH)	CLKi input high pulse width	150		ns
tw(CKL)	CLKi input low pulse width	150		ns
td(C-Q)	TXDi output delay time		160	ns
th(C-Q)	TXDi hold time	0		ns
tsu(D-C)	RCDi input setup time	100		ns
tn(C-D)	RCDi input hold time	90		ns

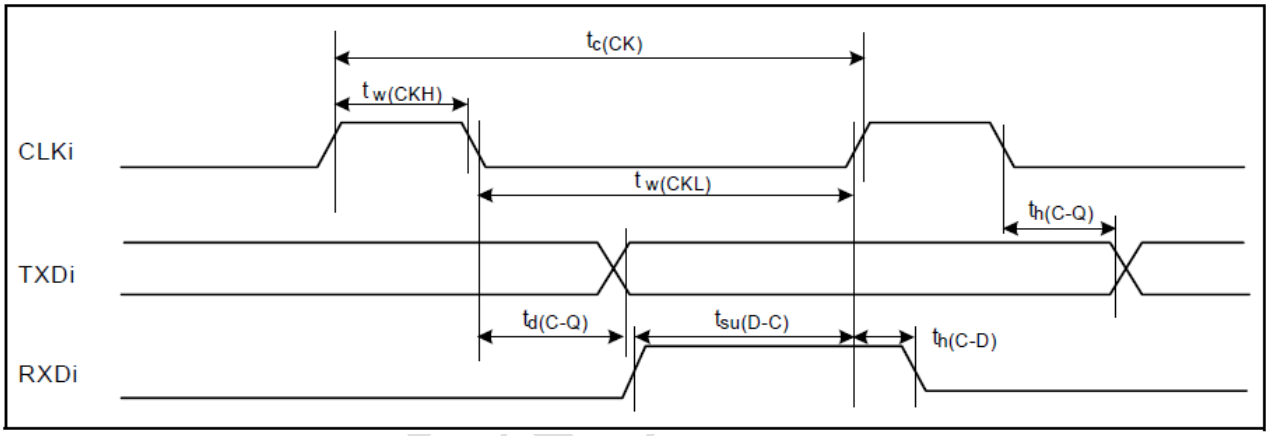


Figure 34: Serial Interface

6.9.5 External Interrupt INTi Input

Table 6.28: External Interrupt INTi Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(INH)	INTi input high pulse width	380		ns
tw(INL)	INTi input low pulse width	380		ns

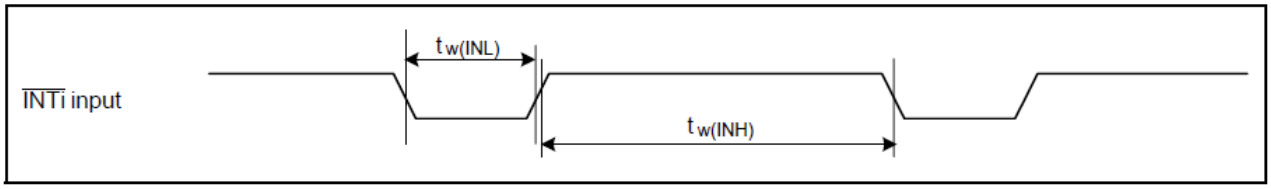


Figure 35: External Interrupt INTi Input

6.10 PHY Specifications

Parameter		Value
Dynamic Range		95 dB
Narrowband Interference rejection		−60dB
AWGN Interference rejection		−7dB
Maximum Data Rate	FCC	500 Kbps*
	ARIB	500 Kbps*
	CENELEC A	150Kbps*
	CENELEC B	50 Kbps*
Output Tx Power	FCC	1.1 dBm @ BW=1kHz
	ARIB	-3 dBm @ BW=1kHz
	CENELEC A	5.6 dBm @ BW=1kHz
	CENLEC 3	TBD
	CENELEC B	9.5 dBm @ BW=1kHz

***does not take into account the FEC.**

6.11 Network Layer Specifications

Parameter		Value
Maximum Network Depth		16
Maximum RMT Nodes in Network		2000
Performance‡‡‡	RMT Connection to BST	< 30 sec
	Route Fail Detection	< 1 minute

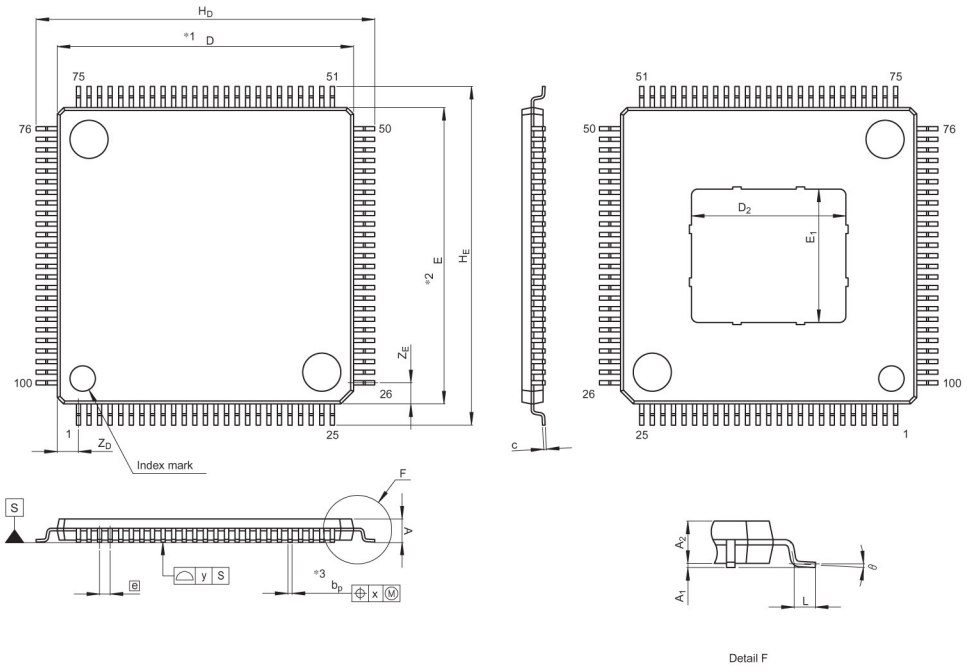
‡‡‡ For a network with 20 RS. For other network sizes, please consult Yitran's parameter configuration recommendation application note.

6.12 CRYSTAL SPECIFICATIONS

Parameter	Minimum	Nominal	Maximum	Unit
Operating Frequency		5.12 or 15.36		MHz
Overall Accuracy (over time and temperature)		120		PPM
Drive Level			150	µW
Equivalent Series Resistance			100	Ω
Motional Capacitance	3			fF
Shunt Capacitance			7	pF
Load Capacitance	15	18	20	pF

6.13 Mechanical Dimensions & Package Tolerances

JEITA Package Code	MASS[Typ.]
P-HTQFP100-14x14-0.50	0.5g

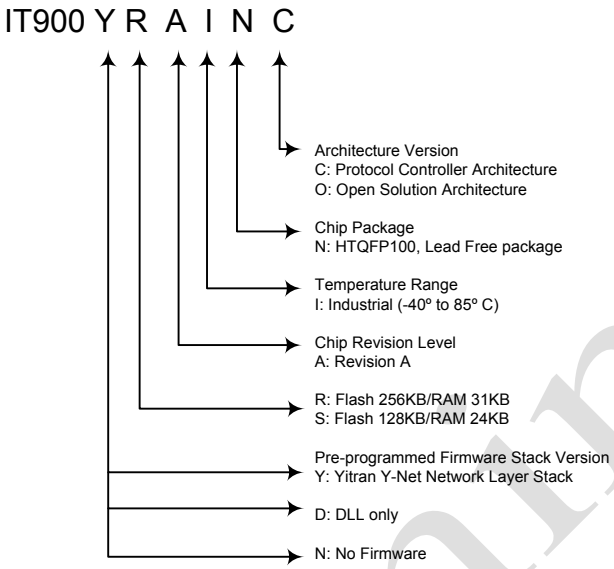


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.0	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.2
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
c	0.09	0.145	0.20
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.4	0.5	0.6
D_2	—	7.3	—
E_1	—	6.3	—

7 ORDERING INFORMATION

The IT900 part naming convention for ordering parts is shown below:



Document Control

Rev	Date	Description
1.0	February 2011	• Initial Release
1.1	November 2011	• Table 3.6: Internetworking Unicast and Internetworking Broadcast values corrected
1.2	February 2012	• PHY Operating Modes : CENELEC A3 Removed

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