

## FDC654P

### P-Channel Enhancement Mode Field Effect Transistor

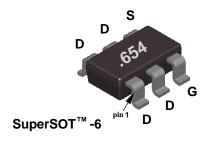
#### **General Description**

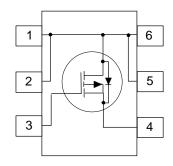
These P-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

### **Features**

- SuperSOT<sup>TM</sup>-6 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low R<sub>DS(ON)</sub>.
- Exceptional on-resistance and maximum DC current capability.







#### Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise note

Symbol	Parameter		FDC654P	Units
V <sub>DSS</sub>	Drain-Source Voltage		-30	V
V <sub>GSS</sub>	Gate-Source Voltage - Continuous		±20	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	-3.6	A
	- Pulsed		-10	
P <sub>D</sub>	Maximum Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	0.8	
Γ <sub>J</sub> ,Τ <sub>STG</sub>	Operating and Storage Temperature Range		-55 to 150	°C
THERMA	AL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	30	°C/W

Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CHAR	ACTERISTICS						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$		-30			V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient	I <sub>D</sub> = -250 μA, Referenced to 25 °C			-29		mV /°C
DSS	Zero Gate Voltage Drain Current	$V_{DS} = -24 \text{ V}, \ V_{GS} = 0 \text{ V}$				-1	μA
			$T_J = 55^{\circ}C$			-10	μA
GSSF	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
GSSR	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHARA	ACTERISTICS (Note 2)	•					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$		-1	-1.7	-3	V
$\Delta V_{GS(th)}/\Delta T_{J}$	Gate Threshold VoltageTemp.Coefficient	I <sub>D</sub> = -250 μA, Referenced to 25 °C			3.6		mV /°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = -10 \text{ V}, I_D = -3.6 \text{ A}$			0.065	0.075	Ω
, ,			T <sub>J</sub> = 125°C		0.094	0.127	1
		$V_{GS} = -4.5 \text{ V}, I_D = -2.7 \text{ A}$			0.11	0.125	
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = -4.5 \text{ V}, V_{DS} = -5 \text{ V}$		-5			Α
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = -10 \text{ V}, I_{D} = -3.6 \text{ A}$			3		S
DYNAMIC (	CHARACTERISTICS	•					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = -15 \text{ V}, \ V_{GS} = 0 \text{ V},$			435		pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz			245		pF
C <sub>rss</sub>	Reverse Transfer Capacitance				70		pF
SWITCHING	CHARACTERISTICS (Note 2)						
t <sub>D(on)</sub>	Turn - On Delay Time	$V_{DD} = -15 \text{ V}, I_{D} = -1 \text{ A},$			10	18	ns
t <sub>r</sub>	Turn - On Rise Time	$V_{GS} = -10 \text{ V}, \ R_{GEN} = 6 \Omega$			7	14	ns
t <sub>D(off)</sub>	Turn - Off Delay Time				26	42	ns
t,	Turn - Off Fall Time				18	29	ns
$Q_g$	Total Gate Charge	$V_{DS} = -15 \text{ V}, I_{D} = -3.6 \text{ A},$			10.5	15	nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = -10 \text{ V}$			2		nC
$Q_{gd}$	Gate-Drain Charge				2.6		nC
DRAIN-SOL	JRCE DIODE CHARACTERISTICS						,
l <sub>s</sub>	Continuous Source Diode Current					-1.3	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -1.3 \text{ A}$ (N	ote 2)		-0.8	-1.2	V
			T <sub>1</sub> = 125°C		-0.62	-1	1

#### Notes

<sup>1.</sup>  $R_{\text{Bulk}}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\text{Buc}}$  is guaranteed by design while  $R_{\text{Bck}}$  is determined by the user's board design.

a.  $78^{\circ}\text{C/W}$  when mounted on a minimum on a 1 in² pad of 2oz Cu in FR-4 board.

b. 156°C/W when mounted on a minimum pad of 2oz Cu in FR-4 board.

<sup>2.</sup> Pulse Test: Pulse Width  $\leq$  300 $\mu$ s, Duty Cycle  $\leq$  2.0%.

# **Typical Electrical Characteristics**

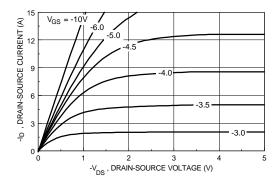


Figure 1. On-Region Characteristics.

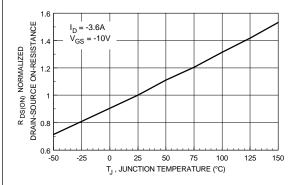


Figure 3. On-Resistance Variation with Temperature.

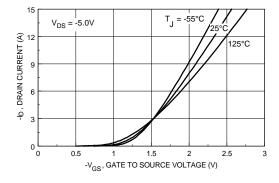


Figure 5. Transfer Characteristics.

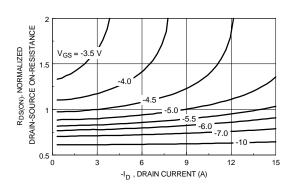


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

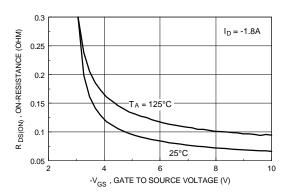


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

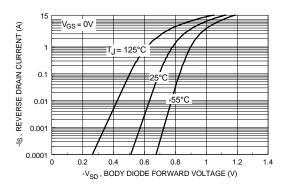


Figure 6. Body Diode Forward Voltage
Variation with Source Current
and Temperature.

## **Typical Electrical And Thermal Characteristics**

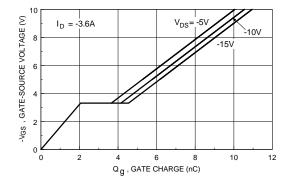
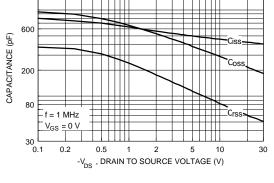


Figure 7. Gate Charge Characteristics.



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Figure 8. Capacitance Characteristics.

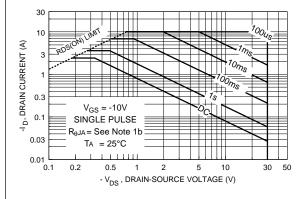


Figure 9. Maximum Safe Operating Area.

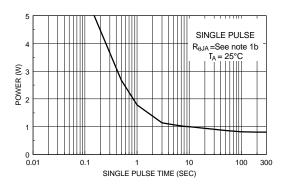


Figure 10. Single Pulse Maximum Power Dissipation.

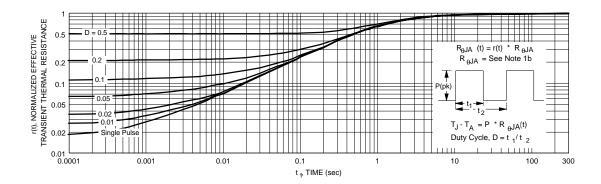


Figure 11. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.