HIGH TEMPERATURE 40V FLOATING DRIVER

FEATURES

- ▲ Operational beyond the -60°C to +230°C temperature range.
- ▲ Drives P- as well as N-channel MOSFETs (V_{GS}=5V).
- ▲ Input-to-output stages offset voltage from -30V to +40V.
- ▲ Operation as low-side or high-side driver.
- ▲ Under Voltage Lockout (UVLO) on PVDD domain.
- ▲ Standard Schmitt-trigger CMOS input.
- ▲ Plug-and-play with any digital 3.5V to 5V output.
- ▲ Up to 1A sink/source current (@ T_j=+230°C).
- ▲ Desaturation protection for both P- and N-channel MOSFETs.
- ▲ Soft-shutdown function in case of desaturation detected.
- ▲ Error reporting to digital controller.
- ▲ Monolithic design.
- ▲ Latch-up free.
- ▲ Ruggedized ceramic SMD and through hole packages.
- ▲ Also available as bare die.

APPLICATIONS

- ▲ Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- ▲ DC/DC converters, point-of-load power converters, switching power supplies, PWM control, motor drive, floating or ground-connected switches, Power switches (GaN).

DESCRIPTION

The XTR25410 gate driver family is an extremely flexible floating driver allowing the control of either PMOS or NMOS transistors (V_{GS}=5V) and designed for extreme reliability and high temperature applications. XTR25410 is intended to drive both high-side and low-side switches by converting the digital input signal into a floating control signal referenced to PVDD-PGND. The driver operates in both negative and positive configurations with possible offsets between input and output of -30V to +40V.

XTR25410 parts can be directly driven by any digital output, making them fully plug-and-play devices. This driver features full short circuit protection by means of desaturation detection of the external transistor after a blanking time, with soft turn-off feature and reporting the fault through the ERR pin. Undervoltage protections are provided for floating voltage power supplies. The device also includes an Error status output that can be used as an Enable.

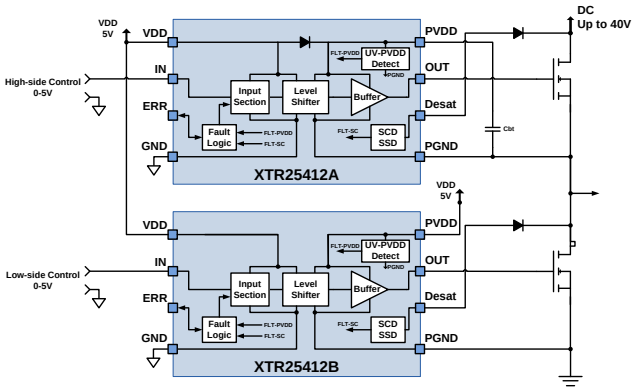
Full functionality is guaranteed from -60°C to +230°C, though operation well below and above this temperature range is achieved.

XTR25410 family parts have been designed to reduce system cost and ease adoption by reducing the learning curve and providing smart and easy to use features.

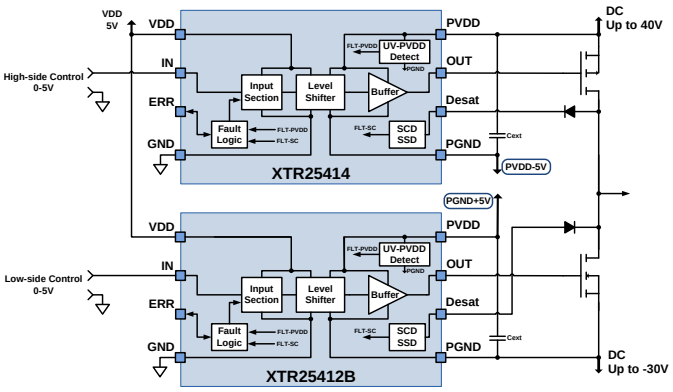
Parts from the XTR25410 family are available in ruggedized SMD and through hole hermetic packages, as well as bare die.

PRODUCT HIGHLIGHT

Totem pole congifuration (NMOS/NMOS)



Push-pull configuration (PMOS/NMOS)



ORDERING INFORMATION

X	TR	25	410
Source: X = X-REL Semi	Process: TR = HiTemp, HiRel	Part family	Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XTR25410-BD	-60°C to +230°C	Bare die		XTR25410
XTR25411-S	-60°C to +230°C	Ceramic SOIC	16	XTR25411
XTR25411-D	-60°C to +230°C	Ceramic side Braze DIP	16	XTR25411
XTR25412A-D	-60°C to +230°C	Ceramic side Braze DIP	8	XTR25412A
XTR25412A-FE	-60°C to +230°C	Gull-wing flat pack with ePad	10	XTR25412A
XTR25412B-D	-60°C to +230°C	Ceramic side Braze DIP	8	XTR25412B
XTR25412B-FE	-60°C to +230°C	Gull-wing flat pack with ePad	10	XTR25412B
XTR25414-D	-60°C to +230°C	Ceramic side Braze DIP	8	XTR25414
XTR25414-FE	-60°C to +230°C	Gull-wing flat pack with ePad	10	XTR25414

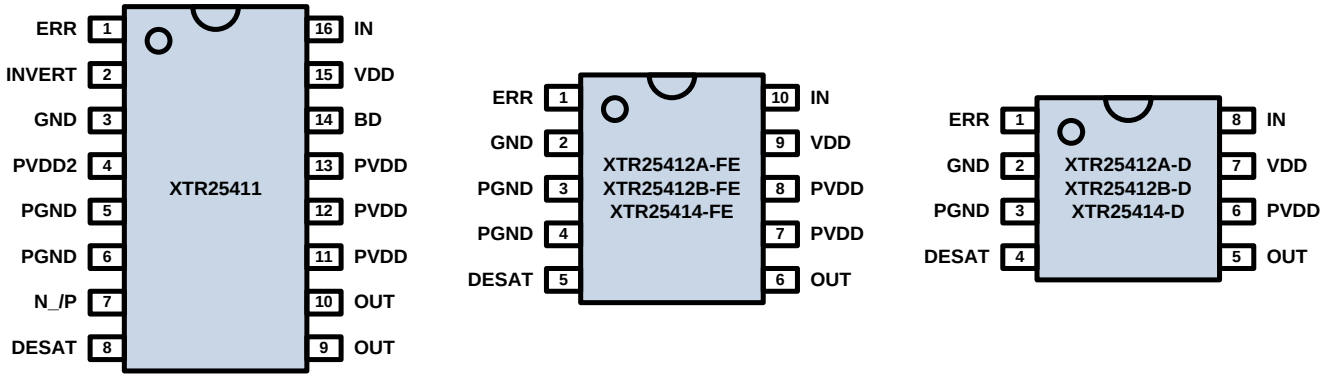
Other packages and packaging configurations possible upon request. MOQ may apply.

ABSOLUTE MAXIMUM RATINGS

Voltage on IN, ERR, INVERT and VDD to GND	-0.5 to 6.0V
Voltage on PVDD to PGND	-0.5 to 7.5V
Voltage on PGND to GND	-40V to 50V
Storage Temperature Range	-70°C to +230°C
Operating Junction Temperature Range	-70°C to +300°C
ESD Classification	1kV HBM MIL-STD-883

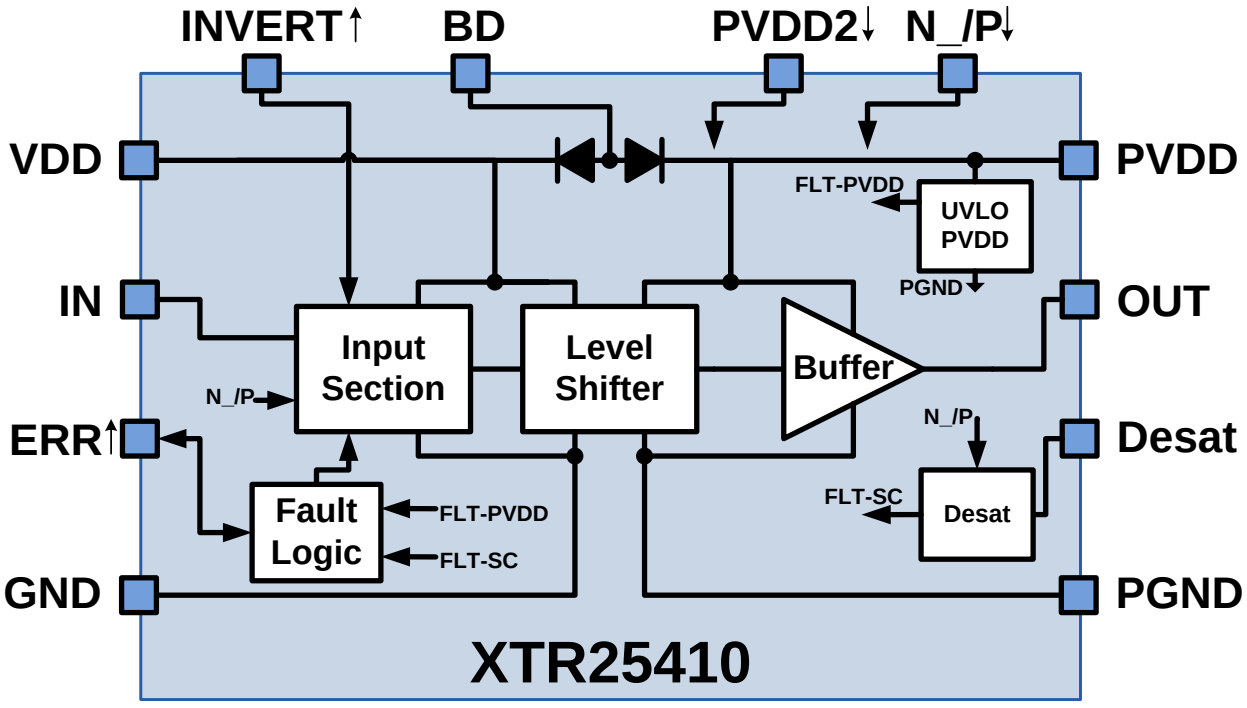
Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

PRODUCT VARIANTS



ePAD on bottom of package of FE packaging option connected to PVDD. It can be left floating on the PCB

BLOCK DIAGRAM



Arrows aside pin names indicate whether the input is internally pulled up or down.

PIN DESCRIPTION

XTR25411		
Pin Number	**Name**	**Description**
1	ERR	Enable and/or Reporting error. Connect to VDD to disable reporting function. Internal pull-up.
2	INVERT	Inverting input. Connect to GND to invert output logic. Internal pull-up.
3	GND	Ground of input section.
4	PVDD2	Auxiliary supply voltage.Connect to PVDD when operating in negative area (PGND<GND).Internal pull-down.
5	PGND	Ground of floating section.
6	PGND	Ground of floating section.
7	N_/P	Configuration pin. Connect to PVDD to drive PMOS; else NMOS type switch is targeted. Internal pull-down.
8	DESAT	Desaturation detection Input. If not used, connect to PGND (PVDD) when driving NMOS (PMOS).
9	OUT	Gate drive output.
10	OUT	Gate drive output.
11	PVDD	Supply voltage of power section. Referenced to PGND.
12	PVDD	Supply voltage of power section. Referenced to PGND.
13	PVDD	Supply voltage of power section. Referenced to PGND.
14	BD	Integrated Bootstrap Diode (Anode). Connect to VDD to use the integrated bootstrap diode.
15	VDD	Supply voltage of the input section. Referenced to GND.
16	IN	Input signal. Referenced to GND.

XTR25412A-FE / XTR25412B-FE		
Pin Number	**Name**	**Description** (NMOS type switch)
1	ERR	Enable and/or Reporting error. Connect to VDD to disable this function.
2	GND	Ground of input section.
3	PGND	Ground of floating section.
4		
5	DESAT	Desaturation detection Input. If not used, connect to PGND.
6	OUT	Gate drive output.
7	PVDD	Supply voltage of power section. Referenced to PGND. Option “A”: a bootstrap diode is connected between VDD and PVDD. Option “B”: VDD and PVDD are independent.
8		
9	VDD	Supply voltage of the input section. Referenced to GND.
10	IN	Input signal. Referenced to GND.

XTR25412A-D / XTR25412B-D		
Pin Number	**Name**	**Description** (NMOS type switch)
1	ERR	Enable and/or Reporting error. Connect to VDD to disable this function.
2	GND	Ground of input section.
3	PGND	Ground of floating section.
4	DESAT	Desaturation detection Input. If not used, connect to PGND.
5	OUT	Gate drive output.
6	PVDD	Supply voltage of power section. Referenced to PGND. Option “A”: a bootstrap diode is connected between VDD and PVDD. Option “B”: VDD and PVDD are independent.
7	VDD	Supply voltage of the input section. Referenced to GND.
8	IN	Input signal. Referenced to GND.

XTR25414		
Pin Number	**Name**	**Description** (PMOS type switch)
1	**ERR**	Enable and/or Reporting error. Connect to VDD to disable this function.
2	**GND**	Ground of input section.
3	**PGND**	Ground of floating section.
4	**DESAT**	Desaturation detection Input. If not used, connect to PVDD.
5	**OUT**	Gate drive output.
6	**PVDD**	Supply voltage of power section. Referenced to PGND.
7	**VDD**	Supply voltage of the input section. Referenced to GND.
8	**IN**	Input signal. Referenced to GND.

THERMAL CHARACTERISTICS

Parameter	Condition	Min	Typ	Max	Units
XTR25411-S (SOIC16)					
Thermal Resistance: J-C R_{Th_J-C}			22		°C/W
Thermal Resistance: J-A R_{Th_J-A}			120		°C/W
XTR25411-D (DIL16)					
Thermal Resistance: J-C R_{Th_J-C}			22		°C/W
Thermal Resistance: J-A R_{Th_J-A}			95		°C/W
XTR2541x-FE (DFP10 with exposed pad)					
Thermal Resistance: J-C R_{Th_J-C}	Measured on ePAD.		7		°C/W
Thermal Resistance: J-A R_{Th_J-A}	ePAD thermally connected to 3cm² PCB copper		70		°C/W
XTR2541x-D (DIL8)					
Thermal Resistance: J-C R_{Th_J-C}			25		°C/W
Thermal Resistance: J-A R_{Th_J-A}			100		°C/W

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply voltage VDD to GND	4.5	5	5.25	V
Supply voltage PVDD to PGND	3.55	5	5.25	V
Voltage on PGND to GND	-30		40	V
Voltage on IN to GND	-0.3		VDD+0.3	V
Junction Temperature[1] T_j	-60		230	°C

[1] Operation beyond the specified temperature range is achieved.

ELECTRICAL SPECIFICATIONS

Static Characteristics

Unless otherwise stated, VDD=5V, PVDD=5V (to PGND), IN=0V , -60°C<T_j<230°C.

Parameter	Condition	Min	Typ	Max	Units
Supply Current					
Static VDD Supply Current **I_{VDD_Sta}**	V_{IN}=GND or VDD			25	µA
Static PVDD Supply Current **I_{PVDD_Sta}**	V_{IN}=GND or VDD			100	µA
Control INPUT					
Input Low voltage **V_{IL}**			2.16	2	V
Input High voltage **V_{IH}**		3.7	3.49		V
Input current **I_{IN}**	V_{IN}=GND or VDD T_j=25°C T_j=230°C			0.1 50	nA
Bootstrap Diode (XTR25412A)					
Continuous Forward Current **I_{BSTD}**		1			A
Forward Voltage **V_{BSTD}**	I_{DIODE}=1A T_j=25°C T_j=230°C		TBD TBD		V

ELECTRICAL SPECIFICATIONS (CONTINUED)

Dynamic Characteristics

Unless otherwise stated, VDD=5V, PVDD=5V (to PGND), Cload=0.5nF, -60°C<T_j<230°C.

Parameter	Condition	Min	Typ	Max	Units
Reporting					
Reporting delay t_{rep}	T_j=25°C T_j=230°C		250 350		ns
Enable Dead time t_{en}	T_j=25°C T_j=230°C		1.5 1.6		µs
Desaturation Time					
Detection Blanking Time t_{blank}	T_j=25°C T_j=230°C		300 400		ns
Shutdown Delay t_{shut}	T_j=25°C T_j=230°C		100 140		ns
Output Current peak					
Peak current I_{Peak}	T_j=25°C (10nF load) T_j=230°C (10nF load)		1.5 1		A
Soft Turn Off current I_{Soft}	T_j=25°C T_j=230°C		110 80		mA
Switching Time					
Delay ON Time $t_{d(ON)}$	T_j=25°C T_j=230°C		158 283		ns
Rise Time t_r	T_j=25°C T_j=230°C		6 9		ns
Delay OFF Time $t_{d(OFF)}$	T_j=25°C T_j=230°C		114 192		ns
Fall Time t_f	T_j=25°C T_j=230°C		7 11		ns

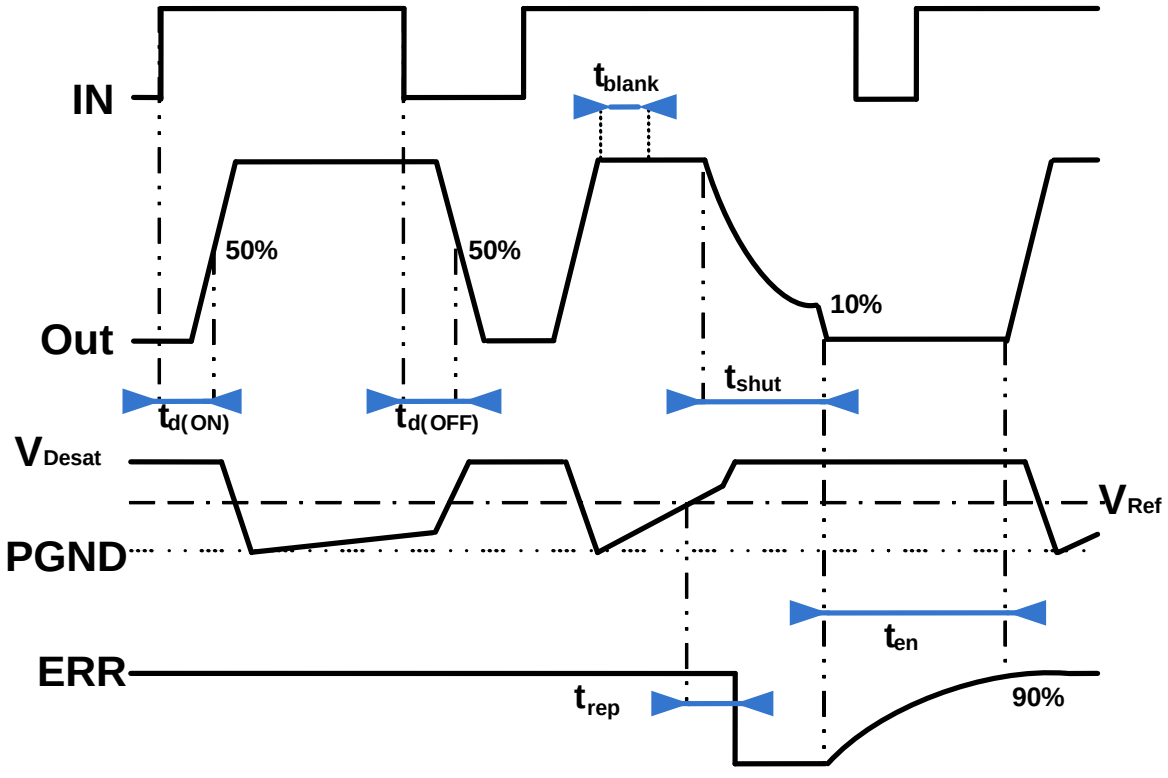


Figure 1. Soft Shutdown and Reporting Error Timing Waveform (NMOS type switch)

Figure 1 shows the Soft Shutdown and the reporting error timing waveform. When OUT is high and V_{Desat} is higher than V_{Ref}, a desaturation error is detected. A blanking time (t_{blank}) is used to avoid false detection when turning ON the external switch. The delay between desaturation detection and the error reporting is called t_{rep}.
The desaturation process takes t_{shut} to smoothly turn OFF the external switch.
When error disappears, ERR/ENB signal is pulled up through an integrated RC circuit producing a blanking time called t_{en}.

THEORY OF OPERATION

Product description

The XTR25410 is a high temperature, high reliability 5V gate driver able to operate from -60°C to 230°C. Depending on packaging options, multiple-versions are available. One important feature of those devices is their ability to shift the 0/5V control signal up to 35V/40V or down to -25V/-30V.

This unique and highly configurable gate driver allows the control of either PMOS or NMOS transistors. It can be used on each high side or low side configuration. Floating power supply (PVDD/PGND) may be positive or negative. At the same time, protection functions are provided as well as reporting errors function.

The full featured version is the XTR25411, presented in 16-pin packages (SOIC and SB DIP). This device is able to drive either NMOS or PMOS transistors with voltage shifts from -30V to 40V. XTR25412 devices are NMOS gate drivers. Option XTR25412A, with integrated bootstrap diode, can be used as both high side (Figure 2) and low side drivers.

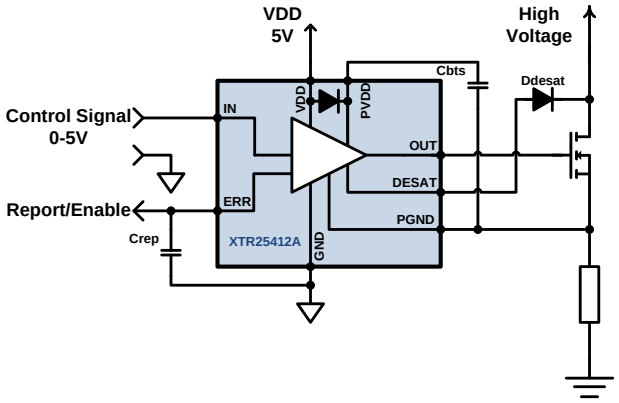


Figure 2. XTR25412A gate driver used with bootstrap supply on high side configuration

Option XTR25412B, without integrated bootstrap diode, can be used for positive (Figure 3) or negative (Figure 4) configuration.

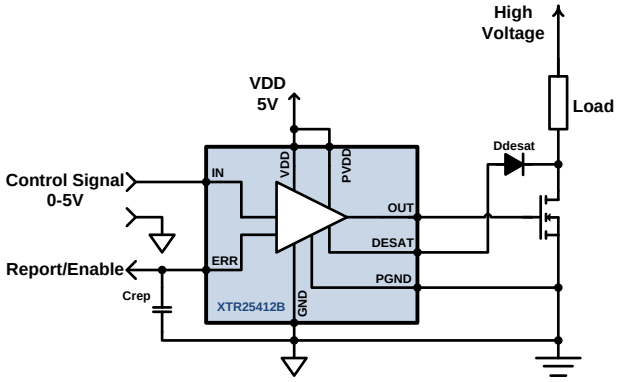


Figure 3. XTR25412B gate driver used on positive configuration

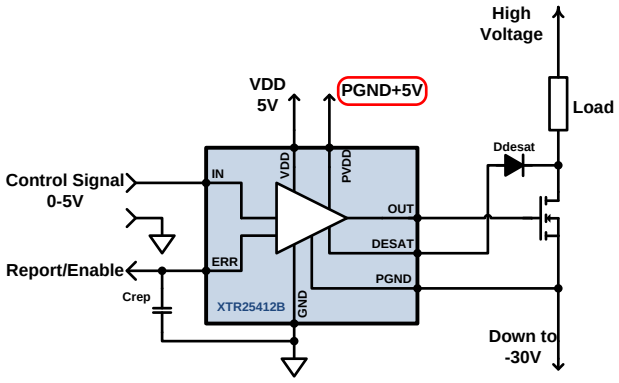


Figure 4. XTR25412B gate driver used on negative configuration

The XTR25414 is a PMOS gate driver that can be used as a high side (Figure 5) driver in push-pull configuration. As for the other parts in this driver family, desaturation protection is provided as well as error reporting functionality.

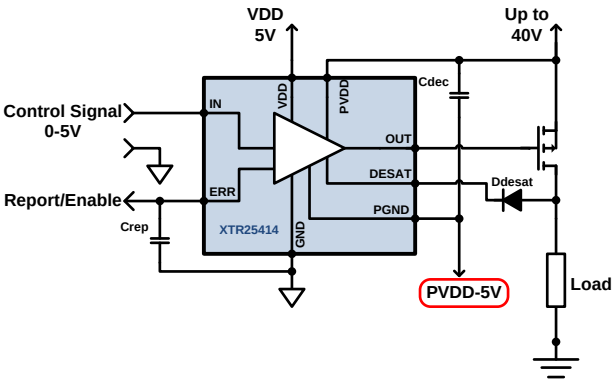


Figure 5. XTR25414 used as high side gate driver

Features Description

Start-Up

At power supply start-up, ERR signal is pulled down as long as the supply voltage isn't properly established (Figure 6). A minimum supply voltage of 4.5V on VDD is recommended to clear this fault and allow the driver to operate safely. At low supply on PVDD, UVLO on PVDD is reported (ERR signal low) only at the rising edge of IN.

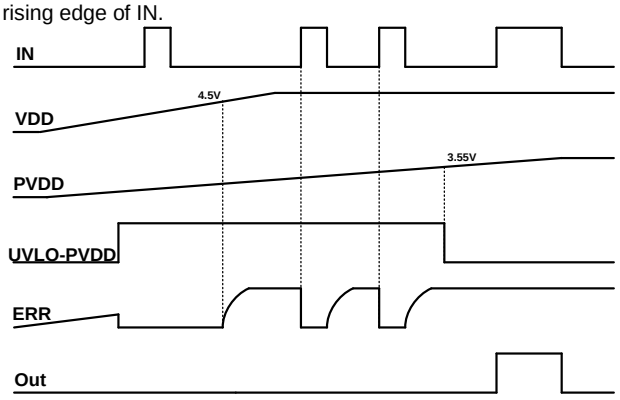


Figure 6. Start-up Timing waveform

Normal Operation

After start-up, the ERR signal is set high and the driver is operative. Turning the input signal high to VDD produces output to turn high to PVDD when driving NMOS type load, or low to PGND when driving PMOS type.

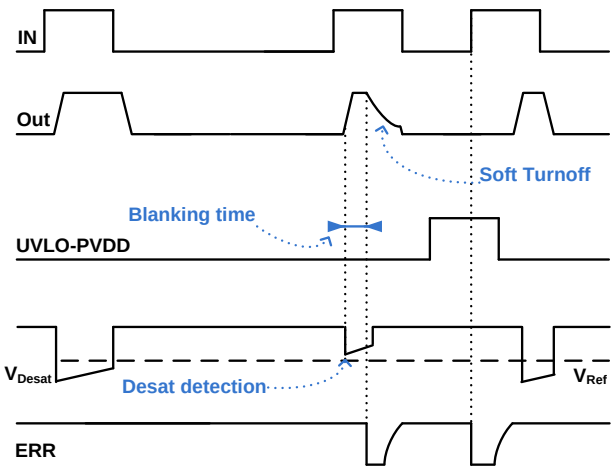


Figure 7. Normal Operation Waveform when driving NMOS

Under Voltage Lock Out (UVLO)
To assure safe control of the external switch, the UVLO protection disables the driver's output when the floating supply voltage (PVDD vs. PGND) is less than the undervoltage threshold.
The recommended VDD range is between 4.5V and 5.25V. At lower VDD, the circuit could be functional with longer propagation delay.
However, when supply voltages are bellow recommended value, it is guaranteed that the driven load is protected whatever the control signal is (Output signal is low). In this condition, a fault signal is generated (ERR is low).
For PVDD floating side, UVLO condition can't be reported through ERR pin while input control signal is low (Figure 7).

Desaturation protection
The XTR25410 desaturation circuit monitors the Drain to Source voltage of the driven switch through external diode. This voltage is compared to a reference voltage of 2.4V to PGND (Figure 8).
When desaturation event is detected a Soft Turnoff sequence begins to turn off the driven switch smoothly. This sequence will protect the driver from high dI/dt on the external MOSFET that may cause overvoltage on the driver side and so its destruction.
This protection is available for both PMOS and NMOS configurations.

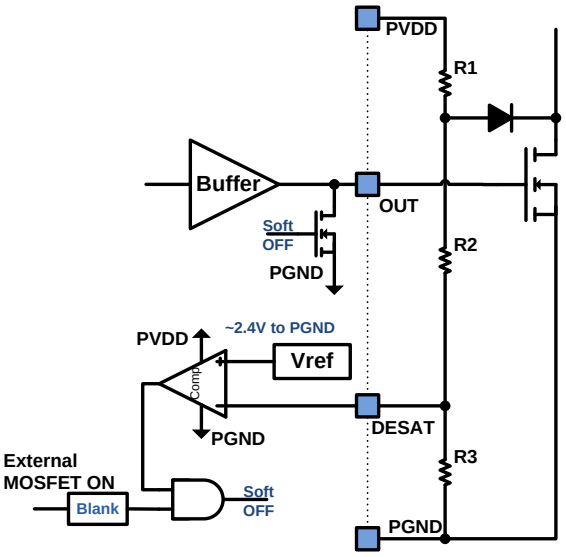


Figure 8. Desaturation detection circuit

The external desaturation diode should have high breakdown voltage and low capacitance in order to minimize noise coupling and switching delay.
Pull-up resistor R1 is used to allow detection when the drain voltage is lower than PVDD-V_{diode}. Typically, it is chosen to be higher than 15k to make sure there is no significant current being drawn from PVDD.

R2 and R3 are optional resistors that can be used to tune-up the desaturation threshold:

$$V_{DSth} = V_{ref} \times \frac{R2 + R3}{R3} - V_{diode}$$

An example is giving in the following table:

V_{DSth}	R_1	R_2	R_3
2V	15k	33k	100k
5V	15k	56k	33k
8V	15k	150k	56k

Error reporting
ERR pin can be used as an enable pin connected to 0/5V control signal of µC (Figure 9), or pulled up to VDD with an external resistor (Figure 10). A reporting error function is provided with the same pin. When UVLO or Desat errors appears, an integrated pull down set ERR signal to GND. Otherwise, if this function is not needed, ERR pin is set high to VDD (REnb=0 on Figure 10).

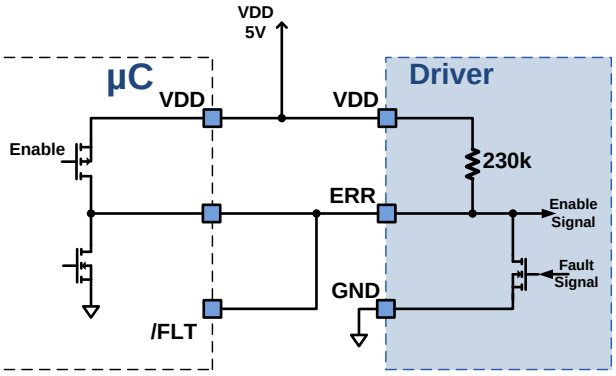


Figure 9. Error reporting function used with µC

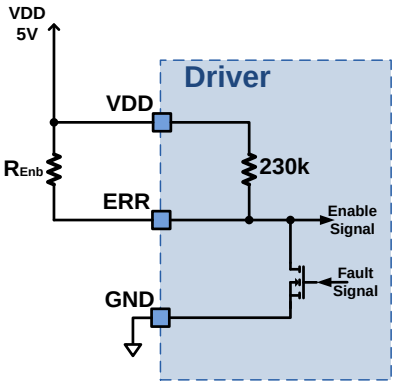
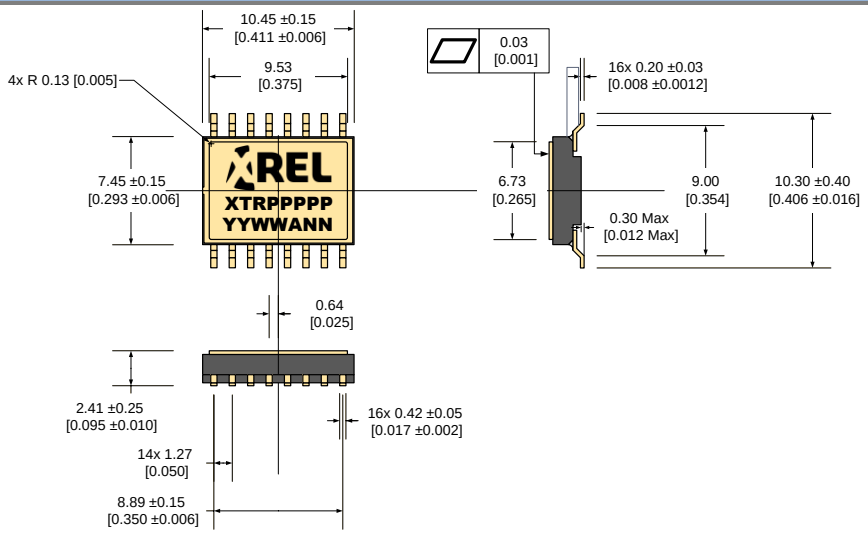


Figure 10. ERR pin used for enable only

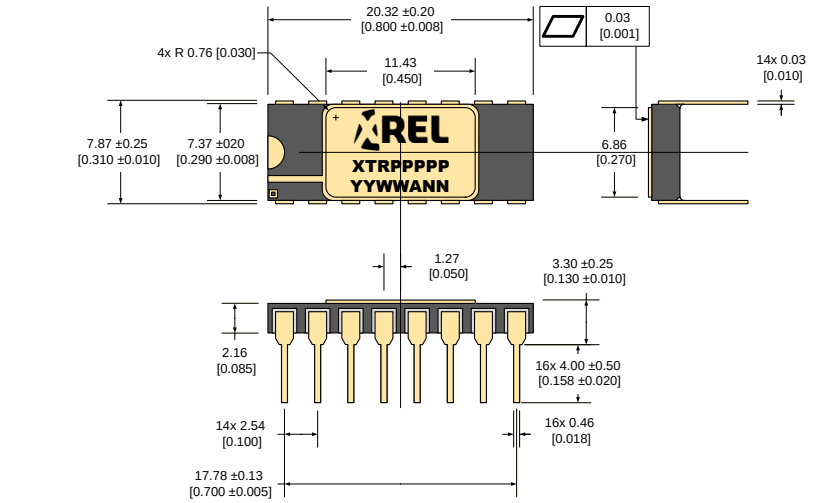
PACKAGE OUTLINES

Dimensions shown in mm [inches].

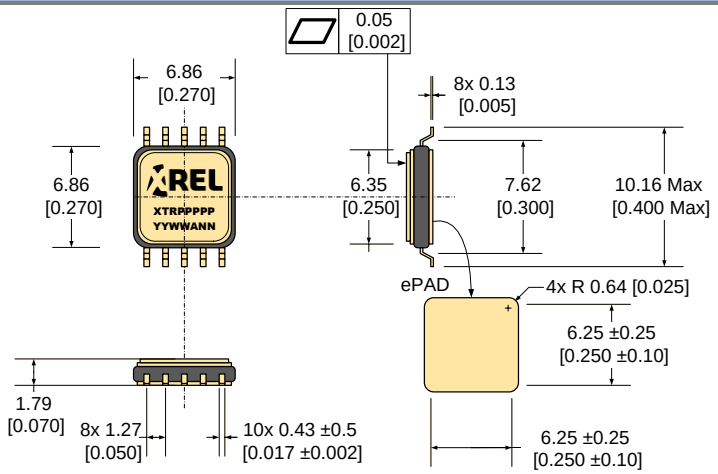
Ceramic Small Outline IC SOIC16



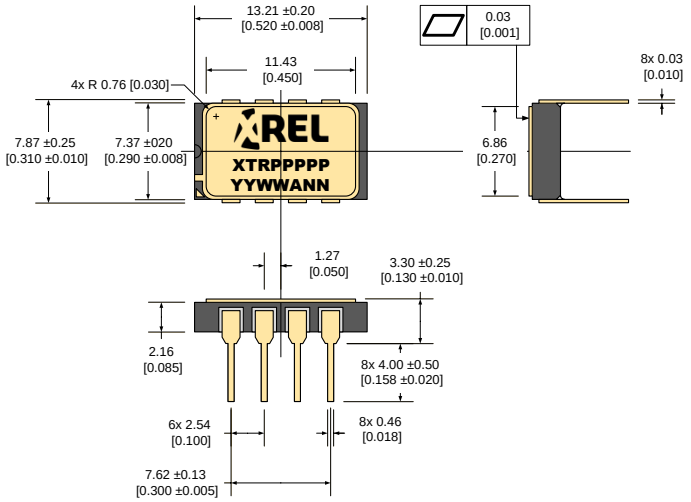
Ceramic Side Brazed Dual In-line DIP16



Gull-wing flat pack with ePad CDFP10



Ceramic Side Braze Dual In-line DIP8



Part Marking Convention	
Part Reference: XTRPPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

IMPORTANT NOTICE & DISCLAIMER

CONTACT US

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