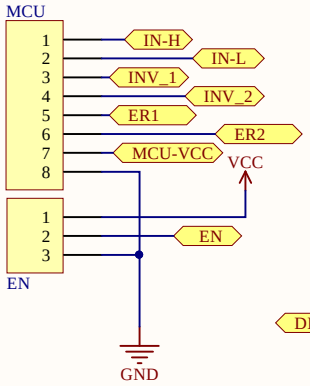
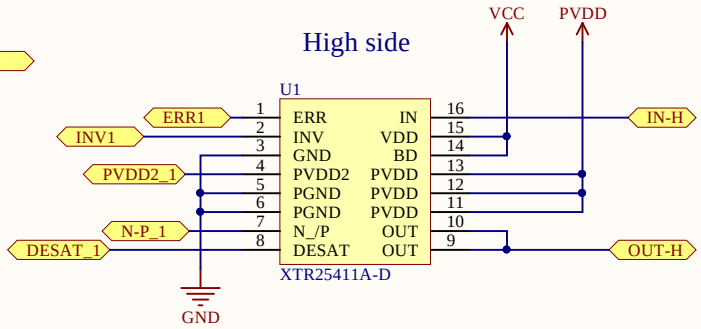
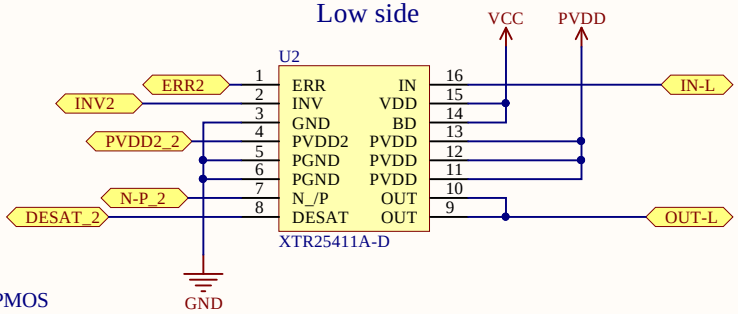
Transmitter side



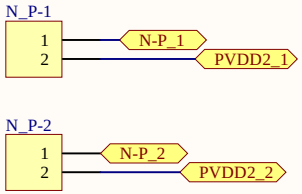
High side



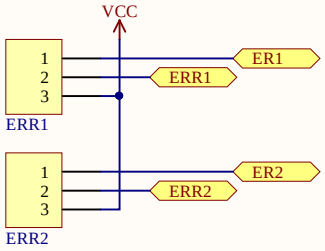
Low side



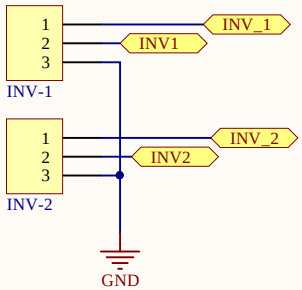
N_/P: connect to PVDD for PMOS

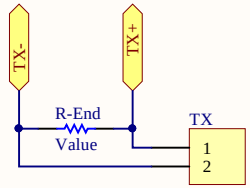


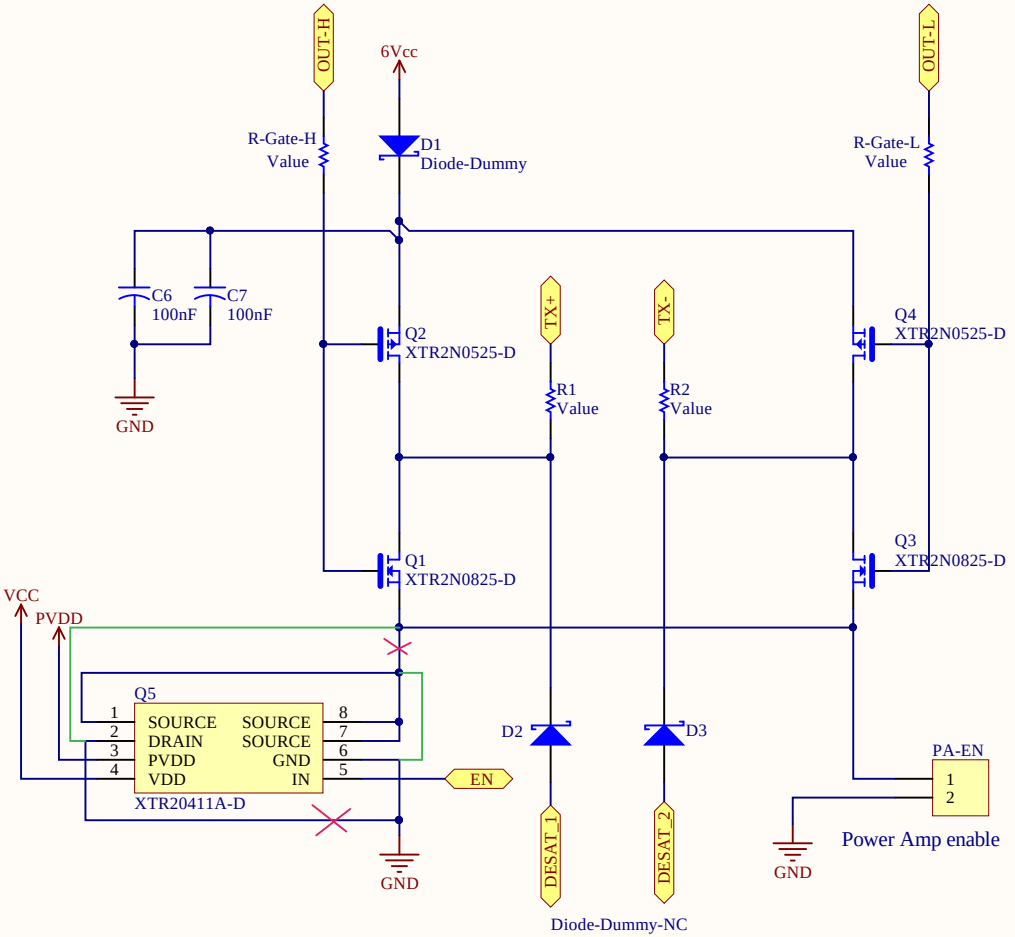
Error/Report: connect to Vdd to disable



Invert: connect to GND to invert logic or use extrnal MCU







Title	DVT Discrete	
Size: A4	Number: PN10034	Revision: 1.0
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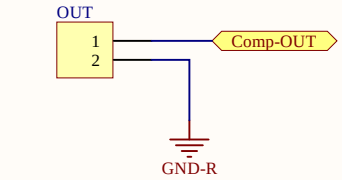
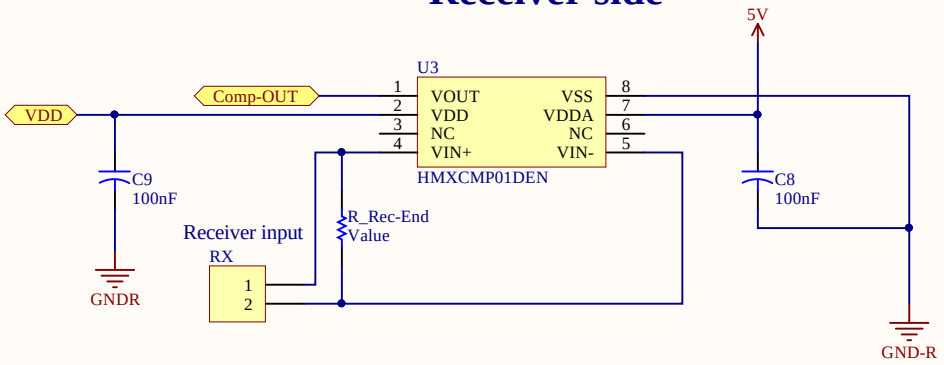
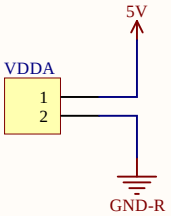
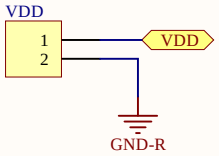
Receiver side

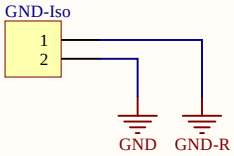


to avoid the GND loop not connect GND if not isolated

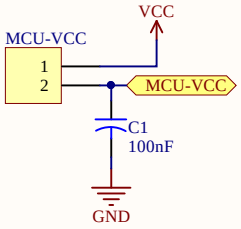




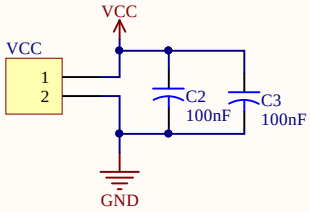




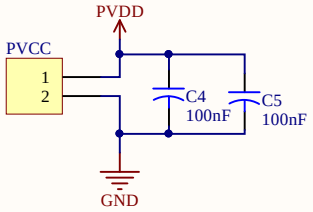
MCU-VCC jumper



Low Power VCC/5V



High Power VCC/5V



Comparator VDD

Title: DVT Integrated		
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