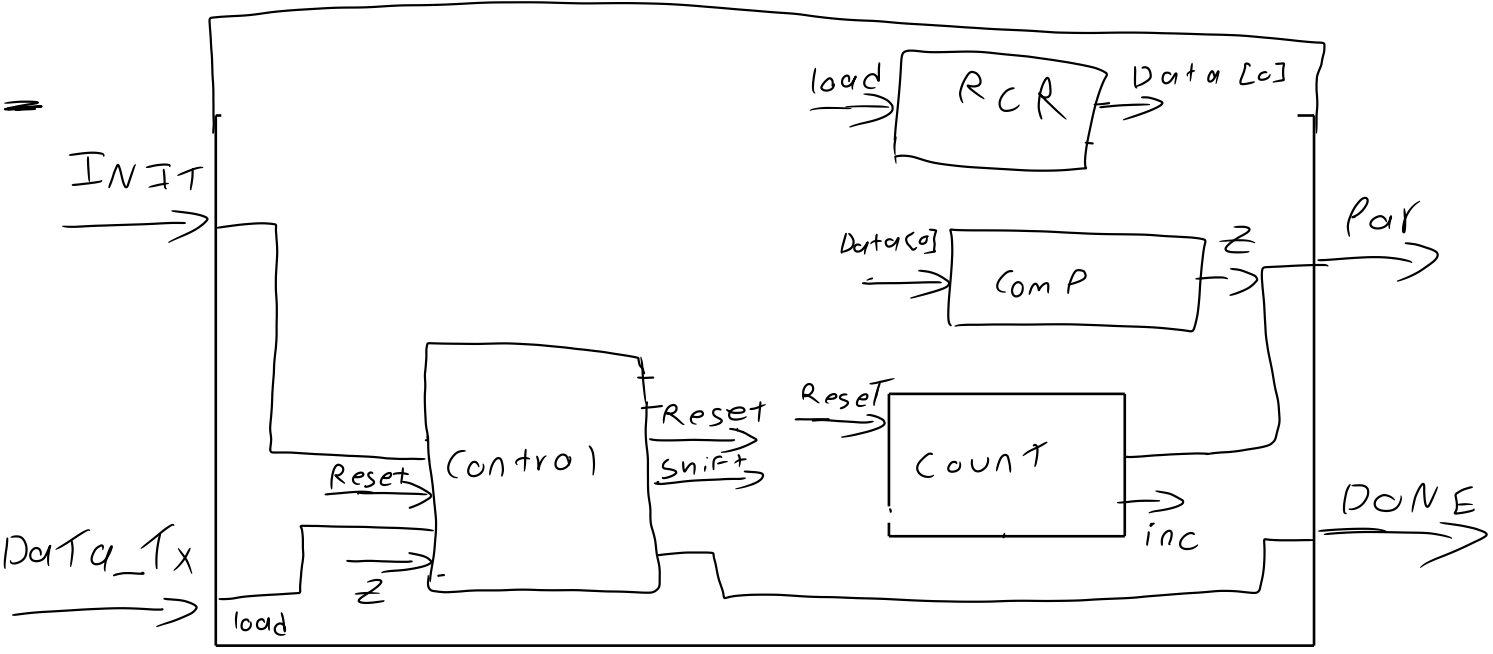


```
module Paridad (Clk, Reset, init, Data_Tx, Par, Done)

  input Clk;
  input Reset;
  input init;
  input Data_Tx [0:7];

  wire z;
  wire shift;
  wire reset;
  wire load;

  wire Data[0:7]
  wire inc;
  Wire count;

  output Par;
  output Done;


endmodule

comp comp0(.in_Data(Data), .out_z(z));
RcR RcR0(.clk(clk), .in_Data(Data_Tx), .out_Shft(shift));
count count0(.in_inc(inc), .out_Par(Par), .resety(reset));
control control0(.in_z(z), .in_init(Init), .Done1(Done), .Reset(Reset),
```