MSE | MASTER OF SCIENCE IN ENGINEERING

TTHF LAB

ADVANCED ELECTRONIC DESIGN

EMC, signal integrity, grounding and power supply routing, decoupling, transmission lines, simulation tools

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Topics of this series of 3 lessons

PCB Design

- Lesson 1:
  - Introduction
  - Partitioning, filtering
  - Shielding
  - Image planes
  - Continuous vs split GND concepts
  - Mixed signal circuits
- Lesson 2:
  - Decoupling
  - Transmission lines
  - Guard rings
  - Crosstalk, Ground bounce
  - Differential signaling
  - Terminations
  - Clock distribution: clock skew and clock jitter
- Lesson 3:
  - Place & route strategy
  - Components selection
  - Layer stackups
  - Multicard systems, backplanes
  - Enclosures, connectors and cables
  - ESD + Burst protection
  - 2-layer PCBs
  - Design for testability
  - Prototyping

Introduction

The terms of the problem

When designing printed circuit boards (PCBs) we are faced with EMC questions:

- Product must operate reliably and pass compliance tests with a minimum of design iterations
- System must be immune to external perturbations (GSM, DECT, WLAN, Broadcast. etc).
- We want to reduce costs of external shielding
- Product should offer wired or wireless data communications
- We want to use the newest and fastest ICs and processors
- Product may contain high precision analogue circuits or sensors
- We need to use low voltage logic (3.3V and less)
- We have mixed signal (digital+analog) circuits
- Product should be lightweight

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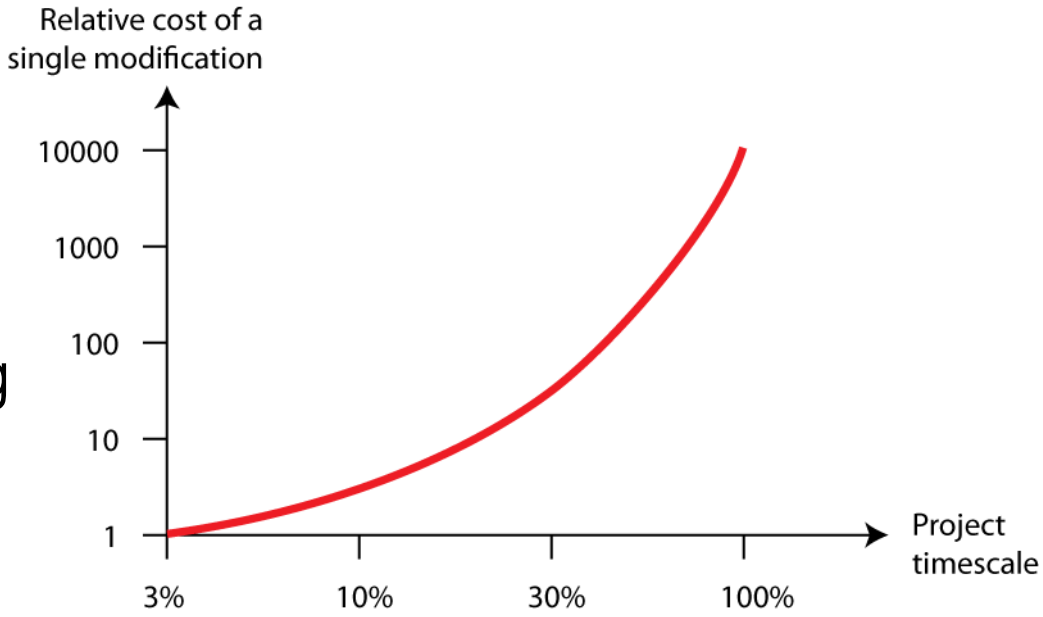
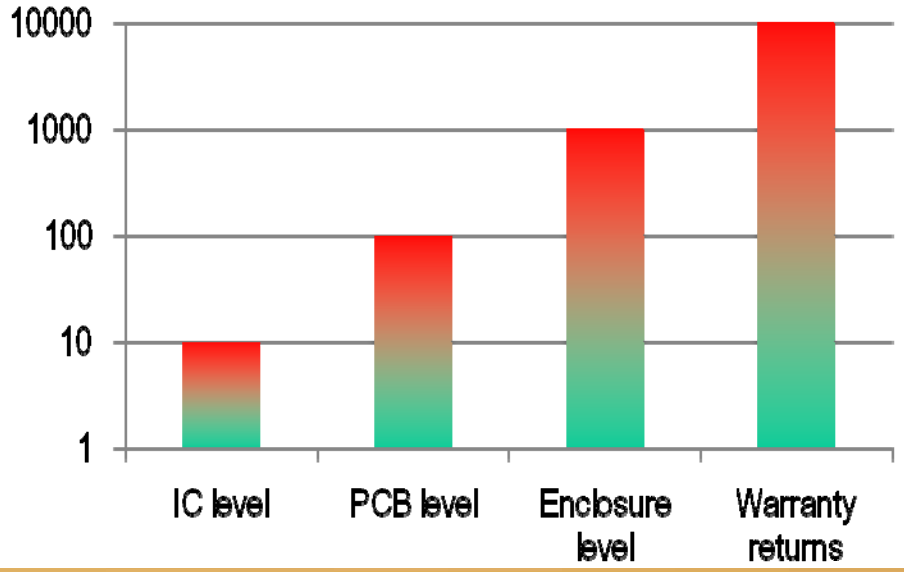
A matter of costs

In order to reduce costs:

- Avoid errors from the beginning
- Solve signal integrity issues at component/PCB level
- Pass EMC compliance tests
- Avoid warranty returns





Relative cost of achieving EMC

(Source: [5])

Definition of "high speed" circuit

We consider a circuit as *high speed*, when we need to consider the signal traces as transmission lines.

Rule of thumb:

For a given signal having a rising/falling time t_r , a signal trace of length l must be considered under the transmission line theory, if

$$t_r < 2\tau$$

where τ is the time the signal takes to travel the distance l

$$\tau = \frac{l}{v_{ph}}$$

(v_{ph} is the signal velocity. Typical values on PCBs are: 0.5c .. 0.6c)

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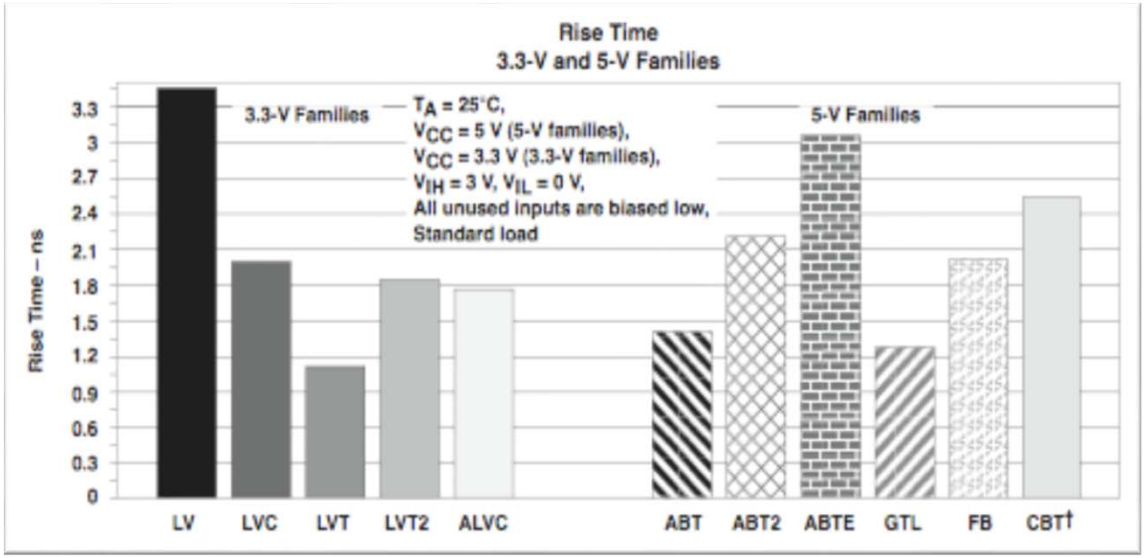
Definition of "high speed" circuit

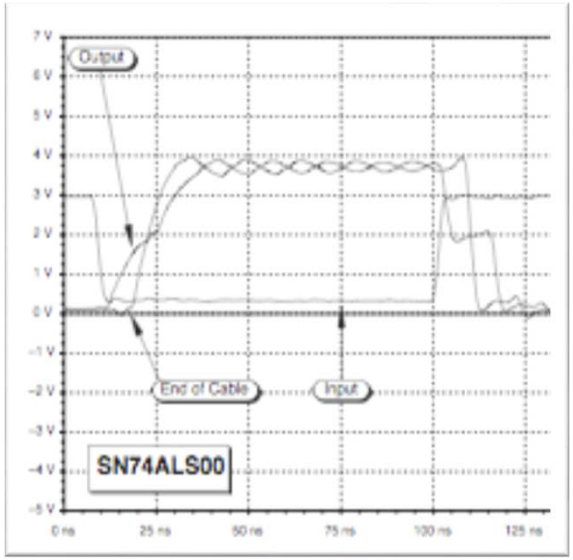
Example

A 74LVCxx buffer (3.3V) has a rise time t_r of 2 ns.

With v_{ph} = 0.5c we start having transmission line effects with a trace length of:

$$l = \tau \cdot v_{ph} > \frac{t_r}{2} \cdot v_{ph} = \frac{2 \cdot 10^{-9} s}{2} \cdot 1.5 \cdot 10^{8} \, m/s = 15 \, cm$$





➔ even with today's standard components and moderate trace lengths (and PCB sizes), we must consider transmission line effects.

(Source: Texas Instruments)

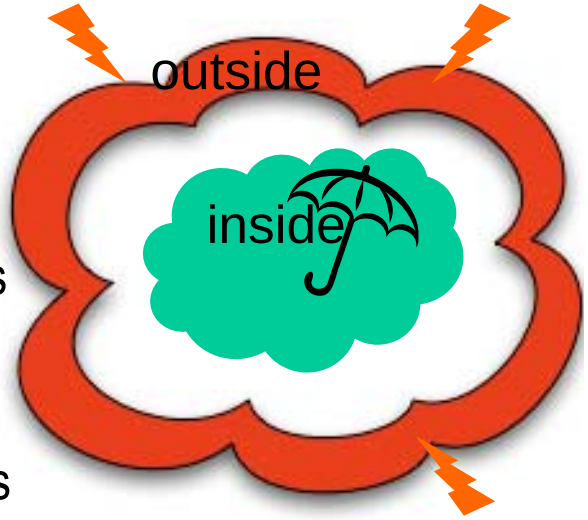
Quiz time

1. When do we need to take transmission line effects into consideration

- ☐ always
- ☑ when signal traces are longer than λ/2
- ☑ when the signal transition time is shorter than twice the propagation time on the line
- ☐ when signal frequency is >100 MHz
- ☐ only when we are dealing with cables and connectors

PCB partitioning and shielding

Keep inside and outside worlds separated

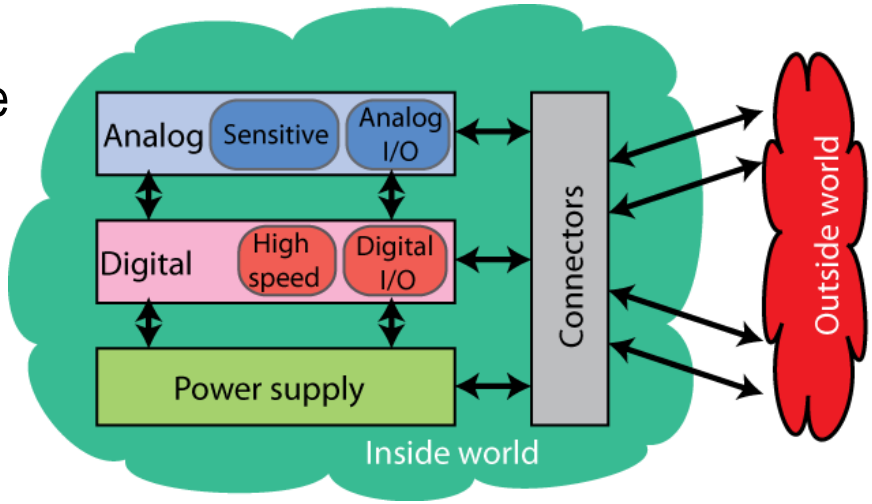


- Inside world: protected, filtered area
- Outside world: any cable (except shielded), connector (including board-to-board), components and PCB traces that are not over a continuous reference plane, pins or heatsinks that are taller than λ/10
- Goal: reduce design iterations, costly shielding and fixes
- Think as if you do not have a shielded cabinet (even if you do): make the design immune at PCB level to external and internal (!) noise sources
- Do not wait or postpone this partitioning until the design is completed. Do not rely on costly afterward shielding.
- other PCBs in the same cabinet must often be considered as "outside" components

PCB partitioning and shielding

Further divide the inside world

- identify functional blocks having different signal properties (sensitive analog, noisy digital, RF, I/O, etc)
- keep high speed clock sources (oscillators) far from connectors
- separate noisy blocks (e.g. switching power supplies) from sensitive analog circuits (e.g. sensor conditioning)
- carefully route signals leaving one zone for another (more on this in this course)
- apply adequate filtering or suppressing to these signals
- be cautious when using an autorouter (define keep-out traces or no-route areas)



PCB partitioning and shielding

Watch out for self generated problems

- different internal blocks can affect each other with EM phenomena:
  - noise emitted by PWM circuits (switching power supplies, motor drives, inverters)
  - GND noise generated by fast switching logic circuits
  - RF noise from oscillators or wireless transceivers
  - harmonics due to signal distortion, inter modulation
  - spurious signals generated by unwanted demodulation (in p-n junctions)
- examples of coupling of these phenomena
  - through common power supplies ("supply noise")
  - capacitively, inductively

PCB partitioning and shielding

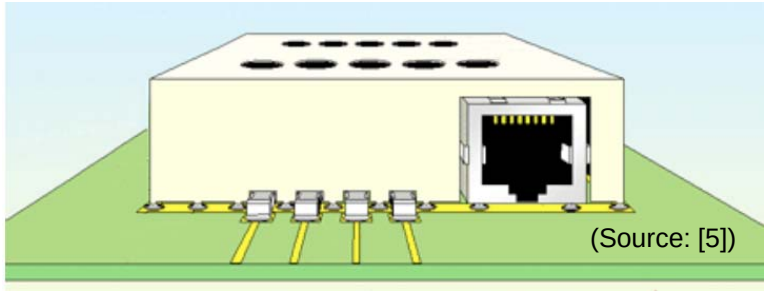
Prevent noise from crossing a functional block's boundary

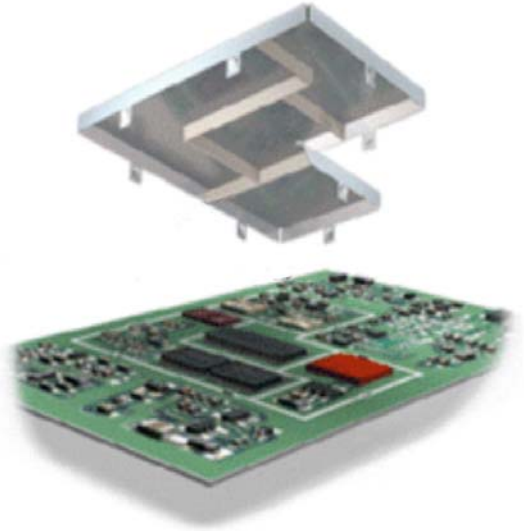
- Consider the following protective measures
  - ferrite beads
  - filters (π, L)
  - opto couplers
  - common mode chokes
  - fiber optic link instead of copper cable
  - add series impedance (R, L) to I/O signals
  - adequately filter signals going to the front panel against ESD (e.g. LEDs, keyboards) by using one of above techniques
  - add shielding at PCB level

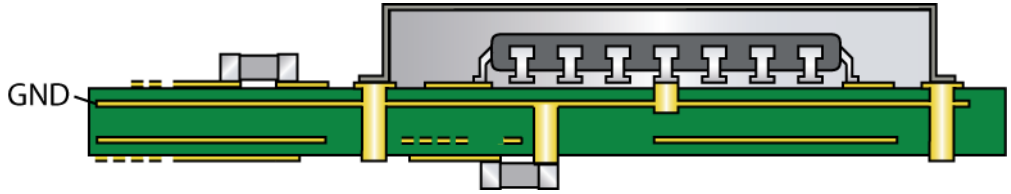
PCB partitioning and shielding

Shielding

- Shielding at cabinet level is possible but has disadvantages
  - weight, cost
  - it is often not possible: e.g. when we have antennas inside (Bluetooth, GSM, …), apertures for displays, memory cards, connectors, etc.
- Always first try to shield at PCB level
  - Examples:







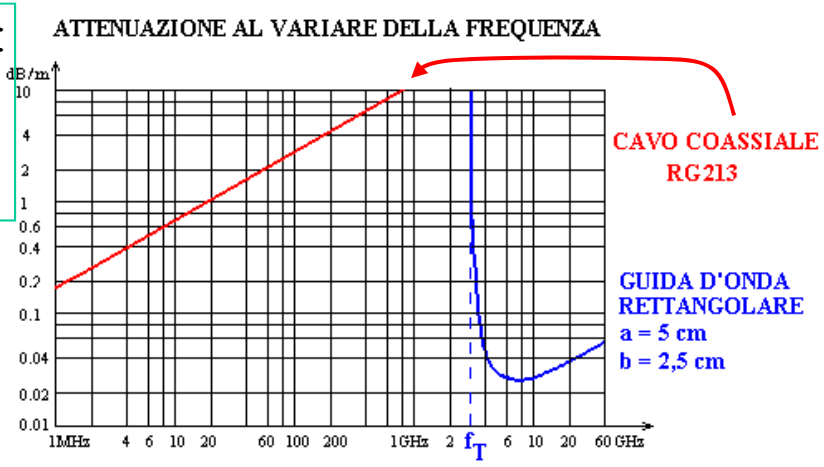
PCB partitioning and shielding

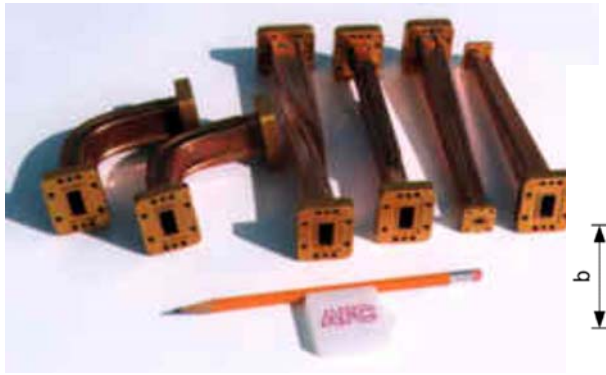
A quick introduction to waveguides

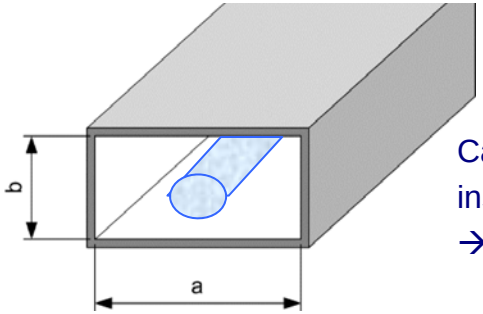
- EM-waves can propagate inside hollow waveguides above a certain frequency f_c
- Above f_c, the attenuation is very low. Below f_c, attenuation is very strong

The critical or cutoff frequency is defined by :

$$a = \frac{\lambda_c}{2} where \lambda_c = \frac{c}{f_c}$$







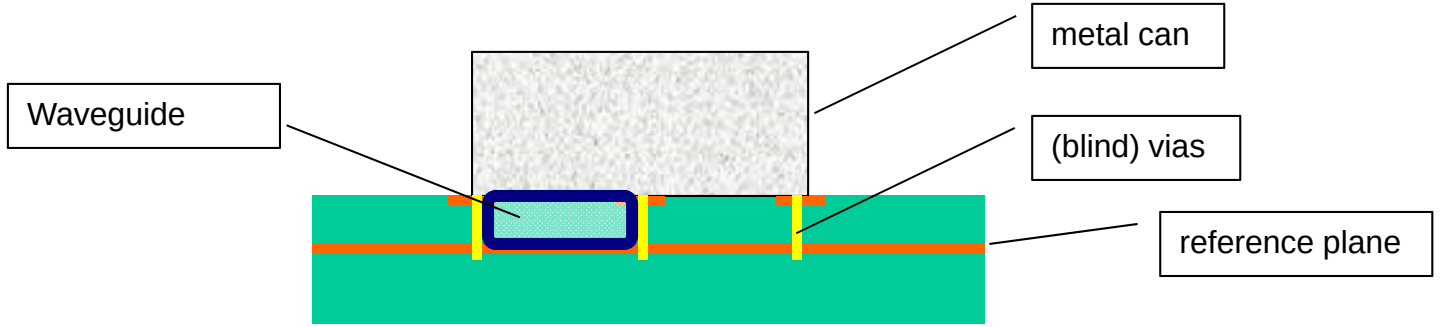
Caution: with a conductor inside it becomes a coax cable
→ $f_c = 0$!

(Source: [22])

PCB partitioning and shielding

Waveguide: what does it have to do with PCBs?

- we can use its properties to block signal propagation through the apertures inside the PCB
- this is accomplished by overlaying guard rings (top layer) and reference planes (internal layer) over a distance of λ/10 or more in order to create waveguides of this depth
- place as many blind vias on the waveguide's side walls as possible
- keep aperture of the waveguides so that a <λ/2 (at the highest signal frequency)
- do not pass signal traces inside these "waveguides"



PCB partitioning and shielding

Waveguide as resonator

- a closed metal box has many resonance frequencies inside. The lowest resonant frequency is at $f_0 = \frac{c}{2a}$, where a is the broadest side length of the box
- resonances are often unwanted inside the metal can: they change the circuit's behavior (increased coupling, HF currents, etc)
- a metal can having resonances inside has decreased shielding effect

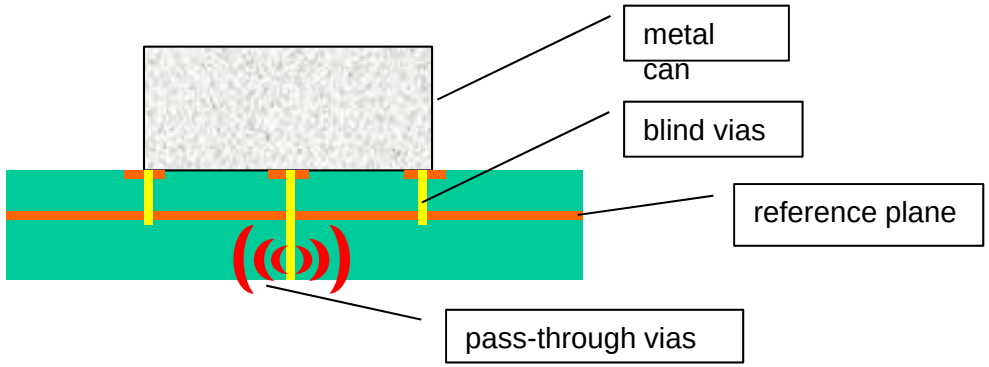
Therefore ...

- keep metal cans as small as possible
- make small compartments inside
- if necessary, coat the inner of the metal can with a film of absorbing material (ferrite)

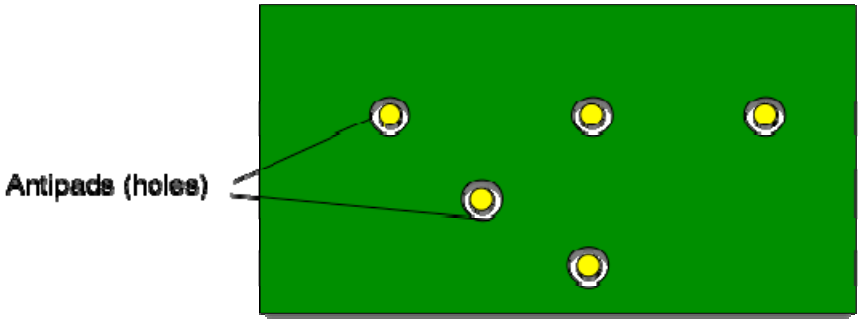
PCB partitioning and shielding

Vias: buried (blind) vs. pass-through

- pass-through vias are short stubs (signal reflections) and emitting antennas



- pass-through vias create holes in the reference plane, reducing its shielding effect



Quiz time

2. What happens if we insert a cable inside a waveguide?

The waveguide is no longer a waveguide, but becomes a sort of coaxial cable (the waveguide forms the shield). Therefore, the optical high-pass filtering property of the waveguide disappears and all frequencies (down to DC) are allowed to pass. This can void the original intent of shielding against signals having frequencies below the waveguide‘s cutoff frequency f_0

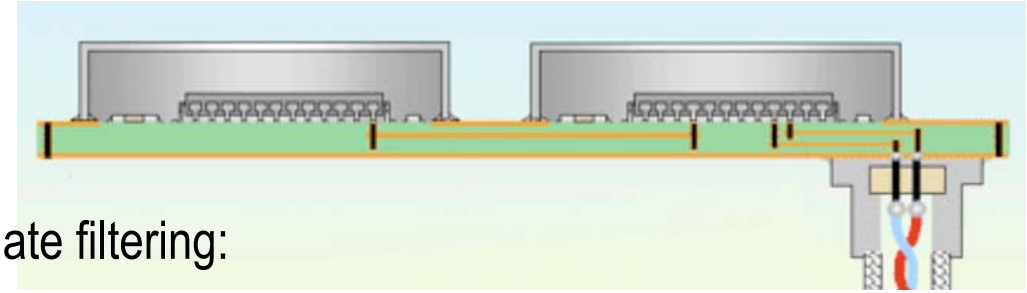
3. What should we observe when shielding parts of a PCB with metallic cans:

- ☑ material of the metal (conductivity)
- ☑ resonances
- ☑ number of contacting points to the PCB's 0V plane
- ☐ thermal stress (expansion)

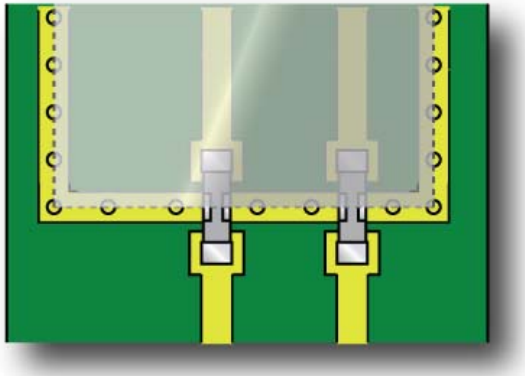
PCB partitioning and shielding

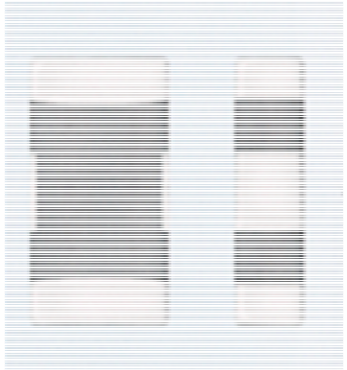
Passing signals across different PCB areas – Filtering (1)

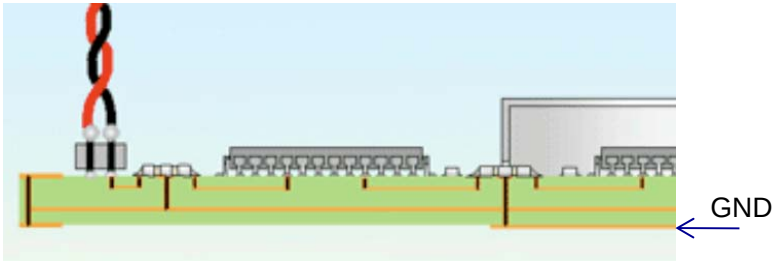
- when different functional areas are considered to be part of the same shielded group: signal traces must be shielded (=inside) as well. This pertains also to blocks connected through a shielded coax cable



- in all other cases, apply adequate filtering:



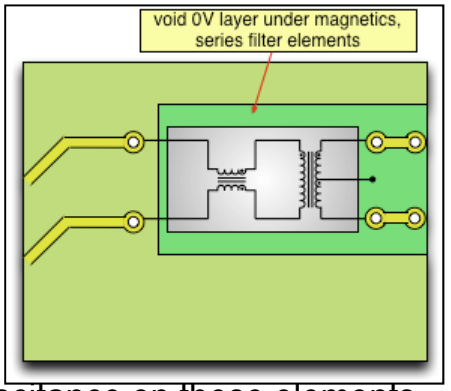




- optocouplers are a valid alternative for crossing the boundary of a shielded zone

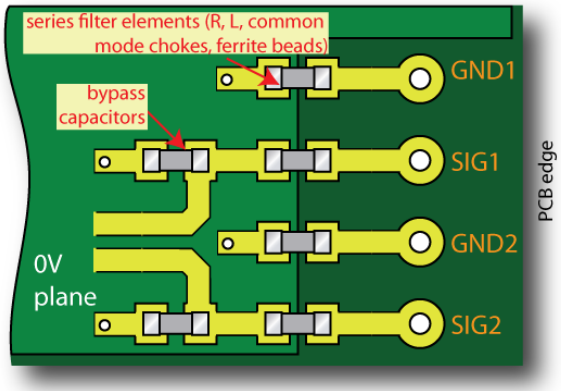
(Source: [5])

PCB partitioning and shielding



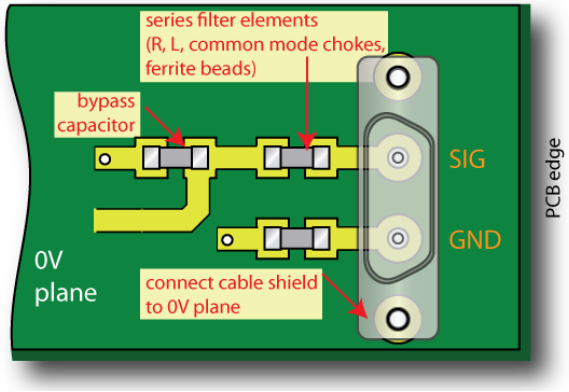
Filtering (2)

- add series L,R to I/O signals going to connectors
  - void GND area under these components to reduce input/output stray capacitance on these elements
- add capacitors to the 0V plane
  - keep connections very short. Use vias directly to the reference plane
- at frequencies > 100MHz, replace inductors with ferrite beads (SMD)
- consider using common mode chokes
- whenever possible, group all connectors on the same side of the PCB
- keep internal signals away from the connector area



example for unshielded cable I/O

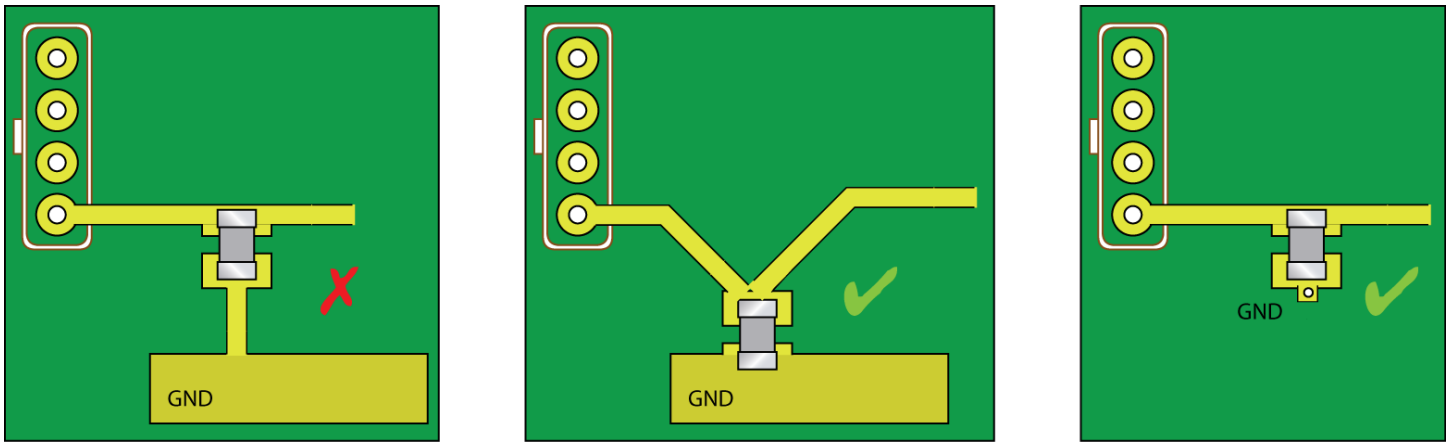
example for shielded cable I/O



PCB partitioning and shielding

Filtering (3)

- keep GND connections of filtering components as short as possible (reduce L)

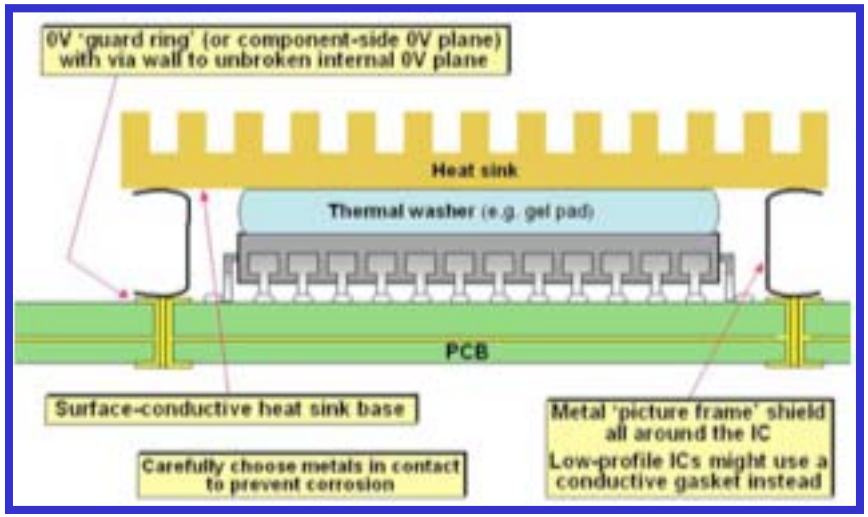


(Source: [22])

PCB partitioning and shielding

Heatsinks: can be a problem or a solution

- today's high speed logic / uP's often require heatsinks
  - a big antenna radiating the high frequency signals (clock, etc) if not handled correctly
- however, a heatsink can become the top lid of a shielding can:



(Source: [5])

PCB partitioning and shielding

A suggested workflow for the PCB design

- Use multi-layer PCBs and assign two layers to the reference planes (GND, VCC)
- Position I/O connectors at the periphery of the PCB under consideration of external cabling layout requirements (cabinet, rack)
- This defines the outer world area of the PCB
- Place "critical" components (active/passive): high speed interfaces, fast clock circuits, sensitive analog circuits, …, and partition them carefully. Keep them at some distance from I/O connectors
- This defines the inner world area of the PCB
- Draw reference planes (underlying "ground" planes)
- Draw critical nets (adjust their line impedance) and power supply lines
- Place the remaining (uncritical) components
- Route the remaining nets. This is the only task that should be assigned to the autorouter.

Quiz time

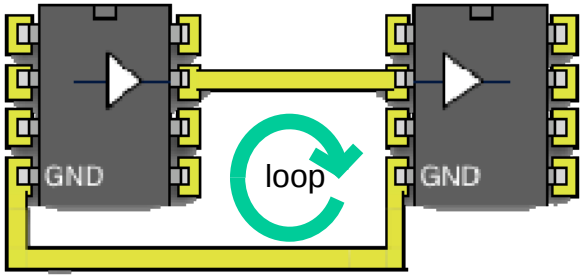
4. How can we protect the inner (sensitive) world of a PCB?

- ☐ by powering the circuit from batteries
- ☑ by partitioning
- ☑ by shielding the sensitive components,
- ☑ by filtering the signals to/from the inner part
- ☐ by placing the PCB inside a metallic enclosure
- ☐ by connecting the circuit GND to the protective earth (PE)

Image (or reference) planes

Theory:

- every signal must have a return path
- keeping the distance between "forward" and "return" path small reduces the loop area → reduced emissions (see "E-M field radiated by a small current loop")



- when an image plane is present, the return current will choose the path forming the smallest loop:
  this is the solution for the minimal inductance and the minimal stored energy in the magnetic field

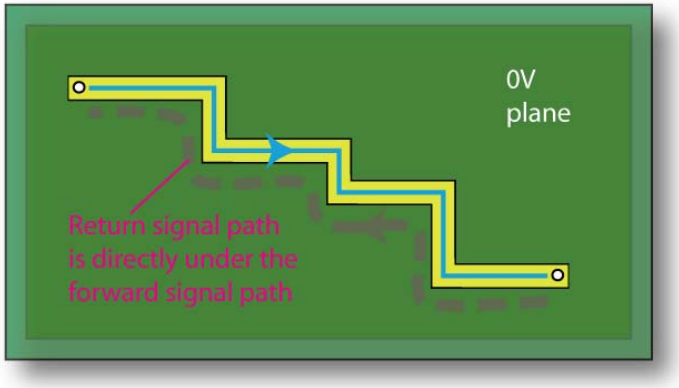
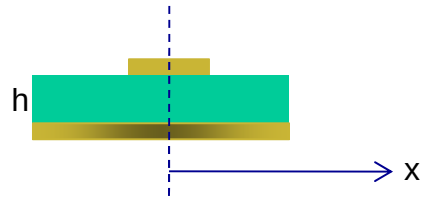


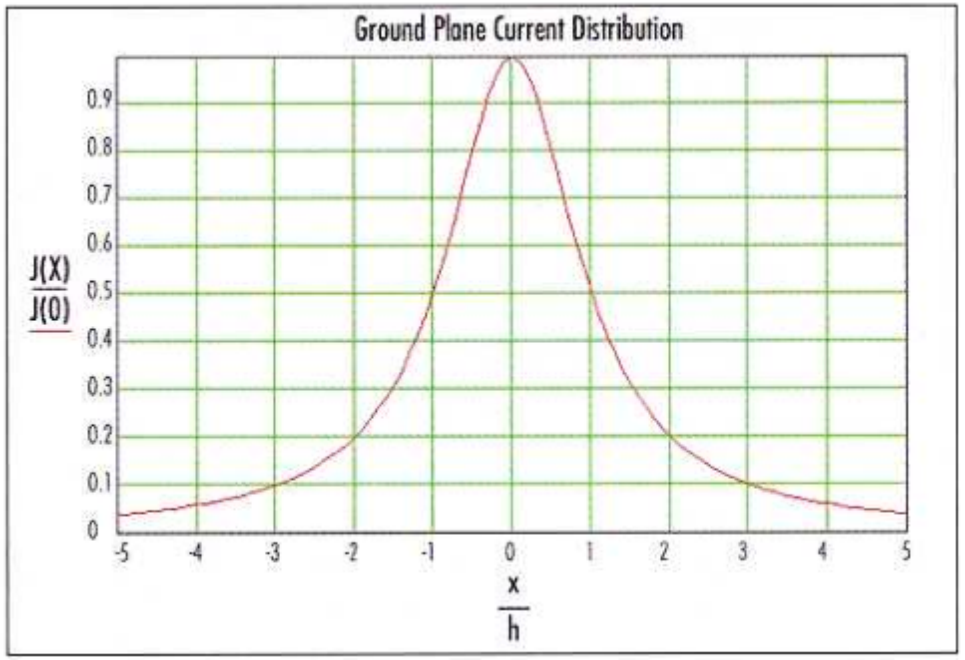
Image (or reference) planes

Return current distribution in the image plane:

- in the image plane, the return current concentrates directly under the signal trace
  example: if h=1mm then at x=2mm the current is already decreased to <20%
- the current density J at a distance x from the center under the signal trace is:

$$J(x) = \frac{I_0}{\pi h} \cdot \frac{1}{1+\left(\frac{x}{h}\right)^2}$$



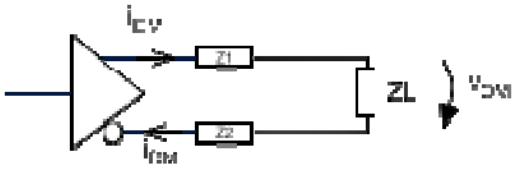


(Source: [19])

Image (or reference) planes

What is the goal?

- keep in mind - we want to:
  1. avoid that some signals on the PCB perturbate others
  2. keep RF emissions of the PCB (and attached cables) at a minimum
- RF fields generated by differential mode currents (2slides back) are only a (minor) part of the problem, because they are confined to small loops (at far field they cancel each other)



- Common mode currents of smaller amplitude generate much higher emissions (they "add" at far field – "dipole" emission)

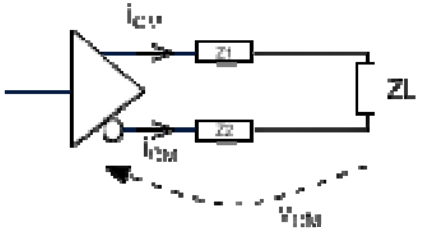
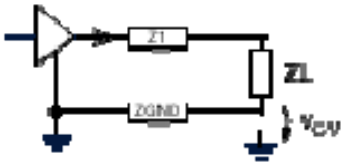


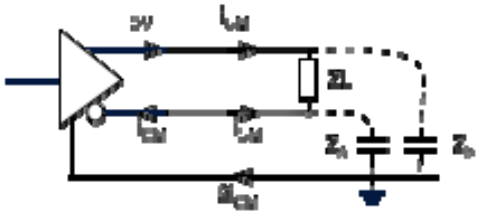
Image (or reference) planes

Examples of how common mode currents are generated

1. consequence of *ground noise* generated by series impedance in the GND return trace



2. even if return is not through GND (differential line), different parasitic loading can induce common mode currents



3. Noise sources external to the circuit

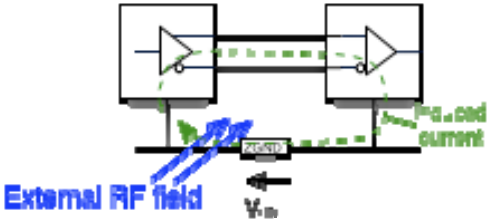
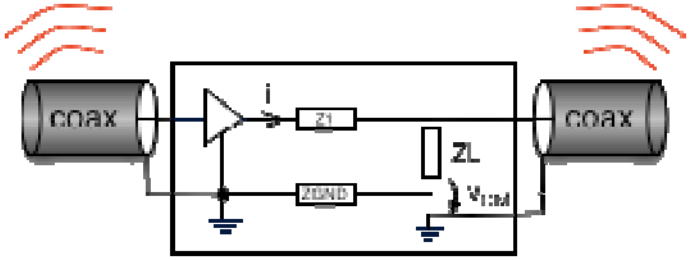


Image (or reference) planes

Why is common mode noise so undesired?

1. *ground noise* can translate to emissions if cables are attached (dipole!)



2. common mode currents can produce unwanted voltages inside the circuit.
   In the example, when $Z_A \neq Z_B$ then i_{cm} produces a voltage on Z_L

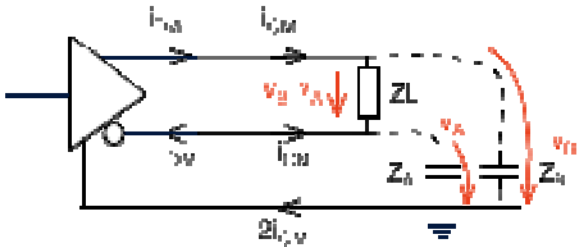


Image (or reference) planes

Common mode currents/voltages in general happen…

- if forward and return currents do not cancel out locally. This happens when:
  - return path is far from forward path and has different impedance or parasitic load
  - presence of multiple return paths (wanted and unwanted (=parasitic))
- if there is voltage drop in the GND return path ($Z_{GND} \neq 0$) → GND noise

⇒ always provide a return path as close as possible to the forward path!

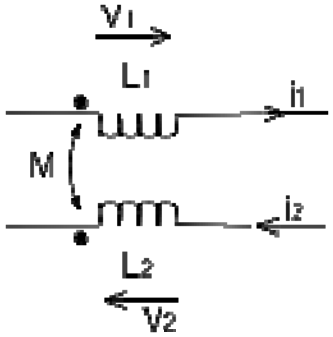
- this is best accomplished by a near reference or image plane (GND)

Minimizing the return path impedance is important because

- voltage drop on return path (GND noise) is reduced
- return current avoids searching for alternate (parasitic) paths

Image (or reference) planes

Mathematical proof that the effective impedance is minimized when forward and return traces are near:



$$V_1 = L_1 \frac{di_1}{dt} - M \frac{di_2}{dt}$$

$$V_2 = L_2 \frac{di_2}{dt} - M \frac{di_1}{dt}$$

if $i_1=i_2=i$ then the voltage drop on each path is $V = (L - M)\frac{di}{dt}$ and we call (L-M) the "net partial inductance of each conductor".

- even if the traces have L_1, L_2 (≠0), the voltage drop can be nearly zero if M is maximized. This is the case when the two lines are as close as possible.
- this is best achieved with an uninterrupted image/reference plane for the return signal, at a PCB layer adjacent to the layer carrying the signal trace.

- it can be shown [20] that ground noise on a 2-layer PCB can be reduced by simply placing an unconnected metallic surface (image plane) near the PCB
  (a full GND area (layer) is however still better!)

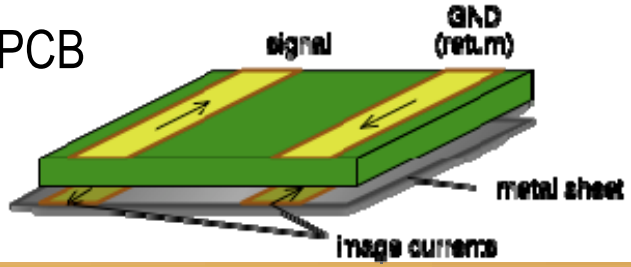
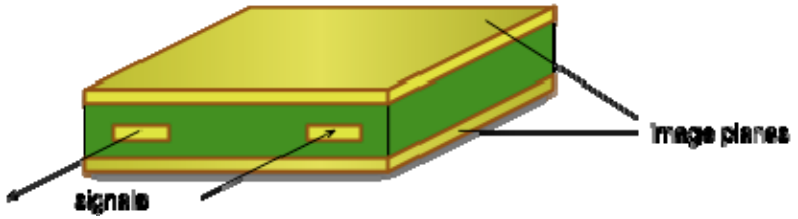


Image (or reference) planes

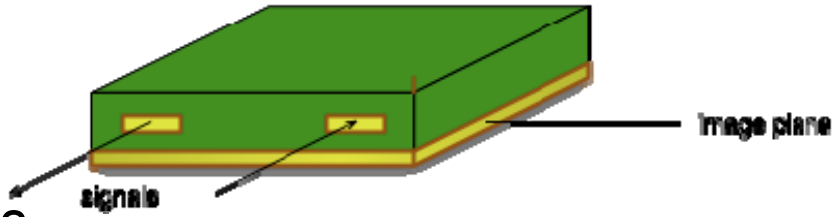
Stripline technology

- embed signal traces between two image planes ("sandwich" construction) for best shielding of noisy signals to effectively protect sensitive analog traces against external noise



Microstrip technology

- this is the most commonly used technology. It is a little less effective than stripline, however.

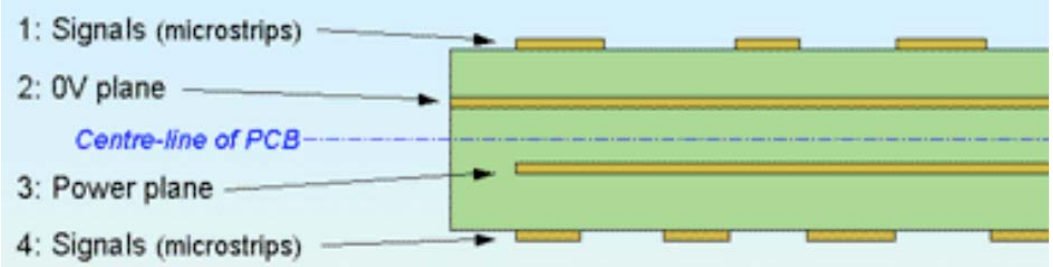


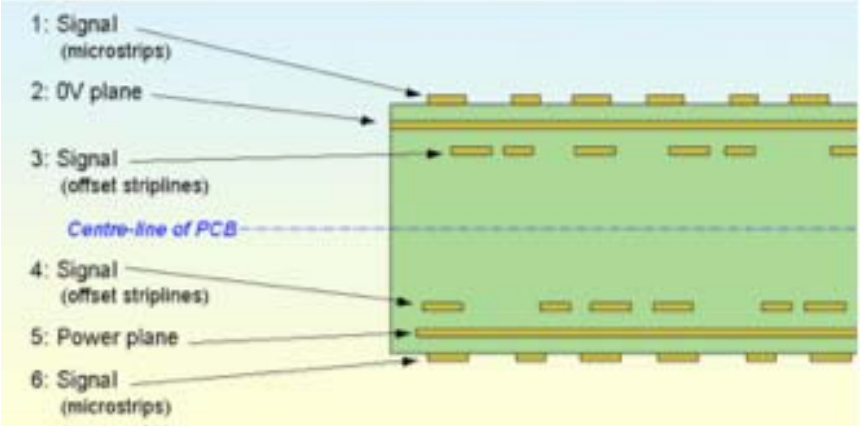
Which image plane is most suitable?

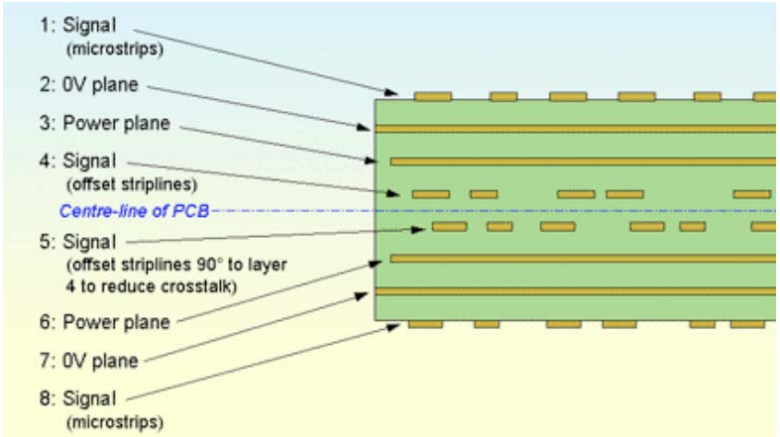
- both GND and VCC can be used. VCC however is generally more noisy than GND.

Image (or reference) planes

Examples of reference planes in multilayer PCBs







(Source: [5])

Quiz time

5. What is an image plane and how does it work?

Answer:

An image plane is a continuous (uninterrupted) copper plane in one or more PCB layers. It is connected to GND (or VCC) and serves as the return path for signal traces on other (adjacent) PCB layers.

PCB partitioning and shielding

To split or not to split the GND plane ?

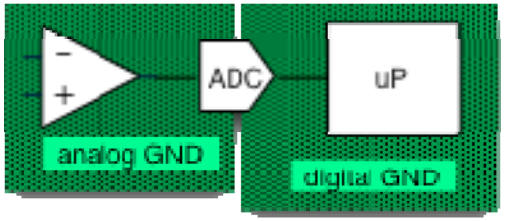
- Literature is quite discordant on this subject (Books, Application Notes, …)
- up to 10-15 years ago (<30 MHz clock speeds) partitioning the GND plane was a recommended practice
- today, the specialists tend to agree that this should be done only in very special circumstances (e.g. isolation required) and under advice of an EMC expert.

PCB partitioning and shielding

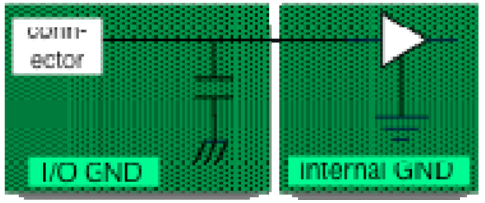
Rationale behind the idea of splitting the GND plane

old

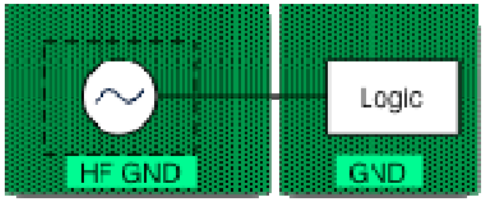
- Some examples:
  - Separate GND for sensitive analog circuitry from noisy digital



  - separate GND for I/O signals



  - high-speed oscillator

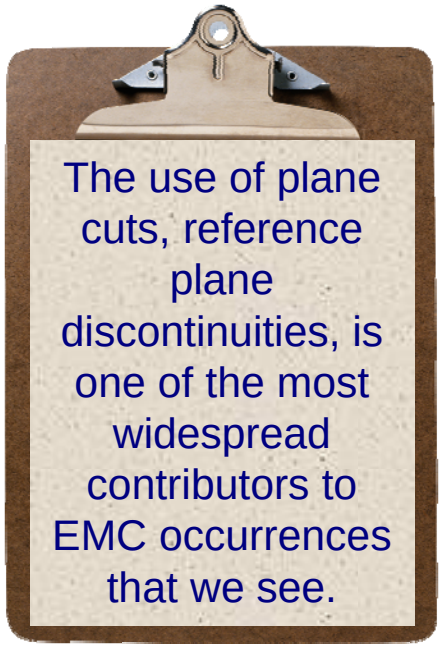


PCB partitioning and shielding

Arguments of the opposers of split GND concepts

- most recent publications and Application Notes suggest not to split the 0V plane

(K. Armstrong, EMC consultant, [5])

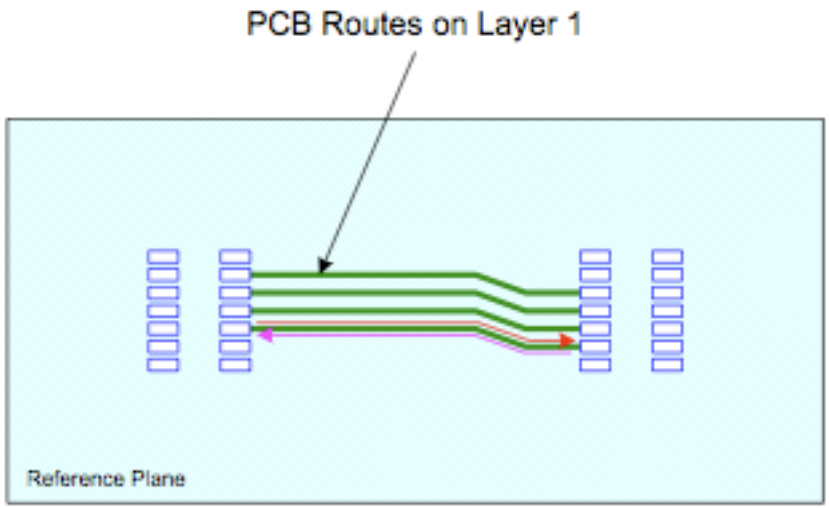


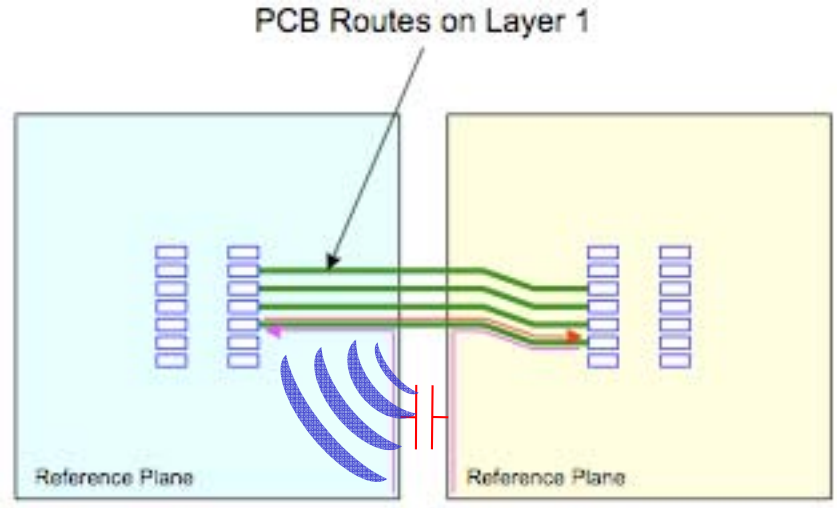
(SMSC Semiconductor, world leading supplier of fast communication chips, [21])

PCB partitioning and shielding

Why splitting a 0V plane can be a bad choice

- every signal has its own return path. Typically, the return path finds its way in the 0V plane just under the signal trace.
- voiding or splitting the plane forces the return path to take a detour
- forward and return path forms a loop. Increasing the loop area inevitably increases its HF radiation (loop antenna)
- planes having a HF voltage difference act as a dipole antenna

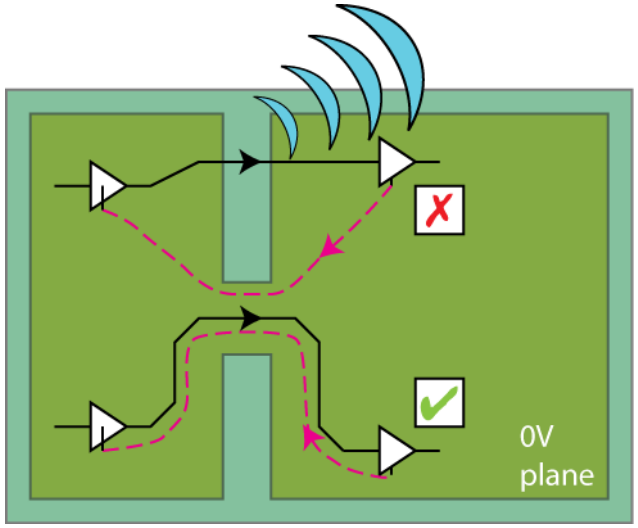


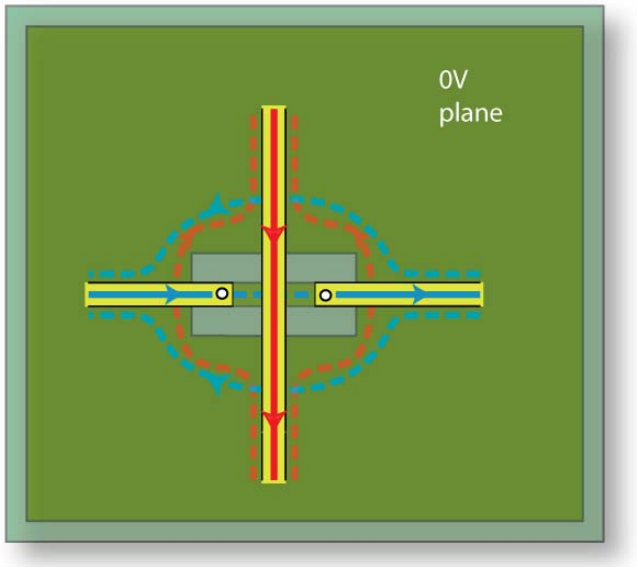


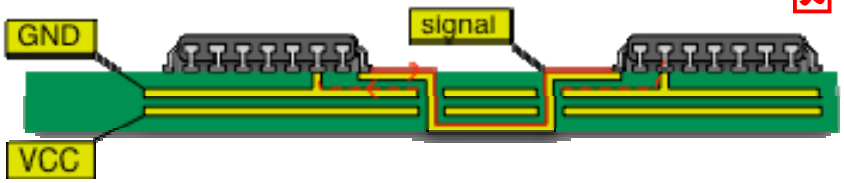
(Source: [21])

PCB partitioning and shielding

Bad examples







- do not void a reference plane just to route a signal
- always think at the return paths

(Source: [11])

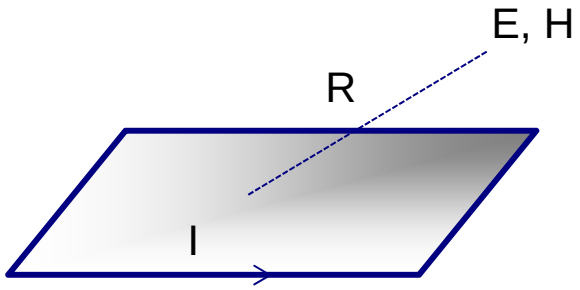
PCB partitioning and shielding

Electromagnetic field radiated by a small current loop

- in the main radiating direction, a PCB trace carrying a current I and forming a loop of area A generates an electromagnetic field at a point distant R in the order of:

$$E \sim \frac{k^2 IA}{4\pi}\sqrt{\frac{\mu}{\varepsilon}}\left(\frac{1}{R}\right)$$

$$H \sim \frac{k^2 IA}{4\pi}\left(\frac{1}{R}\right)$$



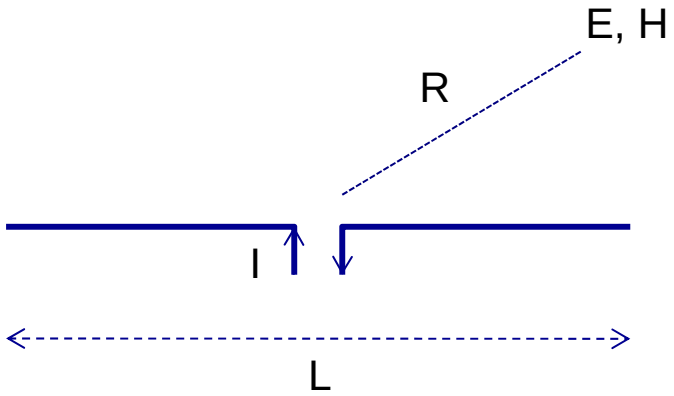
- where:
  - I is the current
  - A is the loop area
  - R is the distance of the measuring point
  - $k = \frac{2\pi}{\lambda} = \frac{\omega}{c}$ (ω is the current's frequency)

PCB partitioning and shielding

Electromagnetic field radiated by a small dipole antenna

- in the main radiating direction, a small dipole antenna fed by a current I and having a length L generates an electromagnetic field at a point distant R in the order of:

$$E \sim \frac{I \cdot L \cdot f}{4\varepsilon_0 R}$$

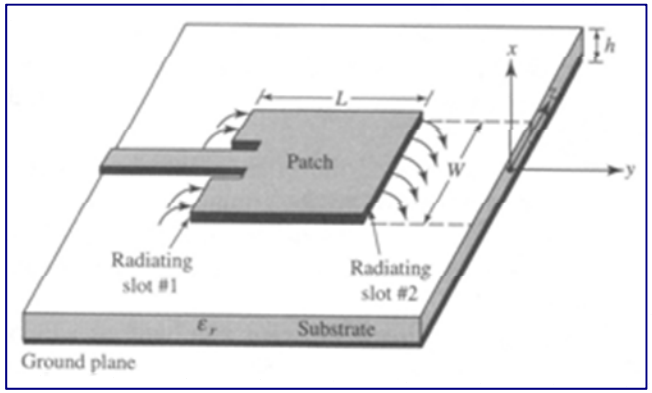


- where:
  - I is the current
  - L is the dipole's length
  - R is the distance of the measuring point
  - *f* is the current's frequency

PCB partitioning and shielding

Possible (but rare) issues with continuous reference planes

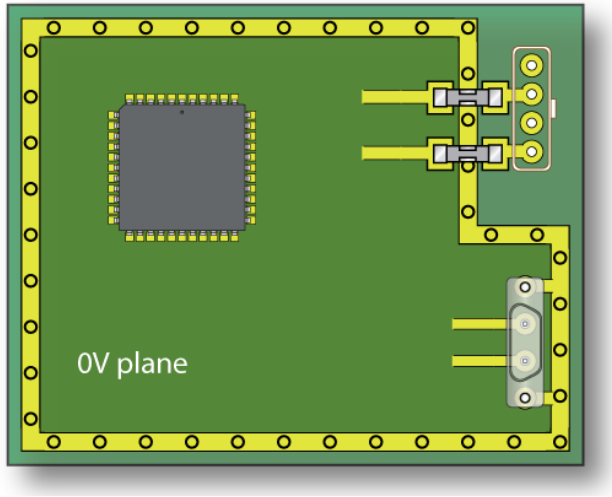
- if we are unlucky, we could excite the resonant frequency of the plane
- if we have more planes (0V, power) in a multilayer PCB, resonance can build up between them
- the resonant field between two planes can escape along the PCB edges



A patch antenna

Countermeasures:

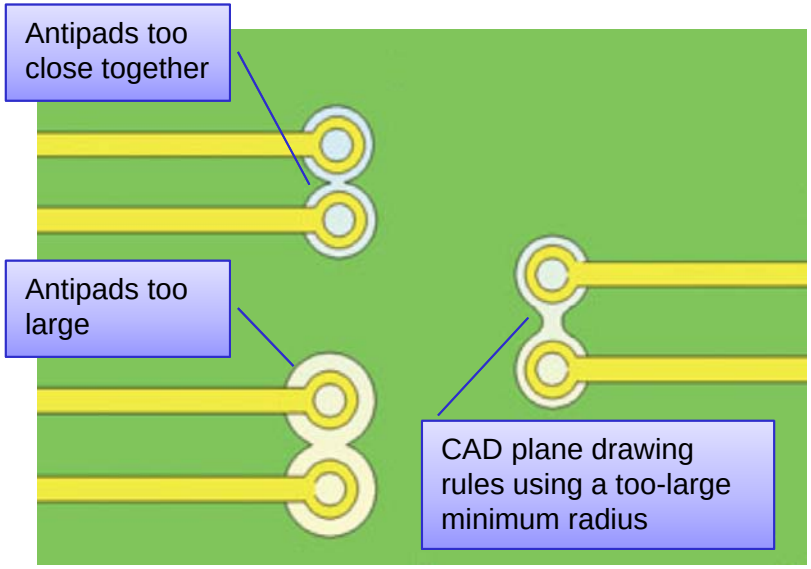
- put many vias at short distance (λ/10) to contact the various 0V planes
- put many bypass capacitors or some shunt resistors between 0V and power planes
- to avoid fringing fields from the PCB edges, put a GND guard ring on the top and bottom layer and connect them with many vias to block emission

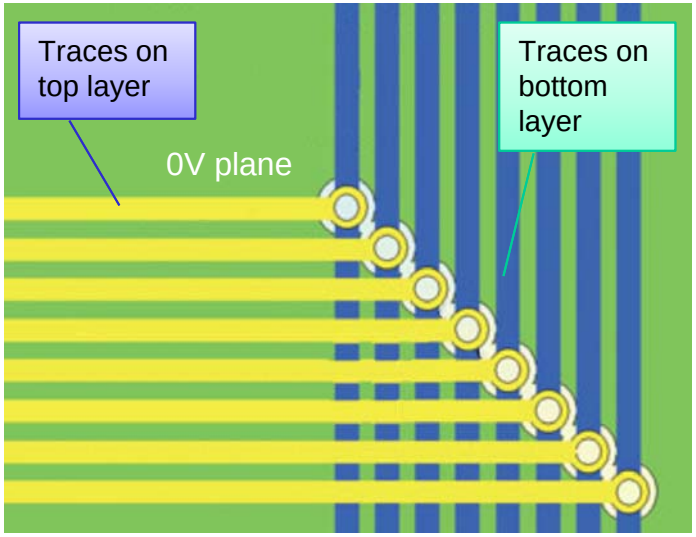


PCB partitioning and shielding

Avoid accidental interruptions of reference planes

- do not place antipads too close together





- reduce the number of vias crossing (but not contacting) the reference plane
- reduce the number of THT components

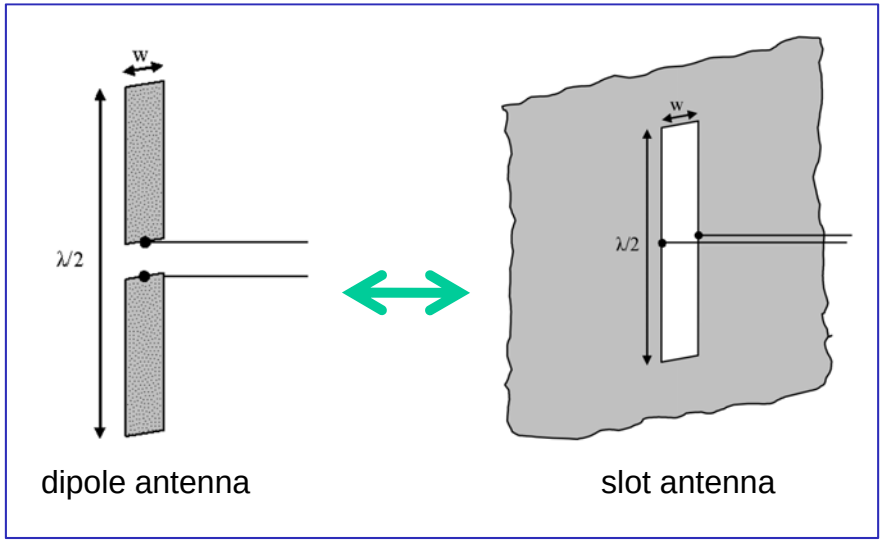
(Source: [5])

PCB partitioning and shielding

Beware of slot antennas

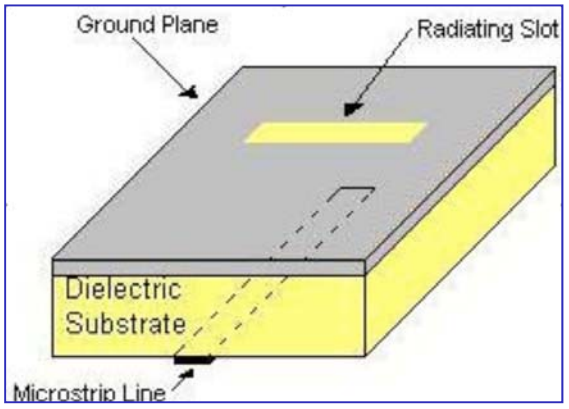
- a slot antenna is an "inverted" dipole, with equivalent radiation characteristics
- it can be excited by an voltage source or an electromagnetic field
- any interruption in a reference plane is a potential slot antenna, when a signal trace carrying an AC signal crosses over/under it

Principle:

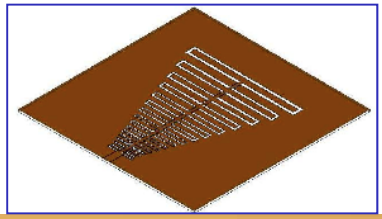


(Source: [22])

Excitation example:



Log-periodic slot antenna on PCB:



PCB partitioning and shielding

A few situations where we may still want to split the planes:

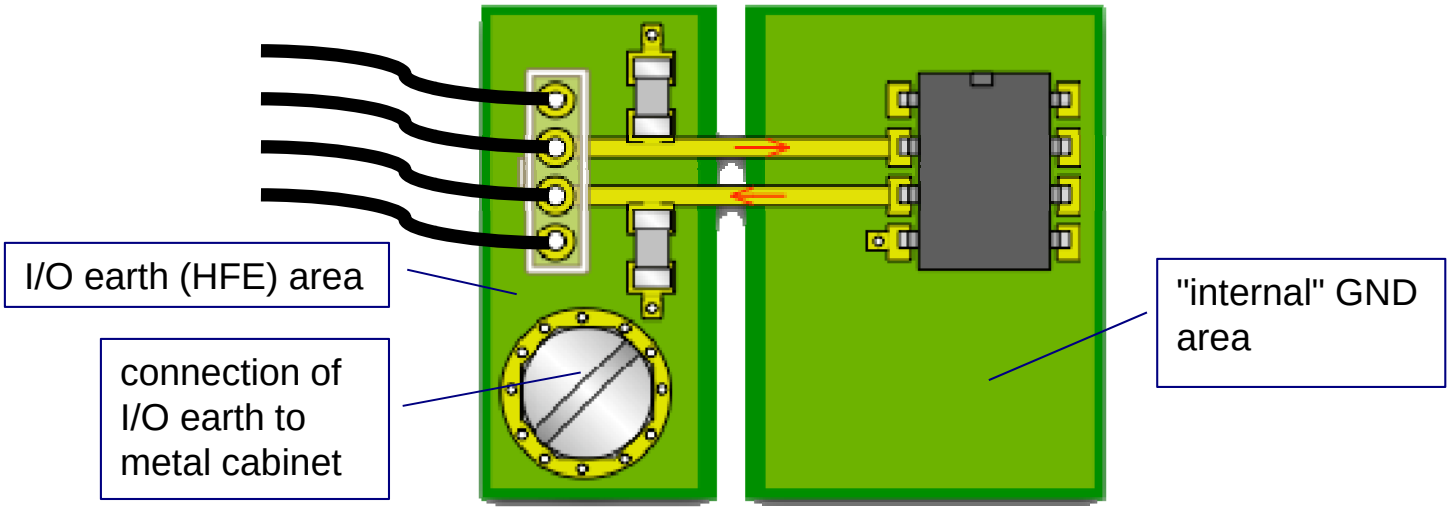
- we want to control where a particular return current travels or where it should never go
  - very high impedance (analog) circuits
  - very small currents (sensor signal conditioning circuits)
  - outputs connected to very noisy, high power (electromechanical) equipment
- isolation needed (safety): optocoupler circuits
- reduction of parasitic C to GND in filters, line transformers

→ consider connecting the different reference planes with a number of small capacitors. They do not influence the low frequency behavior but help reduce the HF emissions due to differential mode noise between the planes

PCB partitioning and shielding

A widespread solution for I/O sections

- Purpose: shunt HF noise (incl. ESD, burst) captured by I/O cables to the metal cabinet with the shortest possible path
- Always provide a nearby signal return path also in the I/O cable



Quiz time

6. Describe some sorts of antennas and how they can involuntarily be created in a PCB

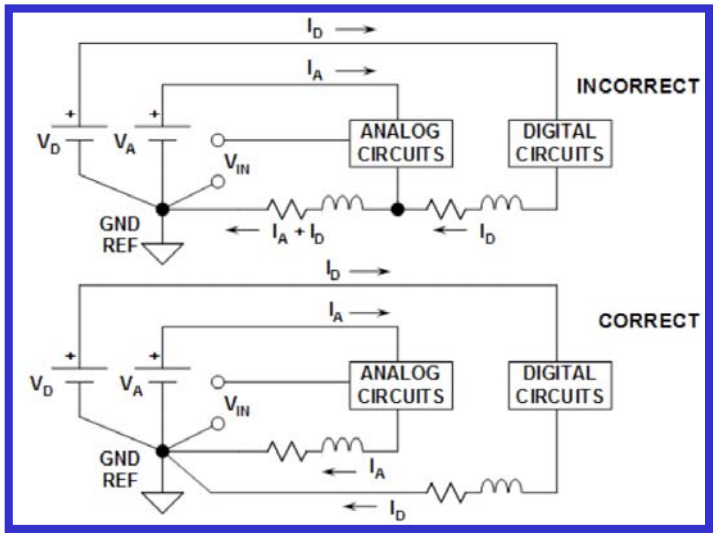
Answer:

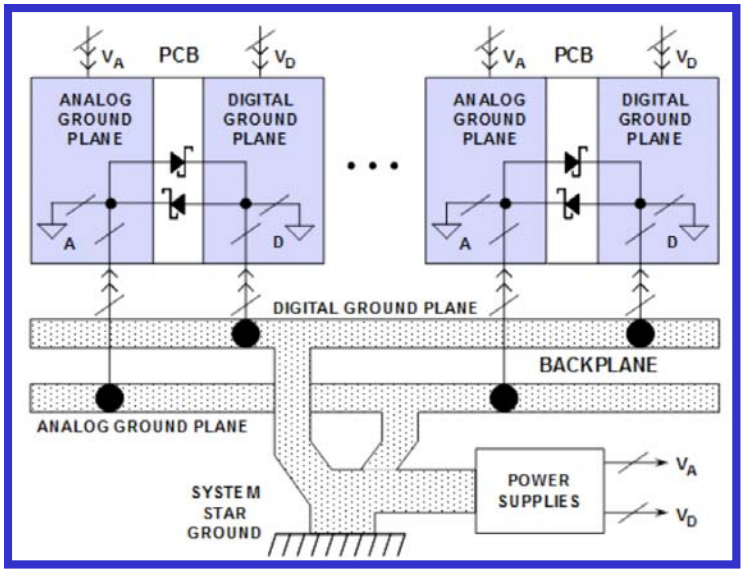
- patch antenna (slide 44)
- slot antenna (slide 46)
- dipole antenna (slide 31)
- and generally, antennas formed by PCB traces with missing or far return paths (loop antennas) and antennas formed by attached cables

PCB partitioning and shielding

Mixed signal circuits (1)

- manufacturers of mixed signal components often suggest to implement split GND planes (AGND, DGND)
- the reason is to avoid having digital noise superposed on the analog signal





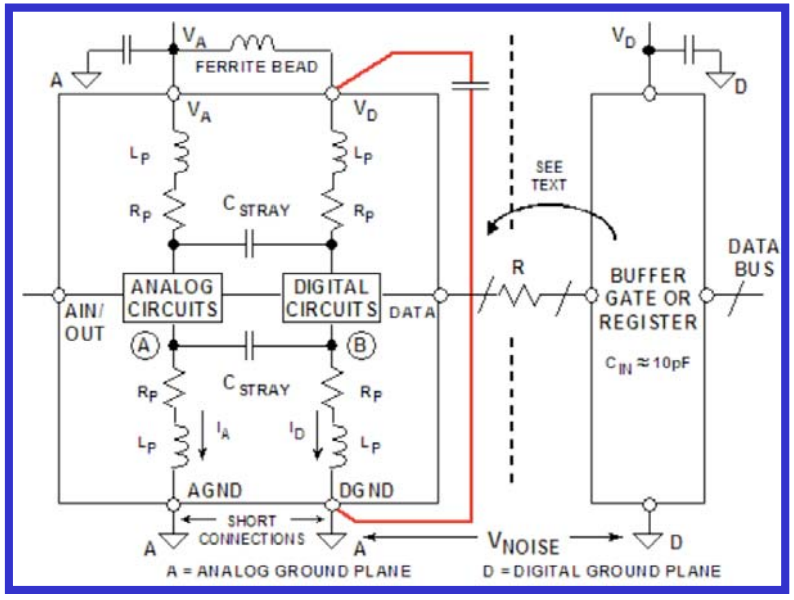
- Analog Devices suggests connecting the two GNDs via anti-parallel shottky diodes or a ferrite bead

(Source: [2])

PCB partitioning and shielding

Mixed signal circuits (2)

- many A/D, D/A converters have separated *analog* and *digital* GND / supply pins
- generally, this is only for practical reasons, because internal bonding has L≠0 and therefore with a single GND pins, digital noise would couple into the analog section.



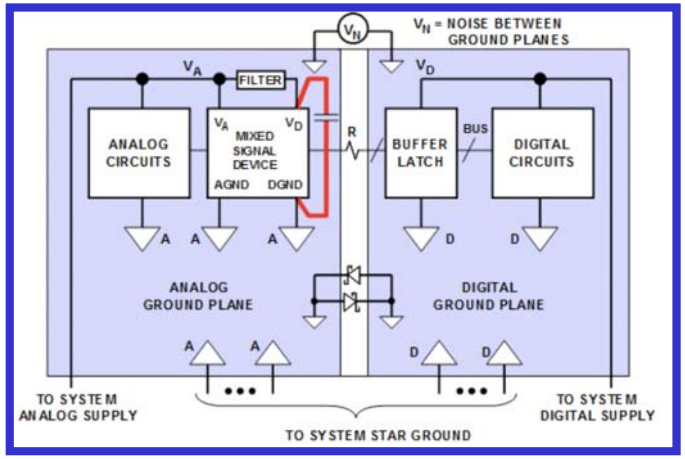
(Source: [2])

But externally, we can tie them together (at AGND) in most cases (next slide)

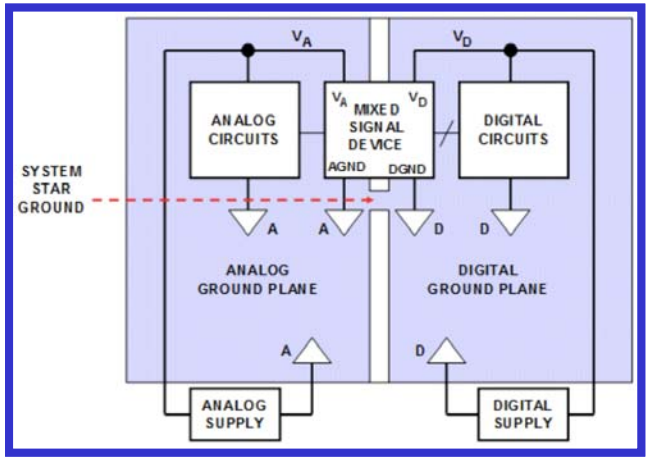
PCB partitioning and shielding

Mixed signal ICs with low digital currents

- connect AGND and DGND pins together to the analog reference plane (the IC is located completely in the analog part (*left*)), or place it over the star connection point between AGND and DGND (*right*) (if we have only one ADC):



PCB with single or multiple mixed signal ICs



PCB with single mixed signal ICs

- further decouple the AVCC with a ferrite bead and its own decoupling capacitor
- to further reduce noise consider adding a digital buffer IC on the digital interface
  - decouple noise from the digital bus (the buffer is connected to DGND)
  - the buffer reduces loading (=> current drawn) on the digital outputs of the ADC (use series resistors to further reduce the current

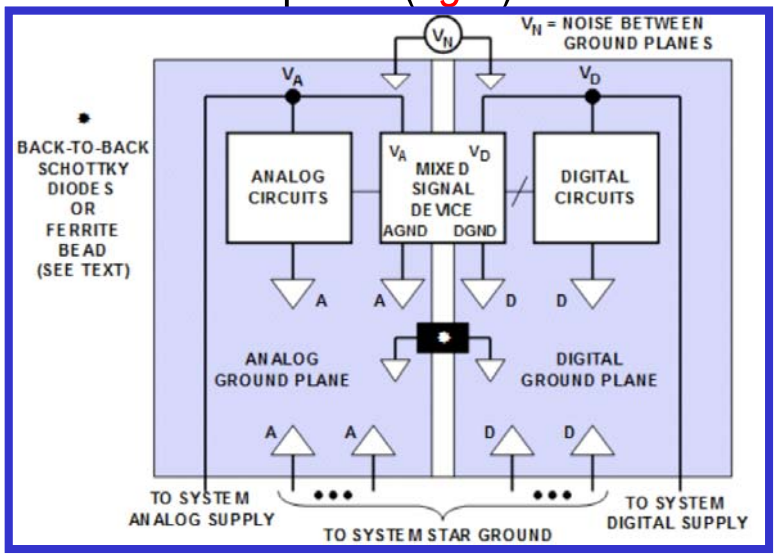
(Source: [2])

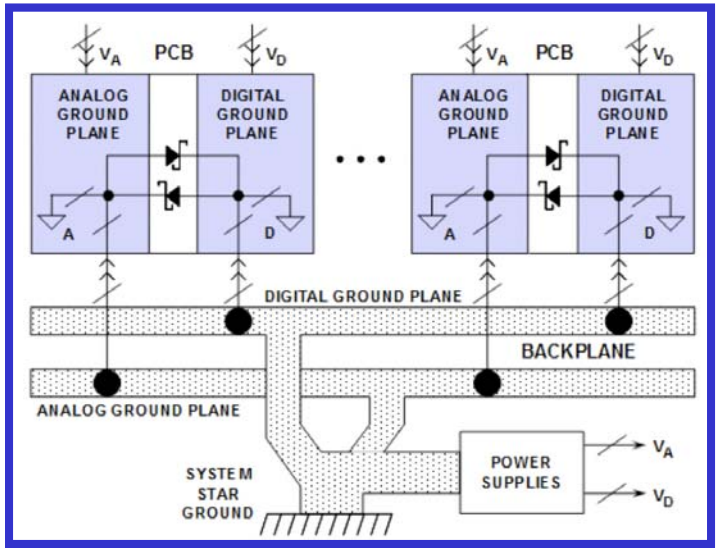
PCB partitioning and shielding

Mixed signal ICs with high digital currents and/or multicard systems

- connect AGND and DGND pins to the respective reference plane (*left*).
- this scheme works only for ICs designed with well isolated analog/digital circuits
- tie AGND and DGND together in a "star point". In multicard systems this can be at the backplane (*right*)

(Source: [2])





- always refer to the IC manufacturer's recommendations, use evaluation boards!

PCB partitioning and shielding

Mixed signal circuits – sampling clock circuits (1)

- jitter on the sampling clock severely deteriorates the SNR of an ADC
- SNR of an ideal ADC (infinite resolution) exposed to clock jitter:
  where f is the signal frequency, t_j is the sampling clock jitter

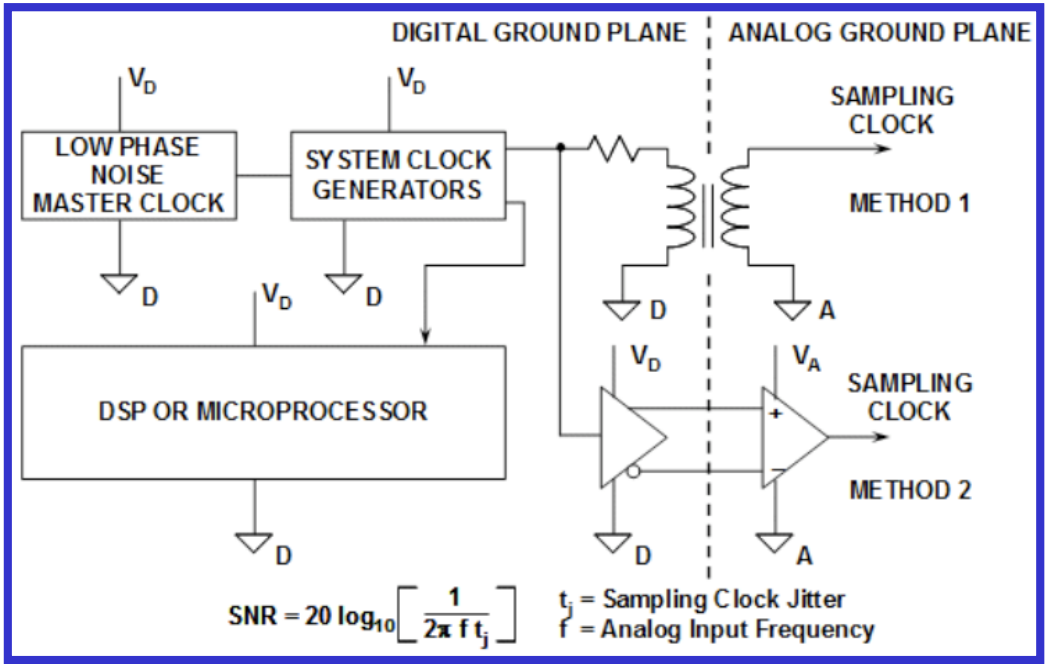
$$SNR = 20\log_{10}\left[\frac{1}{2\pi \cdot f \cdot t_j}\right]$$

- noise superposed to a clock signal translates into clock jitter
- the best solution is to create the clock locally (in the analog, low noise section)
- use a low jitter oscillator such as a quartz crystal. Beware from programmable (PLL) oscillators.

PCB partitioning and shielding

Mixed signal circuits – sampling clock circuits (2)

- if the clock comes from the digital section, try to minimize its superposed noise (against AGND) by transmitting it over a differential line (originating directly at the oscillator) and/or using isolation (transformer, optocoupler)



(Source: [2])

- *we will see more on clock jitter ahead (digital circuits)…*

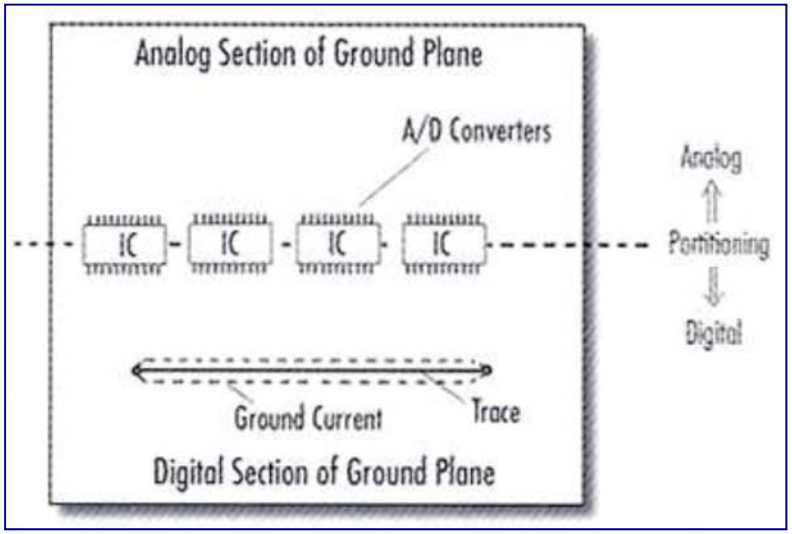
PCB partitioning and shielding

Mixed signal circuits – more suggestions

by Henry Ott, a renown EMC consultant (www.hottconsultants.com):

- split the power (VCC) plane: AVCC, DVCC
- generally avoid splitting the GND plane
- instead, partition carefully the components: analog and digital in different PCB areas
- noisy digital return currents flow directly under the respective signal traces and do not propagate inside the analog section
- do not route digital signal traces in the analog zone

(Source: [19])



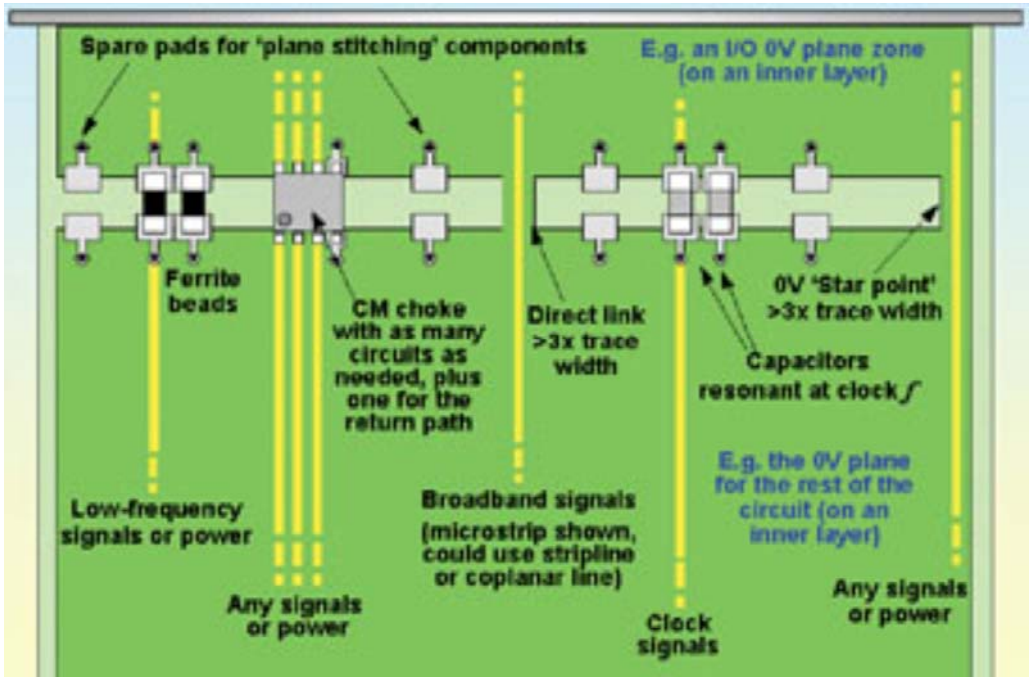
- in case of doubt you can always design a PCB with split grounds, but provide means for connecting the two planes together at intervals of λ/10 with jumpers or zero ohm resistors. Laboratory tests will tell which solution is better.

PCB partitioning and shielding

How to cross a plane split with signals

- always provide a nearby path for the return signal
- it is a good place to use a common mode choke, an optocoupler
- it is also a good place to add signal filters (π, LC, etc)
- or provide a "bridge" between the two planes (see center of the figure)
- use differential signal lines

☑



(Source: [5])

Quiz time

7. PCBs with separate copper areas for different grounds (analog/digital):

- ☐ are a good idea (explain why)
- ☐ are not a good idea (explain why)
- ☑ should be used only under special circumstances, i.e. when: _____

- *when dealing with sensitive analog circuits (high impedance, very small signal)*
- *when outputs are connected to very noisy, high power (electromechanical) equipment*
- *when isolation is needed (safety reasons/regulations)*
- *to reduce parasitic C to GND in filters, line transformers*

And only if we are very sure about what we're doing or under an EMC expert's advice

PCB partitioning, shielding, image planes

Conclusions

- the first and best guess is: make one single reference plane
- read the recommendations of the IC manufacturers. Purchase evaluation kits and see how their PCB layout is made
- be skeptical about Application Notes dating prior to 2000-2003, suggesting a partitioned ground plane. Exceptions:
  - noisy I/O sections
  - analog input sections with low noise or low leakage current requirements
- it is more important to carefully partition the components (analog and digital circuits should be placed in different PCB regions). Avoid placing digital signal lines inside the analog zone.
- make your PCB design so that it can be configured to various solutions (split or common ground plane, various kinds of short-lays between the planes).
- Tests will determine the most favorable layout concept

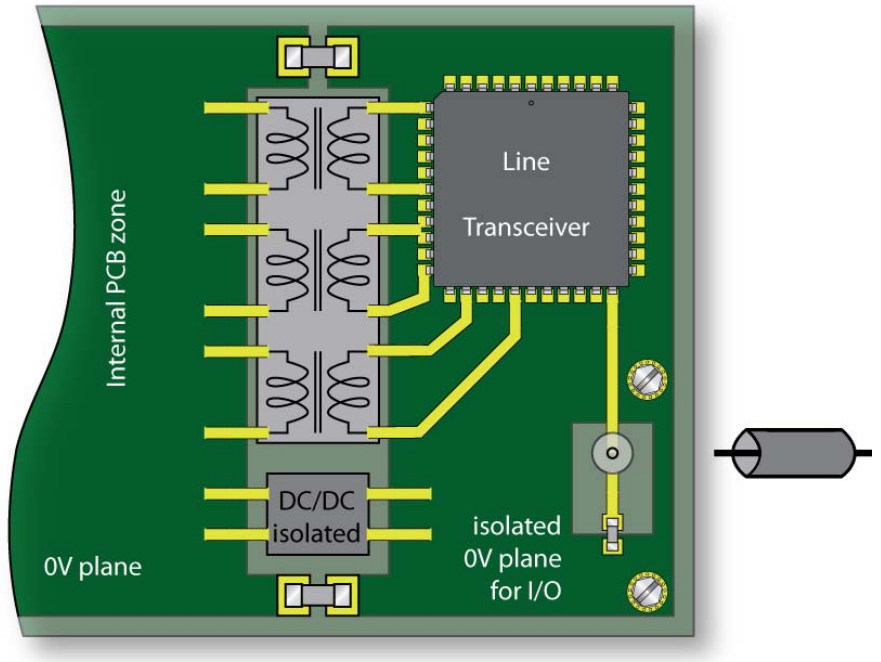
An Application Case

Ethernet LAN (10Base2 and 100BaseTx) interfaces

PCB partitioning and shielding

An application case: Ethernet interface

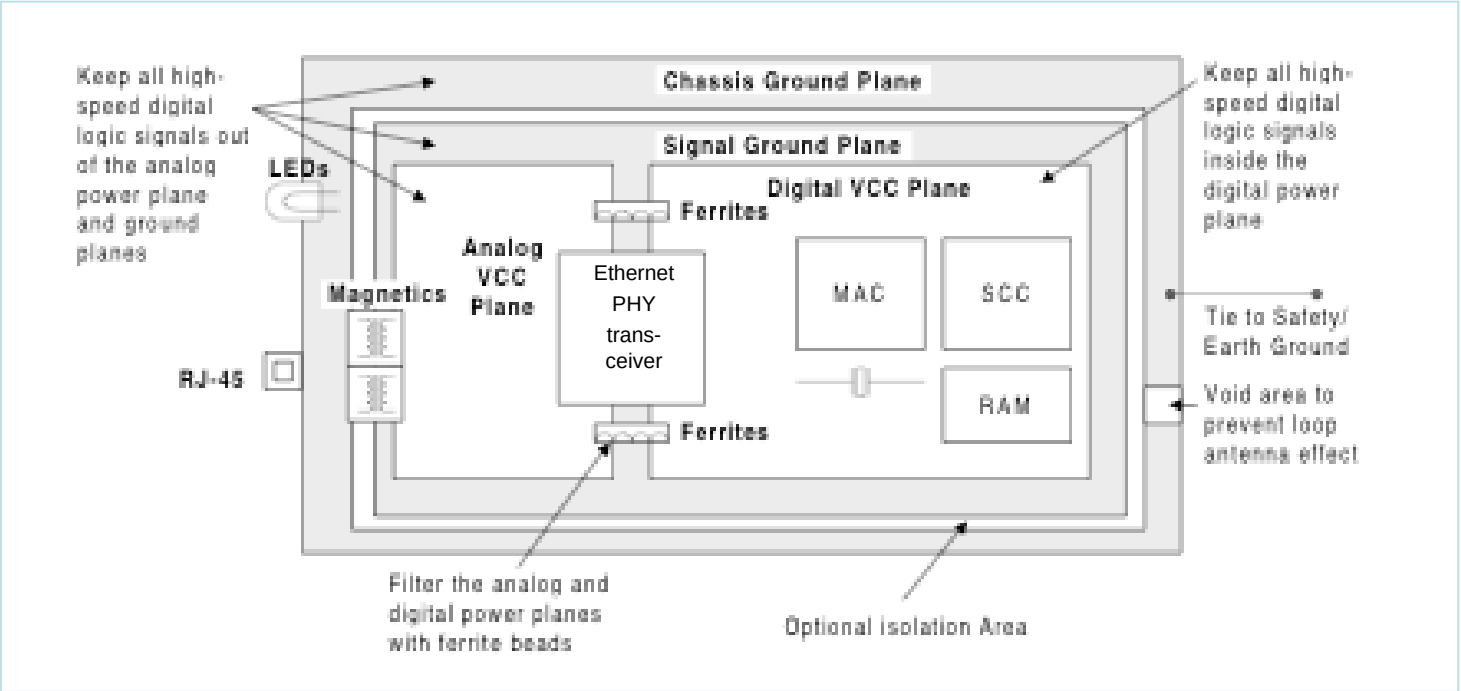
- Ethernet uses isolation between network cable and controller/equipment
- 10Base2 standard is for coaxial cable (below),
- 100BaseTx is for twisted pair cable (RJ45)(*next slides*)



PCB partitioning and shielding

An application case: Ethernet interface

- A chip manufacturer's layout recommendation for a fast Ethernet interface

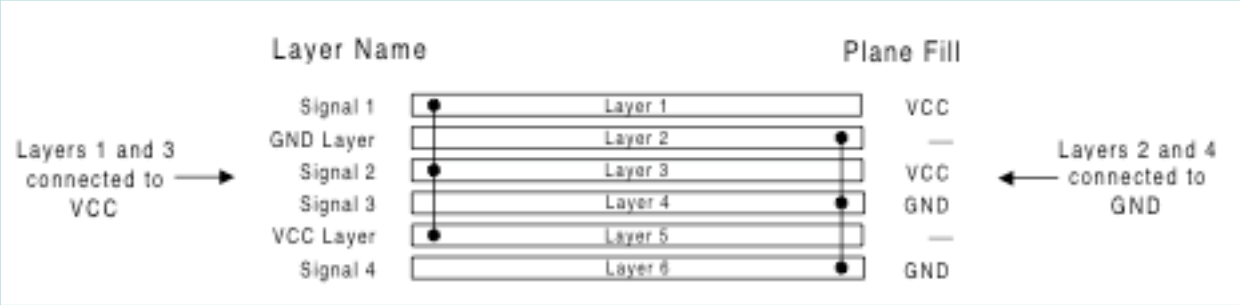


(Source: LevelOne/Intel)

PCB partitioning and shielding

"Signal layer filling" technique *(suggested by a chip manufacturer)*:

"When possible, fill in unused areas of the signal planes with solid copper and attach them with vias to a VCC or ground plane that is not located adjacent to the signal layer. This technique can improve capacitive coupling of the power planes"

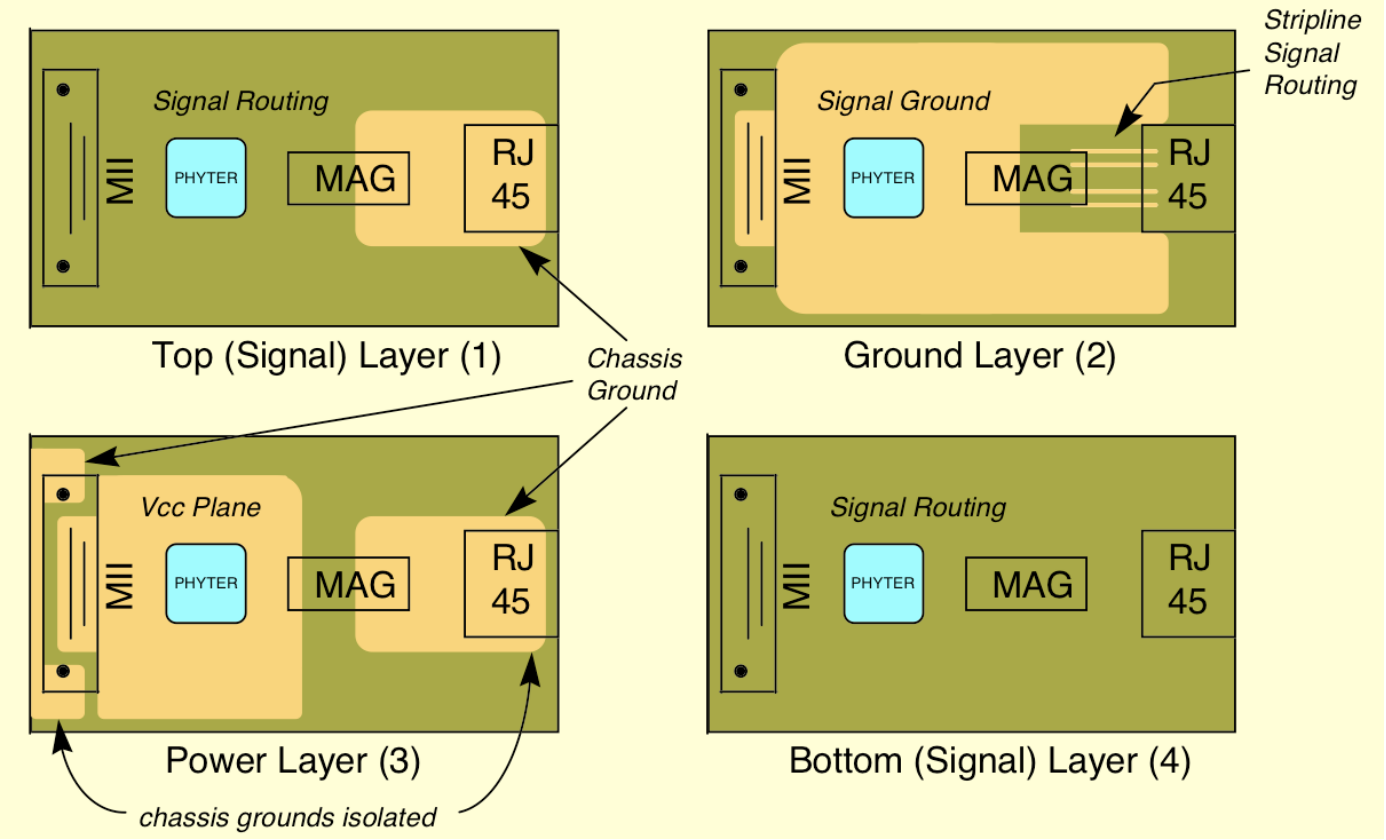


(Source: LevelOne/Intel)

PCB partitioning and shielding

Application case: Ethernet interface (from another IC manufactuer)

- Another chip manufacturer's layout recommendation for a fast Ethernet interface



(Source: National Semiconductor)

Exercises

9. The return current of a signal is always on the nearest conducting plane, regardless of its DC voltage?

- ☑ correct
- ☐ incorrect

Exercises

10. What is common mode noise and how can it be avoided?

Answer:

Common mode noise is noise that's present with the same polarity on a signal and its return line. Therefore, the electromagnetic field generated the common mode current on the pair of lines does not cancel at far distance. When GND noise (voltage drop on the GND connection) is present, then this generally translates into common mode noise on components attached to GND.

Possibilities to reduce common mode noise:

→ *[next slide]*

Exercises

(cont'd)

Possibilities to reduce common mode noise:

- reduce the impedance on the GND path, e.g. by using a continuous GND plane that acts as a good return path for the signals
- avoid false (parasitic) return paths : if they exist, then the sum of the currents on the "true" signal and return path is no longer zero, meaning that there is a common mode component on the these paths.
- shield against external noise sources (electromagnetic fields)
- avoid asymmetries (parasitic loading) on differential lines

Generally, differential signaling is more immune to common mode noise.

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