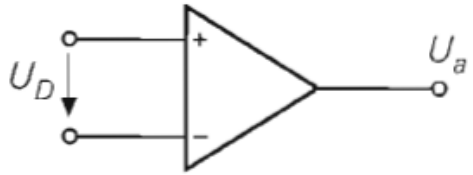
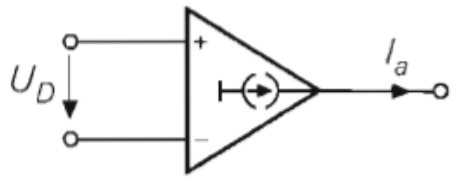
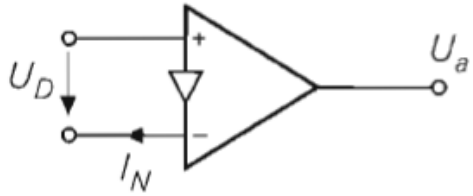
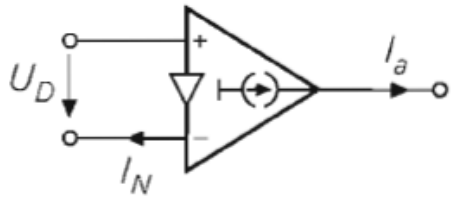
Contents

Categories of ideal operational amplifiers

	Voltage output	Current output
Voltage input	Normal opamp VV-opamp  $U_a = A_D U_D$	Transconductance opamp VC-opamp  $I_a = S_D U_D$
Current input	Transimpedance opamp CV-opamp  $U_a = I_N Z = A_D U_D$	Current opamp CC-opamp  $I_a = k_I I_N = S_D U_D$

Voltage controlled voltage source

Voltage controlled current source

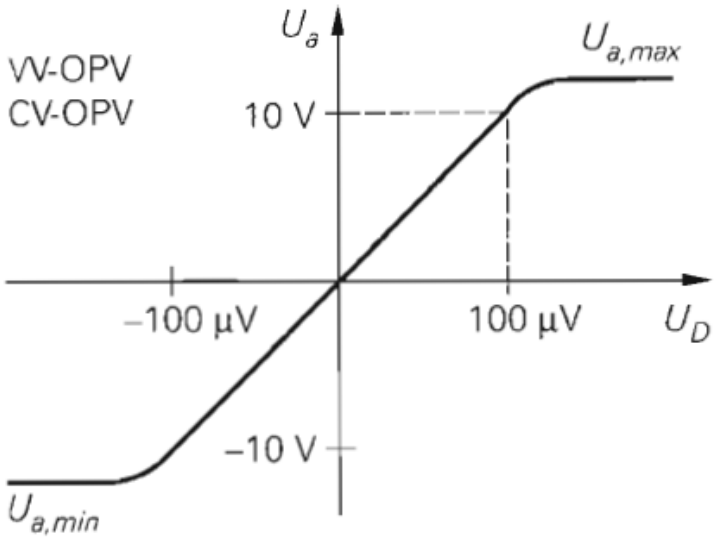
Current controlled voltage source

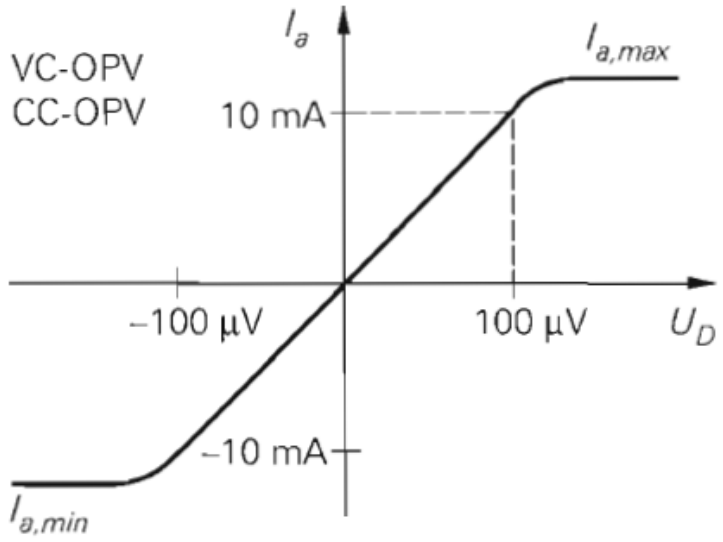
Current controlled current source

Transfer characteristics of operational amplifiers

The gain is

- very high (ideally infinite), and
- limited at or close to the supply voltages (reduced by an output resistance).





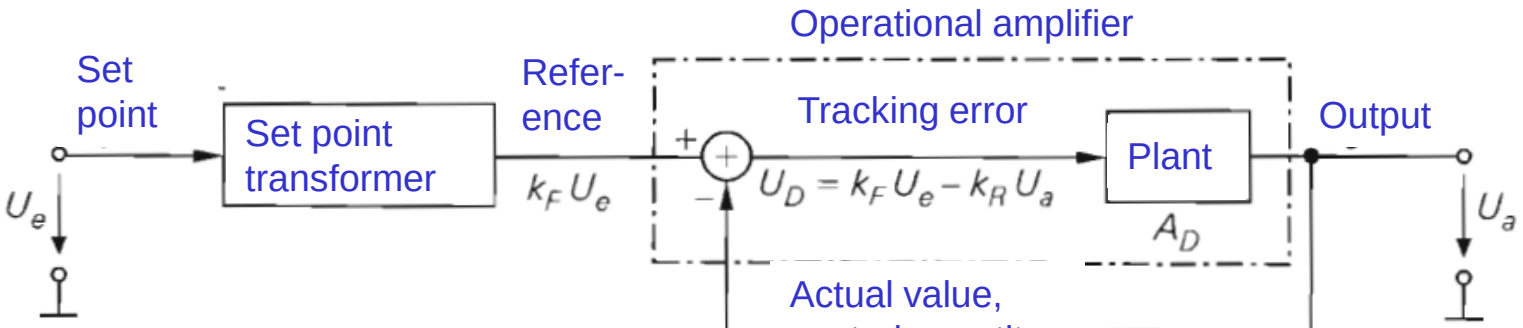
With the high gain

- difference between input potentials is close to zero, and
- virtually (ideally) input potentials are identical.

Other hypotheses for simplified analysis of operational amplifier circuits :

- input resistances are very high (ideally infinite), and
- output resistance is very small (ideally zero).

Control loop block diagram



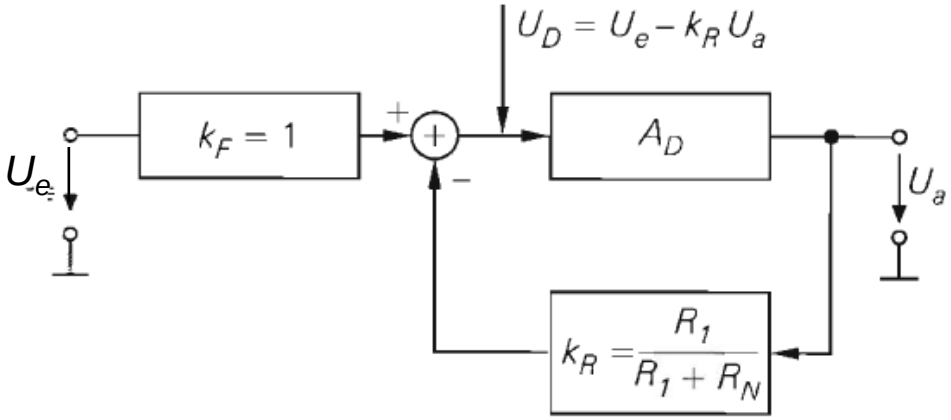
$$U_D = k_F U_e - k_R U_a$$

$$A = \frac{U_a}{U_e} = \frac{k_F A_D}{1 + k_R A_D} \cong \frac{k_F}{k_R}$$

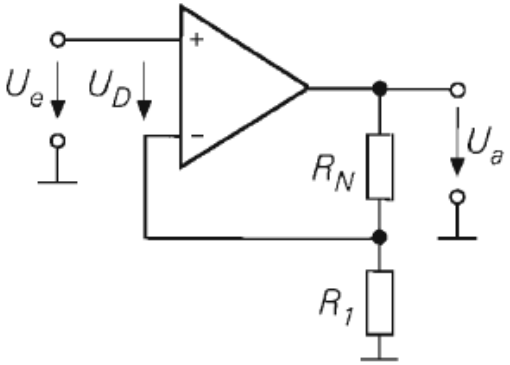
Linear operational amplifier based circuits may be regarded as feedback loops:

- Part of the output voltage is compared to the weighted input difference voltage.
- With infinite feedback loop gain $g = k_R A_D$, simple determination of output voltage in function of input difference voltage.
- If the gain is ‘very high’ its precise value is without noticeable influence on the output.

Control loop representation of non-inverting amplifier



Feedback loop model



Non-inverting ampilfier

$$U_a = A_D U_D = A_D (U_P - k_R U_a)$$

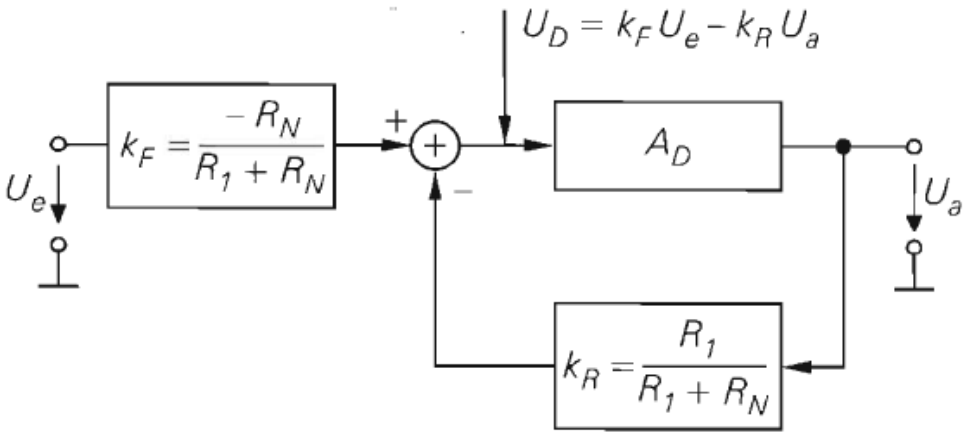
$$A = \frac{U_a}{U_e} = \frac{A_D}{1 + k_R A_D} \cong \frac{1}{k_R} = 1 + \frac{R_N}{R_1}$$

The simplification is valid if the loop gain $g = k_R A_D$ is very high.

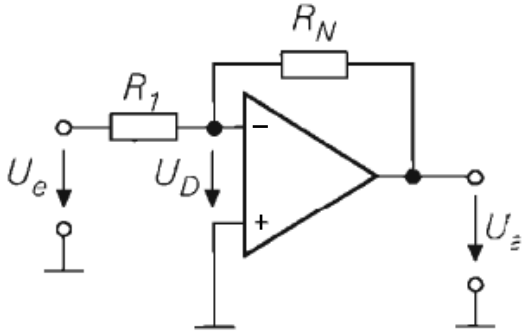
Distinguish four gain definitions:

- open loop gain A_D
- closed loop input → output gain A
- feedback loop gain g
- feedback factor k_R

Control loop representation of inverting amplifier



Feedback loop model



Inverting ampilfier

$$U_a = A_D U_D = A_D\left(k_F U_e - k_R U_a\right)$$

$$A = \frac{U_a}{U_e} = \frac{k_F A_D}{1 + k_R A_D} \cong \frac{k_F}{k_R} = -\frac{R_N}{R_1}$$

For an ideal amplifier, both inputs are at virtual ground, and the node law yields: $\frac{U_e}{R_1} + \frac{U_a}{R_N} = 0$

If A_D is not infinite: $0 = \frac{U_e + U_D}{R_1} + \frac{U_a + U_D}{R_N} \quad \Rightarrow \quad 0 = R_N\left(A_D U_e + U_a\right) + R_1 U_a\left(A_D + 1\right)$

$$A = \frac{U_a}{U_e} = -\frac{R_N A_D}{R_1 A_D + R_N + R_1} = k_F \frac{A_D}{1 + k_R A_D}$$

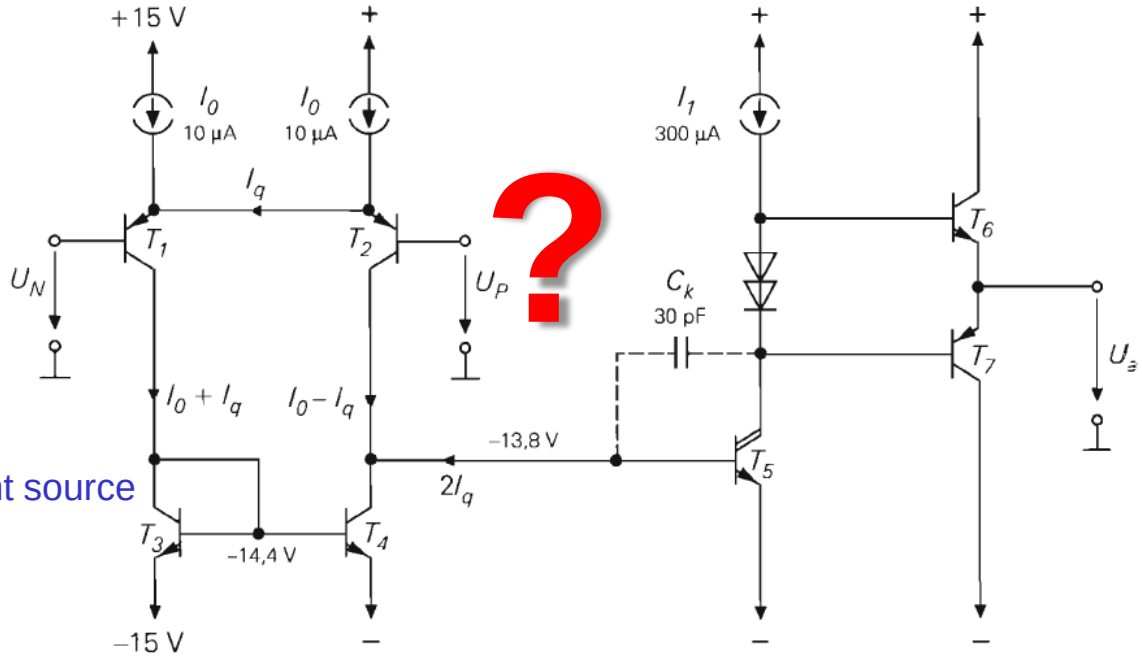
Exercice:
Control loop representation of differential amplifier

- Draw the schematic of a differential amplifier.
- Represent the differential amplifier by a control loop model, analogous to those for non inverting and inverting amplifiers.

What is inside an operational amplifier?

To understand operational amplifiers, also as a user, we need to have a basic understanding of internal cicuits:

1) the differential amplifier
2) the current mirror and current source
3) the active load
4) the cascode circuit
5) the impedance converter
6) the push-pull amplifier
7) the Darlington transistor



In the following slides, we briefly review these circuit building blocks.

They will help us to understand specialized architectures, e.g. for rail-to-rail in- and outputs, and for high speed amplifiers.

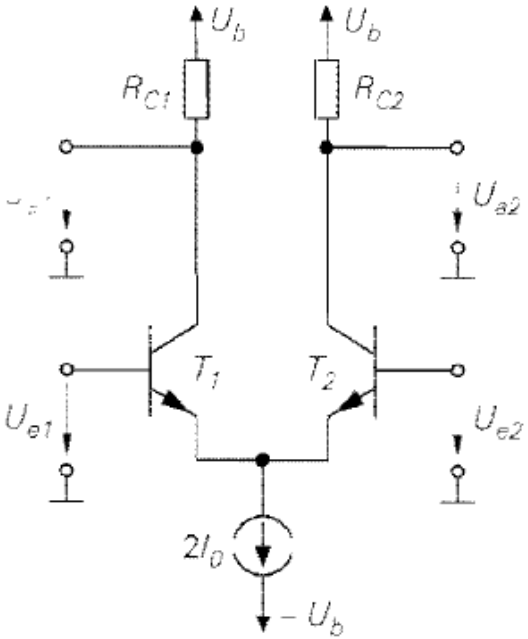
How do we realize a very high, quasi infinite DC gain?

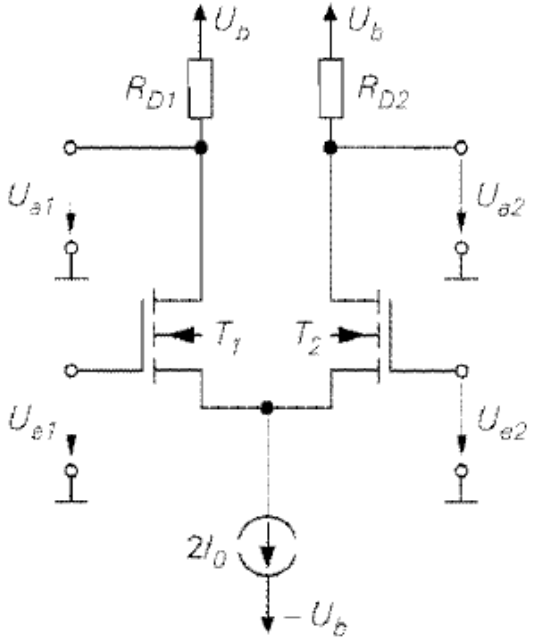
1) Differential amplifier

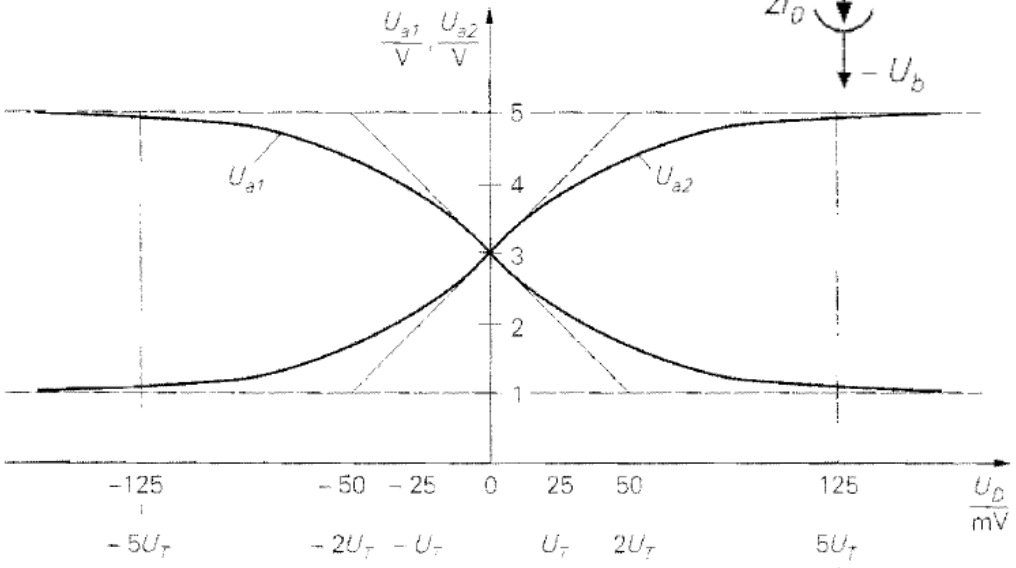
Large signal analysis:

$$I_{C1} = I_0 + \Delta I = I_0(1 + \tanh\frac{U_D}{2U_T})$$

$$I_{C2} = I_0 - \Delta I = I_0(1 - \tanh\frac{U_D}{2U_T})$$

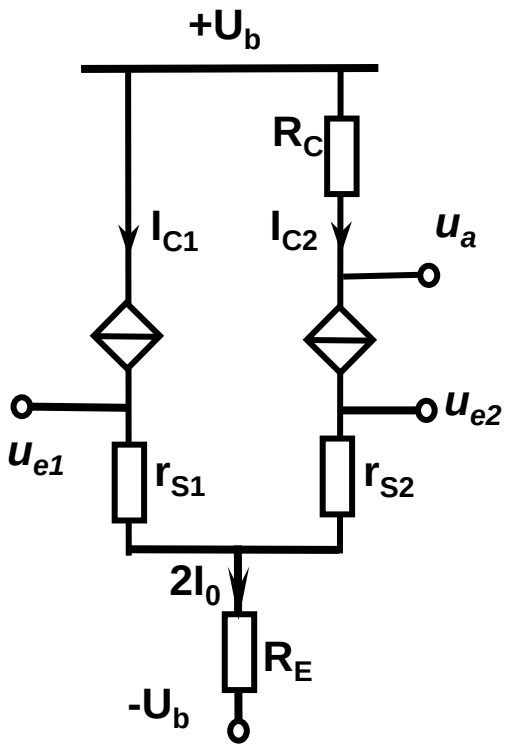






Differential amplifier

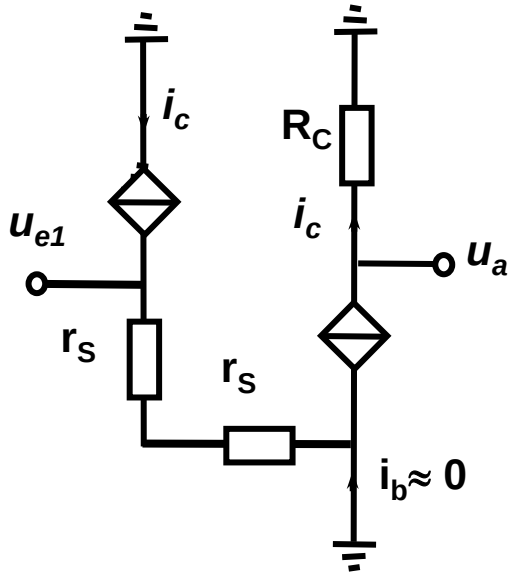
Small signal analysis:



Apply the principle of superposition →

Gain from input u_{e1}:
Suppose $R_E >> r_S$

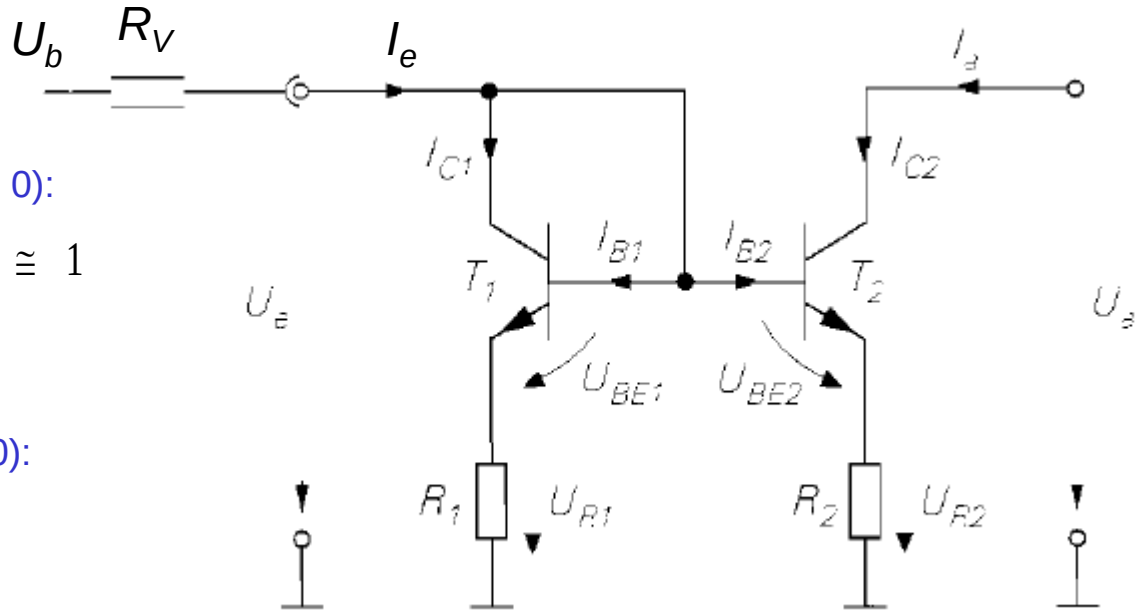
$$\frac{u_a}{u_{e1}} = \frac{R_C}{2r_S}$$



In the same way,
gain from input u_{e2}:

$$\frac{u_a}{u_{e2}} = -\frac{R_C}{2r_S}$$

2) Current mirror



T1 connected like a diode.
Current translation factor ($R_1 = R_2 = 0$):

$$k_I = \frac{1}{\left(1+\frac{1}{\beta}\right)\left(1+\frac{U_a}{U_A}\right)+\frac{1}{\beta}} \cong \frac{1}{1+\frac{2}{\beta}} \cong 1$$

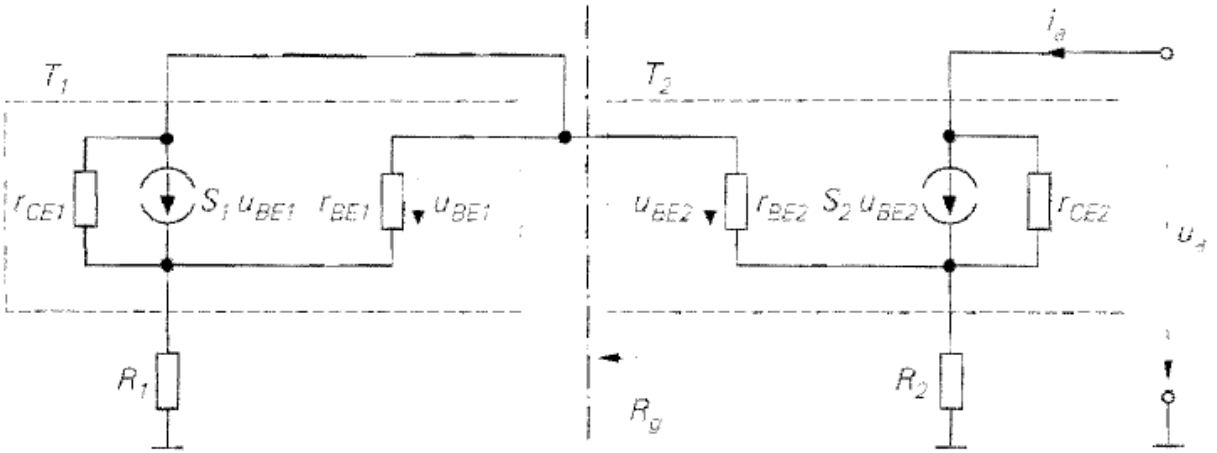
Current translation factor ($R_1, R_2 \neq 0$):

$$k_I = \frac{R_1}{R_2+\frac{R_1+R_2}{\beta}} \cong \frac{R_1}{R_2}$$

Operation as a current source:

$$I_e = \frac{U_b - U_{BE1}}{R_V + R_1}$$

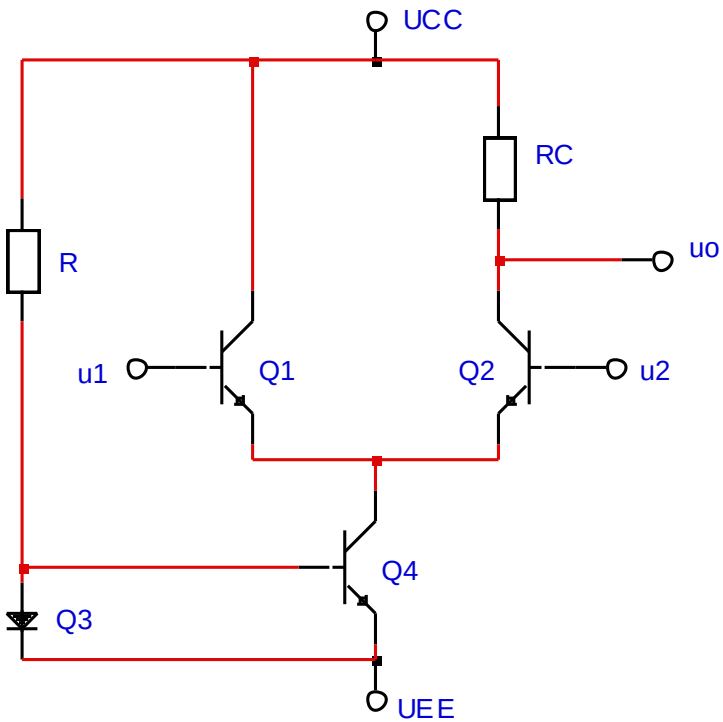
Equivalent schematic
for small signals:

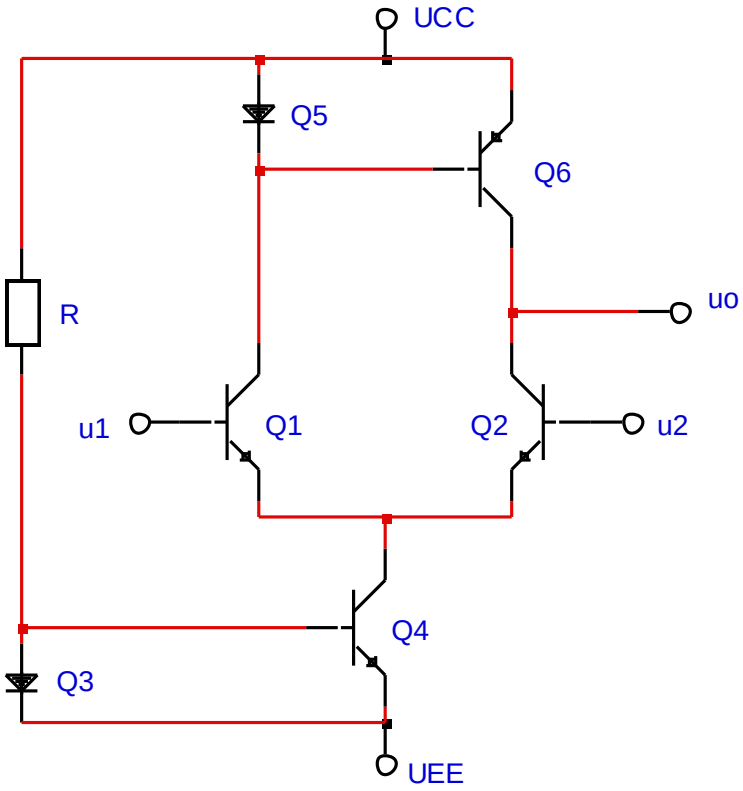


Output resistance:

$$r_a = \left.\frac{u_a}{i_a}\right|_{i_e=0} \cong r_{CE2}\left(1+\frac{\beta R_2}{R_1+R_2+r_{BE2}}\right)$$

3) Mirror used as current source and active load





Q3 is a transistor identical to Q4, where collector and base are connected. The same holds for Q5 and Q6.
The mirror Q3, Q4 sets the poarization current I = (UCC+UEE-UBE)/R.
The mirror Q5, Q6 creates an active load with a small signal collector resistance of Q2 = REarly6.
The differential gain becomes very high without increasing VCC. Also the output resistance is very high.

4) Cascode circuit

Emitter coupled (T_1) and base coupled (T_2) circuits in series.
Polarization of T_2 by U_0:

$$U_0 > U_{CE\,1,sat} + U_{BE\,2} \cong 0.8...1V$$

The total gain is the product of emitter and base circuit open output gains, and of load adaptation between the two stages :

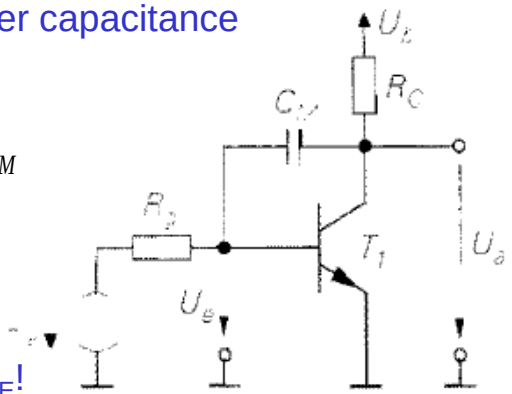
$$A = \frac{u_a}{u_e} = A_E \frac{r_{e,B}}{r_{a,E} + r_{e,B}} A_B = -\frac{r_{CE\,1}}{r_{S1}} \frac{r_{S2}}{r_{CE\,1} + r_{S2}} \frac{R_C}{r_{S2}} \cong -\frac{R_C}{r_{S1}}$$

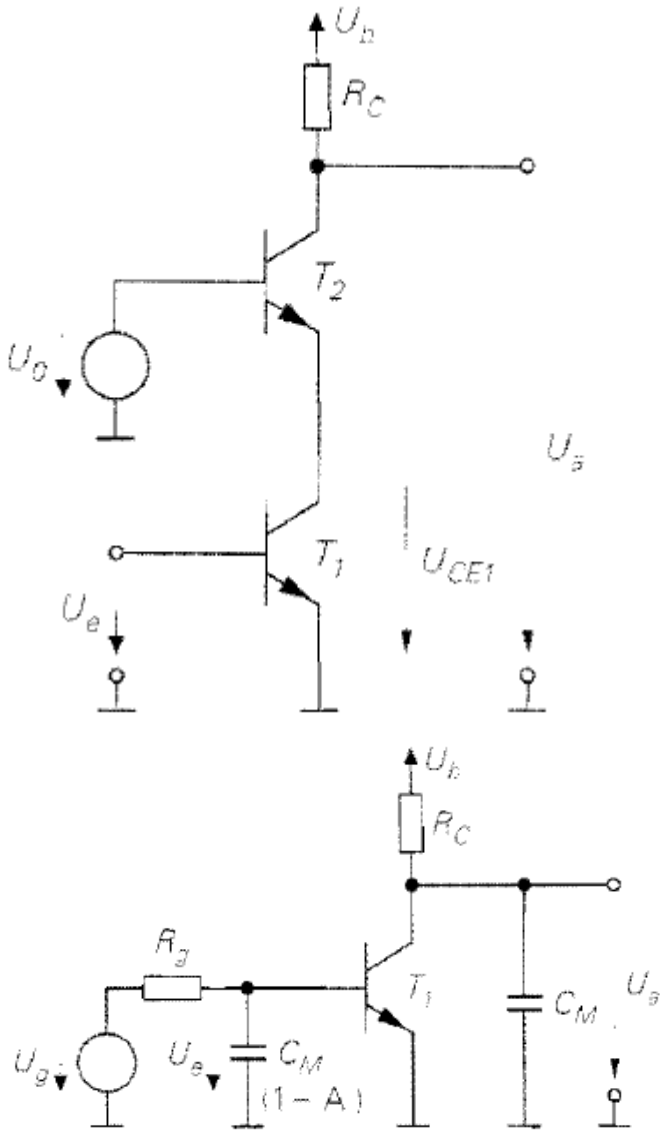
This is the same gain as of the emitter stage alone.
But the emitter stage in the cascode has a gain of -1 only.
Therefore, the equivalent Miller capacitance at its input is only

$$C_e = C_M \left(1 + \left|A_{E,op}\right|\right) \cong 2\,C_M$$

which is much smaller than with the emitter circuit alone.

Also, output resistance ≈ β·r_{CE}!

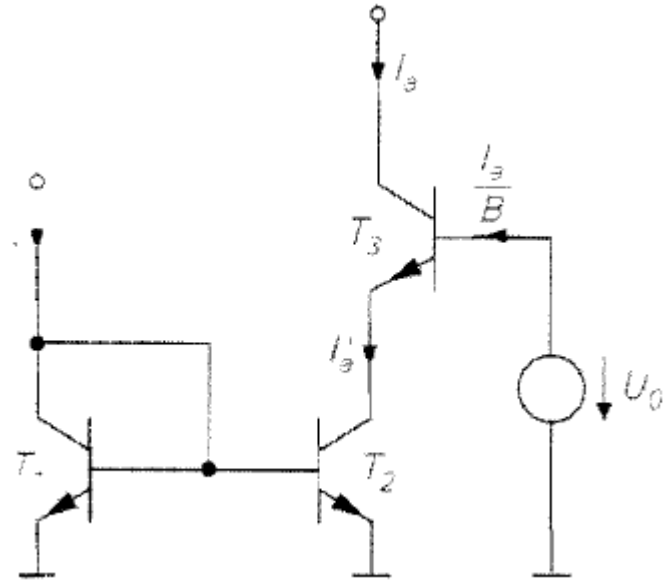


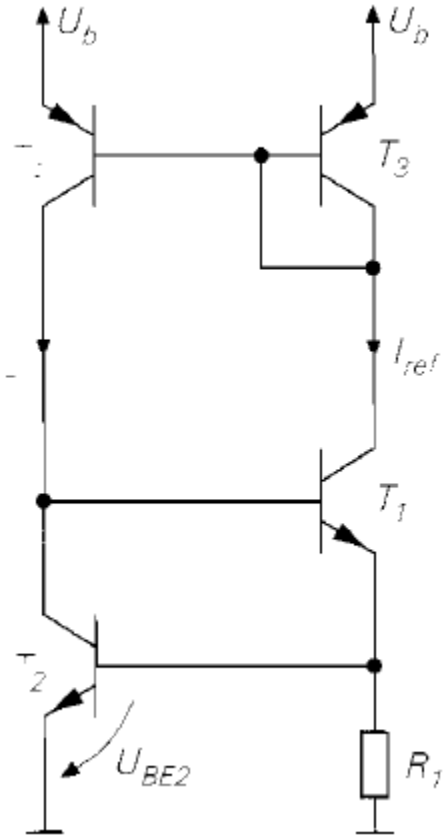


Modified current mirrors

Current mirror with cascode: increased output resistance

$$r_a = \left.\frac{u_a}{i_a}\right|_{i_e=0} \cong \beta\, r_{CE\ 3}$$



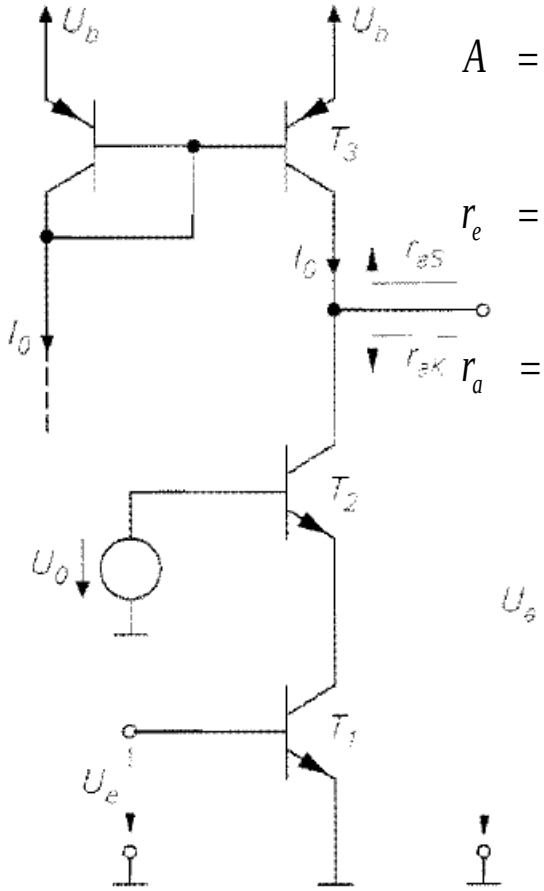


Mirror used as current reference independent of supply voltage:

$$I_{ref} \cong \frac{U_T}{R_1}\ln\left(\frac{I_{ref}}{I_{S2}}+1\right) \cong \frac{U_{BE\ 2}}{R_1}$$

Cascode circuit with current source

Cascode with simple current source with high gain and output resistance:



$$A = \left.\frac{u_a}{u_e}\right|_{i_a=0} = -\frac{r_{aK} \| r_{aS}}{r_{S1}} \cong -\frac{r_{CE\,3}}{r_{S1}}$$

$$r_e = \frac{u_e}{i_e} = r_{BE\,1}$$

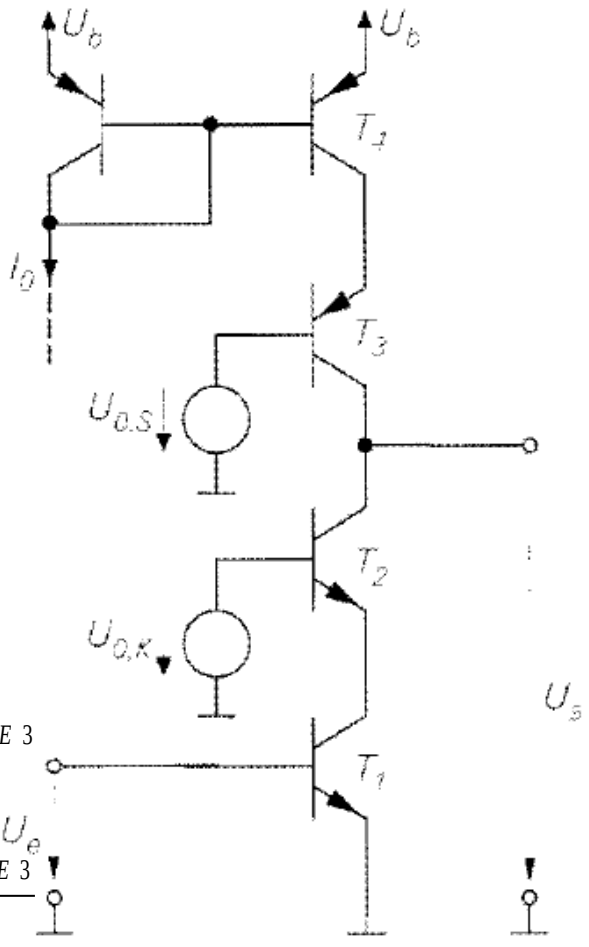
$$r_a = \left.\frac{u_a}{i_a}\right|_{u_e=0} = r_{aK} \| r_{aS} \cong r_{CE\,3}$$

with even more output resistance and gain:

$$r_a = \left.\frac{u_a}{i_a}\right|_{u_e=0} = r_{aK} \| r_{aS} \cong \beta_2\, r_{CE\,2} \| \beta_3\, r_{CE\,3}$$

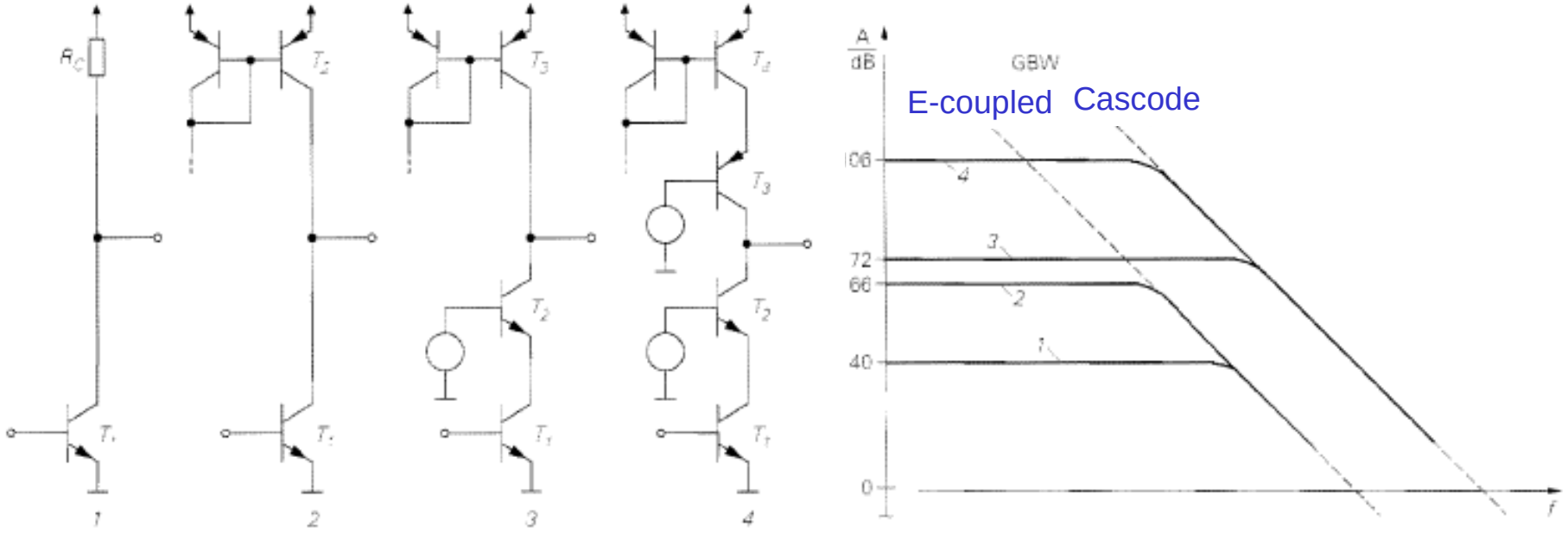
$$A = \left.\frac{u_a}{u_e}\right|_{i_a=0} = -\frac{r_a}{r_{S1}} \cong -\frac{\beta_2\, r_{CE\,2} \| \beta_3\, r_{CE\,3}}{r_{S1}}$$

Cascode with cascode current source



Gain response comparison

The comparison shows the improvements obtained with active load and cascode circuits, of static gain and bandwidth.



Exercice (homework): Amplifier transfer functions

- For the 4 variants of the preceding slide, analytically estimate the passing band gain and cut-off frequency.

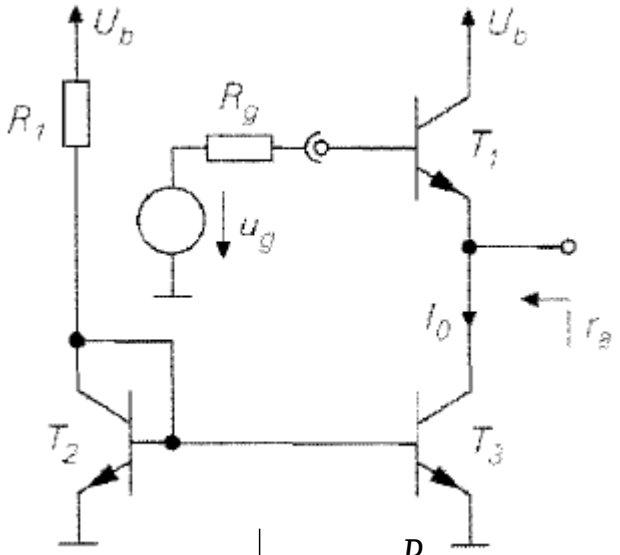
- Use the following parameters (all transistors identical):

  $r'_E = 25\Omega$, $r_{CE} = 100k\Omega$, $\beta = 100$, $R_C = 2.5k\Omega$, $C_M = 30pF$

- Simulate the 4 circuits using LTspice, and verify the gains and cut-off frequencies computed.

5) Impedance conversion

One collector coupled stage:

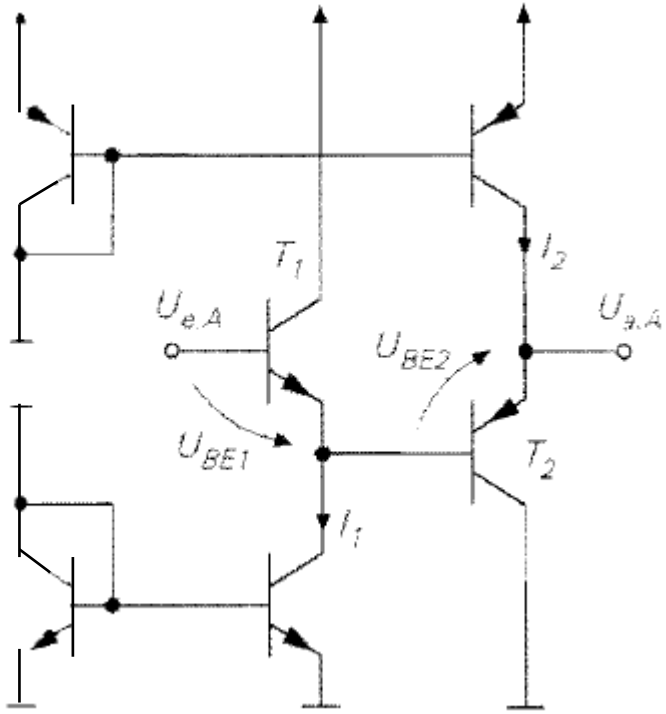


$$r_a = \left.\frac{u_a}{i_a}\right|_{u_e=0} = \frac{R_g}{\beta}$$

$$I_0 \cong \frac{10\,\beta\,U_T}{R_g}$$

Choose quiescent currents such that r_S does not influence r_a.
The second stage has about 10x higher I_0 than the first.

Two collector coupled stages:



$$r_a = \left.\frac{u_a}{i_a}\right|_{u_e=0} = \frac{R_g}{\beta^2}$$

6) Complementary impedance conversion

One collector coupled stage:

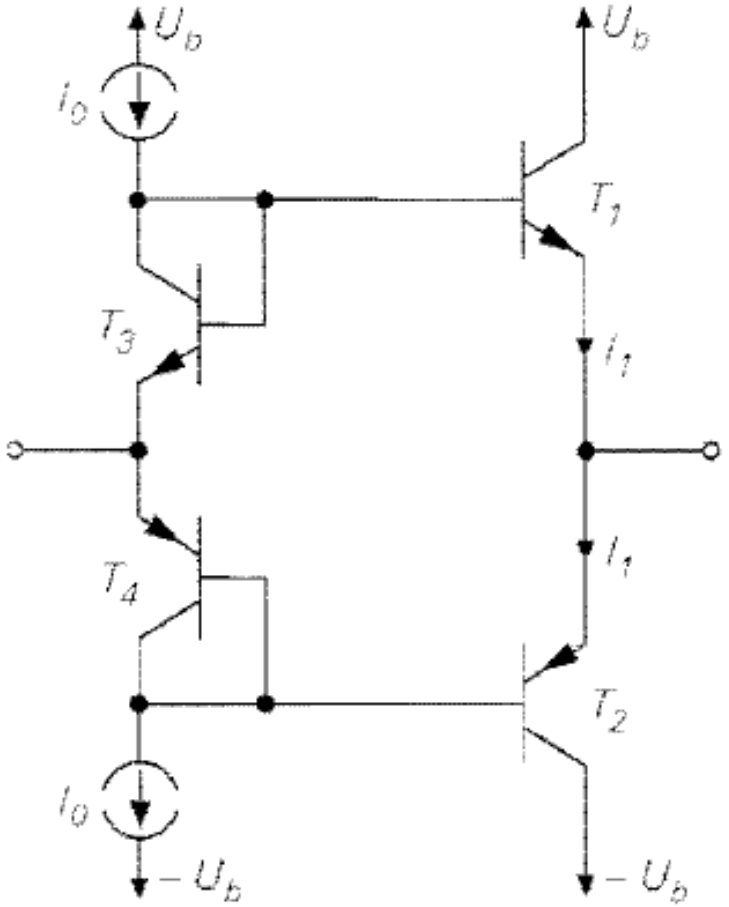
T_1, T_3 and T_2, T_4 operate as current mirrors.

This circuit can be operated with one side in saturation.

Two-stage circuits are also possible.

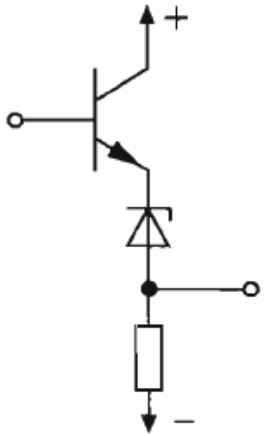
The circuit is called a push-pull amplifier:
Conduction during 180° of each of both transistors
for transmission of sine signals (B class operating mode)

Additional voltage gain can be added in front of the stage.

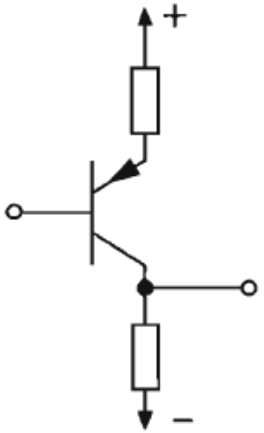


Methods for level-shifting

For DC voltage coupling of amplifier stages, level shifting is needed.



Z-diode
- not precise
- Fixed level difference only



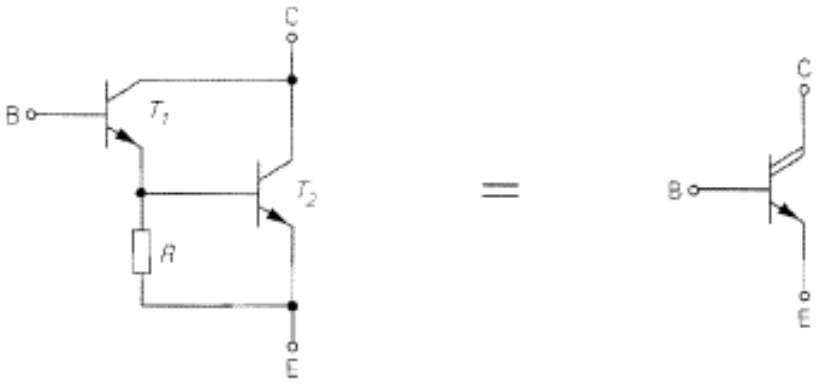
Complementary transistors
e.g. pnp transistor after npn amplifier stage
- adaptive: preferred method
- current mirror output stage may be used

7) Darlington transistor

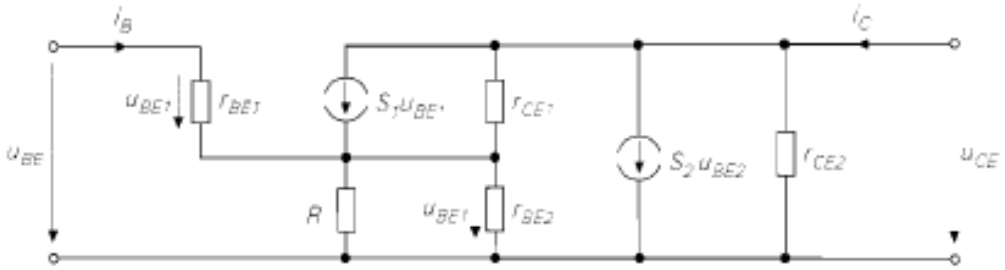
Resistor needed for improved switching behaviour.
Strong increase of current gain and input resistance, as compared to single transistor:

$$\beta \cong \beta_1 \beta_2$$

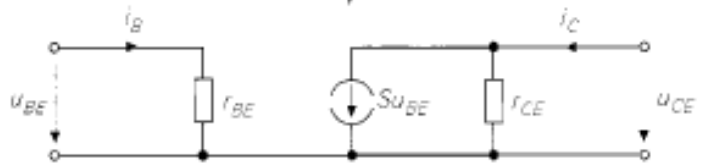
$$r_{BE} \cong r_{BE1} + \beta_1 \left(r_{BE2} \| R \right)$$



Small signal equivalent circuits, detailed:



reduced:

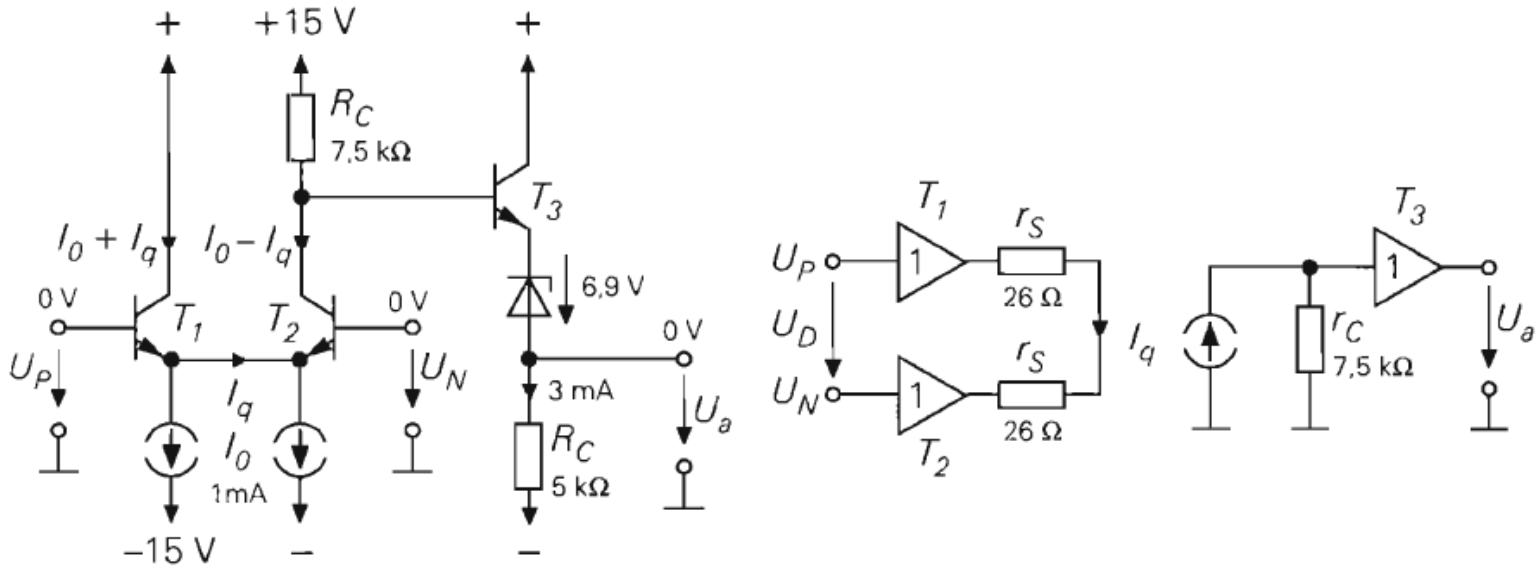


Exercice (homework): MOS-FET circuits

Redraw a cascode amplifier and a complementary impedance conversion stage schematic, each with MOS-FET instead of bipolar transistors.

Rewrite the gain and input capacitance equations for the cascode circuit with MOS-FETs.

Simple operational amplifier circuit



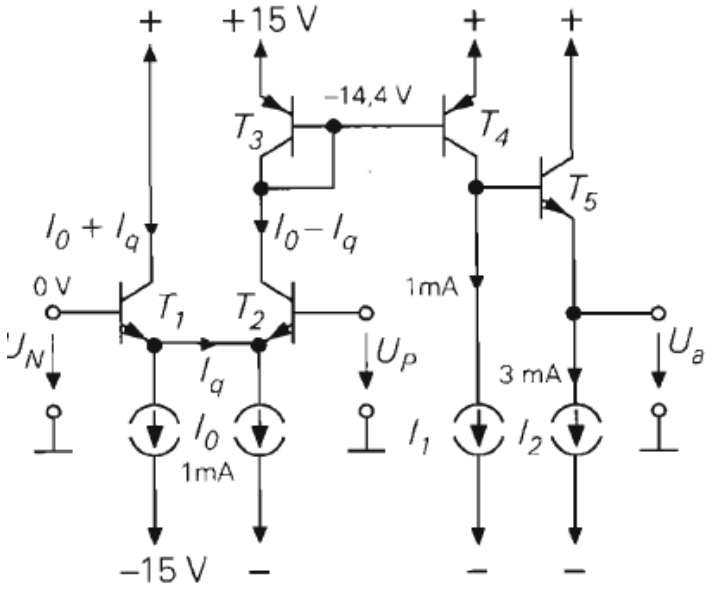
Example design values, quiescent currents and voltages, deviation I_q :

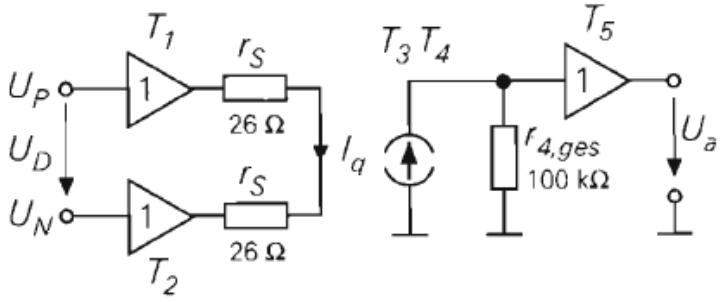
$$I_q = \frac{U_D}{2r_S} = \frac{1}{2}\frac{I_C}{U_T}U_D = \frac{1}{2}\frac{1mA}{26mV}U_D = \frac{19mA}{V}U_D$$

$$U_a = I_q R_C = \frac{1}{2}\frac{I_C R_C}{U_T}U_D = \frac{U_{RC}}{2U_T}U_D = \frac{7.5V}{2\cdot 26mV}U_D = 144\cdot U_D$$

Input common mode range -13.4V < $U_P = U_N = U_{gI}$ < +7.5V (minimum headroom of 1V over I_0 source).
Output range -7.5V < U_a < + 7.5V at $U_{GI} = 0$, otherwise less.

Use of current mirror for level-shifting





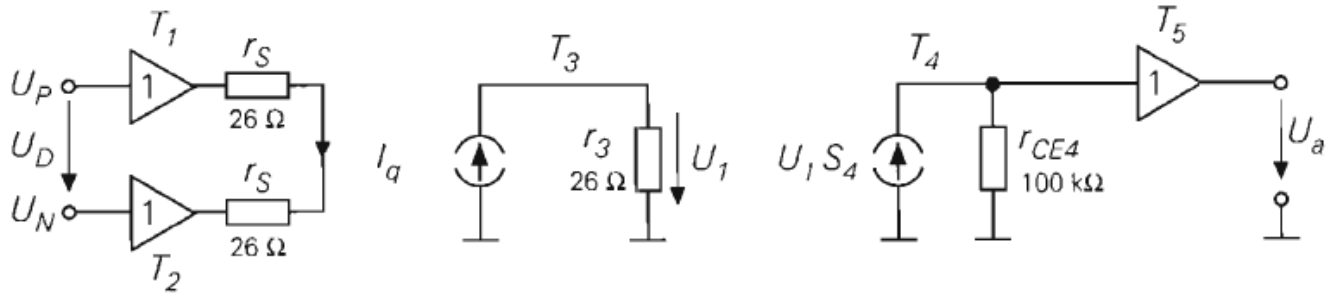
Input common mode range -13.4V < $U_P = U_N = U_{gl}$ < +14.4V (minimum headroom of 1V over I_0 source).

Output range -14V < U_a < + 13.8V.

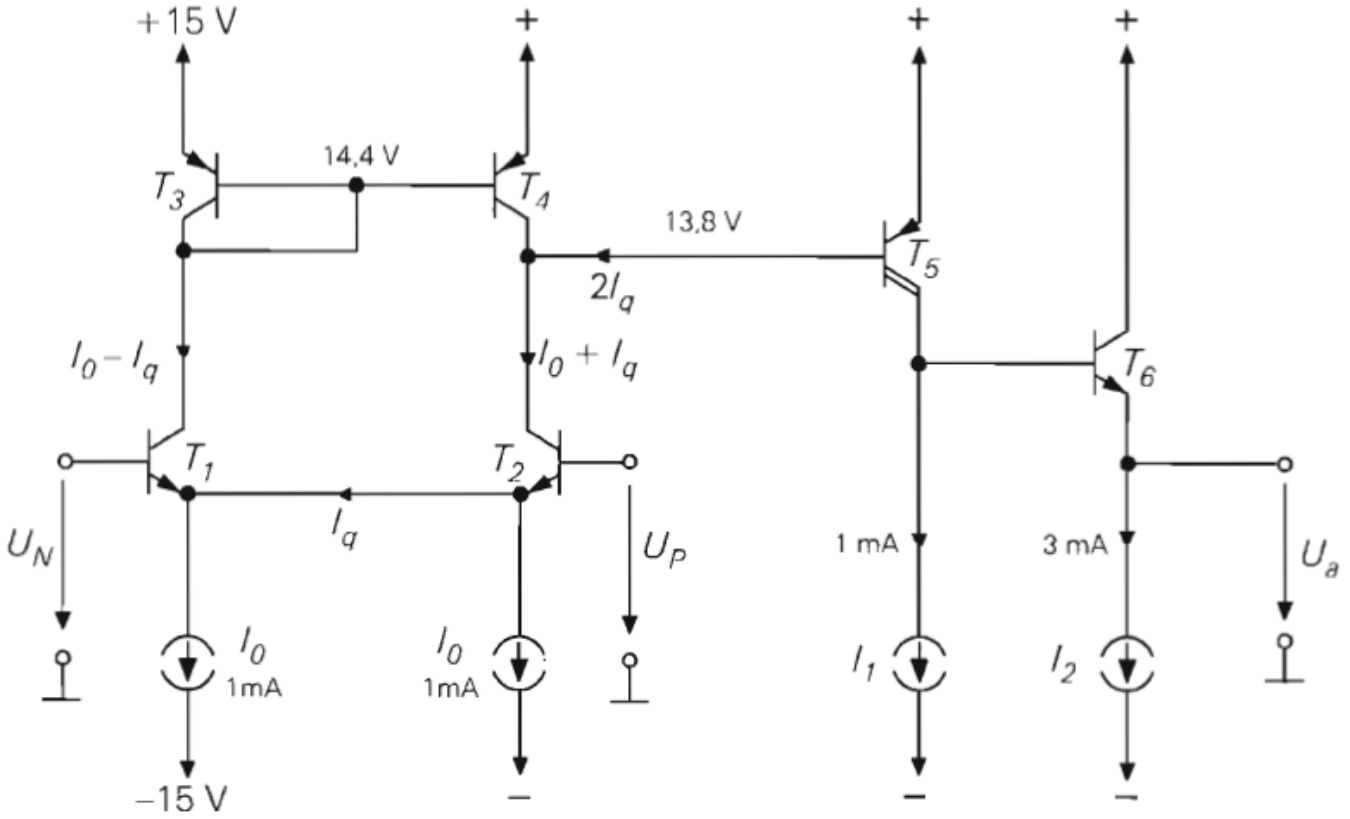
Difference gain:

$$A_D = \frac{r_{CE4}}{2r_S} = \frac{I_0}{2U_T}\frac{U_A}{I_0} = \frac{100V}{2 \cdot 26mV} = 1923$$

Model with 2 amplifying stages:



Operational amplifier with 2 amplifier stages



Example design values for quiescent currents and voltages, deviation Iq.
Advantage of this universal amplifier: two cascaded stages realize higher gain.
T_5 must be a Darlington transistor for high input resistance.

741 class operational amplifier

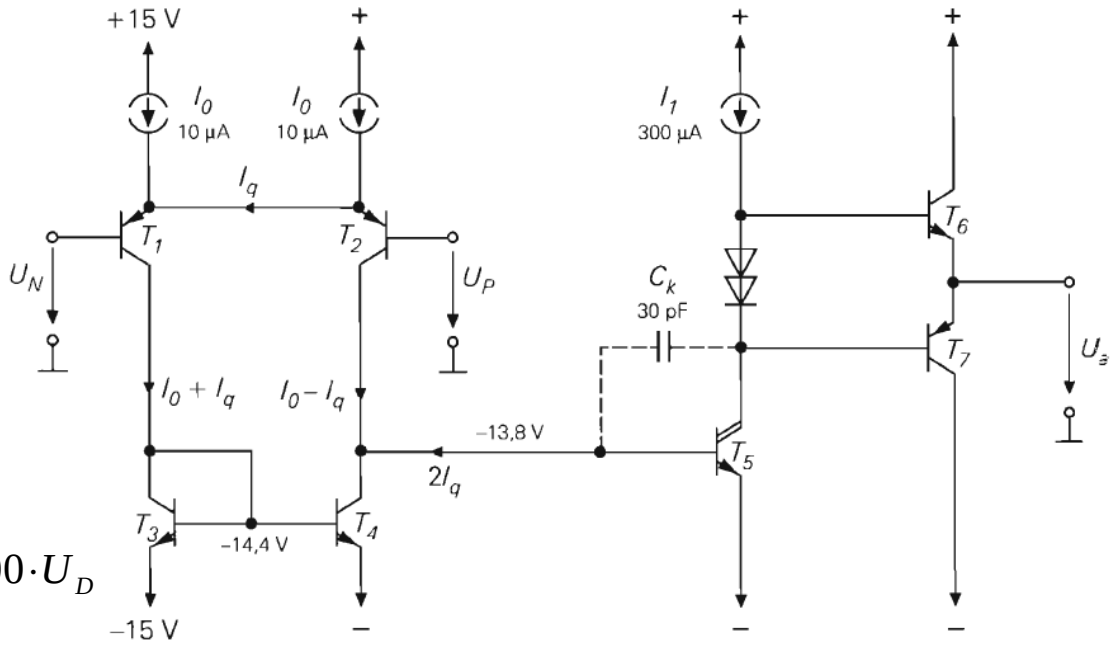
Complementary variant of circuit on preceding slide. Reduced quiescent currents in differential pair. Complemetary emitter follower at output, to reduce quiescent current.

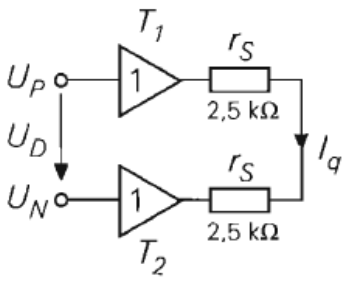
Model of the operational amplifier and gain equations:

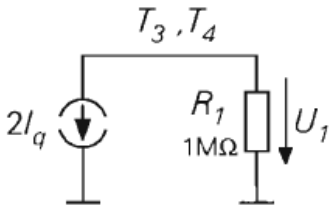
$$U_1 = -2I_q R_1 = -2R_1 \frac{U_D}{2r_S} = -\frac{1M\Omega}{2.5k\Omega} U_D = -400 \cdot U_D$$

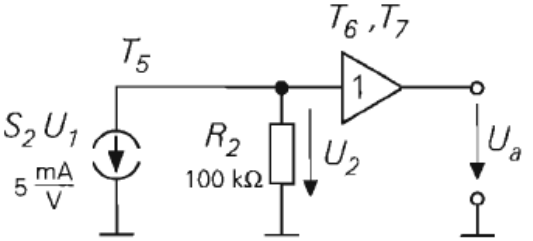
$$U_2 = -S_2 U_1 R_2 = -5\frac{mA}{V} \cdot 100k\Omega \cdot U_1 = -500 \cdot U_1$$

$$A_D = (-400)\cdot(-500) = 2 \cdot 10^5$$







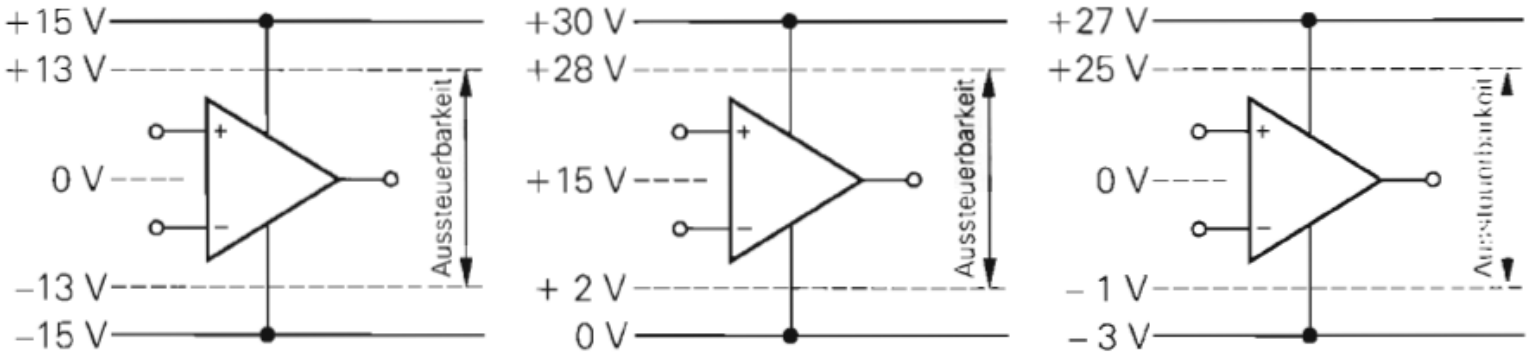


Exercice:
Determination of I/O voltage ranges

- Look at the schematic of the OP741 amplifier (p.26) and determine the highest possible positive and negative input voltages.
- Do the same for the output.
- What will happen if an input pin is driven beyond the power supply voltages?

Supply voltages

How do we reduce supply voltage and go for single supply operation?



a Normalbetrieb

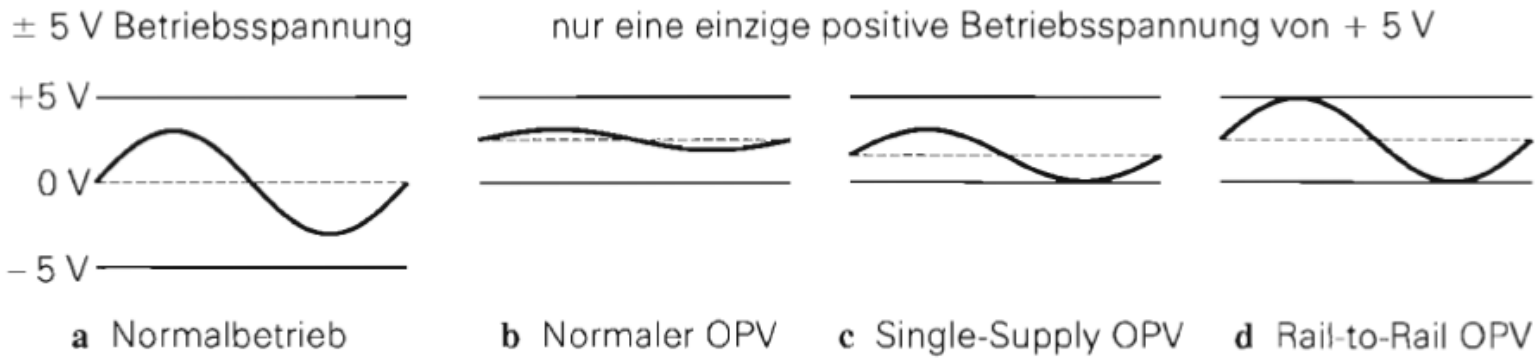
b Betrieb aus einer einzigen Betriebsspannung

c Betrieb für positive Spannungen

Influence on common and differential mode ranges

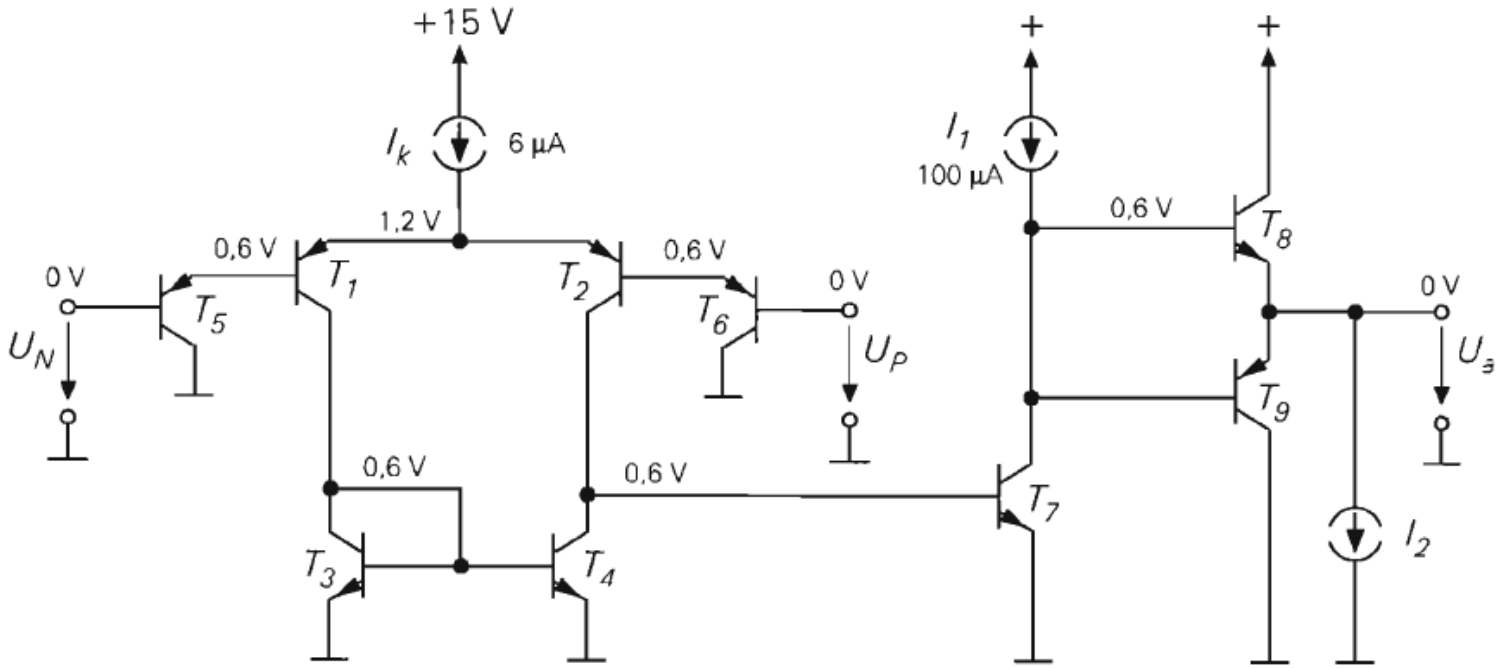
Output ranges with low supply voltages

Different solutions proposed in commercially available devices



Keep in mind that rail-to-rail operation might be possible either with inputs, or with the output, or with both.

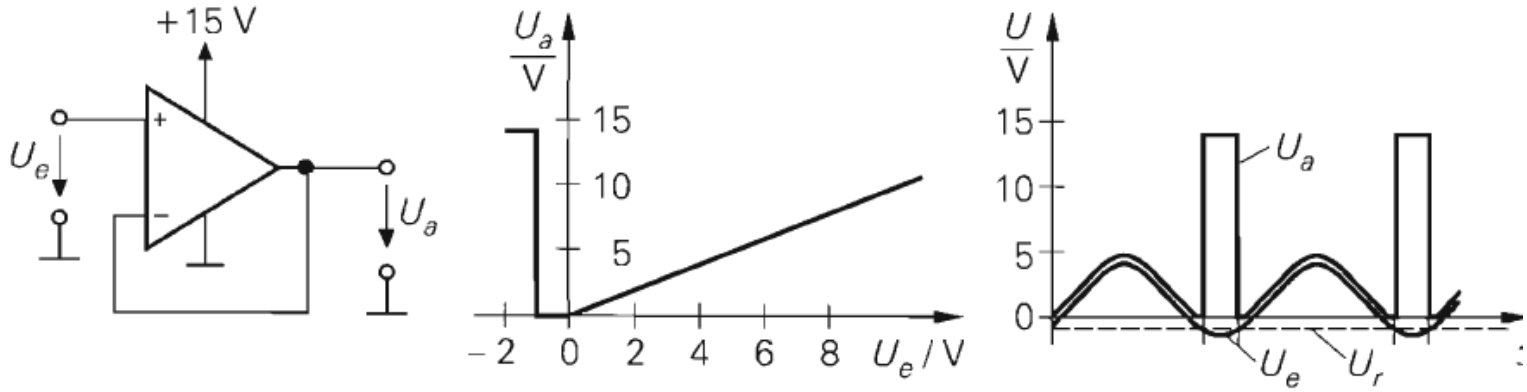
Single supply amplifier LM324



Potentials for 0V output = negative supply voltage
Additional emitter followers T_5, T_6 to shift the emitter potential of the difference amplifier 0.6V upwards, allowing 0V input.
T_7 is not a Darlington circuit, to limit the base potential to 0.6V, avoiding saturation of T_2 at 0V input.
Additional current source I_2 accepting current when T_9 already blocked.

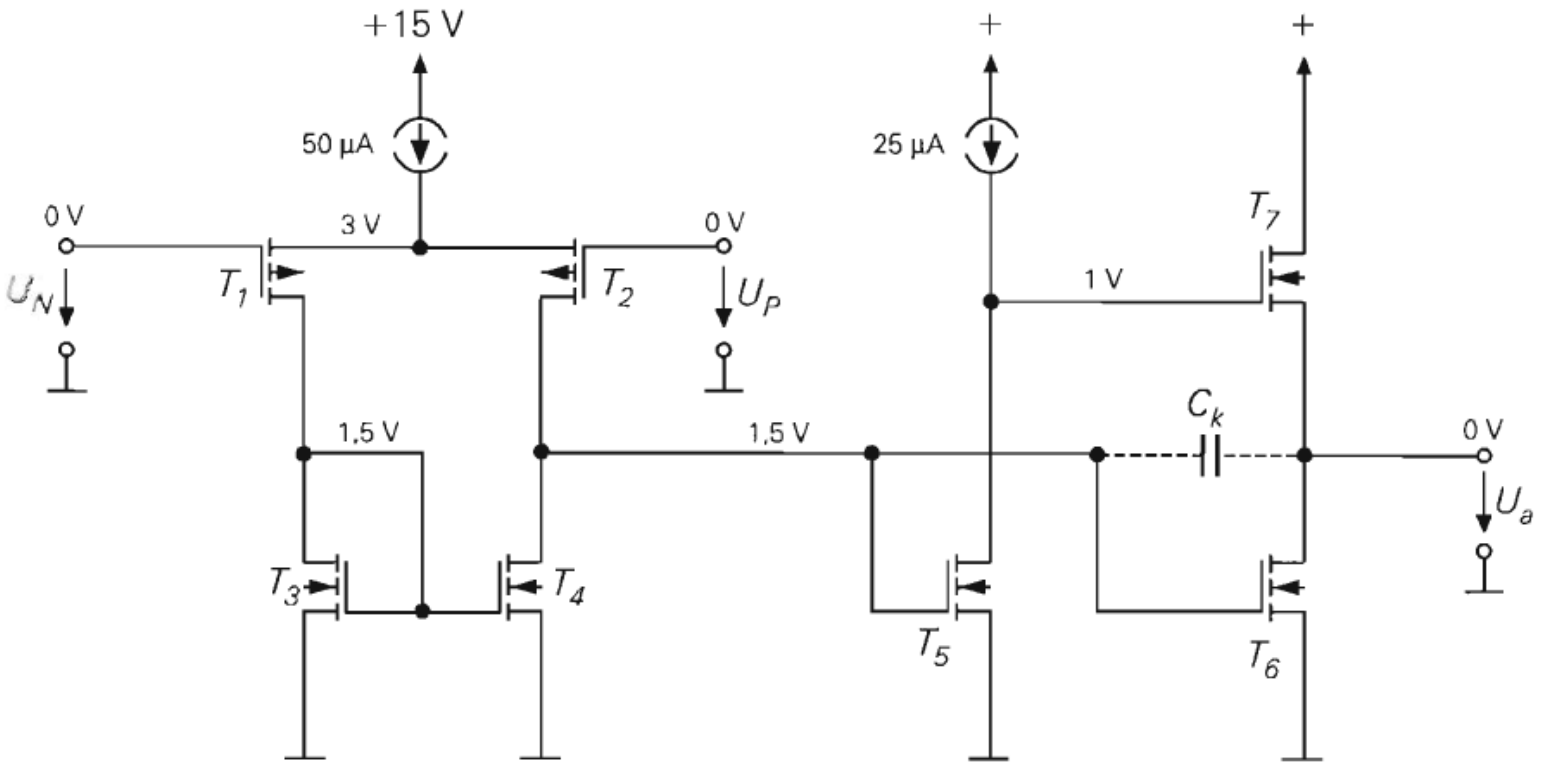
Phase reversal

T_2 saturates when input voltage below -0.4V. Its junction BC conducts, transistor in inverse mode. Emitter of T_6 then linked to T_7 and inverting amplification of T_2 becomes non-inverting: phase reversal.



Effect on transfer behaviour

Single supply CMOS operational amplifier



TLC series

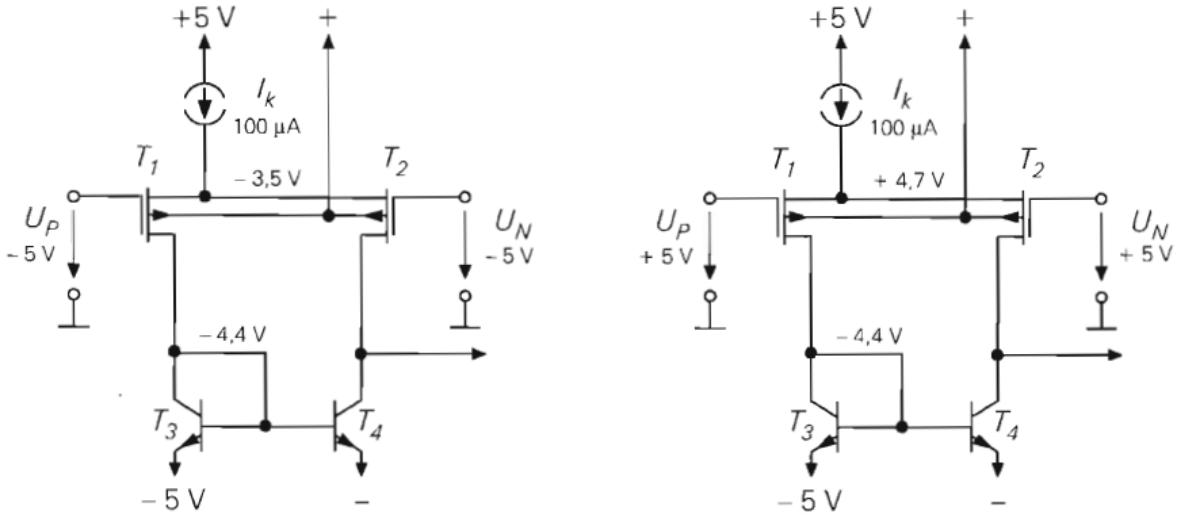
Not affected by phase reversal, since gate electrodes are insulated in CMOS and cannot conduct current.

T_6 is not a complementary source follower, but a common source circuit like T_5.

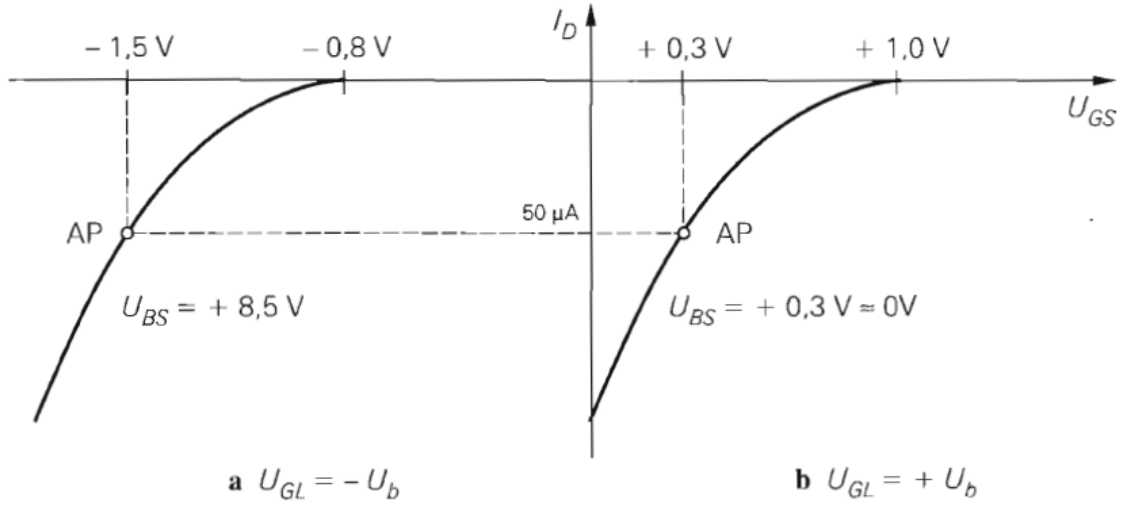
T_6 can pull down the output to zero, without additional current source I_2.

Rail-to-rail CMOS differential amplifier

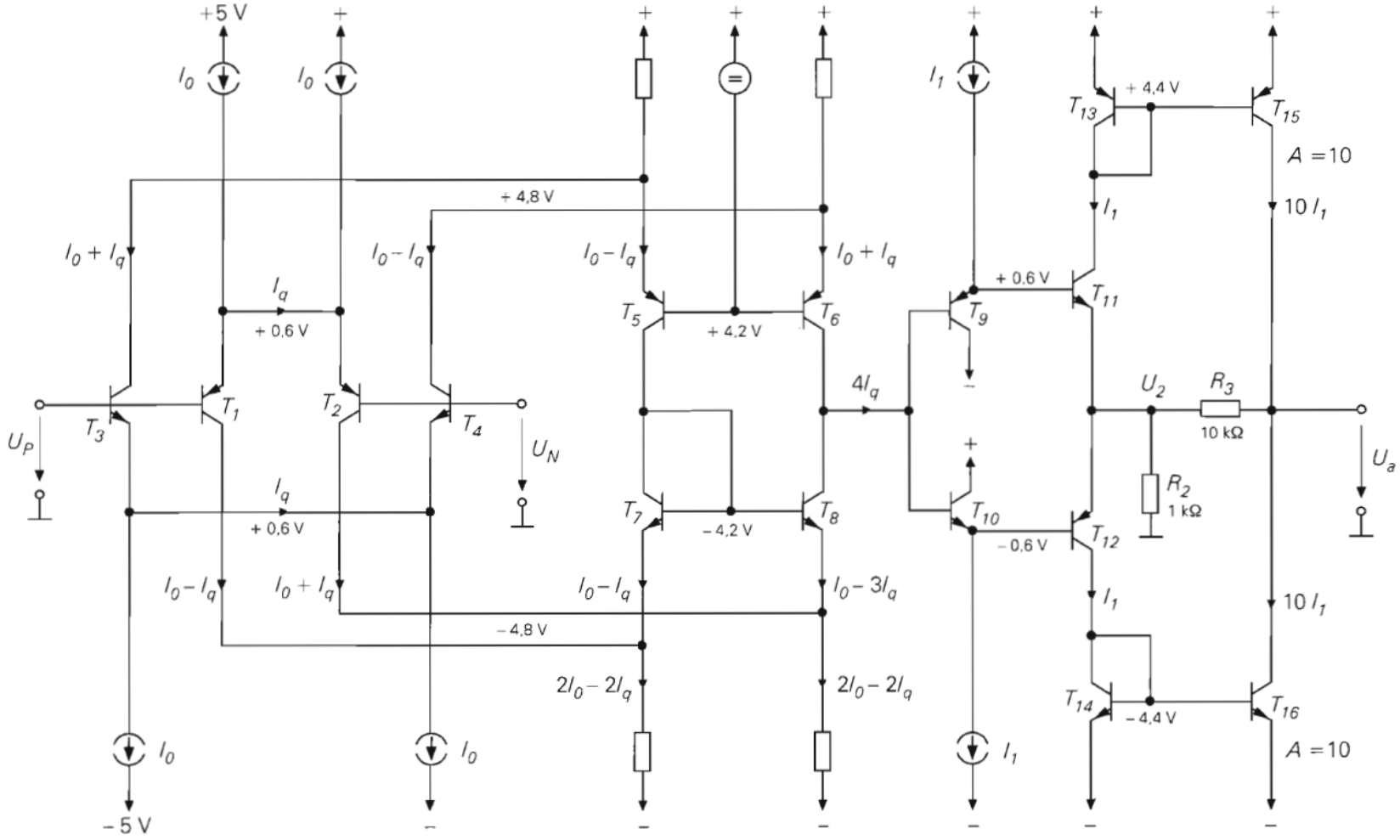
Special MOS-FETs that are self-blocking at negative input maximum, and self-conducting at positive input maximum.



Operating points for two extreme cases:



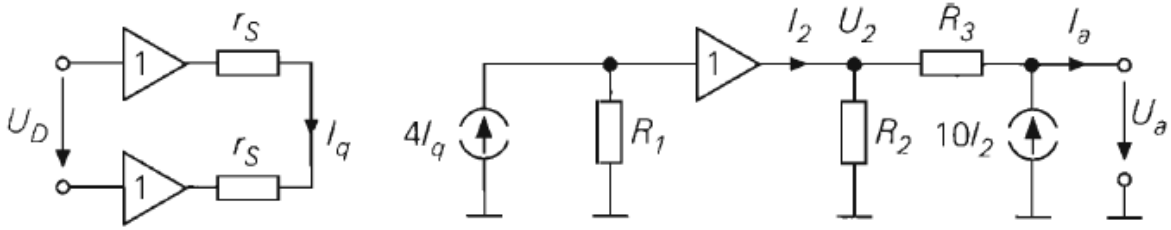
Rail-to-rail I/O operational amplifier



E.g. I_0 = 10μA, I_1 = 100μA

Model of rail-to-rail I/O operational amplifier

Model for output stage analysis:
R_1 is the impedance of the summation output delivering $4I_q$.



$$I_2 - \frac{U_2}{R_2} + \frac{U_a - U_2}{R_3} = 0$$

$$\frac{U_2 - U_a}{R_3} + 10I_2 - I_a = 0$$

$$I_a = 0 \Rightarrow \quad U_a = \frac{11R_2 + 10R_3}{11R_2} U_2 \cong 10U_2 \text{ , with } R_3 = 10R_2$$

$$U_2 = 0 \Rightarrow \quad r_a = -\frac{U_a}{I_a} = \frac{1}{11} R_3$$

Exercice:
Single supply circuits

- Propose the standard operational amplifier circuits (inverting, non-inverting, differential amplifier) for single supply operation.

Books

Tietze, Schenk: *Halbleiter-Schaltungstechnik*, Springer 2008 (13th ed.), ISBN 3-540-64192-0

This book was used as a basis for the present presentation, the illustrations are taken from it.

Millman: *Microelectronics: Digital and Analog Circuits and Systems*, McGraw-Hill 1984, ISBN 0-07-066410-2

Chatelain, Dessoulavy: *Electronique* , Traité d'électricité: vol VIII, PPUR 1982, ISBN 2-604-00010-5

Gray, Meyer: *Analysis and Design of Analog Integrated Circuits*, Wiley 1984 (2nd ed.), ISBN 0-471-81454-7

Jung: *OpAmp Application Handbook*, Analog Devices 2005, ISBN 0-750-67844-5

Mancini: *OpAmps for everyone*, Texas Instruments 2002