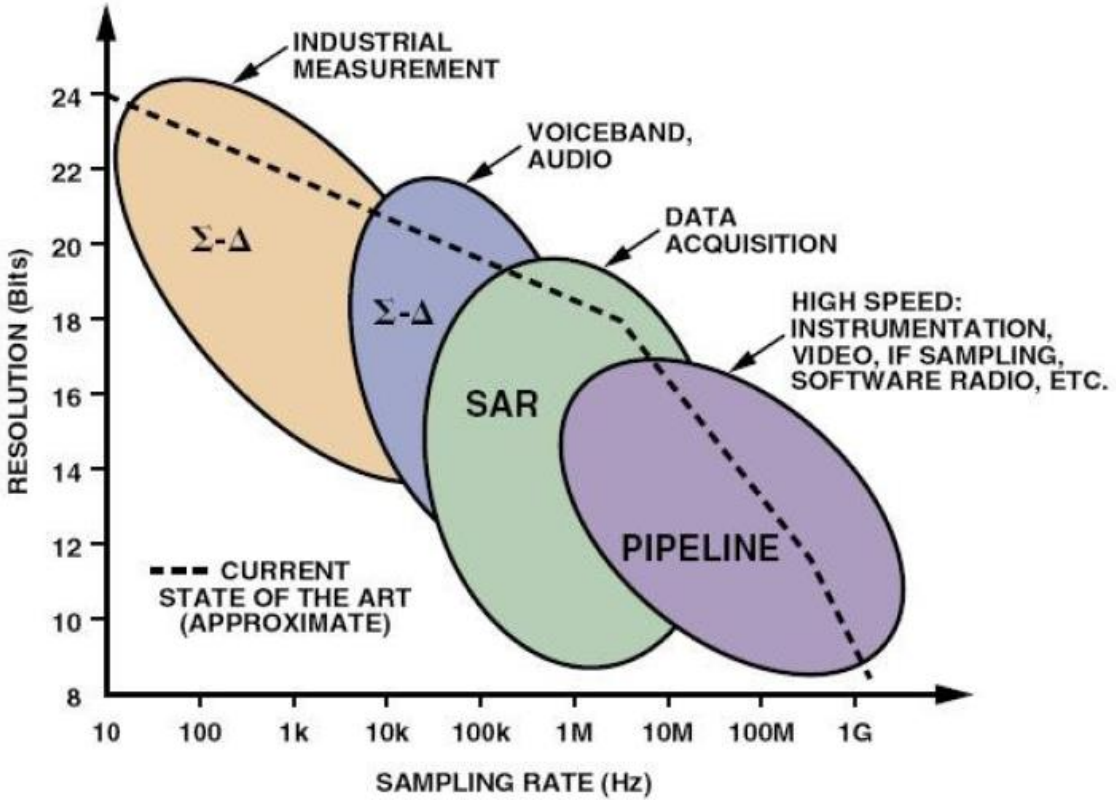
Contents

- A/D converter architectures
- Noise of A/D and D/A conversion
- Power supply
- Input filters and buffers
- Output filters and buffers

- References

ADC Structures

- Overview



Flash Converter

- Structure :
  2^N Resistors
  2^N Comparators
  - Primary coding is like a thermometer code
  - Need a 2^N-to-N encoder

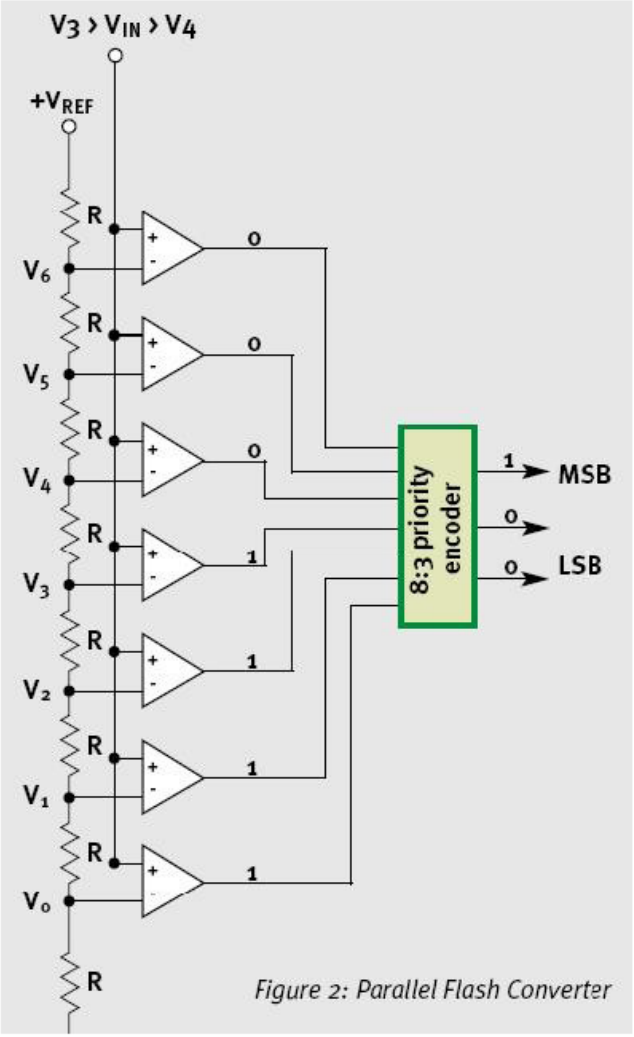


Figure 2: Parallel Flash Converter

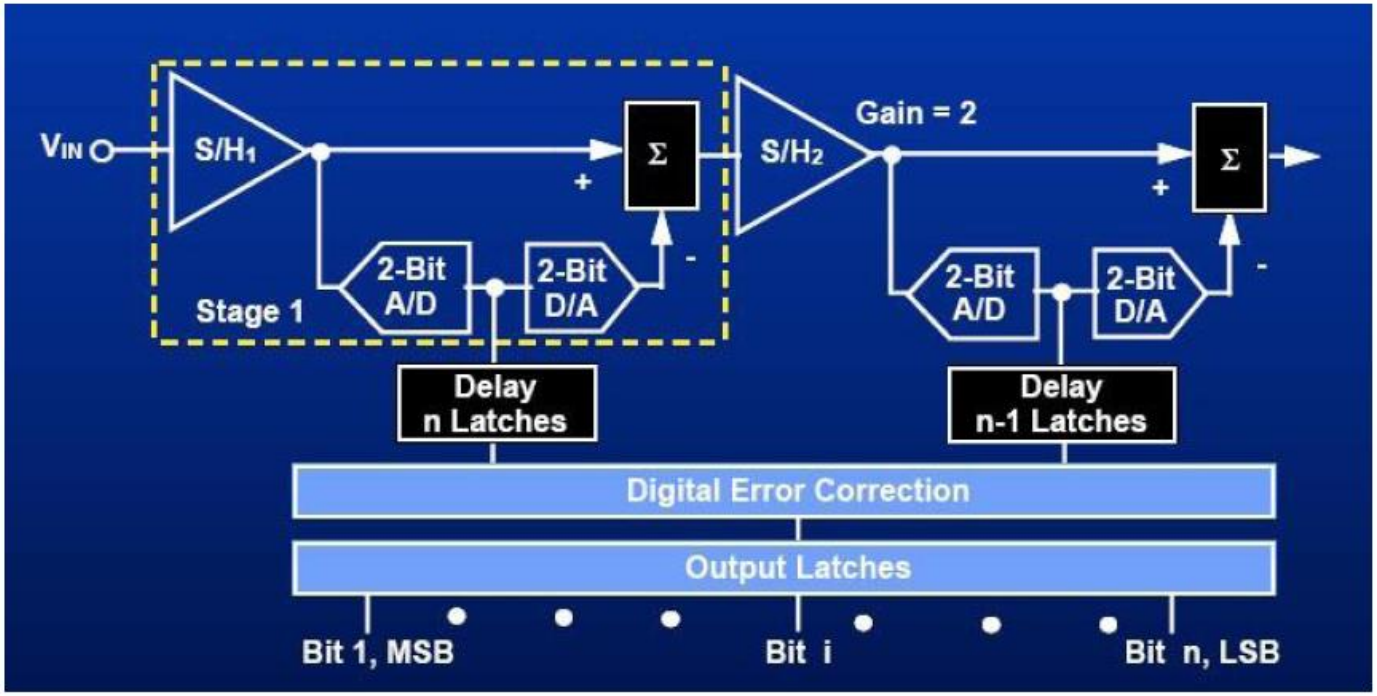
Flash Converter

- Resolution : 6-8 bits
- Speed : 100M - 1G sps (one cycle for latches)
- Throughput : idem
- Power : high!
- Applic Domain : very fast sampling (oscilloscopes, spectrum analyser, ...)

- Flash conv don't need à S/H amplifier

Pipeline Converter

- Structure



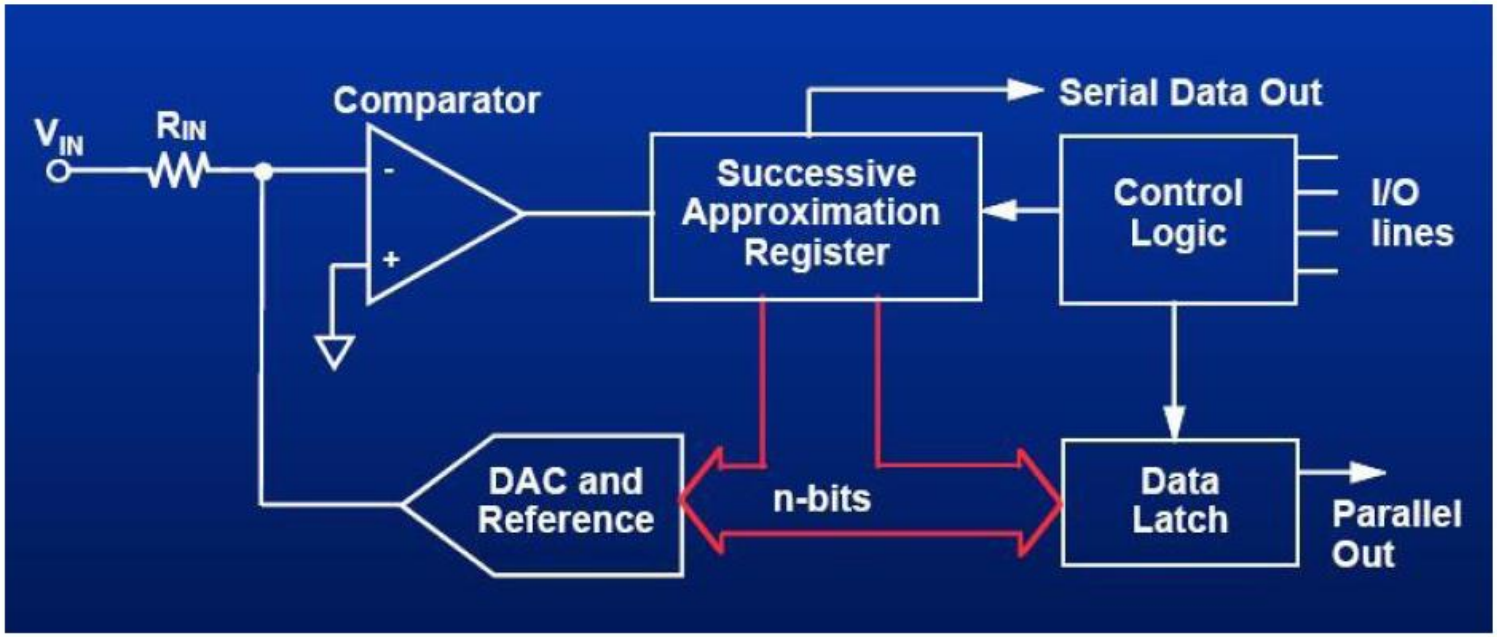
Pipeline Converter

- Resolution : 8-12 bits
- Speed (Latency) : 1M - 500M sps (3-4 stages X 1 clock cycle)
- Throughput : full speed = clock cycle
- Power : high
- Applic Domain : high speed applic, communications

- S/H at each stage

SAR Converter

- Structure



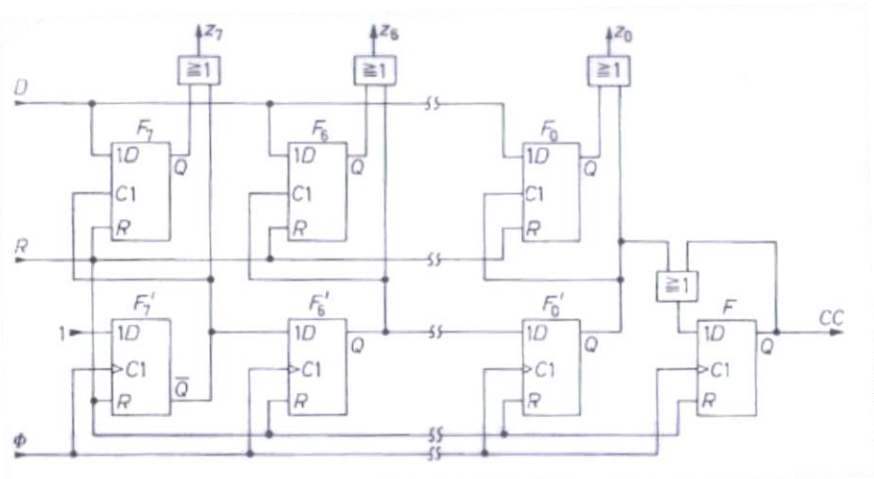
SAR Converter

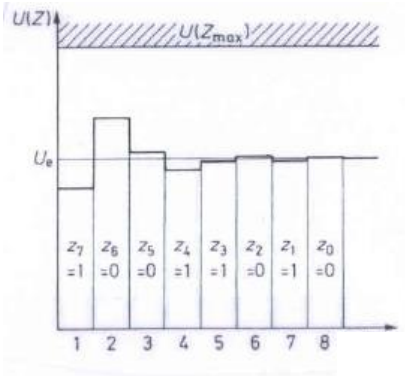
- Resolution : 8-16 bits
- Speed (Latency) : 100k - 10M sps (~N cycles latency)
- Throughput : 1 sample/~N clk cycles
- Power : medium
- Applic Domain : industrial domain, suits for multi-channel (i.e analog inputs for uC)

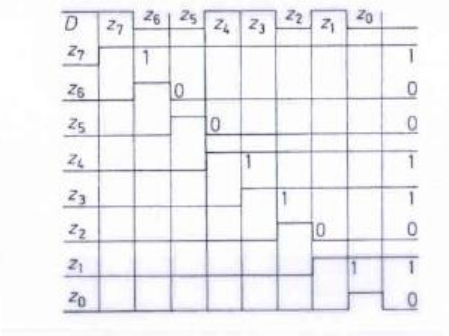
- Need a S/H

Successive approximation register

The logic circuit below is a successive approximation register processing the comparator output D and generating the conversion result Z. Describe its operation in time with the help of the conversion example presented below.



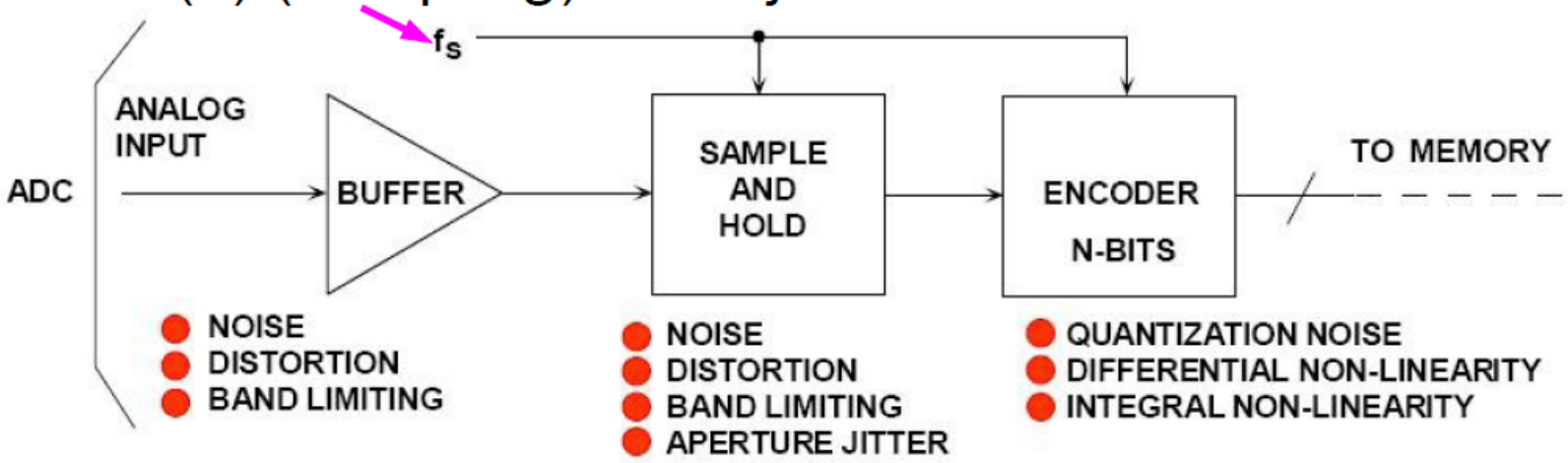




T	R	D	z_7	z_6	z_5	z_4	z_3	z_2	z_1	z_0	CC
0	1	D_7	1	0	0	0	0	0	0	0	0
1	0	D_7	D_7	1	0	0	0	0	0	0	0
2	0	D_6	D_7	D_6	1	0	0	0	0	0	0
3	0	D_5	D_7	D_6	D_5	1	0	0	0	0	0
4	0	D_4	D_7	D_6	D_5	D_4	1	0	0	0	0
5	0	D_3	D_7	D_6	D_5	D_4	D_3	1	0	0	0
6	0	D_2	D_7	D_6	D_5	D_4	D_3	D_2	1	0	0
7	0	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	1	0
8	0	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	1

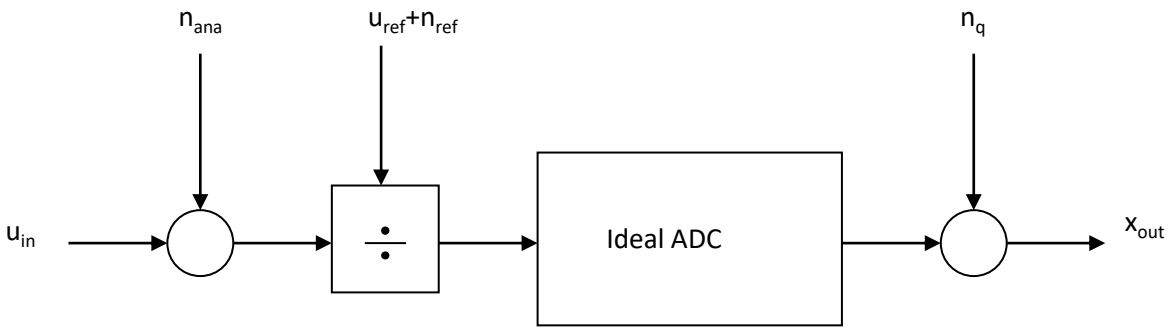
Noise sources (1)

- In an A/D converter, noise comes from many sources:
  - (1) quantization noise, (see last week)
  - (2) noise generated by the converter itself,
  - (3) application circuit noise (Reference & Power Supply, GND bounce, LAYOUT consideration)
  - (4) (sampling) clock jitter.



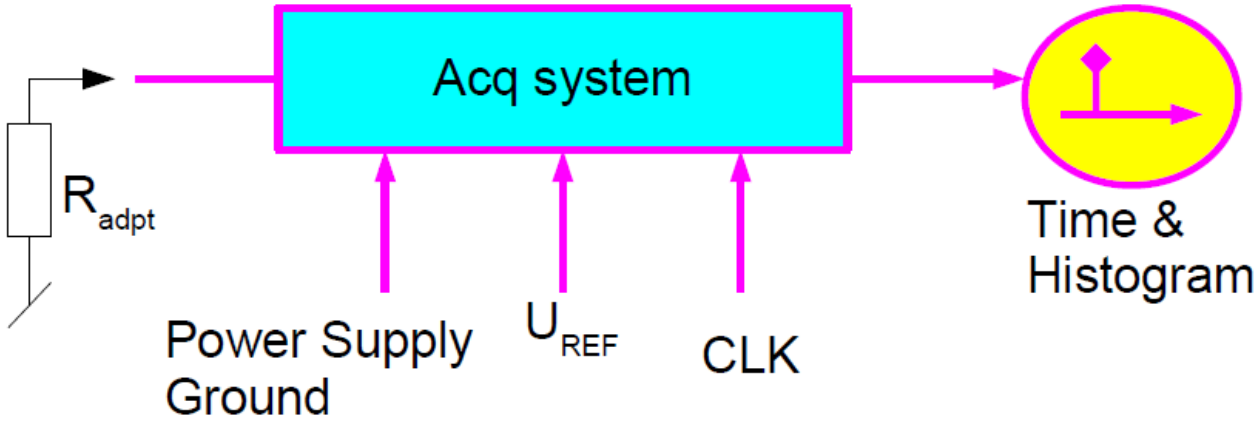
Noise sources (2)

- Analog input circuit noise is *additive.*
- Voltage reference noise is *multiplicative.*
- Quantisation noise is *additive.*



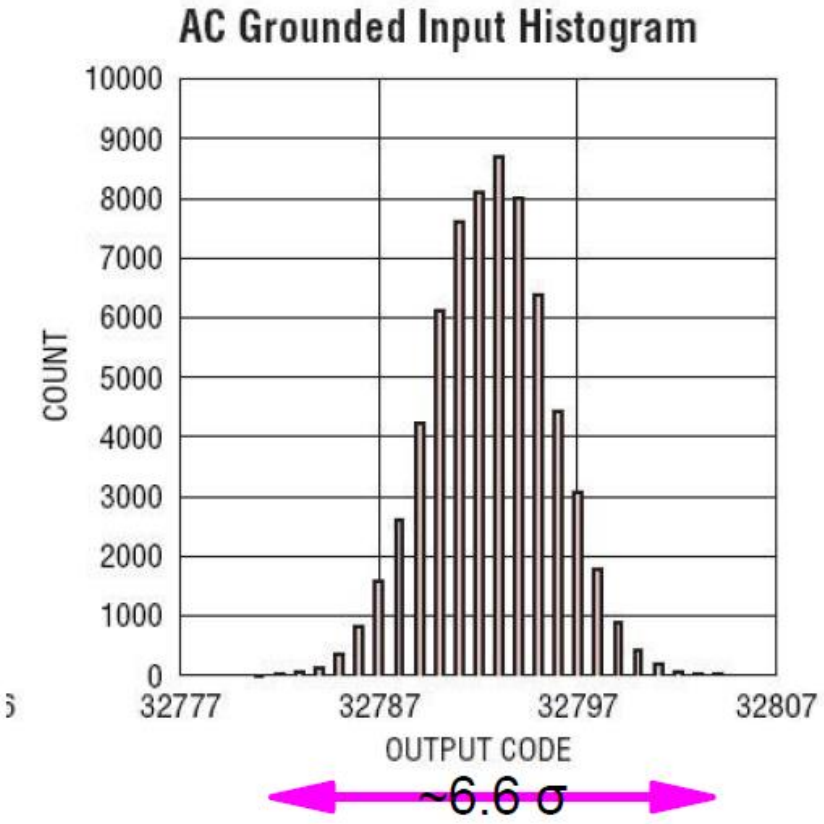
Noise sources (3)

- Noise sources have to be decorrelated: White noise can be assumed only in this case.
- Many noise are correlated => very difficult to predict the effective behviour !
- Make this test !



Zero Volt test

- AD2274:



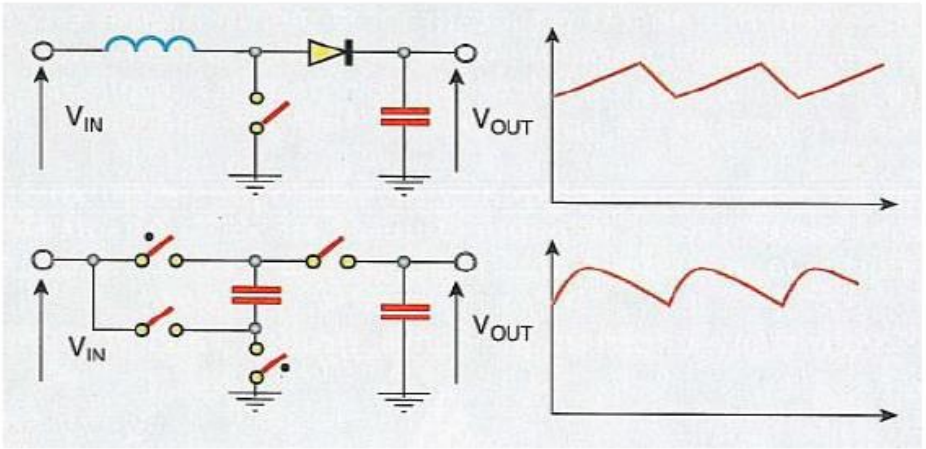
- Evaluate the RMS value of Noise. (σ ≈)

Voltage reference

- Stability of the REFERENCE is crucial for best performance of the Converter.
  - While these voltages appear static, they coud be dynamically used in the ADC system.
  - During every conversion the voltages on these pins are sampled and must settle within a fraction of the ADC clock rate, for example.
- Ref Voltage Sources are never good enough !
  - They introduces NOISE in the system
  - Quality of the DECOUPLING on the PCB

Power supply

- If ±15V power supply available, use them!
  - Design much easier (Low-noise amp, mature technologies, availability of the components...)
- But portable equipement have only one battery (e.g. 2.7V)
  - => DC/DC boost needed, but Analog circuits don't like it !



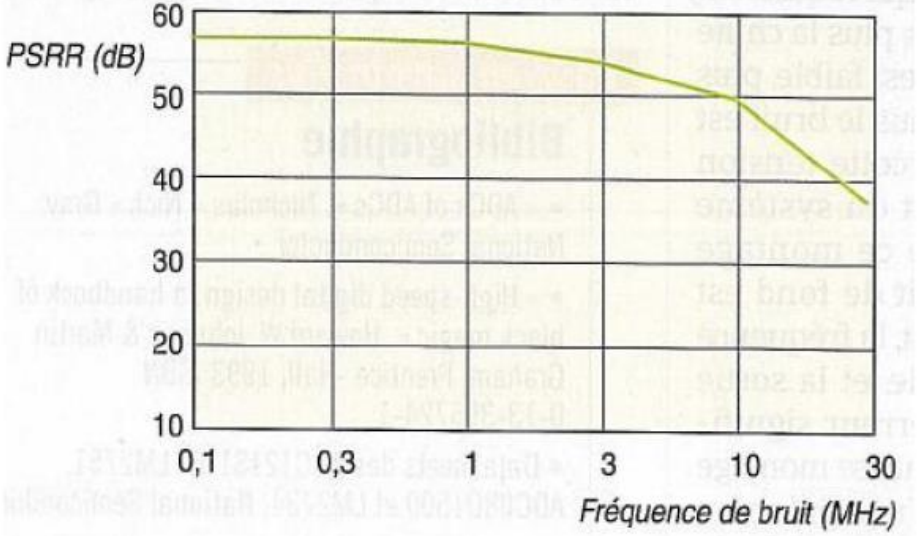
Power supply rejection

- How much tolerant are ADC to supplies
- Ideal:

PSRR	Power-supply rejection ratio	Without 0.1-µF board supply capacitors, with 100-kHz supply noise	85	85	dB

- Reality:

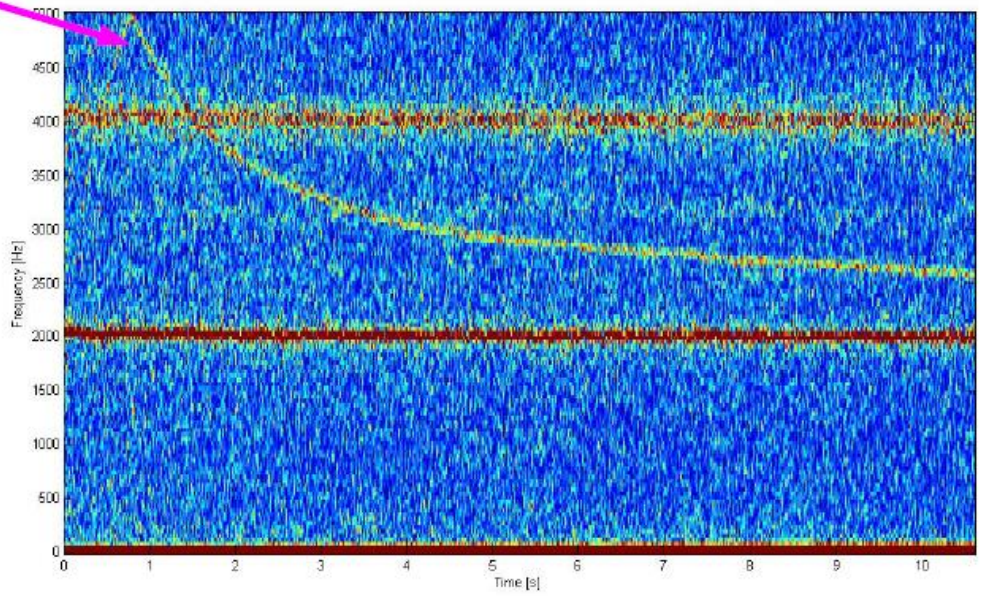
Taux de réjection de l'alimentation du CAN 12 bits ADC12040. Pour ce faire, un bruit d'amplitude 200 mV est injecté dans l'alimentation à différentes fréquences.



- Modern DC/DC switching freq : [500k … 2MHz]

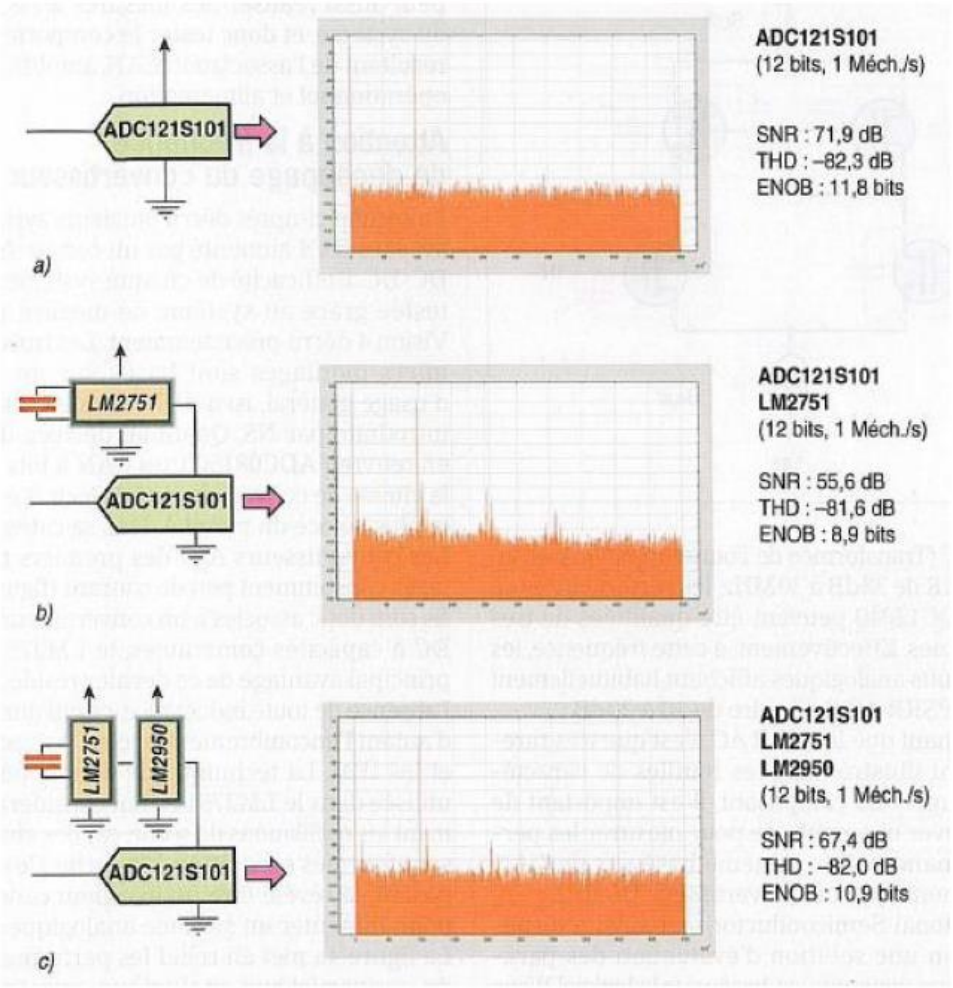
Power supply scheme (1)

- Synchronize DC/DC regulator to the master sampling clock
  to avoid this (Input grounded test; no LDO after DC/DC regulators):



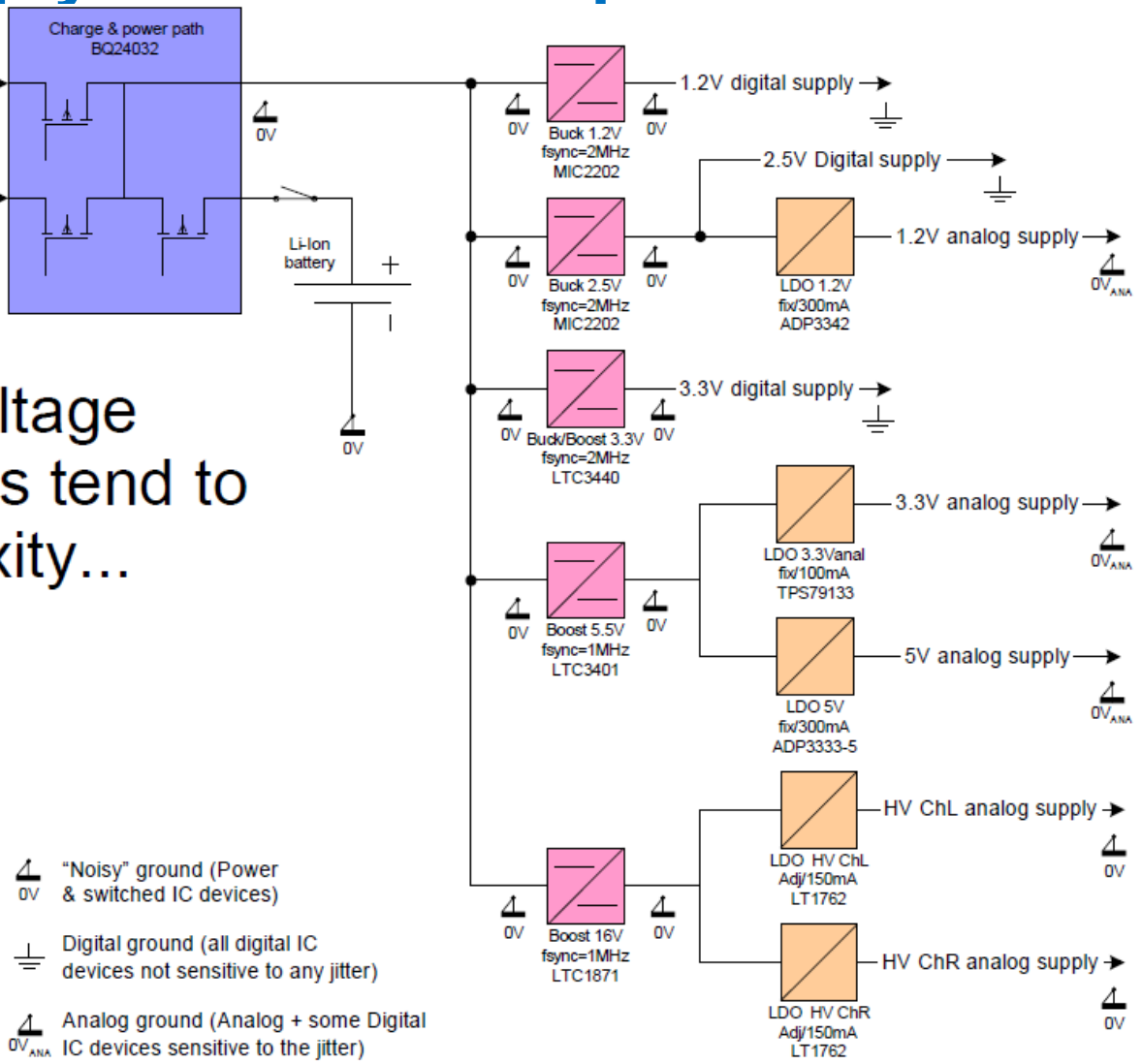
Power supply scheme (2)

- Analog Power Supply needs LDO !
  - 8-10 bits not dramatic
  - 12 bits & + : very important



Power supply scheme example

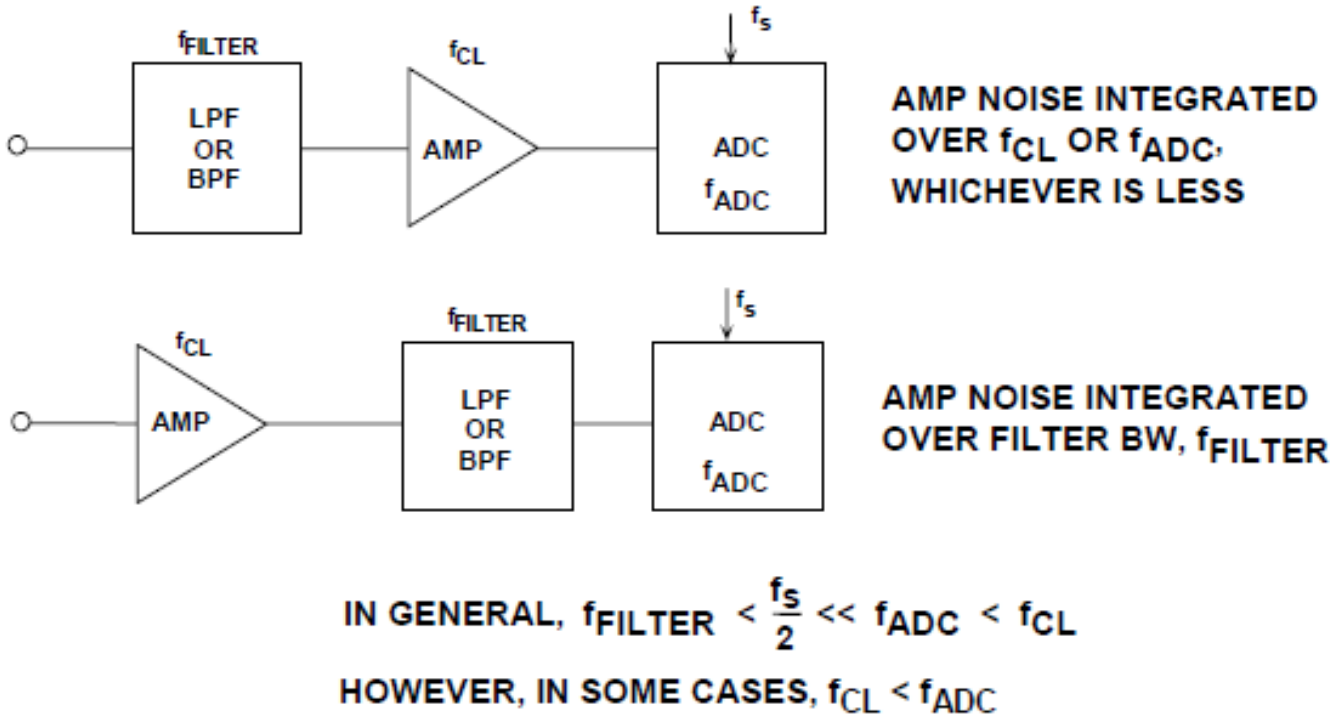
- Multi-voltage schemes tend to complexity...



Input matching (1)

- Determine the Nyquist freq and choose an ideal sample frequency. (1.2 .. 2 f_{NYQ})
- Evaluate the feasibility of an Over- / Undersampling process.
  - First selection of the ADC's family
- Evaluate the needs & specifications of an antialiasing filter (passive - active, corner freq, order...)
- Evaluate the needs & specifications of the voltage matching (attenuator, amplifier, level-shifter,...)

Input matching (2)



$$\text{IN GENERAL, } f_{FILTER} < \frac{f_S}{2} << f_{ADC} < f_{CL}$$

$$\text{HOWEVER, IN SOME CASES, } f_{CL} < f_{ADC}$$

Figure 6.39: *Proper Positioning of the Antialiasing Filter Will Reduce the Effects of Op Amp Noise*

Single ended and common mode adaptation

- Modern ADC are single supply

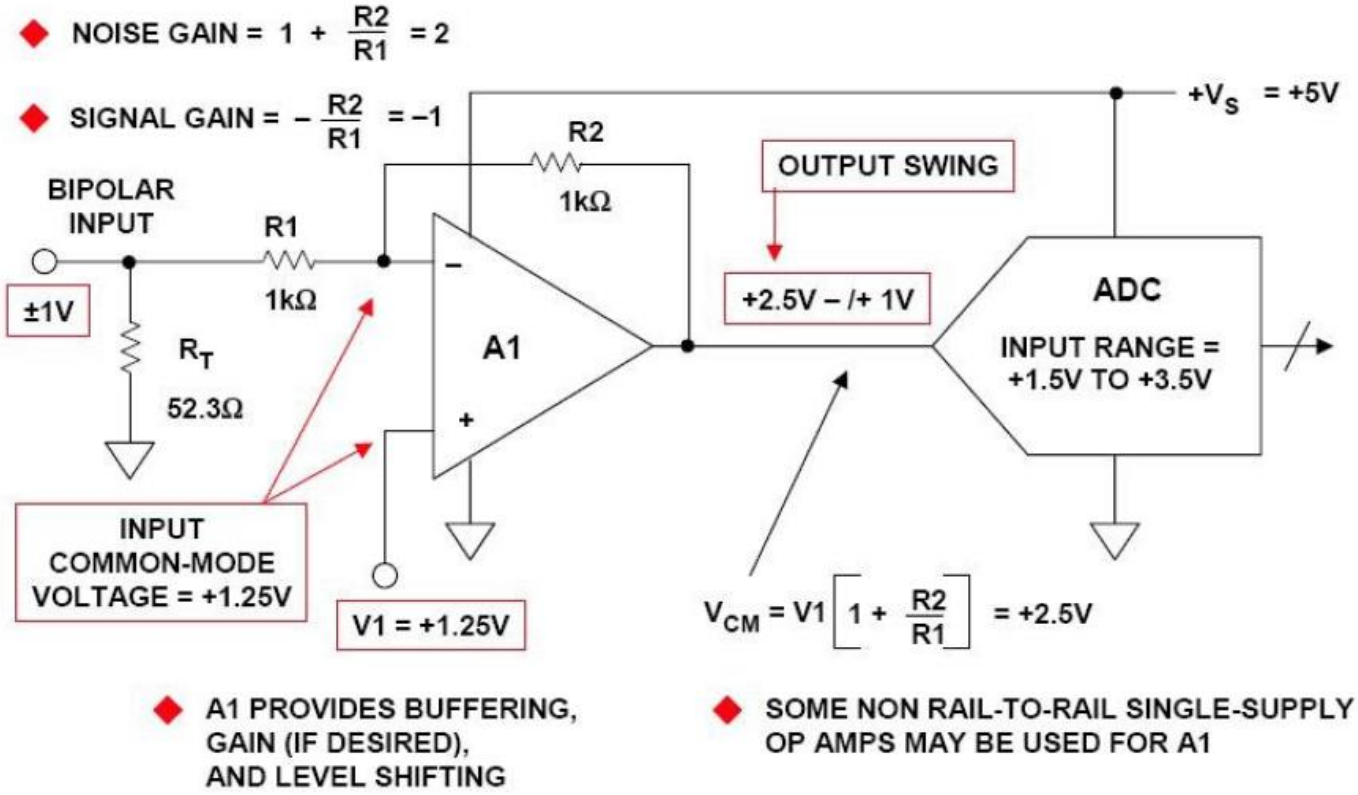


Figure 6.11: *Single-Ended Single-Supply DC-Coupled Level Shifter*

Single ended to differential (AC) conversion

- Transformer suits HF

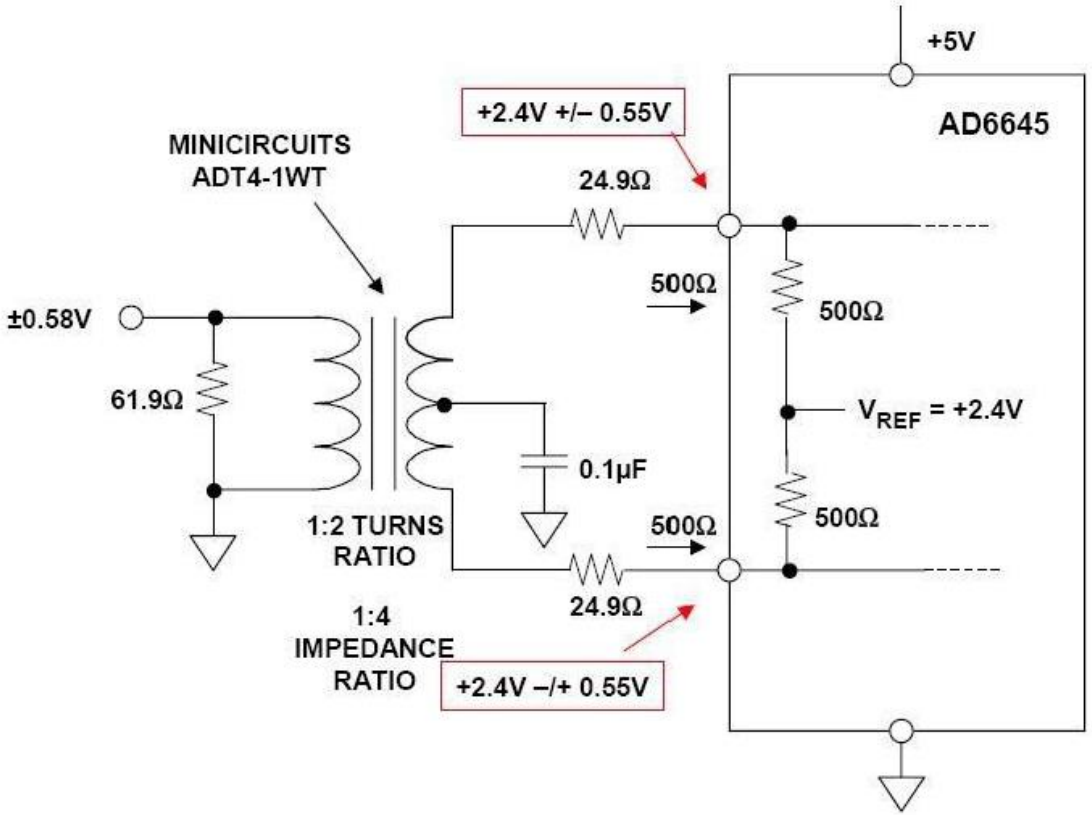


Figure 6.29: *Transformer Coupling into the AD6645 14-Bit, 80-/105-MSPS Complementary Bipolar Process ADC*

Single ended to differential (DC) conversion

- AO: high BW, high slew-rate, low-noise …

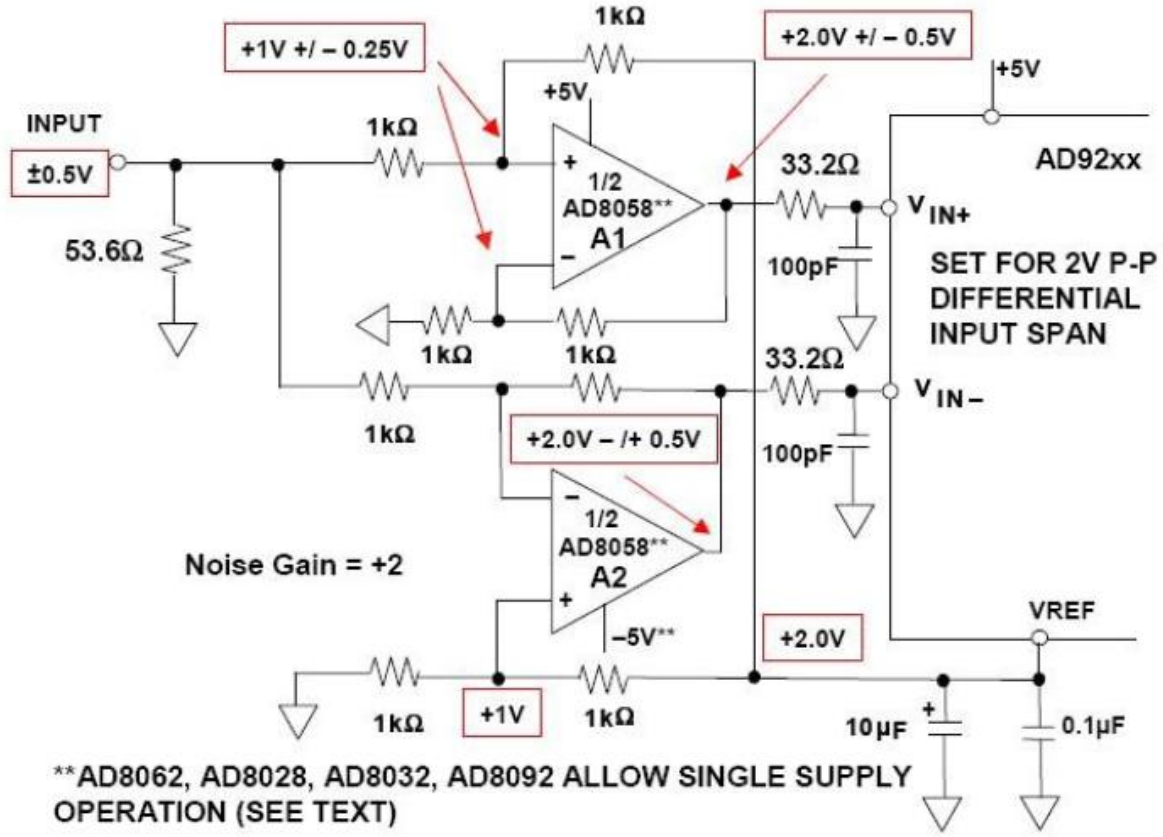
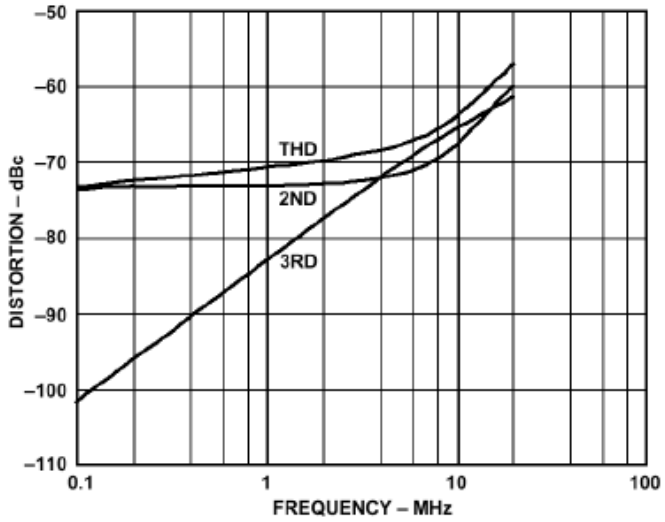
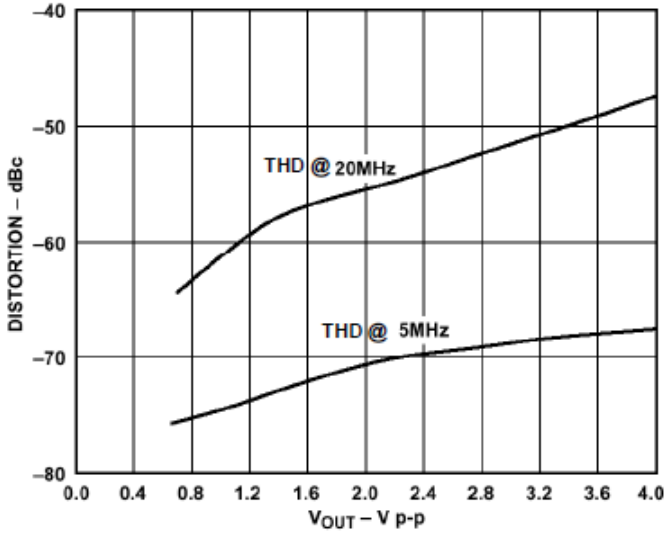


Figure 6.31: *Op Amp Single-Ended to Differential DC-Coupled Driver with Level Shifting*

Example for buffer distorsion performance



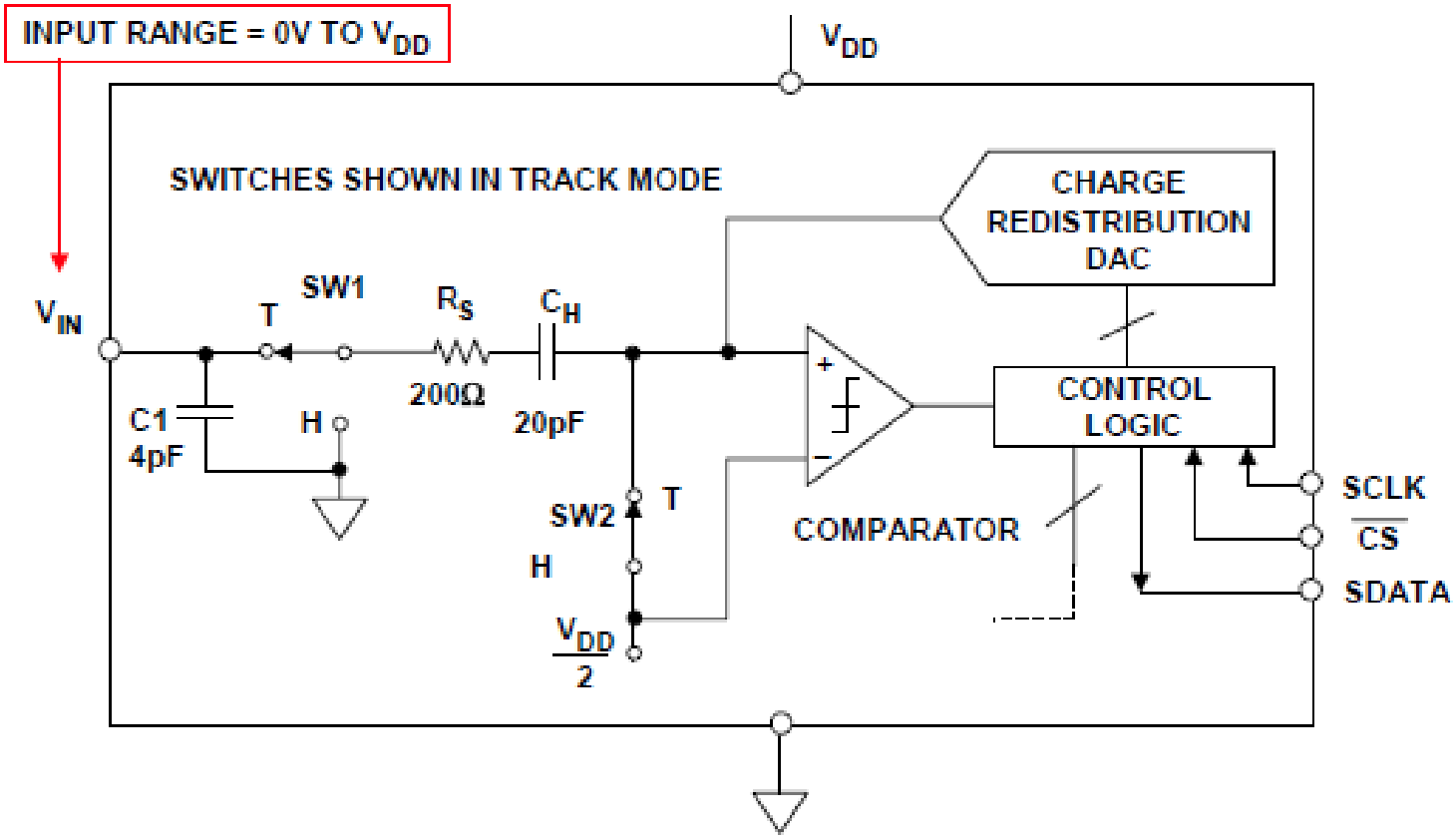
AD8057/AD8058 Op Amp Distortion Versus Frequency
G = +1, R_L = 150 Ω, V_S = ±5 V



AD8057/AD8058 Op Amp Distortion Versus Output Voltage
G = +1, R_L = 150 Ω, V_S = ±5 V

- Beware of distortion increase at high frequencies
- Performance may be better for higher load resistance

SAR ADC input characteristics



- Example: AD7466

Single supply SAR ADC with bipolar input

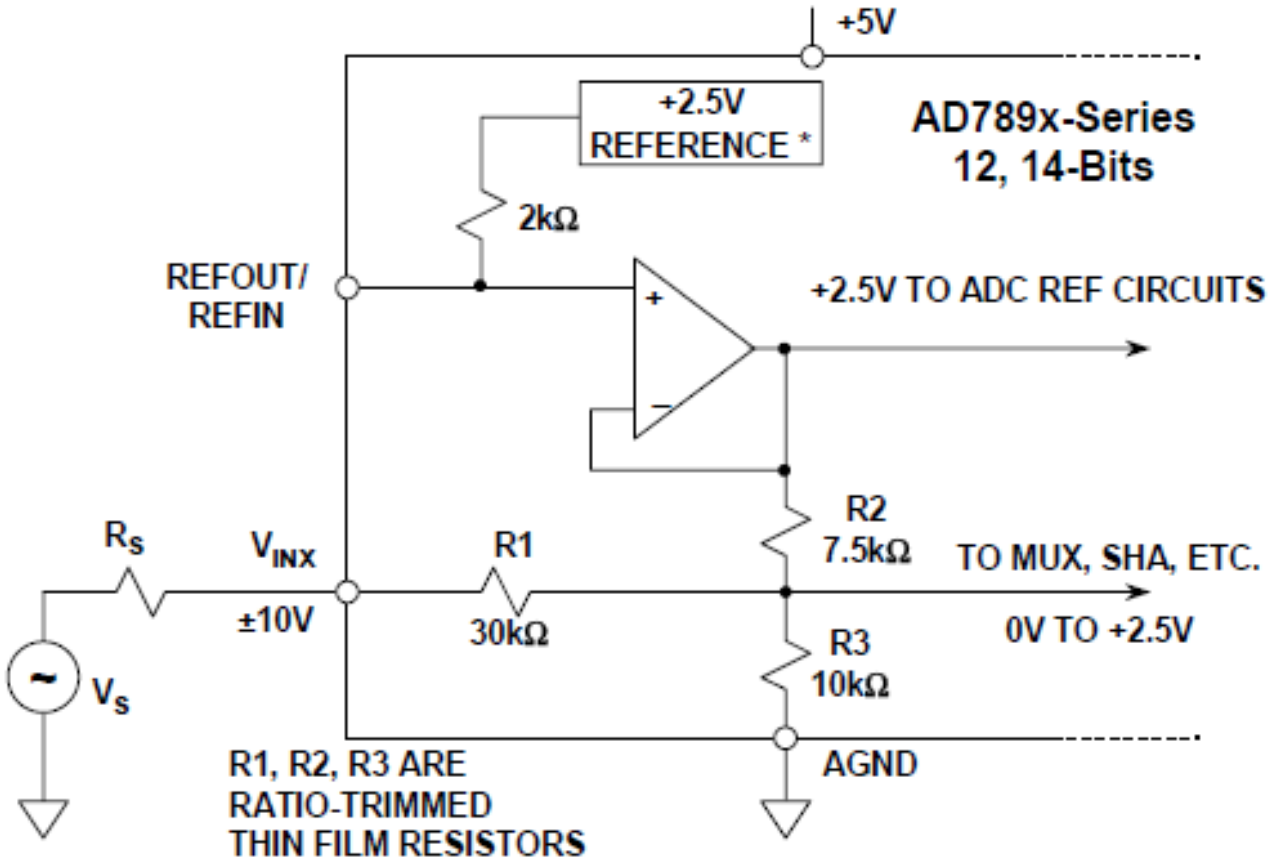
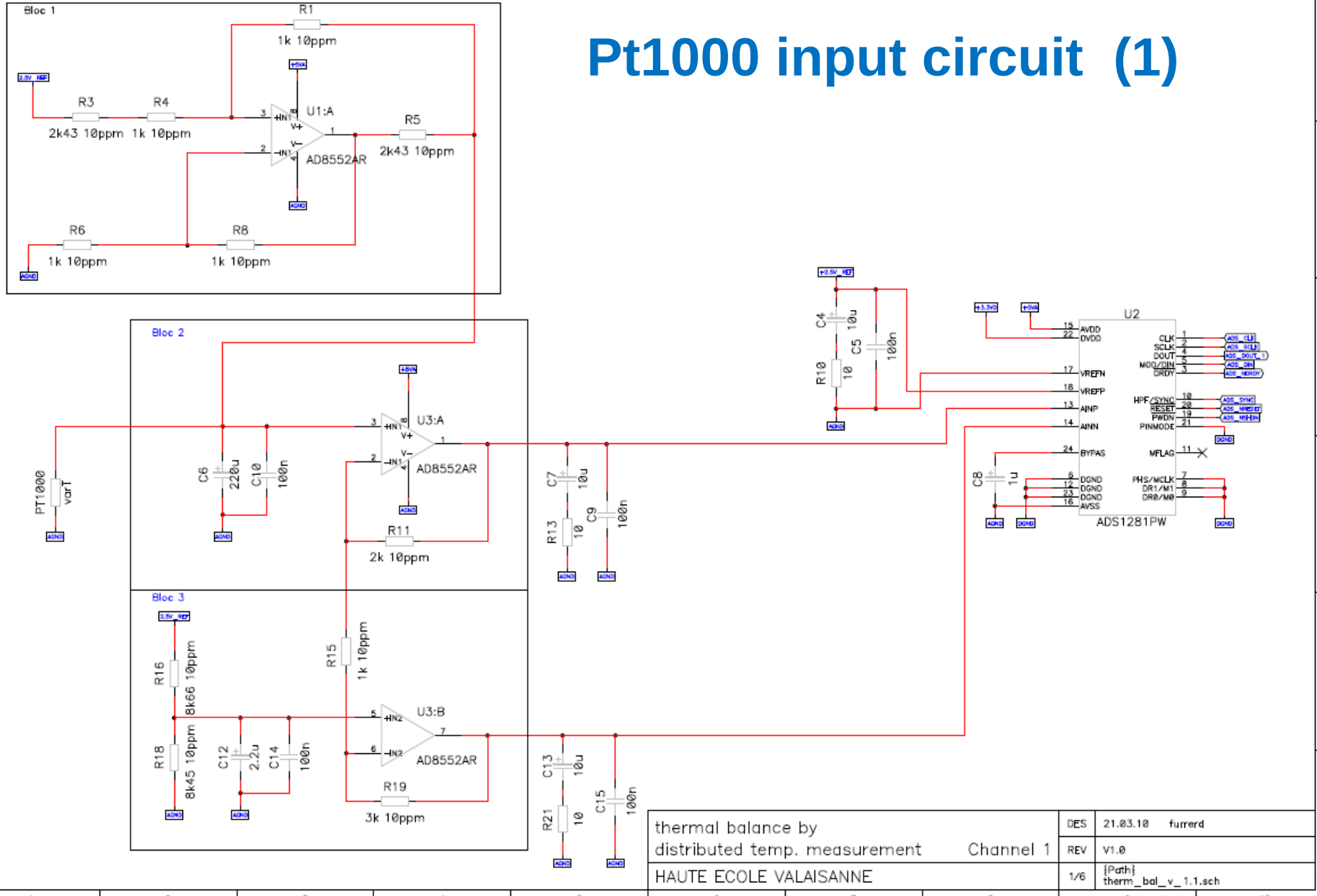


***Figure 6.19**: Driving Single-Supply Data Acquisition ADCs With Scaled Inputs*

- Scaling network at the input

Pt1000 input circuit (1)

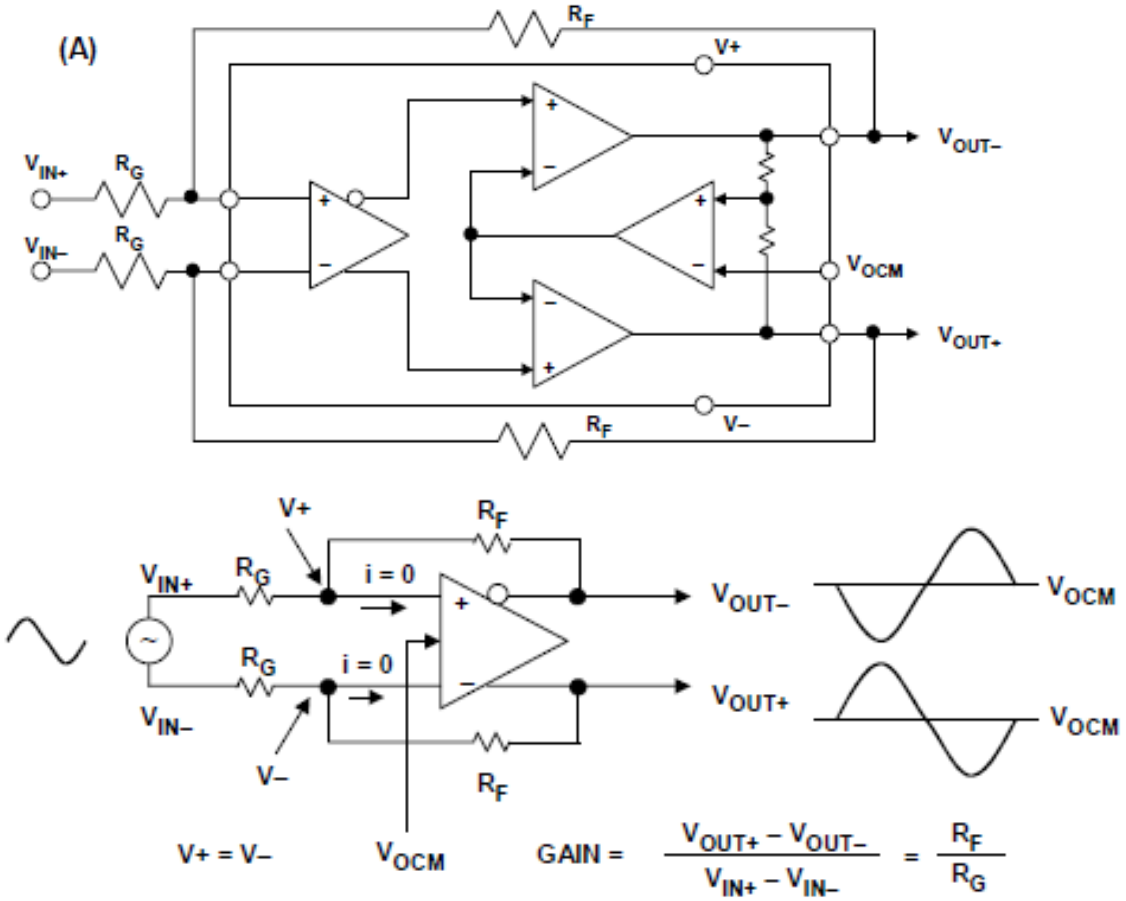


Pt1000 input circuit (2)

The circuit on the slide above acquires a temperature measured by a Pt1000 resistor, through a 24 bits ADC (ADS1281), with the following characteristics : f_s = 10Hz, dynamic range of AINP and AINN : 0…V_{ref}, conversion of V_{AINP}-V_{AINN} within the range ±V_{ref}. V_{ref} = 2.5V (net +2.5V_REF).

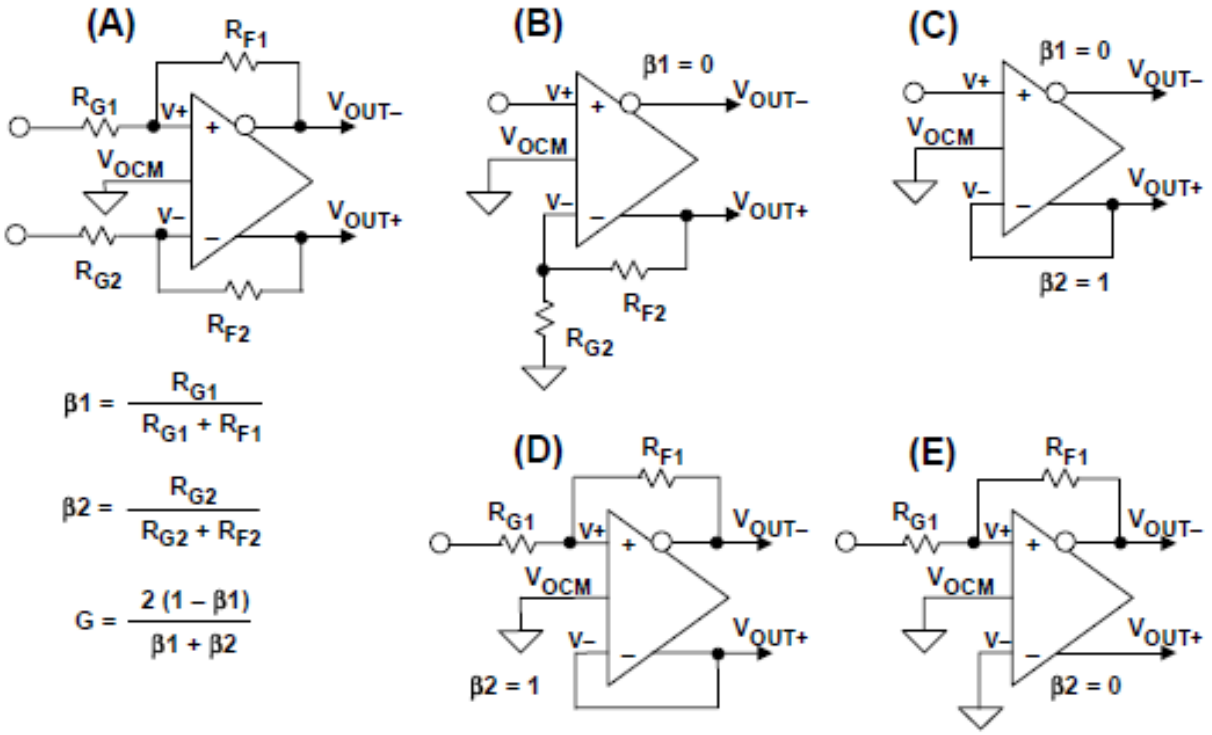
- Describe in words the function of each of the 3 framed blocks.
- Why are resistors R16 and R18 not set to equal values ?
- Determine the temperature measurement range in °C and the circuit sensitivity in LSB/°C, knowing that the resistance of the Pt1000 sensor is 1000Ω at 0°C, increasing by 0.4%/°C.
- Consider only voltage and current noises of the operational amplifiers AD8552: 40nV/rtHz and 2fA/rtHz, supposed to be uniform over frequency. What is the spectral density of the current noise in the Pt1000 sensor ? What is the spectral density of the voltage noise at inputs AINP and AINN of the A/D converter ? What is the signal-to-noise ratio between 0 and 5Hz after A/D conversion, taking into account quantization noise and noise in the operational amplifiers ?

Integrated differential amplifier drivers (1)



- + and – input currents are zero
- + and – input voltages are equal
- Output voltages are 180° out of phase and symmetrical about V_{OCM}
- Gain = R_F/R_G

Integrated differential amplifier drivers (2)



$$\beta 1 = \frac{R_{G1}}{R_{G1} + R_{F1}}$$

$$\beta 2 = \frac{R_{G2}}{R_{G2} + R_{F2}}$$

$$G = \frac{2\,(1 - \beta 1)}{\beta 1 + \beta 2}$$

- β_1 : Amount of feedback from V_{out-} to V+
- β_2 : Amount of feedback from V_{out-} to V+

Integrated differential amplifier drivers (3)

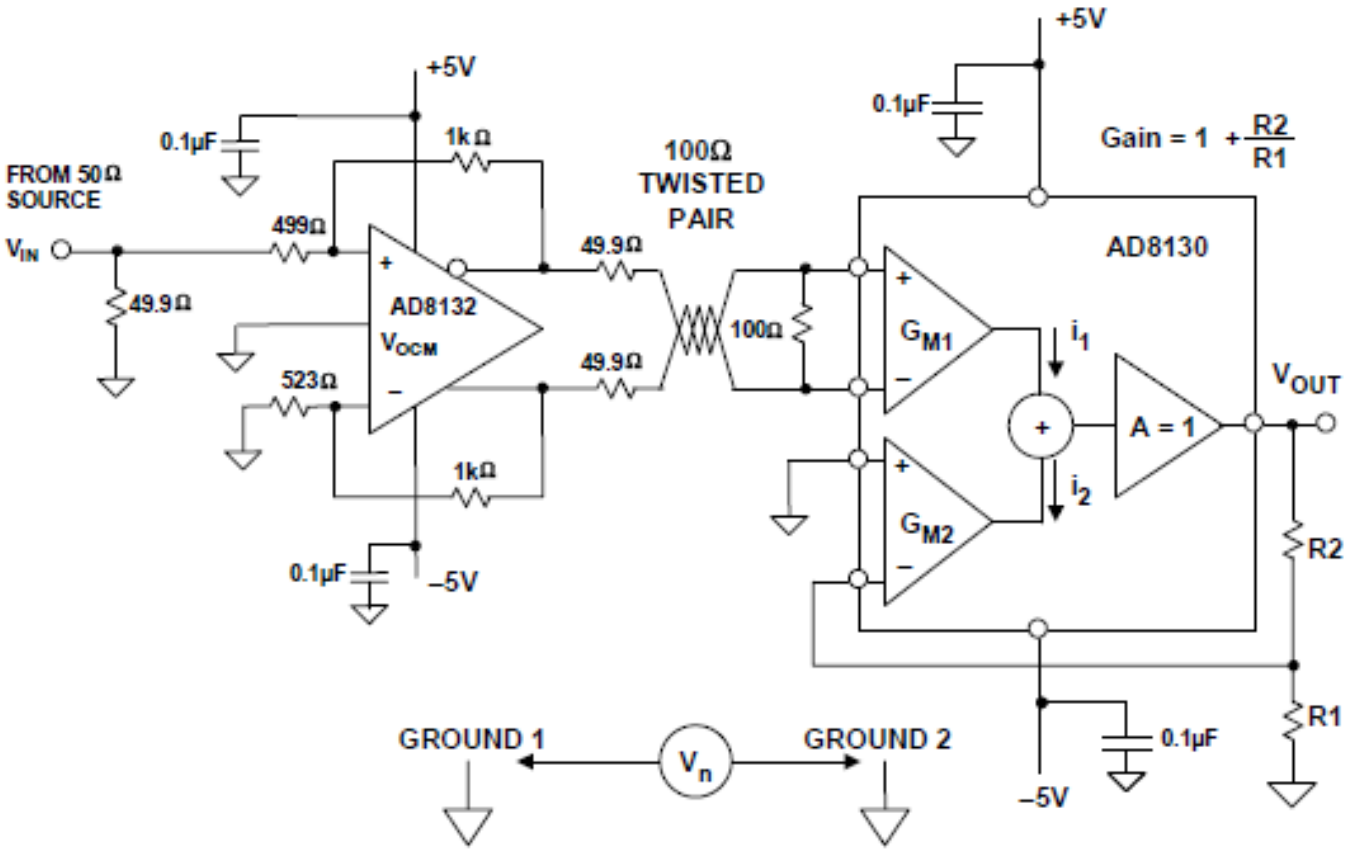


Figure 6.35: *High Speed Differential Line Driver, Line Receiver Applications*

Integrated differential amplifier drivers (4)

- Replacement for baluns when direct coupling required

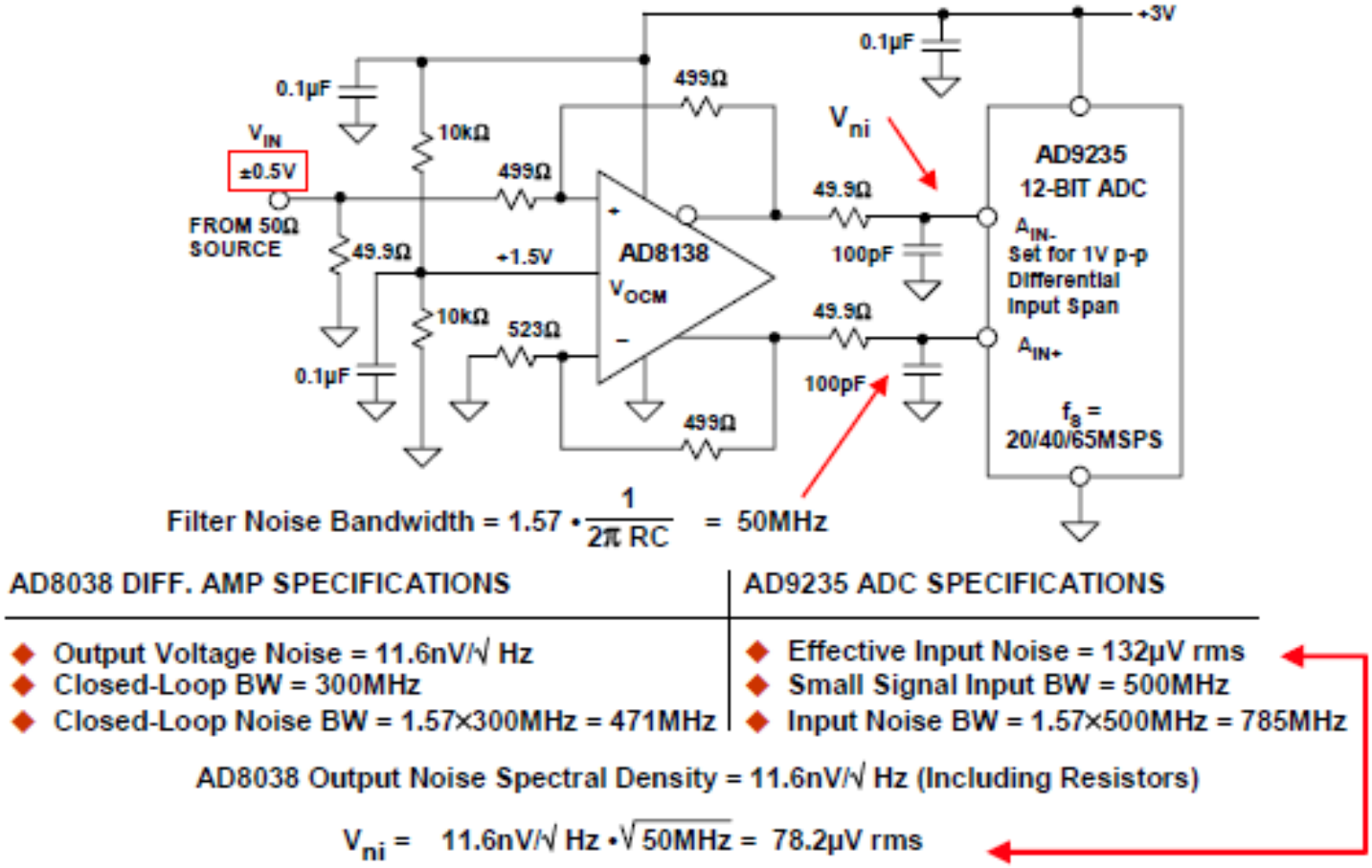


Figure 6.38: *Noise Calculations for the AD8138 Differential Op Amp Driving the AD9235 12-Bit, 20-/40-/65-MSPS ADC*

Front end bridge connection

- 4 wire Kelvin connection
- Ratiometric conversion

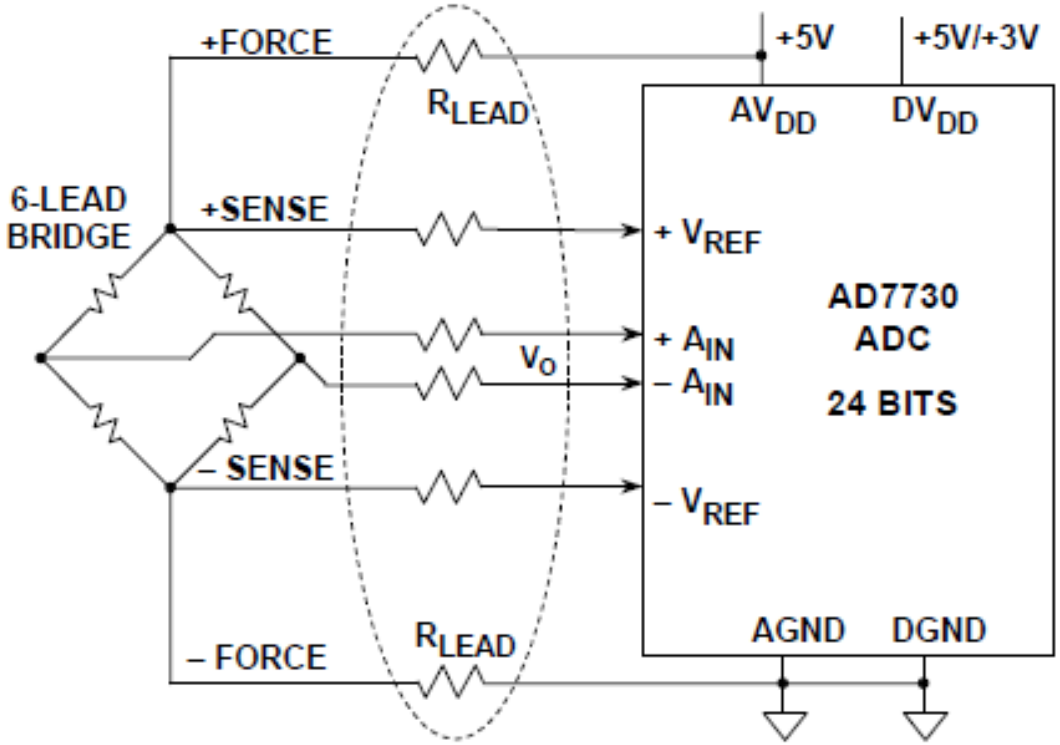
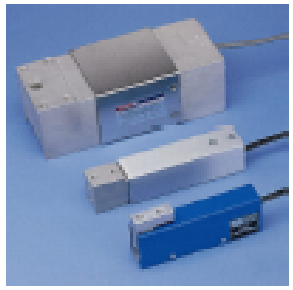


Figure 8.7: *AD7730 Bridge Application Showing Ratiometric Operation and Kelvin Sensing*

Weigh scale example (1)

- **Full Load:** 2 kg
- **Sensitivity:** 2 mV/V
- **Excitation:** 10 V max

- **Other Features**
  - Impedance 350 Ω
  - Total Error 0.025 %
  - Hysteresis 0.025 %
  - Repeatability 0.01%
  - Temperature drift: 10ppm
  - Overload 150%
  - Dimensions
  - Cost ($200)



TYPICAL LOAD CELLS

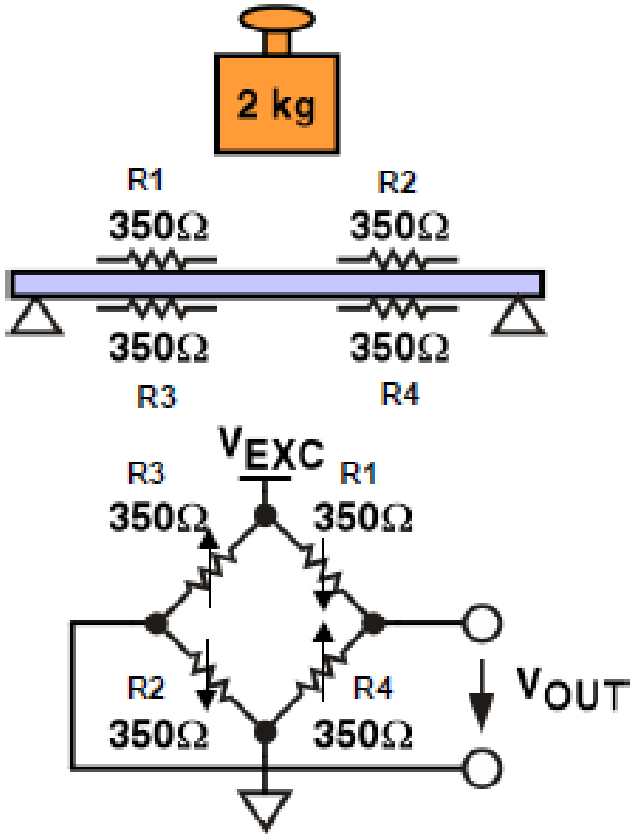


Figure 8.9: *Load Cell Characteristics*

Weigh scale example (2)

- **Full Load:** 2 kg
- **Sensitivity:** 2 mV/V
- **Excitation:** 5 V
  - $V_{FS} = V_{EXC} \times$ Sensitivity
  - $V_{FS} = 5V \times 2mV/V = 10$ mV
  - $V_{CM} = 2.5$ V
- **Full-Scale Output Voltage: 10 mV**
- **Proportional to excitation voltage**
  - "Ratiometric"

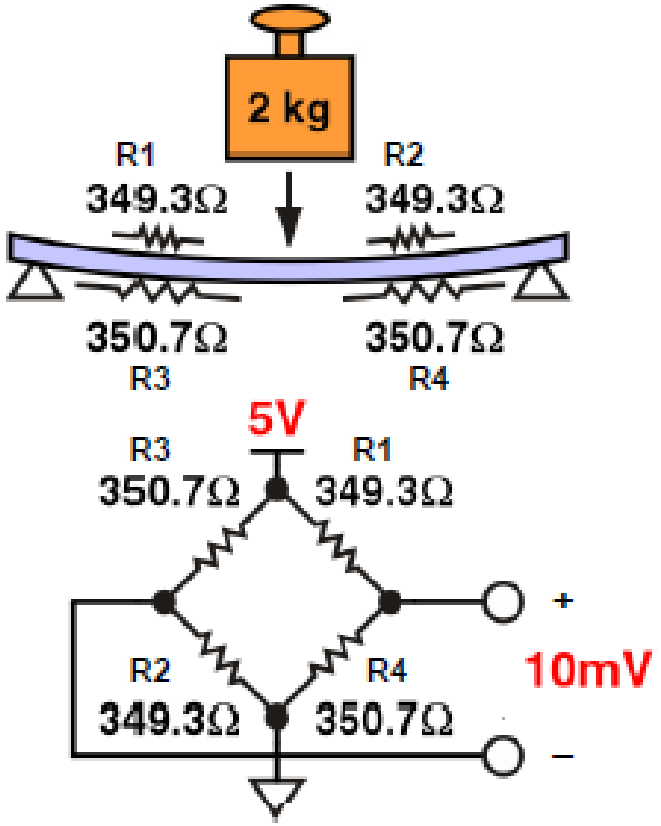


Figure 8.10: *Determining Fullscale Output of Load Cell with 5-V Excitation*

Weigh scale example (3)

- Required 0.1 g in 2 kg
  - # counts = full-scale / resolution
  - # counts = 2000 g / 0.1g = 20,000
- 20,000 counts
  - V_{FS} = 10mV @ 5V excitation
  - $V_{P-P} = V_{FS}$ / # counts
  - V_{P-P} = 10mV / 20,000 = 0.0005mV
- 0.5µV p-p noise
  - $V_{RMS} \approx V_{P-P} / 6.6$
  - $V_{RMS} \approx$ 0.5µV / 6.6 = 0.075µV
- 75nV RMS noise
  - Bits p-p = $\log_{10}(V_{FS} / V_{P-P}) / \log_{10}(2)$
  - Bits p-p = log(10mV / 0.0005mV) / 0.3
- 14.3 bits p-p in 10mV range (Noise-free bits)
  - Bits RMS = $\log_{10}(V_{FS} / V_{RMS}) / \log_{10}(2)$
  - Bits RMS = $\log_{10}$(10mV / 0.000075) / 0.3
- 17.0 bits RMS in 10mV range (Effective resolution)

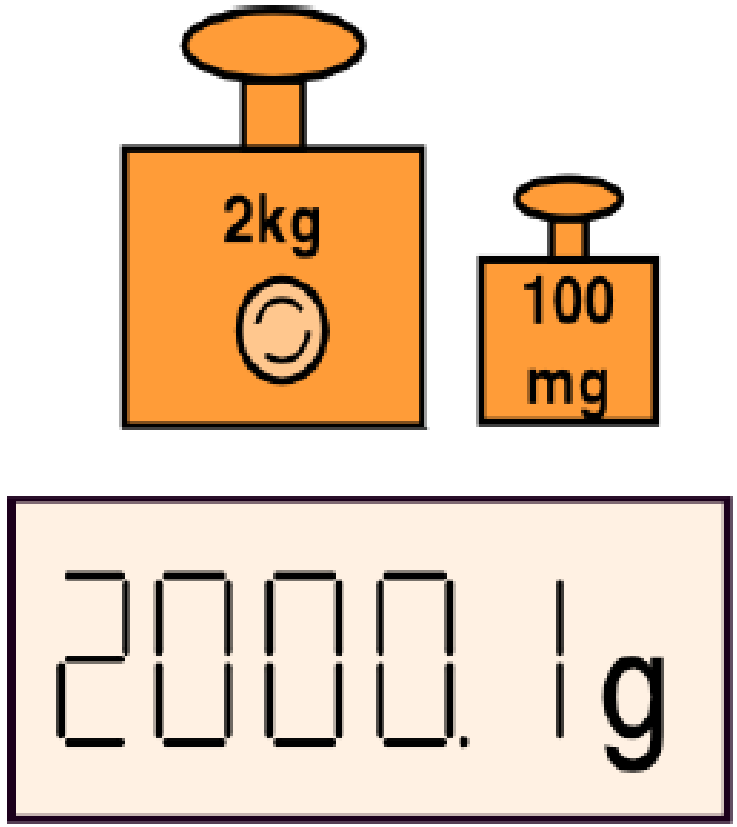


Figure 8.11: *Determining Resolution Requirements*

Weigh scale example (4)

The noise-free code resolution of the ADC is calculated as follows:

$$\text{Noise-Free Code Resolution (Bits)} = \frac{\log_{10}\left(\frac{V_{FS}}{V_{PP}}\right)}{\log_{10}(2)}$$

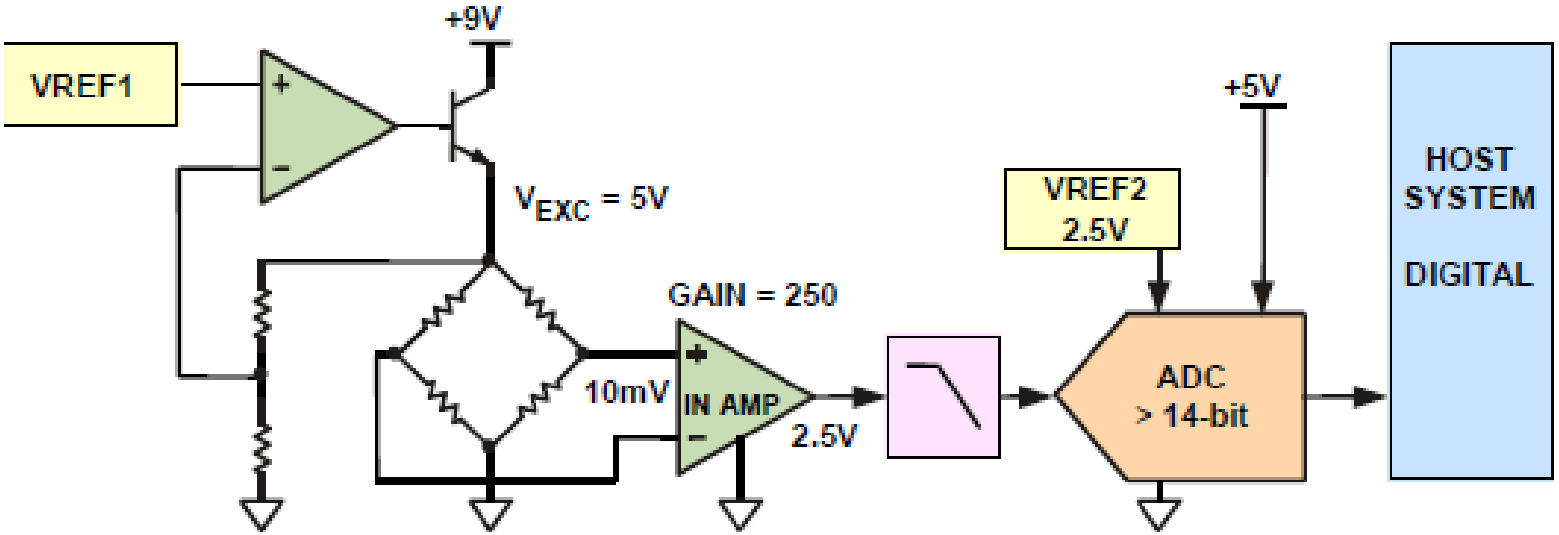
$$= \frac{\log_{10}\left(\frac{10\text{mV}}{0.5\mu\text{V}}\right)}{\log_{10}(2)} = 14.3 \text{ bits} .$$

The effective resolution of the ADC is calculated as follows:

$$\text{Effective Resolution (Bits)} = \frac{\log_{10}\left(\frac{V_{FS}}{V_{PP}/6.6}\right)}{\log_{10}(2)}$$

$$= \frac{\log_{10}\left(\frac{10\text{mV}}{0.5\mu\text{V}/6.6}\right)}{0.3} = 17 \text{ bits.}$$

Weigh scale example (5)

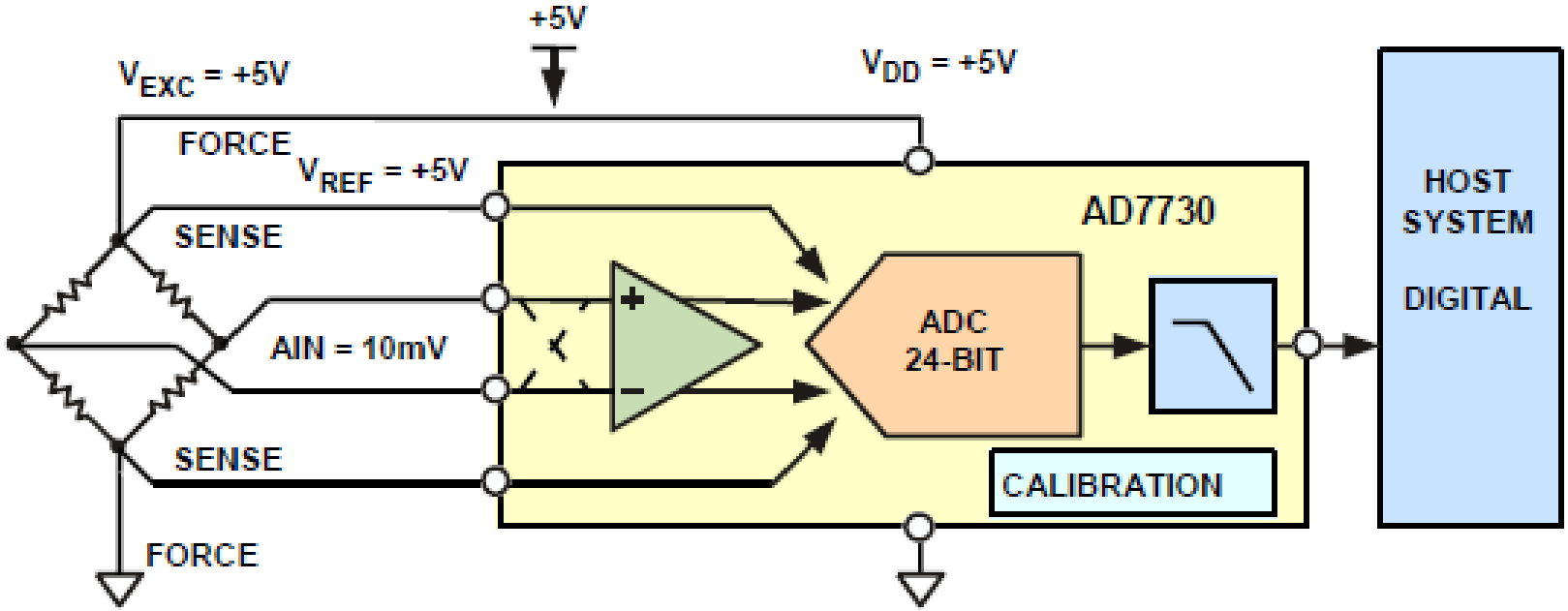


- **Complicated design**
- **Low pass filter is needed to keep low noise**
  - For example, –3dB @ 10Hz, –60dB @ 50Hz (difficult filter design)
- **Instrumentation amplifier performance is critical**
  - Low noise (AD620: 0.28µV p-p noise in 0.1Hz to 10Hz BW is approximately 42nV RMS), low offset, low gain error

Figure 8.12: *Traditional Approach to Design*

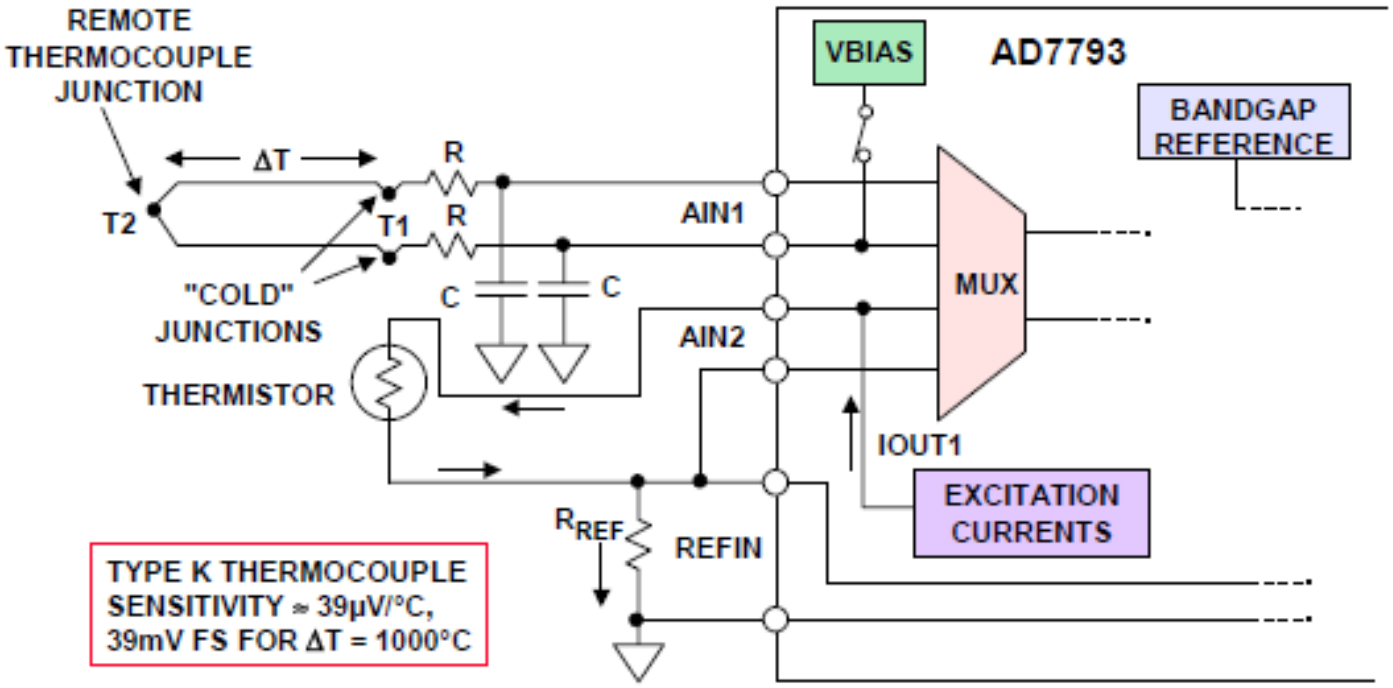
Weigh scale example (6)

- Ratiometric conversion



- **AD7730 was designed for bridge transducers**
  - Chopper, Buffer, PGA, Digital filter, tare DAC, Calibrations, …
- **Fully Ratiometric, changes on V_{EXC} = V_{REF} eliminated**
  - Load ≈ V_{OUT} / V_{EXC}, AD7730 Data ≈ V_{IN} / V_{REF}, V_{REF} = V_{EXC}

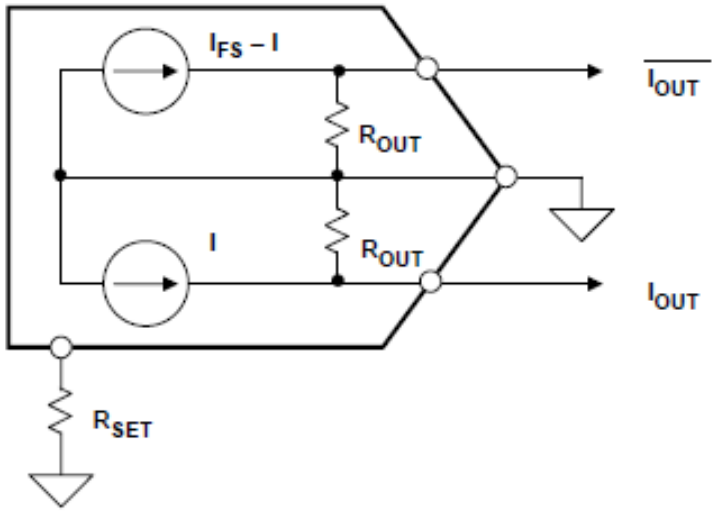
Thermocouple interface



- Bias voltage generator used to generate a common mode voltage for AIN1
- Current source provides current to thermistor for cold junction compensation and ratiometric operation using REFIN

Figure 8.19: *Thermocouple Design with Cold Junction Compensation using the AD7793*

DAC output model



- I_{FS} 2 - 20mA typical
- Bipolar or BiCMOS DACs sink current, $R_{OUT} < 500\Omega$
- CMOS DACs source current, $R_{OUT} > 100k\Omega$
- Output compliance voltage < ±1V for best performance

Figure 6.68: *Generalized Model of a High Speed DAC Output such as the AD976x and AD977x Series*

Output buffers

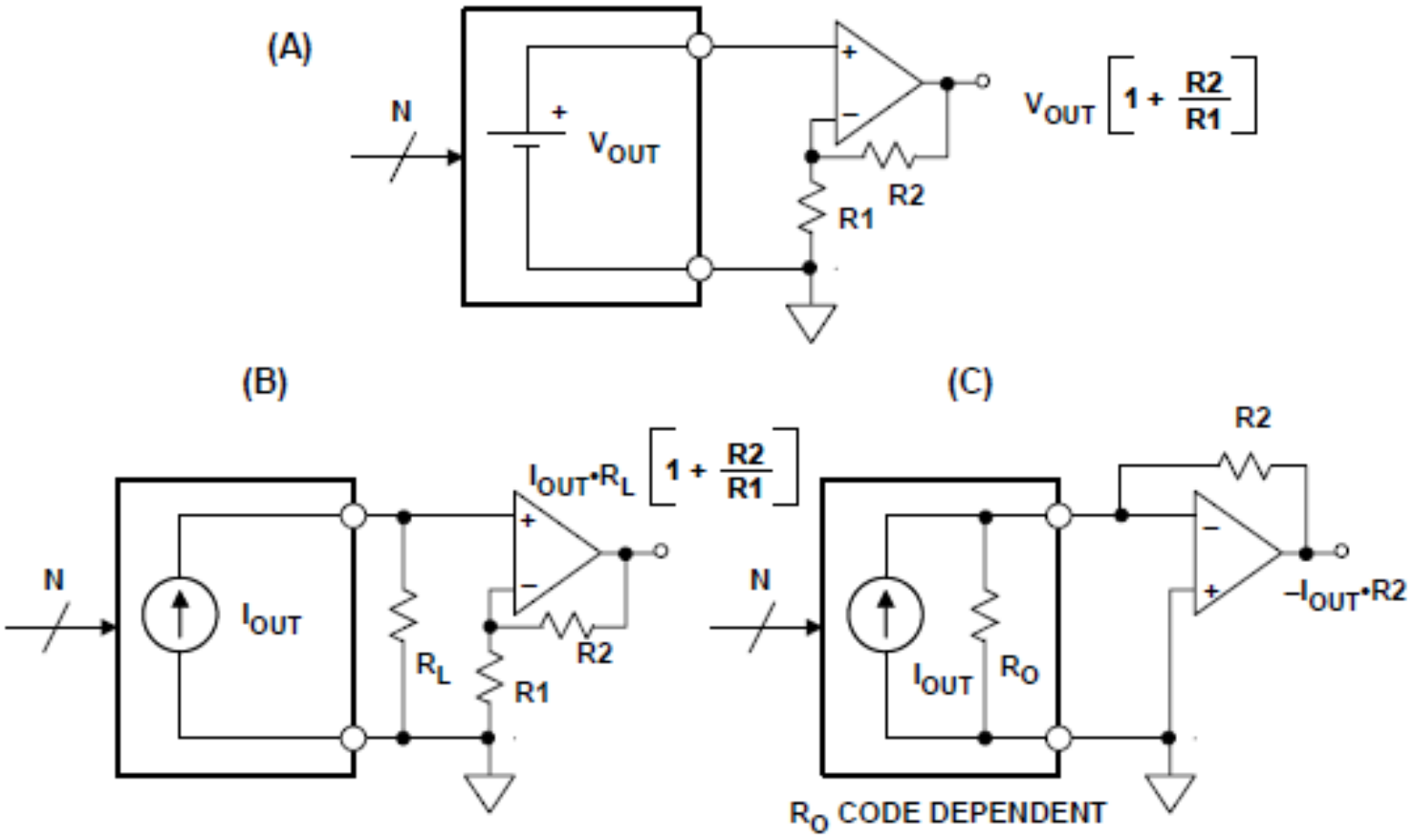


***Figure 6.67**: Buffering DAC Outputs with Op Amps*

AC coupled differential DAC output

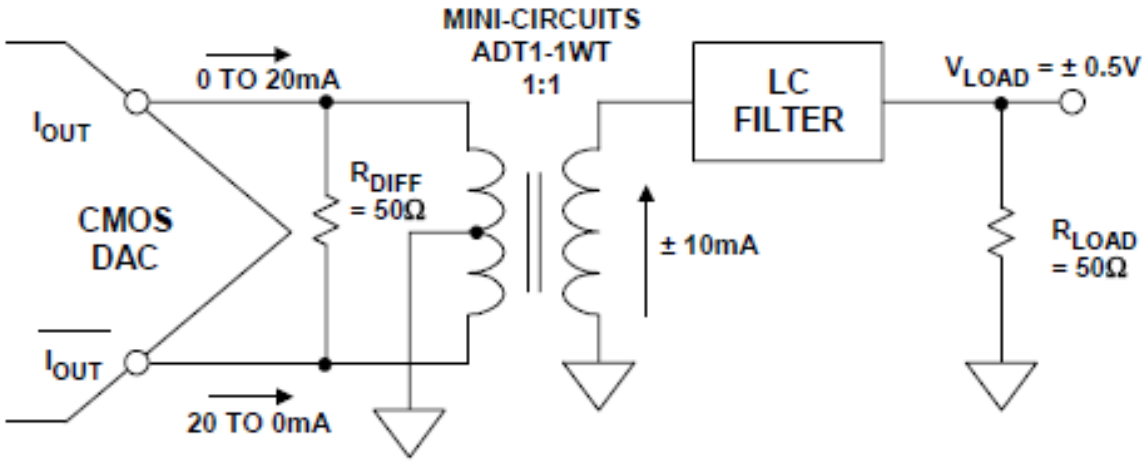
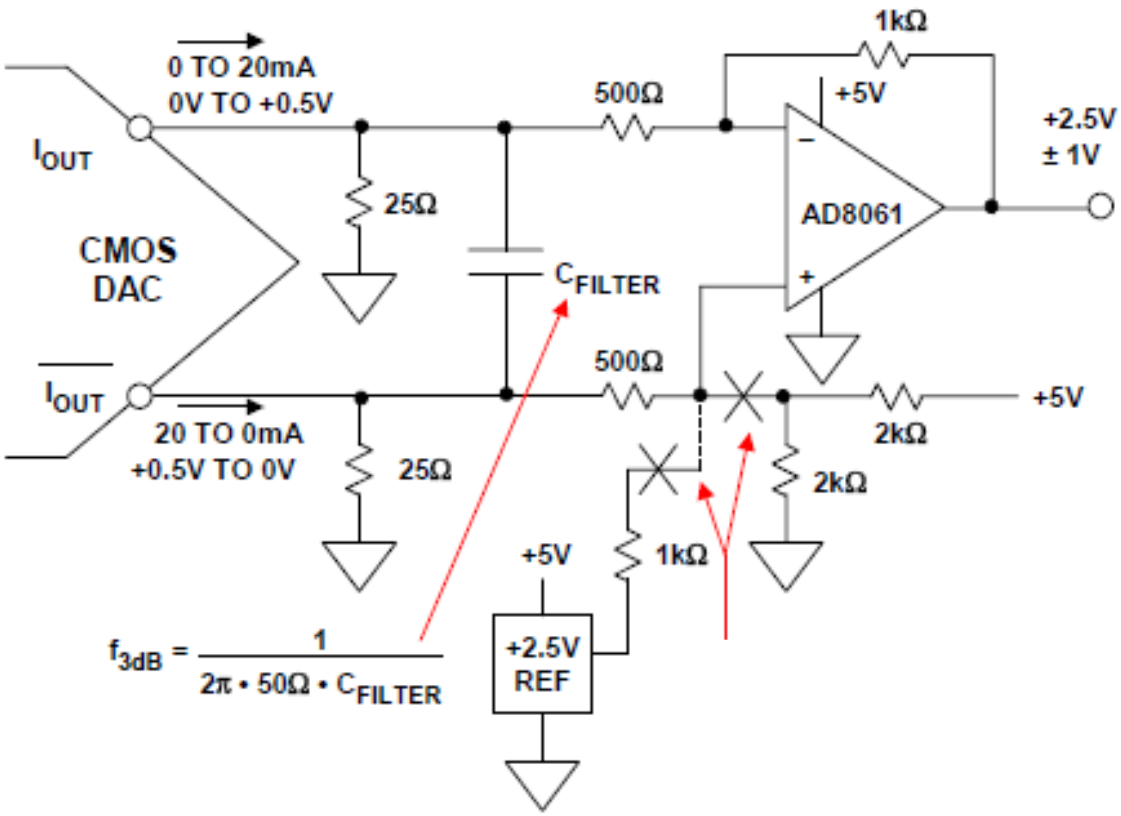


Figure 6.69: *Differential Transformer Coupling*

DC coupled differential DAC output



Differential DC Coupled Output Using a Single-Supply Op Amp

Output low-pass filtering

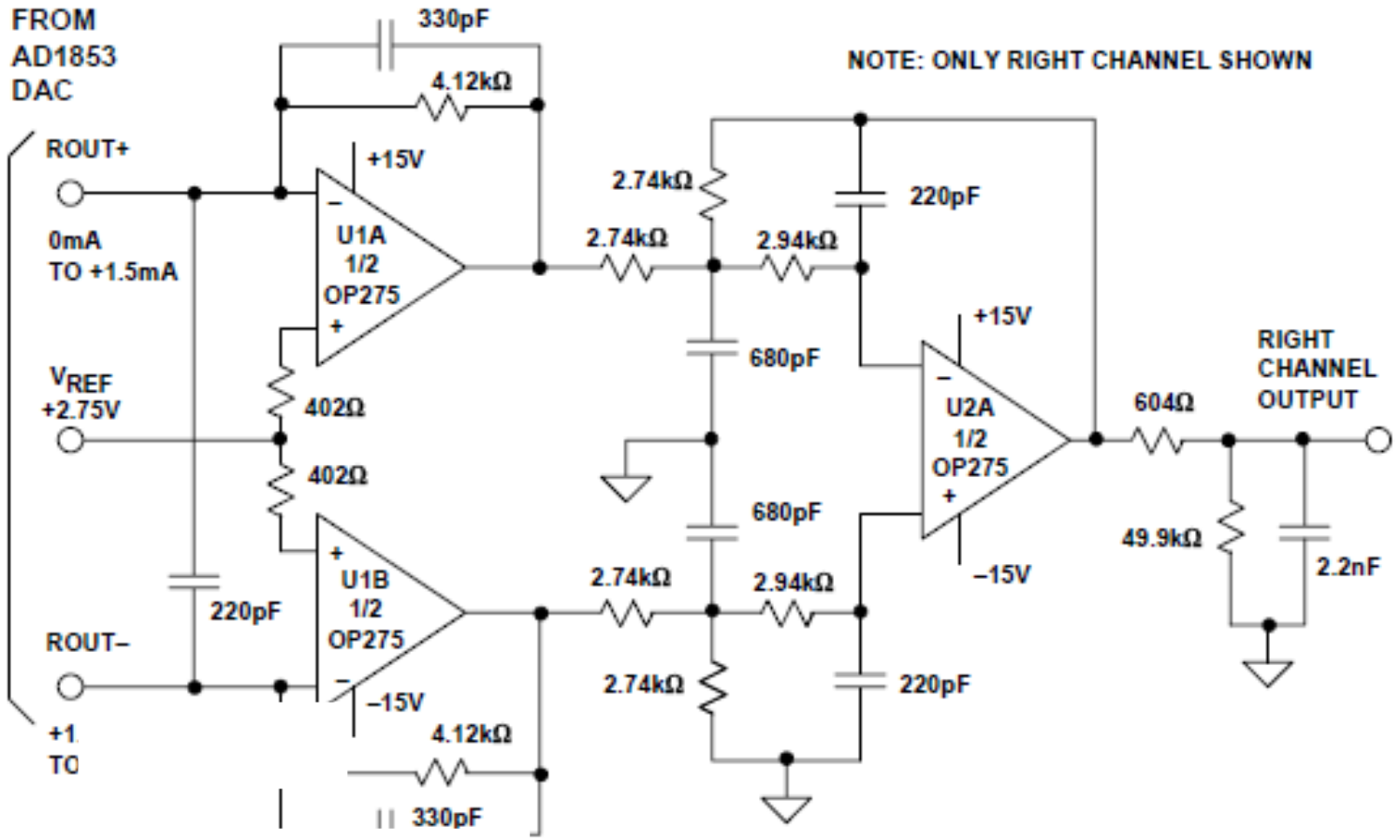


Figure 6.75: *A 75-kHz 4-Pole Gaussian Active Filter for Buffering the Output of the AD1853 Stereo DAC*

References

W. Kester (ed.): *Analog-Digital Conversion*, Analog Devices 2004, ISBN 0-916550-27-3

This reference was used as a basis for the present presentation, a series of illustrations are taken from it.

The book is available for download on the moodle server.

Tietze, Schenk: *Halbleiter-Schaltungstechnik*, Springer 2012 (14th ed.), ISBN 3-540-64192-0