AdvElDes

Exercices

Digital Timing Analysis

Classe	Date :
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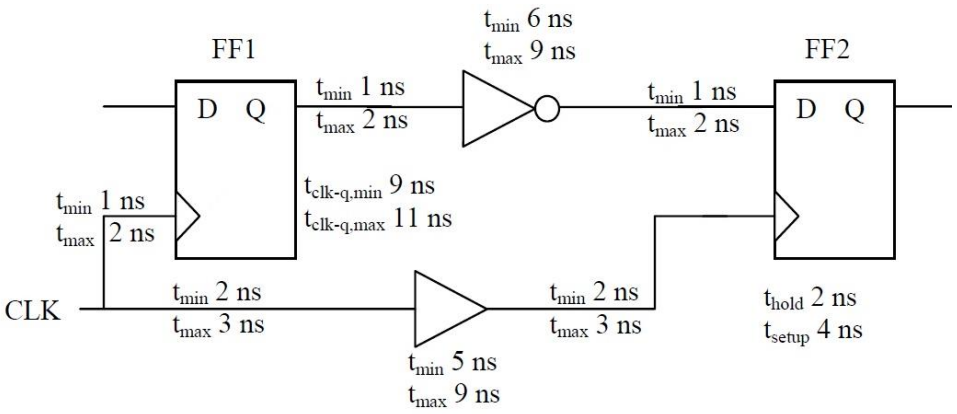
Exercice 1

In the following circuit, verify if there is any setup or hold violation (clock period=15ns).



Solution

1. Hold Time Constraint Analysis

Calculate **Minimum** delay along data path

Calculate **Maximum** delay along the clock path

If the difference between the data path and the clock path is negative, then a hold timing violation has occurred.

Data path: FF1/CLK -> FF1/Q-> inverter->FF2/D

Minimum delay in Data Path: min (wire delay CLK to CLK input of FF1) +min(tpcq)+ min(tpinv)+min (2 wire delay) = (1+9+6+2) ns=18ns

Maximum delay in clock Path: max (wire delay) +max(tpbuf)+max (wire delay) +max (thold FF2) = (6+9+3) ns+2ns=17ns

Difference between the data path and the clock path: 18ns-17ns=1ns ← positive Hold slack, hold timing violation

2. Setup Time Constraint Analysis

Calculate **Maximum** delay along data path

Calculate **Minimum** delay along the clock path

If the difference between the clock path and the data path is negative, then a setup timing violation has occurred.

Maximum delay in Data Path: max (wire delay CLK to CLK input of FF1) +max(tpcq)+ max(tpinv)+max (2 wire delay= (2+11+9+2*2) ns=26ns

Minimum delay in clock Path: (clock period) + min (wire delay) +min(tpbuf)+min (wire delay) -min (tsetup FF2) = (15ns) +(2+5+2) ns-4ns=20ns

Difference between the clock path and the data path: 20ns-26ns=-6ns ← negative setup time violation