Contents

- Principles of DA and AD conversion
- Static performance characteristics of DAC and ADC
- Review of DA converter structures

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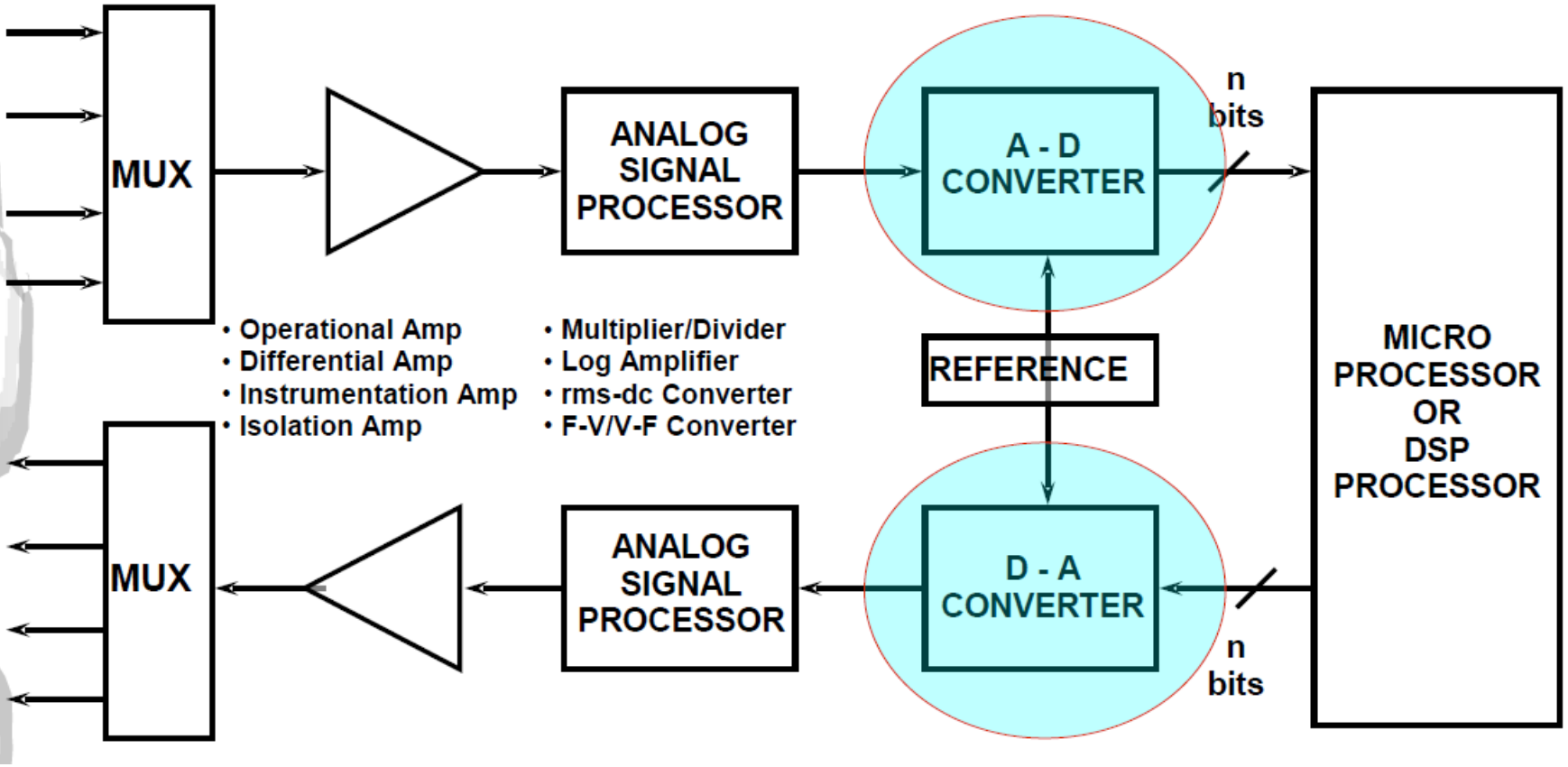
Converter's basics

⌘ Physical Domain ↔ Digital Domain



Converter's basics

AD & DA Converters are not only circuits but must be seen as a SYSTEM, with two kind of processes :

- Quantization of the AMPLITUDE (today)
- Quantization of the TIME (next week!)

AMPLITUDE Quantization

- (Analog) Signal Vs (Digital) Number [1.2]

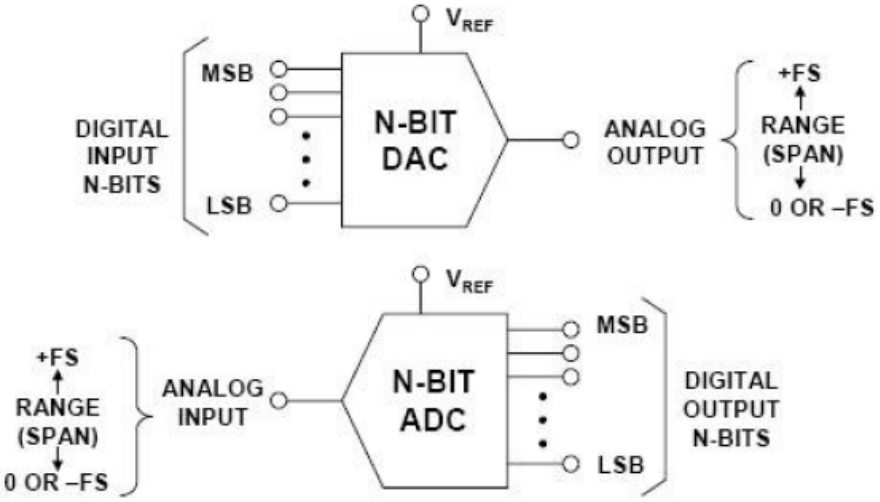


Figure 2.1: *Digital-to-Analog Converter (DAC) and Analog-to-Digital Converter (ADC) Input and Output Definitions*

Analog Side: Full Scale

- Amplitude of the analog domain must meet the Full Scale of the converter (FS value)
  - FS is a technological constraint of the converter (Circuit selection!)
- FS is related to a Reference Value (V_{REF})
- « Input Voltage » right understanding!
  - Input Channel single-ended (SE) or differential (Diff) ?
  - Unipolar or bipolar ? Middle value of FS at 0V or $V_{CC}/2$ (or …)

Analog Side: Dynamic Range

- The Dynamic Range is the ratio of the larger and the smaller voltage of the INPUT SIGNAL
- DR is a primary caracteristic of the application, not of the converter!
- Converter have to be better than signal's DR, but how much better?

Def. : Resolution

- Resolution N is the *number of bits* of the digital number side
- Resolution Step is the *analog value* of the interval between two adjacent code values, also called « 1 LSB »
- 2^N digital levels (codes) : [0 to 2^N -1]
  - $Nbr_{MAX} = 2^N - 1$: « 1111111... »
  - By def. « all-1's code » => 1 lsb below FS value

Coding style of numbers

- Number's coding : format of codes are ...
  - Straight binary
  - (Gray)
  - Offset binary
  - 2's complement
  - (1's complement)
  - (sign + magnitude)

Def. : Transfer Function

- Ideal TF

$$\text{Code} = \frac{V_{IN}}{V_{FS}} * 2^{N} - 1$$

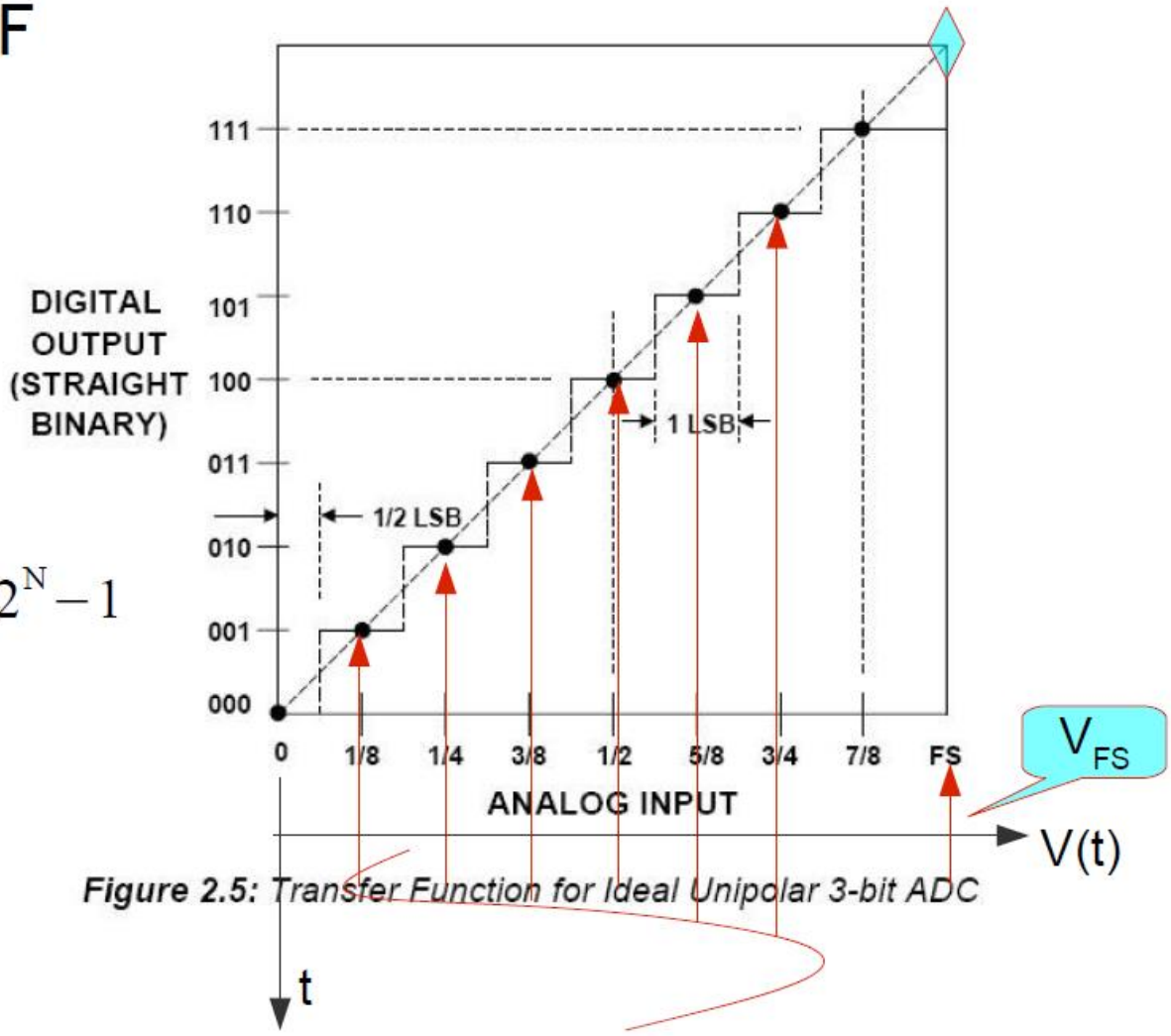
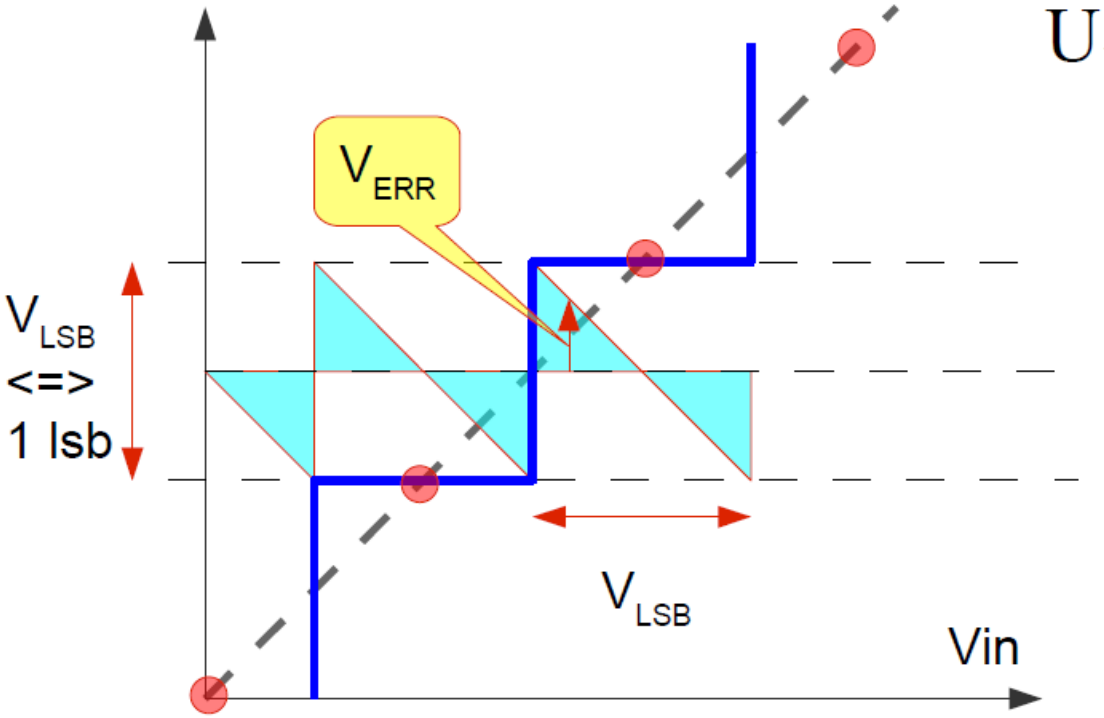


Figure 2.5: Transfer Function for Ideal Unipolar 3-bit ADC

Amplitude quantization error

- Power : $$E_N = \frac{1}{V_{LSB}} \int_{-q/2}^{q/2} V_{ERR}^2(V_{IN})\, dV_{IN} = \frac{V_{LSB}^2}{12}$$

$$U_{N(RMS)} = \frac{V_{LSB}}{\sqrt{12}}$$

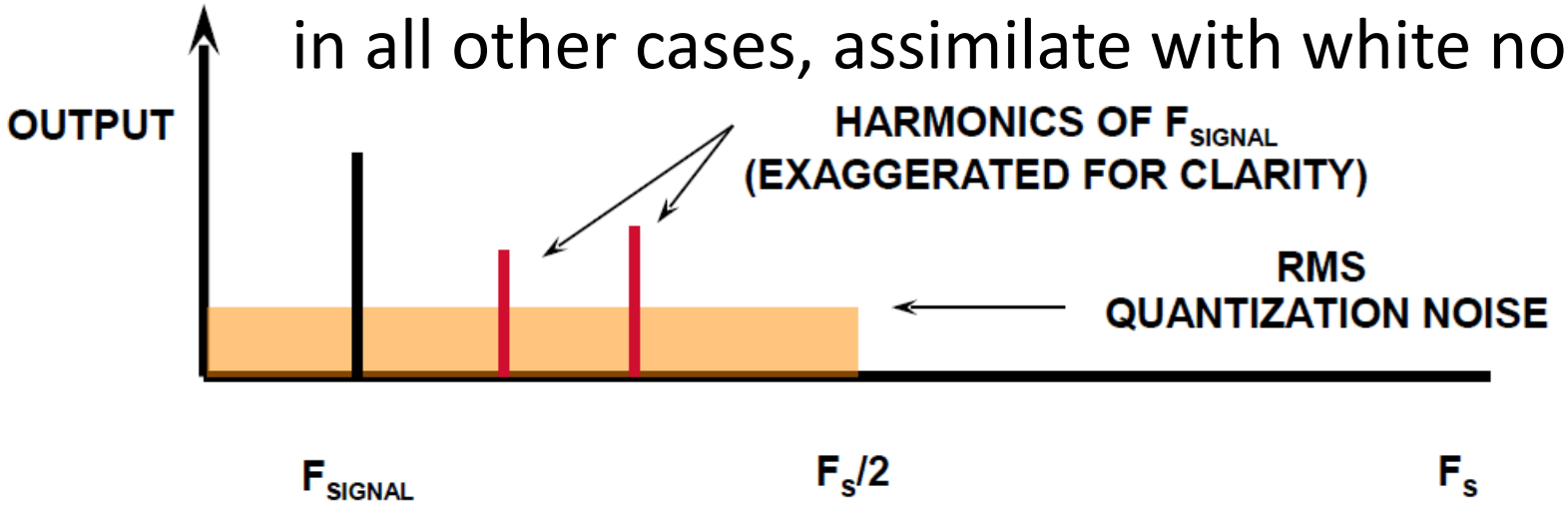


Amplitude quantization error

- Quantization error is assumed to be white noise : folded in the base band, the noise level is (1.76 + N*6.02)*dB* below the full-scale SINUS power level.

  => quantization is distortion!

  (of synchronously sampled, periodic signals, in all other cases, assimilate with white noise)



Real Transfer Function

- Ideality don't exist in physics !

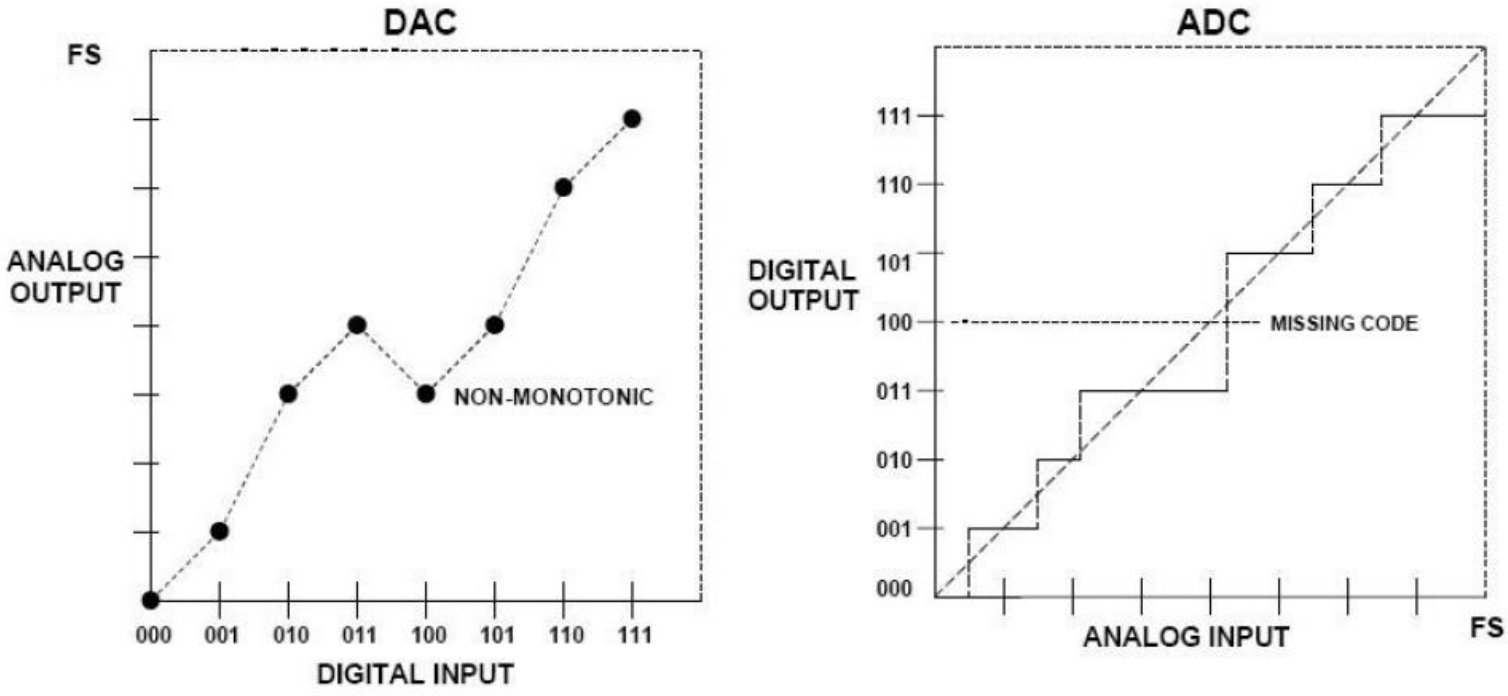


Figure 2.19: *Transfer Functions for Non-Ideal 3-Bit DAC and ADC*

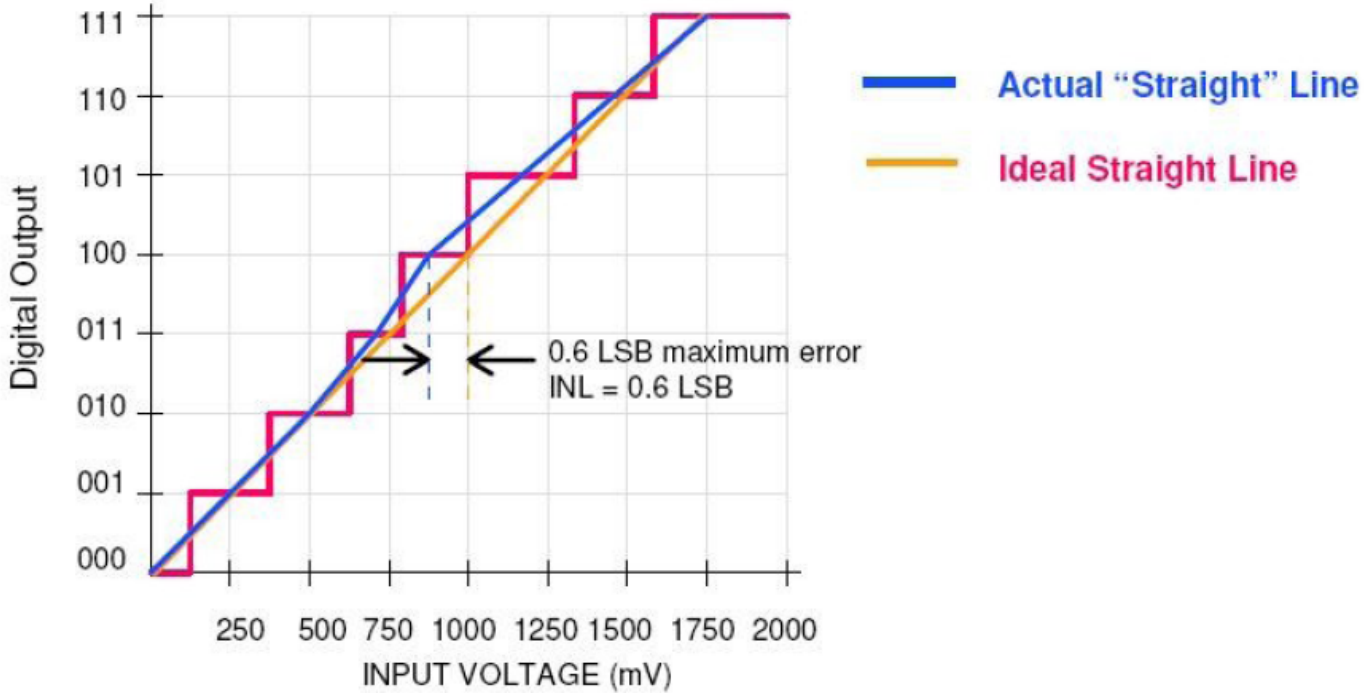
Def. : INL

- Integral Non-Linearity : a mesure of the distance of the current Transfer line Function to the ideal TF
  - A static parameter
  - Mesure on the analog side!
  - Unity : in #LSB or in %FS

DC ACCURACY					S, B versions, V_{DD} = (2.35 V to 3.6 V)[4]; A version, V_{DD} = (2.7 V to 3.6 V)
Resolution	12	12	12	Bits	
Integral Nonlinearity[3]		±1.5	±1.5	LSB max	
	±1	±0.6	±0.6	LSB typ	
Differential Nonlinearity[3]		−0.9/+1.5	−0.9/+1.5	LSB max	Guaranteed no missed codes to 12 bits
	±0.75	±0.75	±0.75	LSB typ	
Offset Error[3]		±1.5	±2	LSB max	
	±0.5			LSB typ	
Gain Error[3]		±1.5	±2	LSB max	
	±0.5			LSB typ	

INL

- INL values are « lower » as we choose a best fitting line !
  - Zero-based line
  - Best fitting line



INL

- INL is the measure of the overall linearity (also called « precision »)
  - INL's profile is significative of the internal structure of the converter.
- INL isn't allways needed! (feedback loop systems)
-

INL example

- AD 7687, Analog Devices

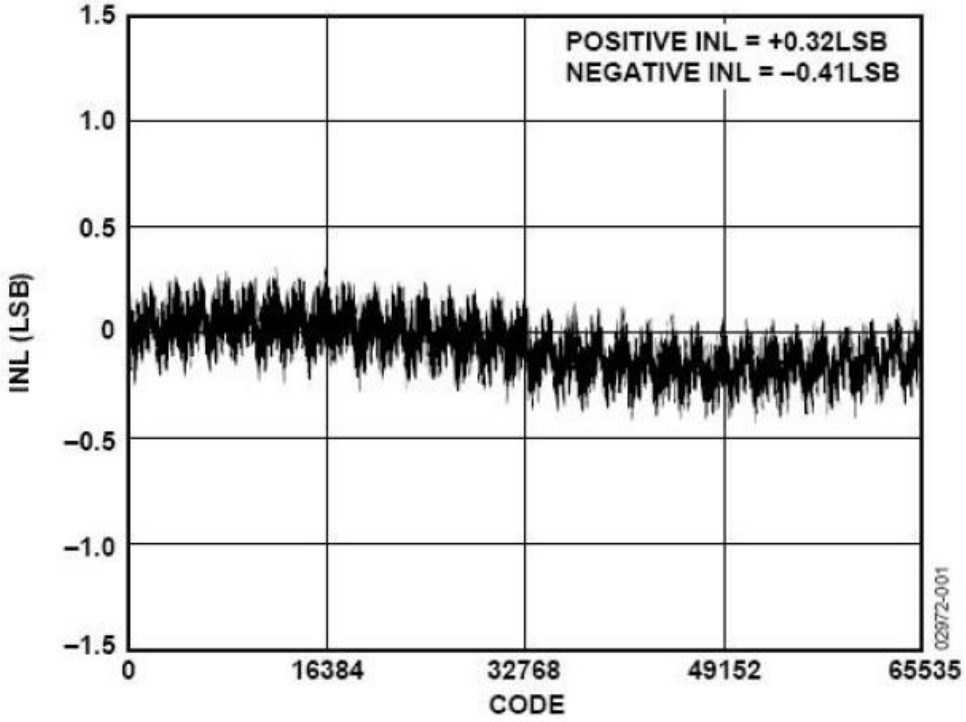


Figure 1. Integral Nonlinearity vs. Code

Def. : DNL

- Differential Non-Linearity : difference of each current step value of the TF from the ideal one
  - Measure on the analog side
  - Unity : in #LSB or in %FS

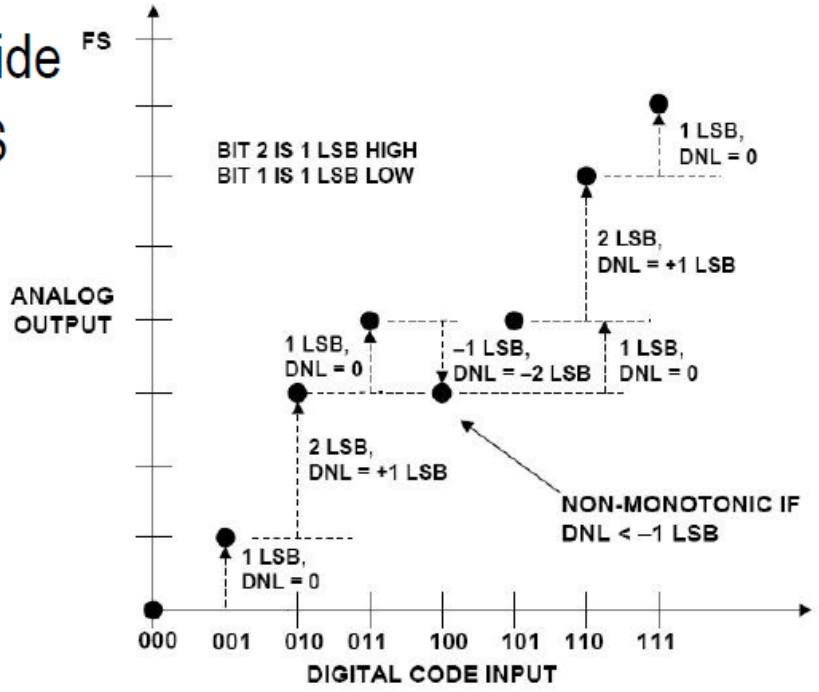
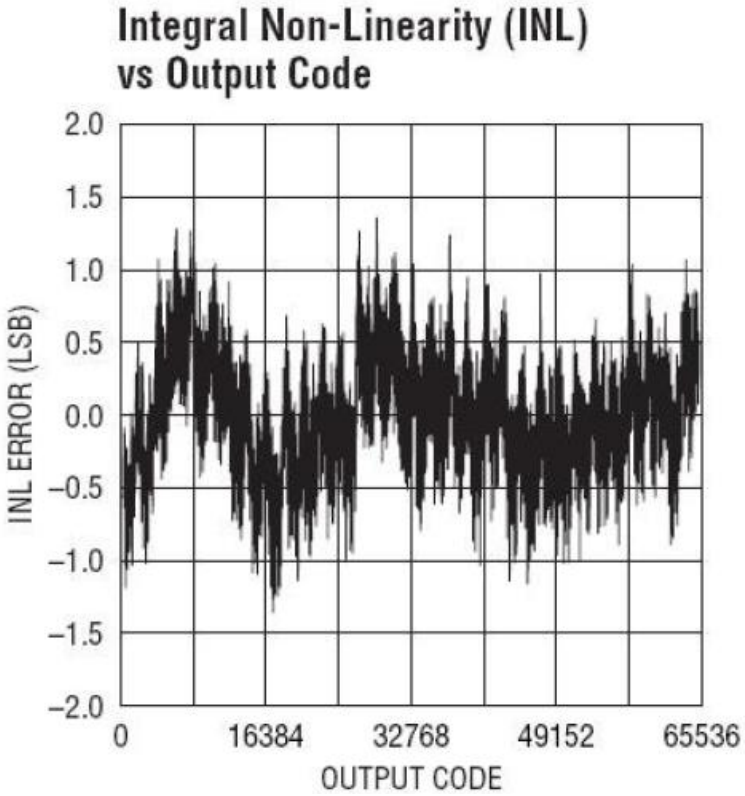


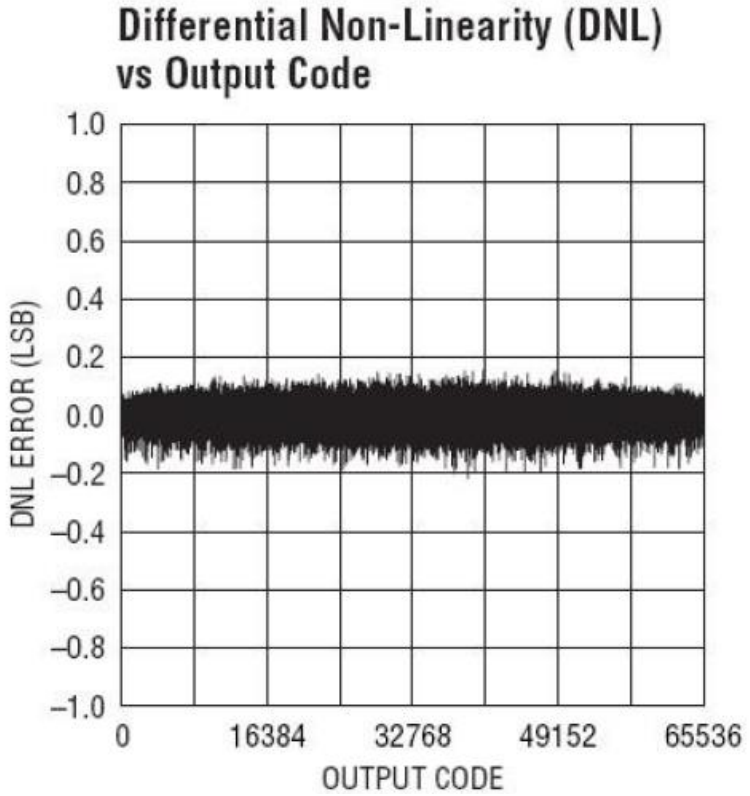
***Figure 2.20**: Details of DAC Differential Nonlinearity*

DNL

- DNL > -1 : non-monotonic
- DNL > +1 : missing code
- DNL is important for :
  - Closed loop systems
  - When small variations most significatives than big DC steps (video, graphics, sensors ...)

DNL example


Integral Non-Linearity (INL)
vs Output Code
INL ERROR (LSB)
2.0
1.5
1.0
0.5
0.0
–0.5
–1.0
–1.5
–2.0
0
16384
32768
49152
65536
OUTPUT CODE

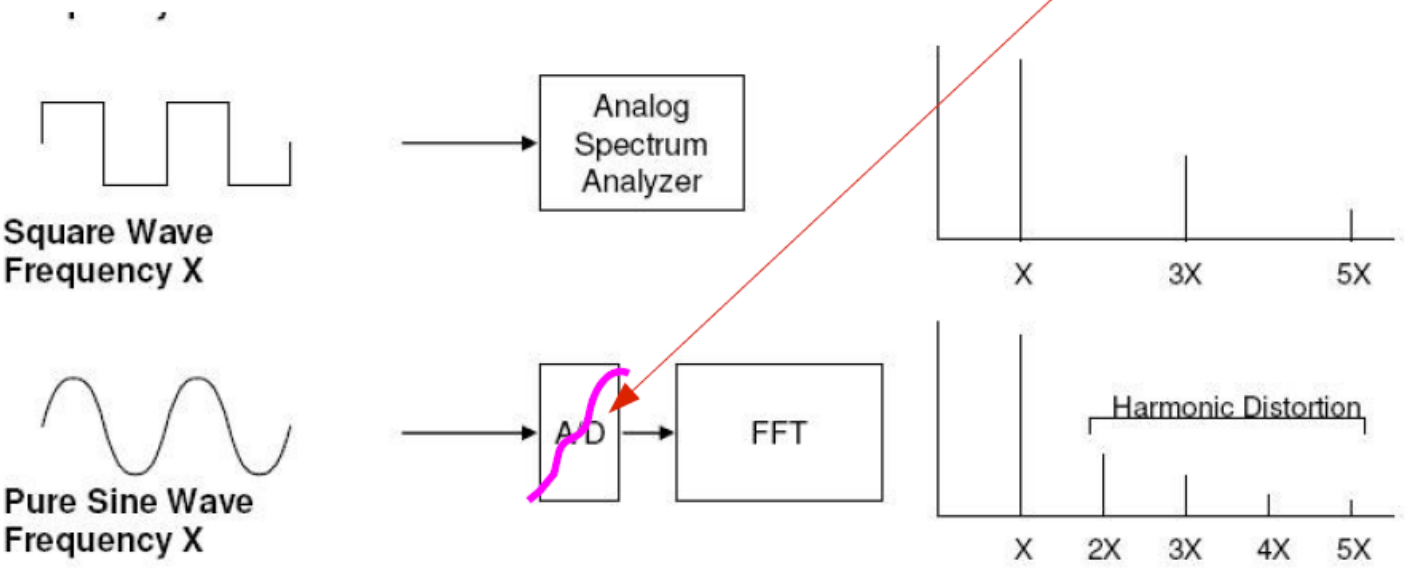

Differential Non-Linearity (DNL)
vs Output Code
DNL ERROR (LSB)
1.0
0.8
0.6
0.4
0.2
0.0
–0.2
–0.4
–0.6
–0.8
–1.0
0
16384
32768
49152
65536
OUTPUT CODE

Def. : SNR

- SNR : Signal over Noise POWER Ratio
- SNR is one of the expression of the fundamental limitation of the converter
  - => the *SNR of the input signal* is the most useful specification for the choice of the converter's resolution
- Unit : $$SNR_{dB} = 10 \cdot \log\left(\frac{\text{signal Power } P_S}{\text{noise Power } P_N}\right)$$
- Or $$SNR_{dB} = 20 \cdot \log\left(\frac{\text{signal RMS Voltage } U_S}{\text{noise RMS Voltage } U_N}\right)$$

Harmonic distortion

- 2nd order and 3rd order TF leads to distortion :
  - Pair and unpair harmonics are growing!
  - Distortion is a « dynamic » parameter but comes from the non-linearity of the TF



Total Harmonic Distortion THD

- THD is the ratio of 2 RMS values :
  - RMS value of the fundamental sinus
  - RMS value of a given number of harmonics

$$THD = \sqrt{\frac{\sum U_{h2}^2 + U_{h3}^2 + \cdots + U_{hn}^2}{U_{sin}^2}}$$

Signal-to-Noise And Distortion SINAD

⌘ Distance between a sinus @FS amplitude and (noise + distortion) power is called SINAD

$$SINAD = 10 \log \frac{A_{SinFS}^2}{\sum \text{(noise + distortion) power to fs/2}}$$

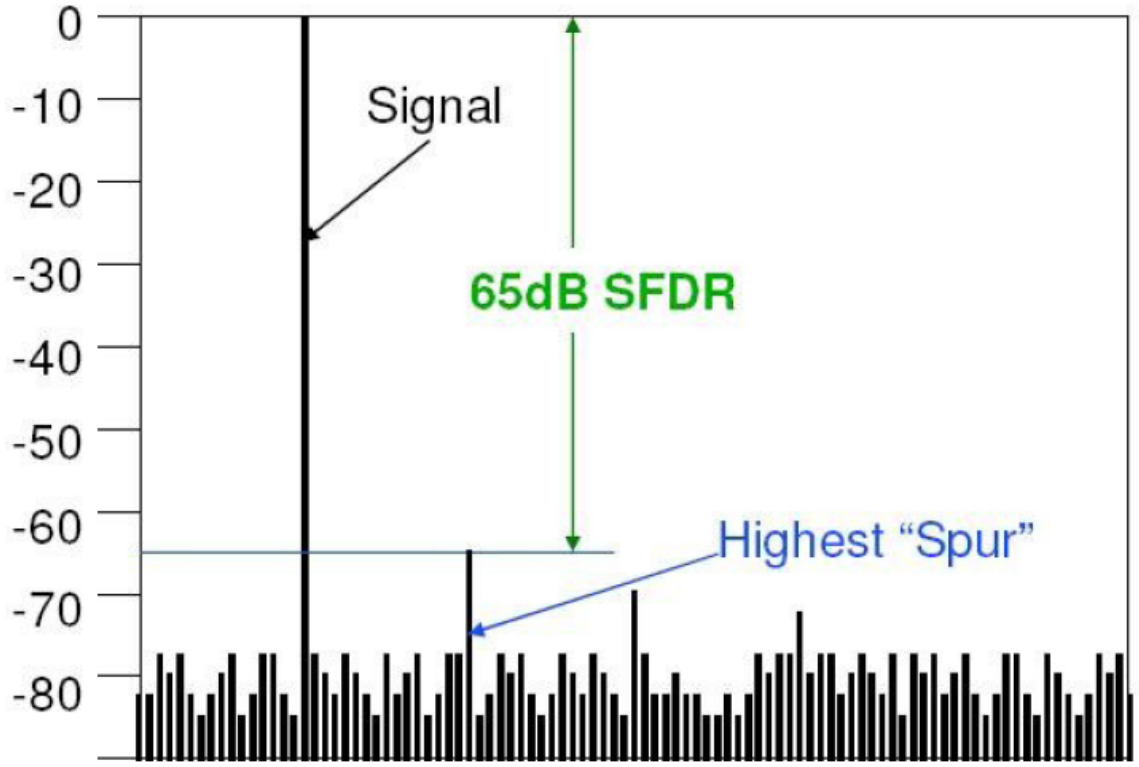
Effective Number Of Bits ENOB

$$ENOB = \frac{SINAD_{dB} - 1.76}{6.02}$$

- ENOB says that the ADC is equivalent to this number of bits as far as SINAD is concerned
  - That is, a converter with an ENOB of 7.0 has the same SINAD as a theoretically perfect 7-bit converter.

Spurious Free Dynamic Range SFDR

⌘ « Distance » to the highest distortion line



Data sheet analysis

Have a look at the following datasheets,

- DAC8411, MAX542
- AD7687, ADS5463

and determine the key performance characteristics: range, resolution, INL, DNL, SNR, THD, SINAD, ENOB, SFDR.

Exercice

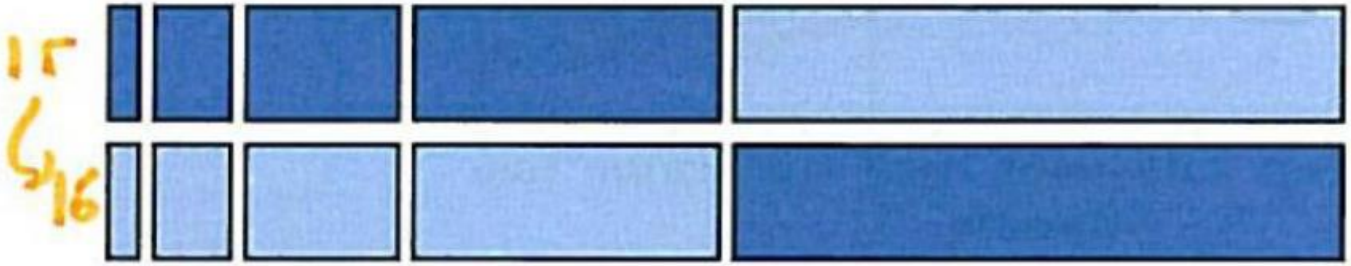
DAC Structures

- Unary and binary types

Unary: serie of 2^N times 2^0 (LSB) values

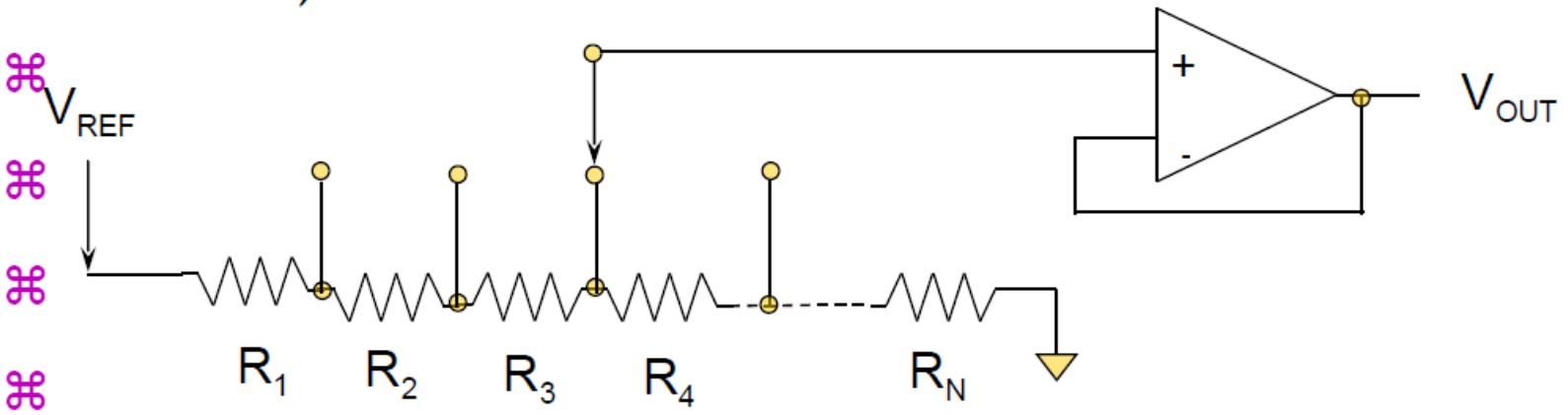
Next value always more: monotonicity guaranteed.

Binary: N different values: $2^0, 2^1, 2^2, 2^3, 2^4 \ldots 2^{N-1}$, small in area, MSB transition is critical:



Unary Structures

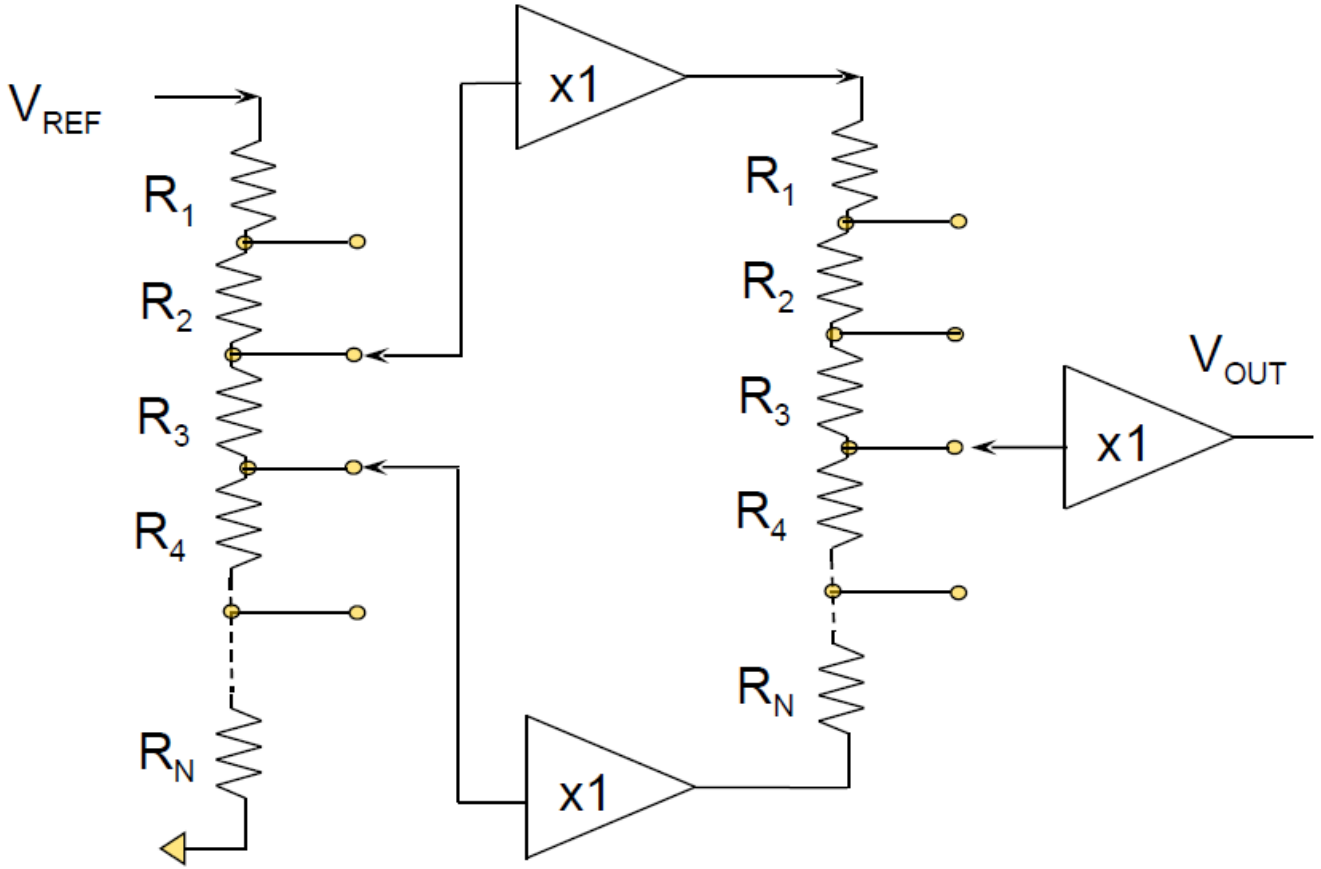
- Simple D-A using a resistor chain (Kelvin Divider)



  - Not practical for large N (2^N resistors!)
  - Output is monotonic garanteed

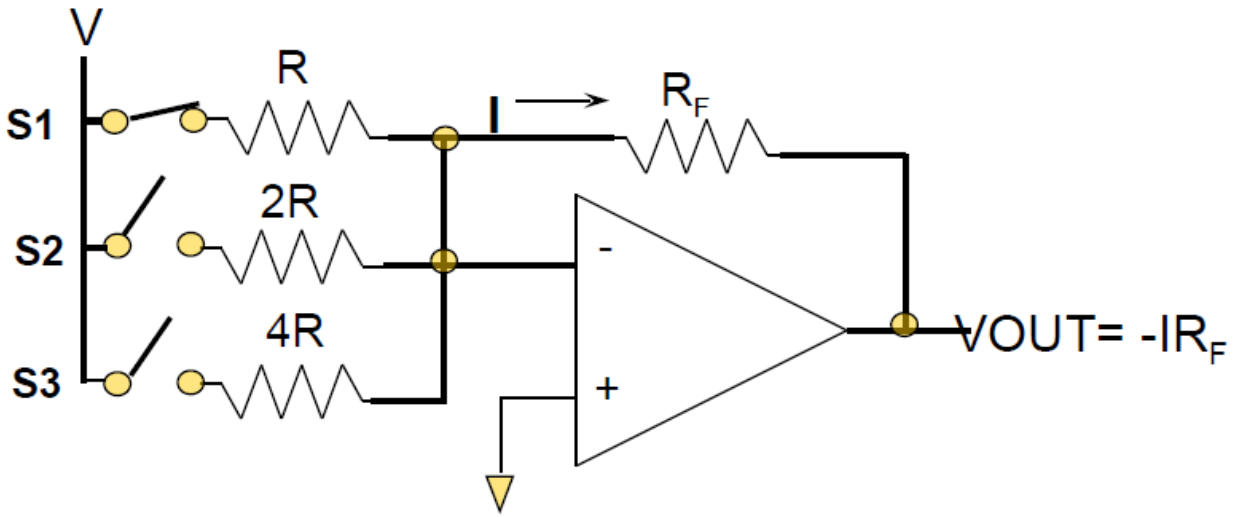
Unary Structures

- Segmented chains



Binary-weighted Structure

- A simple low-N U-DAC



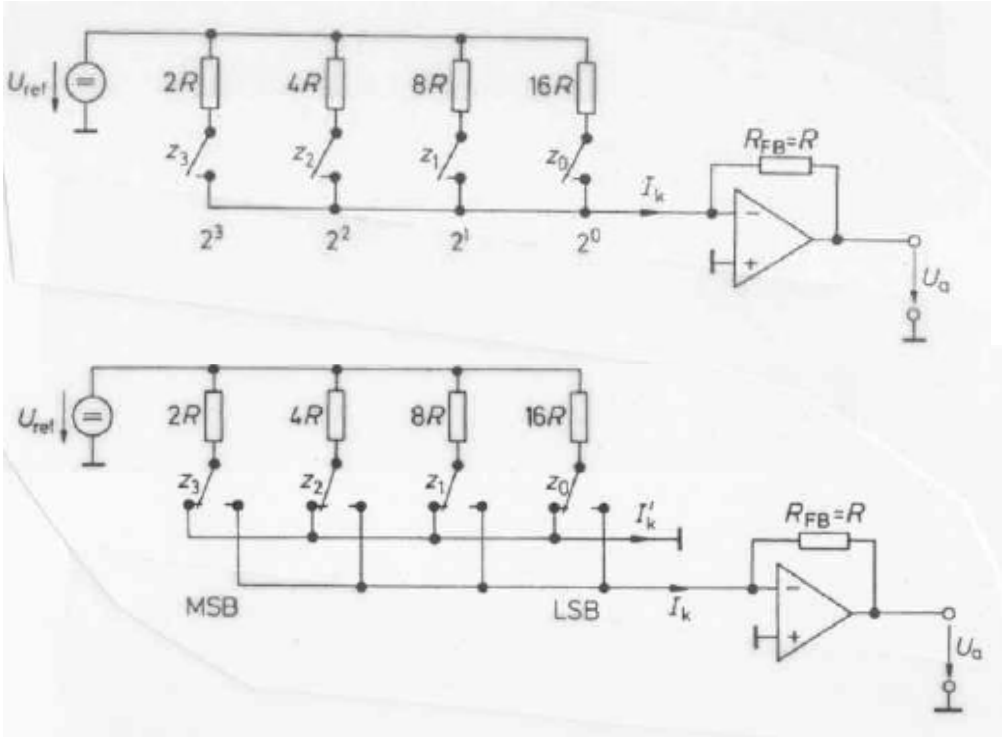
  - Matching of the current sources?

Binary weighted structure

The two schematics below show binary weigthed structures for DA conversion. The principal inconvenients of the upper structure are

- The load of Uref is not constant, but depends on z.
- The parasitic capacitances of the switches are (dis)charged when switching.

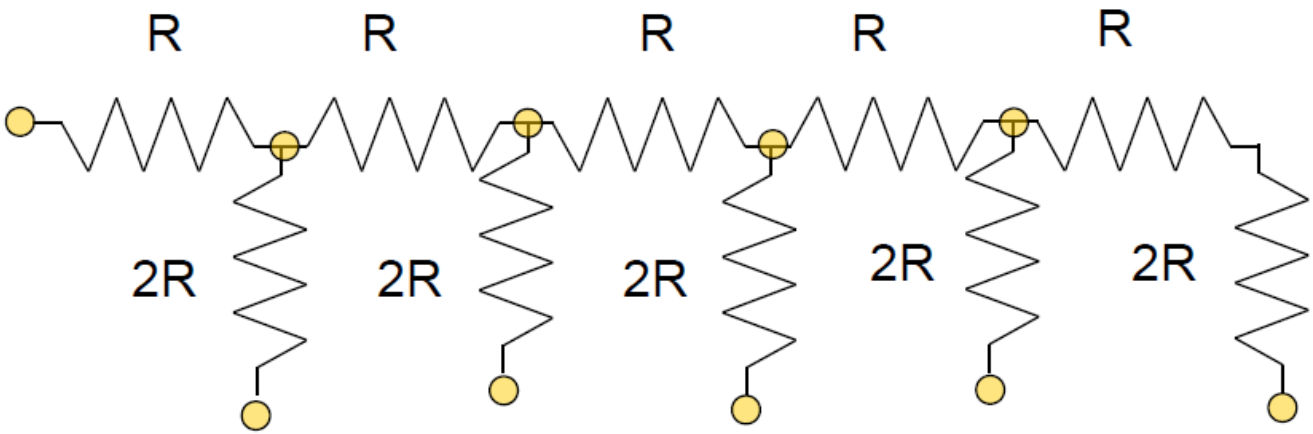
Explain why the lower schematic solves these problems.



Exercice

Binary-weighted Structure

- A simple low-N U-DAC



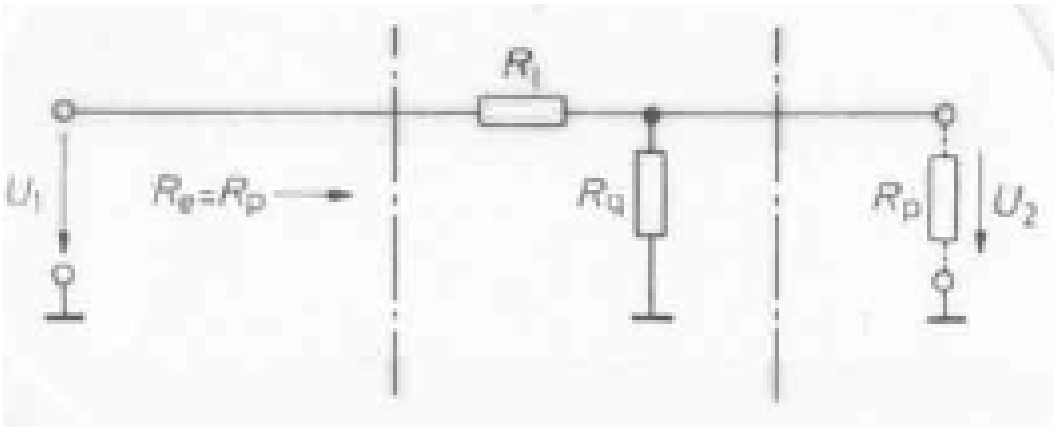
  - Matching easier! (only R &2R values)
  - Absolute Value Not Important (typ. 10-20k, +/- 20%)

Generalized ladder network

Draw a schematic of a voltage output 4bit-DAC with an R/2R ladder network, using commutators between two output current rails.

With the help of the circuit shown below, express R_l and R_p as functions of R_q, so that

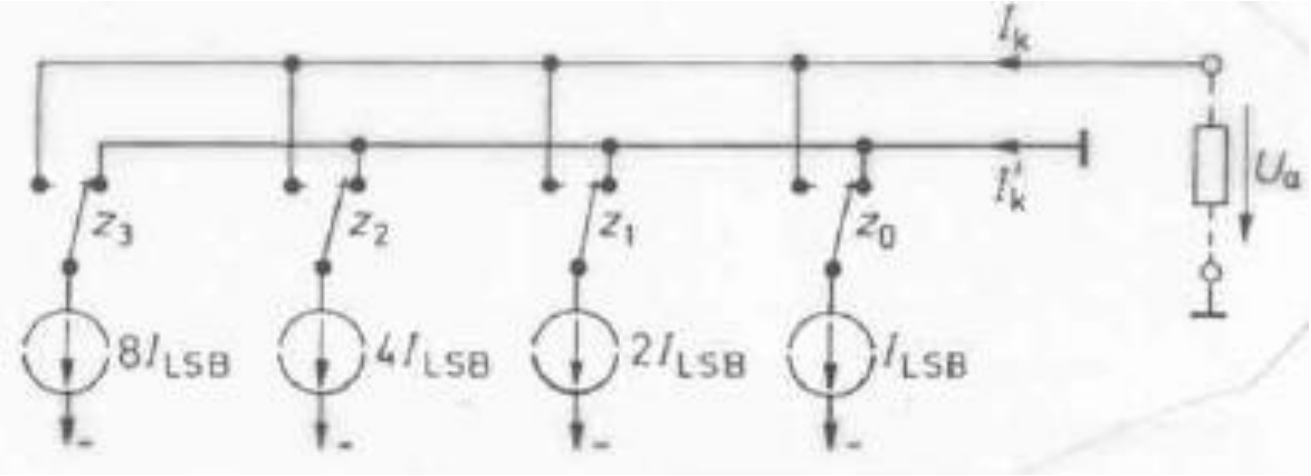
$$U_2/U_1 = \alpha$$



Exercice

Arrays of current sources

Instead of a reference voltage and a set of weighted resistors, a set of weighted current sources can be used for DA converion as shown below.

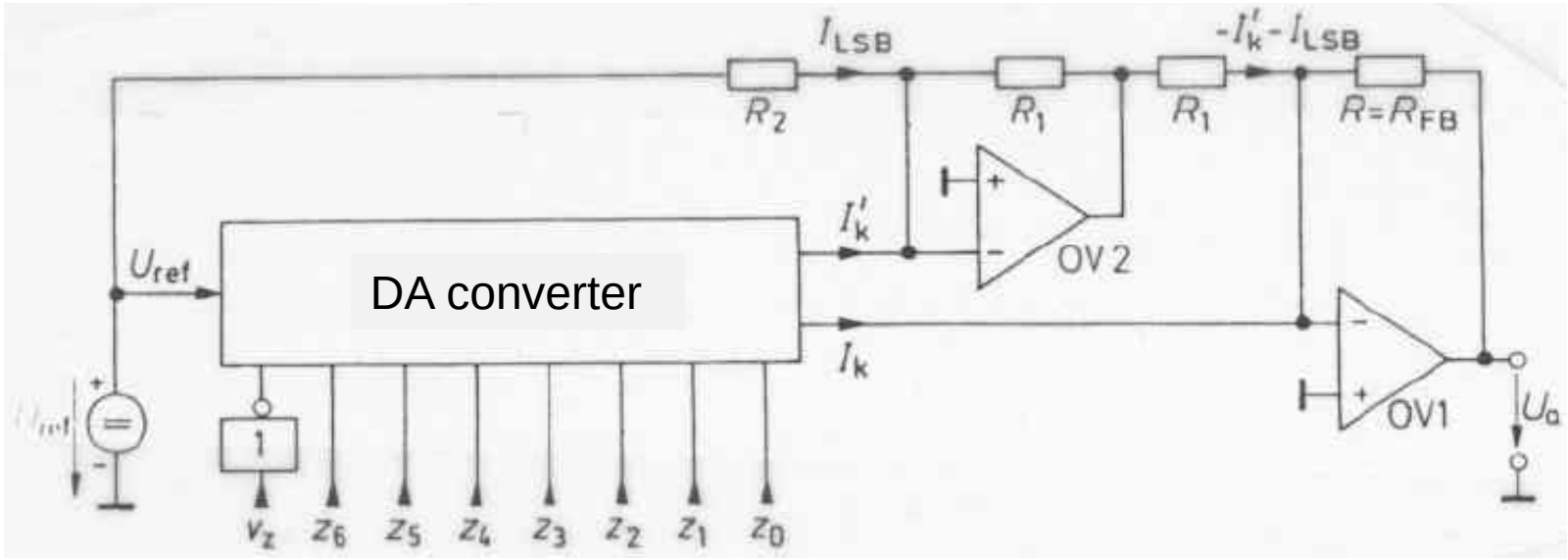


Propose an alternative circuit using a set of current sources of same value and a ladder network for DA conversion.

Exercice

Bipolar output

For the circuit shown below, determine U_a as a function of Z, a signed binary number in 2's complement representation. I_k and I_k' are the two complementary current outputs of the DA converter.

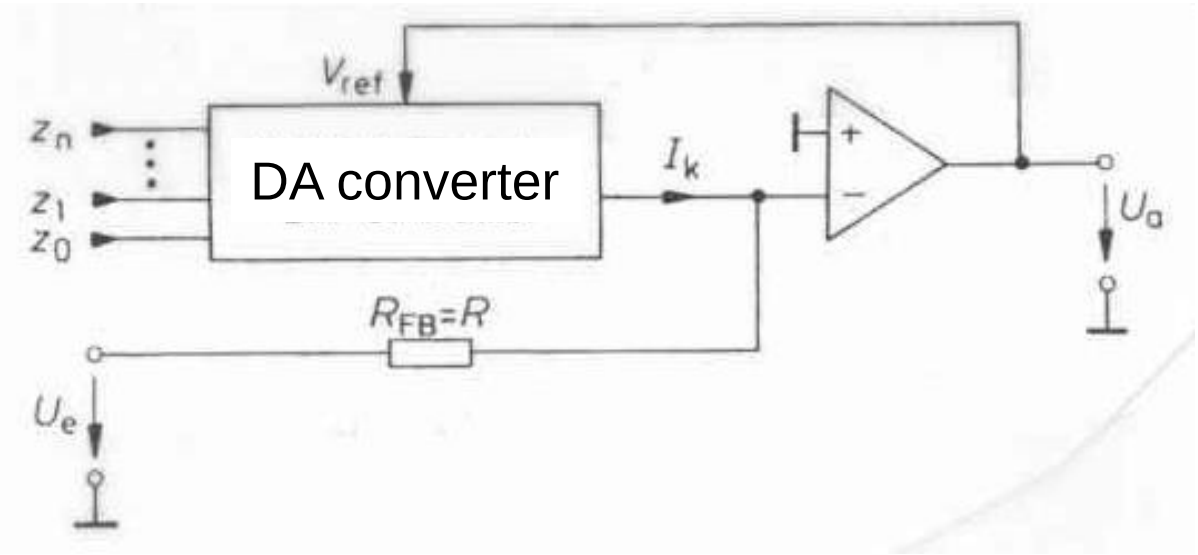


What is the range of U_a?

Exercice

Multiplication / division

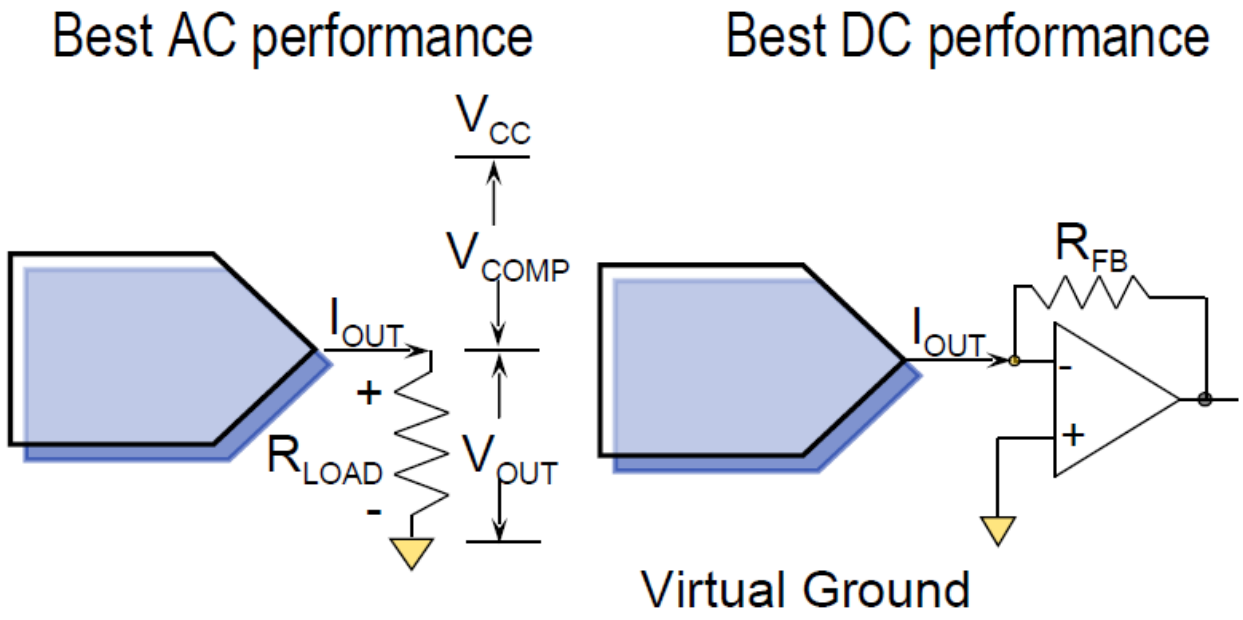
Show that in the circuit below, the output voltage U_a is proportional to U_e/Z.



Exercice

U-I output

- Use Voltage-output DAC for DC applications, Current-output for AC



DAC Summary

- Unary (Resistor String)
  - Inherent Monotonicity
  - Compact Design Leading to the basis of Multi-Channel DACs
  - Difficult to get High performance INL
- Binary (R-2R Ladder)
  - Good DC performance
  - Suffer from distributed R-C effects and signal-dependant loading in frequency-domain applications
  - Multiplying Capability
  - Can Operate in Voltage Mode for Single Supply Applications

DAC Summary

- Bipolar Switched Current
  - Suffers AC limitations because R-2R is typically required to create LSB currents
- CMOS Switched Current
  - Best Choice for frequency-domain applications:
  - No R-2R to limit AC performance
  - Good matching for DC specifications (calibration sometimes needed)
  - Allows for integration with discrete signal processing blocks to ease implementation and improve performance

References

W. Kester (ed.): *Analog-Digital Conversion*, Analog Devices 2004, ISBN 0-916550-27-3

This reference was used as a basis for the present presentation, a series of illustrations are taken from it.

The book is available for download on the moodle server.

Tietze, Schenk: *Halbleiter-Schaltungstechnik*, Springer 1999 (11th ed.), ISBN 3-540-64192-0