MSE | MASTER OF SCIENCE IN ENGINEERING

TTHF LAB

ADVANCED ELECTRONIC DESIGN

EMC, signal integrity, grounding and power supply routing, decoupling, transmission lines, simulation tools

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Topics of this series of 3 lessons

PCB Design

- Lesson 1:
  - Introduction
  - Partitioning, filtering
  - Shielding
  - Image planes
  - Continuous vs split GND concepts
  - Mixed signal circuits
- Lesson 2:
  - Decoupling
  - Transmission lines
  - Guard rings
  - Crosstalk, Ground bounce
  - Differential signaling
  - Terminations
  - Clock distribution: clock skew and clock jitter
- Lesson 3:
  - Place & route strategy
  - Components selection
  - Layer stackups
  - Multicard systems, backplanes
  - Enclosures, connectors and cables
  - ESD + Burst protection
  - 2-layer PCBs
  - Design for testability
  - Prototyping

Components placement and trace routing

General guidelines (summary) (1)

Execute the design of a PCB in the following order and make sure to:

1. place the I/O connectors at the periphery of the board and partition them according to their function
2. place oscillators and fast circuits at the center of the PCB, far from connectors and I/Os.
3. place power circuits near the power supply/voltage regulators
4. partition and place the remaining components carefully (according to the connector's position). Place components so that critical signal traces can be kept short.
5. reserve room for mounting holes for GND stitches (screws)
6. route the power supplies (reference planes) and decoupling capacitors
7. route critical signals: fast clocks and signals, high speed interfaces (Ethernet, USB) and their termination networks. Consider using stripline technology for them.
8. route analog signals
9. route the remaining digital signals *)

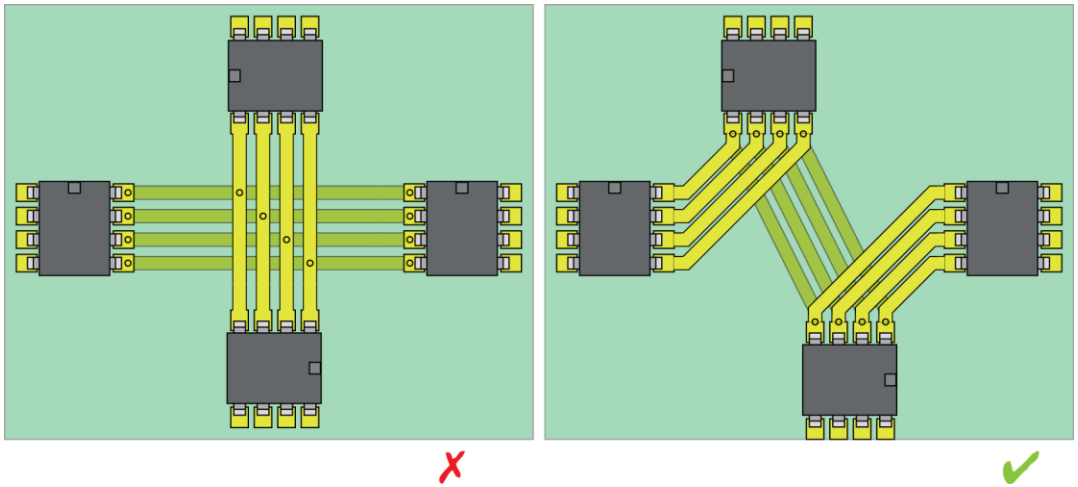
*) use the autorouter only here, but double check its result!

Components placement and trace routing

General guidelines (summary) (2)

More on routing…

- avoid:
  - stubs,
  - T-junctions.
  - grid routing



- route all critical nets on a single layer that is adjacent to a GND layer (avoid vias)
- verify that fast signals have a good return path (immediately under the trace)
- do not route over interruptions of the reference plane
- avoid sharp corners in the PCB traces, as they cause signal reflections
- do not place vias between differential pairs

Components selection

Keep signal integrity and EMC problems small with:

- use no faster logic family than that dictated by your design requirements *)
  The same also applies to power switching components (MOSFETs, IGBTs)
- be careful when selecting second source components
- choose components with the smallest possible enclosure (chip capacitors and ICs with the smallest available SMD footprint)
- choose ICs with a "good" pinout (e.g. a GND pin available next to the crystal oscillator pins, a sufficient number of GND and VCC pins, placed closely, etc)
- when choosing decoupling capacitors, check their series resonance frequency

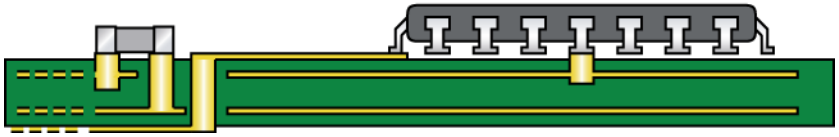
*) When a slower logic IC is not available, you should consider:

- using ICs with controlled slope outputs and/or reduced output swing
- slowing the output transitions through RC (or ferrite bead + C) filters

PCB technology

Microvias (high density interconnect, HDI)

- the name refers to vias having a diameter of < 0.15 mm and that do not go through all of the layers



- PCBs with microvias have a higher cost, but also have important advantages:
  - allows "via-in-pad", which reduces decoupling inductances
  - allows a more efficient routing and often helps reduce the number of layers
  - often allows shorter trace lengths and therefore reduces transmission line effects
  - reference planes are less perforated and have a lower impedance, provide a better signal return path and have a better shielding effect
  - shorter vias do not radiate beyond the layers of interest and do not act as open stubs

PCB technology

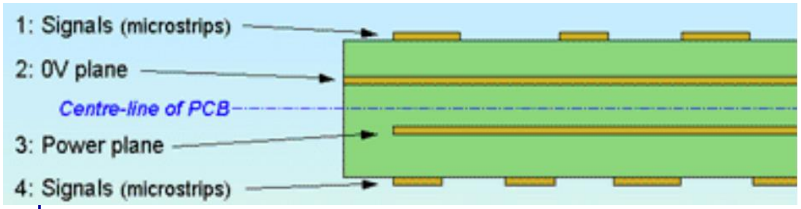
Layer stack-up

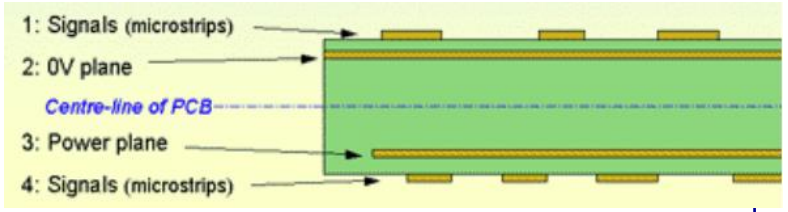
- an old rule of thumb (the "5/5 rule") states: if the signals in a circuit have frequency contents >5MHz or rise/fall times <5ns, then a multilayer PCB should be used

- the optimal multilayer stack-up should fulfill the following requirements:
  - GND and VCC layers should be near, for maximum capacity (decoupling)
  - image planes (GND, VCC) should be adjacent and near to the outer layers for best signal integrity
  - a GND plane is the preferred image plane near the component side and near a signal layer with fast signals
  - long high speed traces should be routed on layers located inside the image planes for best shielding (stripline). Signal traces on the external layers should be kept short.

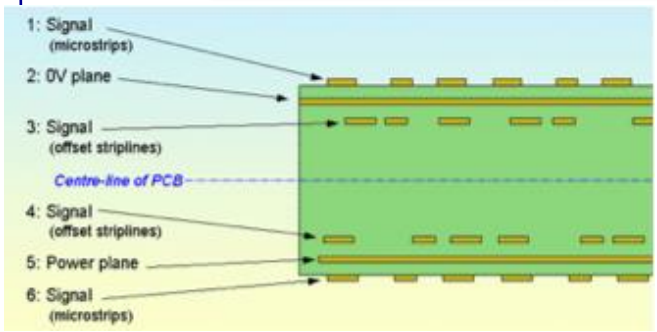
PCB technology

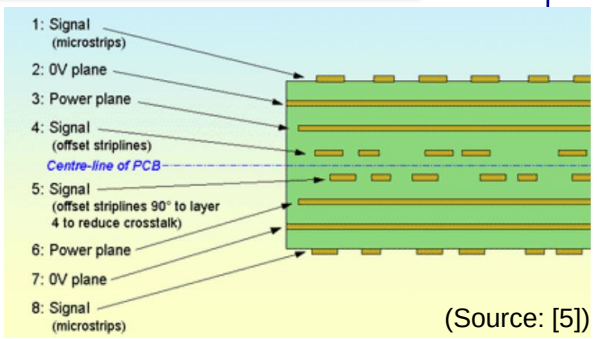
Layer stackups compared





maximum GND-VCC capacitance	image planes *near* signal layers	GND layer near component side	internal signal layers in stripline
		(✓)	
	✓	✓	
	✓	✓	✓
✓	✓	✓	✓





(Source: [5])

Quiz time

1. **Explain some criteria when choosing a logic family (speed, output voltage swing, etc)**

   Answer:

   Lowest possible speed, lower possible output voltage swing (e.g. 2.5V logic), small case, optimal pinout with many GND pins.

   All these criteria have an impact on the switching noise and associated problems (emissions, crosstalk, reflections, etc.)

1. **When specifying a multilayer PCB stackup**

   - ☐ always keep the same distance between all layers
   - ☐ VCC and GND should always be the outer most (top+bottom) layers
   - ☑ it depends

1. **Describe in what sequence you execute the various steps involved in the design of a PCB**

   Answer:

   See slides 2 + 3

Multicard systems and connectors

..involve passing signals through connectors and backplanes

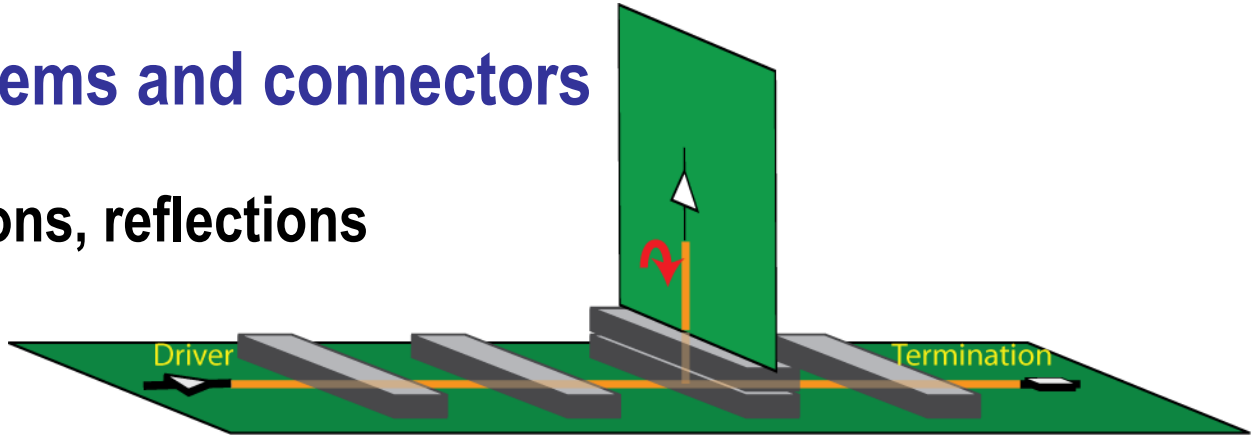
- rule #1: for best signal integrity and EMC performance, always try to fit your system within one single PCB!

- Problems:
  - transmission line impedance control
  - crosstalk
  - signal reflections (terminations, stubs)
  - clock and signal skew

- fast serial buses are today's preferred solution over parallel buses for signals leaving a PCB:
  - less wires, crosstalk. Easier signal routing.
  - accurate impedance control of a few (often differential) serial lines is easier to accomplish
  - reduced cost (connectors, PCB real estate)

Multicard systems and connectors

Signal terminations, reflections



- capacitively loaded stubs on daughter cards should be kept short, as they cause reflections
- backplane transmission line loading depends on the number of inserted daughter cards and their input impedance. This modifies the characteristic impedance Z_0 of the line. It can become difficult to find a termination concept that accommodates all possible situations. A tradeoff must be taken.
- Z_0 should be kept constant over the entire length of the backplane signal traces
- if the communication is bidirectional, the lines must be terminated at both ends
- apply design recommendations provided by the bus standards (PCI, VME, etc)

Multicard systems and connectors

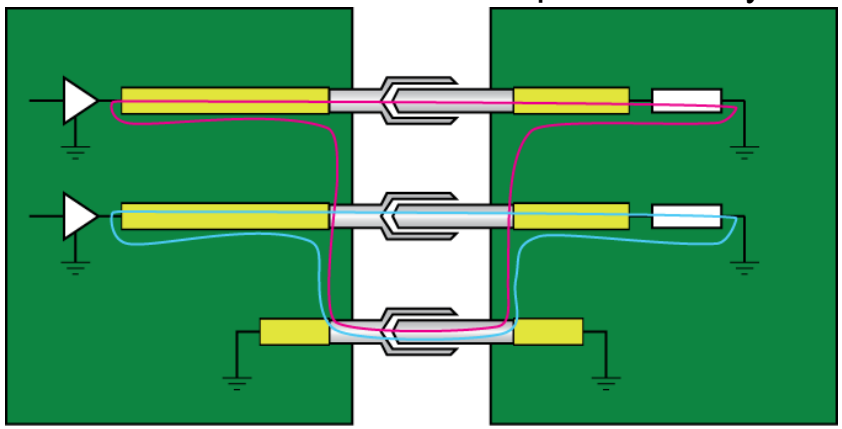
Signal routing and layout considerations

- prevent crosstalk on the backplane by using multilayer boards with reference (GND) planes between any two signal layers. Keep adequate distance between traces on the same layer
- route critical signals against a GND (not VCC) layer
- consider using stripline technology for fast signals on the backplane
- use impedance controlled connectors. Use as many GND pins as possible with the allocated connector size and pin number (minimum: one for each signal pin)
- RF coupling between nearby daughter cards can be a problem. (mount a grounded metal plate between the cards *or* design the cards so to have bottom layer = GND)
- since the backplane's GND layer and the connectors have non zero impedance, crosstalk and ground bounce problems could arise. Reduce GND impedance on the backplane and provide sufficient GND pins in the connectors
- keep logic transitions as slow as possible
- avoid layer changes (vias) with the signals on the backplane
- beware of card connectors whose THT pads (and antipads) completely interrupt the reference planes (SMD connectors are better from this point of view)

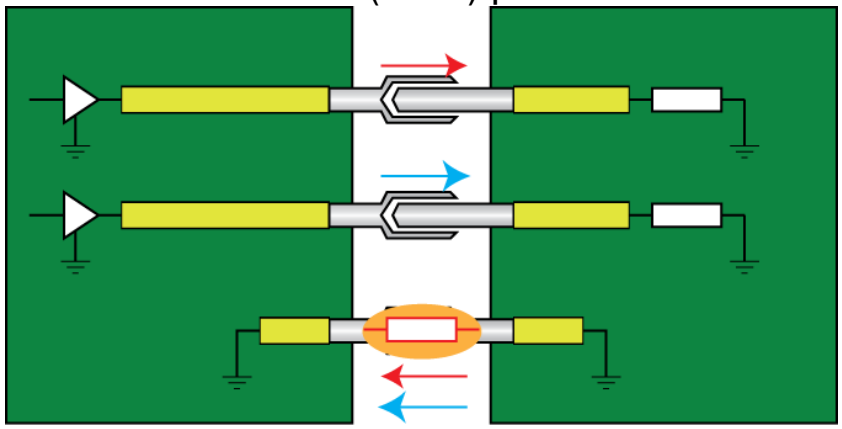
Multicard systems and connectors

Crosstalk at the connector level

- inductive (M, mutual inductance between current loops formed by different signals)
  - $u_1 = M_{12} \cdot \frac{di_2}{dt}$



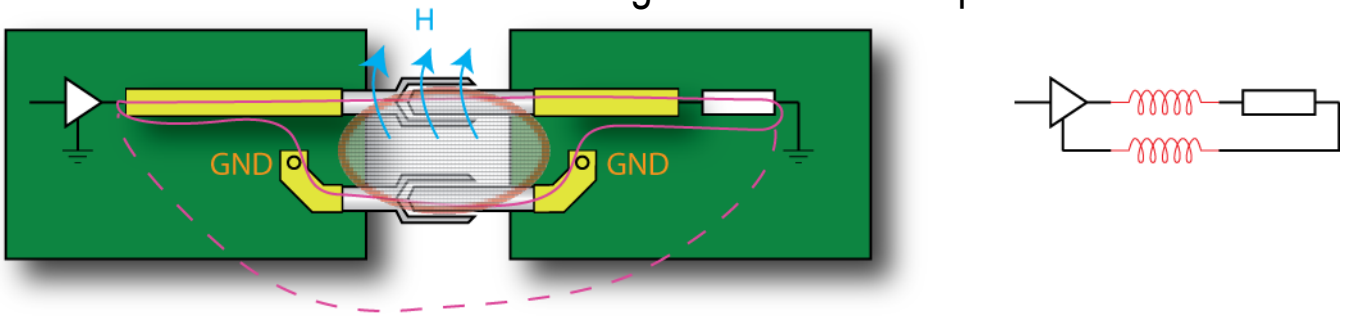
  Workarounds:
  - reduce M
  - reduce di/dt
- due to series impedance on *shared* return (GND) pins



Multicard systems and connectors

Avoid false current return paths

- whenever the connector has a series R or L, the signal will try to find alternate return paths
- the increased distance between a signal and its return path in the connector generates:
  - increased current loop area => noise emissions!
  - increased series inductance (in the connector)
- try to minimize the distance between the signal and its return pin

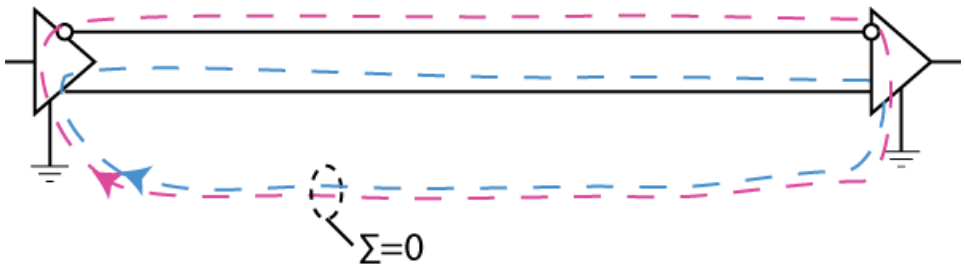


- alternate return currents cause EMI problems
- due to the higher connection series impedance in daughter cards, attaching I/O cables to daughter cards should be avoided (risk of alternate return paths from cables, emissions)
- if two cards are connected with multiple connectors, keep them close together

Multicard systems and connectors

Differential signaling through connectors

- here we see again an advantage of the differential signaling:
  if the currents on the two wires of a differential pair are exactly balanced (Σcurrent = 0), then there can not exist any return current over false (parasitic) paths regardless of the connector impedance



- for this to work, we must design the line driver, receiver and the termination network in order to guarantee that Σcurrent = 0, always.

Quiz time

4. You need to connect a uP on a PCB to a very fast data acquisition system (ADC) located on another PCB. How would you connect the two circuits for best performance (speed and EMC) ?
Explain your choice.
(in all cases, the signals are passed through a backplane connection):

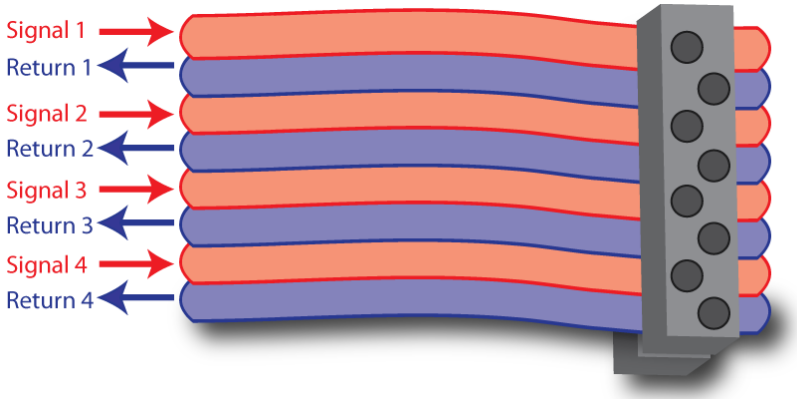
- ☐ connect the ADC directly to the uP's fast local (parallel) bus
- ☑ use a high speed serial differential channel (LVDS)
- ☐ use a parallel bus with optocoupler isolation

Reason:
Passing fast signals over a backplane is always a headache. The best we can do is to reduce their number (i.e. using serial instead of parallel bus) and use a technology that is optimized for this purpose and allows easy impedance matching (termination). LVDS is such a technology, that uses differential signaling with very small voltage swing. At the same time, it is very fast, allowing it to achieve the same throughput as normal parallel busses.

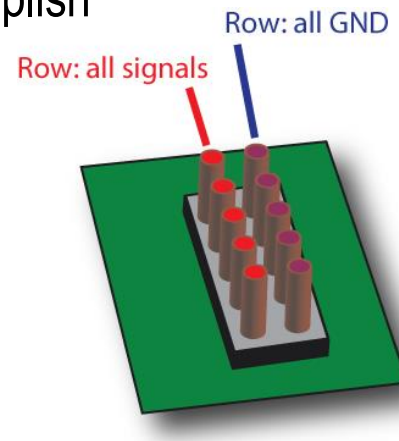
Cables and cabinets

Ribbon (flat) cables

- Advantages:
  - controlled distance (→ impedance) between conductors.
  - good transmission line (over short distances) when using 2 adjacent wires for signal and return
  - easy to assemble (connector mounting)
- For the signal integrity reasons just discussed, every signal wire should have nearby its own return wire:



- This is easy to accomplish on the PCB:

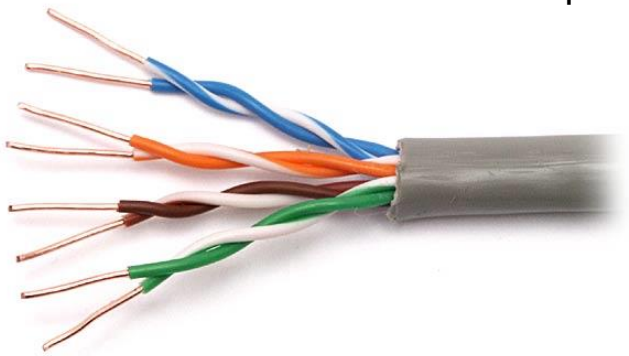


Cables and cabinets

Twisted cables

- Every signal line forms a twisted pair with its own return line
- Advantages:
  - better than flat cables over longer distances
  - reduced emissions and crosstalk: at each twist, the effect reverses resulting in ≈0 in average
- Available shielded or unshielded versions (e.g. STP, UTP Ethernet cables)

- Ethernet cable with twisted pairs:



- Ribbon cable with twisted pairs:

Cables and cabinets

Shielded (coaxial) cables

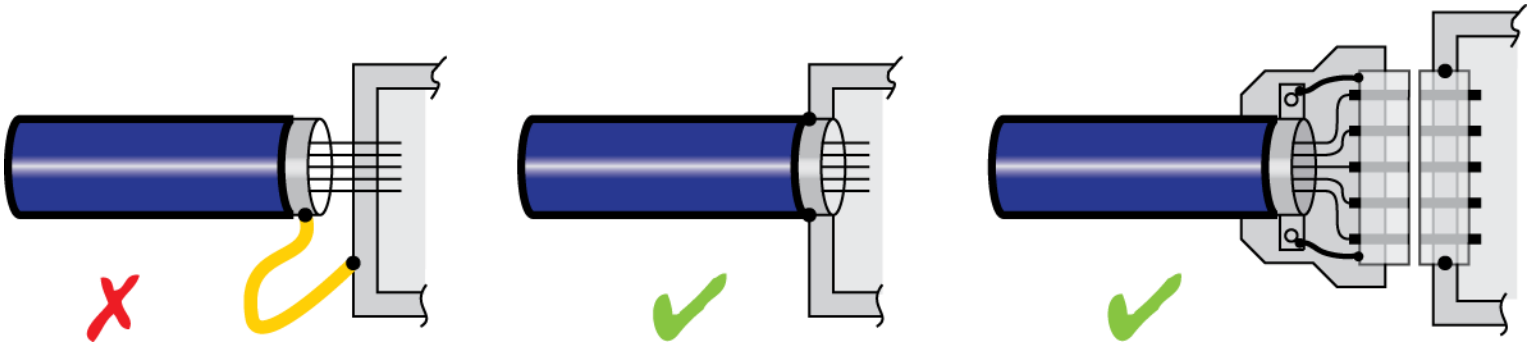
- The ultimate (but costly) solution for wired high speed data transmission
- Advantages:
  - Excellent transmission line impedance control
  - Availability of impedance matched coax connectors up to 26 GHz and more
  - Perfect shielding (no emissions, no crosstalk, no external noise pickup) when properly installed
- Improper connection of the shield can void (!!) the advantages of a shielded cable

Cables and cabinets

Shielded cables – important considerations

1. Connect the shield directly to the cabinet's chassis
2. Use the shortest possible connection for this. Don't use "pigtails"!

(list continues on next slide)



Cables and cabinets

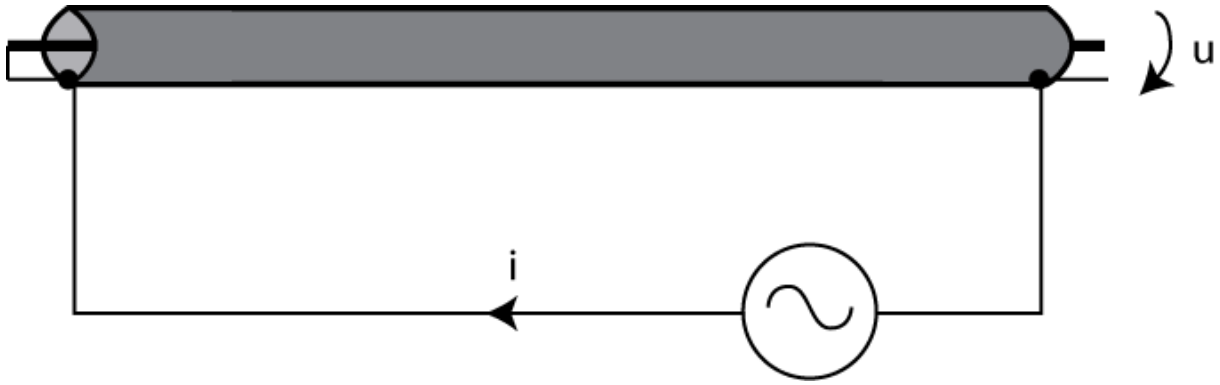
Shielded cables – important considerations *(cont'd)*

3. Connect the shield to the cabinet chassis (GND) at both ends of the cable.
   Some older LF / audio textbooks recommend connecting the shield at one end only. This may work on a laboratory testbench, but is not recommended at system level. Instead of splitting the shield connection at one end, do the following to reduce 50Hz noise ("hum") in audio/video equipment:
   - improve ground connections (reduce impedance), e.g. using meshed ground
   - apply rule #4 and/or galvanic isolation
   - reduce loop areas by deploying the cables near the metallic structures (cabinets, rails). Keep noisy cables distant from small signal cables.
4. Avoid using the shield as return wire: instead use 2 wires (signal+return) plus shield. Best results are achieved when using (balanced) differential signaling on these 2 wires (and driver+receivers are balanced as well, with good CMRR)

Cables and cabinets

Shielded (and coax) cables – definition of Transfer Impedance

- Definition:

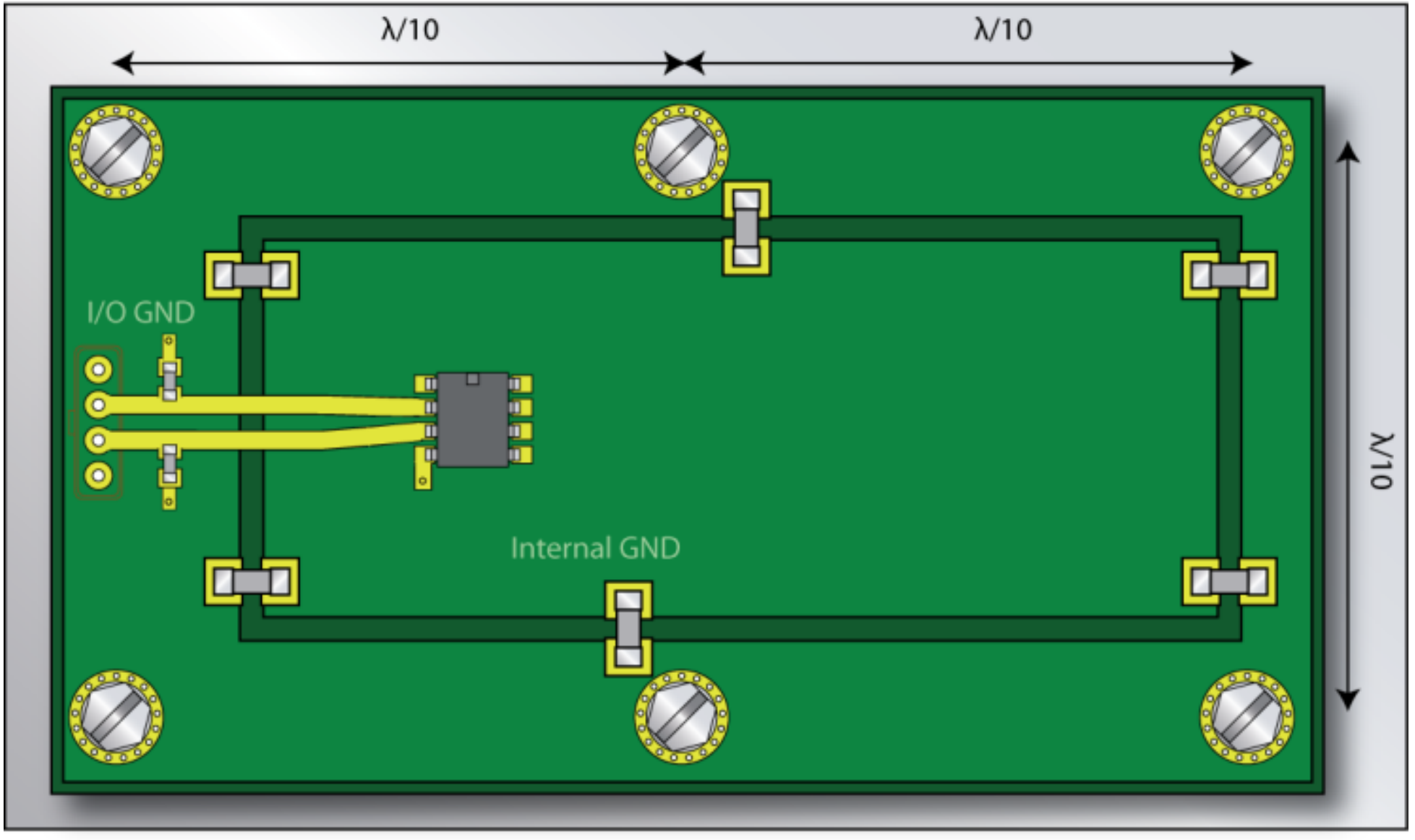


$$Z_{transfer} = \frac{u_{(measured)}}{i_{(applied)}} \qquad [\Omega, \text{per unit length}]$$

Cables and cabinets

EMI prevention measures on cables

- Filter the signals to remove high-frequency content. This slows the signal transitions. The filter must be located directly at the entrance of the cabinet or PCB and have an excellent GND/chassis connection.
- Shield the cable. Proper connection between the shield and the cabinet chassis is critical.
- Place a common mode choke on the cable. This increases the inductance of remote current paths, lowering their current flow.


λ/10
λ/10
λ/10
I/O GND
Internal GND

Cables and cabinets

Special situations

Remember: always first try to shield at PCB level (cheaper than at enclosure level)!

- Shielded cables with non-metallic cabinets:
  - connect the cable shields to a bottom metal plate (located under the PCB and connected to its GND with screws or bolts), using short connections (metal clamps, clips)
  - design a grounded guard ring around the PCB and connect the cable shields to it
- Isolated coax connections (e.g. 10Base2 Ethernet with coax cable)
  - apply signal filtering, common mode chokes
  - shunt the cable shield to the cabinet's ground through a capacitor
  - apply galvanic isolation for the signal (transformer, optocoupler)
- Unshielded cables with metallic cabinets: (see slide: "EMI prevention measures on cables")
  - filter the signals near their entry point into the cabinet
  - apply common mode filters on the cables

Cables and cabinets

Electrostatic discharge (ESD) and Burst protection

- Protect the electronic circuit from ESD and burst coming from the I/O cables:
  - partition the circuit
  - apply filtering immediately where the cable enters into the cabinet or the PCB
  - reduce loop areas, in particular with the I/O signals (signal and return path)
  - ground the PCB against the cabinet or bottom plate with multiple screws, bolts.
  - add some series impedance (R, L) in the input signals (from I/O cables, front panel buttons, keyboards): they reduce the overcurrents that can enter into the ICs
  - effectively ground cable shields against the cabinet's chassis
  - add ferrite clips on the cables

- A system that is robust against ESD and burst is usually also good from the radiated EMI emissions point of view

Quiz time

5. You need to connect a fast peripheral through a shielded cable. What cable should you take and why?

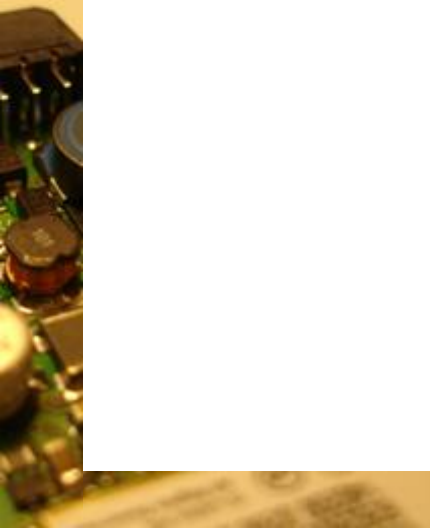
- ☑ 2 internal conductors + screen connected at both ends
- ☐ 2 internal conductors + screen connected only at one end
- ☐ 1 internal conductor + screen (coaxial cable)

5. How can you improve your circuit's immunity against ESD and Burst coming from input cables?

- if the cable is shielded, connect the cable's shield directly to the chassis. Do the same with the PCB's GND.
- partition the circuit carefully (keep sensitive circuits away from the I/O connector zone)
- filter the signals as soon as they enter into the PCB
- add series impedances (ferrites, resistors) to the input signals where they enter into the PCB
- make sure that I/O signals (and their return paths) do not form large loops, therefore reducing the risk of coupling with HF fields)

An Application Case

USB High Speed (480Mb/s) host controller platform

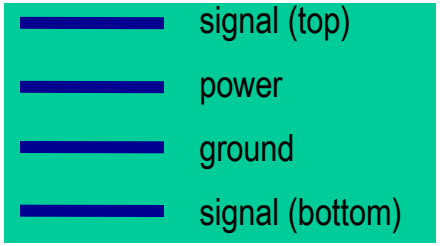


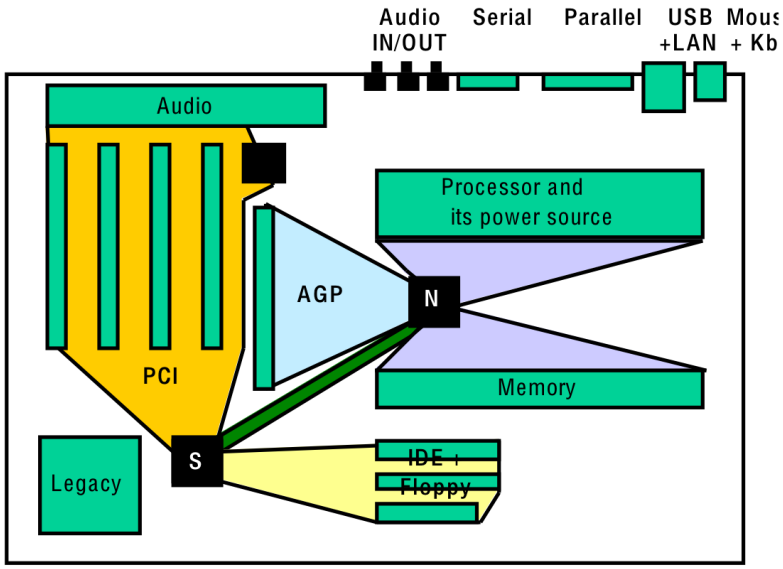
An Application Case

USB High Speed (480Mb/s) host controller platform

(source: Intel document: "High Speed USB Platform Design Guidelines")

- The guideline is for a 4-layer PCB
  - fast signals on bottom
  - most routing on bottom
  - more room for components on top
- High speed USB host controller implemented on a PC main board
- The USB host controller is connected to the PCI bus
- USB controller chip is from NEC





An Application Case – USB High speed platform

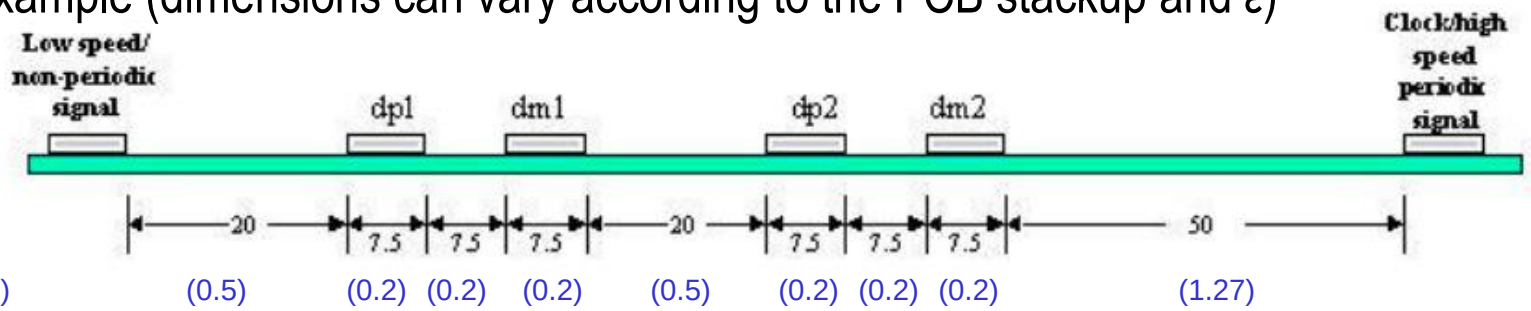
Component placement and trace routing recommendations

Item	Description
1	Place the high-speed USB host controller and major components on the unrouted board first.
2	With minimum trace lengths, route high-speed clock and high-speed USB differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to high speed USB differential pairs and any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors).
3	Route high-speed USB signals on bottom whenever possible.
4	Route high-speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.
5	When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
6	Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
7	Stubs on high speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, no stub should be greater than 200 mils. (5mm)
8	Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces as much as practical.
9	Route USB trace pairs together.
10	~~9.~~12. Keep high-speed USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.

An Application Case – USB High speed platform

USB traces and terminations

- USB signaling uses differential pair forming a transmission line with Z_0 = 90Ω
- The example is for a PC with two USB ports
- Example (dimensions can vary according to the PCB stackup and ε)

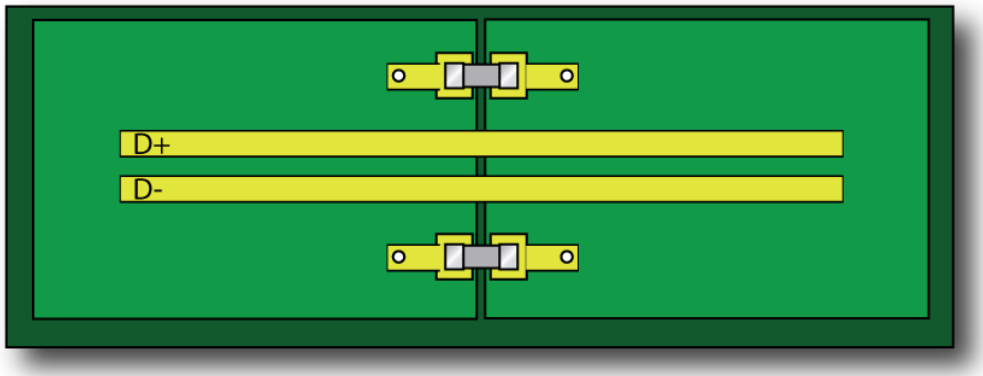


- These distances ensure low crosstalk between USB pairs and/or other signals
- Signal pairs require termination resistors. Place them as close as possible to the USB controller chip
- Length differences between the signal traces of a USB pair should be 150mils (3.8mm) or less

An Application Case – USB High speed platform

Ground planes and layer changes

- Do not split the reference planes (use uninterrupted planes, in particular for GND)
- If plane splits are unavoidable and USB signal traces need to cross them, provide stitching capacitors next to the traces to guarantee a close return path
  (USB signaling is not purely differential in all speeds (i.e. the FS Single Ended Zero is common mode)

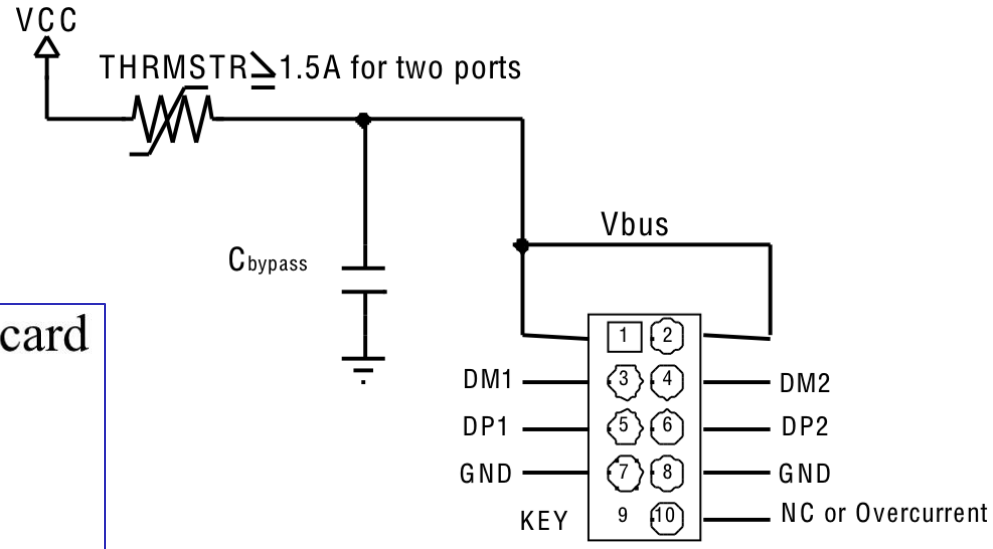


- Avoid changing layers with the signals as much as possible.
- However, changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

An Application Case – USB High speed platform

Front panel connector

- In certain designs, the two USB connectors are mounted on a small carrier board at the front panel
- Connection between the main board and front panel board is through a cable
  → only use 90Ω cables approved for USB
- Recommended cable connector pinout on the main board:



front panel connector card

An Application Case – USB High speed platform

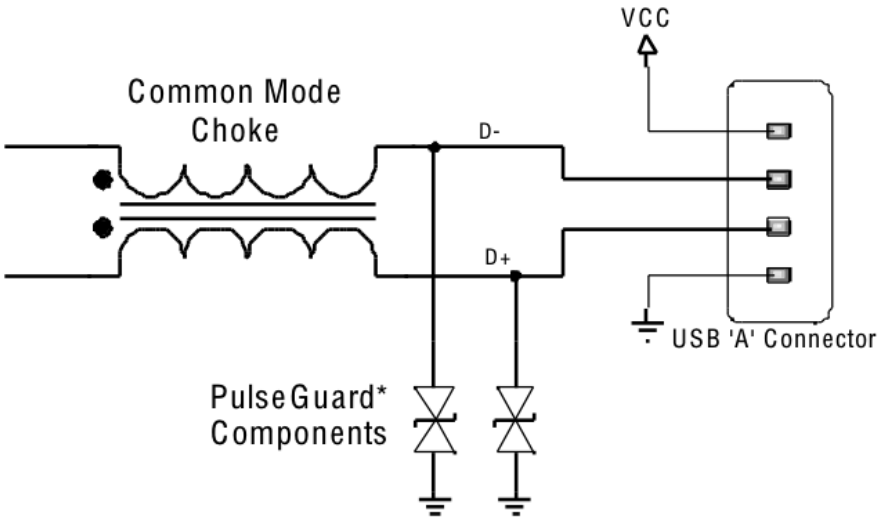
Remaining components placement

Item	Description
1	Locate high current devices near the source of power and away from any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors.) This reduces the length that the return current travels and the amount of coupling to traces that are leaving the PCB..
2	Keep clock synthesizers, clock buffers, crystals and oscillators away from the high speed USB host controller, high speed USB traces, I/O ports, PCB edges, front panel headers, power connector, plane splits and mounting holes. This reduces the amount of radiation that can couple to the USB traces and other areas of the PCB.
3	Position crystals and oscillators so that they lie flat against the PCB. Add a ground pad with the same or larger footprint under crystals and oscillators having multiple vias connecting to the ground plane. These will help reduce emissions.

An Application Case – USB High speed platform

Filtering and protection devices

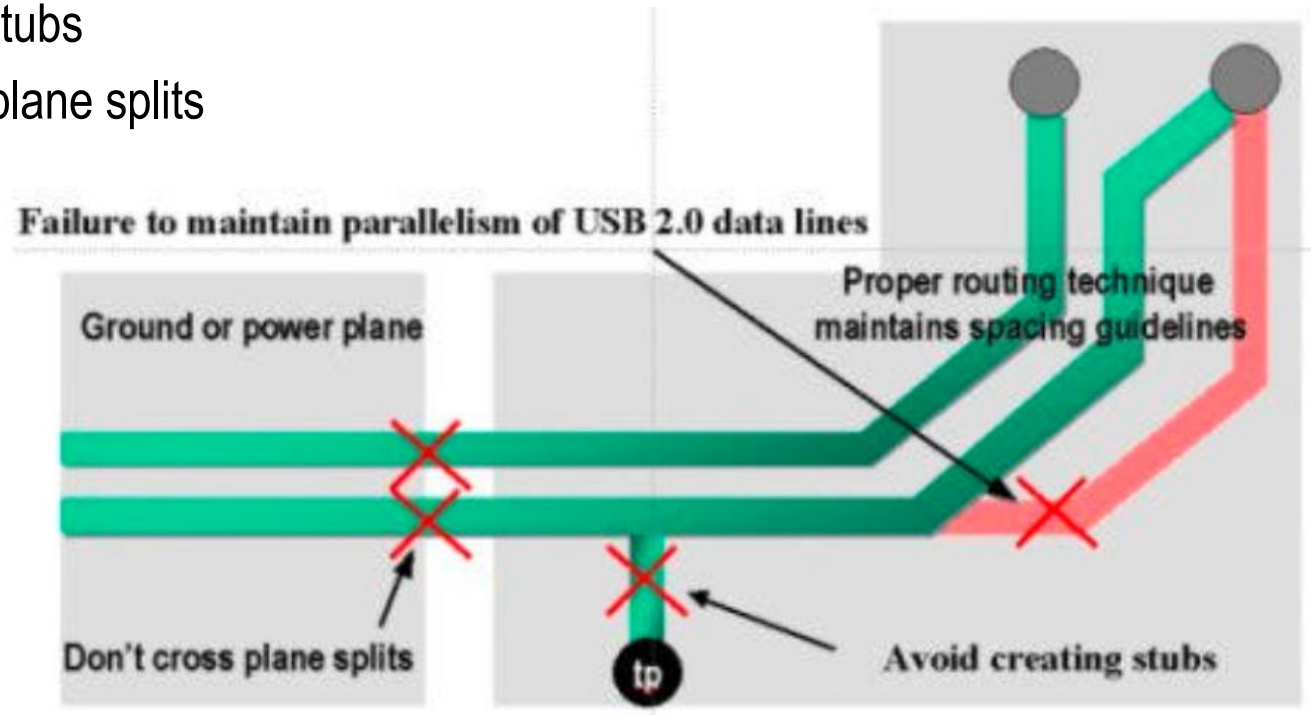
- Use common mode chokes only if strictly necessary for EMI, as they reduce the quality of the very fast USB signals
- Carefully select overvoltage protection devices, as they degrade the signal due to their capacitance



An Application Case – USB High speed platform

Frequent mistakes

- failing to maintain trace parallelism
- creating stubs
- crossing plane splits



2-Layer PCBs

Why use 2-Layer PCBs today?

- Old technology, not recommended for new designs!
- Today, a 4-layer PCB costs only 20% more than a 2-layer
- Only usable if the circuit operates below 5MHz and has signal transitions slower than 5ns ("5/5 rule")
- Main concern: missing GND plane:
  - Signal integrity problems, emissions
  - Less intrinsic decoupling between VCC and GND

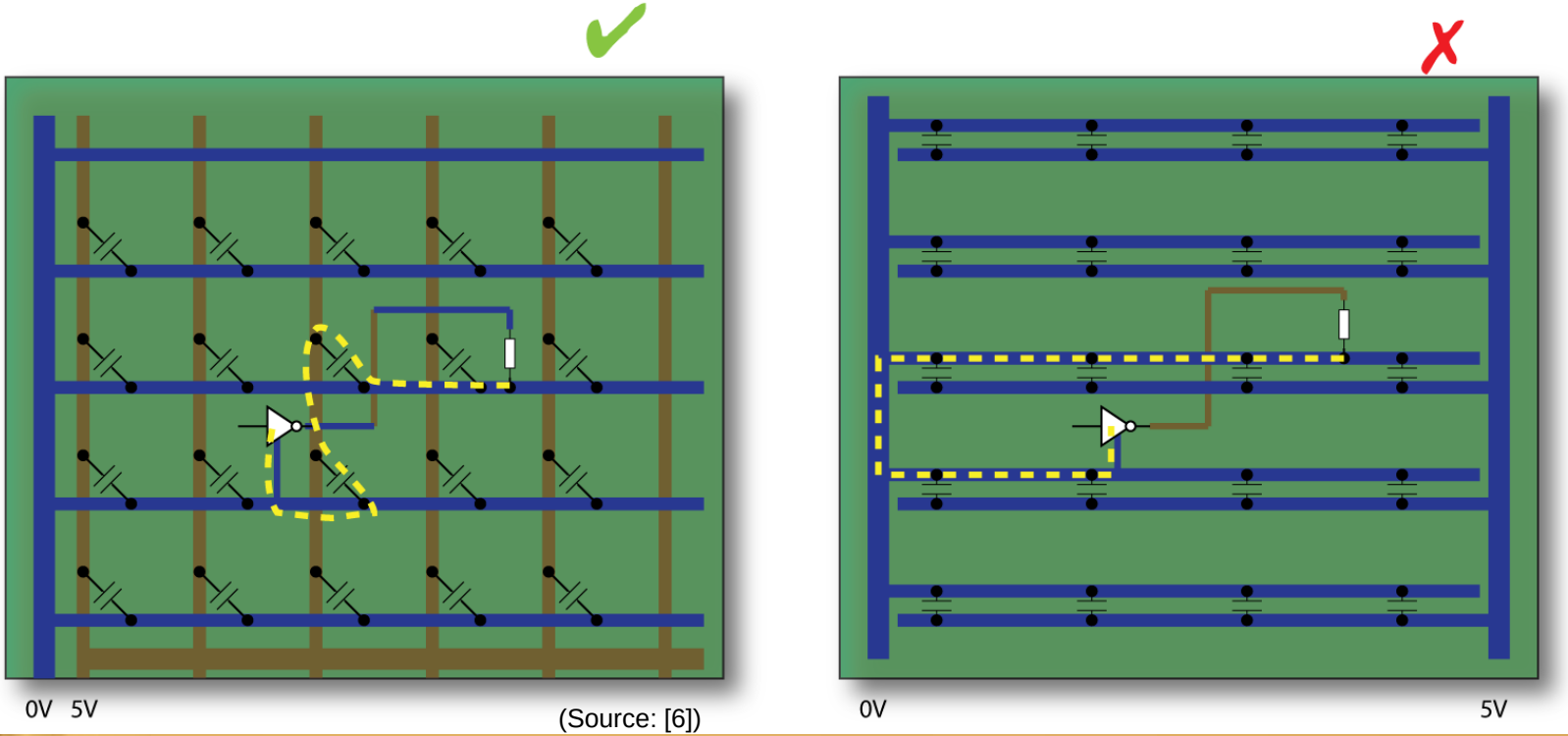
Should you still need to design a 2-layer PCB, here are some suggestions:

- Try to route all signals and VCC on one layer, leaving the other layer as a solid GND plane (microstrip technology). Best solution.
- If this is not possible, see more suggestions on the next slides …

2-Layer PCBs

VCC and GND routing

- Use orthogonal VCC and GND layout (route these traces first!)
- At the end of the routing, try to close as many GND meshes as possible by adding vertical GND lines (on top or bottom)



(Source: [6])

2-Layer PCBs

Some other general recommendations

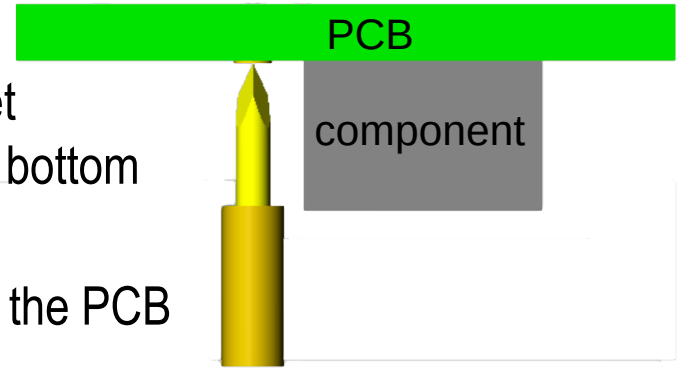
- Fill unused areas with copper and connect them to GND
- Draw a dedicated signal return trace (i.e. an additional GND trace) adjacent to critical signal traces (fast clock or low voltage analog signals)
- If possible, draw small GND areas (islands) under critical components (oscillators, low voltage signal amplifiers)
- Use a lot of decoupling capacitors and connect them with short traces, forming small loops
- Partition the layout carefully in function blocks (analog, digital, power, etc)

- But:
  Think twice before discarding the much better multilayer solution. The money you save in PCB costs with a 2-layer PCB will be spent, multiplied by a factor 10x or 100x in tweaking the 2-layer PCB and adding filtering, to pass the CE EMI requirements or to meet your own project specifications!

Design for testability (DFT)

Some general guidelines to make the PCB testable (1)

Test points for in-circuit test:



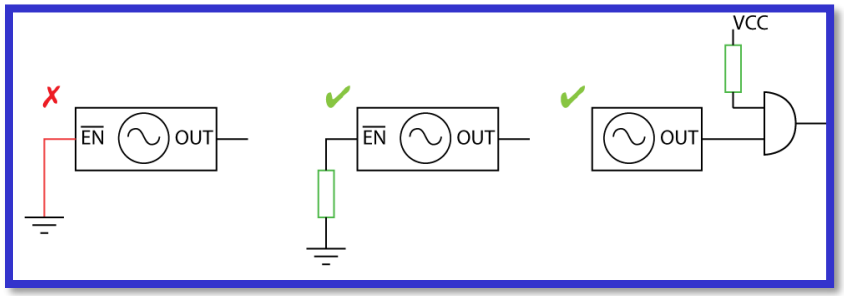
- Add a test point (it can also be a vias) on each net of the PCB. Place the test point preferably on the bottom (solder) side. It must be solder covered.
- Place 3 non-plated tooling holes at the corners of the PCB (for automated fixing/tooling of the PCB)
- Fill all vias with solder or soldermask (for vacuum actuated fixtures)
- Check your PCB manufacturer's rules for test point dimensions and min. distances
- BGA devices should have 100% access to all pins from the bottom side
- Thin PCBs can be difficult to test because they can bend under the pressure of the test probes
- Add test points to the power supply pins of each IC

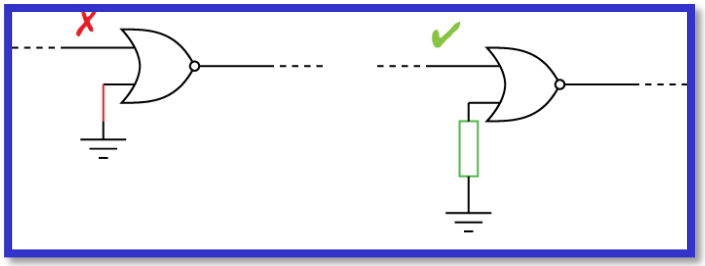
Design for testability (DFT)

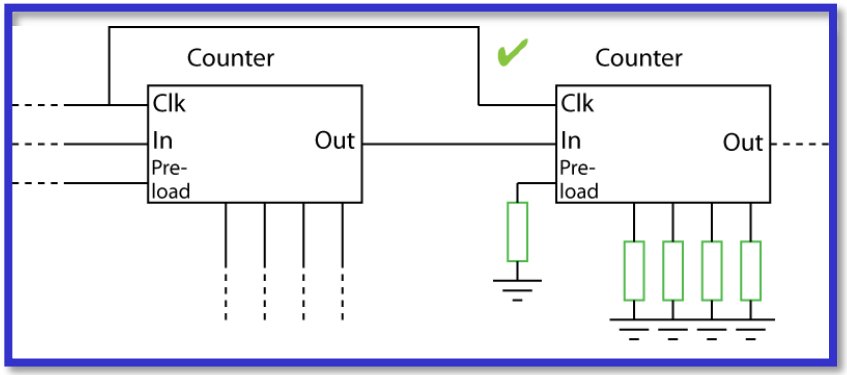
Some general guidelines to make the PCB testable (2)

Electrical rules:

- Make it possible to disable oscillators
- Add a test point to a Reset input
- Tie unused inputs to GND through a resistor
- Break serial chains (e.g. counters) with test points in order to allow pre-loading (this reduces test duration)



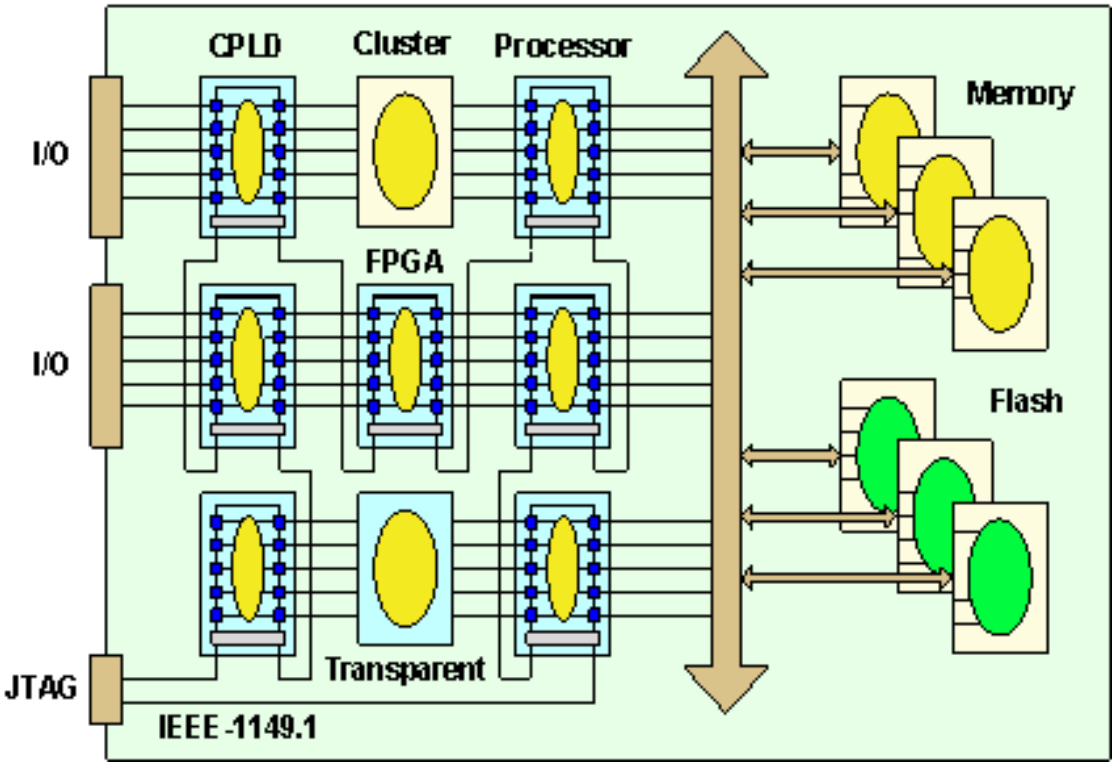


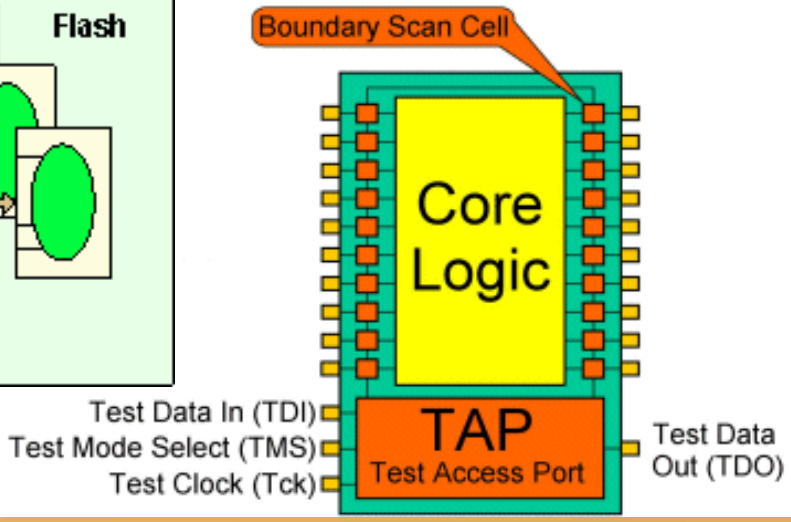


Design for testability (DFT)

Some general guidelines to make the PCB testable (3)

- Make use of "Boundary Scan" (IEEE 1149.1):





Quiz time

7. Give some reasons why a 2-layer PCB is not a good choice from electromagnetic compatibility (EMC) and signal integrity point of view.

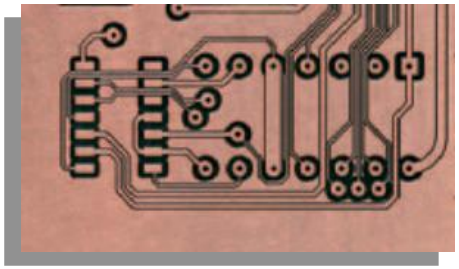
Answer:

the problem with 2-layer PCBs is that generally both layers are used for signals and therefore there's no continuous GND and VCC plane. Signals and their return paths generally form larger (uncontrolled) loops, therefore increasing emissions and signal integrity problems (crosstalk, reflections, etc). The missing GND (and VCC) plane also means more GND noise and less intrinsic decoupling capacitance between VCC and GND.

7. Test points

- ☐ can be placed near any component, regardless of its height
- ☑ should be added to each signal net on the PCB
- ☐ need not to be added to input pins that are tied to VCC or GND

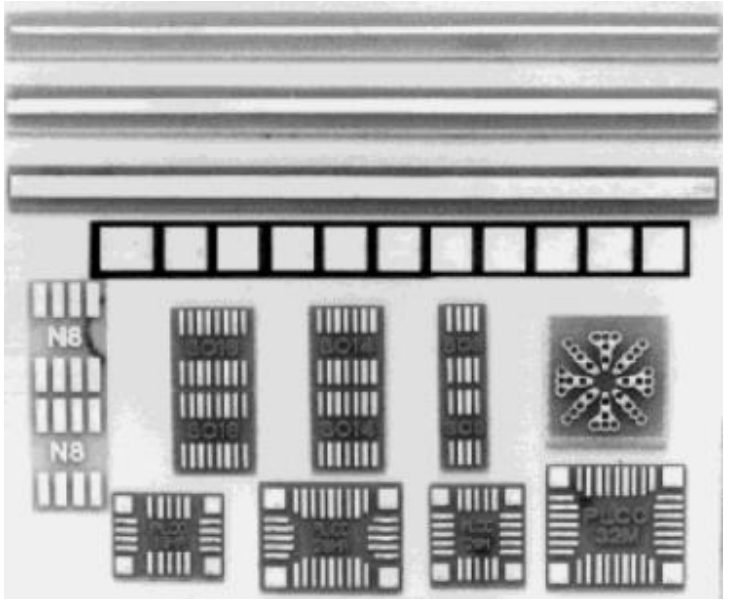
Prototyping



Milling / drilling plotter

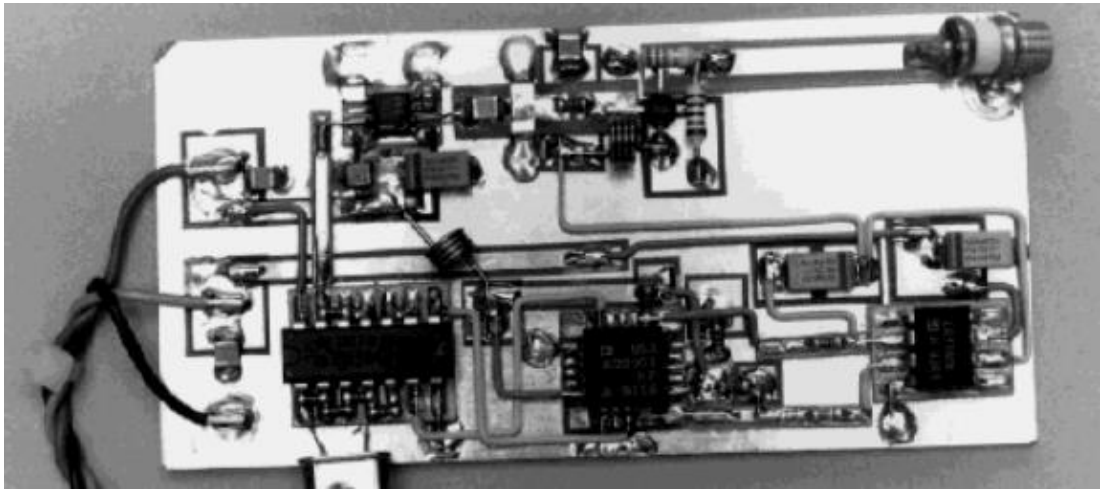
- Can prepare 2-layer PCBs starting from CAD (Gerber) files
  - Minimum track width: 4 mils (0.1 mm)
  - Minimum isolation width: 8 mils (0.2 mm)
  - Minimum drill hole diameter: 12 mils (0.3 mm)
- Prototypes and also small series
- Suitable for RF circuits
- Optional additional tools:
  - Press to assemble "multilayer" boards
  - Hole metallization system:

Prototyping



Mini-Mount®

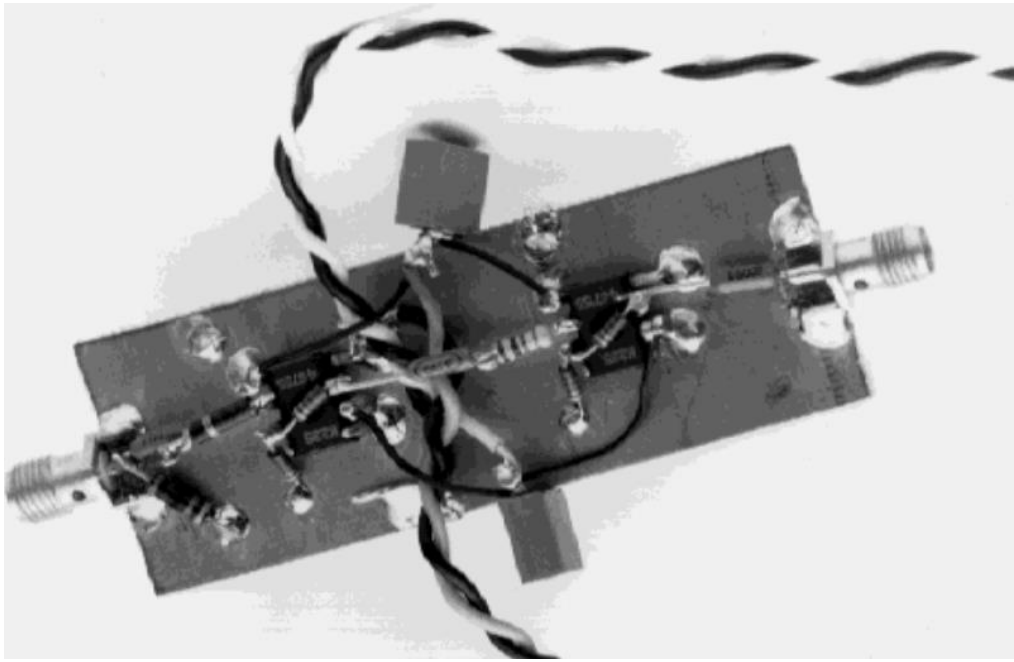
- A collection of small pieces of PCB with etched patterns (for ICs, discrete components, transmission lines, etc) on one side and contact adhesive on the other
- Assemble prototypes by sticking the pieces on a solid copper plane and soldering components on them
- Analog and high frequency circuits.
- Good for transmission lines (variants with 50Ω, 60Ω, 75Ω or 100Ω are available)



Prototyping

"Air mount" over a copper plate

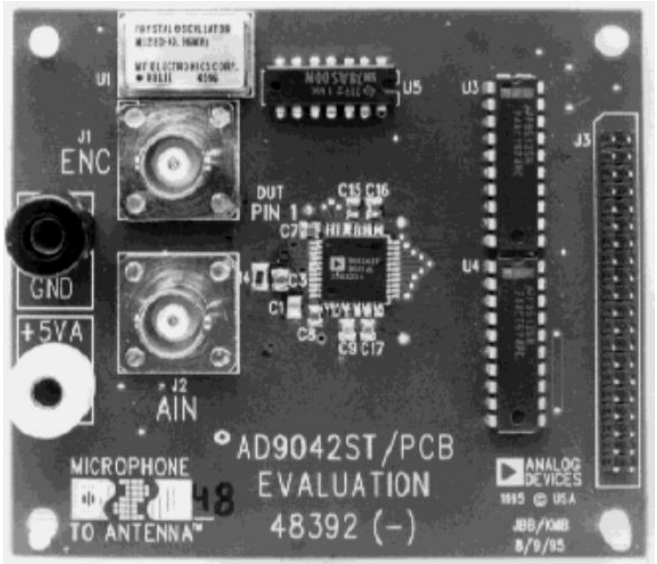
- The copper plate is the GND plane. Directly solder GND pins of the ICs to it.
- Components and wiring is implemented "in the air" above the copper plate
- Keeping wires at low height from the plate yields a fairly good "image plane" effect



Prototyping

Evaluation kits

- When available, it is always worth to invest in an evaluation board:
  - the circuit is mounted and operational
  - connectors already mounted
  - schematics and example software (when the kit includes a uP) are provided
  - good starting point and example for the own PCB layout
  - expected results (scope waveforms) are included and useful for verifications

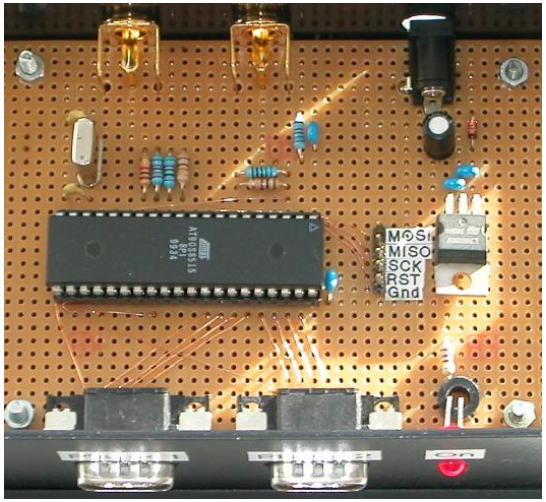


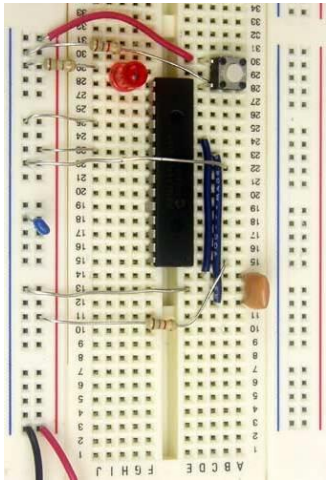
(Source: [1])

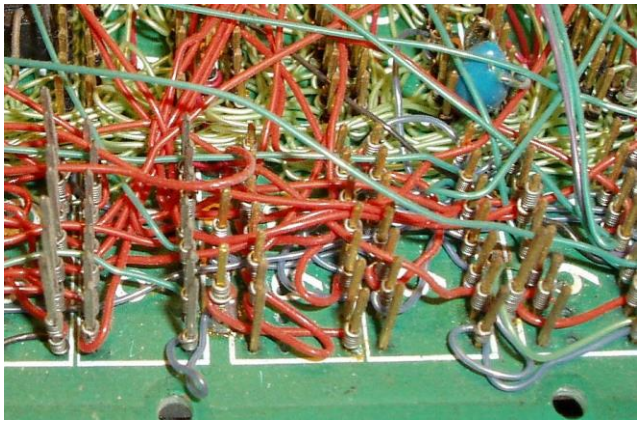
Prototyping

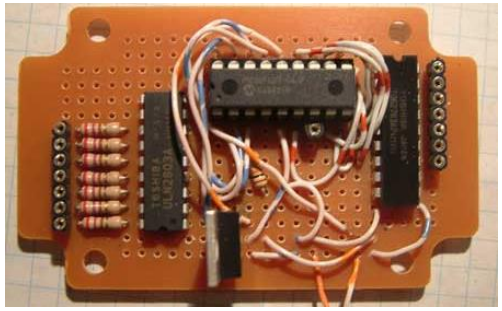
Old techniques

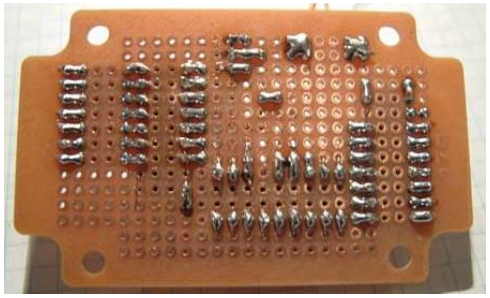
- These techniques should be avoided, unless you have a very slow circuit that is insensitive to noise and crosstalk











Prototyping

Some PCB manufacturers have special offers for prototyping

- starting from 1 piece: 2 and 4 layer PCBs
- 6 day lead time

Single-Pool
The perfect and low priced solution for **1 to 4 pcs. PCB Prototypes** with **2 or 4 layers** (No Discount on Re-Order).
Attention: from 4 pieces **ECO-POOL** (with Discount on Re-Order) is mostly lower priced!

No hidden costs!

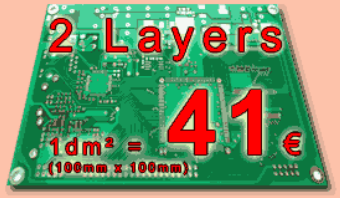
PCBs always INCLUDING:

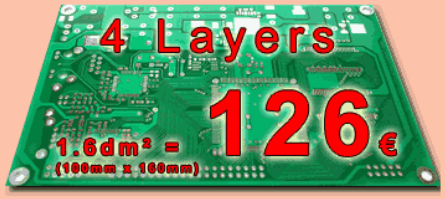
- ✓ ca. **6WD Production Time*** (standard)
- ✓ Design Rule Check
- ✓ **E-Test**
- ✓ Solderstop 2x
- ✓ Marking print 1x
- ✓ **Gerber-**, Eagle-, Target- **Import**
- ✓ Tooling cost
- ✓ Photoplot
- ✓ Tracks: 150µm min.
- ✓ Annular Ring: 150µm min.
- ✓ Drills: 0.3mm min.
- ✓ Unlimited Drills
- ✓ Milled outline
- ✓ Surface HAL leadfree **(RoHS compliant)**
- ✓ Material FR4 1.55mm
- ✓ 35µm Cu

Optional:
with surcharge

- ✓ Express from 48h
- ✓ Drills: 0.2mm min. (+15%)
- ✓ Routing: € 0,03 per mm
- ✓ Tracks: 125µm min. (+15%)
- ✓ Tracks: 100µm min. (+30%)
  (100µm not with **complex panel**)
- ✓ If needed: **Overproduction at ¼ Price!**

Pricing Examples:





*4 Layers: 8WD Production Time

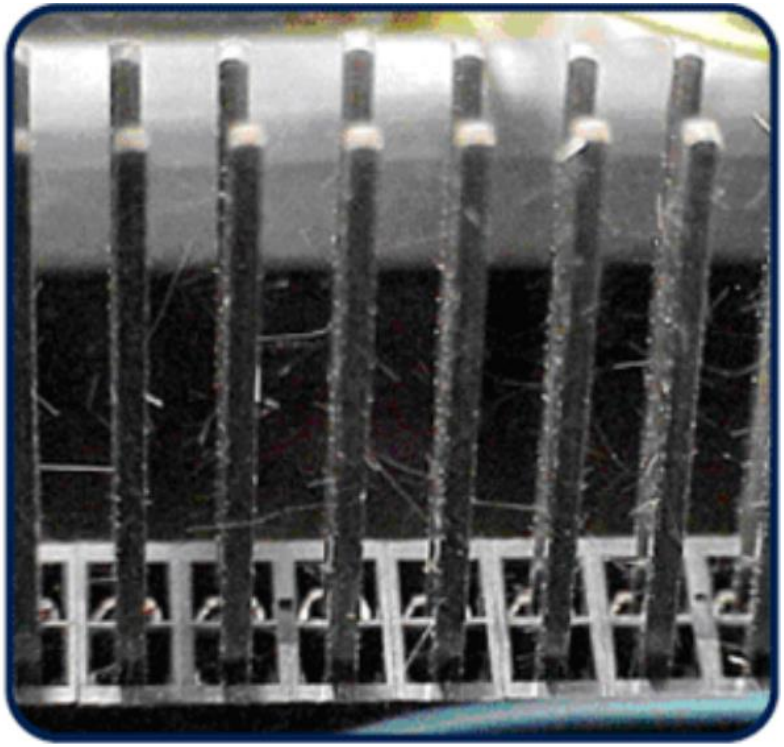
Directly from your Data:

ODB++ GERBER +extended EAGLE TARGET

ROHS

Can lead-free (no Pb) tin generate whiskers?

- This discussion is still open
- Lead-free tin is used as solder and to plate electrodes (connectors, etc)
- Risk of short circuits after 5-10 years of operation?



Computer Simulation Tools

Electromagnetic simulation software

- Helps improve the chance of first success in PCB layout (in particular at higher frequencies)
- Predict and mitigate signal integrity issues (crosstalk, line impedance, signal reflections, etc)
- Reduce problems with EMC compliance (emissions) at PCB or system level
- What if… analysis of the effect of different layouts and reference plane concepts
- Antenna and high frequency circuit design

- 2D and 3D solvers
- Various products from many companies, for example:
  - CST Microwave
  - Ansoft
  - Semcad
  - Agilent EEsof

- Most of them offer free "Student" versions (with very few limitations)

Exercise

9. A good pinout for a ribbon cable is:

☐	1: signal,	2: signal,	3: GND,	4: GND, ….
☑	1: signal,	2: GND,	3: signal,	4: GND, ….
☑	1: GND,	2: signal,	3: GND,	4: signal, ….
☐	1: GND,	2: signal,	3: signal,	4: signal, ….

Exercise

10. Explain the reasons why/how crosstalk can happen on connectors

Answer:
(see slides Series 12+13):

- inductive crosstalk can happen when the loop areas of different signals with their return wire partially overlap (mutual inductance). To avoid this, reduce the area that each signal forms with its return signal: the best is to reserve a return wire next to each signal wire
- crosstalk can also happen due to a non-zero impedance on the return path (GND) that is shared among two or more signals.

Thank you!