

ADVANCED ELECTRONIC DESIGN

EMC, signal integrity, grounding and power supply routing,
decoupling, transmission lines, simulation tools

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Topics of this series of 3 lessons

PCB Design

- Lesson 1:
 - Introduction
 - Partitioning, filtering
 - Shielding
 - Image planes
 - Continuous vs split GND concepts
 - Mixed signal circuits
- Lesson 2:
 - Decoupling
 - Transmission lines
 - Guard rings
 - Crosstalk, Ground bounce
 - Differential signaling
 - Terminations
 - Clock distribution: clock skew and clock jitter
- Lesson 3:
 - Place & route strategy
 - Components selection
 - Layer stackups
 - Multicard systems, backplanes
 - Enclosures, connectors and cables
 - ESD + Burst protection
 - 2-layer PCBs
 - Design for testability
 - Prototyping



Introduction

The terms of the problem

When designing printed circuit boards (PCBs) we are faced with EMC questions:

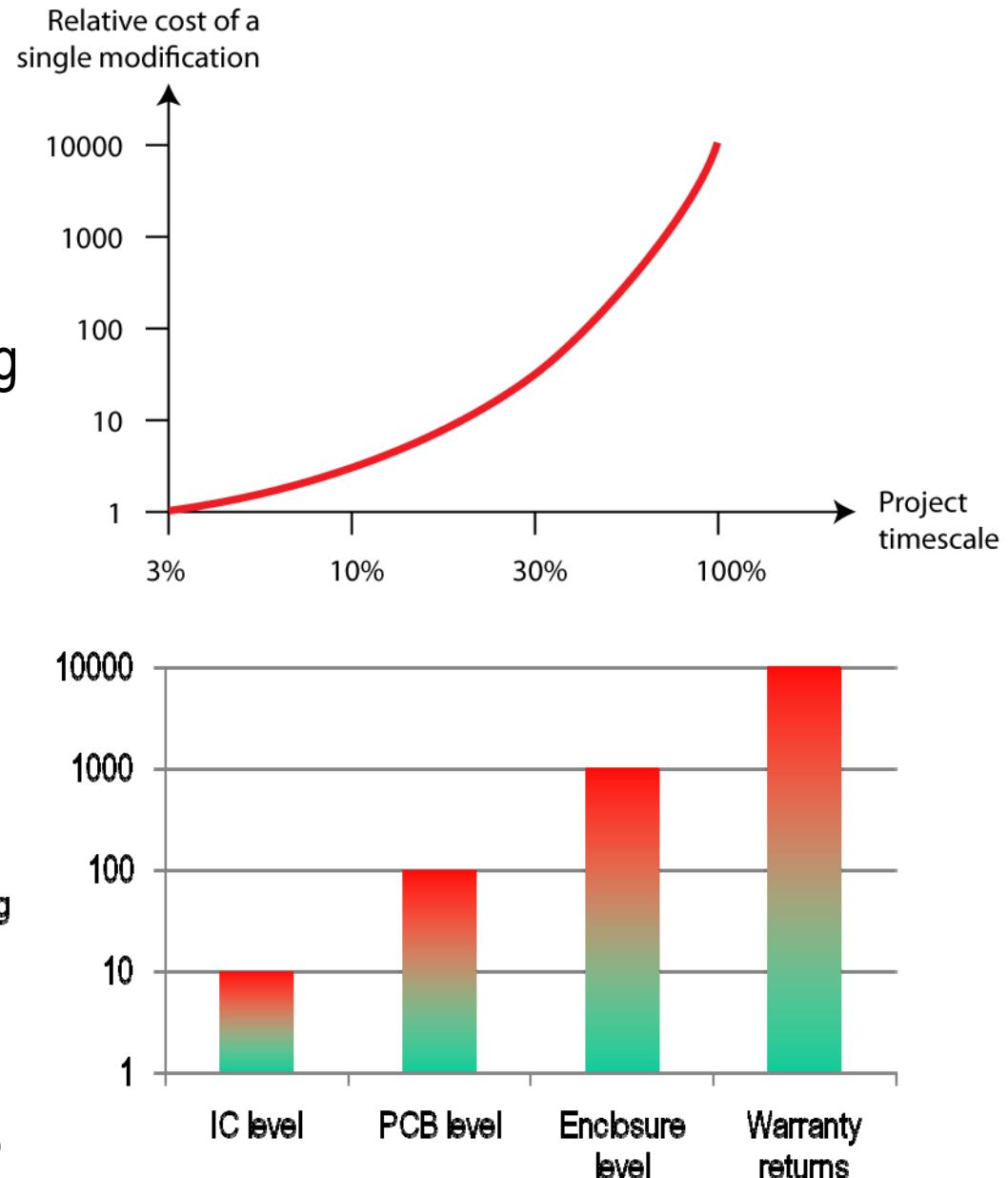
- Product must operate reliably and pass compliance tests with a minimum of design iterations
- System must be immune to external perturbations (GSM, DECT, WLAN, Broadcast. etc).
- We want to reduce costs of external shielding
- Product should offer wired or wireless data communications
- We want to use the newest and fastest ICs and processors
- Product may contain high precision analogue circuits or sensors
- We need to use low voltage logic (3.3V and less)
- We have mixed signal (digital+analog) circuits
- Product should be lightweight



A matter of costs

In order to reduce costs:

- Avoid errors from the beginning
- Solve signal integrity issues at component/PCB level
- Pass EMC compliance tests
- Avoid warranty returns



Definition of "high speed" circuit

We consider a circuit as *high speed*, when we need to consider the signal traces as transmission lines.

Rule of thumb:

For a given signal having a rising/falling time t_r , a signal trace of length $|l|$ must be considered under the transmission line theory, if

$$t_r < 2\tau$$

where τ is the time the signal takes to travel the distance $|l|$

$$\tau = \frac{|l|}{v_{ph}}$$

(v_{ph} is the signal velocity. Typical values on PCBs are: 0.5c .. 0.6c)

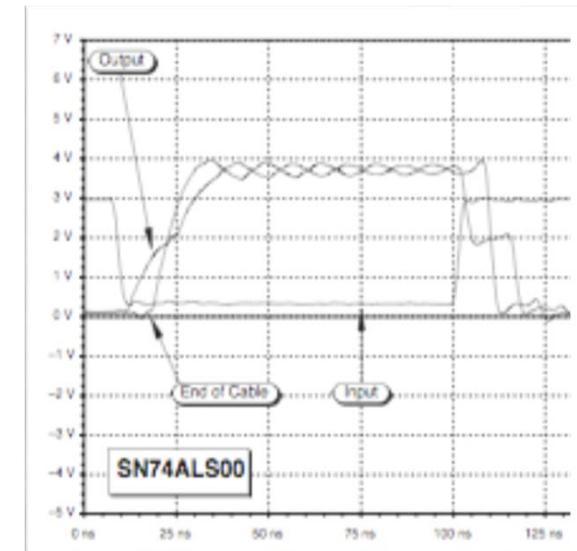
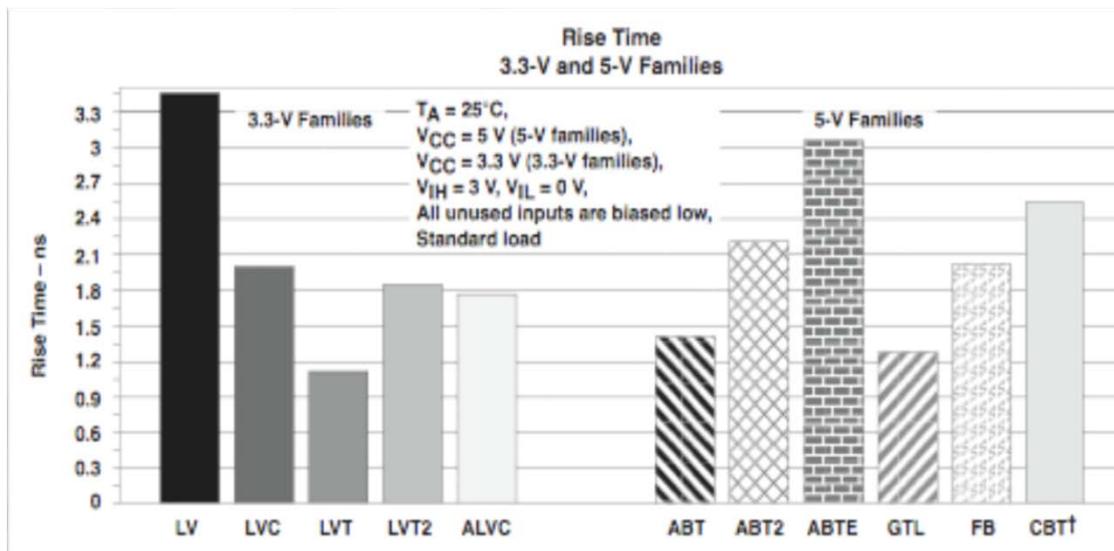
Definition of "high speed" circuit

Example

A 74LVCxx buffer (3.3V) has a rise time t_r of 2 ns.

With $v_{ph} = 0.5c$ we start having transmission line effects with a trace length of:

$$l = \tau \cdot v_{ph} > \frac{t_r}{2} \cdot v_{ph} = \frac{2 \cdot 10^{-9} s}{2} \cdot 1.5 \cdot 10^8 \text{ m/s} = 15 \text{ cm}$$



- even with today's standard components and moderate trace lengths (and PCB sizes), we must consider transmission line effects.

(Source: Texas Instruments)



Quiz time

1. When do we need to take transmission line effects into consideration

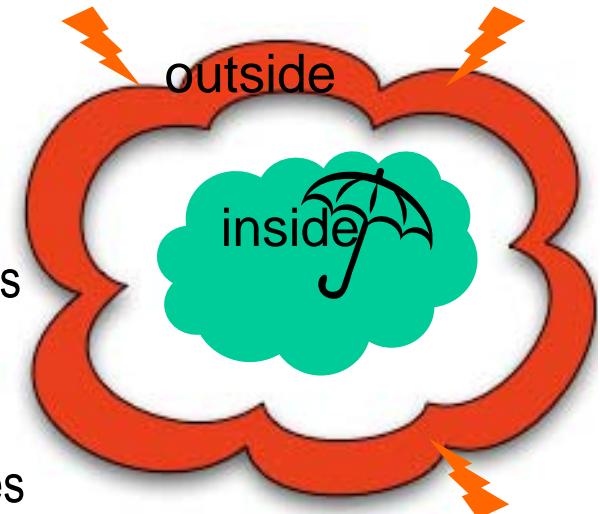
- always
- when signal traces are longer than $\lambda/2$
- when the signal transition time is shorter than twice the propagation time on the line
- when signal frequency is >100 MHz
- only when we are dealing with cables and connectors



PCB partitioning and shielding

Keep **inside** and **outside** worlds separated

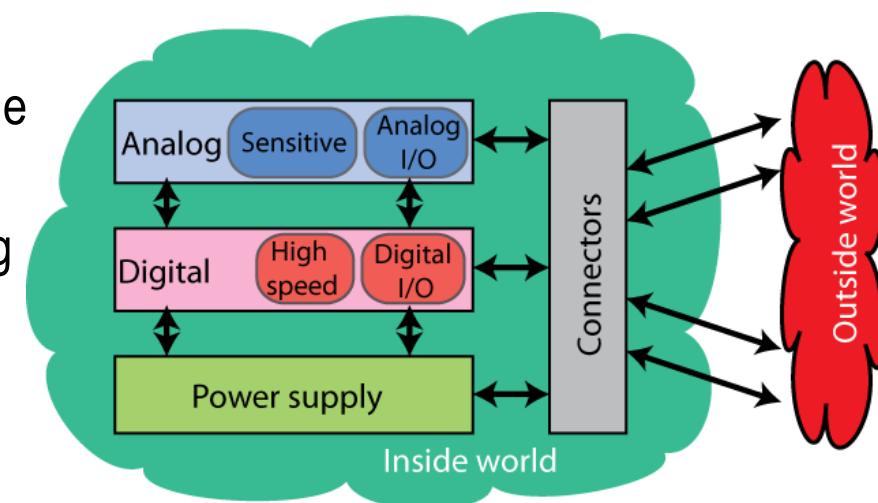
- **Inside** world: protected, filtered area
- **Outside** world: any cable (except shielded), connector (including board-to-board), components and PCB traces that are not over a continuous reference plane, pins or heatsinks that are taller than $\lambda/10$
- Goal: reduce design iterations, costly shielding and fixes
- Think as if you do not have a shielded cabinet (even if you do): make the design immune at PCB level to external and internal (!) noise sources
- Do not wait or postpone this partitioning until the design is completed. Do not rely on costly afterward shielding.
- other PCBs in the same cabinet must often be considered as "outside" components



PCB partitioning and shielding

Further divide the **inside world**

- identify functional blocks having different signal properties (sensitive analog, noisy digital, RF, I/O, etc)
- keep high speed clock sources (oscillators) far from connectors
- separate noisy blocks (e.g. switching power supplies) from sensitive analog circuits (e.g. sensor conditioning)
- carefully route signals leaving one zone for another (more on this in this course)
- apply adequate filtering or suppressing to these signals
- be cautious when using an autorouter (define keep-out traces or no-route areas)





PCB partitioning and shielding

Watch out for self generated problems

- different **internal** blocks can affect each other with EM phenomena:
 - noise emitted by PWM circuits (switching power supplies, motor drives, inverters)
 - GND noise generated by fast switching logic circuits
 - RF noise from oscillators or wireless transceivers
 - harmonics due to signal distortion, inter modulation
 - spurious signals generated by unwanted demodulation (in p-n junctions)
- examples of coupling of these phenomena
 - through common power supplies ("supply noise")
 - capacitively, inductively

PCB partitioning and shielding

Prevent noise from crossing a functional block's boundary

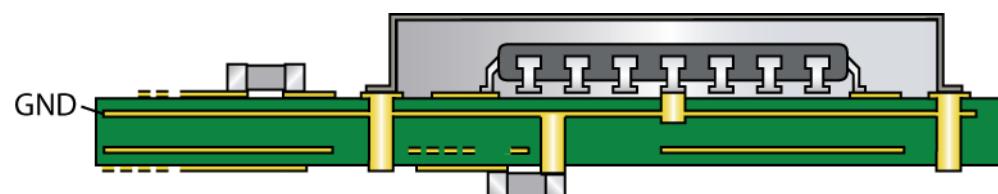
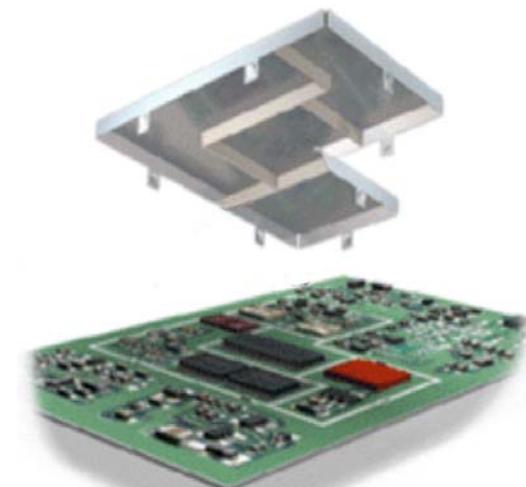
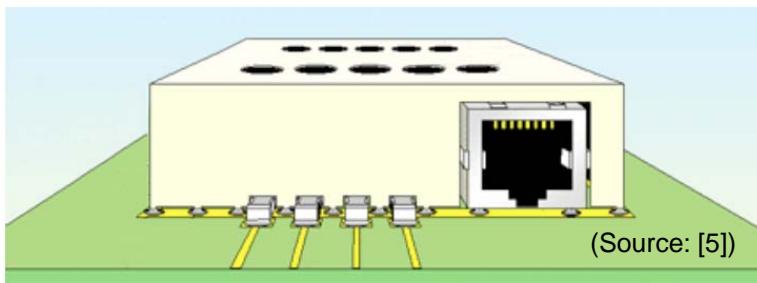
- Consider the following protective measures
 - ferrite beads
 - filters (π , L)
 - opto couplers
 - common mode chokes
 - fiber optic link instead of copper cable
 - add series impedance (R, L) to I/O signals
 - adequately filter signals going to the front panel against ESD (e.g. LEDs, keyboards) by using one of above techniques
 - add shielding at PCB level



PCB partitioning and shielding

Shielding

- Shielding at cabinet level is possible but has disadvantages
 - weight, cost
 - it is often not possible: e.g. when we have antennas inside (Bluetooth, GSM, ...), apertures for displays, memory cards, connectors, etc.
- Always first try to shield at PCB level
 - Examples:



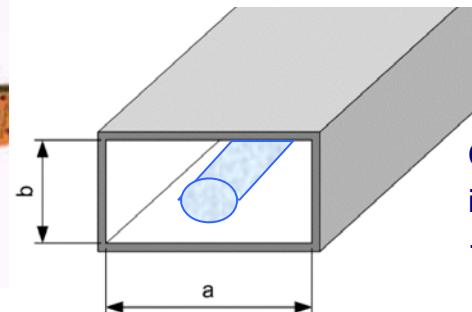
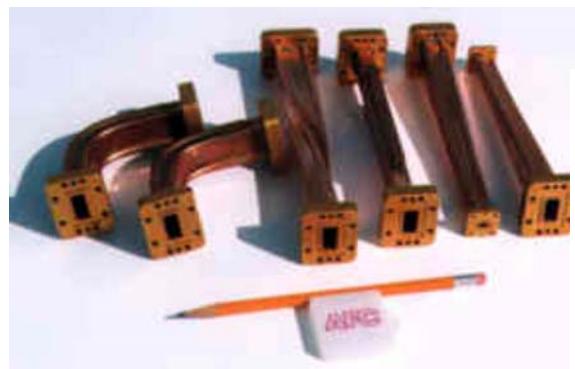
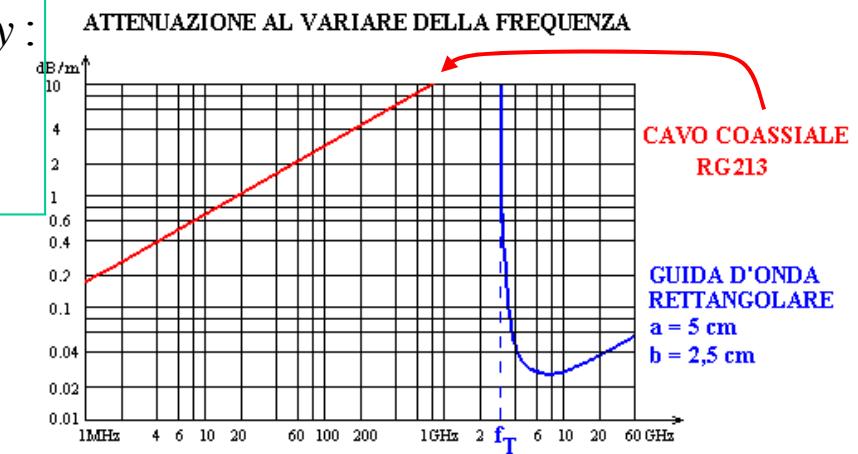
PCB partitioning and shielding

A quick introduction to waveguides

- EM-waves can propagate inside hollow waveguides above a certain frequency f_c
- Above f_c , the attenuation is very low. Below f_c , attenuation is very strong

The critical or cutoff frequency is defined by :

$$a = \frac{\lambda_c}{2} \text{ where } \lambda_c = \frac{c}{f_c}$$



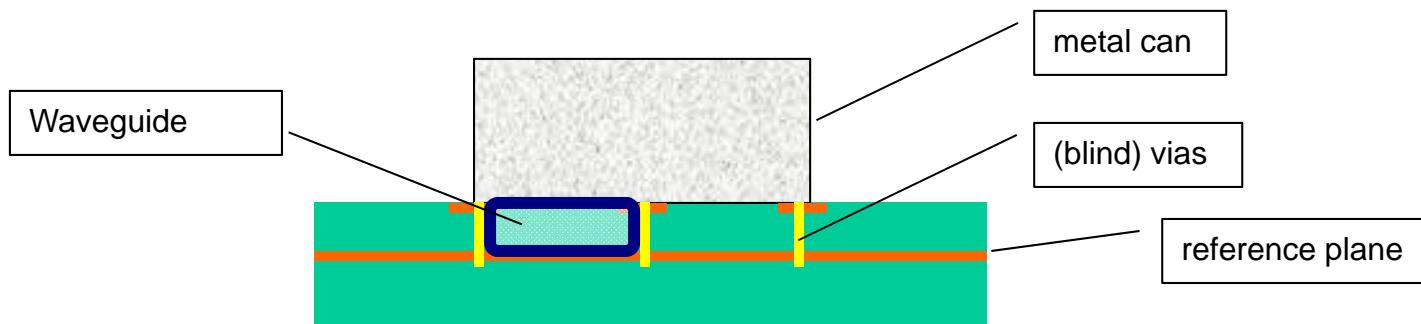
Caution: with a conductor inside it becomes a coax cable
 $\rightarrow f_c = 0 !$

(Source: [22])

PCB partitioning and shielding

Waveguide: what does it have to do with PCBs?

- we can use its properties to block signal propagation through the apertures inside the PCB
- this is accomplished by overlaying guard rings (top layer) and reference planes (internal layer) over a distance of $\lambda/10$ or more in order to create waveguides of this depth
- place as many blind vias on the waveguide's side walls as possible
- keep aperture of the waveguides so that a $<\lambda/2$ (at the highest signal frequency)
- do not pass signal traces inside these "waveguides"





PCB partitioning and shielding

Waveguide as resonator

- a closed metal box has many resonance frequencies inside. The lowest resonant frequency is at $f_0 = \frac{c}{2a}$, where a is the broadest side length of the box
- resonances are often unwanted inside the metal can: they change the circuit's behavior (increased coupling, HF currents, etc)
- a metal can having resonances inside has decreased shielding effect

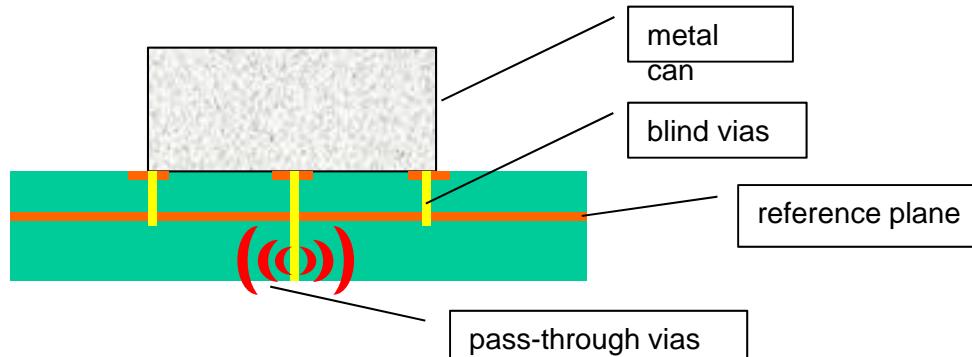
Therefore ...

- keep metal cans as small as possible
- make small compartments inside
- if necessary, coat the inner of the metal can with a film of absorbing material (ferrite)

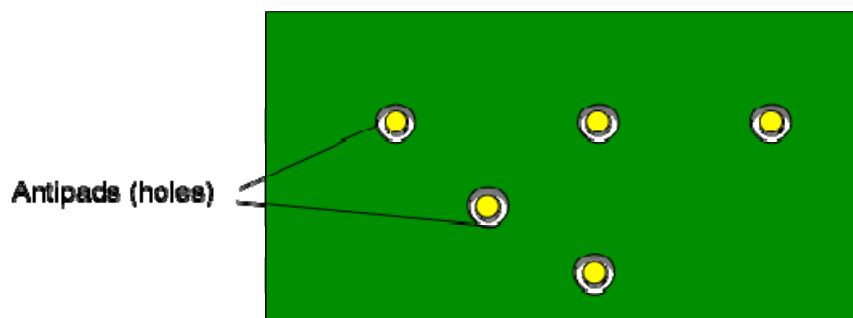
PCB partitioning and shielding

Vias: buried (blind) vs. pass-through

- pass-through vias are short stubs (signal reflections) and emitting antennas



- pass-through vias create holes in the reference plane, reducing its shielding effect



Quiz time

2. What happens if we insert a cable inside a waveguide?

The waveguide is no longer a waveguide, but becomes a sort of coaxial cable (the waveguide forms the shield). Therefore, the optical high-pass filtering property of the waveguide disappears and all frequencies (down to DC) are allowed to pass. This can void the original intent of shielding against signals having frequencies below the waveguide's cutoff frequency f_0

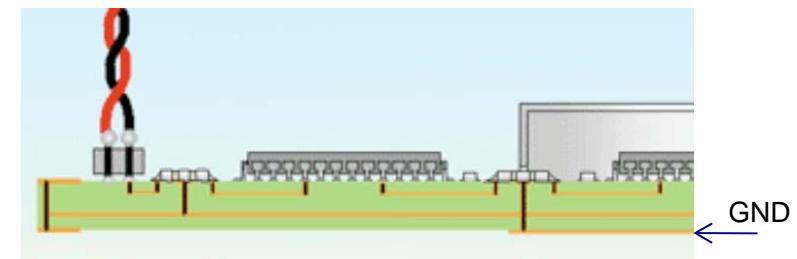
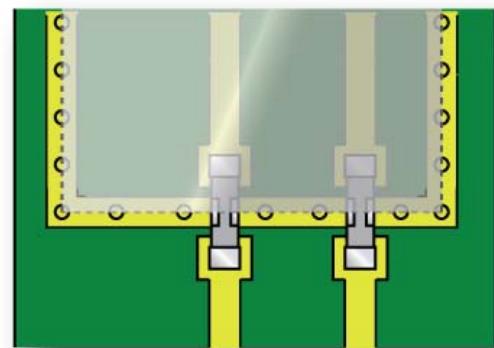
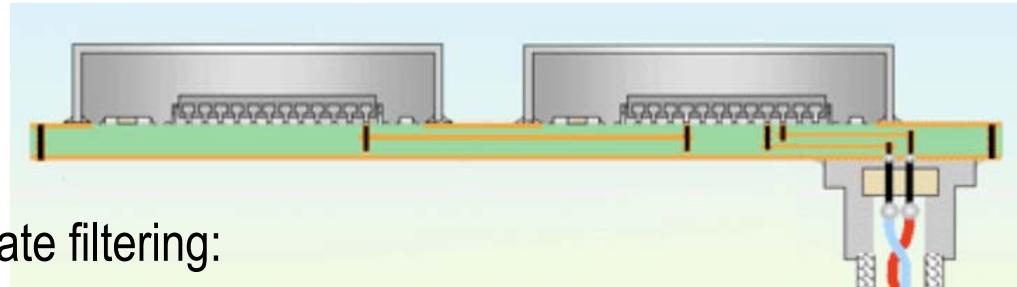
3. What should we observe when shielding parts of a PCB with metallic cans:

- material of the metal (conductivity)
- resonances
- number of contacting points to the PCB's 0V plane
- thermal stress (expansion)

PCB partitioning and shielding

Passing signals across different PCB areas – Filtering (1)

- when different functional areas are considered to be part of the same shielded group: signal traces must be shielded (=inside) as well. This pertains also to blocks connected through a shielded coax cable
- in all other cases, apply adequate filtering:



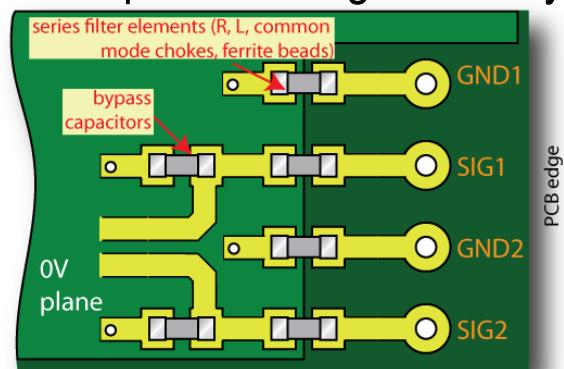
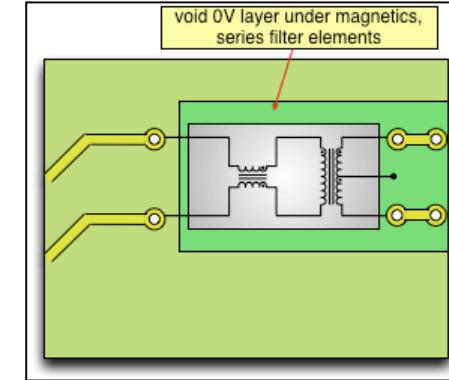
- optocouplers are a valid alternative for crossing the boundary of a shielded zone

(Source: [5])

PCB partitioning and shielding

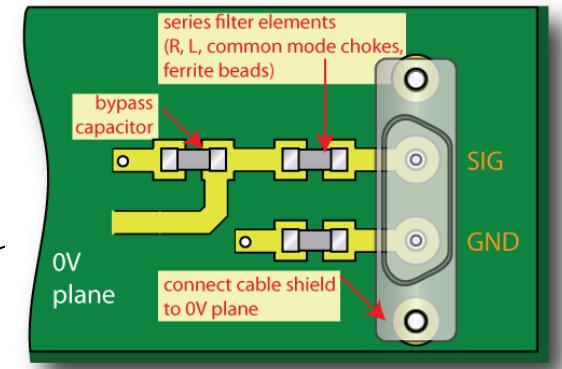
Filtering (2)

- add series L,R to I/O signals going to connectors
 - void GND area under these components to reduce input/output stray capacitance on these elements
- add capacitors to the 0V plane
 - keep connections very short. Use vias directly to the reference plane
- at frequencies > 100MHz, replace inductors with ferrite beads (SMD)
- consider using common mode chokes
- whenever possible, group all connectors on the same side of the PCB
- keep internal signals away from the connector area



example for
unshielded
cable I/O

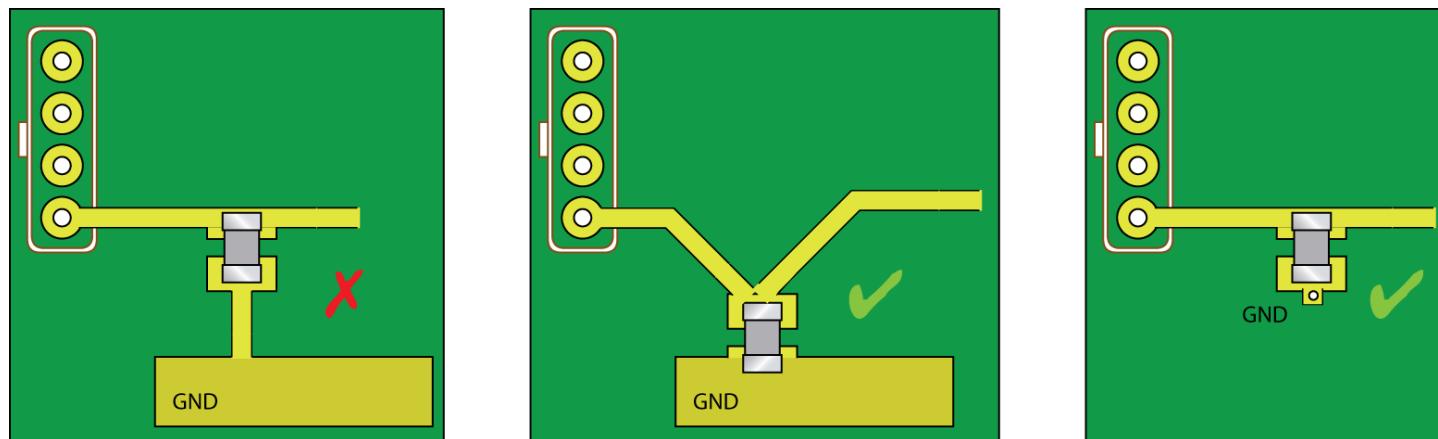
example for
shielded
cable I/O



PCB partitioning and shielding

Filtering (3)

- keep GND connections of filtering components as short as possible (reduce L)

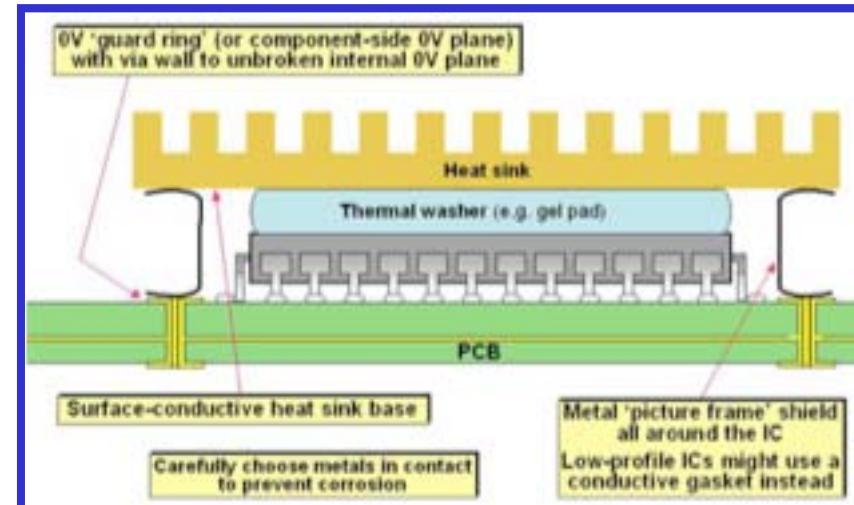


(Source: [22])

PCB partitioning and shielding

Heatsinks: can be a problem or a solution

- today's high speed logic / uP's often require heatsinks
 - a big antenna radiating the high frequency signals (clock, etc) if not handled correctly
- however, a heatsink can become the top lid of a shielding can:



(Source: [5])



PCB partitioning and shielding

A suggested workflow for the PCB design

- Use multi-layer PCBs and assign two layers to the reference planes (GND, VCC)
- Position I/O connectors at the periphery of the PCB under consideration of external cabling layout requirements (cabinet, rack)
- This defines the **outer** world area of the PCB
- Place "critical" components (active/passive): high speed interfaces, fast clock circuits, sensitive analog circuits, ..., and partition them carefully. Keep them at some distance from I/O connectors
- This defines the **inner** world area of the PCB
- Draw reference planes (underlying "ground" planes)
- Draw critical nets (adjust their line impedance) and power supply lines
- Place the remaining (uncritical) components
- Route the remaining nets. This is the only task that should be assigned to the autorouter.

Quiz time

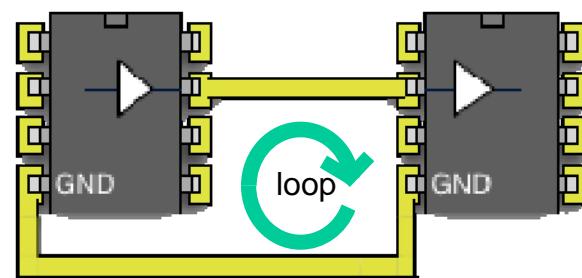
4. How can we protect the inner (sensitive) world of a PCB?

- by powering the circuit from batteries
- by partitioning
- by shielding the sensitive components,
- by filtering the signals to/from the inner part
- by placing the PCB inside a metallic enclosure
- by connecting the circuit GND to the protective earth (PE)

Image (or reference) planes

Theory:

- every signal must have a return path
- keeping the distance between "forward" and "return" path small reduces the loop area → reduced emissions (see "E-M field radiated by a small current loop")



- when an image plane is present, the return current will choose the path forming the smallest loop:
this is the solution for the minimal inductance and the minimal stored energy in the magnetic field

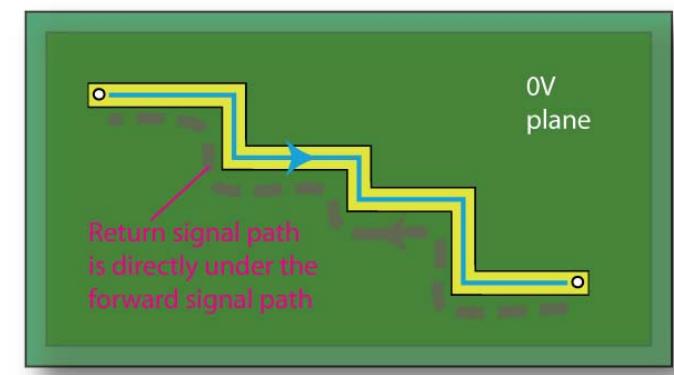
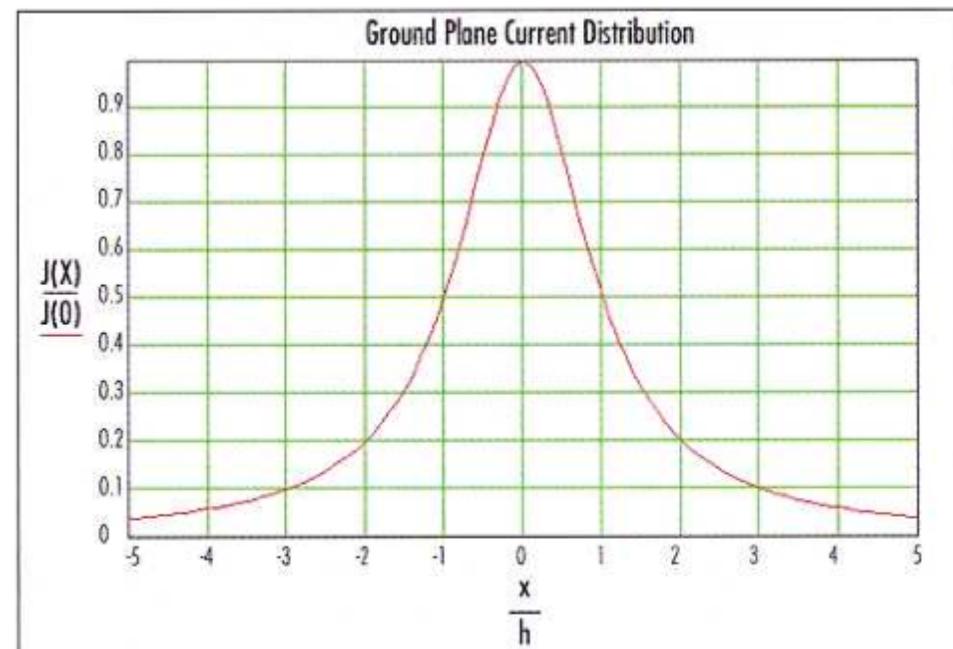
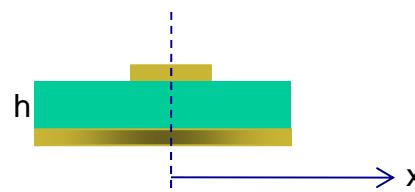


Image (or reference) planes

Return current distribution in the image plane:

- in the image plane, the return current concentrates directly under the signal trace
example: if $h=1\text{mm}$ then at $x=2\text{mm}$ the current is already decreased to <20%
- the current density J at a distance x from the center under the signal trace is:

$$J(x) = \frac{I_0}{\pi h} \cdot \frac{1}{1 + \left(\frac{x}{h}\right)^2}$$

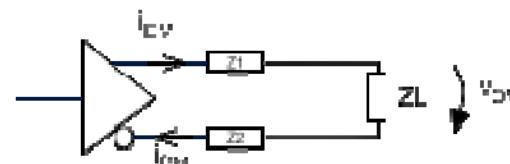


(Source: [19])

Image (or reference) planes

What is the goal?

- keep in mind - we want to:
 1. avoid that some signals on the PCB perturbate others
 2. keep RF emissions of the PCB (and attached cables) at a minimum
- RF fields generated by **differential mode currents** (**2slides back**) are only a (minor) part of the problem, because they are confined to small loops (at far field they cancel each other)



- Common mode currents of smaller amplitude generate much higher emissions (they "add" at far field – "dipole" emission)

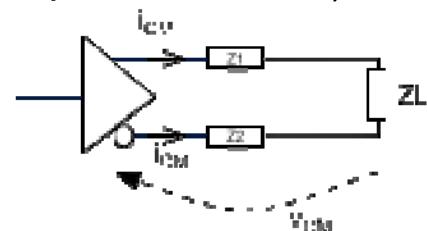
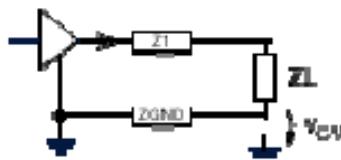


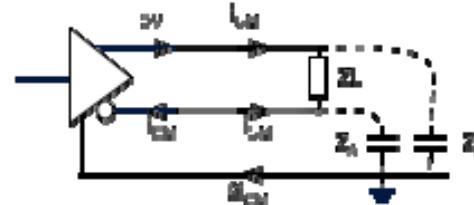
Image (or reference) planes

Examples of how common mode currents are generated

1. consequence of *ground noise* generated by series impedance in the GND return trace



2. even if return is not through GND (differential line), different parasitic loading can induce common mode currents



3. Noise sources external to the circuit

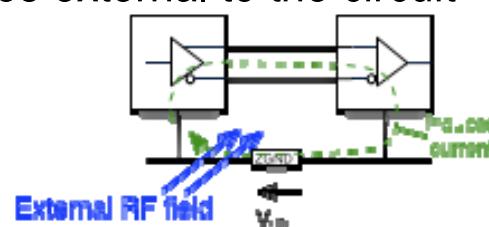
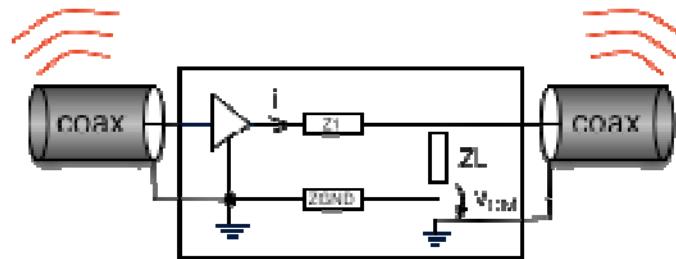


Image (or reference) planes

Why is common mode noise so undesired?

1. *ground noise* can translate to emissions if cables are attached (dipole!)



2. common mode currents can produce unwanted voltages inside the circuit.
In the example, when $Z_A \neq Z_B$ then i_{cm} produces a voltage on Z_L

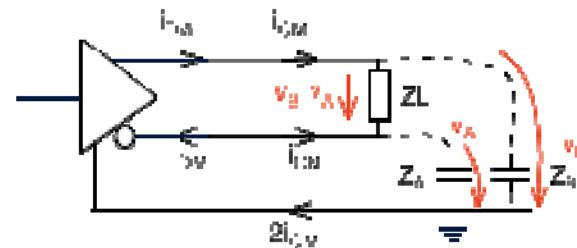




Image (or reference) planes

Common mode currents/voltages in general happen...

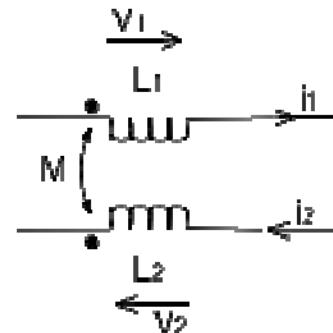
- if forward and return currents do not cancel out locally. This happens when:
 - return path is far from forward path and has different impedance or parasitic load
 - presence of multiple return paths (wanted and unwanted (=parasitic))
 - if there is voltage drop in the GND return path ($Z_{GND} \neq 0$) → GND noise
- ⇒ **always provide a return path as close as possible to the forward path!**
- this is best accomplished by a near reference or image plane (GND)

Minimizing the return path impedance is important because

- voltage drop on return path (GND noise) is reduced
- return current avoids searching for alternate (parasitic) paths

Image (or reference) planes

Mathematical proof that the effective impedance is minimized when forward and return traces are near:



$$V_1 = L_1 \frac{di_1}{dt} - M \frac{di_2}{dt}$$

$$V_2 = L_2 \frac{di_2}{dt} - M \frac{di_1}{dt}$$

if $i_1 = i_2 = i$ then the voltage drop on each path is
 $V = (L - M) \frac{di}{dt}$ and we call $(L - M)$ the
 "net partial inductance of each conductor".

- even if the traces have $L_1, L_2 (\neq 0)$, the voltage drop can be nearly zero if M is maximized. This is the case when the two lines are as close as possible.
- this is best achieved with an uninterrupted image/reference plane for the return signal, at a PCB layer adjacent to the layer carrying the signal trace.
- it can be shown [20] that ground noise on a 2-layer PCB can be reduced by simply placing an unconnected metallic surface (image plane) near the PCB (a full GND area (layer) is however still better!)

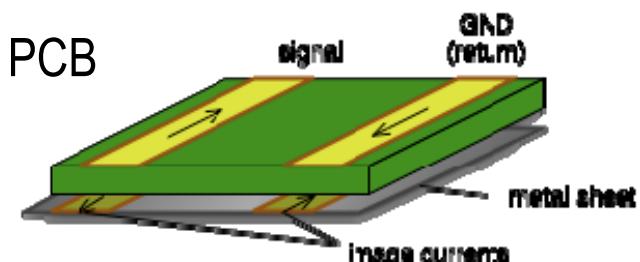
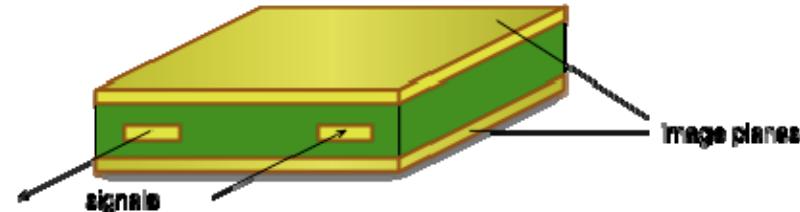




Image (or reference) planes

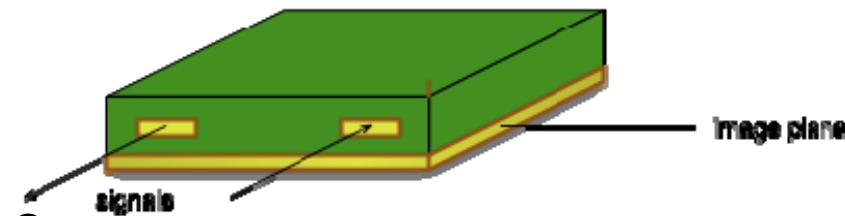
Stripline technology

- embed signal traces between two image planes ("sandwich" construction) for best shielding of noisy signals to effectively protect sensitive analog traces against external noise



Microstrip technology

- this is the most commonly used technology. It is a little less effective than stripline, however.

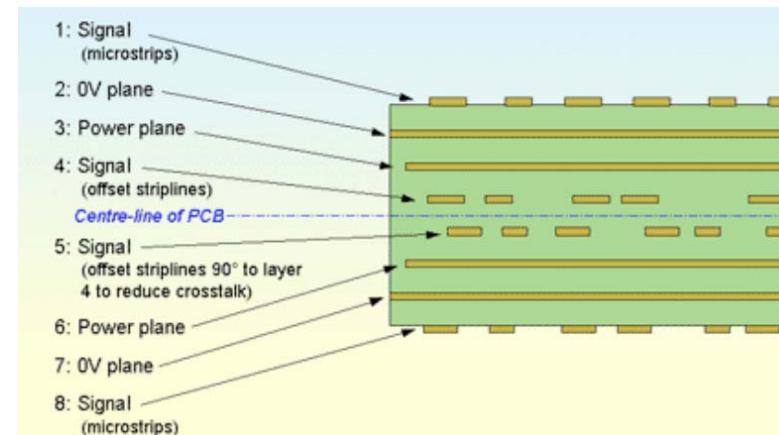
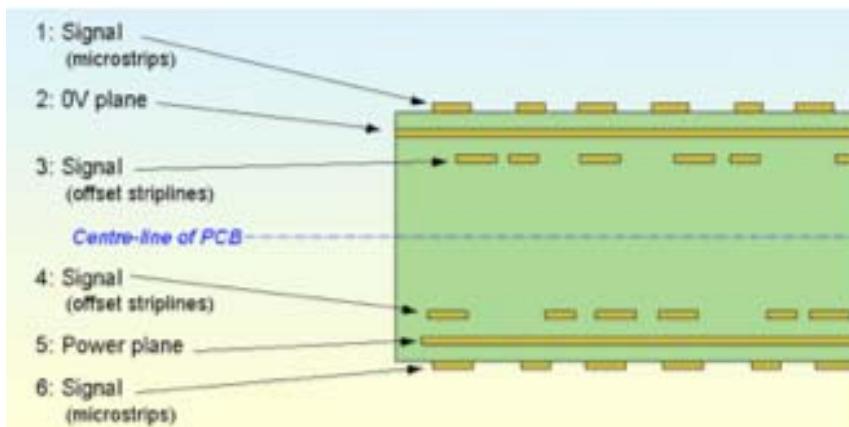
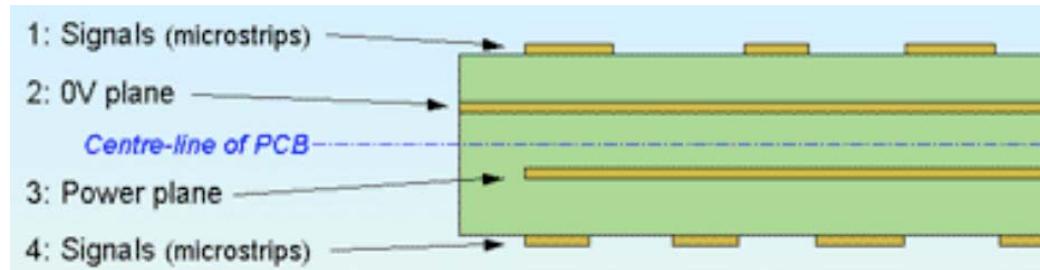


Which image plane is most suitable?

- both GND and VCC can be used. VCC however is generally more noisy than GND.

Image (or reference) planes

Examples of reference planes in multilayer PCBs



(Source: [5])

Quiz time

5. What is an image plane and how does it work?

Answer:

An image plane is a continuous (uninterrupted) copper plane in one or more PCB layers. It is connected to GND (or VCC) and serves as the return path for signal traces on other (adjacent) PCB layers.





PCB partitioning and shielding



To split or not to split the GND plane ?

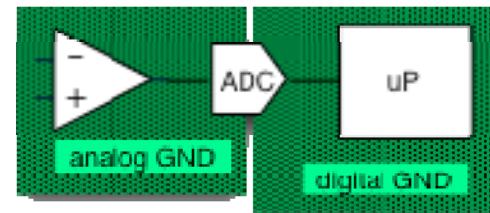
- Literature is quite discordant on this subject (Books, Application Notes, ...)
- up to 10-15 years ago (<30 MHz clock speeds) partitioning the GND plane was a recommended practice
- today, the specialists tend to agree that this should be done only in very special circumstances (e.g. isolation required) and under advice of an EMC expert.



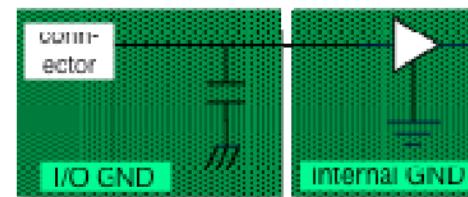
PCB partitioning and shielding

Rationale behind the idea of splitting the GND plane old

- Some examples:
 - Separate GND for sensitive analog circuitry from noisy digital



- separate GND for I/O signals



- high-speed oscillator





PCB partitioning and shielding

Arguments of the opposers of split GND concepts

- most recent publications and Application Notes suggest **not** to split the 0V plane

A well-designed 0V plane on its own layer in a PCB is possibly the most cost-effective EMC design technique that has ever existed, or ever will.

(K. Armstrong,
EMC consultant, [5])

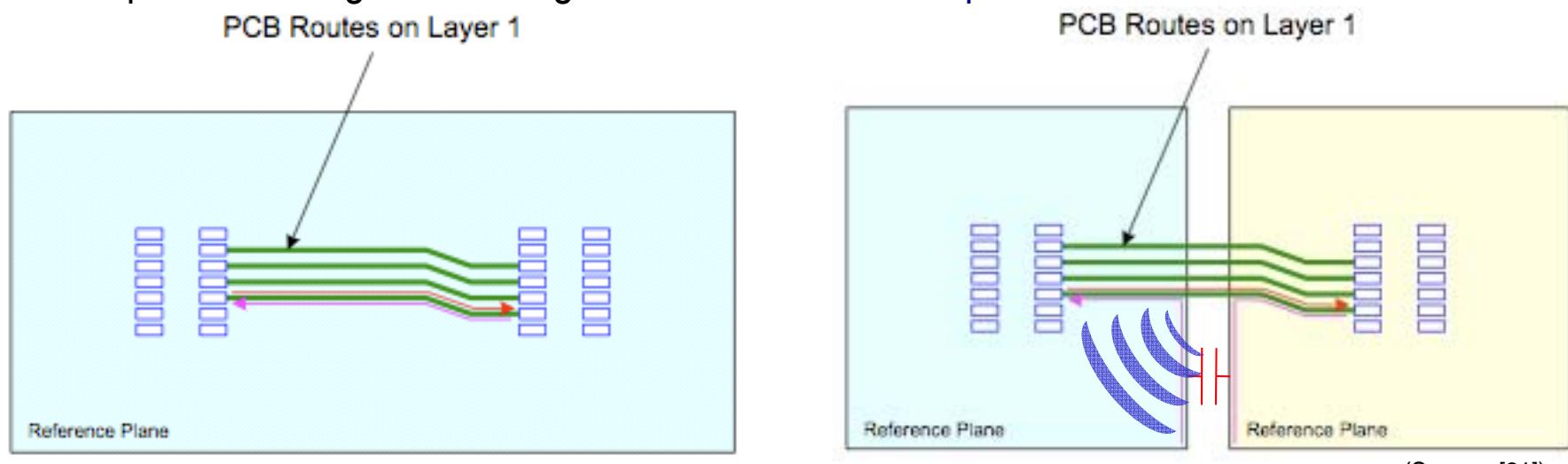
The use of plane cuts, reference plane discontinuities, is one of the most widespread contributors to EMC occurrences that we see.

(SMSC Semiconductor,
world leading supplier of fast communication chips, [21])

PCB partitioning and shielding

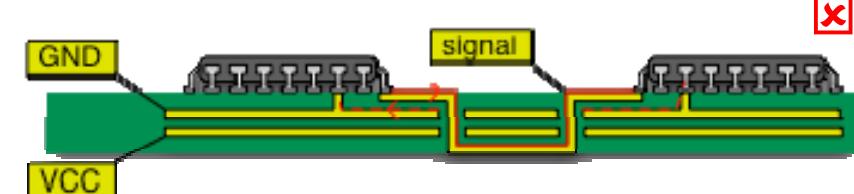
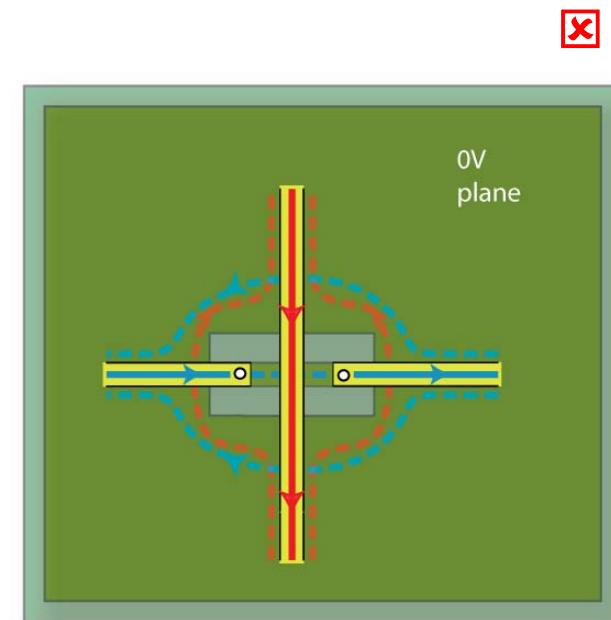
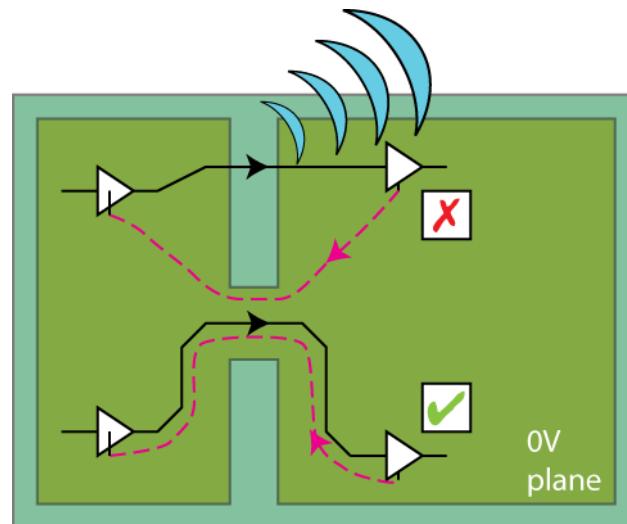
Why splitting a 0V plane can be a bad choice

- every signal has its own return path. Typically, the return path finds its way in the 0V plane just under the signal trace.
- voiding or splitting the plane forces the return path to take a detour
- forward and return path forms a loop. Increasing the loop area inevitably increases its HF radiation (**loop antenna**)
- planes having a HF voltage difference act as a **dipole antenna**



PCB partitioning and shielding

Bad examples



- do not void a reference plane just to route a signal
- always think at the return paths

(Source: [11])

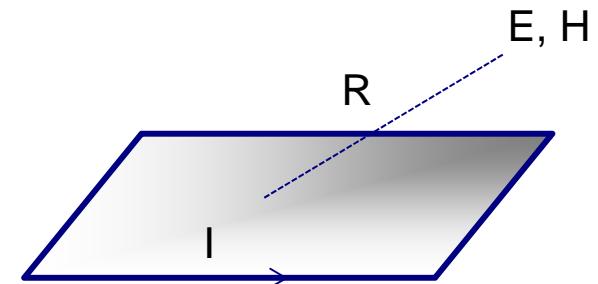
PCB partitioning and shielding

Electromagnetic field radiated by a small current loop

- in the main radiating direction, a PCB trace carrying a current I and forming a loop of area A generates an electromagnetic field at a point distant R in the order of:

$$E \sim \frac{k^2 IA}{4\pi} \sqrt{\frac{\mu}{\epsilon}} \left(\frac{1}{R} \right)$$

$$H \sim \frac{k^2 IA}{4\pi} \left(\frac{1}{R} \right)$$



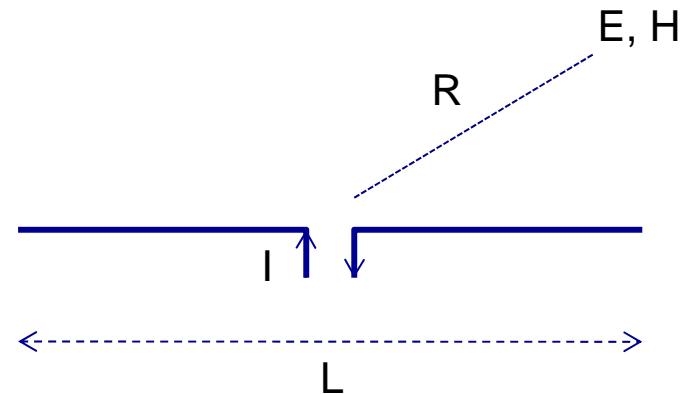
- where:
 - I is the current
 - A is the loop area
 - R is the distance of the measuring point
 - $k = \frac{2\pi}{\lambda} = \frac{\omega}{c}$ (ω is the current's frequency)

PCB partitioning and shielding

Electromagnetic field radiated by a small dipole antenna

- in the main radiating direction, a small dipole antenna fed by a current I and having a length L generates an electromagnetic field at a point distant R in the order of:

$$E \sim \frac{I \cdot L \cdot f}{4\epsilon_0 R}$$

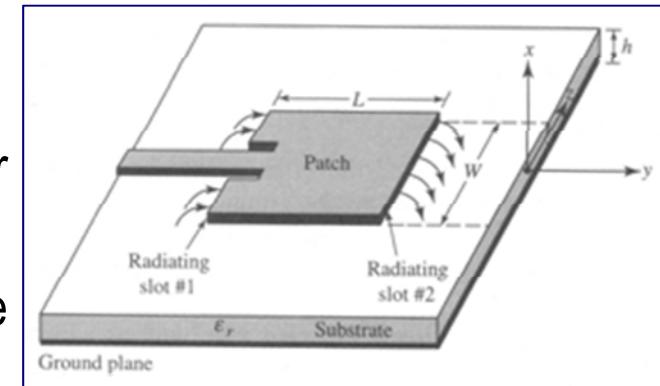


- where:
 - I is the current
 - L is the dipole's length
 - R is the distance of the measuring point
 - f is the current's frequency

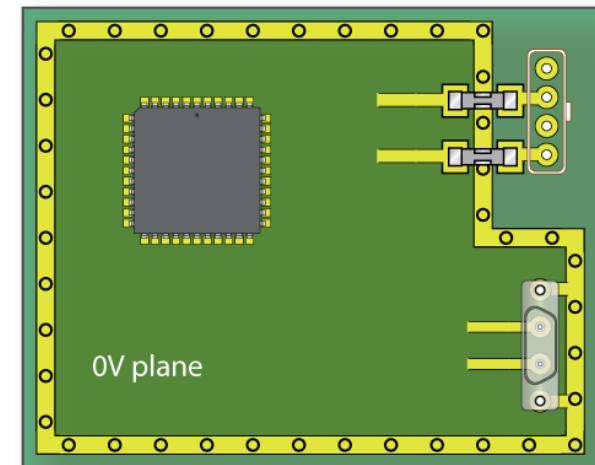
PCB partitioning and shielding

Possible (but rare) issues with continuous reference planes

- if we are unlucky, we could excite the resonant frequency of the plane
- if we have more planes (0V, power) in a multilayer PCB, resonance can build up between them
- the resonant field between two planes can escape along the PCB edges



A patch antenna



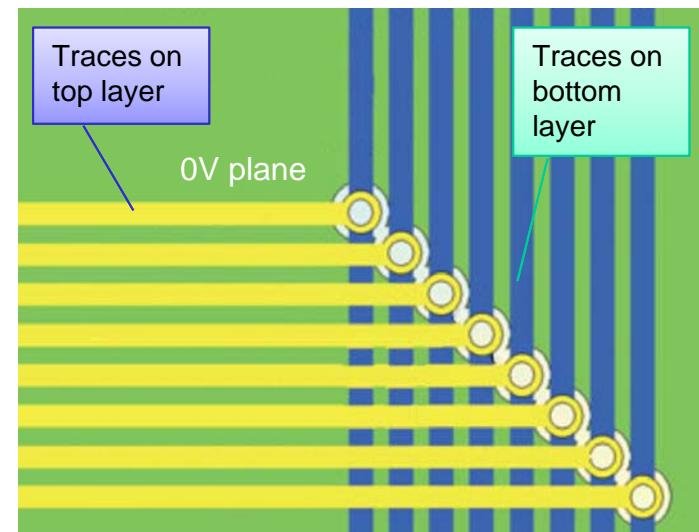
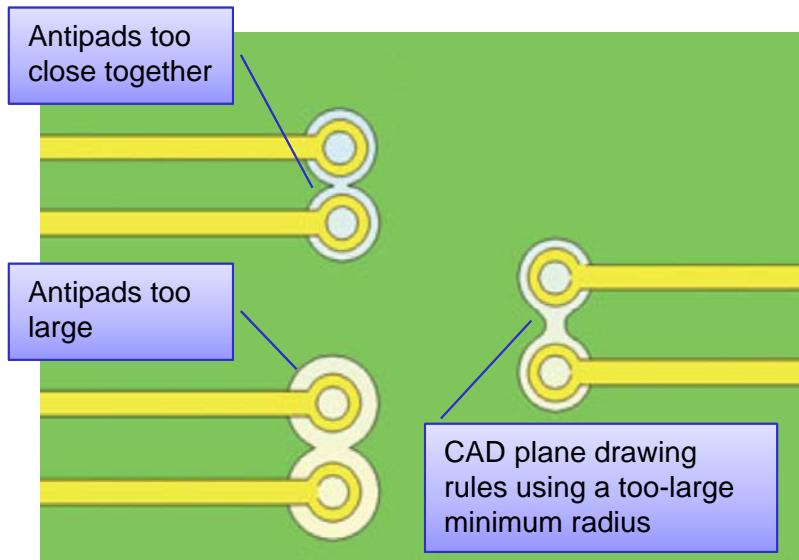
Countermeasures:

- put many vias at short distance ($\lambda/10$) to contact the various 0V planes
- put many bypass capacitors or some shunt resistors between 0V and power planes
- to avoid fringing fields from the PCB edges, put a GND guard ring on the top and bottom layer and connect them with many vias to block emission

PCB partitioning and shielding

Avoid accidental interruptions of reference planes

- do not place antipads too close together



- reduce the number of vias crossing (but not contacting) the reference plane
- reduce the number of THT components

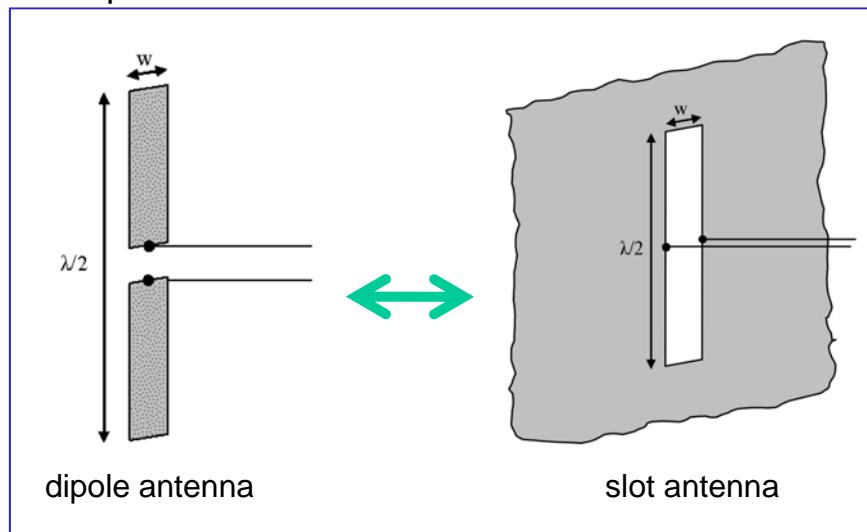
(Source: [5])

PCB partitioning and shielding

Beware of slot antennas

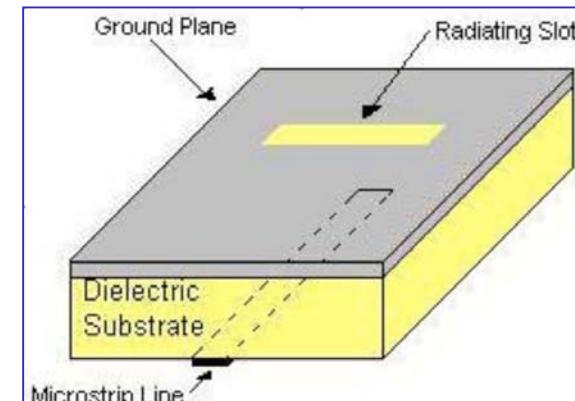
- a slot antenna is an "inverted" dipole, with equivalent radiation characteristics
- it can be excited by an voltage source or an electromagnetic field
- any interruption in a reference plane is a potential slot antenna, when a signal trace carrying an AC signal crosses over/under it

Principle:

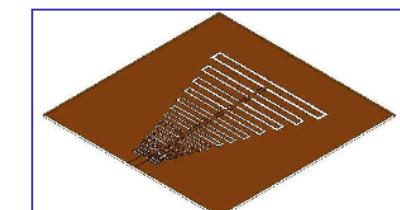


(Source: [22])

Excitation example:



Log-periodic slot antenna on PCB:





PCB partitioning and shielding

A few situations where we may still want to split the planes:

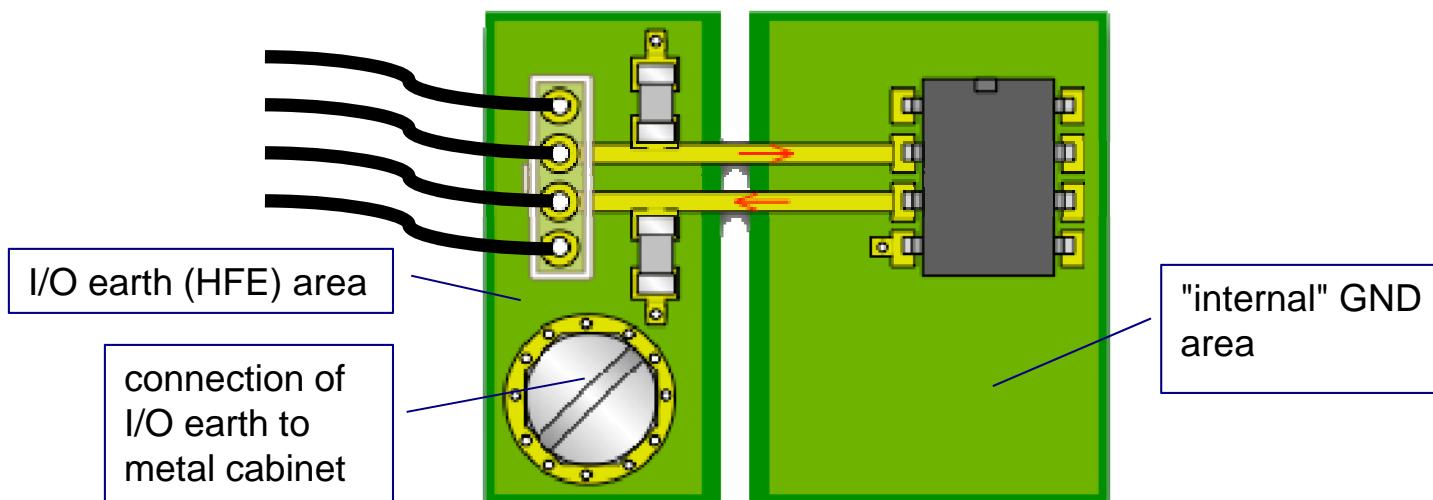
- we want to control where a particular return current travels or where it should never go
 - very high impedance (analog) circuits
 - very small currents (sensor signal conditioning circuits)
 - outputs connected to very noisy, high power (electromechanical) equipment
- isolation needed (safety): optocoupler circuits
- reduction of parasitic C to GND in filters, line transformers

→ consider connecting the different reference planes with a number of small capacitors. They do not influence the low frequency behavior but help reduce the HF emissions due to differential mode noise between the planes

PCB partitioning and shielding

A widespread solution for I/O sections

- Purpose: shunt HF noise (incl. ESD, burst) captured by I/O cables to the metal cabinet with the shortest possible path
- Always provide a nearby signal return path also in the I/O cable



Quiz time

6. Describe some sorts of antennas and how they can involuntarily be created in a PCB

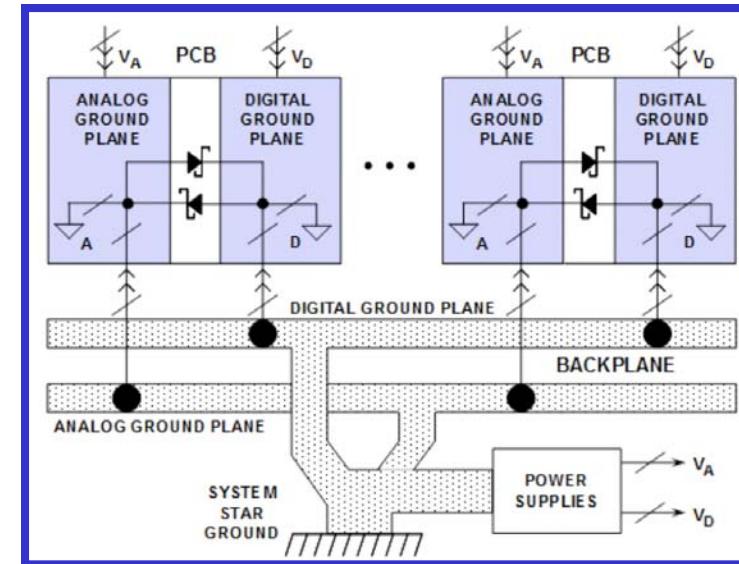
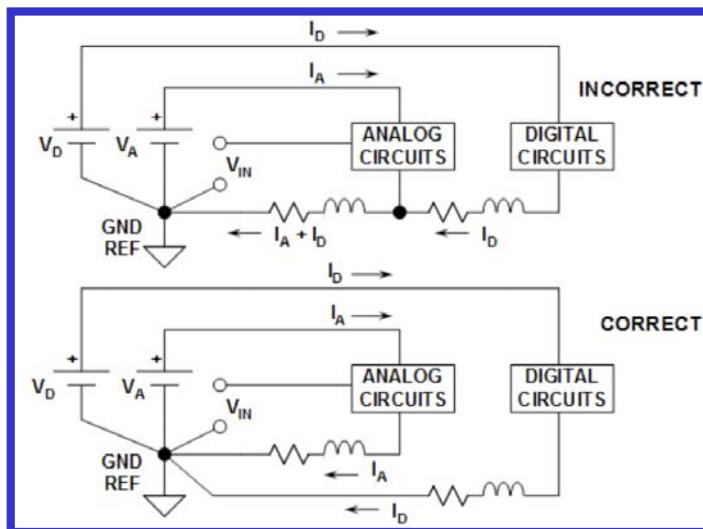
Answer:

- patch antenna (slide 44)
- slot antenna (slide 46)
- dipole antenna (slide 31)
- and generally, antennas formed by PCB traces with missing or far return paths (loop antennas) and antennas formed by attached cables

PCB partitioning and shielding

Mixed signal circuits (1)

- manufacturers of mixed signal components often suggest to implement split GND planes (AGND, DGND)
- the reason is to avoid having digital noise superposed on the analog signal



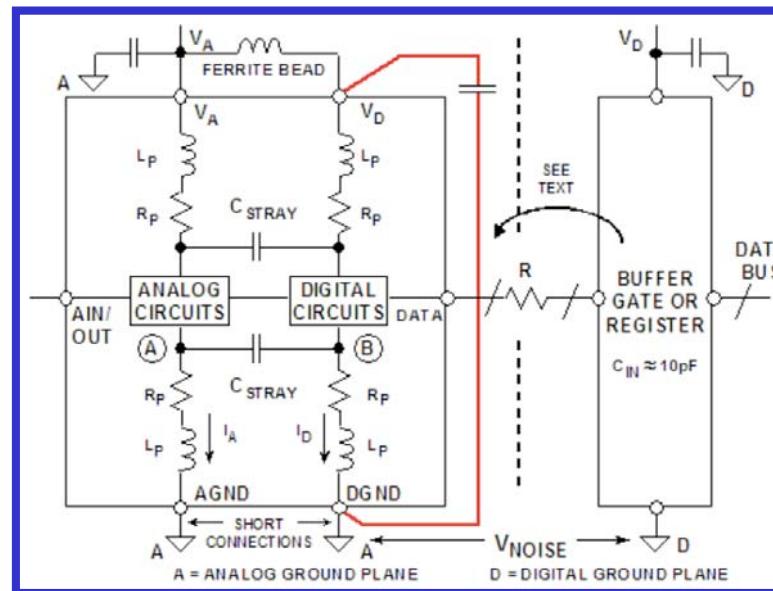
- Analog Devices suggests connecting the two GNDs via anti-parallel shottky diodes or a ferrite bead

(Source: [2])

PCB partitioning and shielding

Mixed signal circuits (2)

- many A/D, D/A converters have separated *analog* and *digital* GND / supply pins
- generally, this is only for practical reasons, because internal bonding has $L \neq 0$ and therefore with a single GND pins, digital noise would couple into the analog section.



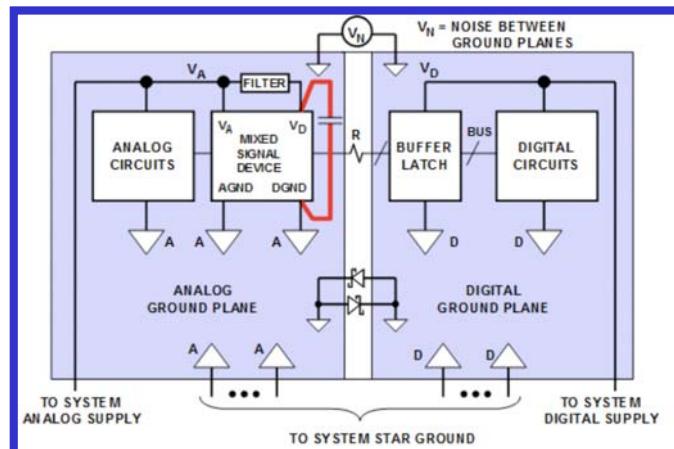
(Source: [2])

But externally, we can tie them together (at AGND) in most cases (next slide)

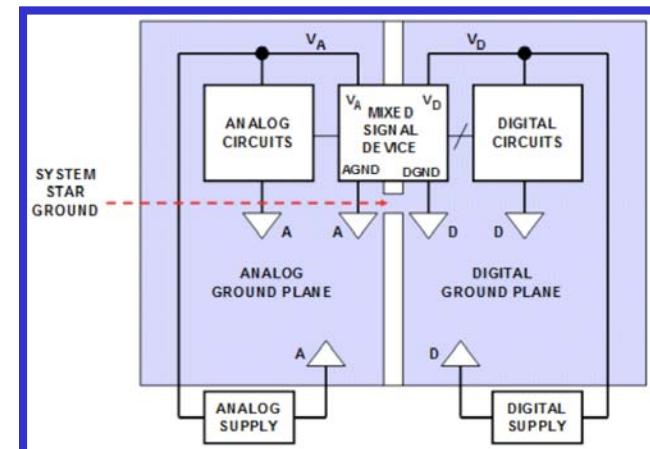
PCB partitioning and shielding

Mixed signal ICs with low digital currents

- connect AGND and DGND pins together to the analog reference plane (the IC is located completely in the analog part (*left*)), or place it over the star connection point between AGND and DGND (*right*) (if we have only one ADC):



PCB with single or multiple mixed signal ICs



PCB with single mixed signal ICs

- further decouple the AVCC with a ferrite bead and its own decoupling capacitor
- to further reduce noise consider adding a digital buffer IC on the digital interface
 - decouple noise from the digital bus (the buffer is connected to DGND)
 - the buffer reduces loading (=> current drawn) on the digital outputs of the ADC (use series resistors to further reduce the current)

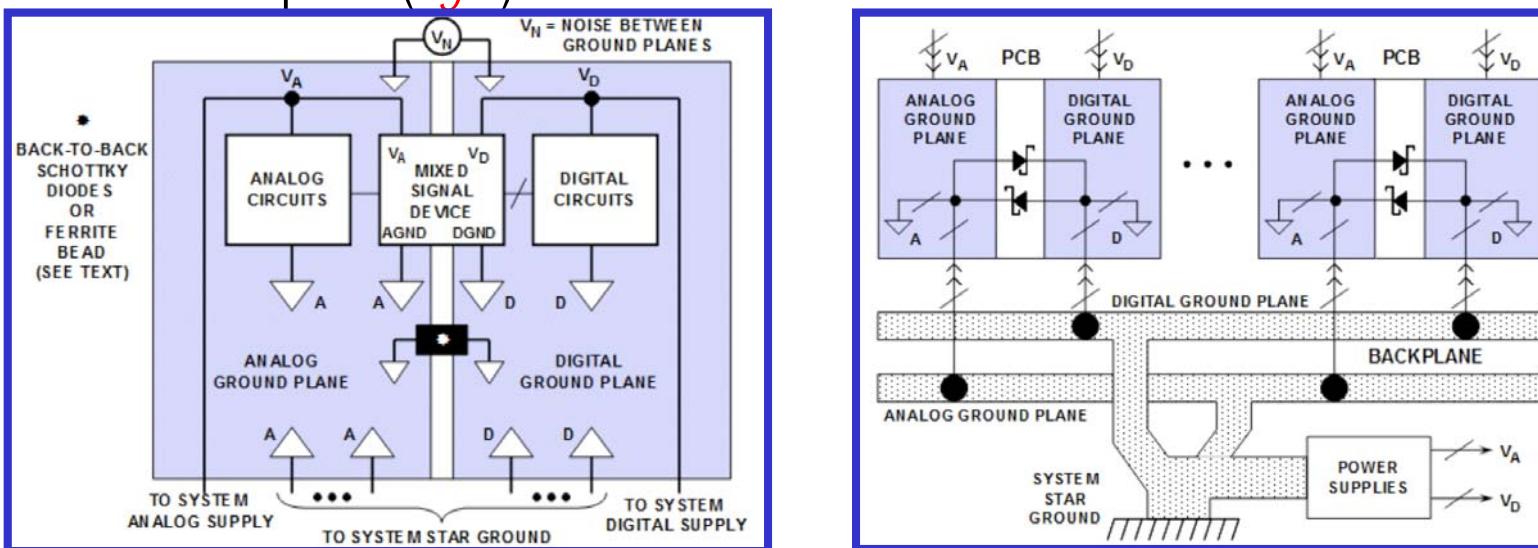
(Source: [2])

PCB partitioning and shielding

Mixed signal ICs with high digital currents and/or multicard systems

- connect AGND and DGND pins to the respective reference plane (*left*).
- this scheme works only for ICs designed with well isolated analog/digital circuits
- tie AGND and DGND together in a "star point". In multicard systems this can be at the backplane (*right*)

(Source: [2])



- always refer to the IC manufacturer's recommendations, use evaluation boards!

PCB partitioning and shielding

Mixed signal circuits – sampling clock circuits (1)

- jitter on the sampling clock severely deteriorates the SNR of an ADC
- SNR of an ideal ADC (infinite resolution) exposed to clock jitter:
where f is the signal frequency, t_j is the sampling clock jitter

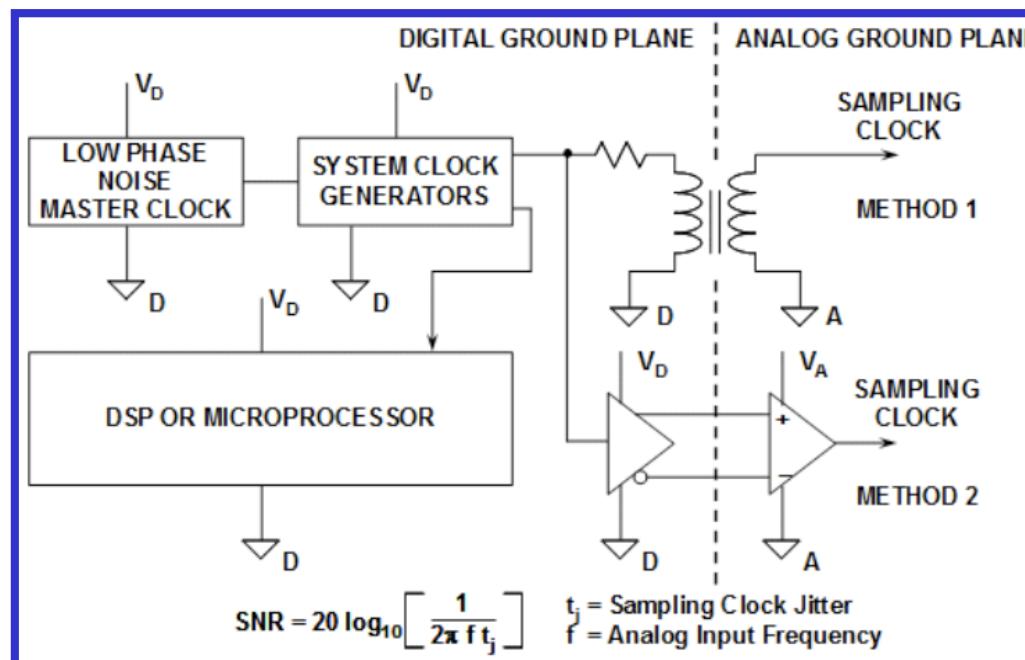
$$SNR = 20 \log_{10} \left[\frac{1}{2\pi \cdot f \cdot t_j} \right]$$

- noise superposed to a clock signal translates into clock jitter
- the best solution is to create the clock locally (in the analog, low noise section)
- use a low jitter oscillator such as a quartz crystal. Beware from programmable (PLL) oscillators.

PCB partitioning and shielding

Mixed signal circuits – sampling clock circuits (2)

- if the clock comes from the digital section, try to minimize its superposed noise (against AGND) by transmitting it over a differential line (originating directly at the oscillator) and/or using isolation (transformer, optocoupler)



(Source: [2])

- we will see more on clock jitter ahead (digital circuits)...



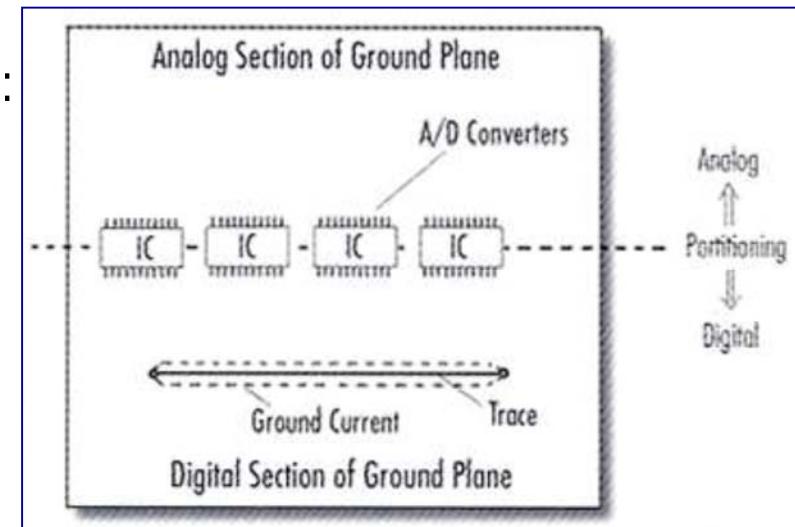
PCB partitioning and shielding

Mixed signal circuits – more suggestions

by Henry Ott, a renown EMC consultant (www.hottconsultants.com):

- split the power (VCC) plane: AVCC, DVCC
- **generally avoid splitting the GND plane**
- instead, partition carefully the components: analog and digital in different PCB areas
- noisy digital return currents flow directly under the respective signal traces and do not propagate inside the analog section
- do not route digital signal traces in the analog zone
- in case of doubt you can always design a PCB with split grounds, but provide means for connecting the two planes together at intervals of $\lambda/10$ with jumpers or zero ohm resistors. Laboratory tests will tell which solution is better.

(Source: [19])

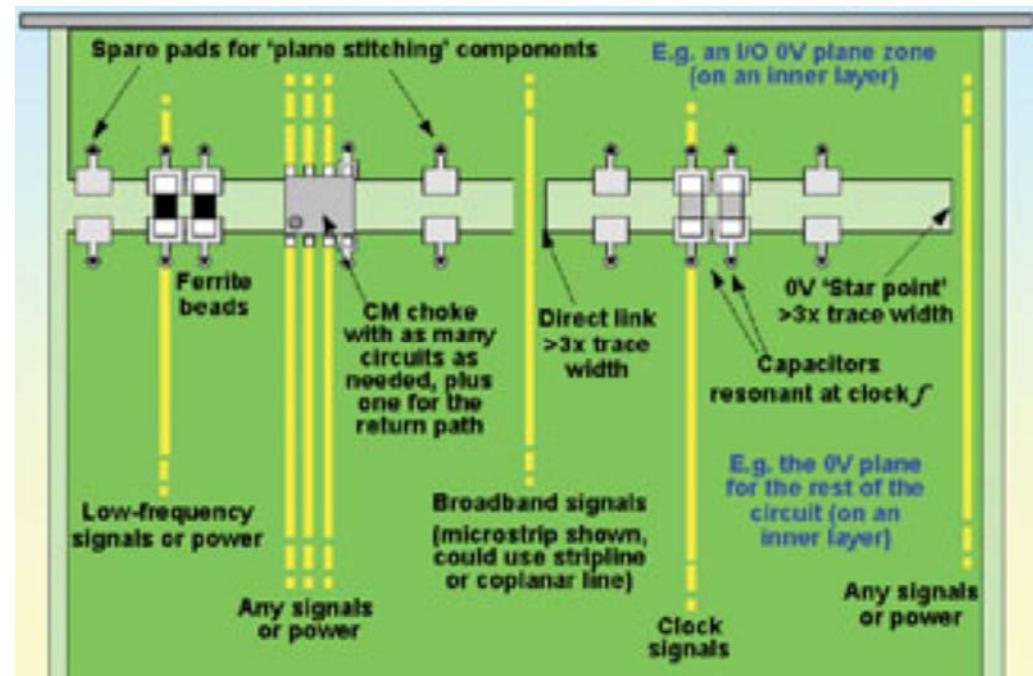




PCB partitioning and shielding

How to cross a plane split with signals

- always provide a nearby path for the return signal
- it is a good place to use a common mode choke, an optocoupler
- it is also a good place to add signal filters (π , LC, etc)
- or provide a "bridge" between the two planes (see center of the figure)
- use differential signal lines



(Source: [5])



Quiz time

7. PCBs with separate copper areas for different grounds (analog/digital):

- are a good idea (explain why)
- are not a good idea (explain why)
- should be used only under special circumstances, i.e. when: _____

- *when dealing with sensitive analog circuits (high impedance, very small signal)*
- *when outputs are connected to very noisy, high power (electromechanical) equipment*
- *when isolation is needed (safety reasons/regulations)*
- *to reduce parasitic C to GND in filters, line transformers*

And only if we are very sure about what we're doing or under an EMC expert's advice

PCB partitioning, shielding, image planes

Conclusions

- the first and best guess is: make one single reference plane
- read the recommendations of the IC manufacturers. Purchase evaluation kits and see how their PCB layout is made
- be skeptical about Application Notes dating prior to 2000-2003, suggesting a partitioned ground plane. Exceptions:
 - noisy I/O sections
 - analog input sections with low noise or low leakage current requirements
- it is more important to carefully partition the components (analog and digital circuits should be placed in different PCB regions). Avoid placing digital signal lines inside the analog zone.
- make your PCB design so that it can be configured to various solutions (split or common ground plane, various kinds of short-lays between the planes).
- Tests will determine the most favorable layout concept

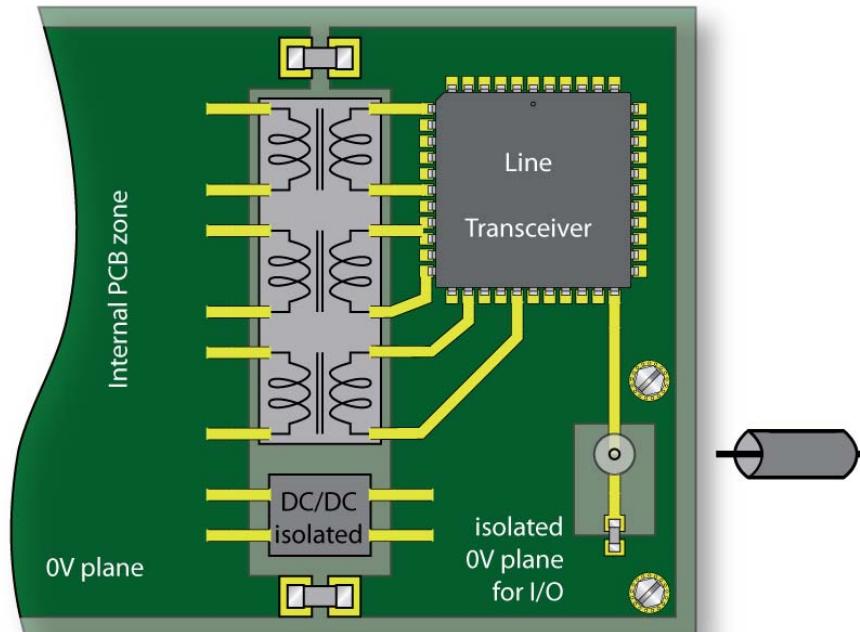
An Application Case

Ethernet LAN (10Base2 and 100BaseTx) interfaces

PCB partitioning and shielding

An application case: Ethernet interface

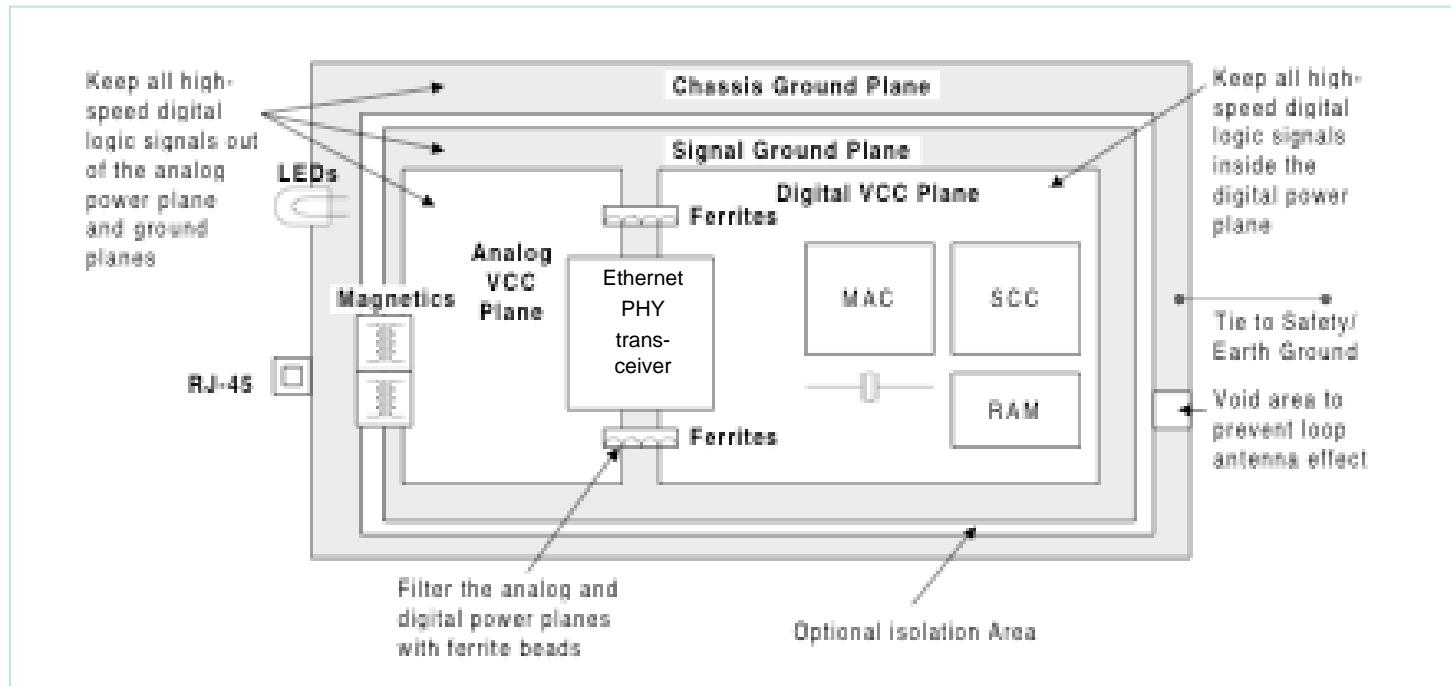
- Ethernet uses isolation between network cable and controller/equipment
- 10Base2 standard is for coaxial cable (**below**),
- 100BaseTx is for twisted pair cable (RJ45)(*next slides*)



PCB partitioning and shielding

An application case: Ethernet interface

- A chip manufacturer's layout recommendation for a fast Ethernet interface

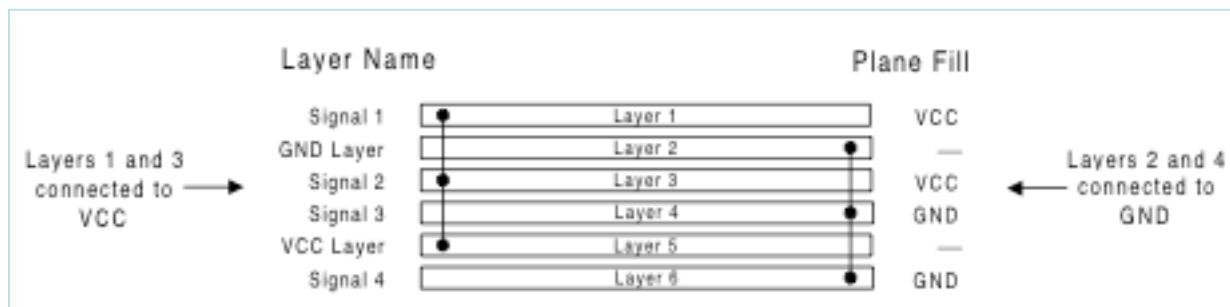


(Source: LevelOne/Intel)

PCB partitioning and shielding

"Signal layer filling" technique (*suggested by a chip manufacturer*):

"When possible, fill in unused areas of the signal planes with solid copper and attach them with vias to a VCC or ground plane that is **not** located adjacent to the signal layer. This technique can improve capacitive coupling of the power planes"

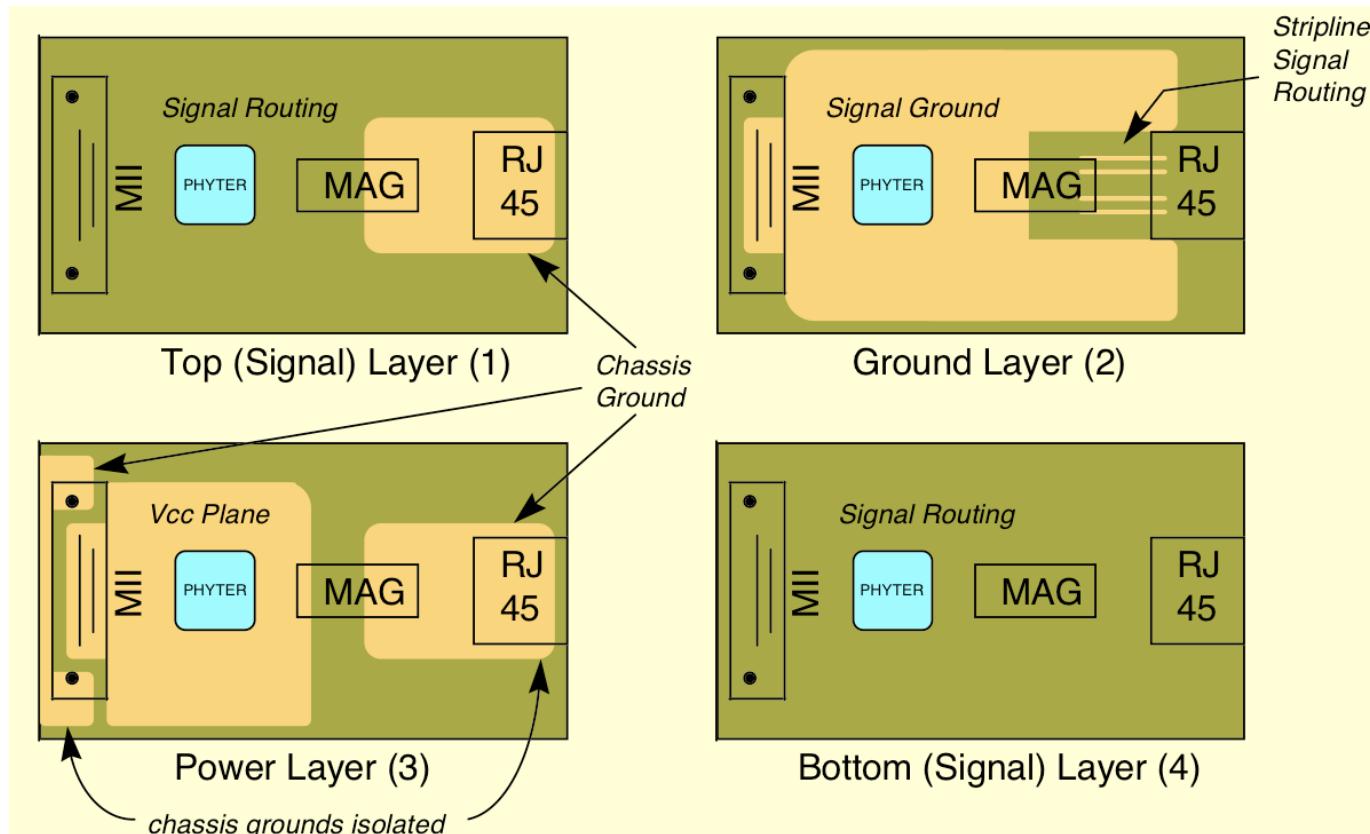


(Source: LevelOne/Intel)

PCB partitioning and shielding

Application case: Ethernet interface (from another IC manufacturer)

- Another chip manufacturer's layout recommendation for a fast Ethernet interface



(Source: National Semiconductor)

Exercises

9. The return current of a signal is always on the nearest conducting plane, regardless of its DC voltage?

- correct
- incorrect



Exercises

10. What is common mode noise and how can it be avoided?

Answer:

Common mode noise is noise that's present with the same polarity on a signal and its return line. Therefore, the electromagnetic field generated by the common mode current on the pair of lines does not cancel at far distance. When GND noise (voltage drop on the GND connection) is present, then this generally translates into common mode noise on components attached to GND.

Possibilities to reduce common mode noise:

→ [next slide]

Exercises

(cont'd)

Possibilities to reduce common mode noise:

- reduce the impedance on the GND path, e.g. by using a continuous GND plane that acts as a good return path for the signals
- avoid false (parasitic) return paths : if they exist, then the sum of the currents on the "true" signal and return path is no longer zero, meaning that there is a common mode component on the these paths.
- shield against external noise sources (electromagnetic fields)
- avoid asymmetries (parasitic loading) on differential lines

Generally, differential signaling is more immune to common mode noise.

Bibliography

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MASTER OF SCIENCE
IN ENGINEERING

ADVANCED ELECTRONIC DESIGN

EMC, signal integrity, grounding and power supply routing,
decoupling, transmission lines, simulation tools

Dipl.-Ing. Ricardo Monleone



Topics of this series of 3 lessons

PCB Design

- Lesson 1:
 - Introduction
 - Partitioning, filtering
 - Shielding
 - Image planes
 - Continuous vs split GND concepts
 - Mixed signal circuits
- Lesson 2:
 - Decoupling
 - Transmission lines
 - Guard rings
 - Crosstalk, Ground bounce
 - Differential signalling
 - Terminations
 - Clock distribution: clock skew and clock jitter
- Lesson 3:
 - Place & route strategy
 - Components selection
 - Layer stackups
 - Multicard systems, backplanes
 - Enclosures, connectors and cables
 - ESD + Burst protection
 - 2-layer PCBs
 - Design for testability
 - Prototyping

Decoupling

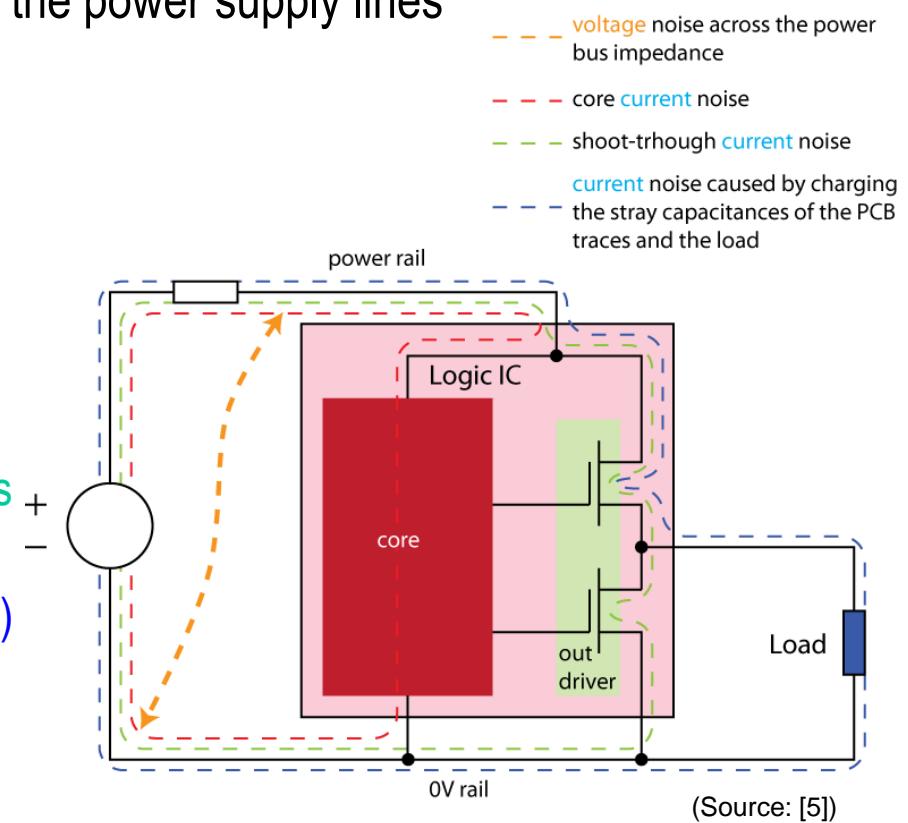
What is decoupling and why do we need it?

We need to reduce the fluctuations on the power supply lines

- to reduce emissions
- to guarantee correct circuit operation

The fluctuations in the power line
are due to:

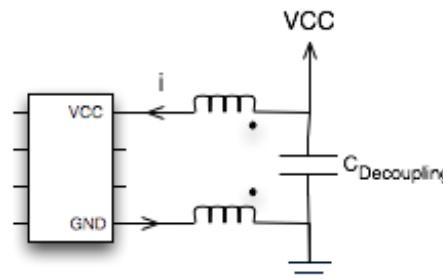
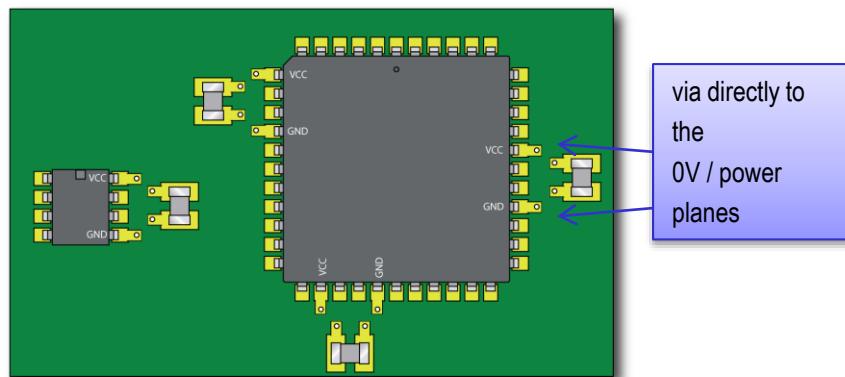
- internal switching noise of the ICs
- vertical shoot-through of output drivers
- high charging/discharging currents of capacitive loads (PCB trace, IC inputs)
- Noisy currents emit magnetic fields
- Noisy voltages emit electric fields



Decoupling

To reduce emissions from the power supply circuits

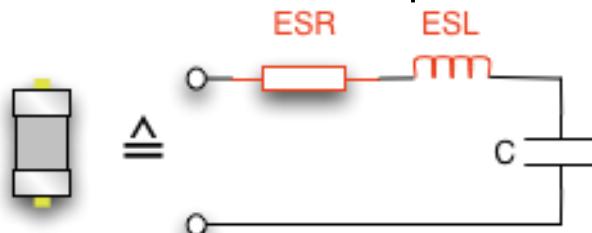
- reduce the amplitude of the voltage fluctuations
 - place decoupling (bypass) capacitors ("decaps") between VCC and GND
 - add one for every power pin of every IC (and even some more...)
- reduce current loop areas
 - reduce connection length between ICs and decoupling capacitors
 - in multilayer PCBs, place 0V and VCC planes adjacent (near)
 - take benefit from mutual inductance in the connection lines to the decap to reduce their voltage drop (impedance) (this is best achieved in multilayer PCBs with GND+VCC layers)



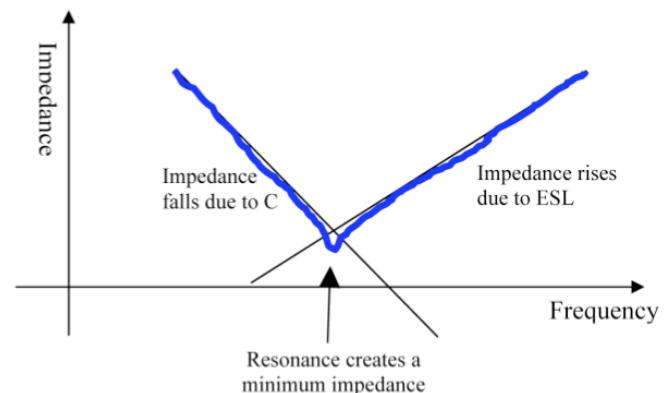
Decoupling

Capacitor series resonance

- equivalent circuit of a capacitor:



- ESL + C form a series resonant circuit: $\omega_{res.} = \frac{1}{\sqrt{LC}}$
→ increasing C reduces $\omega_{res.}$!
- above $\omega_{resonance}$ the capacitor behaves like an inductor!
- ESL depends on the capacitor case type and size
- minimize PCB trace length (inductance) to decoupling capacitors as this adds to the ESL
- in multilayer PCB's, keep GND and VCC layers at a short distance to the top (component layer) to reduce via lengths (L, loop areas)



Decoupling

Capacitor series resonance

- examples of **series resonant frequency** of capacitors:

$$f_{res.} = \frac{1}{2\pi\sqrt{LC}}$$

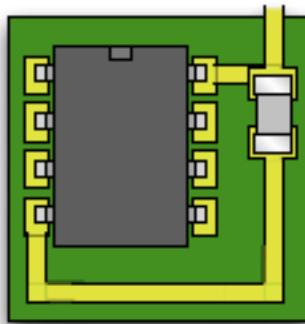
| Capacitor value | THT case (6mm leads) ESL ≈ 3.75 nH | SMD 0805 case ESL ≈ 1 nH |
|-----------------|---------------------------------------|-----------------------------|
| 1.0 µF | 2.6 MHz | 5 MHz |
| 100 nF | 8.2 MHz | 16 MHz |
| 10 nF | 26 MHz | 50 MHz |
| 1 nF | 82 MHz | 159 MHz |
| 100 pF | 260 MHz | 503 MHz |

- rule of thumb: 1 cm of thin wire (0.5mm Ø) or 0.25 mm wide PCB trace has an L of 7...10 nH
=> use smaller components, with shorter leads

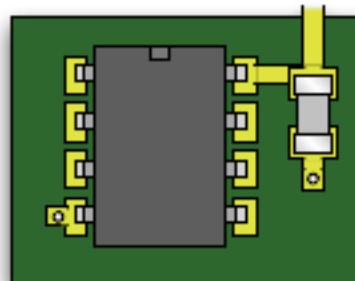
Decoupling

Also reduce external wiring length

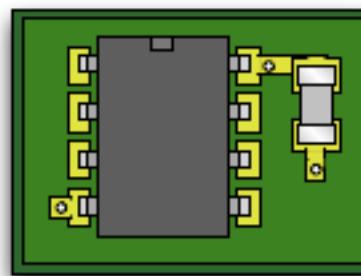
- reduce additional L due to PCB traces that add to the capacitor's ESL
- reduce area of the loop formed by the capacitor and the IC
- examples of positioning and routing of a decoupling capacitor:



BAD



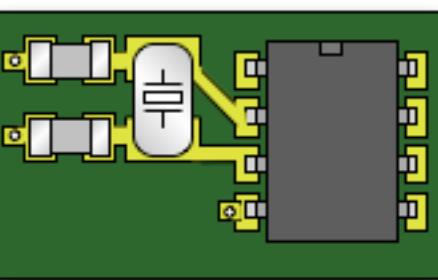
GOOD



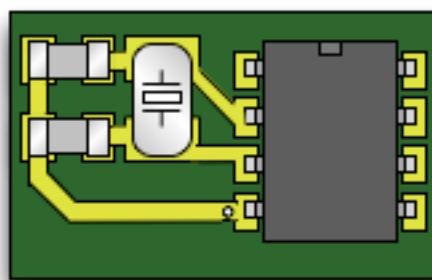
Oscillator circuits

Similar considerations apply as with decoupling

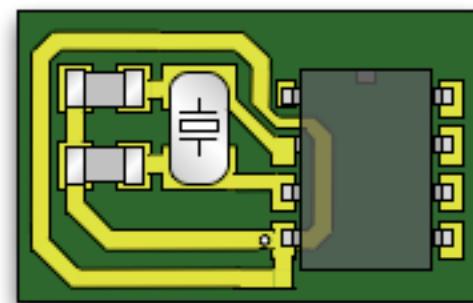
- reduce the area of the oscillator circuit
- keep connections short
- keep noise from GND layer out of the oscillator circuit



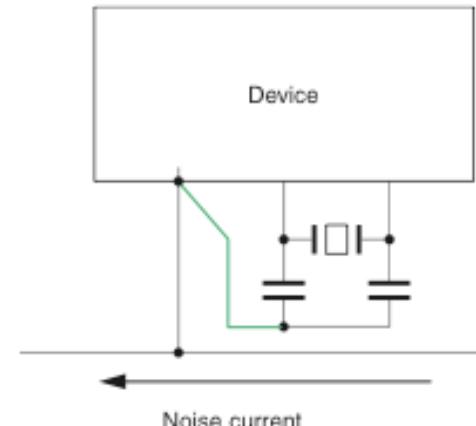
FAIR



GOOD



BEST

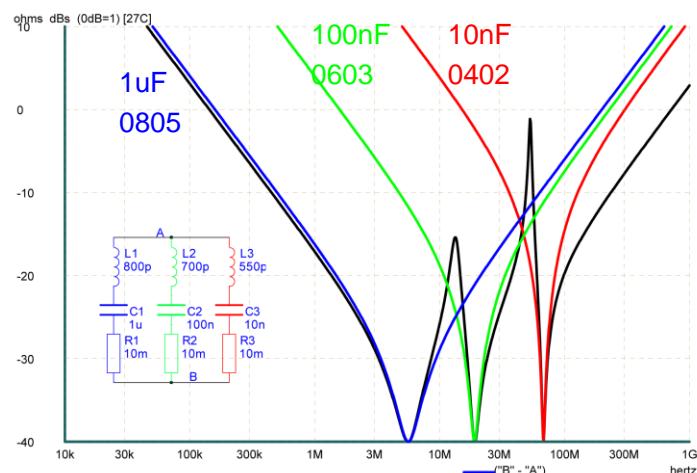


- examples of positioning and routing of an oscillator circuit:

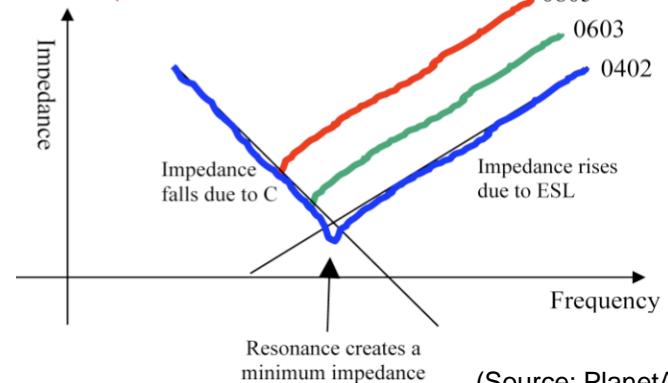
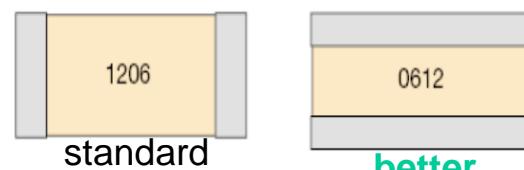
Decoupling

How to choose a decoupling capacitor

- use MLCC (multilayer ceramic) capacitors: X7R, Z5U:
 - low loss
 - compact size
- use the smallest possible SMD case
 - lower equivalent series inductance (ESL)
 - special cases with low ESL are available:
- commonly used values: 100nF, 10nF, 1nF



| Ceramic (EIA Class II) Capacitor Code | | | | | |
|---------------------------------------|-----------------------|---------------|------------------------|---------------|-----------------|
| Letter Symbol | Low Temp. Requirement | Number Symbol | High Temp. Requirement | Letter Symbol | Max. ΔC over ΔT |
| Z | +10°C | 2 | +45°C | A | +/- 1.0% |
| | | 4 | +65°C | B | +/- 1.5% |
| Y | -30°C | 5 | +85°C | C | +/- 2.2% |
| | | | | D | +/- 3.3% |
| X | -55°C | 6 | +105°C | E | +/- 4.7% |
| | | 7 | +125°C | F | +/- 7.5% |
| | | | | P | +/- 10.0% |
| | | | | R | +/- 15.0% |
| | | | | S | +/- 22.0% |
| | | | | T | +22% / -33% |
| | | | | U | +22% / -56% |
| | | | | V | +22% / -82% |

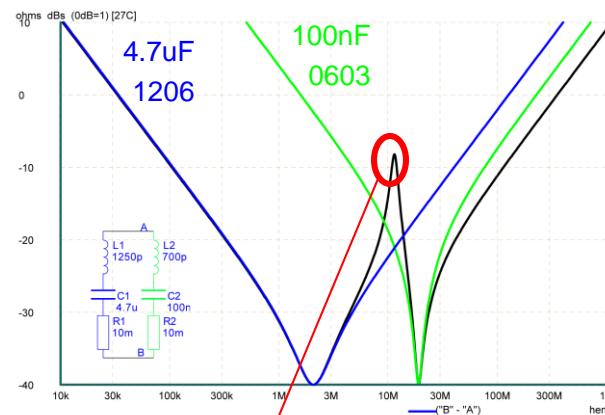


(Source: PlanetAnalog.com)

Decoupling

Paralleling decoupling capacitors

- the idea: above its ω_{res} , a single capacitor has an increasing Z
=> reduce this Z at higher frequencies with a smaller C in parallel



- the risk: parallel resonance: the equivalent circuit is now of 4th order and $Z_{\text{TOT}}(\omega)$ has 2 zeros and 3 poles. Network theory says that they alternate on the frequency axis. Therefore, between the series resonance of each single capacitor we have a frequency where Z becomes **very high**.

Parallel decoupling capacitors

how to mitigate parallel resonance:

- use capacitors with higher ESR (or add a small series R): this extra loss adds more damping to the parallel resonance (less Q)
 - NPO and COG dielectrics (used in high frequency capacitors) have very low losses and are therefore not a good choice for decoupling
- when paralleling capacitors, use all capacitors of the same capacitance
- put a great number of capacitors in parallel, with closely spaced series resonance frequencies

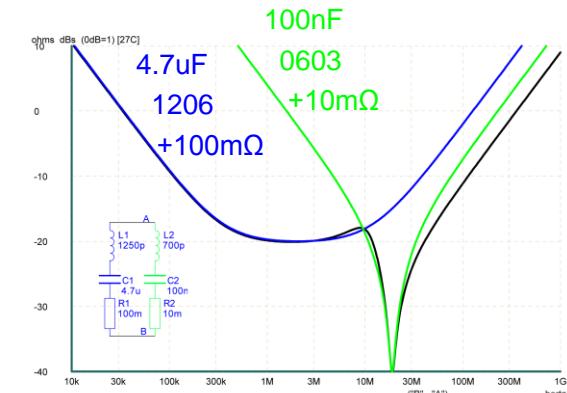


Figure 5L Example of using ten identical 10nF decaps in parallel
(assuming they share the small power plane of a layout similar to Figure 5F)

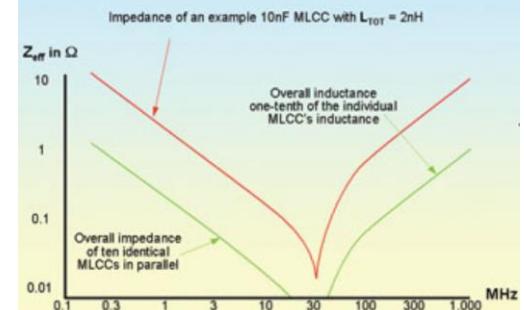
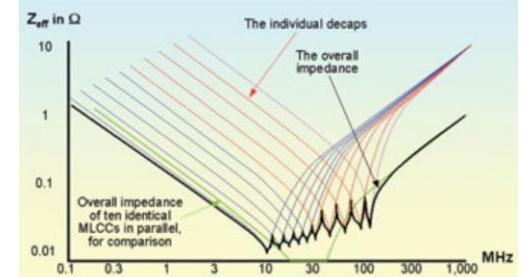


Figure 5N Example of ten parallel decaps with different values
100, 56, 33, 27, 15, 10, 5.6, 3.3, 1.8 and 1nF, each with L_{TOT} = 2nF
(assuming they share the small power plane of a layout similar to Figure 5F)

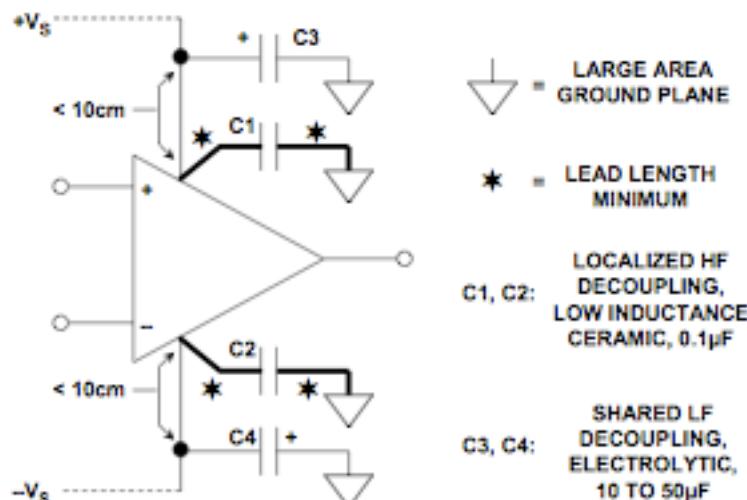


(Sources: PlanetAnalog and [5])

Parallel decoupling capacitors

still recommended in analog circuits:

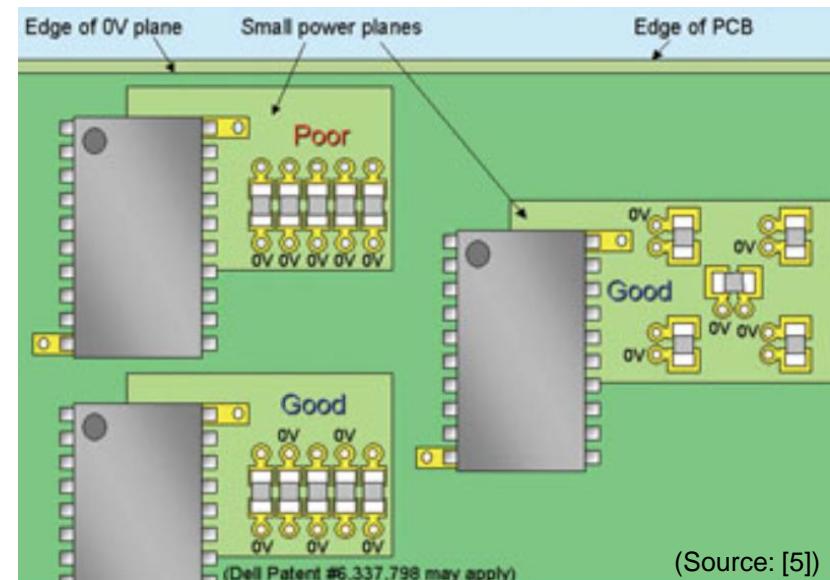
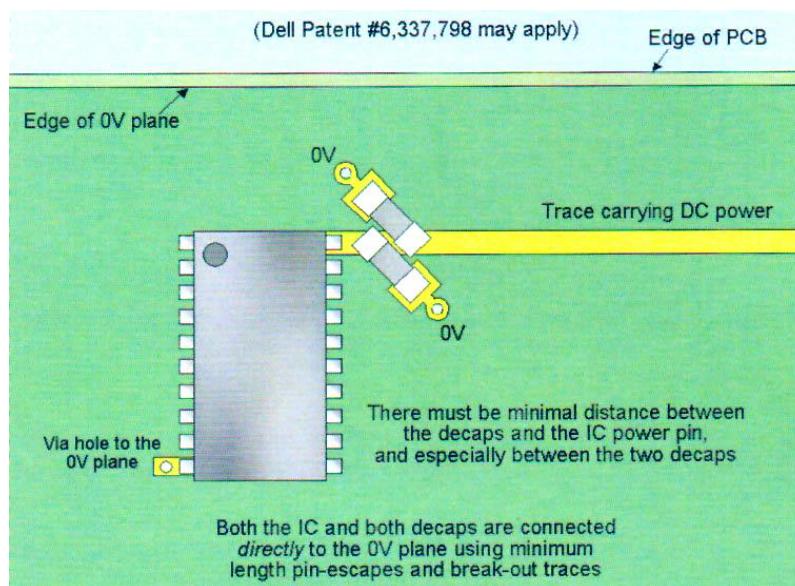
- circuits operating at frequencies below a few MHz are not affected by high frequency parallel resonances
- use the combination of:
 - a large C ($10\mu F \dots 50\mu F$) to decouple noise introduced by the power supply (PSRR)
 - a smaller C ($100nF$) as a return path for higher frequency noise generated by the IC is recommended by analog IC manufacturers [1]:



Decoupling

Parallel decoupling capacitor placement

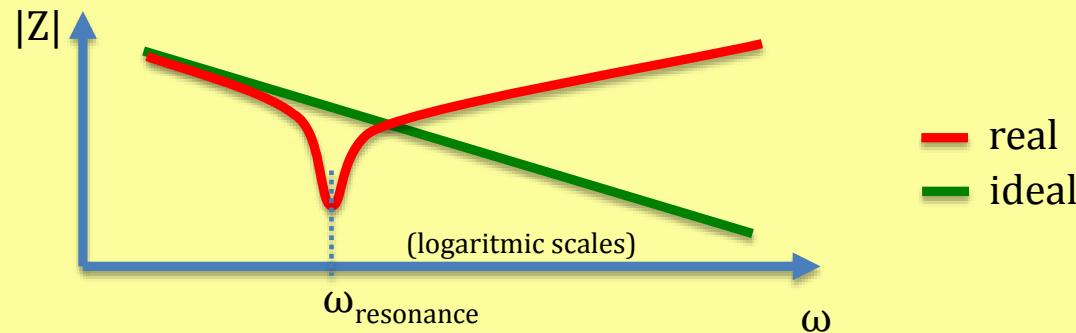
- if possible, take advantage of magnetic flux cancellation that reduces ESL when placing multiple capacitors very close to each other with **opposite** current flow



Quiz time

1. Draw the frequency response $Z(\omega)$ of:
 - an ideal capacitor
 - a real capacitor

Answer:



2. Explain the reason of this difference

Answer:

A real capacitor has parasitic elements, such as a series inductance and a series resistance. The capacitance and its series inductance form a resonant circuit. At the series resonance frequency, $|Z|$ reaches its minimum value. At frequencies above the resonance, the impedance of the inductance prevails. Here the real capacitor acts as an inductor.

Decoupling

Intrinsic capacitance between GND and VCC planes of a PCB

- in multilayer PCBs, placing the VCC and GND planes adjacent and very close ($d < 100\mu m$) produces a good intrinsic decoupling capacitance
- $C = \epsilon_0 \epsilon_r \frac{A}{d}$ (*example : FR4 with $d = 100\mu m$ $\rightarrow C \approx 37 pF/cm^2$*)

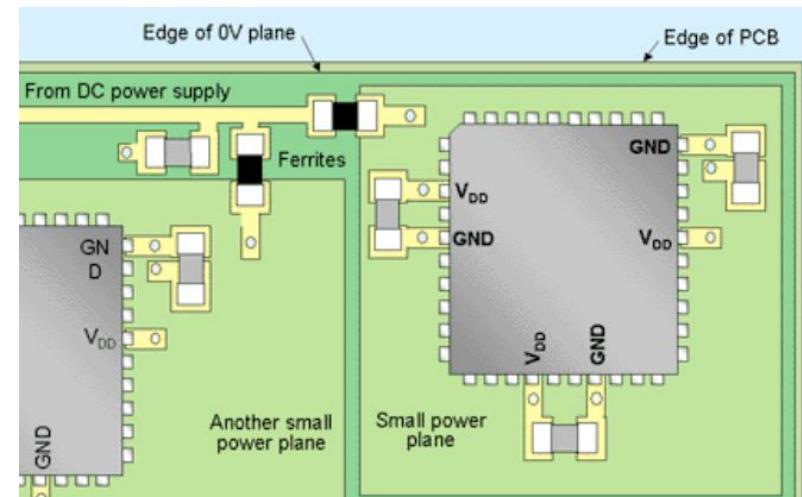
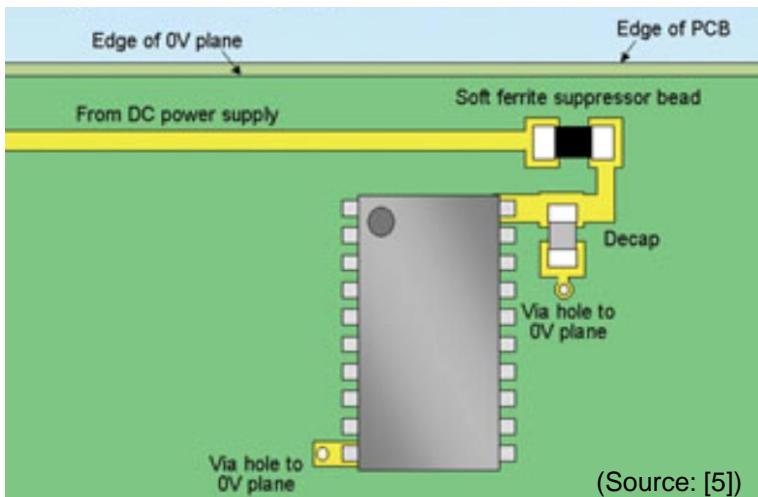
Avoid the risk of resonance of the VCC-GND cavity

- reducing the distance between VCC and GND planes (modify stackup) reduces their cavity's Q
- resize the VCC area so that resonant frequencies along its length L and its width W do not overlap. \Rightarrow Choose $L/W = \text{irrational number}$.
- spread many decoupling capacitors all over the PCB (spaced at $\leq \lambda/4$ of the highest frequency of concern)
- partition the VCC plane into smaller planes, connected through π -filters
 \Rightarrow shift plane resonance to higher (uncritical) frequencies
- if multiple reference planes of the same type (GND or VCC) exist, contact them with many vias (spaced at $< \lambda/10$ of the highest frequency of concern)
- add some damping (R, series R-C or capacitors with higher ESR) between GND and VCC

Decoupling

Ferrite beads or RF suppressors on VCC

- can help further suppress VCC noise from ICs
- useful when VCC is already partitioned
- L or π filters can be implemented with ferrite beads
- T filters can be implemented with pass-through filters
- do not use normal inductors (resonant circuit!)





Transmission lines

A PCB trace is *not* an ideal conductor (1)

- a piece of PCB trace with a length z has a resistance:

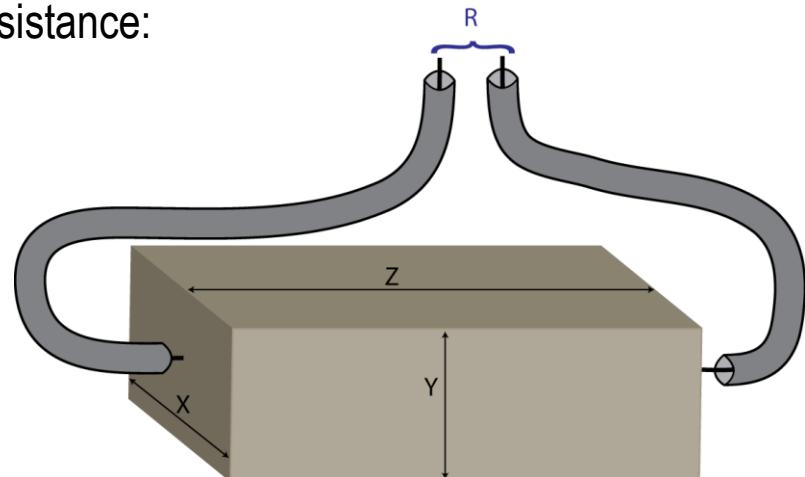
$$R = \rho \frac{Z}{X \cdot Y} \quad (\rho: \text{resistivity } [\Omega\text{m}])$$

- example:

$$Y = 35 \mu\text{m}, \quad X = 0.254 \text{ mm (10 mils)}$$

$$\rho = 0.0175 \Omega \frac{\text{mm}^2}{\text{m}} \quad (\text{copper})$$

$$\Rightarrow R = 19 \text{ m}\Omega/\text{cm}$$

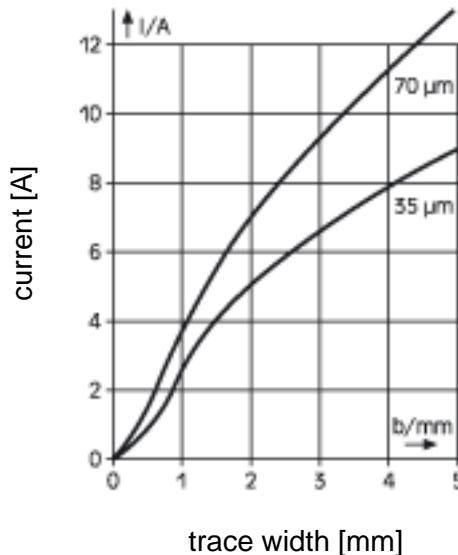


- when driving low impedance loads, the trace R forms with this load a resistive voltage divider. This can be critical for precision analog circuits.

Transmission lines

A PCB trace is *not* an ideal conductor (2)

- current flow produces a temperature rise. Trace widths must be dimensioned accordingly!
- **example:** typical recommended trace widths, for $Y = 35\mu\text{m}$ and $70 \mu\text{m}$, for a max temperature rise of 60°C



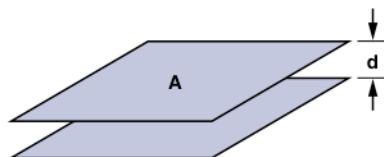
(Source: www.db-electronic.com)

Transmission lines

Intrinsic capacitance *(already seen)*

- the capacitance formed by two copper areas on adjacent PCB layers is:

$$C = \epsilon_0 \epsilon_r \frac{A}{d} \quad (\text{example : FR4 with } d = 100\mu\text{m} \rightarrow C \approx 37 \text{ pF/cm}^2)$$



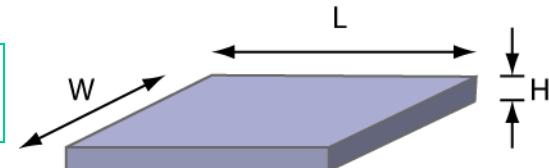
Transmission lines

Inductance

- a PCB trace has a self inductance L.

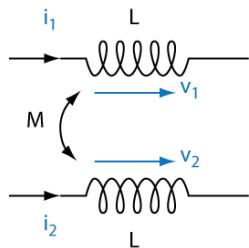
Approximate formula for a copper strip of length L *when no GND plane is present underneath:*

$$\text{inductance} = 0.0002L \left[\ln \frac{2L}{W+H} + 0.2235 \left(\frac{W+H}{L} \right) + 0.5 \right] \quad (\text{in } [\mu\text{H}])$$



- two parallel PCB traces have a mutual inductance M.

This is the case for a signal trace and its return path in the adjacent GND layer



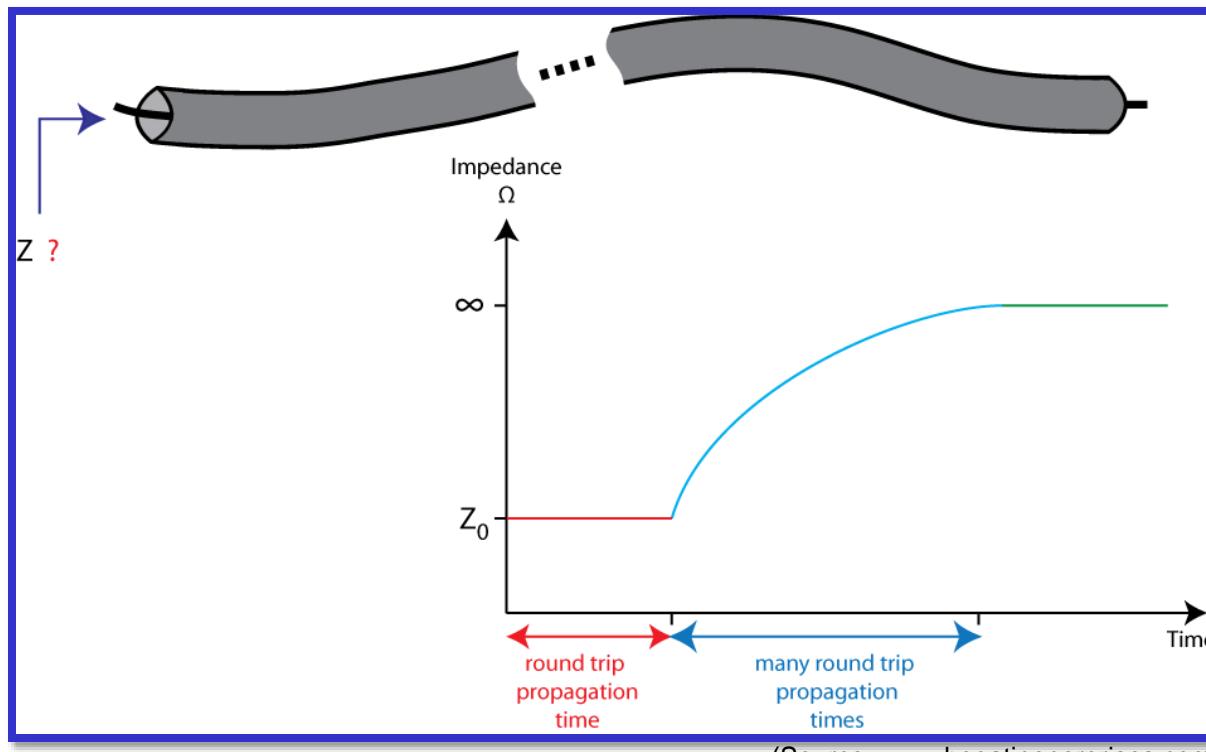
$$\begin{aligned} V_1 &= L \frac{di_1}{dt} + M \frac{di_2}{dt} \\ V_2 &= L \frac{di_2}{dt} + M \frac{di_1}{dt} \end{aligned}$$

- if $i_1 = -i_2$ then $V_1 = -V_2 = (L - M) \frac{di}{dt}$. The term $(L - M)$ is called **mutual partial inductance**.
- if the mutual coupling is good (reference plane carrying the return current is very close to the signal trace) then $(L - M)$ is very small and ΔV due to inductance is very small.
- this is **another good reason** for using continuous reference planes adjacent to each signal plane!

Transmission lines

What is the characteristic impedance Z_0 of a transmission line?

- it is the impedance measured at one end of the line before the signal makes a round trip in the line
- if the line's length is ∞ we will measure Z_0 forever

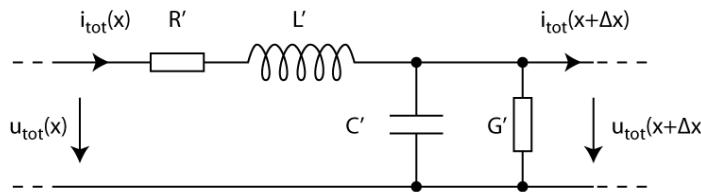


(Source: www.bogatinenerprises.com)

Transmission lines

Every PCB trace is a transmission line (1)

- equivalent schematic:



(R' , L' , C' and G' are the values per unit length)

- the differential equations for $u_{tot}(x)$, $i_{tot}(x)$, $u_{tot}(x+\Delta x)$, $i_{tot}(x+\Delta x)$ are called "Telegrapher's equations"
- Their solution results in two signals that can propagate in the two directions:
 $\rightarrow (u_a, i_a)$ and $\leftarrow (u_b, i_b)$.
(e.g.: *forward and reflected signal*)
For each one, the relationship between u and i is:

$$\frac{|u_a|}{|i_a|} = \frac{|u_b|}{|i_b|} = Z_0$$

Transmission lines

Every PCB trace is a transmission line (2)

- Important properties:

$$\text{Characteristic impedance : } Z_0 \approx \sqrt{\frac{L'}{C'}}$$

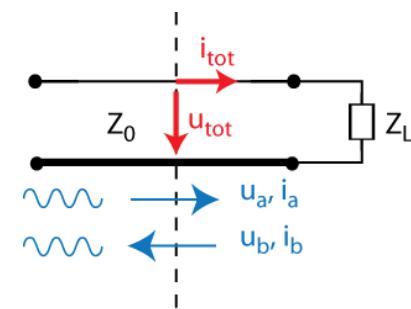
$$\text{Propagation velocity : } v_{ph} = \frac{c}{\sqrt{\epsilon_r \mu_r}} \approx \frac{1}{\sqrt{L' C'}}$$

- when a signal is sent into a transmission line, and before the reflected signal returns we see only u_a, i_a .
- Z_0 is the impedance that we would measure at the beginning of a line with length ∞ or more in general, when no reflected signal \leftarrow exists ($u_b, i_b = 0$)
- in order to avoid reflections at the end of a transmission line, the load impedance Z_L must be equal to the line's Z_0

- at any point in the line, we know that:

$$u_b(x) = u_a(x) + u_s(x)$$

$$i_b(x) = i_a(x) - i_s(x)$$





Transmission lines

Signal reflection (1)

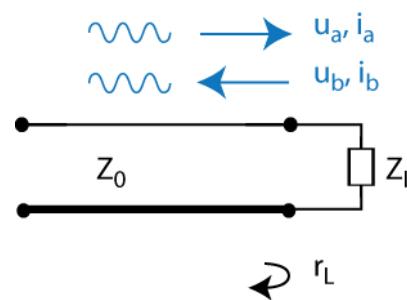
- When $Z_L \neq Z_0$ we have a reflection.
- We define the reflection coefficient r :

$$r_{(complex)} = \frac{u_b}{u_a}$$

- Relationship between Z_L , Z_0 and r :

$$r_L = \frac{Z_L - Z_0}{Z_L + Z_0}$$

$$\underline{Z}_L = Z_0 \frac{1 + r_L}{1 - r_L}$$



Quiz time

3. Calculate the reflection factor at the end of a 100Ω line terminated with a $1\text{k}\Omega$ load

Answer:

$$r = \frac{Z_L - Z_0}{Z_L + Z_0}$$

with $Z_0 = 100\Omega$ and $Z_L = 1\text{k}\Omega$ we have :

$$r = \frac{1000 - 100}{1000 + 100} = \frac{900}{1100} = 0.82 \text{ (real)}$$

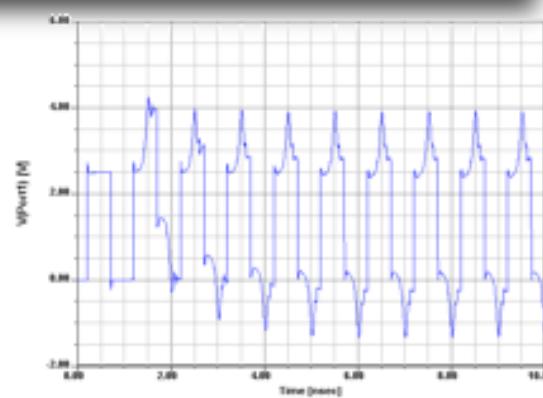
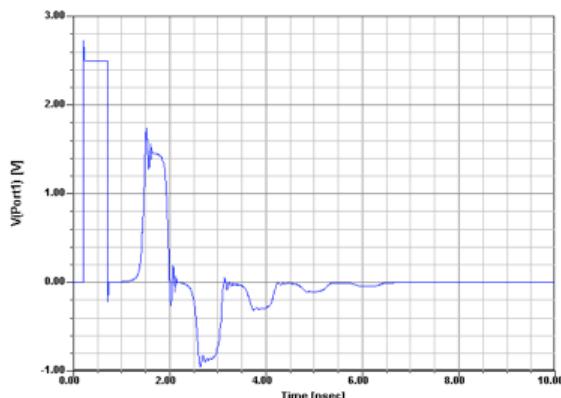
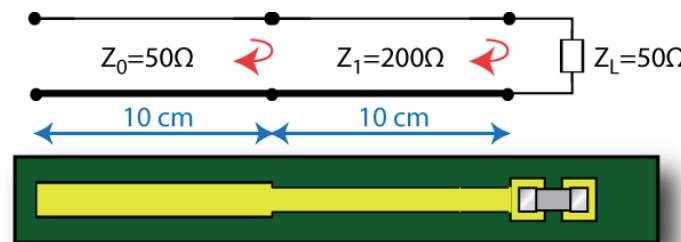
Transmission lines

Signal reflection (2)

- A junction between two transmission lines with different characteristic impedances also generates reflections:
- Examples of signal reflections seen **here**:



$$r_{junction} = \frac{Z_1 - Z_0}{Z_1 + Z_0}$$



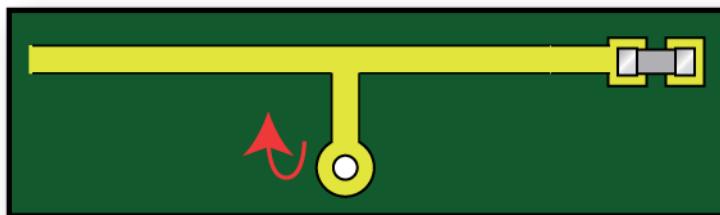
- Be careful with trace width changes, connectors, etc!

(Source: [22])

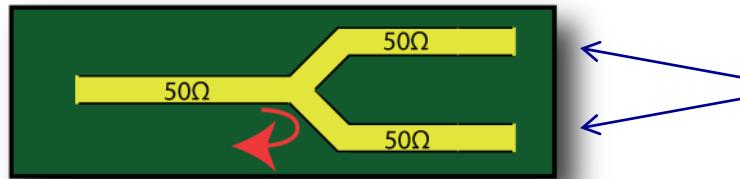
Transmission lines

Traces, stubs and splits

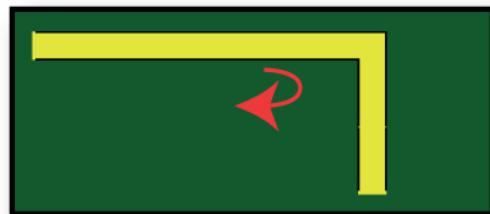
- An unloaded ($Z=\infty$) trace generates reflections ($r = +1$):



- Splitting a trace in two (or more) can generate reflections:



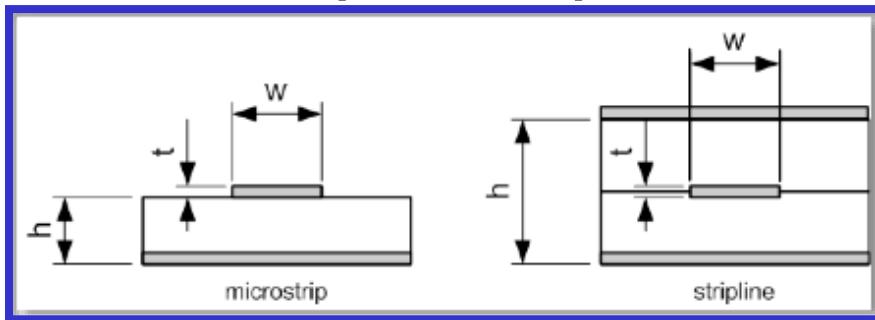
- Sharp corners generate reflections:



(Source: [22])

Transmission lines

Microstrip and stripline



| typical values Z_0 : | $w=3, h=1.6$ [mm] | $w=0.65, h=1.6$ [mm] |
|------------------------|-------------------|----------------------|
| Microstrip (in FR4) | 50 Ω | 98 Ω |
| Stripline (in FR4) | <20 Ω | 50 Ω |

- Microstrip: a signal trace runs over a continuous GND plane:

$$Z_0 \approx \frac{87}{\sqrt{\epsilon_r + 1.41}} \cdot \ln\left(\frac{5.98h}{0.8w + t}\right) \quad [\Omega]$$

$$v_{ph} \approx \frac{1}{1.017\sqrt{0.457 \cdot \epsilon_r + 0.67}} \quad [ft/ns]$$

- Stripline: a signal trace is "sandwiched" between two GND planes:

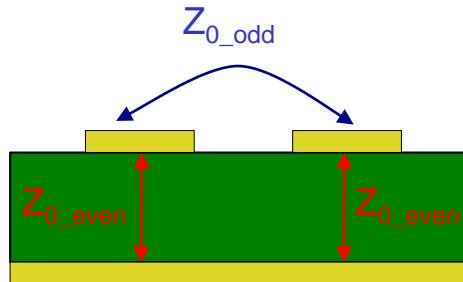
$$Z_0 \approx \frac{60}{\sqrt{\epsilon_r}} \cdot \ln\left(\frac{4h}{0.67\pi w \cdot \left(0.8 + \frac{t}{w}\right)}\right) \quad [\Omega]$$

$$v_{ph} \approx \frac{1}{1.017 \cdot \sqrt{\epsilon_r}} \quad [ft/ns]$$

(Source: [22])

Transmission lines

Differential lines



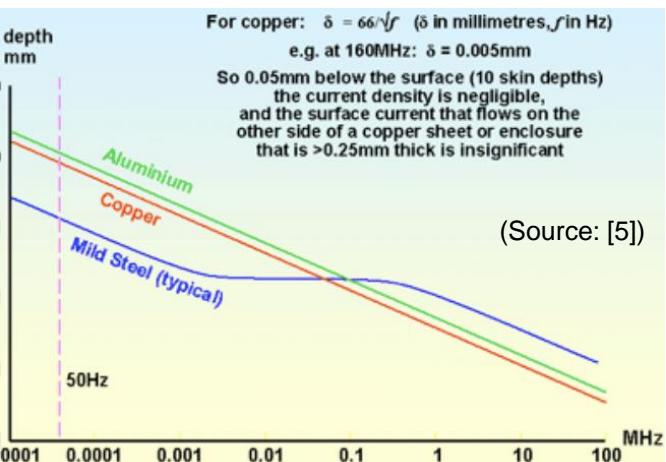
- Actually we can have two different Z_0 's, depending on how the two traces are driven: common mode or differential mode
- Example
 - Z_{0_even} is for common mode signals: the value is similar to that of a single microstrip line and is independent from the distance between the traces
 - Z_{0_odd} is for differential mode signals. Its value increases with increasing distance between the two traces
- Example: $Z_{0_even} = 50 \Omega$, $Z_{0_odd} = 100 \Omega$
- use numeric simulation tools to determine the two Z_0 's

Transmission lines

Skin effect

- As a consequence of Maxwell's equations, AC current tends to distribute on the outer region of a conductor.
- Def: skin depth δ is the depth into the conductor by which the current density has decreased to $1/e$ of what it was ($\sim 37\%$)

$$\delta = \sqrt{\frac{2}{\omega \mu_0 \mu_r \sigma}}$$



where:

ω : frequency ($2\pi f$)

μ_0, μ_r : permeability

σ : conductivity [$\Omega^{-1}\text{m}^{-1}$] ($=5.82 \times 10^7$ for copper)

- since the AC current uses a smaller conductor section, R increases due to the skin effect:

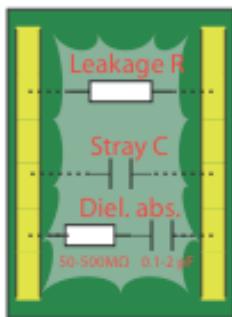
$$R \sim \sqrt{\omega}$$

- Example:

| f | 1 kHz | 1 MHz | 10 MHz | 100 MHz |
|---------------------|-------|-------|--------|---------|
| $\delta[\text{mm}]$ | 2.1 | 0.06 | 0.02 | 0.006 |

Parasitic PCB effects

*...depend from PCB materials, environmental factors (humidity, dirt, salts),
PCB layout and assembly*



Static (affect DC operation of the circuit)

- Leakage resistance
 - even a 10nA leakage current can disrupt operation of a high impedance analog circuit

Dynamic (affect AC operation of the circuit)

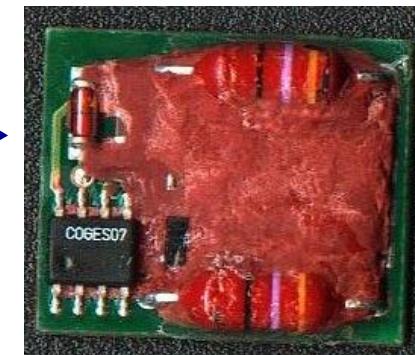
- Stray capacitance (between traces, component cases and leads)
 - can "detune" precision filters or oscillators
- Dielectric absorption (same as in capacitors, 0.1-2.0pF in series with 50-500MΩ)
 - can affect circuit settling time, S/H circuits, active filters
- High frequency losses
 - can affect high-Q circuit and produce signal attenuations



Parasitic PCB effects

Workarounds

- PCB layout
- component mounting (THT leads folding)
- PCB and components coating (resin) →
against atmospheric agents



- use of superior PCB materials (alumina, Rogers[©], Taconic[©], Arlon[©]) [...Link](#)
- guard rings

Quiz time

4. Resistive losses on a conductor

- do not change with frequency
- are higher at higher frequencies
- are higher at lower frequencies

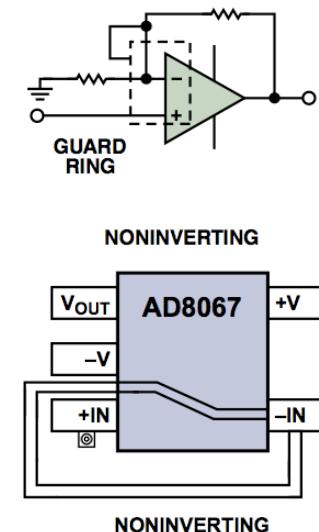
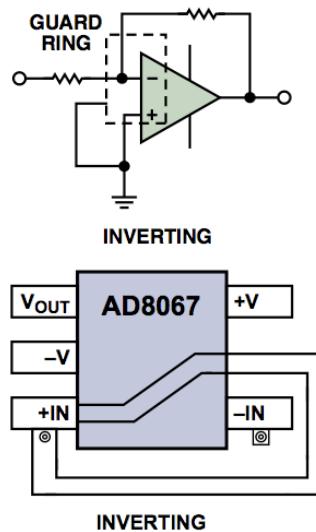
5. A stub is ...

- a test point
- a connector
- an unterminated transmission line
- a branch transmission line

Parasitic PCB effects

Guard rings against parasitic effects (analog circuits)

- *the idea:* Completely surround sensitive nodes with conductors that can readily sink stray currents, and maintain the guard conductors at the exact potential of the sensitive node
- *example* Inverting amplifier
- *example* Non-inverting amplifier



- in THT circuits, repeat the guard ring on *all* layers
- *never* leave guard rings *floating*!

(Source: [1], [2])



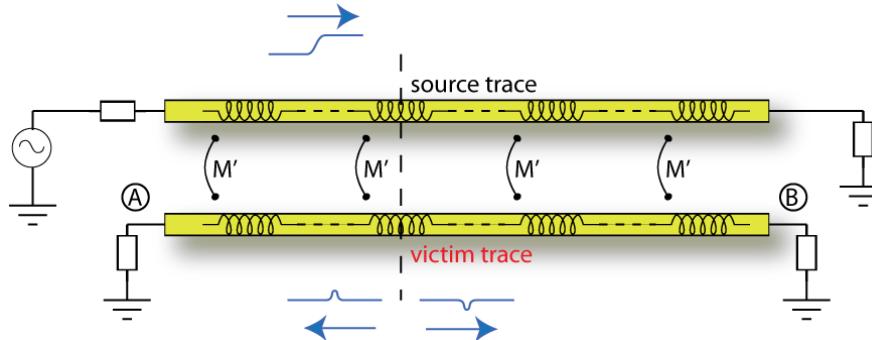
Crosstalk

What is it?

- Crosstalk is the unintended interference between nearby signal traces
- There are several reasons for crosstalk between two (or more) signal traces:
 - inductive coupling
 - capacitive coupling
 - sharing of a common signal return path with non-zero impedance

Crosstalk

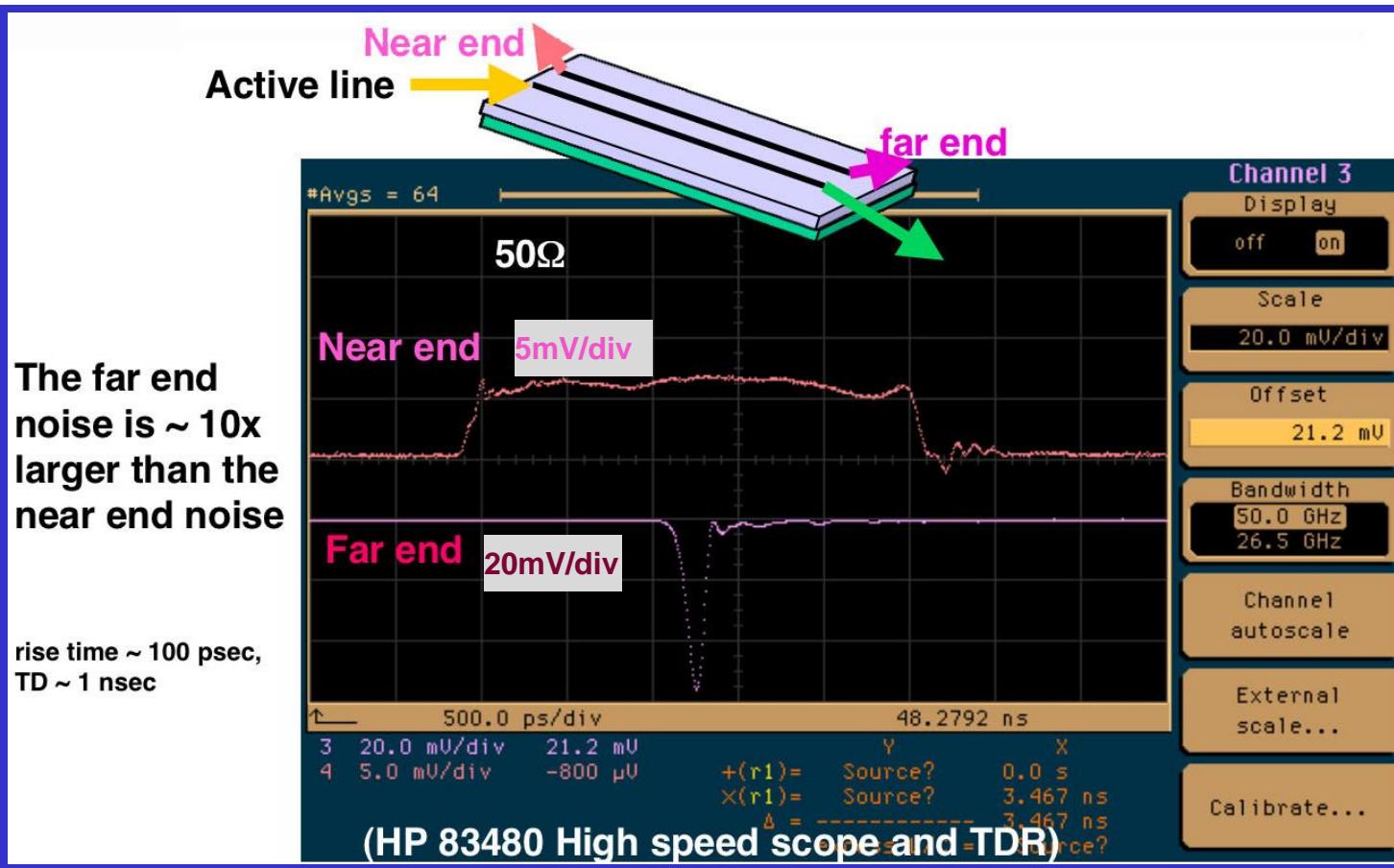
Inductive coupling



- the magnetic field lines generated by the source trace induce a voltage on the victim trace
- $u_{victim} = M \frac{di_{source}}{dt}$
- on the victim trace, the coupled signal propagates in both directions with opposite polarity
- in the victim trace, the "pulses" contributed by each single coupling point arrive at the same time at the far end (B), while they arrive at different times at the near end (A).
- therefore, in B we see a sharp pulse with strong amplitude, whereas in A we see a broad pulse

Crosstalk

Inductive coupling



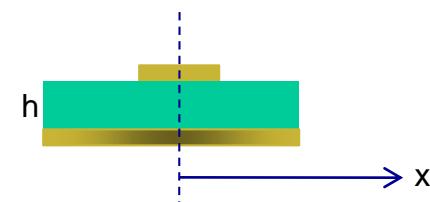
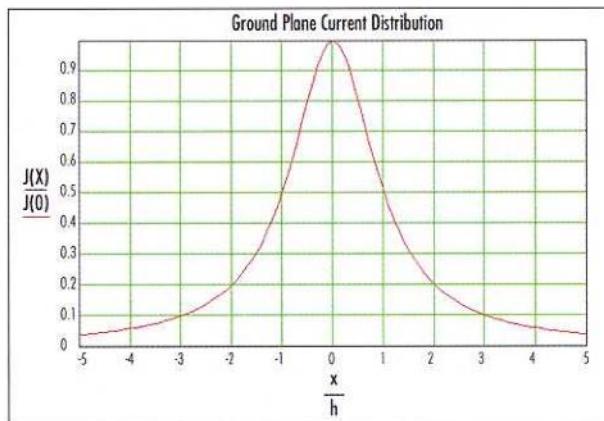
(Source: Agilent)

Crosstalk

Inductive coupling – estimation of the inductive crosstalk

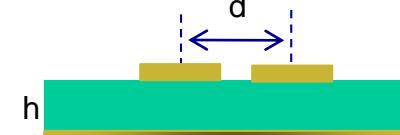
- we have seen (*Image Planes*) that the current distribution in the GND layer underneath a signal trace has the following distribution:

$$J(x) = \frac{I_0}{\pi h} \cdot \frac{1}{1 + \left(\frac{x}{h}\right)^2}$$



- The magnetic field decreases accordingly, therefore, for a parallel trace at distance d we can expect that the inductive cross coupling is proportional to:

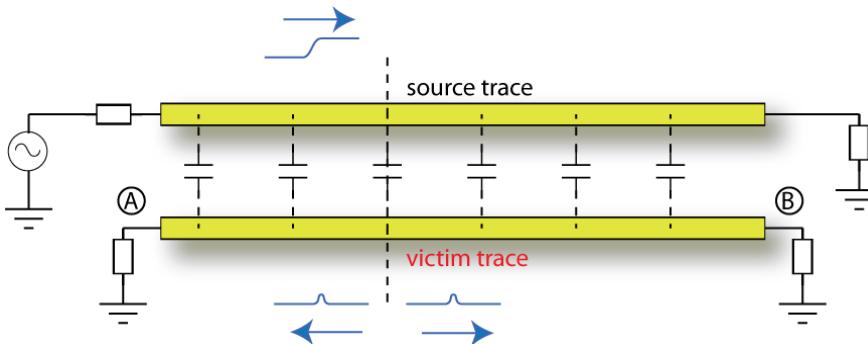
$$\frac{1}{1 + \left(\frac{d}{h}\right)^2}$$



(Source: [6], [19])

Crosstalk

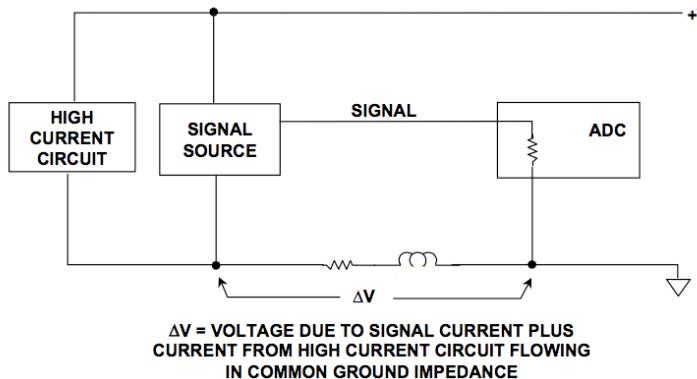
Capacitive coupling



- on the victim trace, the coupled signal propagates in both directions with the same polarity
- in the victim trace, the "pulses" contributed by each single coupling point arrive at the same time at the far end (B), while they arrive at different times at the near end (A).
- therefore, in B we see a sharp pulse with strong amplitude, whereas in A we see a broad pulse
- when a solid reference plane is present, inductive and capacitive crosstalk voltages are roughly of the same amplitude. Therefore, at the far end they tend to cancel (opposite polarity) and at the near end they add up
- we must provide good termination in A to avoid that the coupled signal gets reflected back into the victim trace
- when a solid reference plane is missing, inductive crosstalk prevails

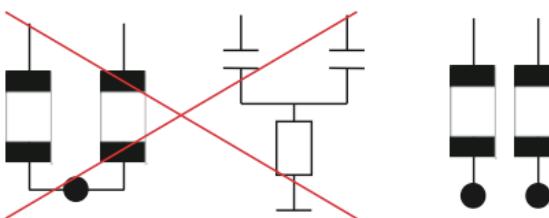
Crosstalk

Crosstalk due to a common signal return path with non-zero impedance



- ground noise (e.g. from high speed logic) can translate to output voltage noise of other circuits if they share a common return path with $Z \neq 0$
- => use uninterrupted GND planes!
- => avoid sharing the same GND via by more than one component

($C_{\text{decoupling}}$, IC GND, etc)





Crosstalk

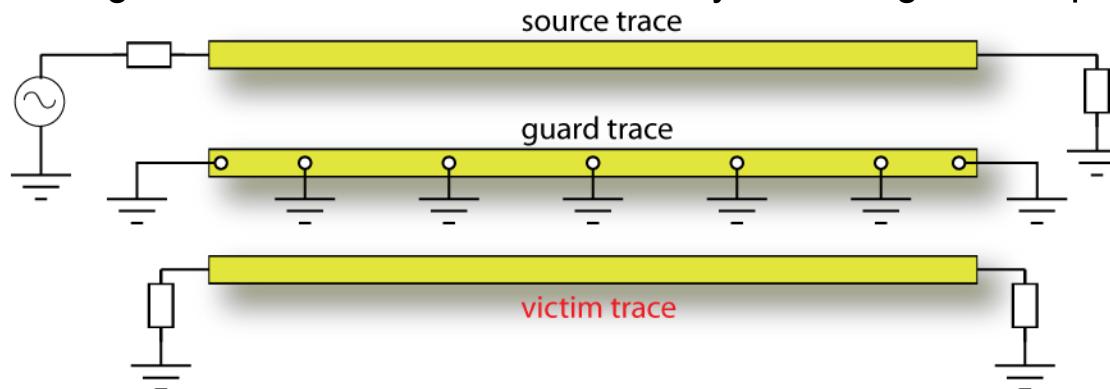
How to reduce it:

- do not run traces parallel over long distances
- minimize the length of all interconnects
- use a continuous reference plane adjacent to each signal layer (reduce coupling between signal layers and reduce impedance of the signal return path)
- reduce the number of layer changes and reduce the impedance of traces
- use the slowest possible signal edges (choice of the logic family)
- provide proper termination of the signal traces at both ends
- use differential signaling
- use lower signaling voltage (e.g. LVDS)
- in connectors, add a separate return (GND) pin for every signal
- use stripline technology for very critical nets (e.g. high speed clocks)
- use guard traces

Crosstalk

Guard traces to reduce crosstalk:

- may be useful to reduce **inductive coupling** as currents induced in the guard trace tend to compensate the magnetic field generated by the source trace
- this technique was seen more frequently on 2-layer PCBs without GND plane
- however in multilayer PCBs, compared to the effectiveness of a continuous reference plane adjacent (at a short distance) to every signal plane, a guard trace adds little benefit against inductive coupling.
- a grounded guard trace can act as a faraday shield against capacitive coupling



- **never** leave a guard trace floating!

Quiz time

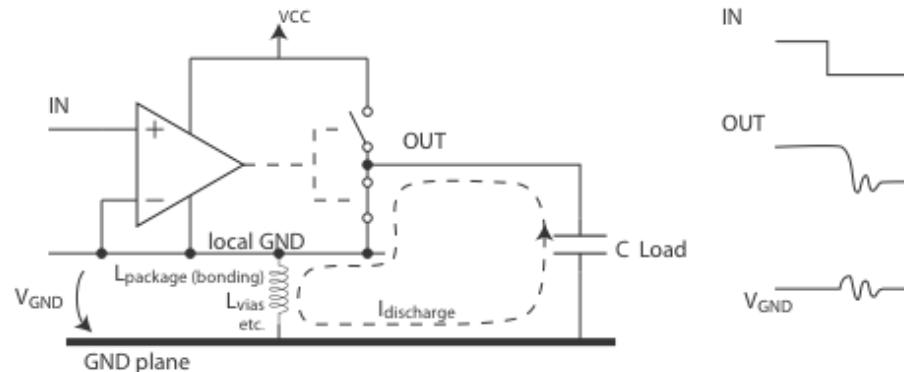
6. The inductive crosstalk between two adjacent signal traces

- increases with the distance
- decreases with the square of the distance
- decreases with the distance
- other

Ground bounce

is a similar problem and can be the origin of crosstalk:

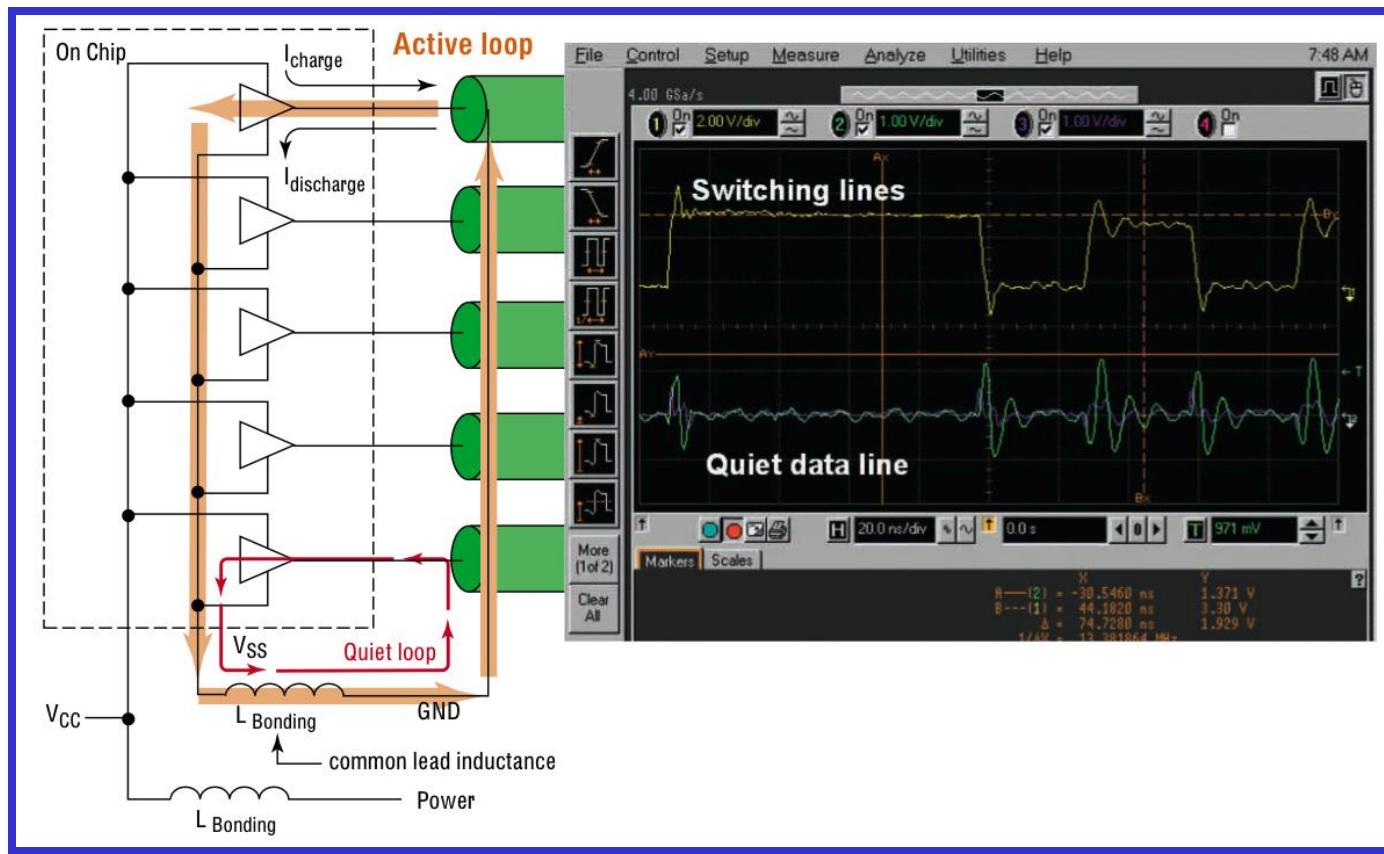
- single gate:



- multiple output drivers, input buffers sharing the same "local GND":
 - outputs that should not change show "ground bounces" when other outputs switch
 - input buffers see a input change due to ground bounce, even if the input signal is not changing (critical for clock circuits!)
 - the problem can extend to multiple ICs, if they share the same local GND or the same via to the main GND plane, etc.

Ground bounce

Ground bounce and crosstalk in action:



(Source: Agilent)

Ground bounce

How to reduce it:

- reduce output slew rate, use slower logic family or one with slew rate control
- use IC cases with smaller L (SMD, BGA) and more GND pins
- do not share the same via to connect multiple ICs to the GND plane
- reduce impedance of connections to the GND plane (e.g. multiple vias)



Differential signaling

advantages from the signal integrity point of view:

- can tolerate much common mode noise (if noise affects equally both lines of a differential pair, it cancels completely in the differential receiver)
- are insensitive to GND noise and non-zero GND impedance
- they have a controlled impedance, which facilitates finding an adequate termination (reduction of signal reflections)
- they generate less emissions (noise) in case of a non optimal (continuous) GND plane, because current return path is not travelling through GND.
- the same noise margin can be achieved with half the voltage swing of a single ended signaling solution (better immunity / less emissions)
- **do not** run a trace very close to a differential pair, as this could unbalance the pair and void some of its advantages!

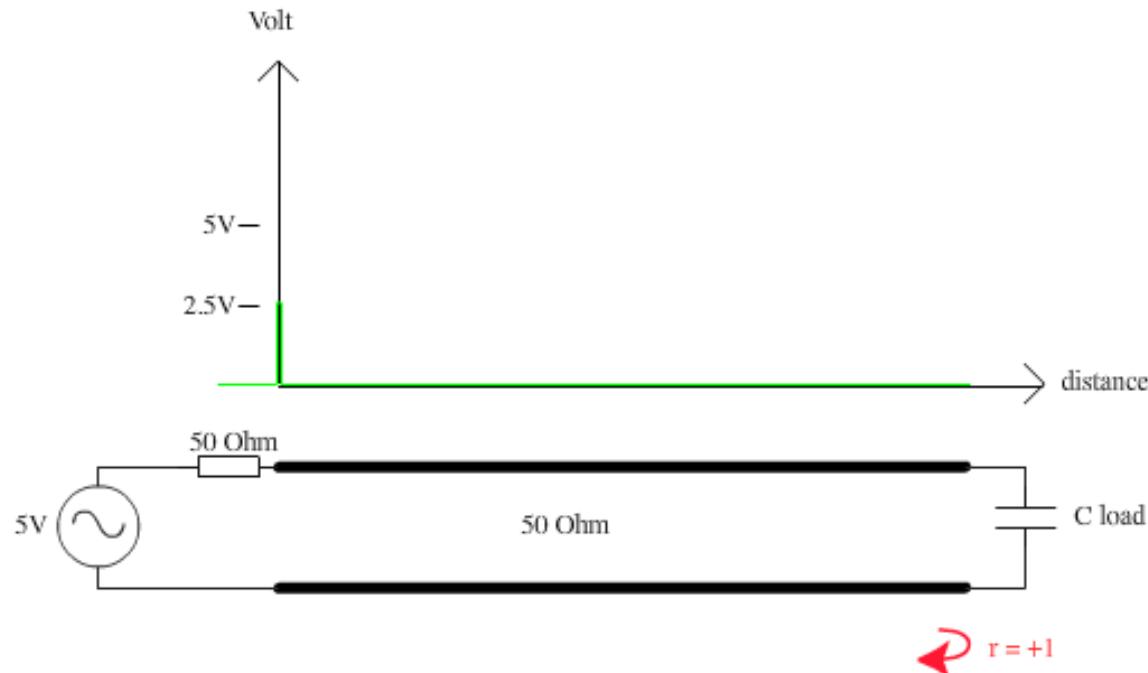
Transmission lines

Terminations

- **the purpose:** provide a load impedance at the end of a transmission line that is equal to its Z_0 , as this will result in **no reflections ($r = 0$)**
(signal reflections can severely compromise the functionality in digital systems)
- extend the possibility to use fast signal rise/fall times also on longer connections
- types of termination:
 - series
 - parallel (including Thevenin)

Transmission lines

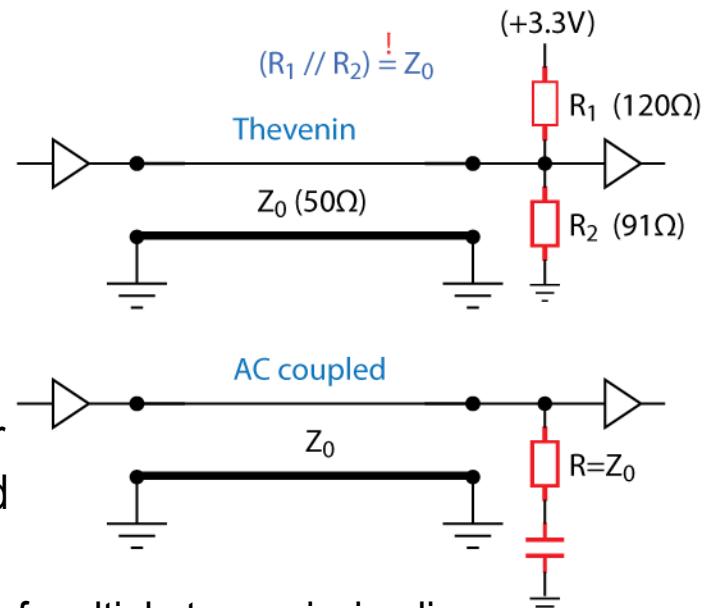
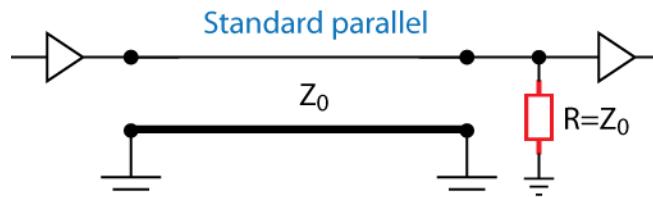
Series termination explained



(Source: [22])

Transmission lines

Parallel terminations

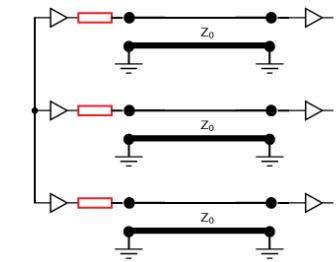
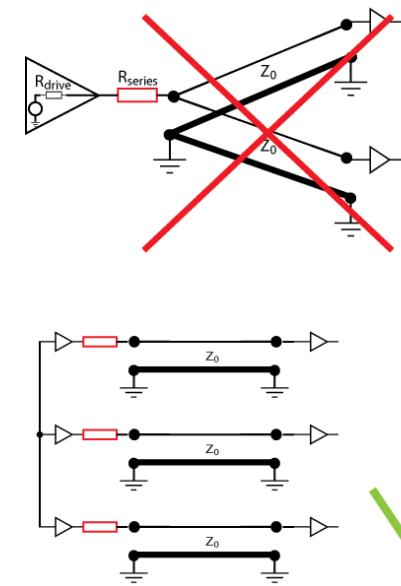
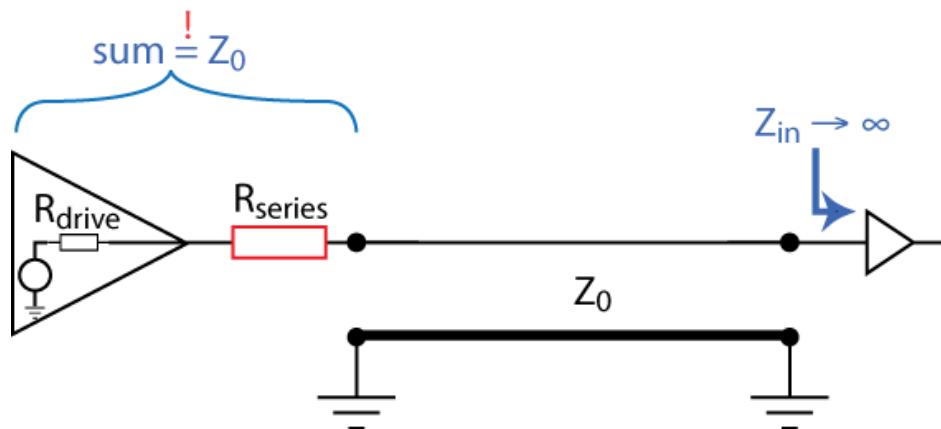


- Thevenin termination: choose R_1 , R_2 so that their center point voltage is halfway from logic high and low levels
- beware from crosstalk in the terminating network of multiple transmission lines:
 - keep resistors at adequate distance
 - do not share GND vias for multiple termination networks
- place termination network *after the last* receiver IC
- place terminations at both ends if the line is bidirectional
- can be used for multidrop bus topologies (e.g. RS485)
- disadvantage: static power consumption (except for "AC coupled" version and in reduced extent in "Thevenin" version)
- disadvantage: reduced noise margin if driver can not source all the required current

Transmission lines

Series terminations

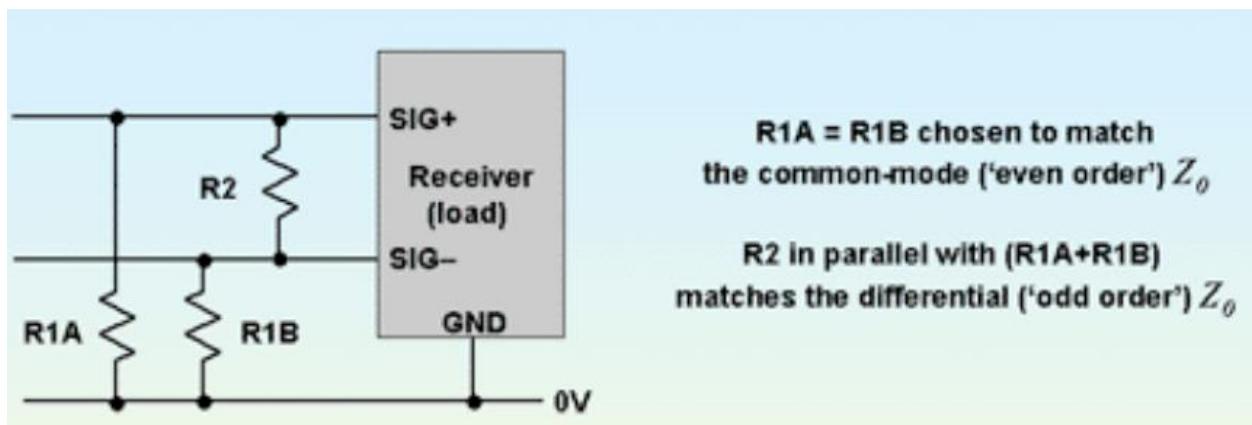
- for point-to-point (1 driver – 1 receiver) connections only
- low power dissipation
- for loads with high Z only (e.g. CMOS inputs)
- driver IC should have same R_{drive} for V_{OH} and V_{OL}
- slightly reduces signal slew rate, at the benefit of better signal integrity
- place R_{series} very close to the driver IC
- place a series termination at both ends of the line, if it is a bidirectional one



Transmission lines

Terminations for differential lines

- Remember?: Differential lines actually have two types of Z_0 : Z_{0_even} and Z_{0_odd}
- We should try to terminate both of them (even in case of a pure differential signal, due to parasitic effects etc we are likely to have some common mode voltage)
- Example of parallel termination ([5]):



Quiz time

7. What is ground bounce and how can it be reduced?

Answer:

Ground bounce happens when an IC with a non ideal (non zero impedance) connection to GND draws a high current spike, for instance when switching a capacitive load. When flowing through the non ideal GND connection of the IC, this current produces a voltage drop here. The "internal" GND of the IC experiences a voltage shift which can be observed also on other outputs that should stay quiet. Both the impedance of a via and that of the IC's internal bonding can contribute to this effect.

8. A series termination is obtained with:

- a series resistor at the end of the line
- a series resistor at the beginning of the line
- a resistive voltage divider at the end of the line



Transmission lines

When do transmission line effects become important

(crosstalk, signal reflections, need for terminations, etc)

Remember

- rule of thumb: transmission line effects must be taken into consideration if the round trip (\Rightarrow) propagation time over a line exceeds the signal's rise/fall time
- Typical values:

| Logic family | Rise / Fall time approx. | is transmission line starting from .. |
|--------------|--------------------------|---------------------------------------|
| 74HC | 13-15 ns | 117 cm |
| 74LS | 9.5 ns | 85.5 cm |
| 74ALS | 2-10 ns | 18 cm |
| 74ACT | 2-5 ns | 18 cm |
| 74F | 1.5 ns | 10.5 cm |
| CPLD/FPGA | 0.5 ns | < 5 cm |

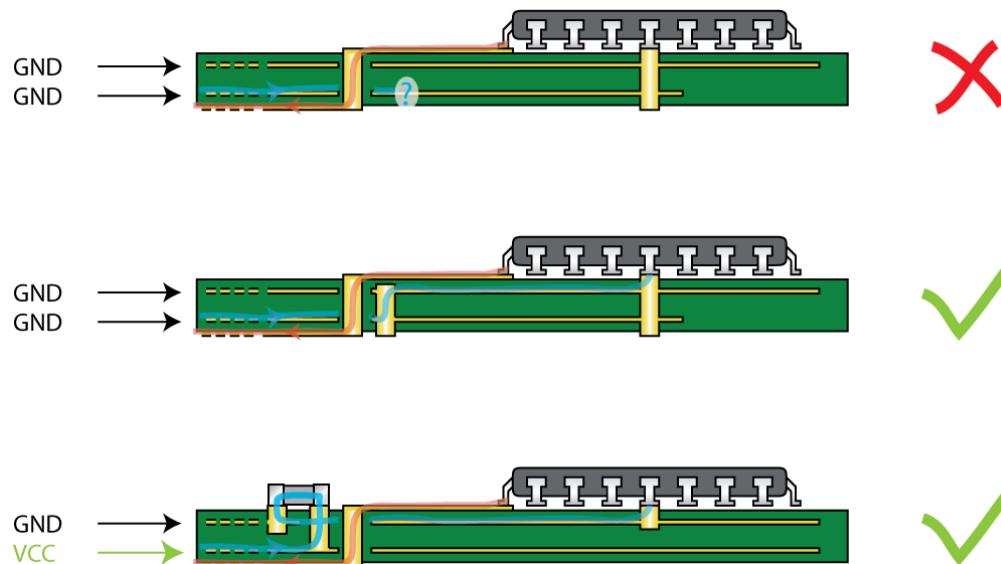
(assuming: microstrip, FR4 ($\epsilon_r = 4.6$), 0.36 ns/cm propag. speed)

(Source: [11])

Transmission lines

Vias

- Rule #1: try to avoid changing layer with high speed signals whenever possible
- Rule #2: if a via can't be avoided, don't forget to assure an uninterrupted return path
- A via represents a discontinuity in the transmission line (capacitance to GND/VCC planes it crosses, series inductance) and can be a source of concern



Clock distribution

- Clock nets are usually carrying high frequency signals. Therefore, transmission line effects arise. It is important to apply all the precautions already seen against signal reflections, ringing, crosstalk, etc.

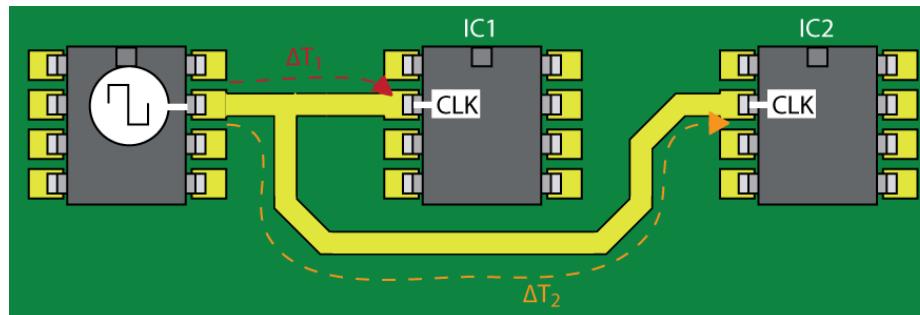
In the next slides we will deal with some special issues related to clock distribution:

- **Clock skew**
- **Clock jitter**

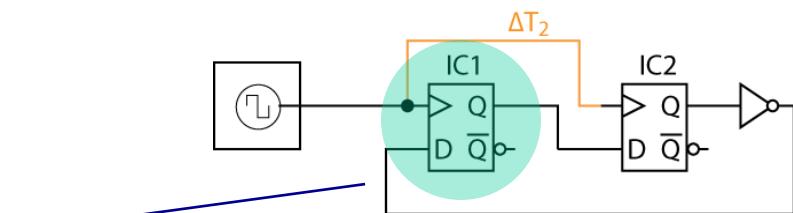
Clock distribution

Clock skew

- ... refers to a situation where the clock signal to a synchronous logic circuit does not arrive at the same time to all IC's clock inputs



- Example:

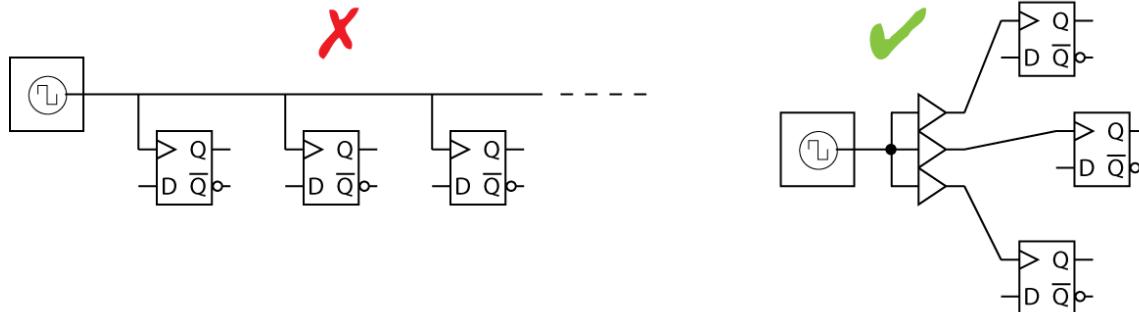


$$t_{SU(CLK)} = T_{CLK} - \Delta T_2 - t_{CKQV(FF)} - t_{P(BUF)}$$

Clock distribution

Clock skew – how to prevent it:

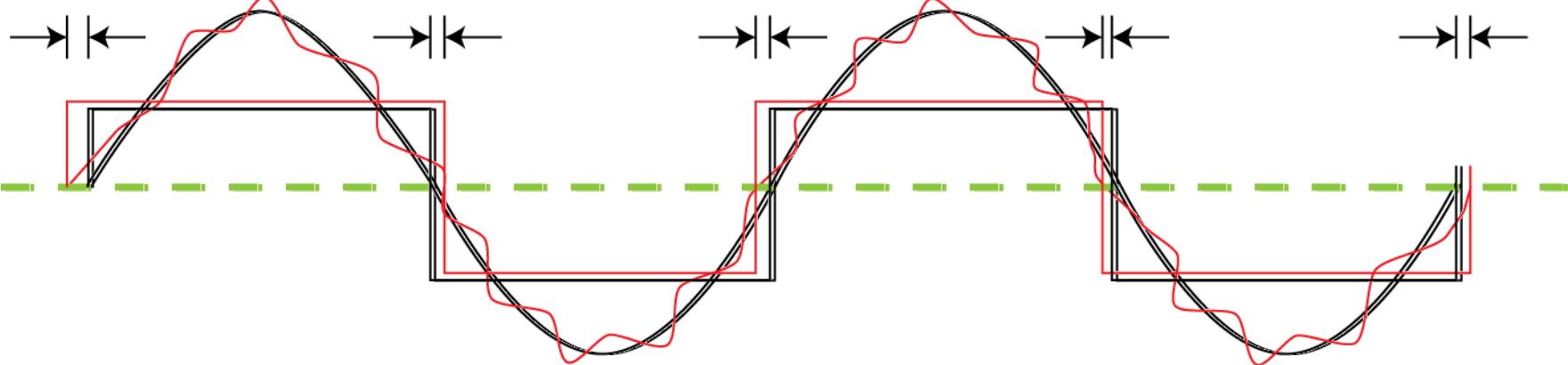
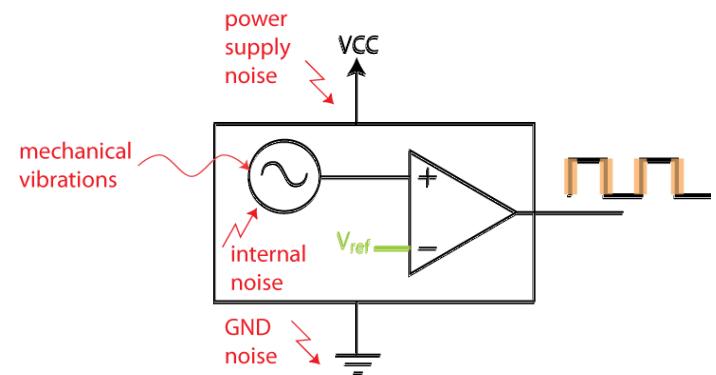
- place all clock inputs in close proximity
- place the clock source at the center and distribute the clock with a "star" topology, consisting of all equal length (terminated) PCB traces.
- if the load becomes excessive for the clock source, there are commercially available clock buffers with multiple outputs having minimum skew
- use PLL based clock retiming circuits (phase adjusting)
- do not use multidrop topology for clock distribution



Clock distribution

Clock jitter

- are small variations of a clock oscillator's output transitions from their ideal positions





Clock distribution

Clock jitter – how to prevent it

- Clock jitter should be addressed with the same approach as signal integrity problems
- reduce noise sources and their coupling
- apply circuit partitioning, shielding
- prevent crosstalk ([see](#))
- provide good signal return paths
- do not share GND connections between components, ICs
- increase immunity against GND noise by using differential clock lines or isolation techniques
([see](#) "Mixed Signal Circuits-sampling clock circuits")

Exercise

9. Discuss some advantages and disadvantages of series vs. parallel termination methods

Answer:

Series terminations have the advantage of generating less power dissipation (if the logic signal does not switch too often). Their disadvantage is that they should be used only in point-to-point (1:1) connections (and not in 1:n connections).

The advantage of parallel terminations (at the end of the line) is that the level switching (high-to-low or viceversa) waveform observed at any point of the line is made of one single step (this is not the case with series terminations: remember the animation shown during the lesson for series terminations, slide n 48 of this lesson). Therefore parallel terminations are better recommended for multidrop applications (=situations with more than one "receiver" distributed throughout the line, e.g. RS-485). The disadvantage of parallel terminations is their power dissipation, even if the signals are static (not changing).

Exercise

Questions related to the circuit & simulation of slide page 48:

10. What happens if we add a 50Ω load at the end of the line?

Answer:

Doing so we end up having a combination of series and parallel termination. The 50Ω load removes reflections at the end of the line since it is matched to the line's impedance. Therefore, we will not see the voltage step from 2.5V to 5V. The final voltage on the line is therefore only 2.5V, which could be insufficient to be recognized as a logic "1" by a 5V CMOS gate.

11. What happens if we increase the driver's R_{series} ?

Answer:

Since R_{series} forms a resistive voltage divider with the line's Z_0 , the voltage of the incident signal wave travelling down the line will be smaller. Due to the reflection at the end of the line, the final voltage will be twice that value. We must check if this is still sufficient for the input requirements of the component attached at the end of the line.

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MASTER OF SCIENCE
IN ENGINEERING

ADVANCED ELECTRONIC DESIGN

EMC, signal integrity, grounding and power supply routing,
decoupling, transmission lines, simulation tools

Dipl.-Ing. Ricardo Monleone

Topics of this series of 3 lessons

PCB Design

- Lesson 1:
 - Introduction
 - Partitioning, filtering
 - Shielding
 - Image planes
 - Continuous vs split GND concepts
 - Mixed signal circuits
- Lesson 2:
 - Decoupling
 - Transmission lines
 - Guard rings
 - Crosstalk, Ground bounce
 - Differential signaling
 - Terminations
 - Clock distribution: clock skew and clock jitter
- Lesson 3:
 - Place & route strategy
 - Components selection
 - Layer stackups
 - Multicard systems, backplanes
 - Enclosures, connectors and cables
 - ESD + Burst protection
 - 2-layer PCBs
 - Design for testability
 - Prototyping



Components placement and trace routing

General guidelines (summary) (1)

Execute the design of a PCB in the following order and make sure to:

1. **place** the I/O connectors at the periphery of the board and partition them according to their function
2. **place** oscillators and fast circuits at the center of the PCB, far from connectors and I/Os.
3. **place** power circuits near the power supply/voltage regulators
4. **partition and place** the remaining components carefully (according to the connector's position). Place components so that critical signal traces can be kept short.
5. **reserve room** for mounting holes for GND stitches (screws)
6. **route** the power supplies (reference planes) and decoupling capacitors
7. **route** critical signals: fast clocks and signals, high speed interfaces (Ethernet, USB) and their termination networks. Consider using stripline technology for them.
8. **route** analog signals
9. **route** the remaining digital signals ***)**

***)** use the autorouter only here, but double check its result!

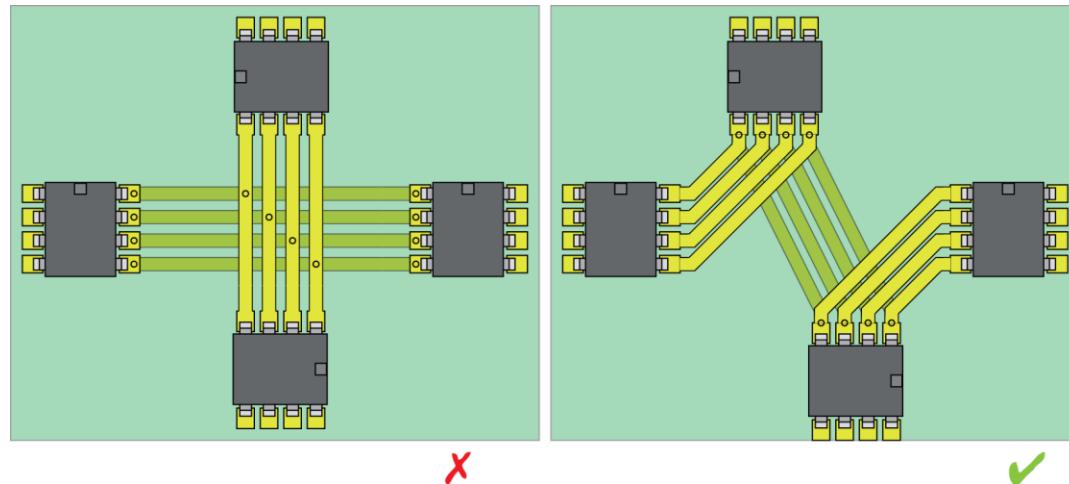


Components placement and trace routing

General guidelines (summary) (2)

More on routing...

- avoid:
 - stubs,
 - T-junctions.
 - grid routing



- route all critical nets on a single layer that is adjacent to a GND layer (avoid vias)
- verify that fast signals have a good return path (immediately under the trace)
- do not route over interruptions of the reference plane
- avoid sharp corners in the PCB traces, as they cause signal reflections
- do not place vias between differential pairs



Components selection

Keep signal integrity and EMC problems small with:

- use no faster logic family than that dictated by your design requirements *)
The same also applies to power switching components (MOSFETs, IGBTs)
- be careful when selecting second source components
- choose components with the smallest possible enclosure (chip capacitors and ICs with the smallest available SMD footprint)
- choose ICs with a "good" pinout (e.g. a GND pin available next to the crystal oscillator pins, a sufficient number of GND and VCC pins, placed closely, etc)
- when choosing decoupling capacitors, check their series resonance frequency

*) When a slower logic IC is not available, you should consider:

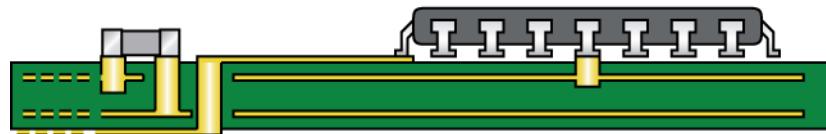
- using ICs with controlled slope outputs and/or reduced output swing
- slowing the output transitions through RC (or ferrite bead + C) filters



PCB technology

Microvias (high density interconnect, HDI)

- the name refers to vias having a diameter of < 0.15 mm and that do not go through all of the layers



- PCBs with microvias have a **higher cost**, but also have **important advantages**:
 - allows "via-in-pad", which reduces decoupling inductances
 - allows a more efficient routing and often helps reduce the number of layers
 - often allows shorter trace lengths and therefore reduces transmission line effects
 - reference planes are less perforated and have a lower impedance, provide a better signal return path and have a better shielding effect
 - shorter vias do not radiate beyond the layers of interest and do not act as open stubs



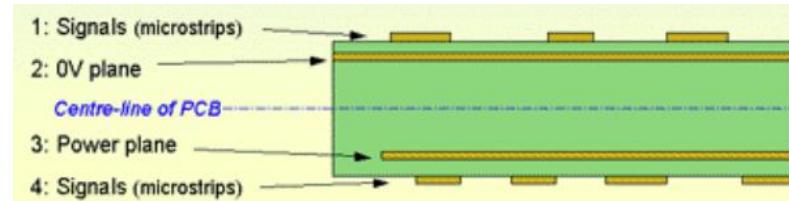
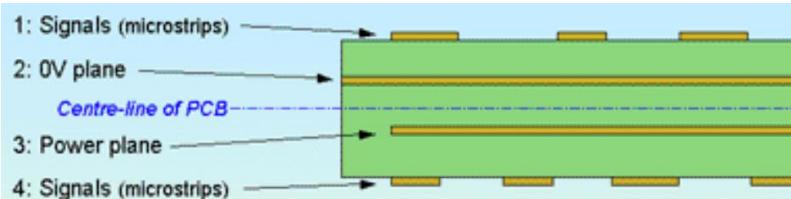
PCB technology

Layer stack-up

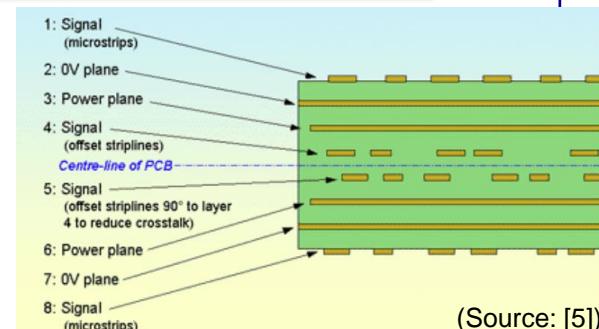
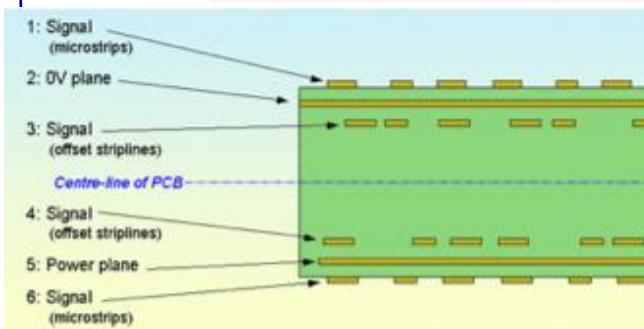
- an old rule of thumb (the "5/5 rule") states: if the signals in a circuit have frequency contents $>5\text{MHz}$ or rise/fall times $<5\text{ns}$, then a multilayer PCB should be used
- the optimal multilayer stack-up should fulfill the following requirements:
 - GND and VCC layers should be near, for maximum capacity (decoupling)
 - image planes (GND, VCC) should be adjacent and near to the outer layers for best signal integrity
 - a GND plane is the preferred image plane near the component side and near a signal layer with fast signals
 - long high speed traces should be routed on layers located inside the image planes for best shielding (stripline). Signal traces on the external layers should be kept short.

PCB technology

Layer stackups compared



| maximum GND-VCC capacitance | image planes near signal layers | GND layer near component side | internal signal layers in stripline |
|-----------------------------|---------------------------------|-------------------------------|-------------------------------------|
| | | (✓) | |
| | ✓ | ✓ | |
| | ✓ | ✓ | ✓ |
| ✓ | ✓ | ✓ | ✓ |



(Source: [5])

Quiz time

1. Explain some criteria when choosing a logic family (speed, output voltage swing, etc)

Answer:

Lowest possible speed, lower possible output voltage swing (e.g. 2.5V logic), small case, optimal pinout with many GND pins.

All these criteria have an impact on the switching noise and associated problems (emissions, crosstalk, reflections, etc.)

1. When specifying a multilayer PCB stackup

- always keep the same distance between all layers
- VCC and GND should always be the outer most (top+bottom) layers
- it depends

1. Describe in what sequence you execute the various steps involved in the design of a PCB

Answer:

See slides 2 + 3



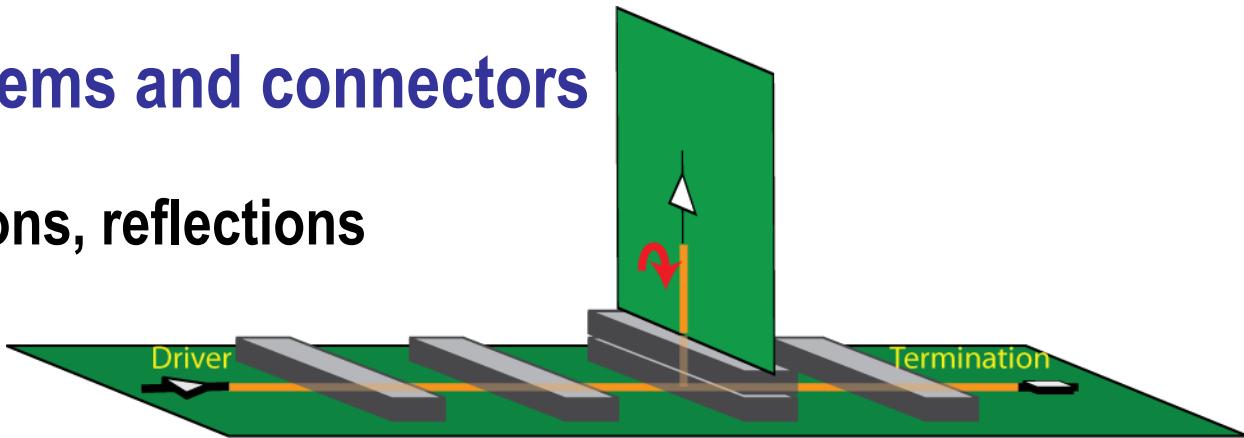
Multicard systems and connectors

..involve passing signals through connectors and backplanes

- rule #1: for best signal integrity and EMC performance, always try to fit your system within one single PCB!
- Problems:
 - transmission line impedance control
 - crosstalk
 - signal reflections (terminations, stubs)
 - clock and signal skew
- fast serial buses are today's preferred solution over parallel buses for signals leaving a PCB:
 - less wires, crosstalk. Easier signal routing.
 - accurate impedance control of a few (often differential) serial lines is easier to accomplish
 - reduced cost (connectors, PCB real estate)

Multicard systems and connectors

Signal terminations, reflections



- capacitively loaded stubs on daughter cards should be kept short, as they cause reflections
- backplane transmission line loading depends on the number of inserted daughter cards and their input impedance. This modifies the characteristic impedance Z_0 of the line. It can become difficult to find a termination concept that accommodates all possible situations. A tradeoff must be taken.
- Z_0 should be kept constant over the entire length of the backplane signal traces
- if the communication is bidirectional, the lines must be terminated at both ends
- apply design recommendations provided by the bus standards (PCI, VME, etc)



Multicard systems and connectors

Signal routing and layout considerations

- prevent crosstalk on the backplane by using multilayer boards with reference (GND) planes between any two signal layers. Keep adequate distance between traces on the same layer
- route critical signals against a GND (not VCC) layer
- consider using stripline technology for fast signals on the backplane
- use impedance controlled connectors. Use as many GND pins as possible with the allocated connector size and pin number (minimum: one for each signal pin)
- RF coupling between nearby daughter cards can be a problem. (mount a grounded metal plate between the cards *or* design the cards so to have bottom layer = GND)
- since the backplane's GND layer and the connectors have non zero impedance, crosstalk and ground bounce problems could arise. Reduce GND impedance on the backplane and provide sufficient GND pins in the connectors
- keep logic transitions as slow as possible
- avoid layer changes (vias) with the signals on the backplane
- beware of card connectors whose THT pads (and antipads) completely interrupt the reference planes (SMD connectors are better from this point of view)

Multicard systems and connectors

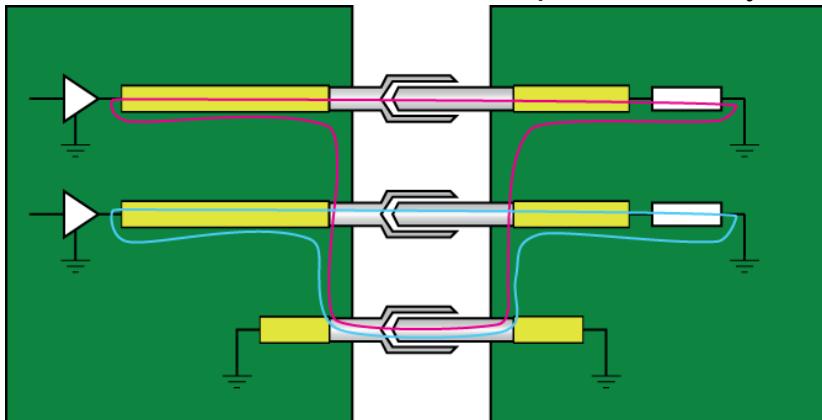
Crosstalk at the connector level

- inductive (M, mutual inductance between current loops formed by different signals)

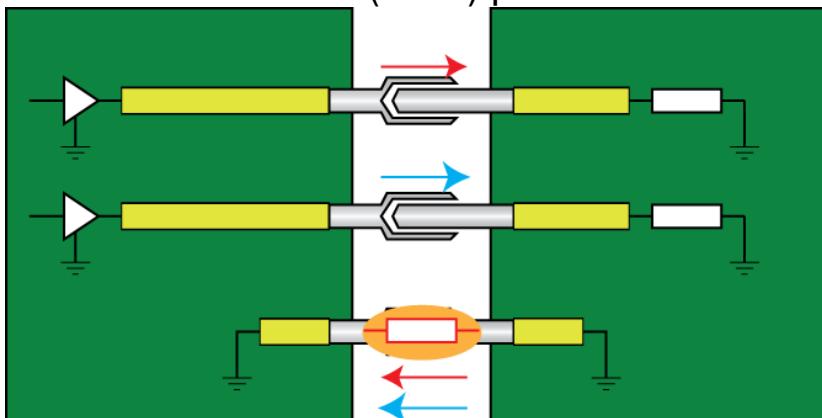
$$\bullet \quad u_1 = M_{12} \cdot \frac{di_2}{dt}$$

Workarounds:

- reduce M
- reduce di/dt



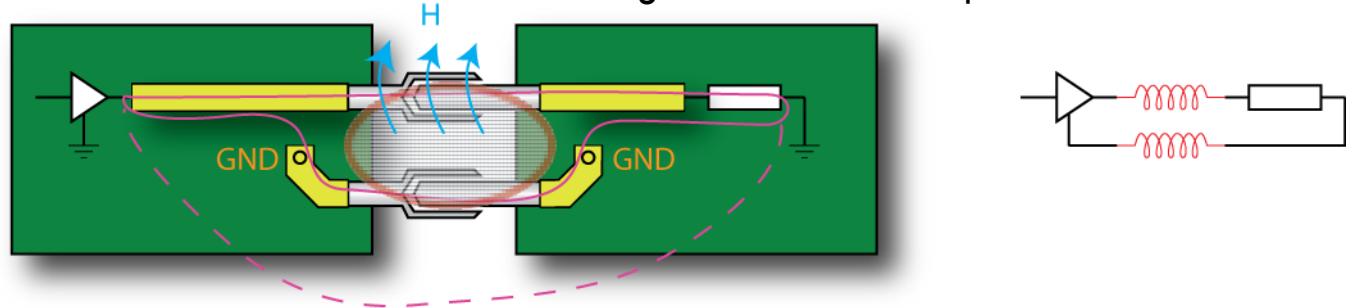
- due to series impedance on shared return (GND) pins



Multicard systems and connectors

Avoid false current return paths

- whenever the connector has a series R or L, the signal will try to find alternate return paths
- the increased distance between a signal and its return path in the connector generates:
 - increased current loop area => noise emissions!
 - increased series inductance (in the connector)
- try to minimize the distance between the signal and its return pin

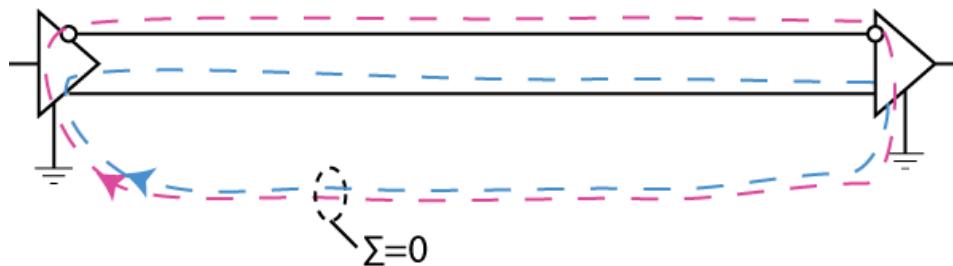


- alternate return currents cause EMI problems
- due to the higher connection series impedance in daughter cards, attaching I/O cables to daughter cards should be avoided (risk of alternate return paths from cables, emissions)
- if two cards are connected with multiple connectors, keep them close together

Multicard systems and connectors

Differential signaling through connectors

- here we see again an advantage of the differential signaling:
if the currents on the two wires of a differential pair are exactly balanced ($\Sigma\text{current} = 0$), then there can not exist any return current over false (parasitic) paths regardless of the connector impedance



- for this to work, we must design the line driver, receiver and the termination network in order to guarantee that $\Sigma\text{current} = 0$, always.



Quiz time

4. You need to connect a uP on a PCB to a very fast data acquisition system (ADC) located on another PCB. How would you connect the two circuits for best performance (speed and EMC) ?

Explain your choice.

(in all cases, the signals are passed through a backplane connection):

- connect the ADC directly to the uP's fast local (parallel) bus
- use a high speed serial differential channel (LVDS)
- use a parallel bus with optocoupler isolation

Reason:

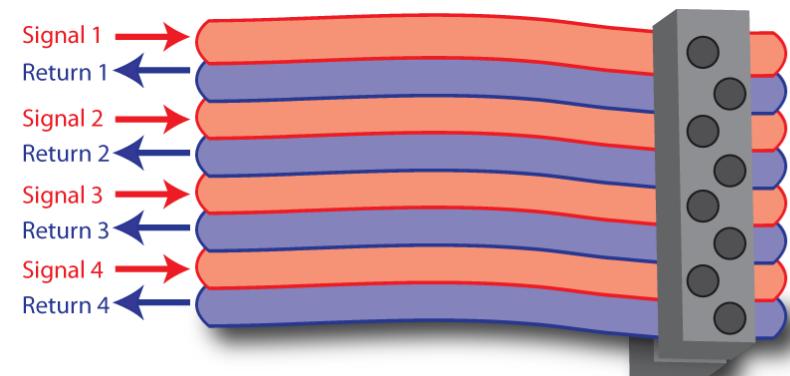
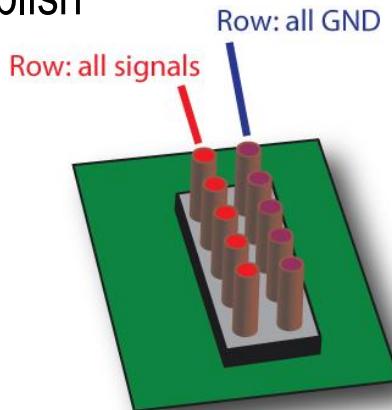
Passing fast signals over a backplane is always a headache. The best we can do is to reduce their number (i.e. using serial instead of parallel bus) and use a technology that is optimized for this purpose and allows easy impedance matching (termination). LVDS is such a technology, that uses differential signaling with very small voltage swing. At the same time, it is very fast, allowing it to achieve the same throughput as normal parallel busses.



Cables and cabinets

Ribbon (flat) cables

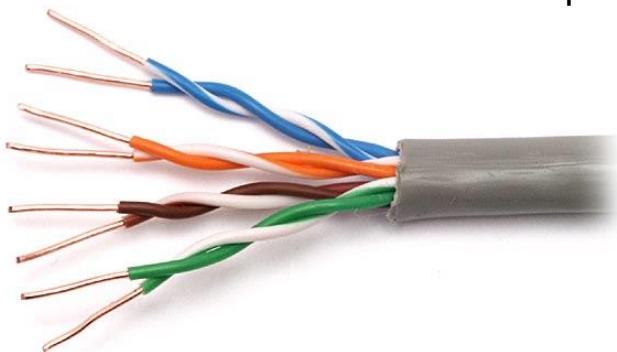
- Advantages:
 - controlled distance (\rightarrow impedance) between conductors.
 - good transmission line (over short distances) when using 2 adjacent wires for signal and return
 - easy to assemble (connector mounting)
- For the signal integrity reasons just discussed, every signal wire should have nearby its own return wire:
- This is easy to accomplish on the PCB:



Cables and cabinets

Twisted cables

- Every signal line forms a twisted pair with its own return line
- Advantages:
 - better than flat cables over longer distances
 - reduced emissions and crosstalk: at each twist, the effect reverses resulting in ≈ 0 in average
- Available shielded or unshielded versions (e.g. STP, UTP Ethernet cables)
 - Ethernet cable with twisted pairs:
 - Ribbon cable with twisted pairs:





Cables and cabinets

Shielded (coaxial) cables

- The ultimate (but costly) solution for wired high speed data transmission
- Advantages:
 - Excellent transmission line impedance control
 - Availability of impedance matched coax connectors up to 26 GHz and more
 - Perfect shielding (no emissions, no crosstalk, no external noise pickup) *when properly installed*
- **Improper** connection of the shield can **void (!!)** the advantages of a shielded cable

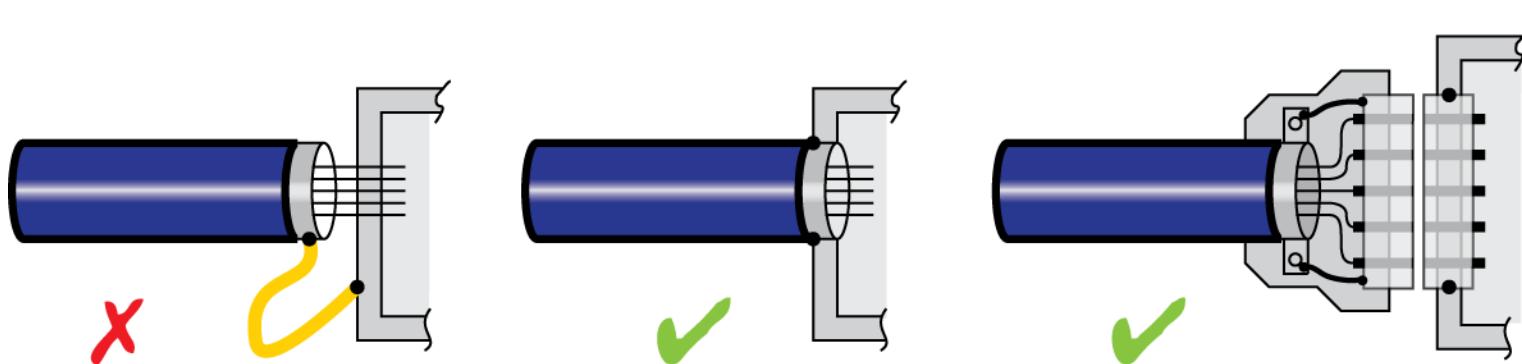


Cables and cabinets

Shielded cables – important considerations

1. Connect the shield directly to the cabinet's chassis
2. Use the shortest possible connection for this. Don't use "pigtails"!

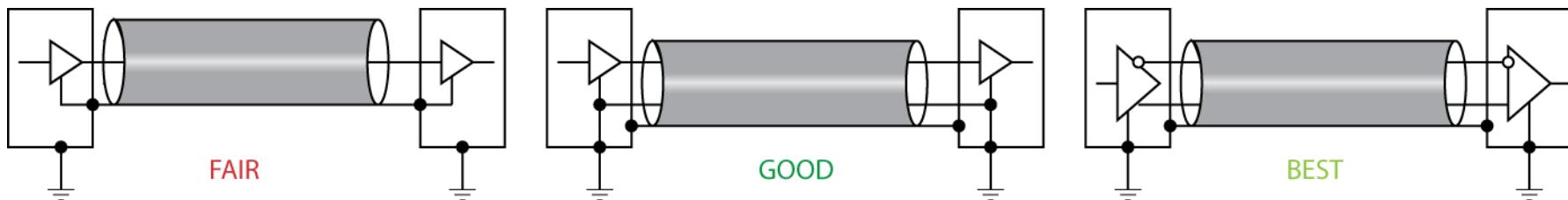
(list continues on next slide)



Cables and cabinets

Shielded cables – important considerations (cont'd)

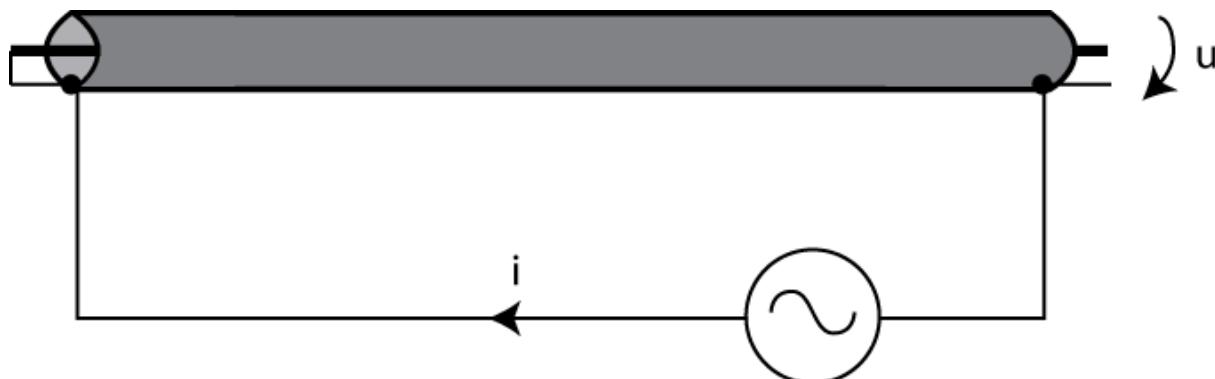
3. Connect the shield to the cabinet chassis (GND) at both ends of the cable.
Some older LF / audio textbooks recommend connecting the shield at one end only. This may work on a laboratory testbench, but is not recommended at system level. Instead of splitting the shield connection at one end, do the following to reduce 50Hz noise ("hum") in audio/video equipment:
 - improve ground connections (reduce impedance), e.g. using meshed ground
 - apply rule #4 and/or galvanic isolation
 - reduce loop areas by deploying the cables near the metallic structures (cabinets, rails). Keep noisy cables distant from small signal cables.
4. Avoid using the shield as return wire: instead use 2 wires (signal+return) plus shield. Best results are achieved when using (balanced) differential signaling on these 2 wires (and driver+receivers are balanced as well, with good CMRR)



Cables and cabinets

Shielded (and coax) cables – definition of Transfer Impedance

- Definition:



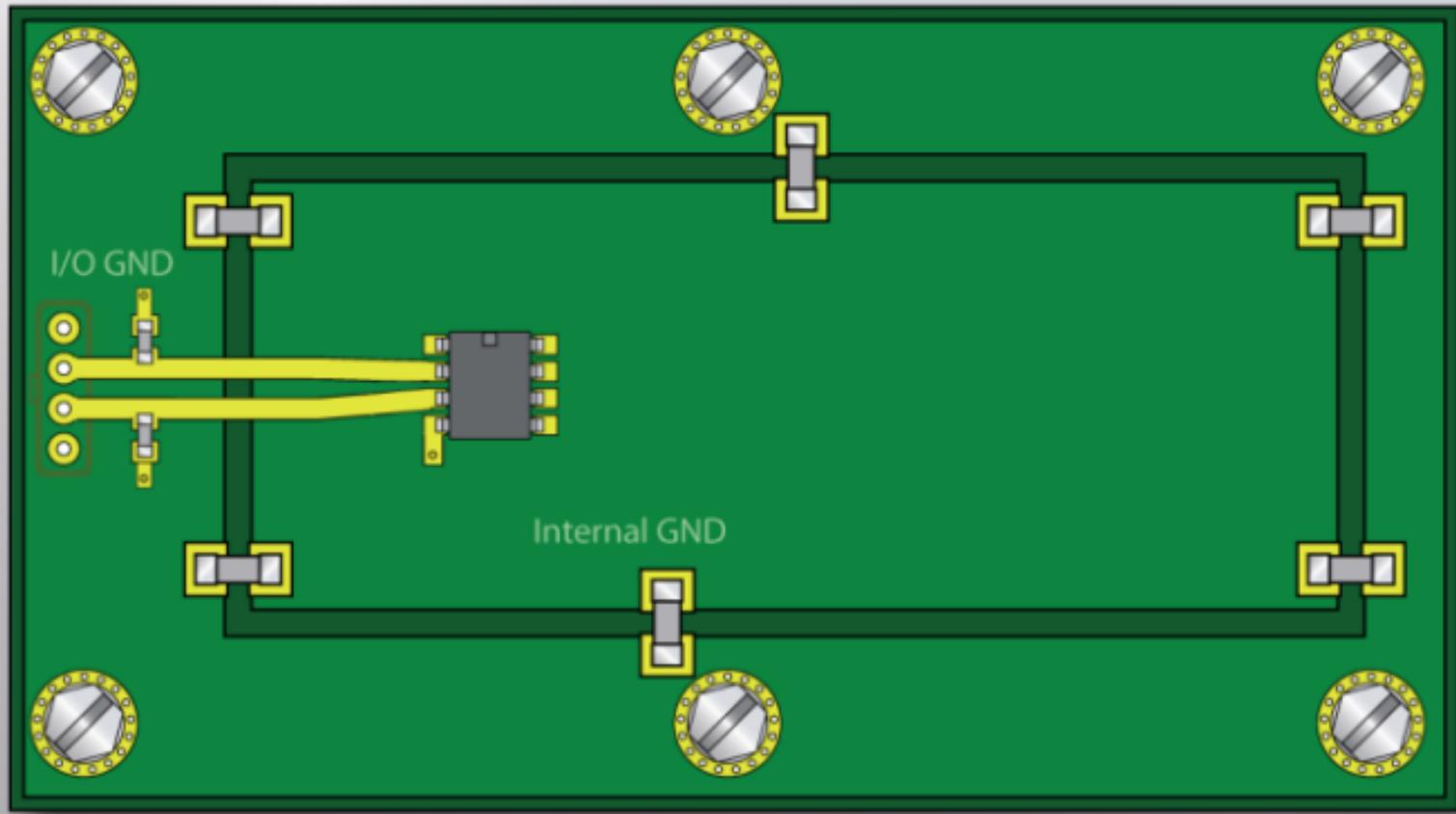
$$Z_{transfer} = \frac{u_{(measured)}}{i_{(applied)}} \quad [\Omega, \text{ per unit length}]$$



Cables and cabinets

EMI prevention measures on cables

- Filter the signals to remove high-frequency content. This slows the signal transitions. The filter must be located directly at the entrance of the cabinet or PCB and have an excellent GND/chassis connection.
- Shield the cable. Proper connection between the shield and the cabinet chassis is critical.
- Place a common mode choke on the cable. This increases the inductance of remote current paths, lowering their current flow.

$\lambda/10$ $\lambda/10$  $\lambda/10$

Cables and cabinets

Special situations

Remember: always first try to shield at PCB level (cheaper than at enclosure level)!

- Shielded cables with non-metallic cabinets:
 - connect the cable shields to a bottom metal plate (located under the PCB and connected to its GND with screws or bolts), using short connections (metal clamps, clips)
 - design a grounded guard ring around the PCB and connect the cable shields to it
- Isolated coax connections (e.g. 10Base2 Ethernet with coax cable)
 - apply signal filtering, common mode chokes
 - shunt the cable shield to the cabinet's ground through a capacitor
 - apply galvanic isolation for the signal (transformer, optocoupler)
- Unshielded cables with metallic cabinets: (see slide: "EMI prevention measures on cables")
 - filter the signals near their entry point into the cabinet
 - apply common mode filters on the cables

Cables and cabinets

Electrostatic discharge (ESD) and Burst protection

- Protect the electronic circuit from ESD and burst coming from the I/O cables:
 - partition the circuit
 - apply filtering immediately where the cable enters into the cabinet or the PCB
 - reduce loop areas, in particular with the I/O signals (signal and return path)
 - ground the PCB against the cabinet or bottom plate with multiple screws, bolts.
 - add some series impedance (R , L) in the input signals (from I/O cables, front panel buttons, keyboards): they reduce the overcurrents that can enter into the ICs
 - effectively ground cable shields against the cabinet's chassis
 - add ferrite clips on the cables
- A system that is robust against ESD and burst is usually also good from the radiated EMI emissions point of view



Quiz time

5. You need to connect a fast peripheral through a shielded cable. What cable should you take and why?

- 2 internal conductors + screen connected at both ends
- 2 internal conductors + screen connected only at one end
- 1 internal conductor + screen (coaxial cable)

5. How can you improve your circuit's immunity against ESD and Burst coming from input cables?

- if the cable is shielded, connect the cable's shield directly to the chassis. Do the same with the PCB's GND.
- partition the circuit carefully (keep sensitive circuits away from the I/O connector zone)
- filter the signals as soon as they enter into the PCB
- add series impedances (ferrites, resistors) to the input signals where they enter into the PCB
- make sure that I/O signals (and their return paths) do not form large loops, therefore reducing the risk of coupling with HF fields)

An Application Case

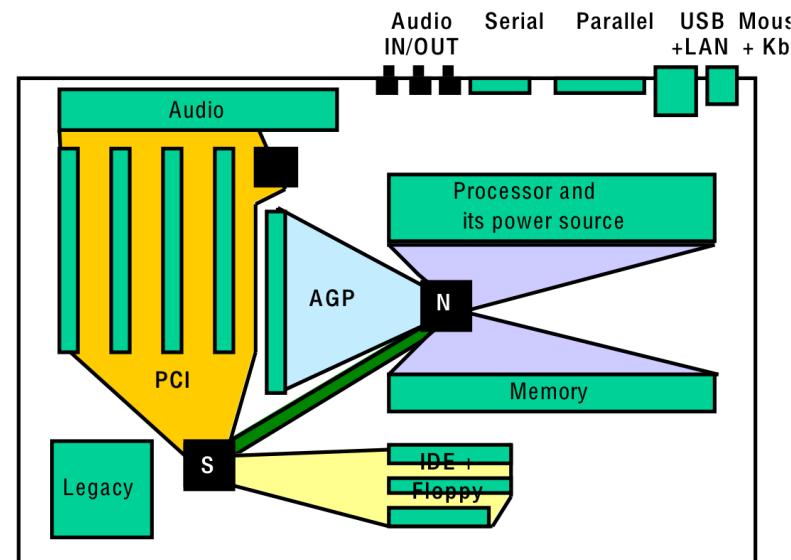
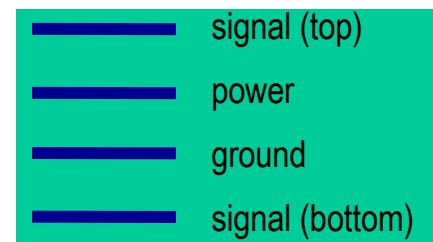
USB High Speed (480Mb/s) host controller platform

An Application Case

USB High Speed (480Mb/s) host controller platform

(source: Intel document: "High Speed USB Platform Design Guidelines")

- The guideline is for a 4-layer PCB
 - fast signals on bottom
 - most routing on bottom
 - more room for components on top
- High speed USB host controller implemented on a PC main board
- The USB host controller is connected to the PCI bus
- USB controller chip is from NEC



An Application Case – USB High speed platform

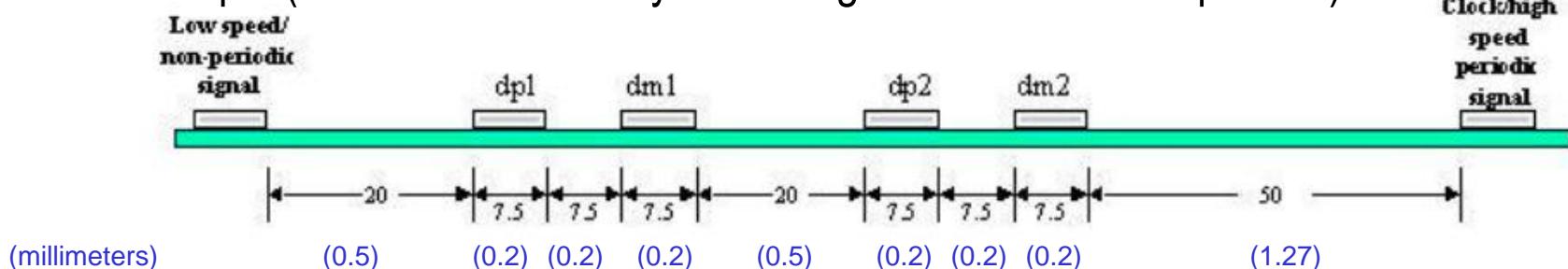
Component placement and trace routing recommendations

| Item | Description |
|------|--|
| 1 | Place the high-speed USB host controller and major components on the unroute board first. |
| 2 | With minimum trace lengths, route high-speed clock and high-speed USB differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to high speed USB differential pairs and any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors). |
| 3 | Route high-speed USB signals on bottom whenever possible. |
| 4 | Route high-speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes. |
| 5 | When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities. |
| 6 | Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks. |
| 7 | Stubs on high speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, no stub should be greater than 200 mils. (<u>5mm</u>) |
| 8 | Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces as much as practical. |
| 9 | Route USB trace pairs together. |
| 10 | <u>9.12.</u> Keep high-speed USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out. |

An Application Case – USB High speed platform

USB traces and terminations

- USB signaling uses differential pair forming a transmission line with $Z_0 = 90\Omega$
- The example is for a PC with two USB ports
- Example (dimensions can vary according to the PCB stackup and ϵ)

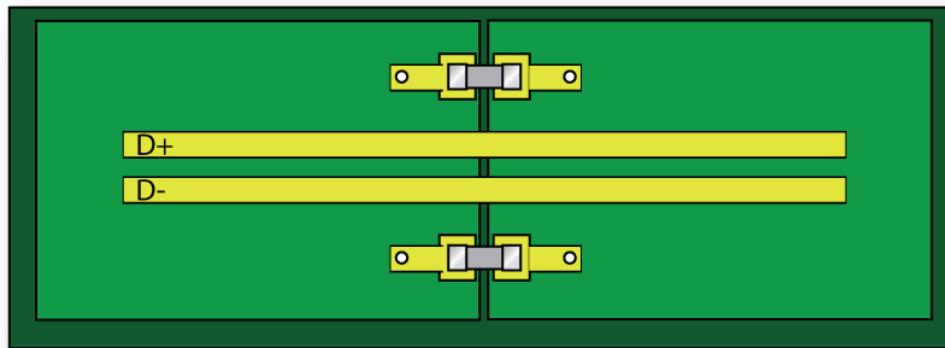


- These distances ensure low crosstalk between USB pairs and/or other signals
- Signal pairs require termination resistors. Place them as close as possible to the USB controller chip
- Length differences between the signal traces of a USB pair should be 150mils (3.8mm) or less

An Application Case – USB High speed platform

Ground planes and layer changes

- Do not split the reference planes (use uninterrupted planes, in particular for GND)
- If plane splits are unavoidable and USB signal traces need to cross them, provide stitching capacitors next to the traces to guarantee a close return path
(USB signaling is not purely differential in all speeds (i.e. the FS Single Ended Zero is common mode))

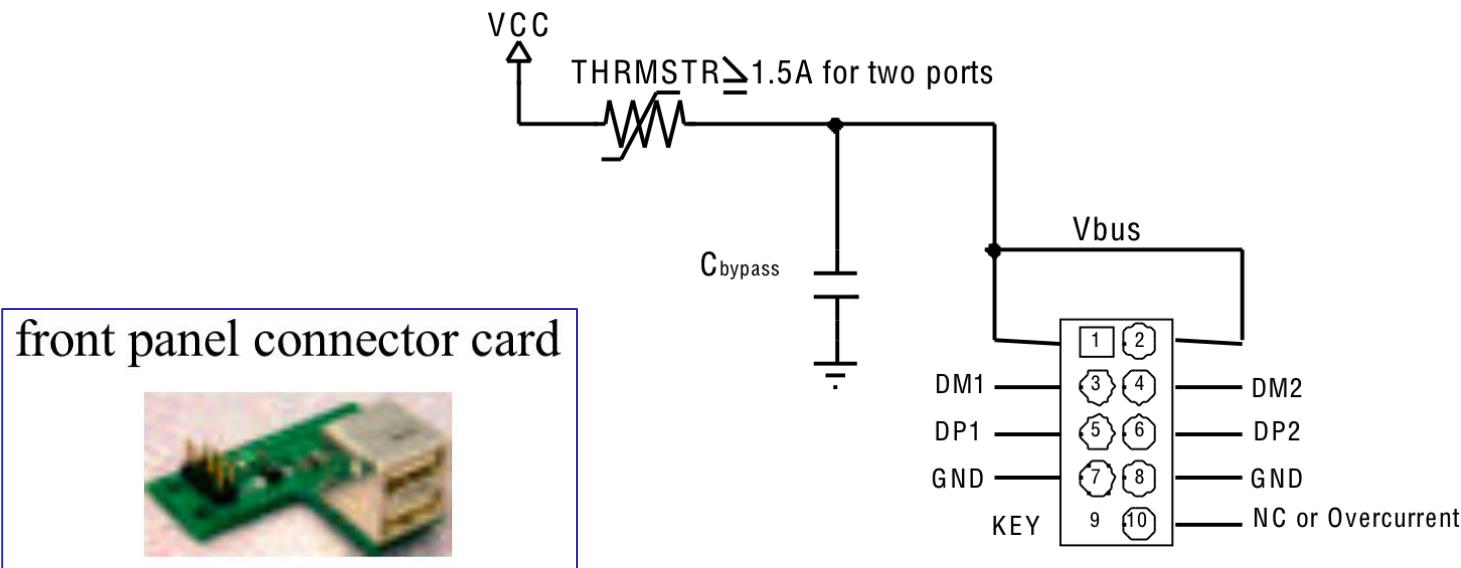


- Avoid changing layers with the signals as much as possible.
- However, changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

An Application Case – USB High speed platform

Front panel connector

- In certain designs, the two USB connectors are mounted on a small carrier board at the front panel
- Connection between the main board and front panel board is through a cable
→ **only** use 90Ω cables approved for USB
- Recommended cable connector pinout on the main board:





An Application Case – USB High speed platform

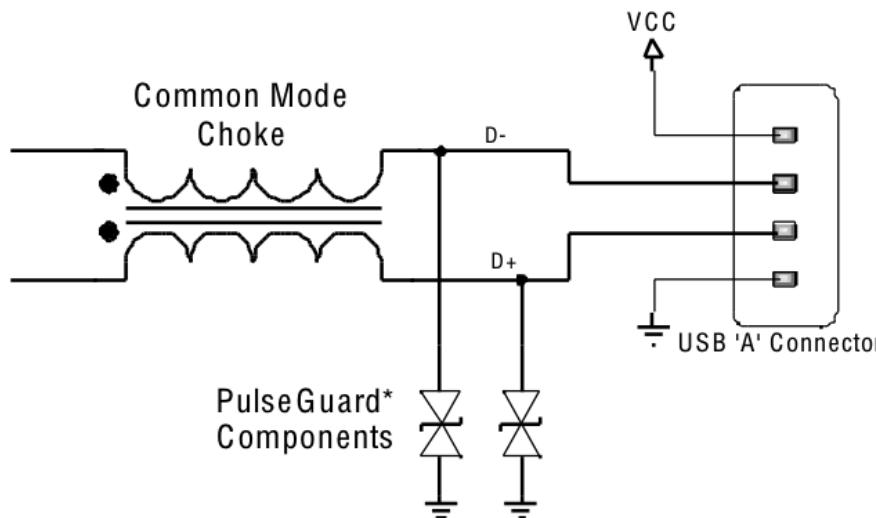
Remaining components placement

| Item | Description |
|------|---|
| 1 | Locate high current devices near the source of power and away from any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors.) This reduces the length that the return current travels and the amount of coupling to traces that are leaving the PCB.. |
| 2 | Keep clock synthesizers, clock buffers, crystals and oscillators away from the high speed USB host controller, high speed USB traces, I/O ports, PCB edges, front panel headers, power connector, plane splits and mounting holes. This reduces the amount of radiation that can couple to the USB traces and other areas of the PCB. |
| 3 | Position crystals and oscillators so that they lie flat against the PCB. Add a ground pad with the same or larger footprint under crystals and oscillators having multiple vias connecting to the ground plane. These will help reduce emissions. |

An Application Case – USB High speed platform

Filtering and protection devices

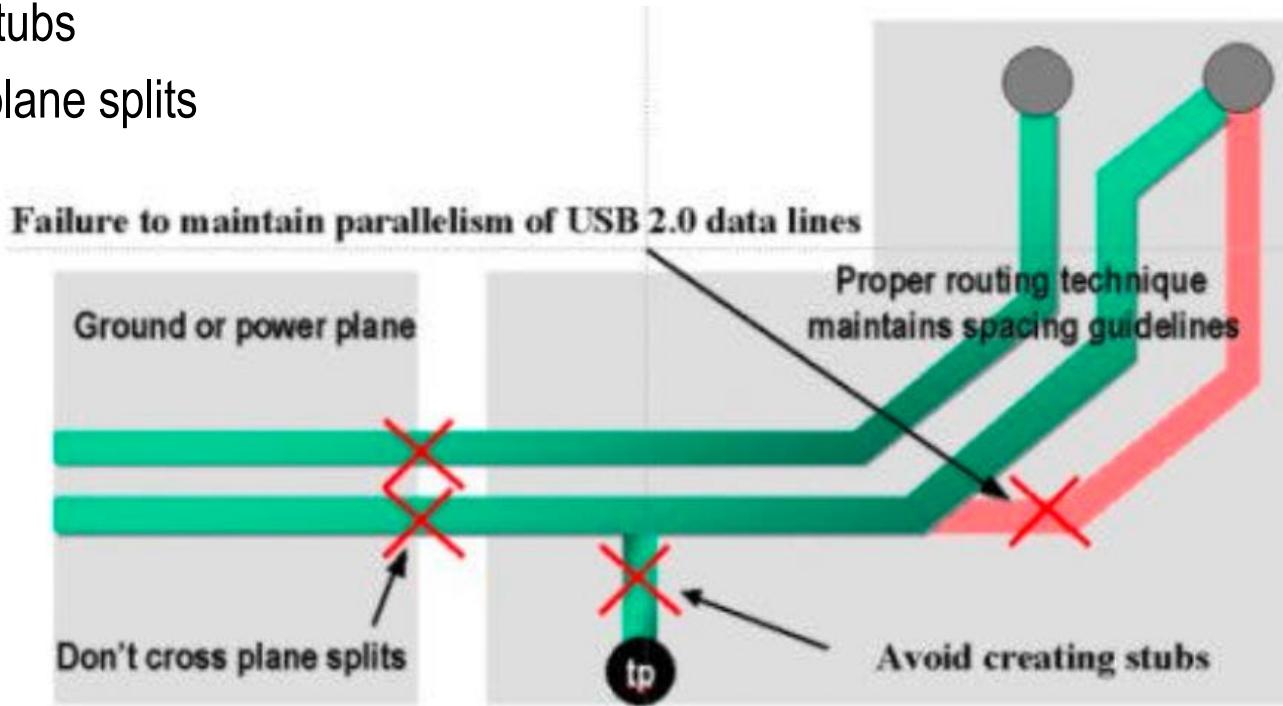
- Use common mode chokes only if strictly necessary for EMI, as they reduce the quality of the very fast USB signals
- Carefully select overvoltage protection devices, as they degrade the signal due to their capacitance



An Application Case – USB High speed platform

Frequent mistakes

- failing to maintain trace parallelism
- creating stubs
- crossing plane splits





2-Layer PCBs

Why use 2-Layer PCBs today?

- Old technology, not recommended for new designs!
- Today, a 4-layer PCB costs only 20% more than a 2-layer
- Only usable if the circuit operates **below 5MHz** and has signal transitions **slower than 5ns ("5/5 rule")**
- Main concern: missing GND plane:
 - Signal integrity problems, emissions
 - Less intrinsic decoupling between VCC and GND

Should you still need to design a 2-layer PCB, here are some suggestions:

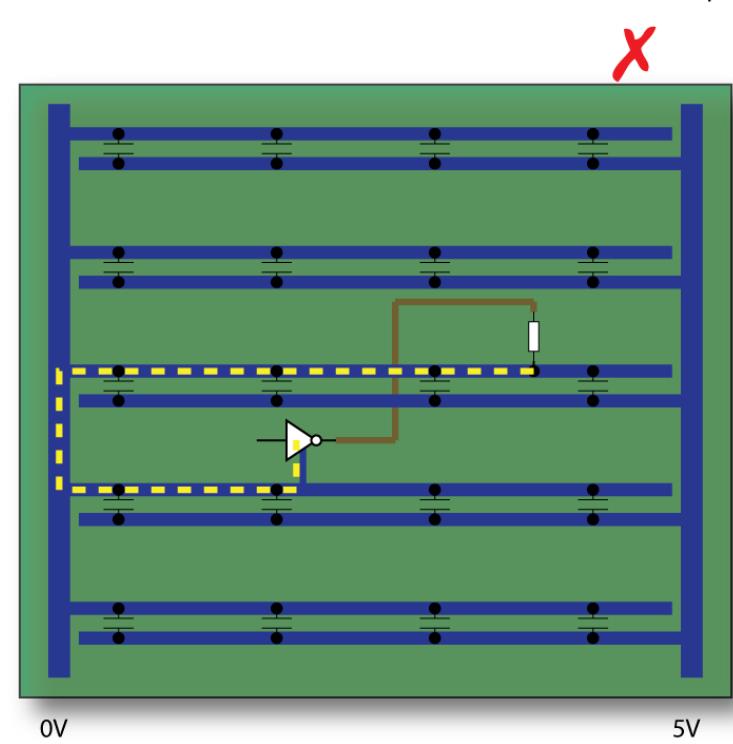
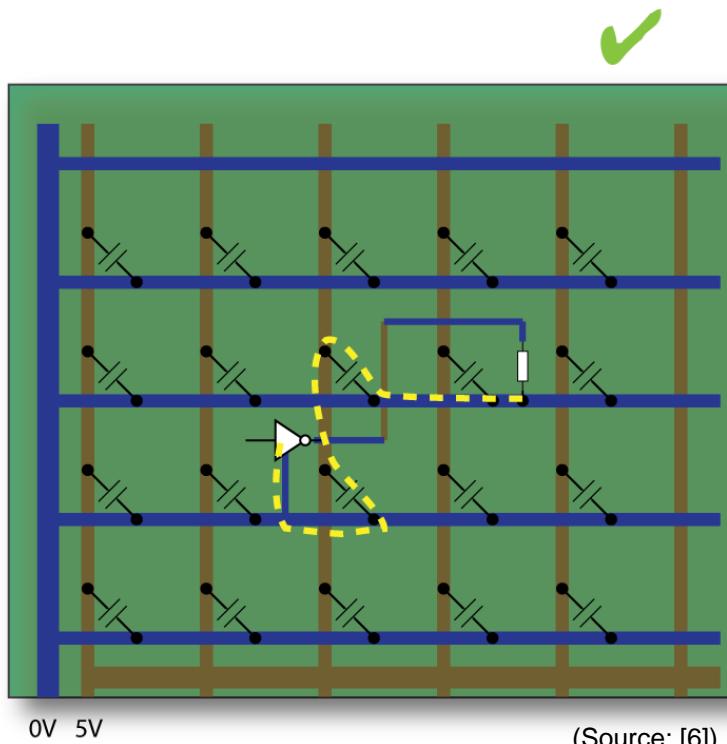
- Try to route all signals and VCC on one layer, leaving the other layer as a solid GND plane (microstrip technology). **Best solution.**
- If this is not possible, see more suggestions on the next slides ...

2-Layer PCBs

VCC and GND routing

- Use orthogonal VCC and GND layout (route these traces first!)
- At the end of the routing, try to close as many GND meshes as possible by adding vertical GND lines (on top or bottom)

top
bottom
return path





2-Layer PCBs

Some other general recommendations

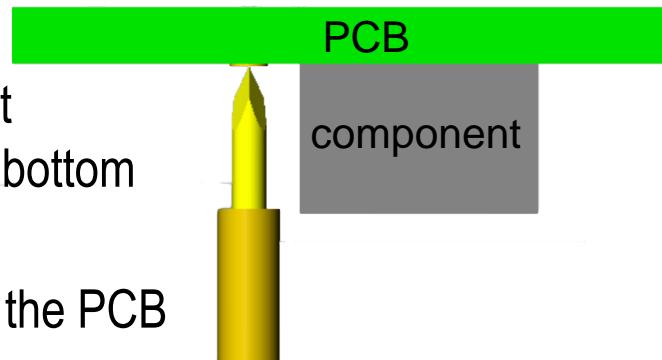
- Fill unused areas with copper and **connect them to GND**
- Draw a dedicated signal return trace (i.e. an additional GND trace) adjacent to critical signal traces (fast clock or low voltage analog signals)
- If possible, draw small GND areas (islands) under critical components (oscillators, low voltage signal amplifiers)
- Use a lot of decoupling capacitors and connect them with short traces, forming small loops
- Partition the layout carefully in function blocks (analog, digital, power, etc)
- **But:**
Think twice before discarding the much better multilayer solution. The money you save in PCB costs with a 2-layer PCB will be spent, multiplied by a factor 10x or 100x in tweaking the 2-layer PCB and adding filtering, to pass the CE EMI requirements or to meet your own project specifications!

Design for testability (DFT)

Some general guidelines to make the PCB testable (1)

Test points for in-circuit test:

- Add a test point (it can also be a vias) on each net of the PCB. Place the test point preferably on the bottom (solder) side. It must be solder covered.
- Place 3 non-plated tooling holes at the corners of the PCB (for automated fixing/tooling of the PCB)
- Fill all vias with solder or soldermask (for vacuum actuated fixtures)
- Check your PCB manufacturer's rules for test point dimensions and min. distances
- BGA devices should have 100% access to all pins from the bottom side
- Thin PCBs can be difficult to test because they can bend under the pressure of the test probes
- Add test points to the power supply pins of each IC

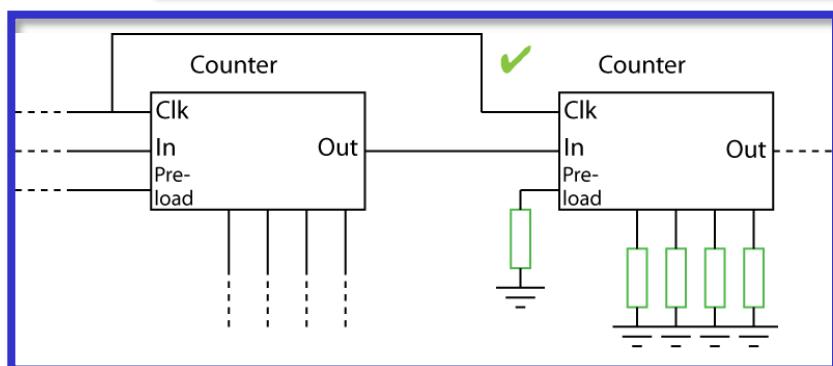
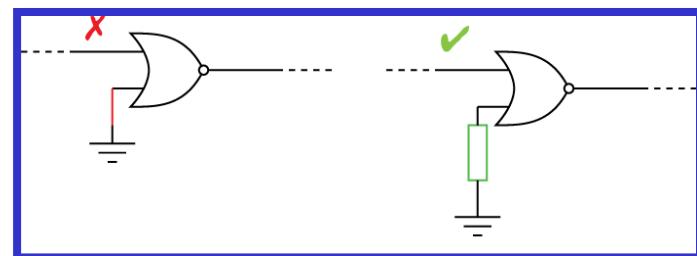
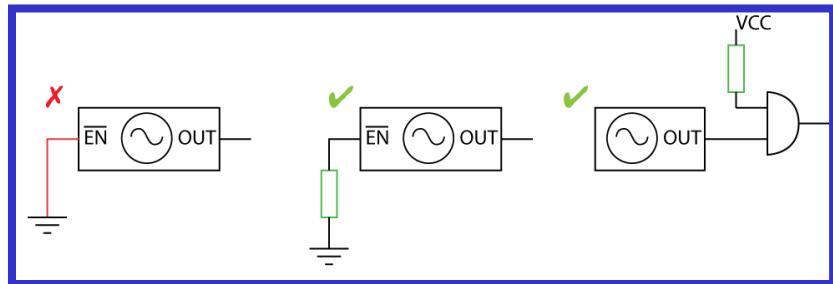


Design for testability (DFT)

Some general guidelines to make the PCB testable (2)

Electrical rules:

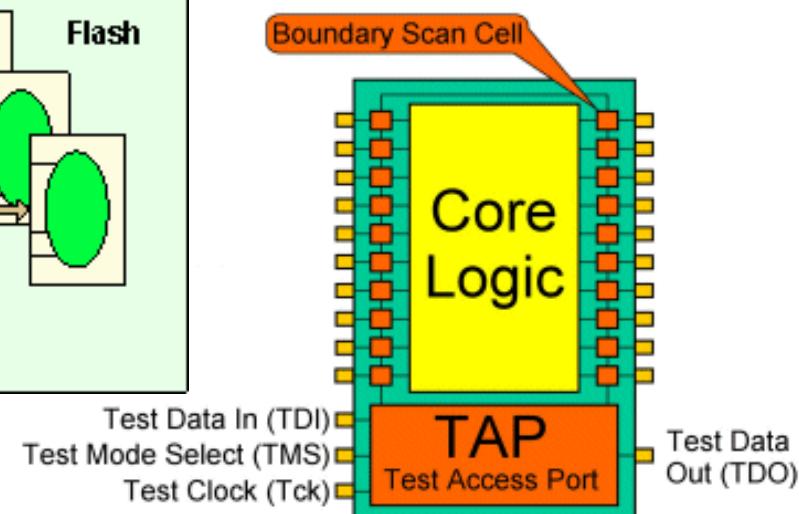
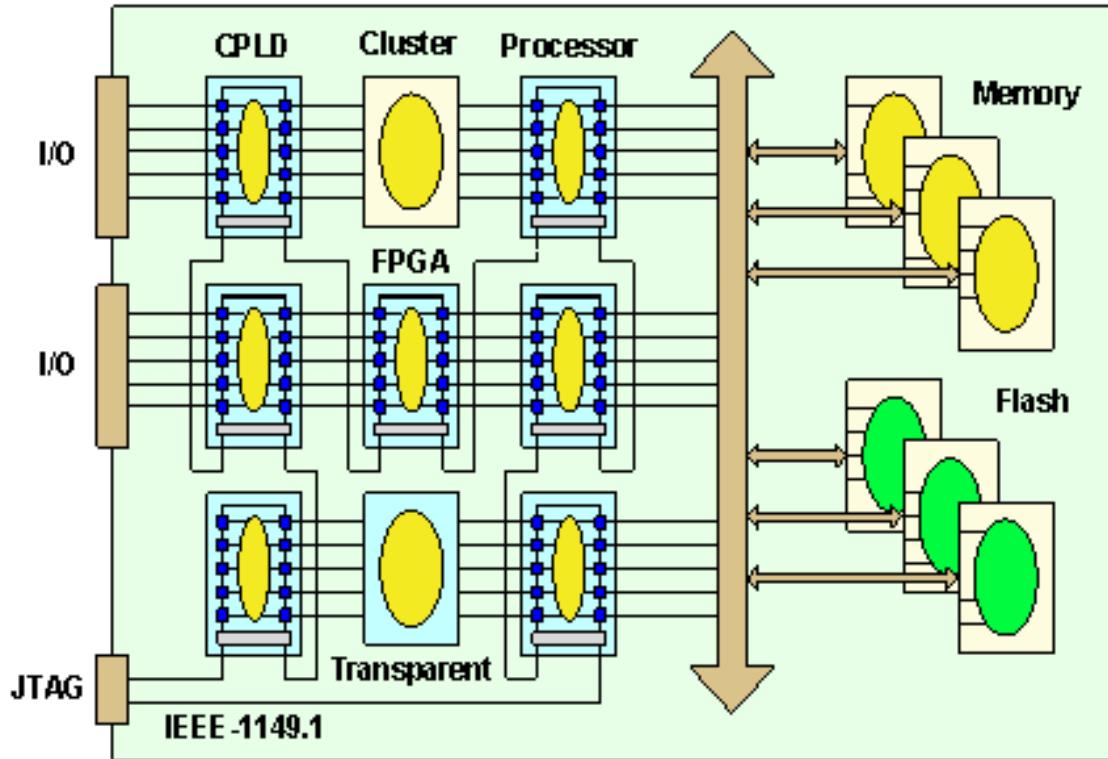
- Make it possible to disable oscillators
- Add a test point to a Reset input
- Tie unused inputs to GND through a resistor
- Break serial chains (e.g. counters) with test points in order to allow pre-loading (this reduces test duration)



Design for testability (DFT)

Some general guidelines to make the PCB testable (3)

- Make use of "Boundary Scan" (IEEE 1149.1):





Quiz time

7. Give some reasons why a 2-layer PCB is not a good choice from electromagnetic compatibility (EMC) and signal integrity point of view.

Answer:

the problem with 2-layer PCBs is that generally both layers are used for signals and therefore there's no continuous GND and VCC plane. Signals and their return paths generally form larger (uncontrolled) loops, therefore increasing emissions and signal integrity problems (crosstalk, reflections, etc). The missing GND (and VCC) plane also means more GND noise and less intrinsic decoupling capacitance between VCC and GND.

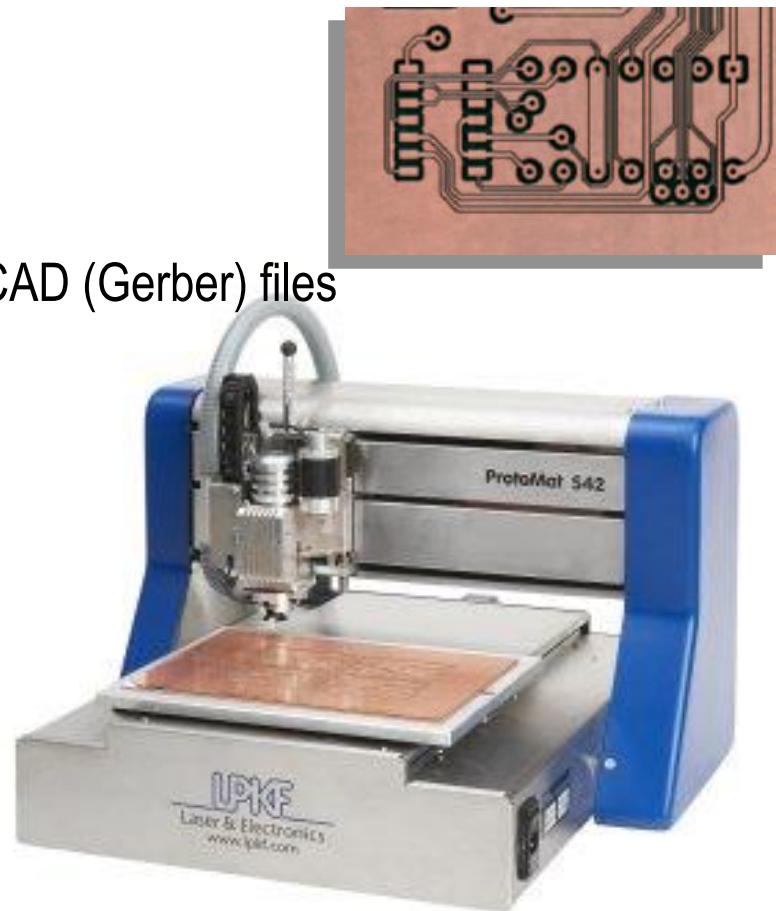
7. Test points

- can be placed near any component, regardless of its height
- should be added to each signal net on the PCB
- need not to be added to input pins that are tied to VCC or GND

Prototyping

Milling / drilling plotter

- Can prepare 2-layer PCBs starting from CAD (Gerber) files
 - Minimum track width: 4 mils (0.1 mm)
 - Minimum isolation width: 8 mils (0.2 mm)
 - Minimum drill hole diameter: 12 mils (0.3 mm)
- Prototypes and also small series
- Suitable for RF circuits
- Optional additional tools:
 - Press to assemble "multilayer" boards
 - Hole metallization system:

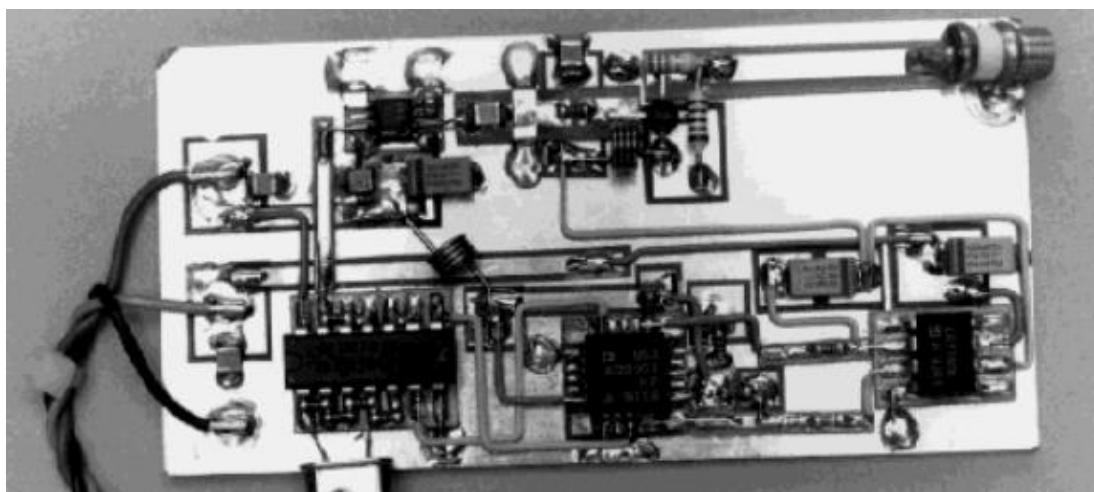
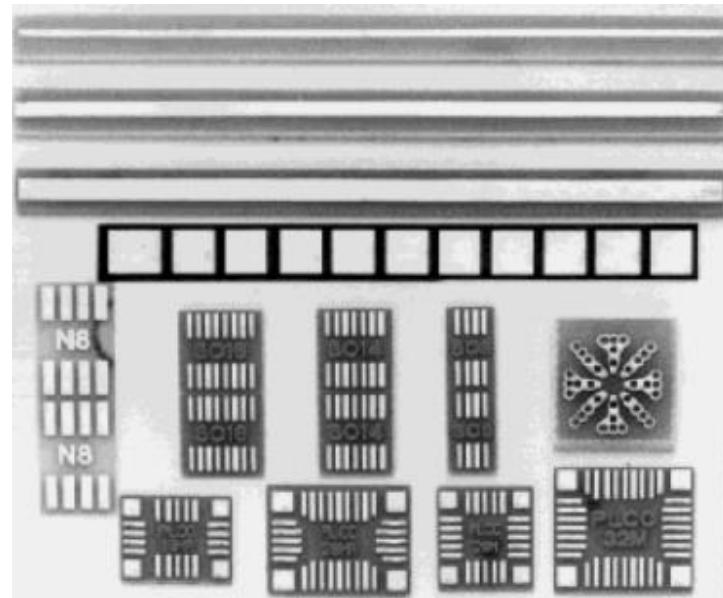




Prototyping

Mini-Mount®

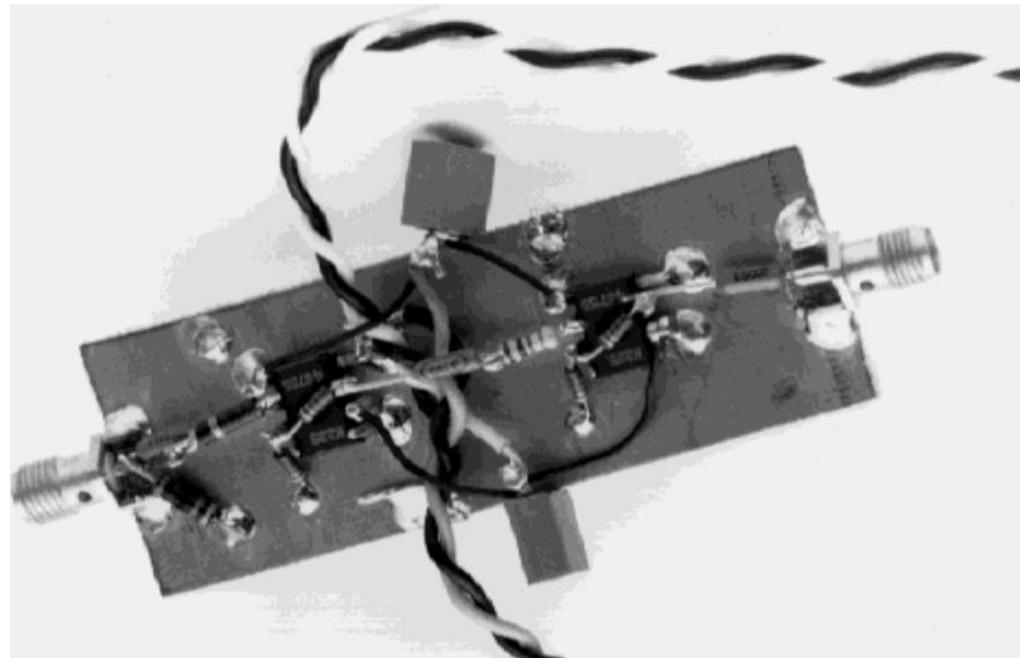
- A collection of small pieces of PCB with etched patterns (for ICs, discrete components, transmission lines, etc) on one side and contact adhesive on the other
- Assemble prototypes by sticking the pieces on a solid copper plane and soldering components on them
- Analog and high frequency circuits.
- Good for transmission lines (variants with 50Ω , 60Ω , 75Ω or 100Ω are available)



Prototyping

"Air mount" over a copper plate

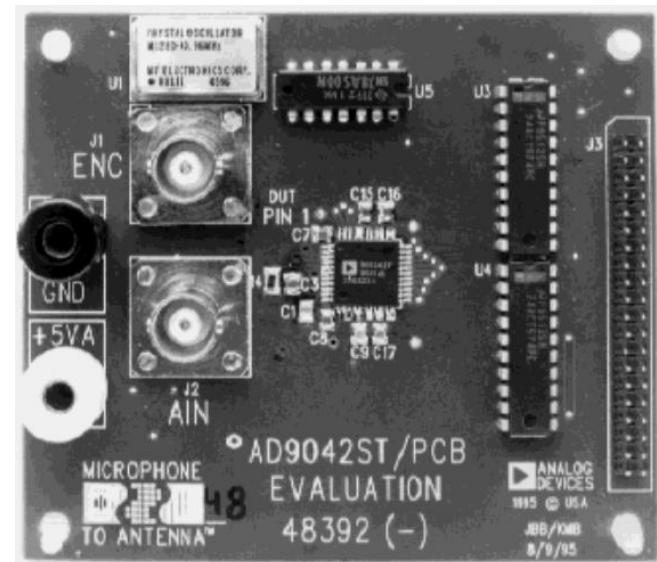
- The copper plate is the GND plane. Directly solder GND pins of the ICs to it.
- Components and wiring is implemented "in the air" above the copper plate
- Keeping wires at low height from the plate yields a fairly good "image plane" effect



Prototyping

Evaluation kits

- When available, it is always worth to invest in an evaluation board:
 - the circuit is mounted and operational
 - connectors already mounted
 - schematics and example software (when the kit includes a uP) are provided
 - good starting point and example for the own PCB layout
 - expected results (scope waveforms) are included and useful for verifications

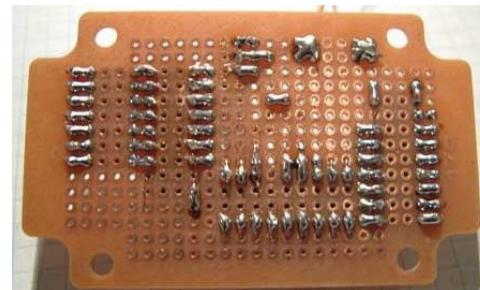
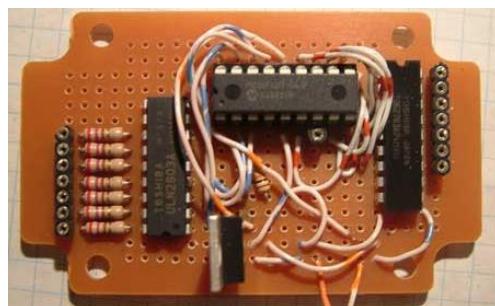
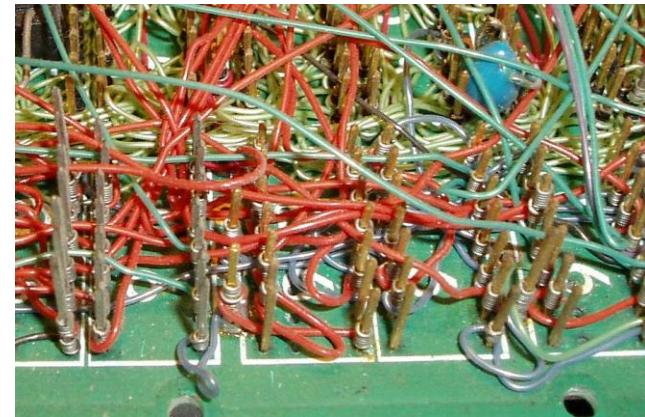
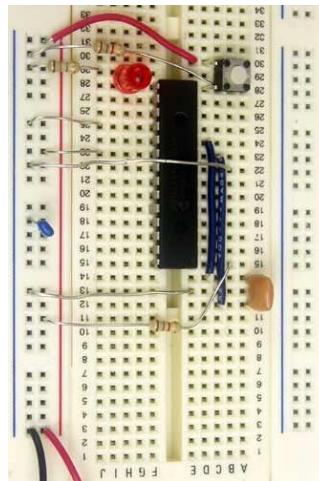
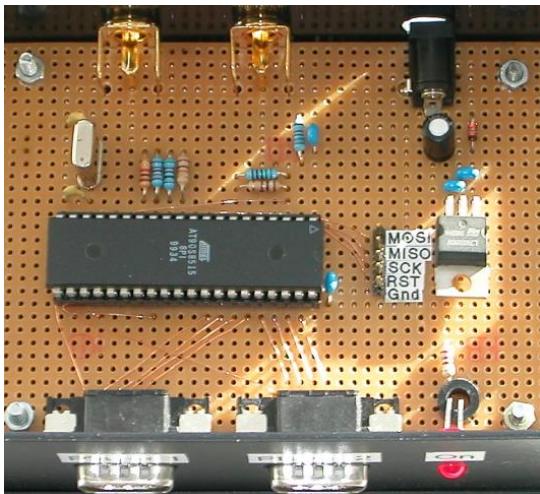


(Source: [1])

Prototyping

Old techniques

- These techniques **should be avoided**, unless you have a very slow circuit that is insensitive to noise and crosstalk



Prototyping

Some PCB manufacturers have special offers for prototyping

- starting from 1 piece: 2 and 4 layer PCBs
- 6 day lead time

Single-Pool
The perfect and low priced solution for 1 to 4 pcs. **PCB Prototypes** with 2 or 4 layers (No Discount on Re-Order).
Attention: from 4 pieces ECO-POOL (with Discount on Re-Order) is mostly lower priced!

No hidden costs!

PCBs always INCLUDING:

- ✓ ca. 6WD Production Time* (standard)
- ✓ Design Rule Check
- ✓ E-Test
- ✓ Solderstop 2x
- ✓ Marking print 1x
- ✓ Gerber-, Eagle-, Target- Import
- ✓ Tooling cost
- ✓ Photoplot
- ✓ Tracks: 150µm min.
- ✓ Annular Ring: 150µm min.
- ✓ Drills: 0.3mm min.
- ✓ Unlimited Drills
- ✓ Milled outline
- ✓ Surface HAL leadfree (**RoHS compliant**)
- ✓ Material FR4 1.55mm
- ✓ 35µm Cu

Optional:
with surcharge

- ✓ Express from 48h
- ✓ Drills: 0.2mm min. (+15%)
- ✓ Routing: € 0,03 per mm
- ✓ Tracks: 125µm min. (+15%)
- ✓ Tracks: 100µm min. (+30%)
(100µm not with **complex panel**)
- ✓ If needed: Overproduction at ¼ Price! ?

Pricing Examples:

2 Layers
41 €
1dm² = (100mm x 100mm)

4 Layers
126 €
1.6dm² = (100mm x 100mm)

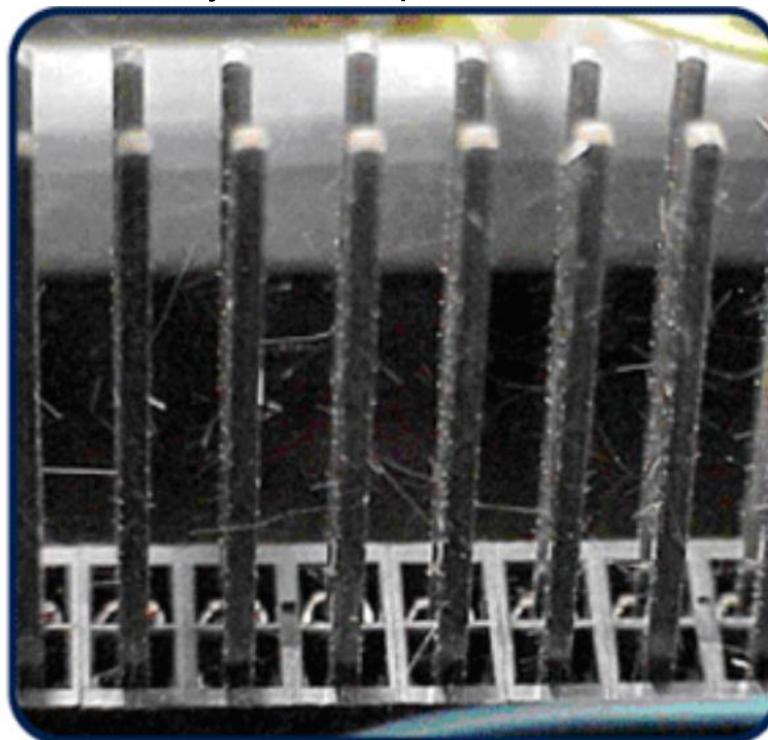
*4 Layers: 8WD Production Time

Directly from your Data:

ROHS

Can lead-free (no Pb) tin generate whiskers?

- This discussion is still open
- Lead-free tin is used as solder and to plate electrodes (connectors, etc)
- Risk of short circuits after 5-10 years of operation?





Computer Simulation Tools

Electromagnetic simulation software

- Helps improve the chance of first success in PCB layout (in particular at higher frequencies)
- Predict and mitigate signal integrity issues (crosstalk, line impedance, signal reflections, etc)
- Reduce problems with EMC compliance (emissions) at PCB or system level
- What if... analysis of the effect of different layouts and reference plane concepts
- Antenna and high frequency circuit design

- 2D and 3D solvers
- Various products from many companies, for example:
 - CST Microwave
 - Ansoft
 - Semcad
 - Agilent EEsof

- Most of them offer free "Student" versions (with very few limitations)

Exercise

9. A good pinout for a ribbon cable is:

- 1: signal, 2: signal, 3: GND, 4: GND,
- 1: signal, 2: GND, 3: signal, 4: GND,
- 1: GND, 2: signal, 3: GND, 4: signal,
- 1: GND, 2: signal, 3: signal, 4: signal,



Exercise

10. Explain the reasons why/how crosstalk can happen on connectors

Answer:

(see slides Series 12+13):

- inductive crosstalk can happen when the loop areas of different signals with their return wire partially overlap (mutual inductance). To avoid this, reduce the area that each signal forms with its return signal: the best is to reserve a return wire next to each signal wire
- crosstalk can also happen due to a non-zero impedance on the return path (GND) that is shared among two or more signals.

Thank you!

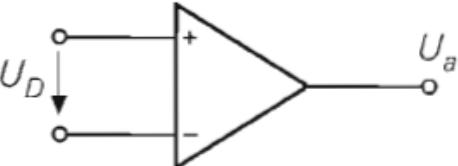
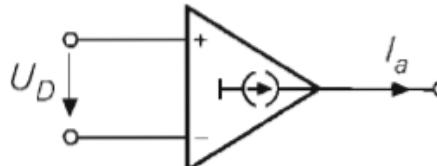
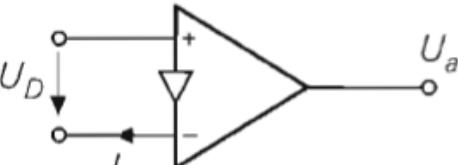
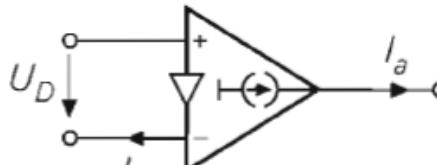


Contents

- Introduction and recall of operational amplifier theory
- Voltage amplifiers
- Low power operation
- High speed operation

- Exercices
- References

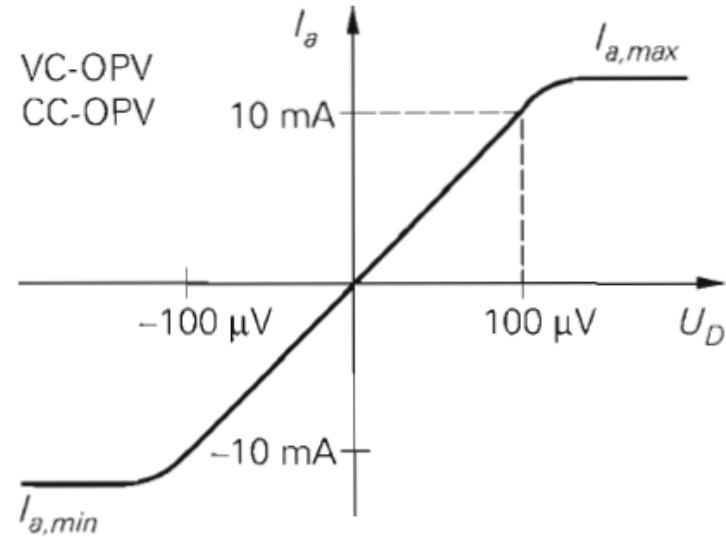
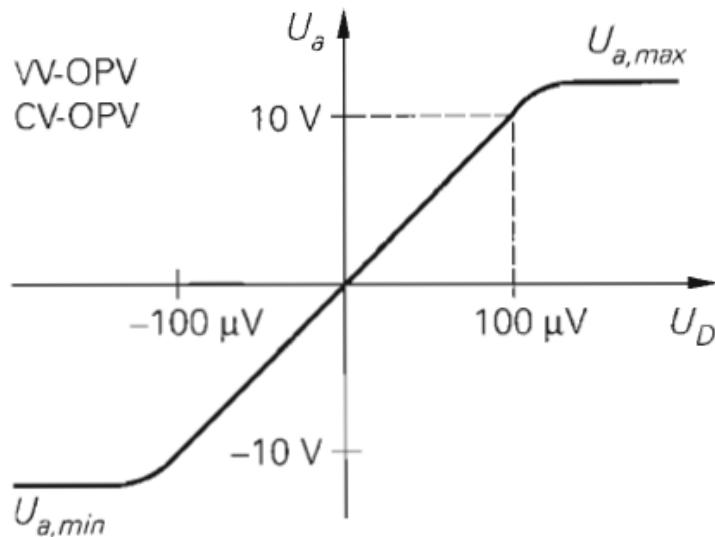
Categories of ideal operational amplifiers

| | Voltage output | Current output | |
|-----------------------------------|---|--|-----------------------------------|
| Voltage controlled voltage source | <p>Normal opamp VV-opamp</p>  $U_a = A_D U_D$ | <p>Transconductance opamp VC-opamp</p>  $I_a = S_D U_D$ | Voltage controlled current source |
| Current controlled voltage source | <p>Transimpedance opamp CV-opamp</p>  $U_a = I_N Z = A_D U_D$ | <p>Current opamp CC-opamp</p>  $I_a = k_I I_N = S_D U_D$ | Current controlled current source |

Transfer characteristics of operational amplifiers

The gain is

- very high (ideally infinite), and
- limited at or close to the supply voltages (reduced by an output resistance).



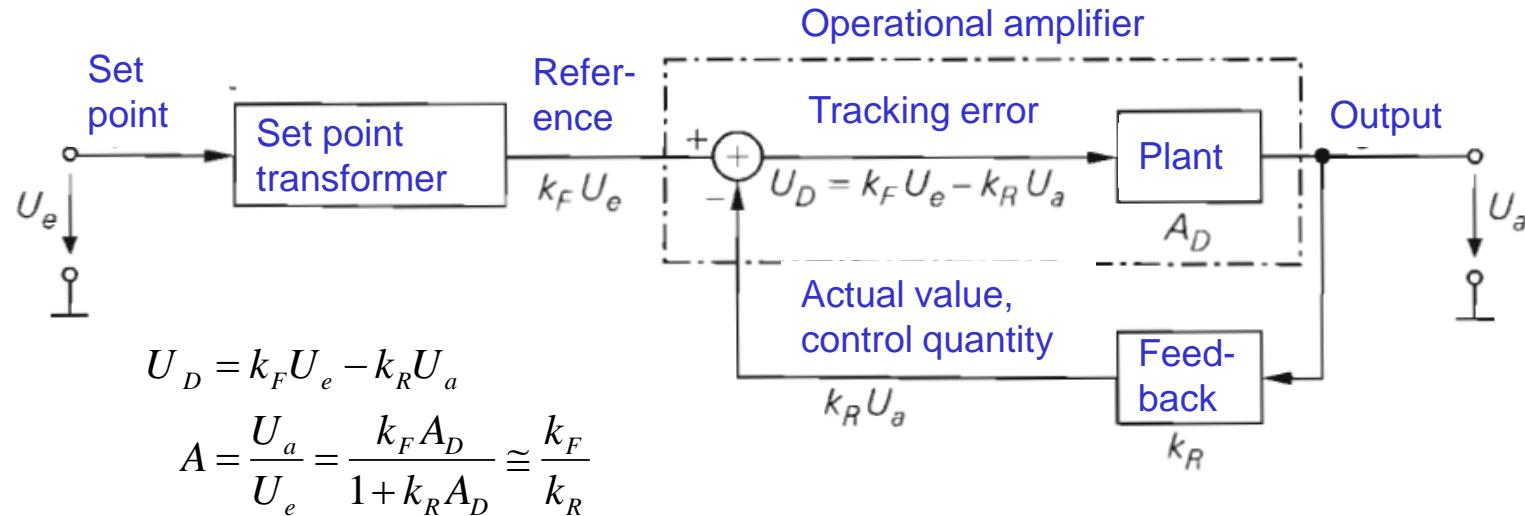
With the high gain

- difference between input potentials is close to zero, and
- virtually (ideally) input potentials are identical.

Other hypotheses for simplified analysis of operational amplifier circuits :

- input resistances are very high (ideally infinite), and
- output resistance is very small (ideally zero).

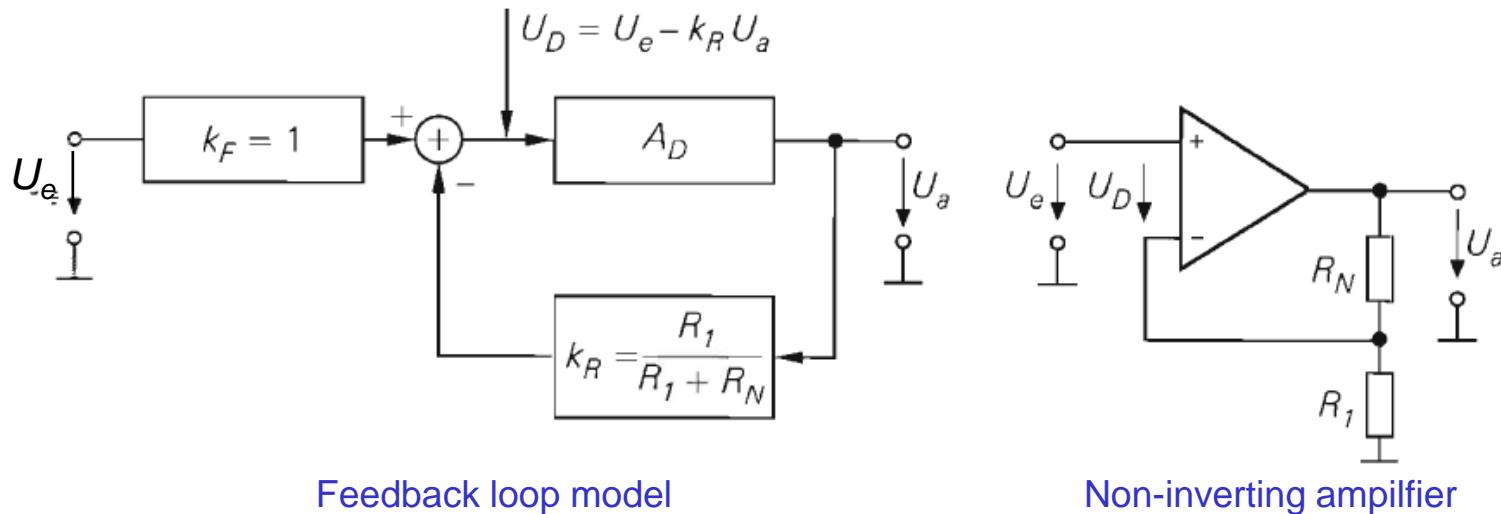
Control loop block diagram



Linear operational amplifier based circuits may be regarded as feedback loops:

- Part of the output voltage is compared to the weighted input difference voltage.
- With infinite feedback loop gain $g = k_R A_D$, simple determination of output voltage in function of input difference voltage.
- If the gain is 'very high' its precise value is without noticeable influence on the output.

Control loop representation of non-inverting amplifier



Feedback loop model

Non-inverting amplifier

$$U_a = A_D U_D = A_D (U_e - k_R U_a)$$

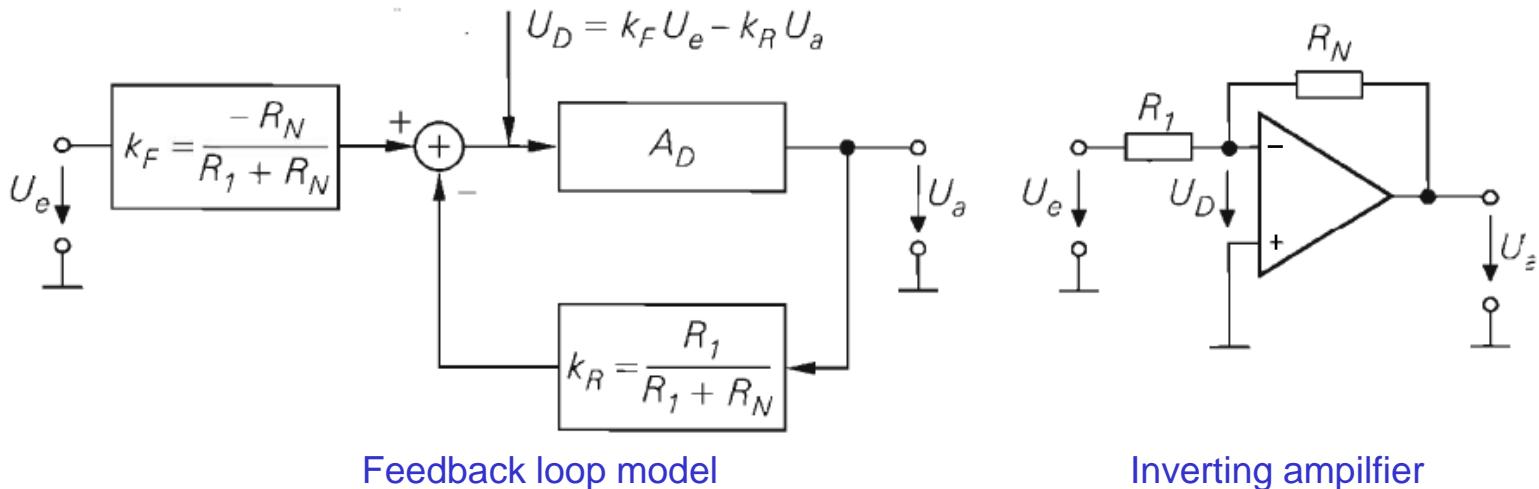
$$A = \frac{U_a}{U_e} = \frac{A_D}{1 + k_R A_D} \cong \frac{1}{k_R} = 1 + \frac{R_N}{R_1}$$

The simplification is valid if the loop gain $g = k_R A_D$ is very high.

Distinguish four gain definitions:

- open loop gain A_D
- closed loop input → output gain A
- feedback loop gain g
- feedback factor k_R

Control loop representation of inverting amplifier



$$U_a = A_D U_D = A_D (k_F U_e - k_R U_a)$$

$$A = \frac{U_a}{U_e} = \frac{k_F A_D}{1 + k_R A_D} \cong \frac{k_F}{k_R} = -\frac{R_N}{R_1}$$

For an ideal amplifier, both inputs are at virtual ground, and the node law yields: $\frac{U_e}{R_1} + \frac{U_a}{R_N} = 0$

If A_D is not infinite: $0 = \frac{U_e + U_D}{R_1} + \frac{U_a + U_D}{R_N} \Rightarrow 0 = R_N (A_D U_e + U_a) + R_1 U_a (A_D + 1)$

$$A = \frac{U_a}{U_e} = -\frac{R_N A_D}{R_1 A_D + R_N + R_1} = k_F \frac{A_D}{1 + k_R A_D}$$

Exercice:

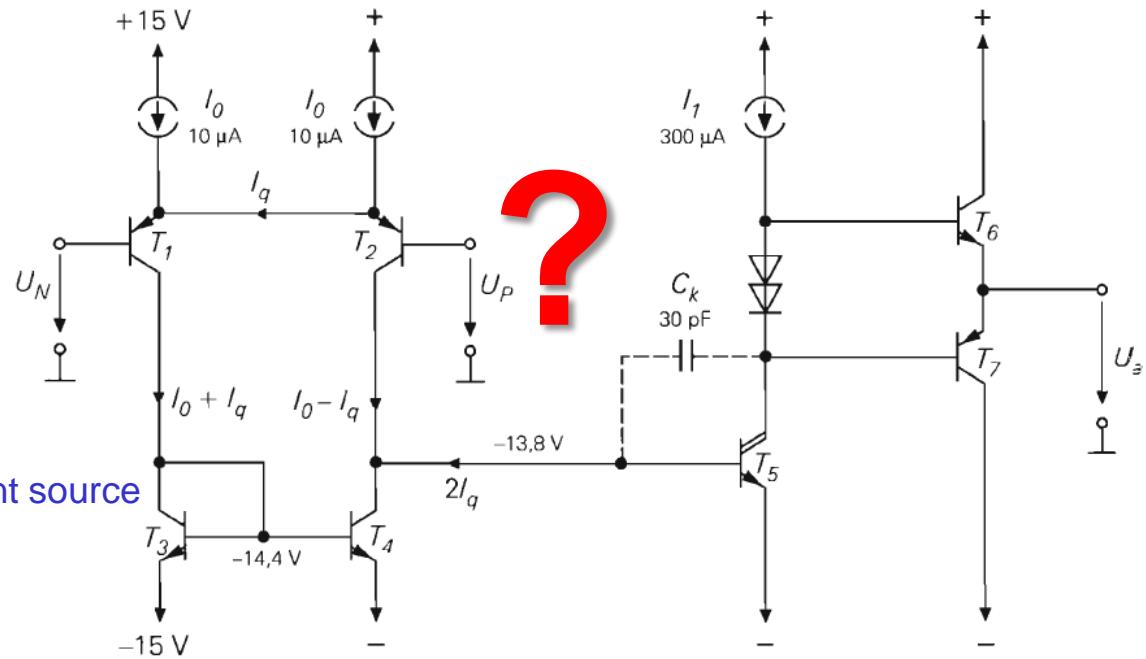
Control loop representation of differential amplifier

- Draw the schematic of a differential amplifier.
- Represent the differential amplifier by a control loop model, analogous to those for non inverting and inverting amplifiers.

What is inside an operational amplifier?

To understand operational amplifiers, also as a user, we need to have a basic understanding of internal circuits:

- 1) the differential amplifier
- 2) the current mirror and current source
- 3) the active load
- 4) the cascode circuit
- 5) the impedance converter
- 6) the push-pull amplifier
- 7) the Darlington transistor



In the following slides, we briefly review these circuit building blocks.

They will help us to understand specialized architectures, e.g. for rail-to-rail in- and outputs, and for high speed amplifiers.

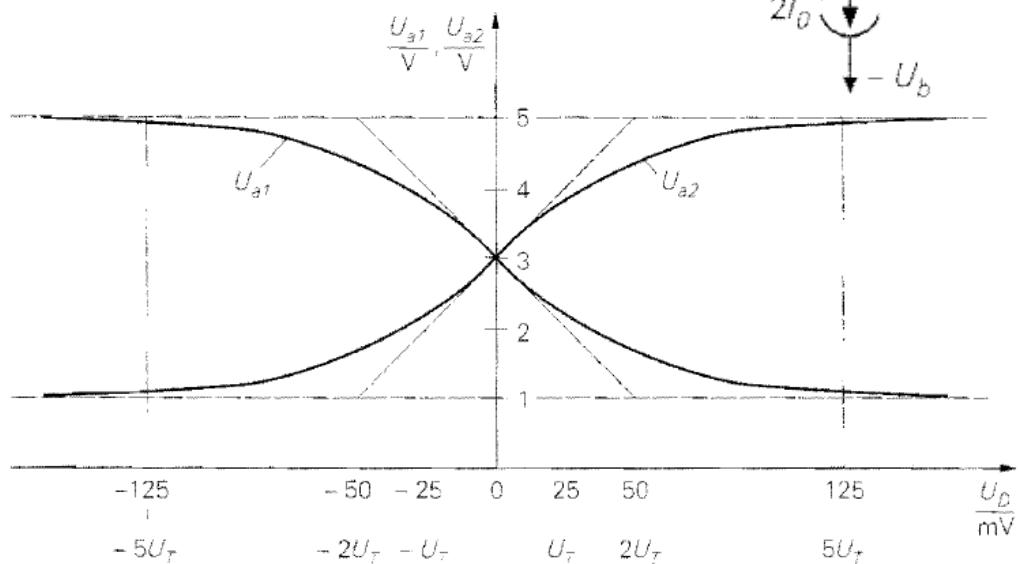
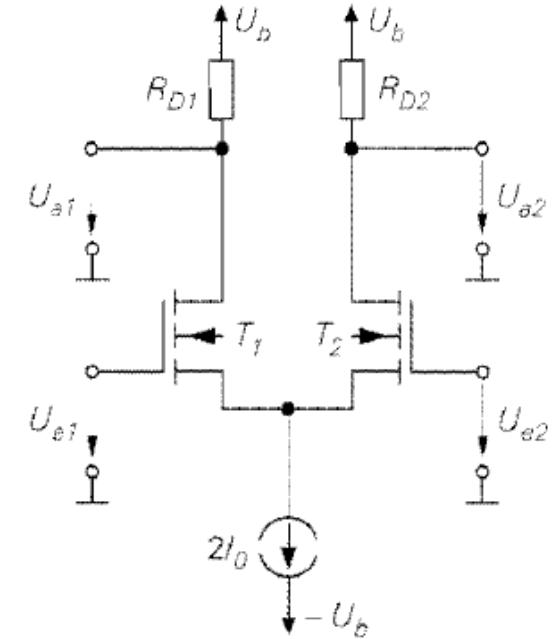
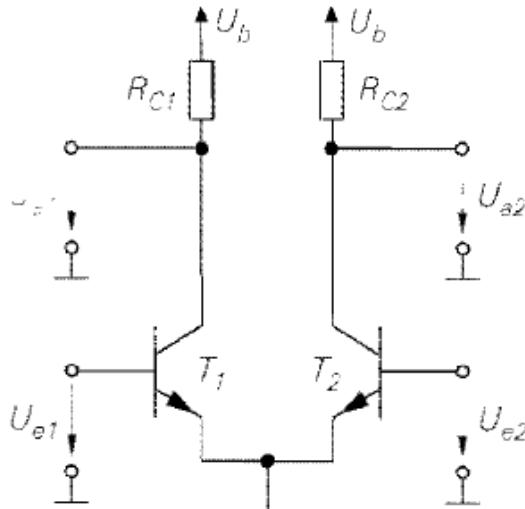
How do we realize a very high, quasi infinite DC gain?

1) Differential amplifier

Large signal analysis:

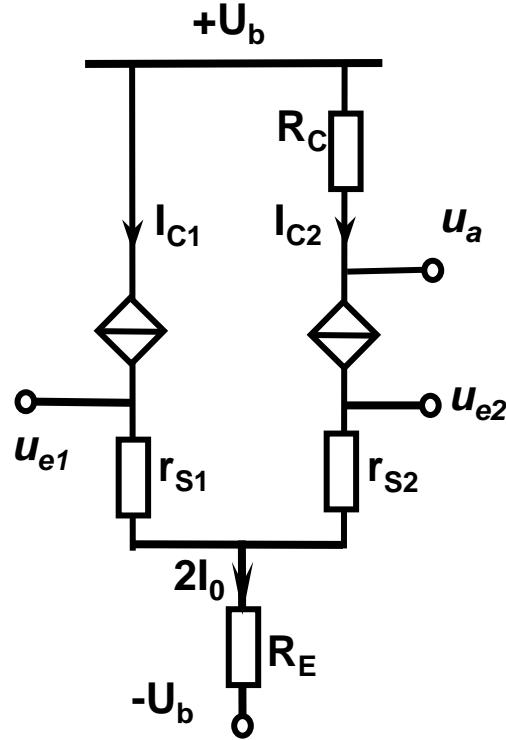
$$I_{C1} = I_0 + \Delta I = I_0 \left(1 + \tanh \frac{U_D}{2U_T}\right)$$

$$I_{C2} = I_0 - \Delta I = I_0 \left(1 - \tanh \frac{U_D}{2U_T}\right)$$



Differential amplifier

Small signal analysis:



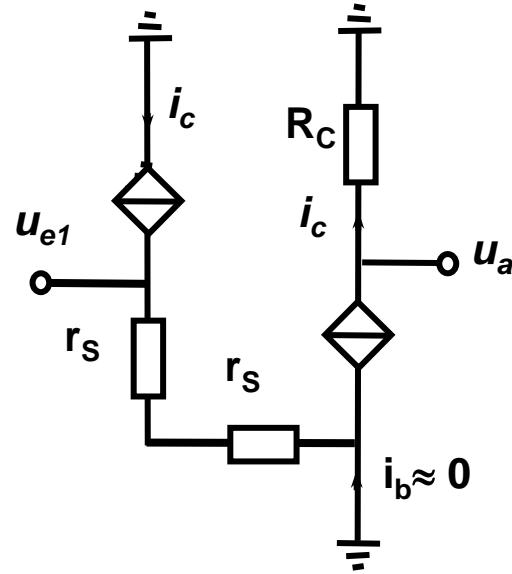
Apply the principle of superposition →

Gain from input u_{e1} :
Suppose $R_E \gg r_s$

$$\frac{u_a}{u_{e1}} = \frac{R_C}{2r_s}$$

In the same way,
gain from input u_{e2} :

$$\frac{u_a}{u_{e2}} = -\frac{R_C}{2r_s}$$



2) Current mirror

T1 connected like a diode.

Current translation factor ($R_1 = R_2 = 0$):

$$k_I = \frac{1}{\left(1 + \frac{1}{\beta}\right)\left(1 + \frac{U_a}{U_A}\right) + \frac{1}{\beta}} \approx \frac{1}{1 + \frac{2}{\beta}} \approx 1$$

Current translation factor ($R_1, R_2 \neq 0$):

$$k_I = \frac{R_1}{R_2 + \frac{R_1 + R_2}{\beta}} \approx \frac{R_1}{R_2}$$

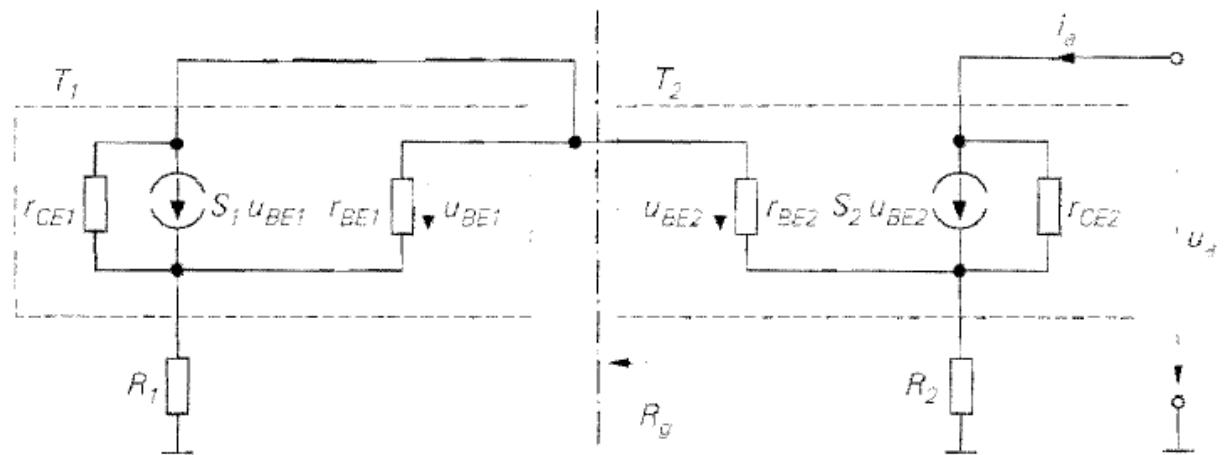
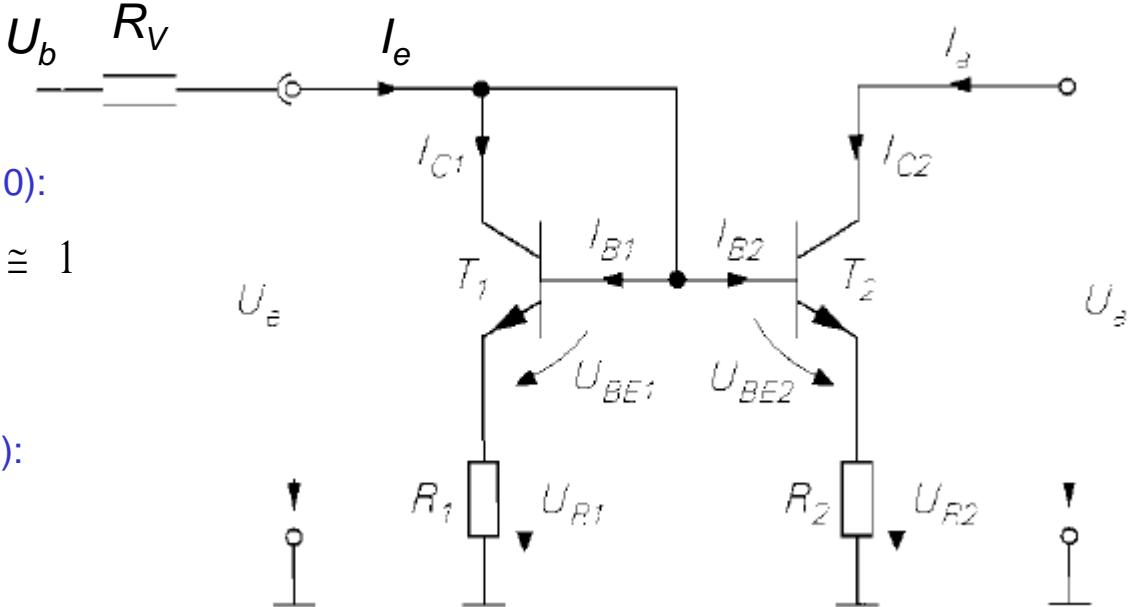
Operation as a current source:

$$I_e = \frac{U_b - U_{BE1}}{R_V + R_1}$$

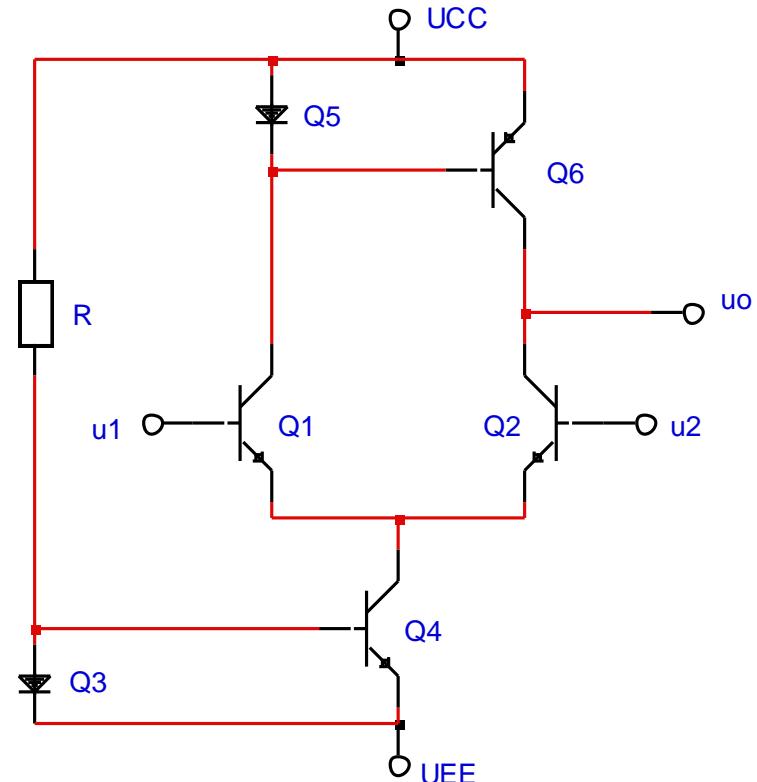
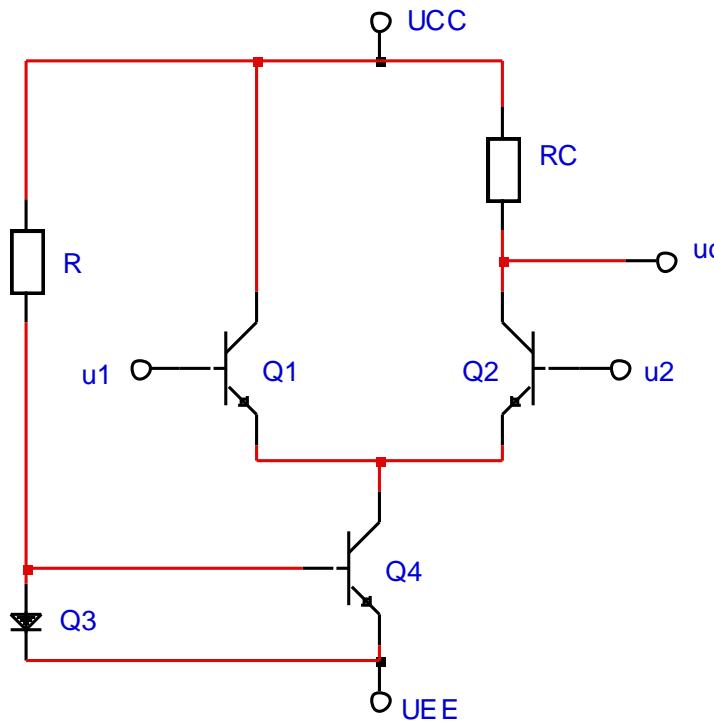
Equivalent schematic
for small signals:

Output resistance:

$$r_a = \left. \frac{u_a}{i_a} \right|_{i_e=0} \approx r_{CE2} \left(1 + \frac{\beta R_2}{R_1 + R_2 + r_{BE2}} \right)$$



3) Mirror used as current source and active load



Q_3 is a transistor identical to Q_4 , where collector and base are connected. The same holds for Q_5 and Q_6 . The mirror Q_3 , Q_4 sets the polarization current $I = (U_{CC}+U_{EE}-U_{BE})/R$. The mirror Q_5 , Q_6 creates an active load with a small signal collector resistance of $Q_2 = R_{Early6}$. The differential gain becomes very high without increasing V_{CC} . Also the output resistance is very high.

4) Cascode circuit

Emitter coupled (T_1) and base coupled (T_2) circuits in series.
Polarization of T_2 by U_0 :

$$U_0 > U_{CE1,sat} + U_{BE2} \approx 0.8...1V$$

The total gain is the product of emitter and base circuit open output gains, and of load adaptation between the two stages :

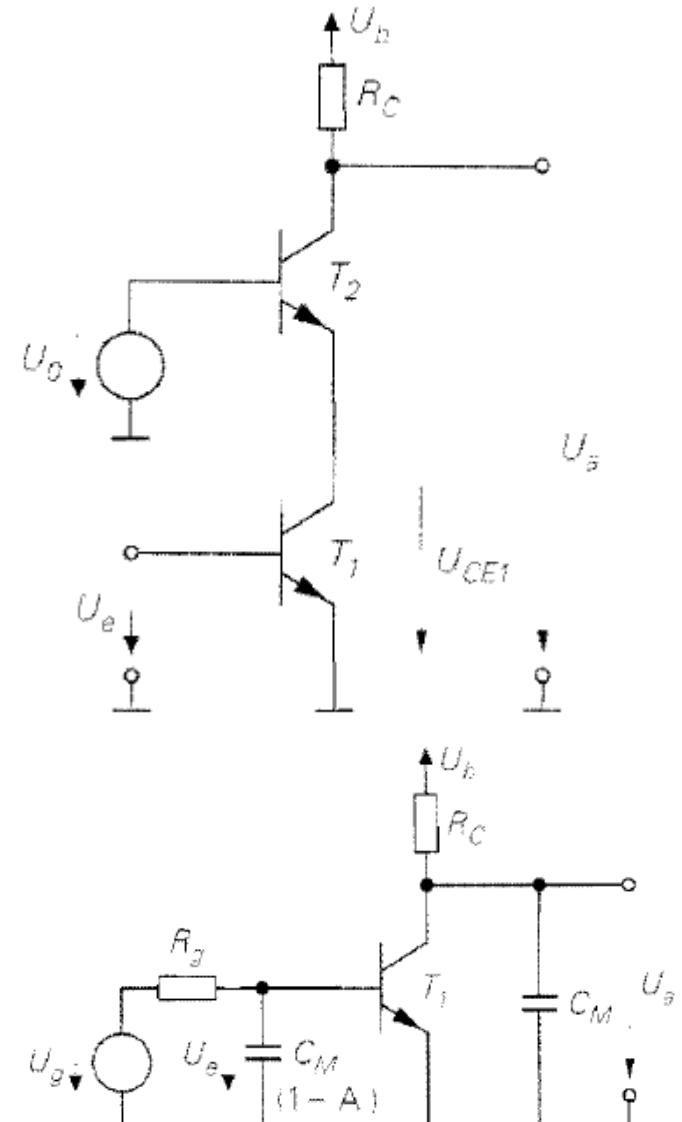
$$A = \frac{u_a}{u_e} = A_E \frac{r_{e,B}}{r_{a,E} + r_{e,B}} A_B = -\frac{r_{CE1}}{r_{S1}} \frac{r_{S2}}{r_{CE1} + r_{S2}} \frac{R_C}{r_{S2}} \approx -\frac{R_C}{r_{S1}}$$

This is the same gain as of the emitter stage alone.
But the emitter stage in the cascode has a gain of -1 only.
Therefore, the equivalent Miller capacitance at its input is only

$$C_e = C_M (1 + |A_{E,op}|) \approx 2 C_M$$

which is much smaller than with the emitter circuit alone.

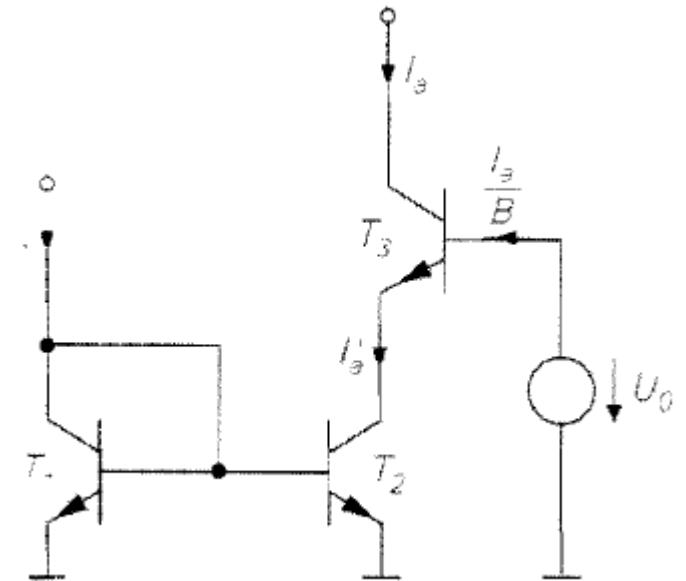
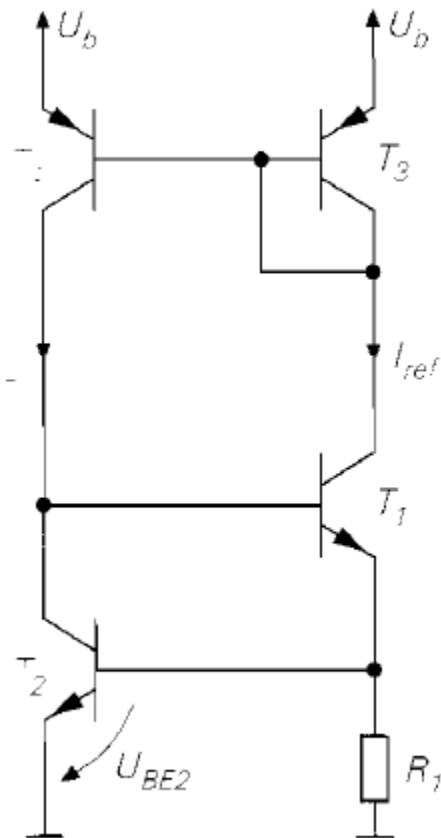
Also, output resistance $\approx \beta \cdot r_{CE}$!



Modified current mirrors

Current mirror with cascode: increased output resistance

$$r_a = \left. \frac{u_a}{i_a} \right|_{i_e=0} \approx \beta r_{CE3}$$

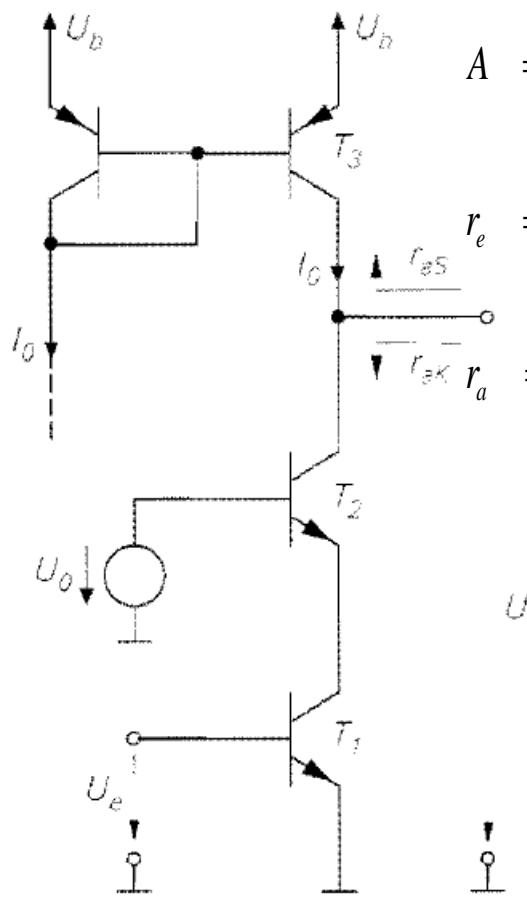


Mirror used as current reference independent of supply voltage:

$$I_{ref} \approx \frac{U_T}{R_1} \ln \left(\frac{I_{ref}}{I_{S2}} + 1 \right) \approx \frac{U_{BE2}}{R_1}$$

Cascode circuit with current source

Cascode with simple current source with high gain and output resistance:



$$A = \frac{u_a}{u_e} \Big|_{i_a=0} = -\frac{r_{aK} \| r_{aS}}{r_{s1}} \cong -\frac{r_{CE\ 3}}{r_{s1}}$$

$$r_e = \frac{u_e}{i_e} = r_{BE\ 1}$$

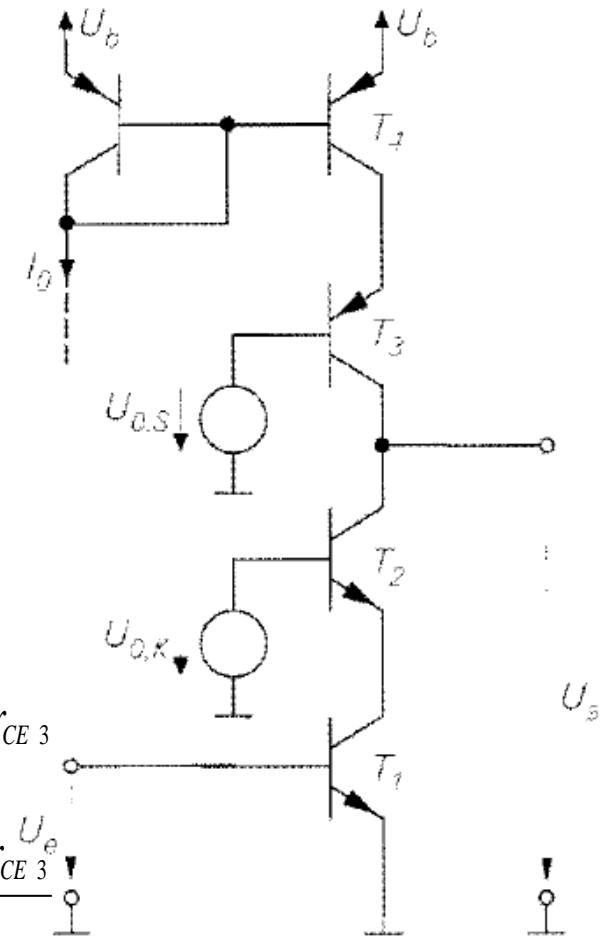
$$r_a = \frac{u_a}{i_a} \Big|_{u_e=0} = r_{aK} \| r_{aS} \cong r_{CE\ 3}$$

with even more output resistance and gain:

$$r_a = \frac{u_a}{i_a} \Big|_{u_e=0} = r_{aK} \| r_{aS} \cong \beta_2 r_{CE\ 2} \| \beta_3 r_{CE\ 3}$$

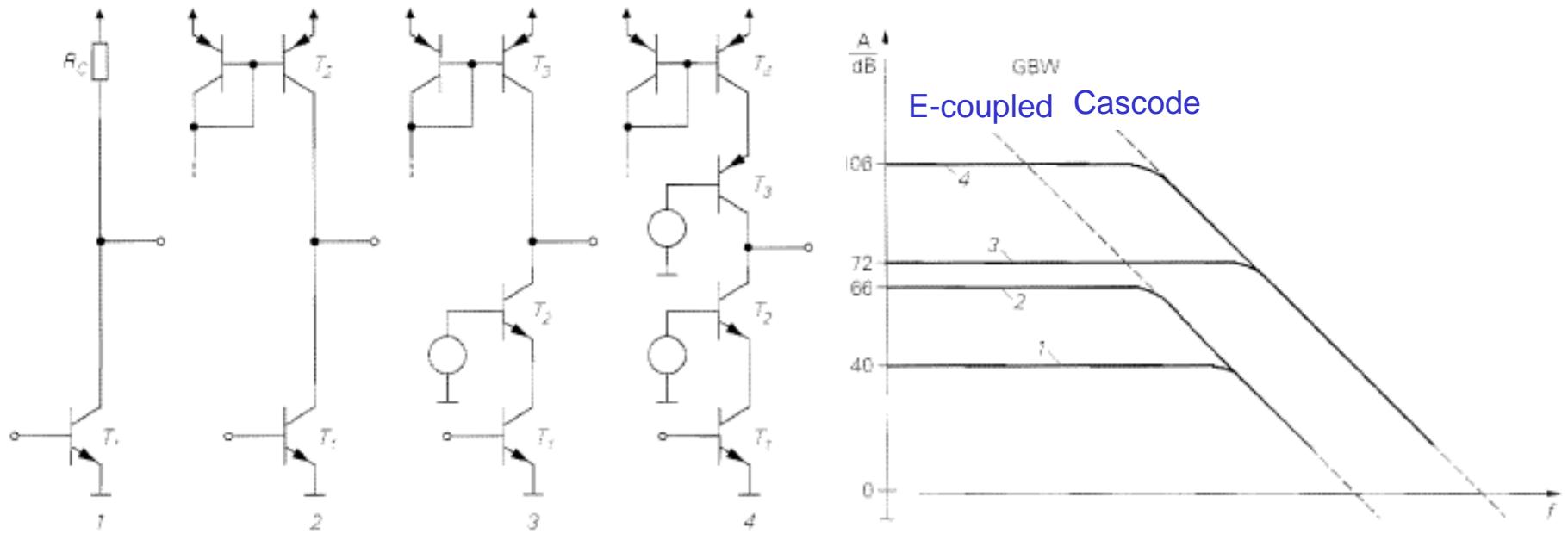
$$A = \frac{u_a}{u_e} \Big|_{i_a=0} = -\frac{r_a}{r_{s1}} \cong -\frac{\beta_2 r_{CE\ 2} \| \beta_3 r_{CE\ 3} U_e}{r_{s1}}$$

Cascode with cascode current source



Gain response comparison

The comparison shows the improvements obtained with active load and cascode circuits, of static gain and bandwidth.

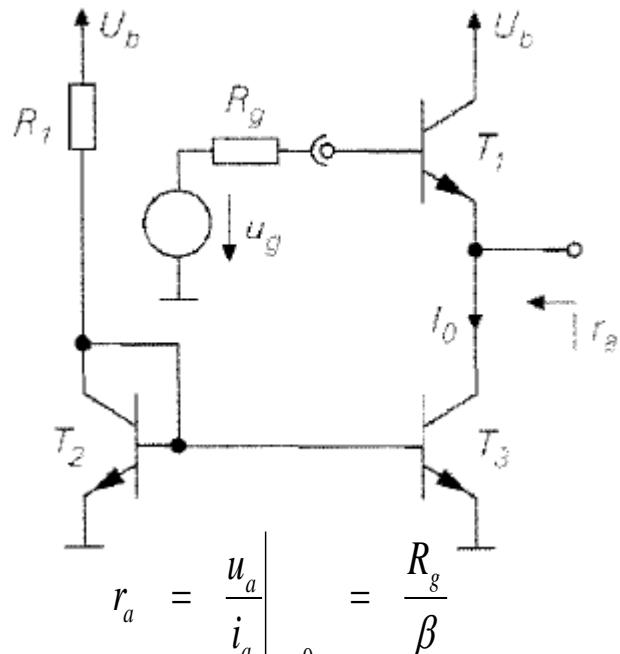


Exercice (homework): Amplifier transfer functions

- For the 4 variants of the preceding slide, analytically estimate the passing band gain and cut-off frequency.
- Use the following parameters (all transistors identical):
 $r'_E = 25\Omega$, $r_{CE} = 100k\Omega$, $\beta = 100$, $R_C = 2.5k\Omega$, $C_M = 30pF$
- Simulate the 4 circuits using LTspice, and verify the gains and cut-off frequencies computed.

5) Impedance conversion

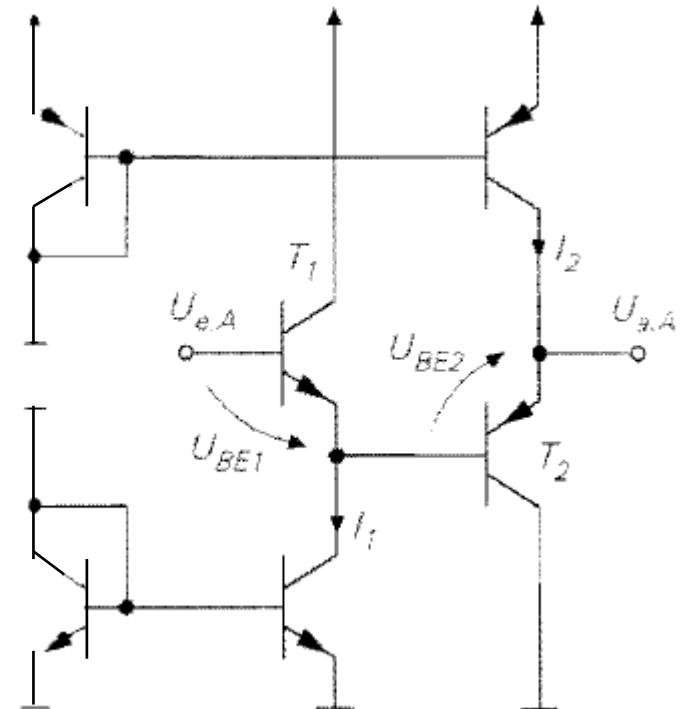
One collector coupled stage:



$$I_0 \approx \frac{10 \beta U_T}{R_g}$$

Choose quiescent currents such that r_s does not influence r_a .
The second stage has about 10x higher I_0 than the first.

Two collector coupled stages:



6) Complementary impedance conversion

One collector coupled stage:

T_1 , T_3 and T_2 , T_4 operate as current mirrors.

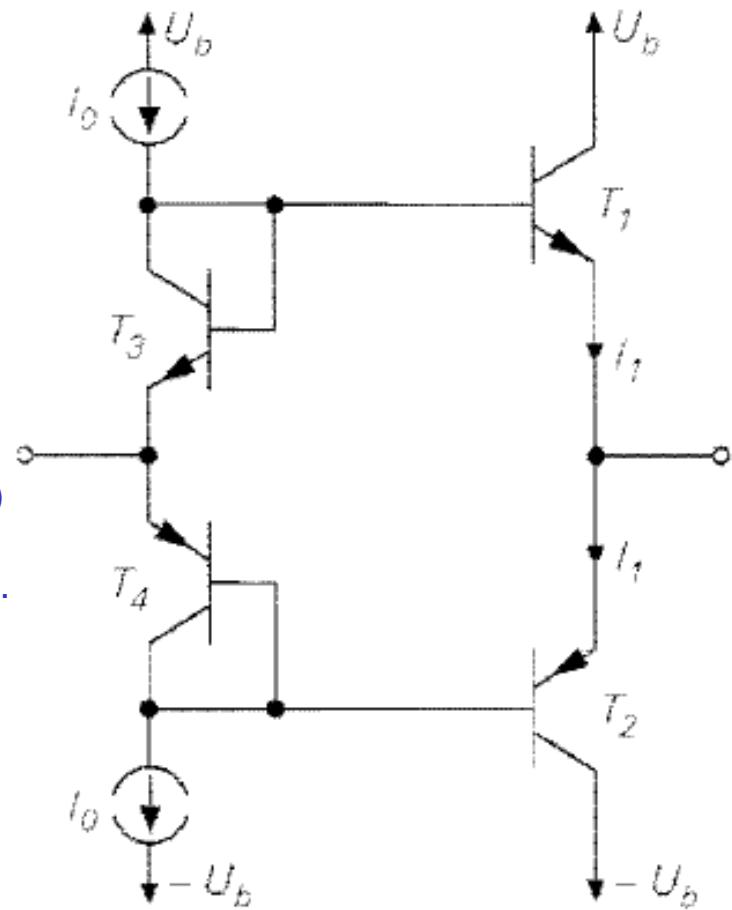
This circuit can be operated with one side in saturation.

Two-stage circuits are also possible.

The circuit is called a push-pull amplifier:

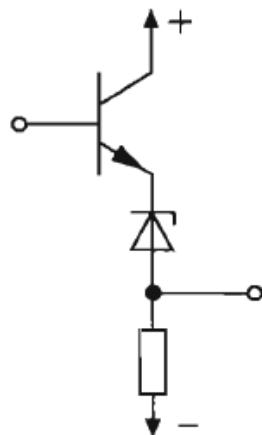
Conduction during 180° of each of both transistors
for transmission of sine signals (B class operating mode)

Additional voltage gain can be added in front of the stage.



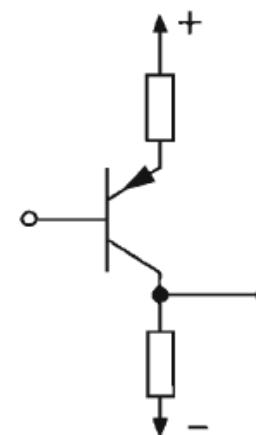
Methods for level-shifting

For DC voltage coupling of amplifier stages, level shifting is needed.



Z-diode

- not precise
- Fixed level difference only



Complementary transistors

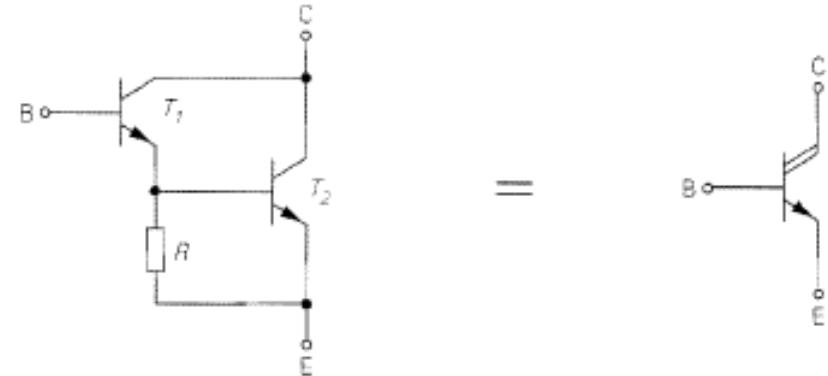
- e.g. pnp transistor after npn amplifier stage
- adaptive: preferred method
- current mirror output stage may be used

7) Darlington transistor

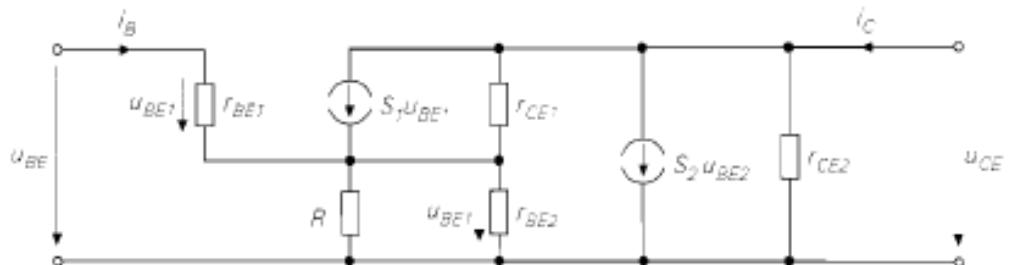
Resistor needed for improved switching behaviour.
Strong increase of current gain and input resistance,
as compared to single transistor:

$$\beta \approx \beta_1 \beta_2$$

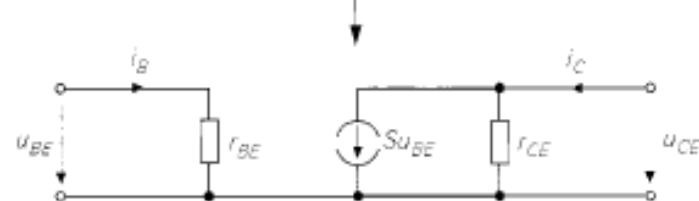
$$r_{BE} \approx r_{BE1} + \beta_1 (r_{BE2} \| R)$$



Small signal equivalent circuits, detailed:



reduced:

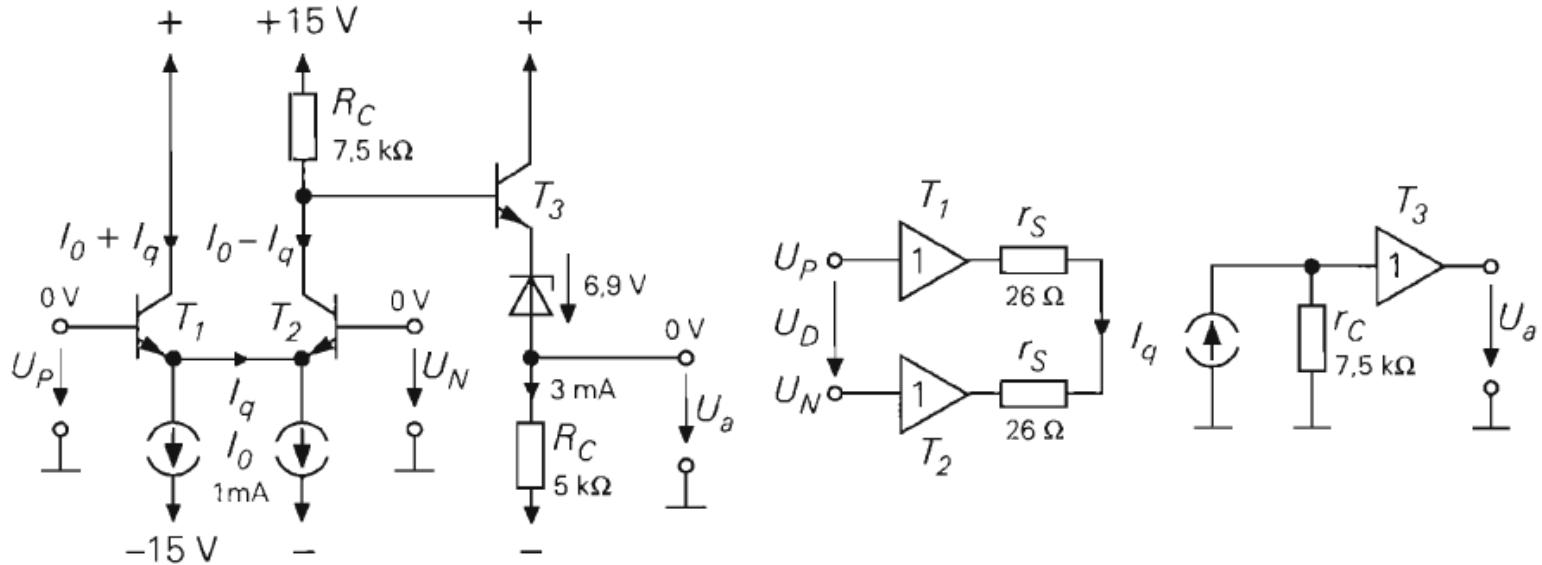


Exercice (homework): MOS-FET circuits

Redraw a cascode amplifier and a complementary impedance conversion stage schematic, each with MOS-FET instead of bipolar transistors.

Rewrite the gain and input capacitance equations for the cascode circuit with MOS-FETs.

Simple operational amplifier circuit



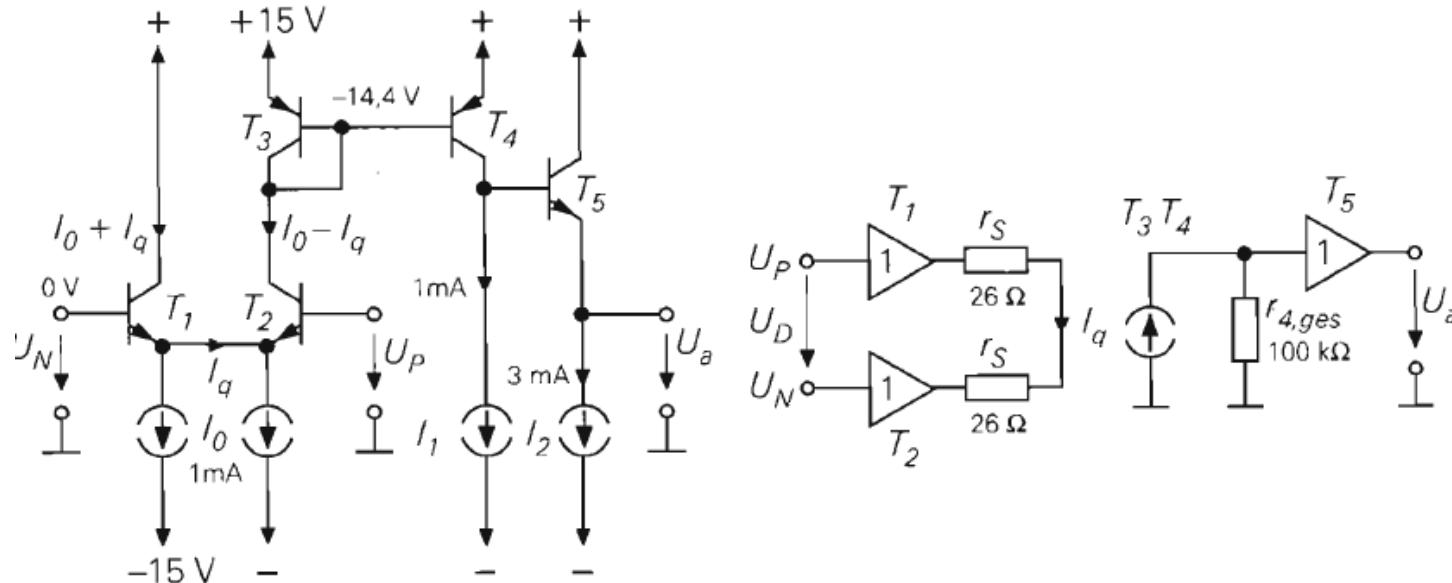
Example design values, quiescent currents and voltages, deviation I_q :

$$I_q = \frac{U_D}{2r_S} = \frac{1}{2} \frac{I_C}{U_T} U_D = \frac{1}{2} \frac{1mA}{26mV} U_D = \frac{19mA}{V} U_D$$

$$U_a = I_q R_C = \frac{1}{2} \frac{I_C R_C}{U_T} U_D = \frac{U_{RC}}{2U_T} U_D = \frac{7.5V}{2 \cdot 26mV} U_D = 144 \cdot U_D$$

Input common mode range $-13.4V < U_P = U_N = U_{gl} < +7.5V$ (minimum headroom of 1V over I_0 source).
Output range $-7.5V < U_a < +7.5V$ at $U_{GI} = 0$, otherwise less.

Use of current mirror for level-shifting



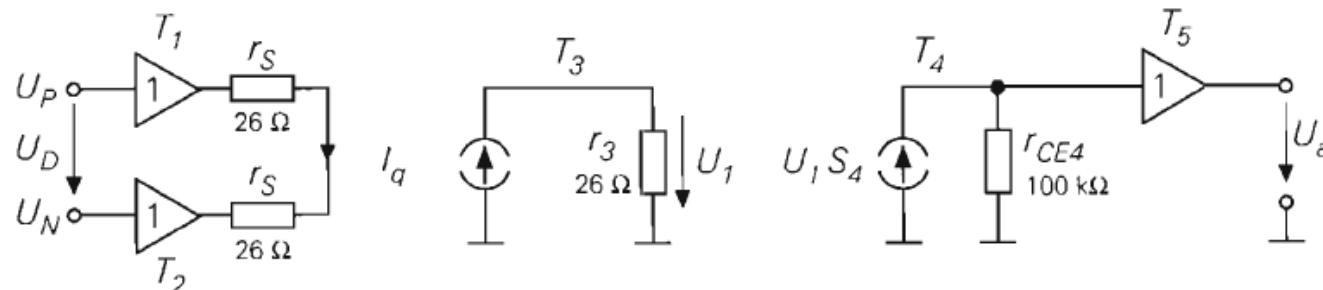
Input common mode range $-13.4\text{ V} < U_P = U_N = U_{gl} < +14.4\text{ V}$ (minimum headroom of 1 V over I_0 source).

Output range $-14\text{ V} < U_a < +13.8\text{ V}$.

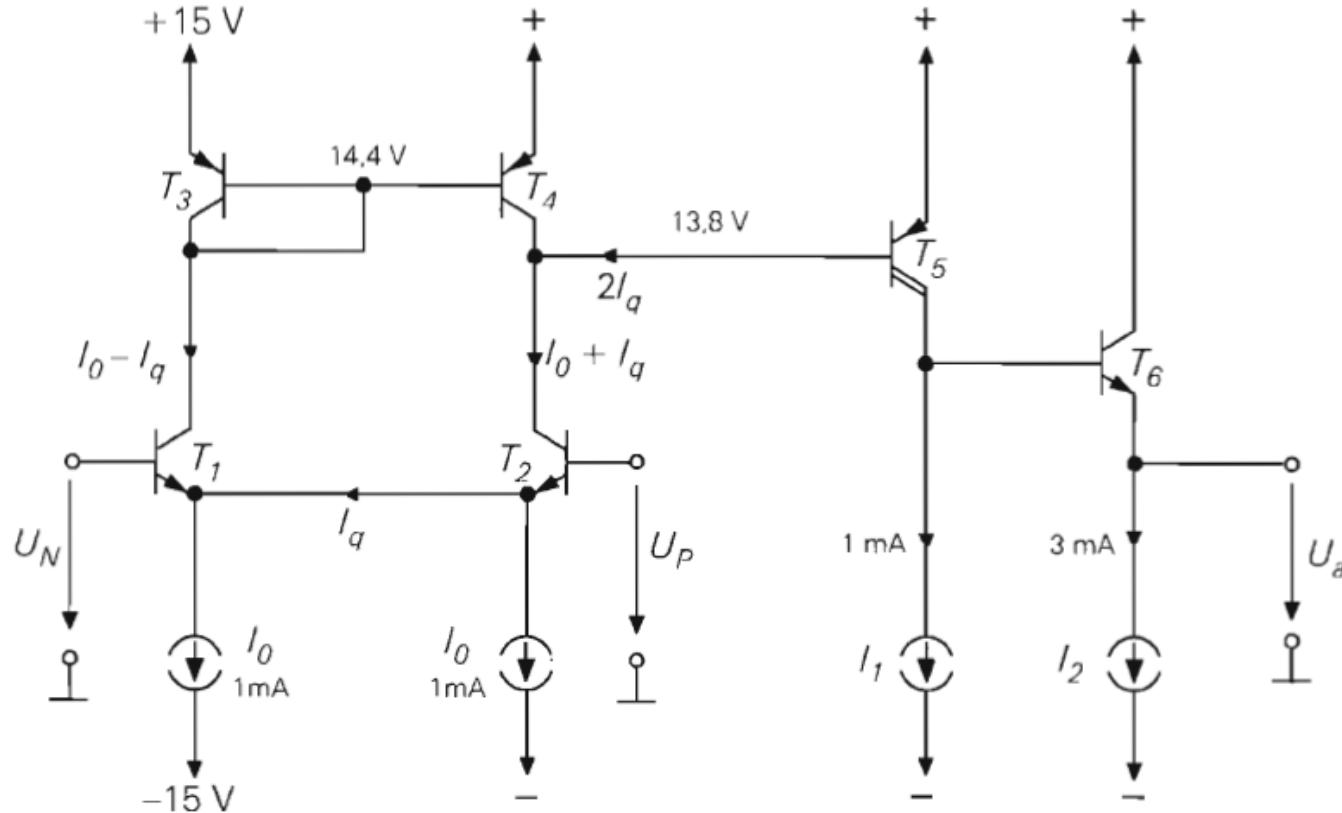
Difference gain:

$$A_D = \frac{r_{CE4}}{2r_S} = \frac{I_0}{2U_T} \frac{U_A}{I_0} = \frac{100\text{ V}}{2 \cdot 26\text{ mV}} = 1923$$

Model with 2 amplifying stages:



Operational amplifier with 2 amplifier stages



Example design values for quiescent currents and voltages, deviation I_q .
Advantage of this universal amplifier: two cascaded stages realize higher gain.
 T_5 must be a Darlington transistor for high input resistance.

741 class operational amplifier

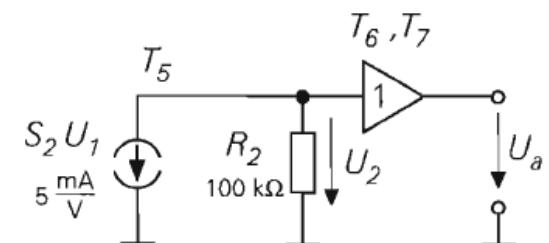
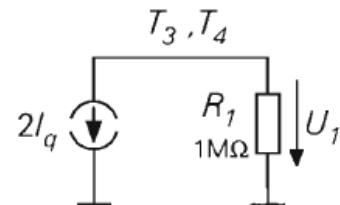
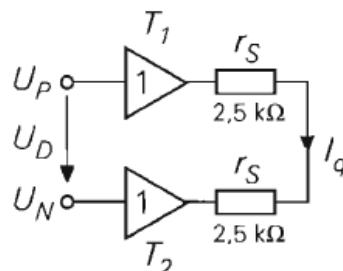
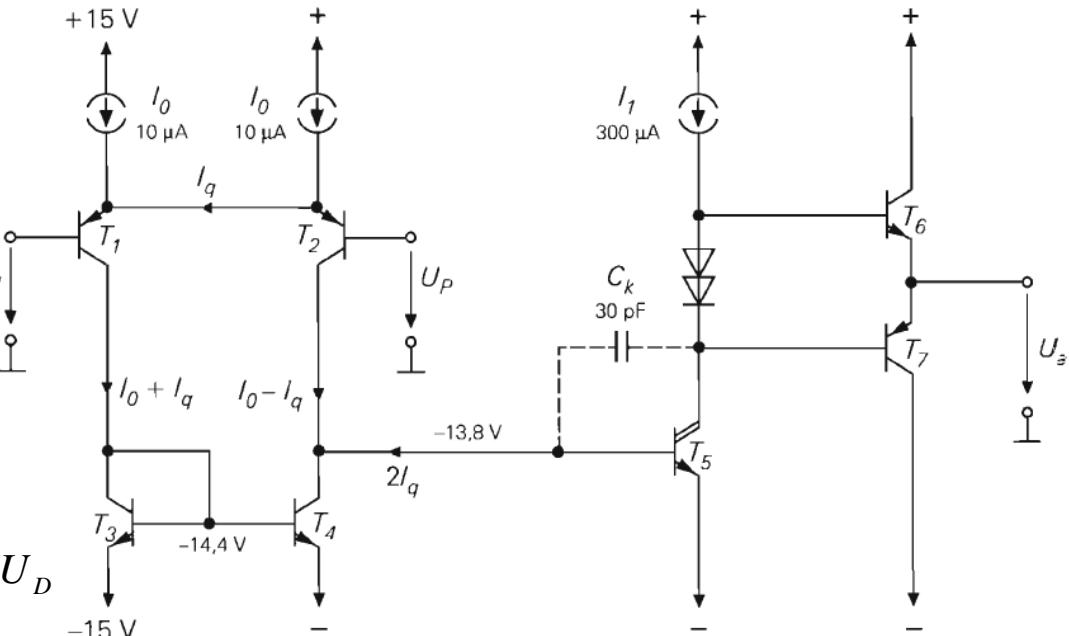
Complementary variant of circuit on preceding slide.
Reduced quiescent currents in differential pair.
Complementary emitter follower at output, to reduce quiescent current.

Model of the operational amplifier and gain equations:

$$U_1 = -2I_q R_1 = -2R_1 \frac{U_D}{2r_s} = -\frac{1M\Omega}{2.5k\Omega} U_D = -400 \cdot U_D$$

$$U_2 = -S_2 U_1 R_2 = -5 \frac{mA}{V} \cdot 100k\Omega \cdot U_1 = -500 \cdot U_1$$

$$A_D = (-400) \cdot (-500) = 2 \cdot 10^5$$

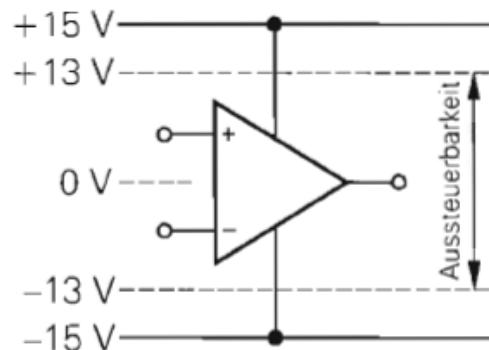


Exercice: Determination of I/O voltage ranges

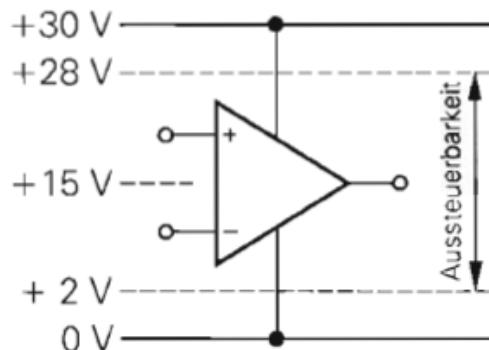
- Look at the schematic of the OP741 amplifier (p.26) and determine the highest possible positive and negative input voltages.
- Do the same for the output.
- What will happen if an input pin is driven beyond the power supply voltages?

Supply voltages

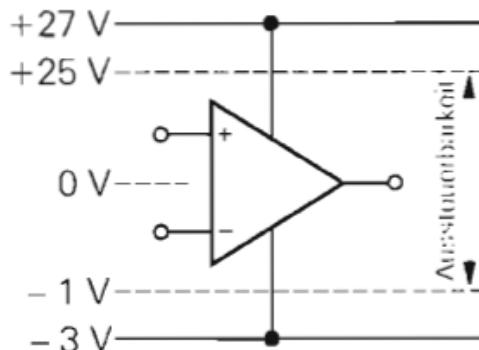
How do we reduce supply voltage and go for single supply operation?



a Normalbetrieb



b Betrieb aus einer einzigen Betriebsspannung



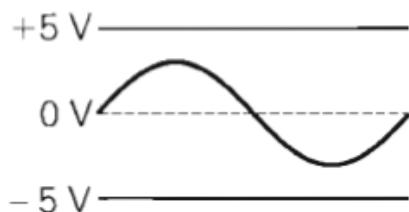
c Betrieb für positive Spannungen

Influence on common and differential mode ranges

Output ranges with low supply voltages

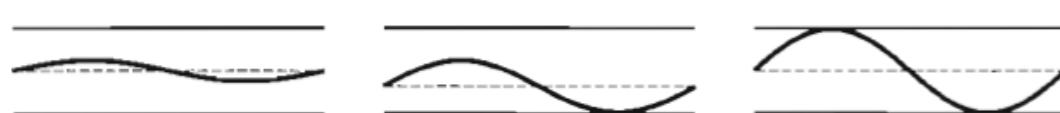
Different solutions proposed in commercially available devices

± 5 V Betriebsspannung

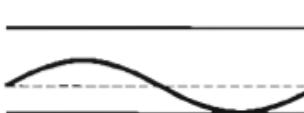


a Normalbetrieb

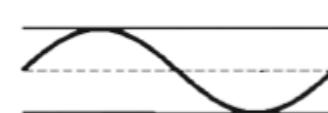
nur eine einzige positive Betriebsspannung von $+5$ V



b Normaler OPV



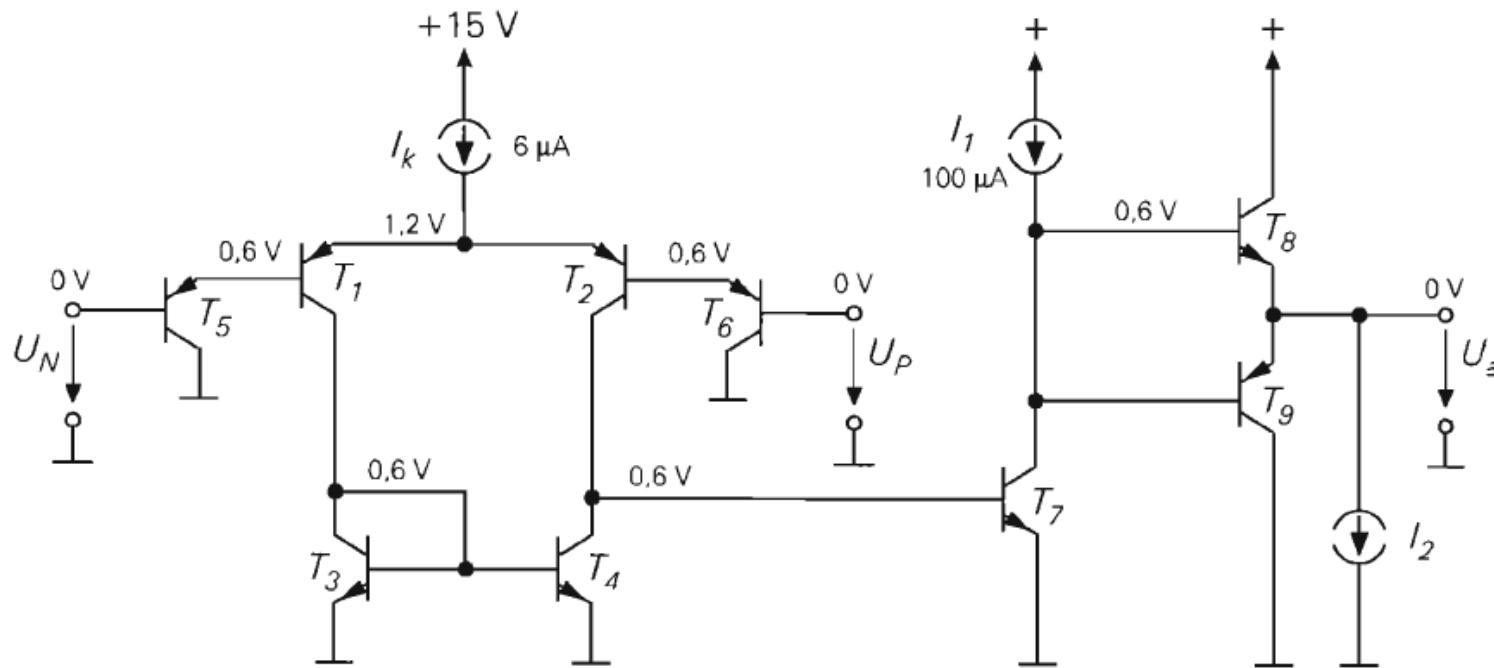
c Single-Supply OPV



d Rail-to-Rail OPV

Keep in mind that rail-to-rail operation might be possible either with inputs, or with the output, or with both.

Single supply amplifier LM324



Potentials for 0V output = negative supply voltage

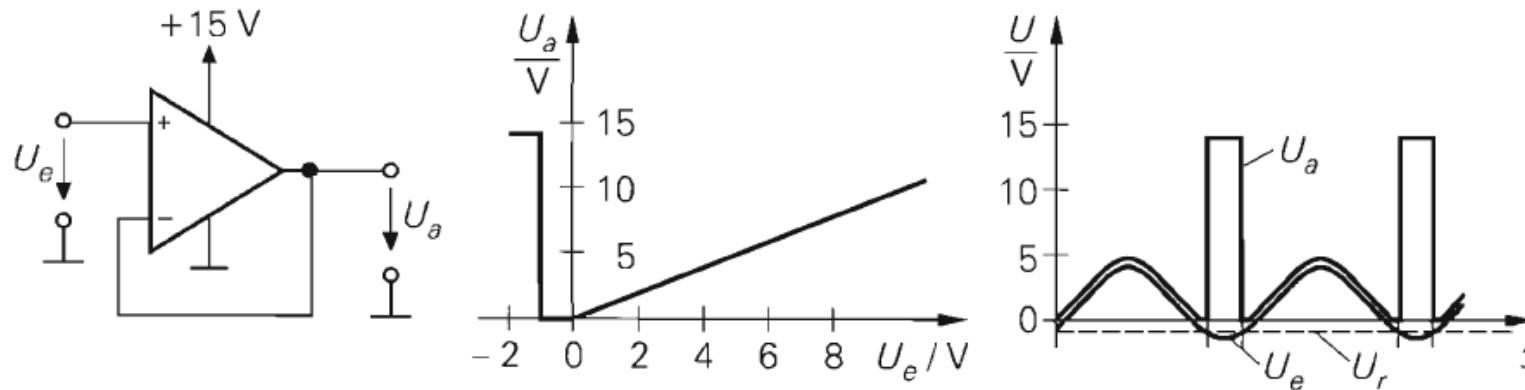
Additional emitter followers T_5 , T_6 to shift the emitter potential of the difference amplifier 0.6V upwards, allowing 0V input.

T_7 is not a Darlington circuit, to limit the base potential to 0.6V, avoiding saturation of T_2 at 0V input.

Additional current source I_2 accepting current when T_9 already blocked.

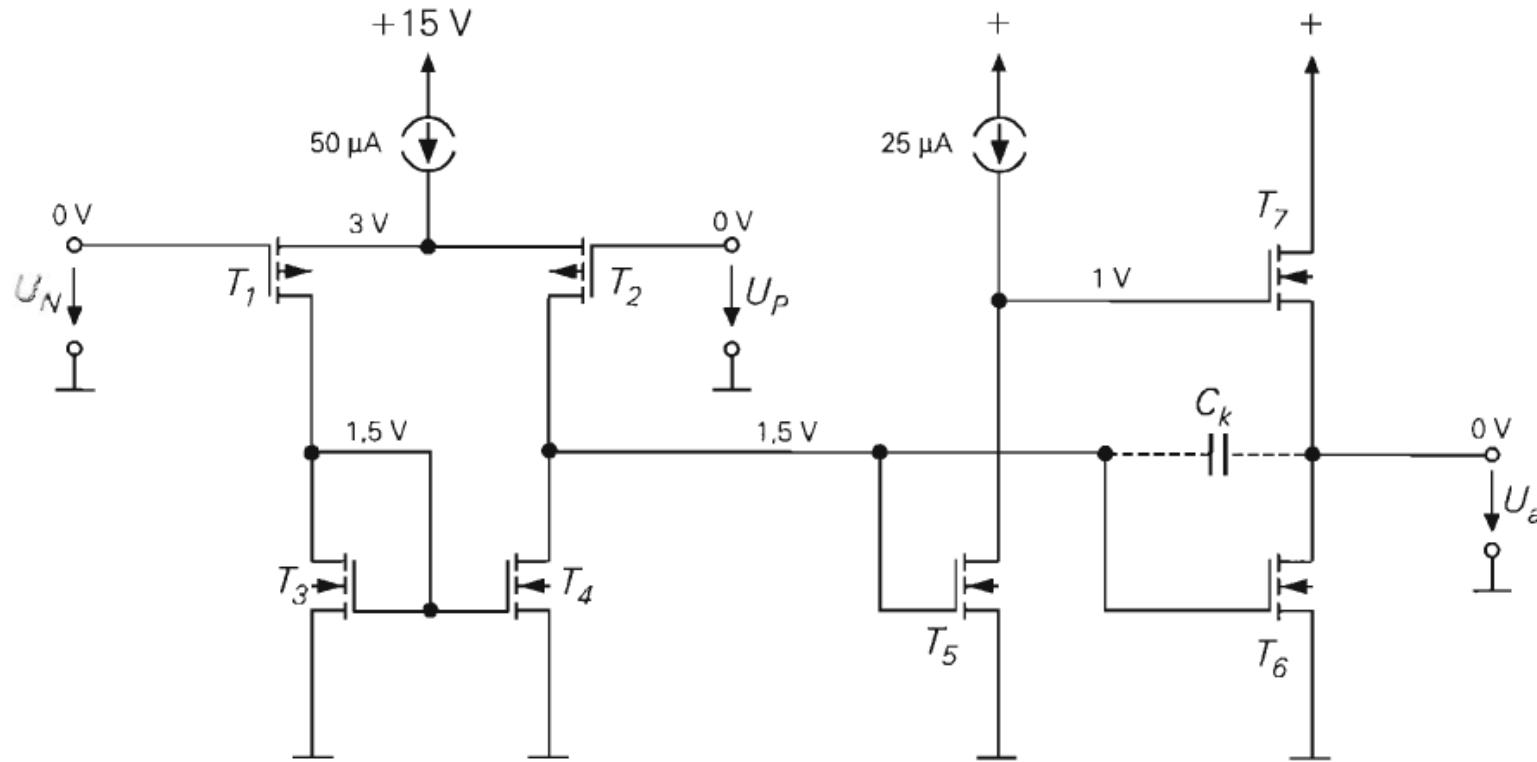
Phase reversal

T_2 saturates when input voltage below -0.4V. Its junction BC conducts, transistor in inverse mode. Emitter of T_6 then linked to T_7 and inverting amplification of T_2 becomes non-inverting: phase reversal.



Effect on transfer behaviour

Single supply CMOS operational amplifier



TLC series

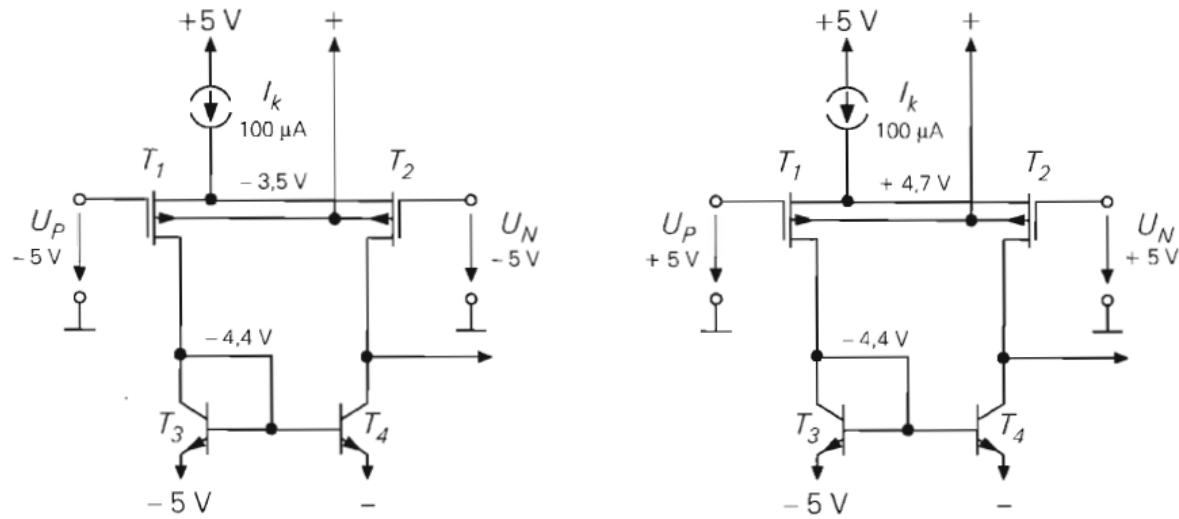
Not affected by phase reversal, since gate electrodes are insulated in CMOS and cannot conduct current.

T₆ is not a complementary source follower, but a common source circuit like T₅.

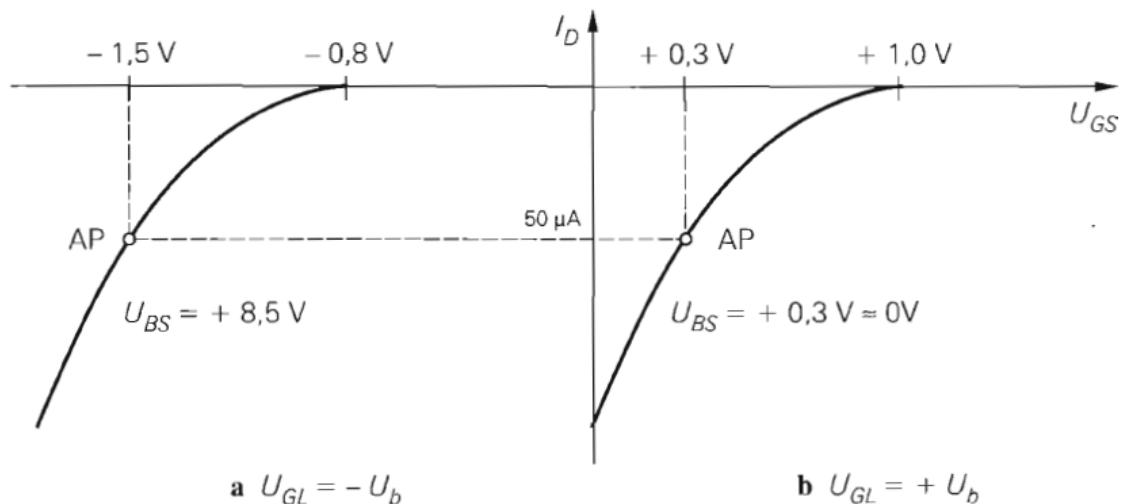
T₆ can pull down the output to zero, without additional current source I₂.

Rail-to-rail CMOS differential amplifier

Special MOS-FETs that are self-blocking at negative input maximum, and self-conducting at positive input maximum.

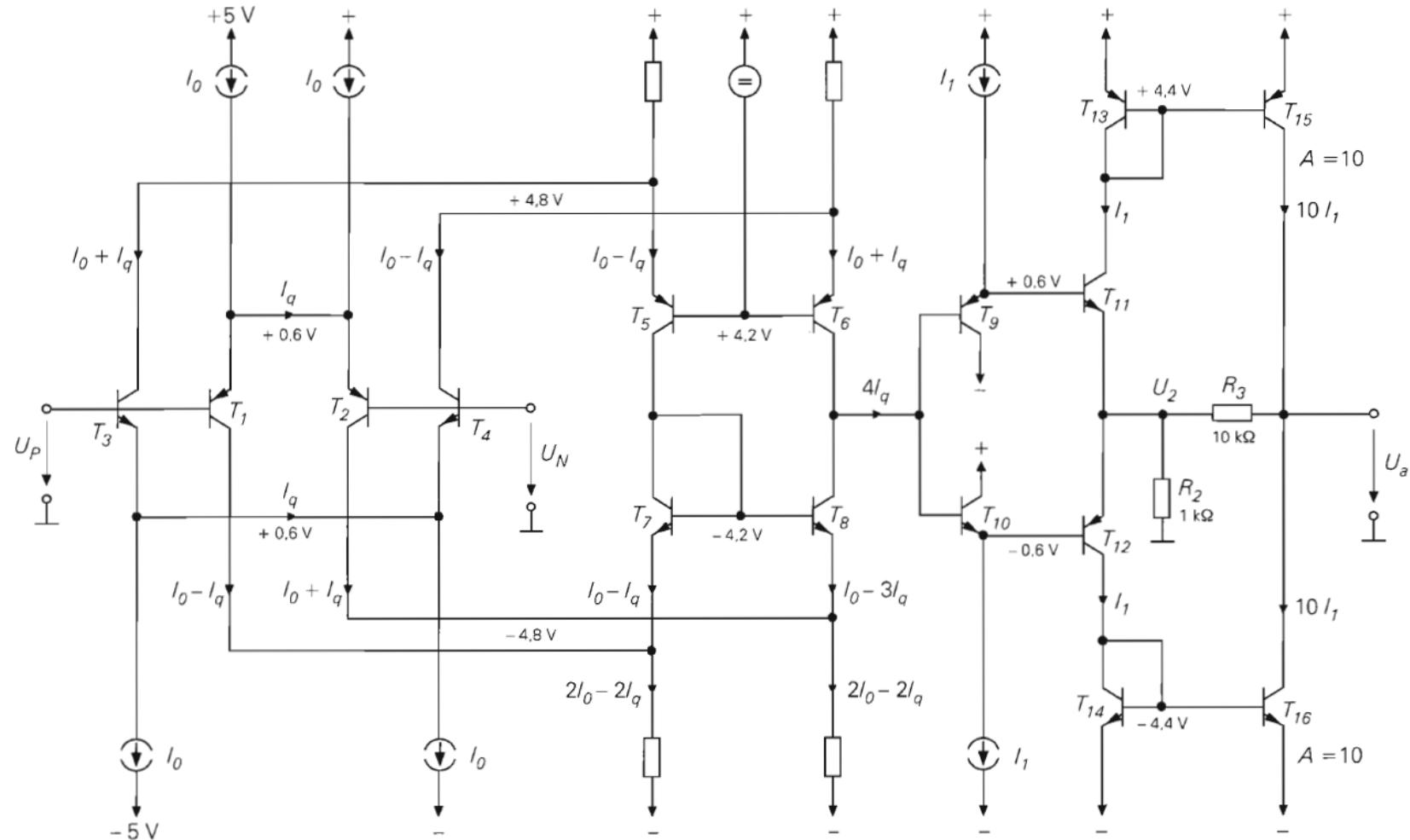


Operating points for two extreme cases:



Low power operation

Rail-to-rail I/O operational amplifier



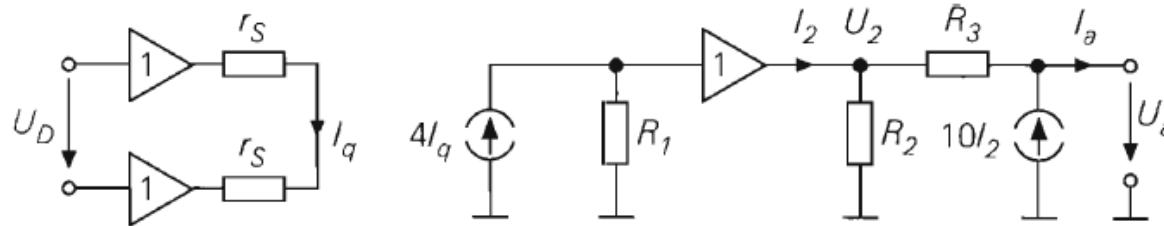
E.g. $I_0 = 10\mu\text{A}$, $I_1 = 100\mu\text{A}$

Low power operation

Model of rail-to-rail I/O operational amplifier

Model for output stage analysis:

R_1 is the impedance of the summation output delivering $4I_q$.



$$I_2 - \frac{U_2}{R_2} + \frac{U_a - U_2}{R_3} = 0$$

$$\frac{U_2 - U_a}{R_3} + 10I_2 - I_a = 0$$

$$I_a = 0 \Rightarrow U_a = \frac{11R_2 + 10R_3}{11R_2} U_2 \cong 10U_2, \text{ with } R_3 = 10R_2$$

$$U_2 = 0 \Rightarrow r_a = -\frac{U_a}{I_a} = \frac{1}{11} R_3$$

Exercice: Single supply circuits

- Propose the standard operational amplifier circuits (inverting, non-inverting, differential amplifier) for single supply operation.

Books

Tietze, Schenk: *Halbleiter-Schaltungstechnik*, Springer 2008 (13th ed.), ISBN 3-540-64192-0

This book was used as a basis for the present presentation, the illustrations are taken from it.

Millman: *Microelectronics: Digital and Analog Circuits and Systems*, McGraw-Hill 1984, ISBN 0-07-066410-2

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Jung: *OpAmp Application Handbook*, Analog Devices 2005, ISBN 0-750-67844-5

Mancini: *OpAmps for everyone*, Texas Instruments 2002

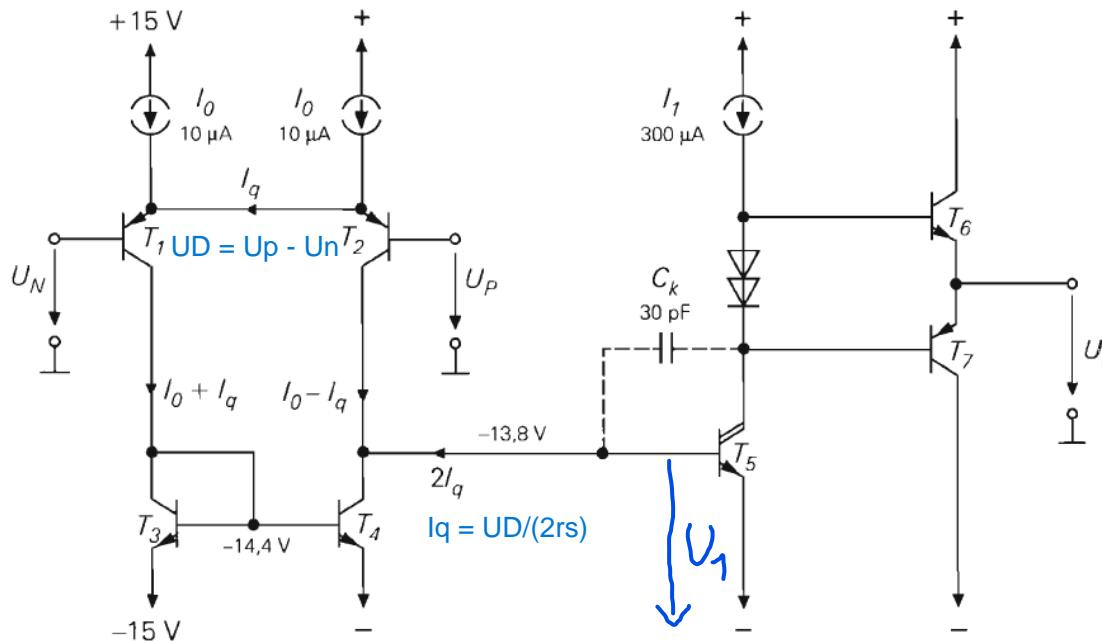
Contents

- Generalized operational amplifier theory: VC, CV and CC structures
- Exercices
- References

Exercice: Analysis of opamp structure

Admit that the sources I_0 and I_1 need a minimum overhead voltage of 1.0V to operate. $U_{BE} = 0.6V$, $U_T = 25mV$ for all transistors and diodes.

Total resistance connected to node of the basis of T_5 $R_1 = 2M\Omega$, of the collector of T_5 $R_2 = 100k\Omega$. Base currents are negligible. Transconductance of T_5 : $1/r_{S5} = 5mA/V$.



What is the admissible input voltage range of U_N, U_P ? What is the possible output voltage range of U_a ?

Determine the gain $A_0 = U_a/(U_P - U_N)$ of this opamp.

Admit that the capacitor C_k determines the dynamic behaviour of the circuit. What is the cut-off frequency of the open-loop transfer function? What is the maximum slew rate?

If the opamp is used as a linear inverting stage, which gain can be realised at 10kHz?

Simple transconductance amplifier

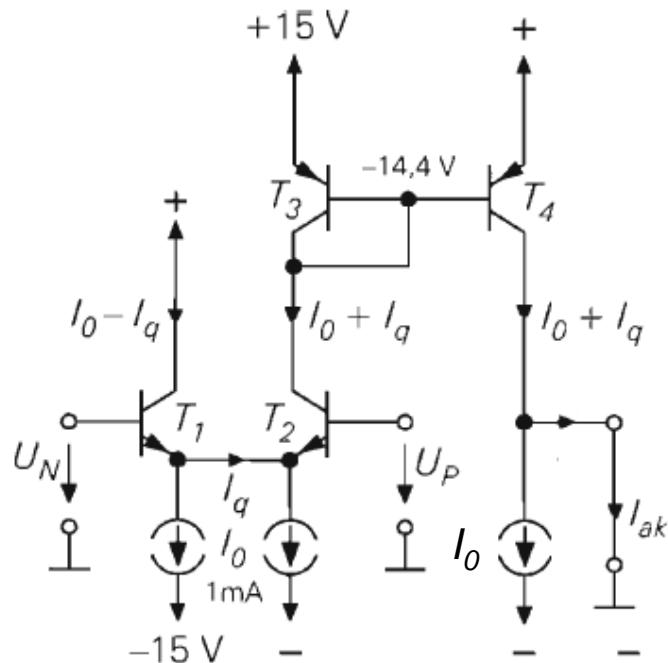
Basic VV operational amplifier structure, where the output stage was suppressed.

Transmission gain = transconductance:

$$S_D = \frac{I_q}{U_D} = \frac{1}{2r_s} = \frac{I_0}{2U_T}$$

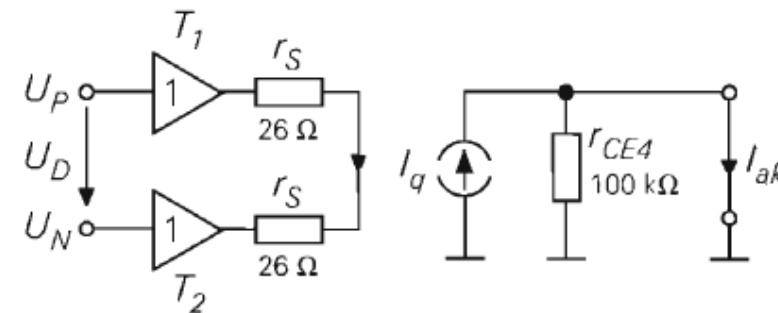
The transconductance can be set by inserting an additional emitter resistance R_E , between the two emitters of the differential stage.

Output resistance:



$$r_a = \left. \frac{u_a}{i_a} \right|_{u_e=0} = r_{CE4}$$

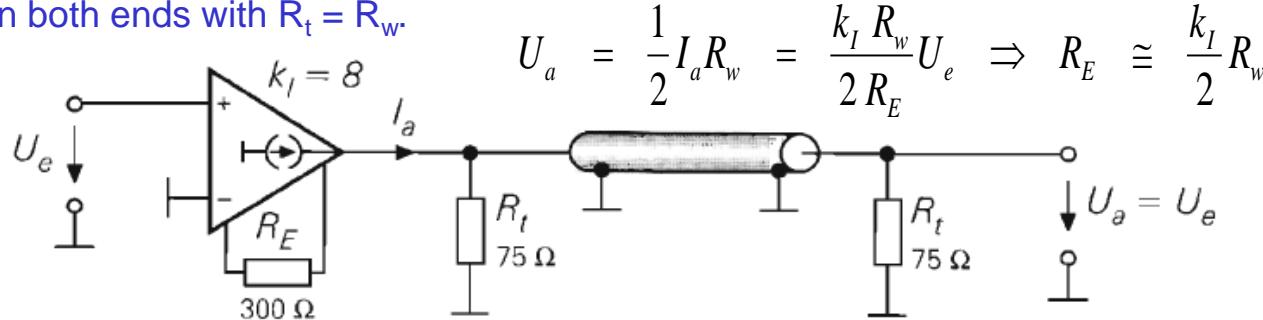
Because of the high output resistance, output voltage strongly dependant on load.



VC operational amplifier

Coax line driver

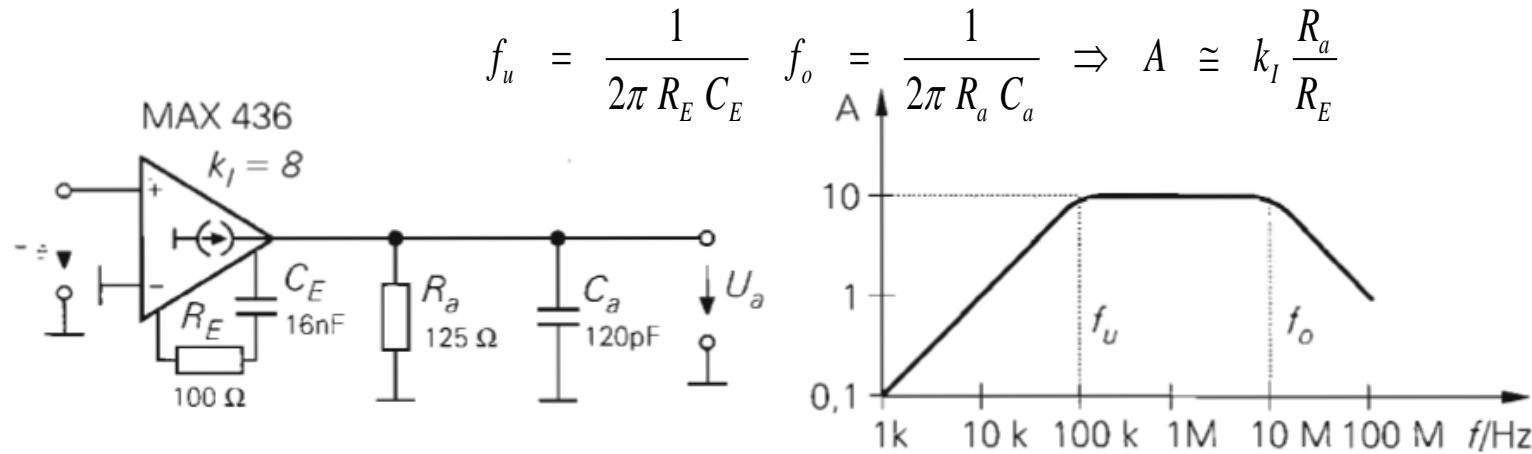
Output resistance supposed to be large as compared to wave impedance R_w . To avoid reflections, line terminated on both ends with $R_t = R_w$.



The particular choice of R_E gives $U_a = U_e$ which is an advantage for low voltage supply.

Passive bandpass

Emitter impedance is here complex, series RC yields high pass. Parallel RC output termination yields low-pass.

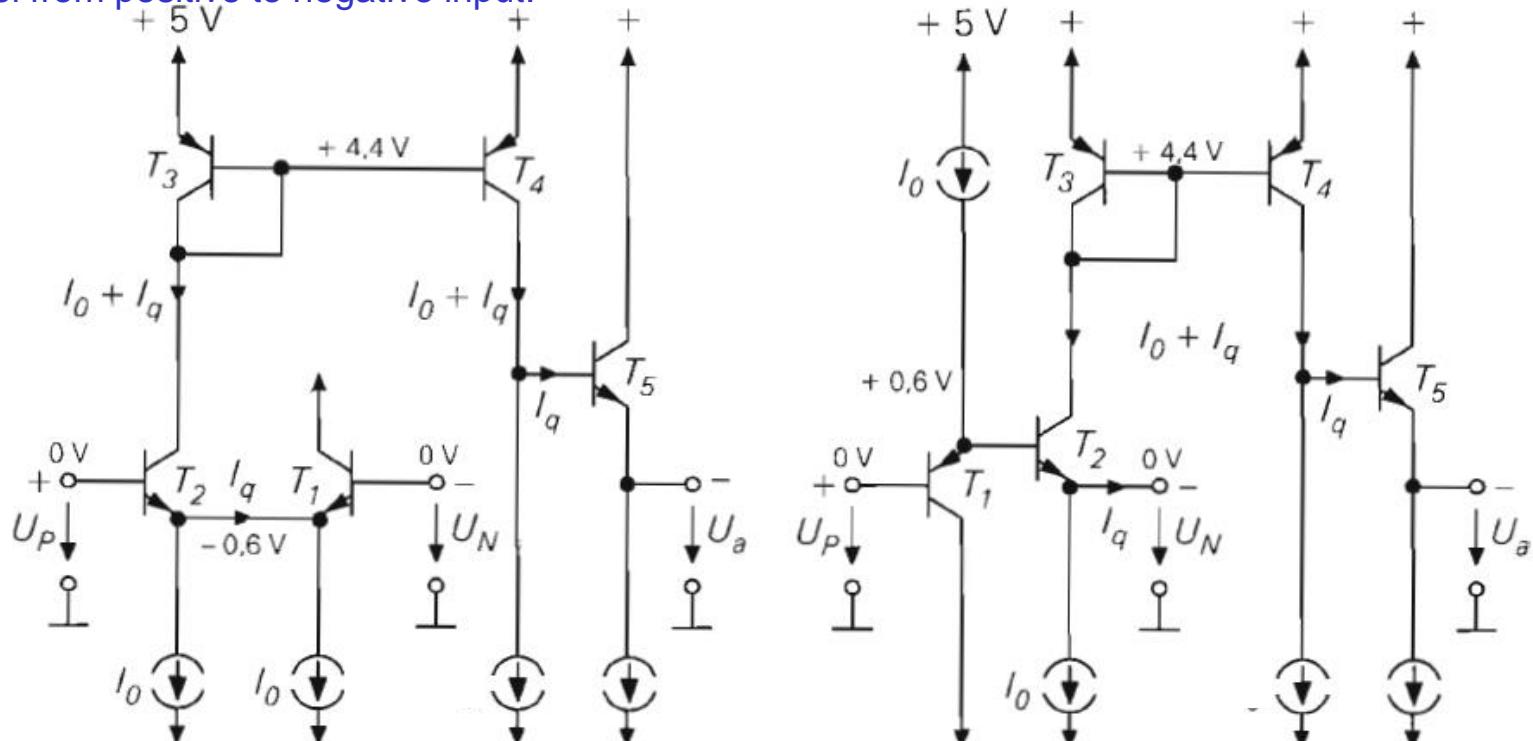


Transimpedance operational amplifier

Standard VV amplifier on left hand figure, CV amplifier for comparison on right hand figure:

I_q is not the total base current of T_5 , but the signal part.

Elimination of T_1 of VV circuit leads to low impedance negative input. T_1 of CV circuit compensates U_{BE} threshold of T_2 : $U_{D0} = 0$ by nature of the circuit, with output resistance r_s at negative input \Rightarrow additional arrow symbol from positive to negative input.

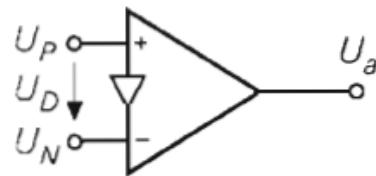


Transimpedance $Z = r_{CE4}$:
(internal resistance of high impedance node)

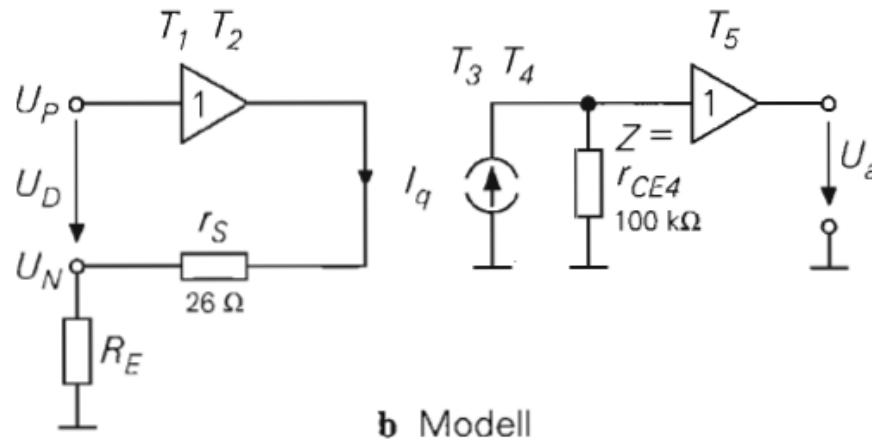
$$U_a = I_q Z = \frac{U_D}{r_s} Z \Rightarrow A_D = \frac{U_a}{U_D} = \frac{Z}{r_s} = \frac{U_A}{U_T}$$

Model of transimpedance operational amplifier

Input resistance R_E of N input to ground (Early resistance of I_0 current source).



a Schaltsymbol

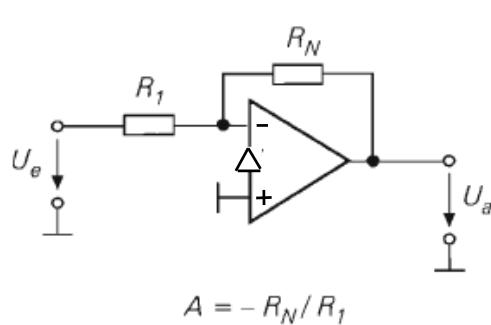


b Modell

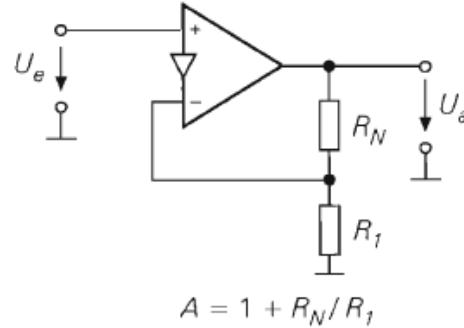
$$A_B = \frac{U_a}{U_p} = \frac{Z}{R_E + r_S}$$

Typical applications

Only resistive feedback is stable, capacitive feedback (e.g. integrator) is not.



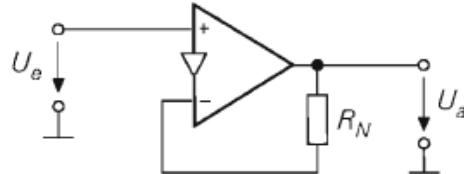
Inverting amplifier



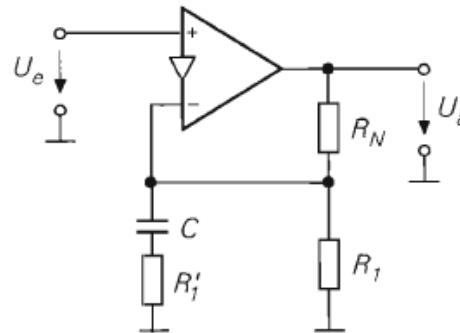
Non-inverting amplifier

R_N determines loop gain, and is therefore to be selected as a function of amplifier type.

For high gain, non-inverting circuit has higher input resistance.



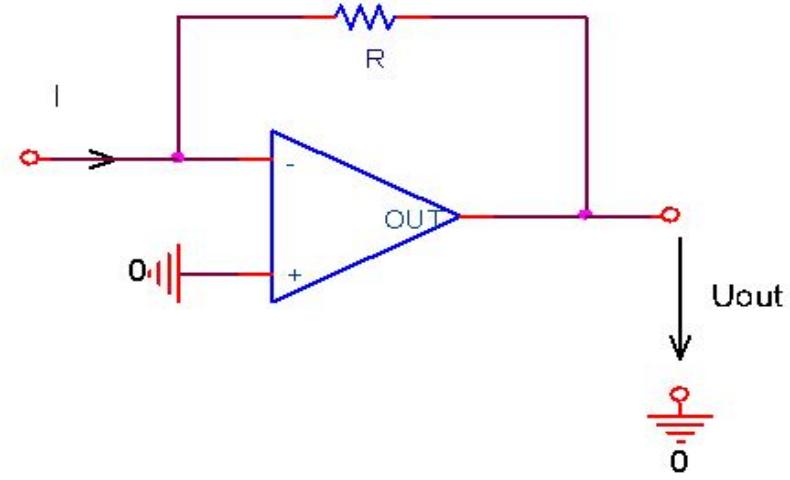
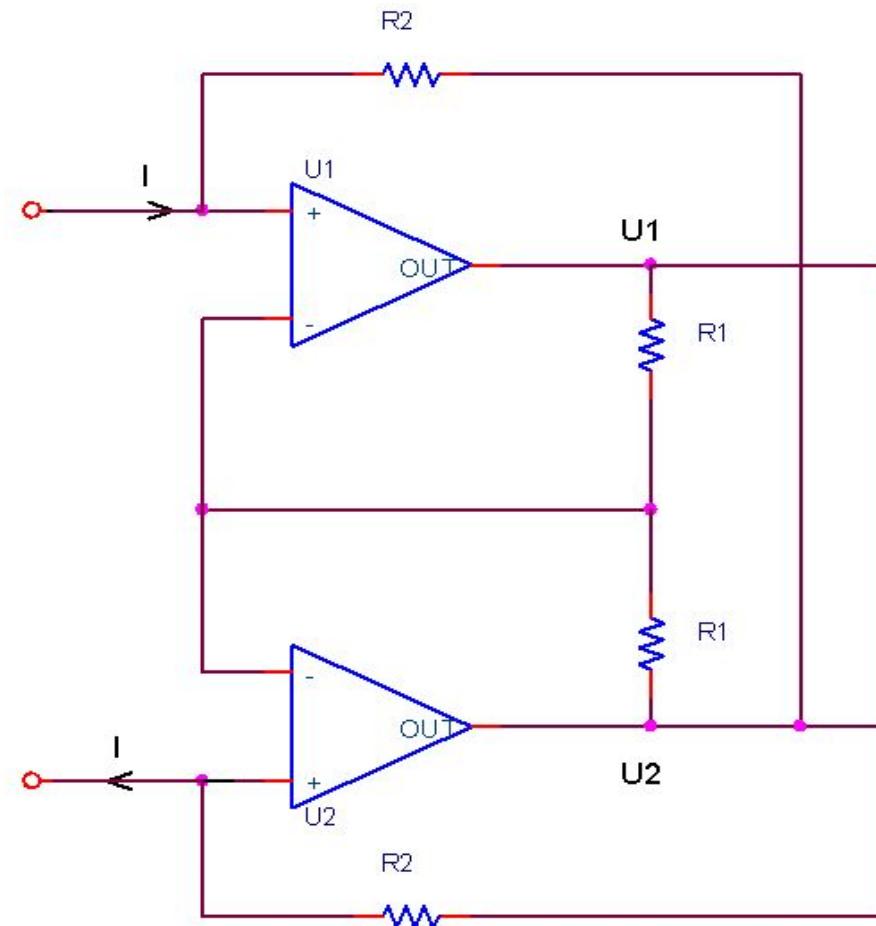
Voltage follower



Compensation of low pass behaviour of loop gain

Current to voltage conversion

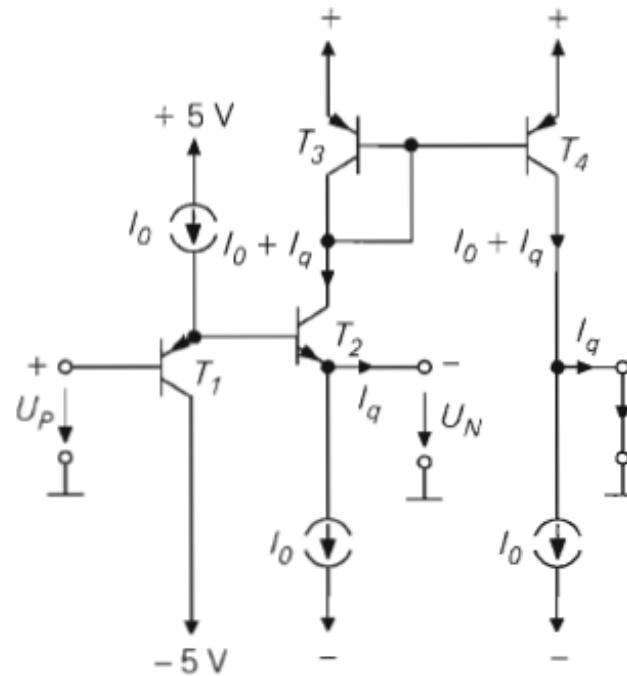
Determine the transfer characteristic
of the following circuits:



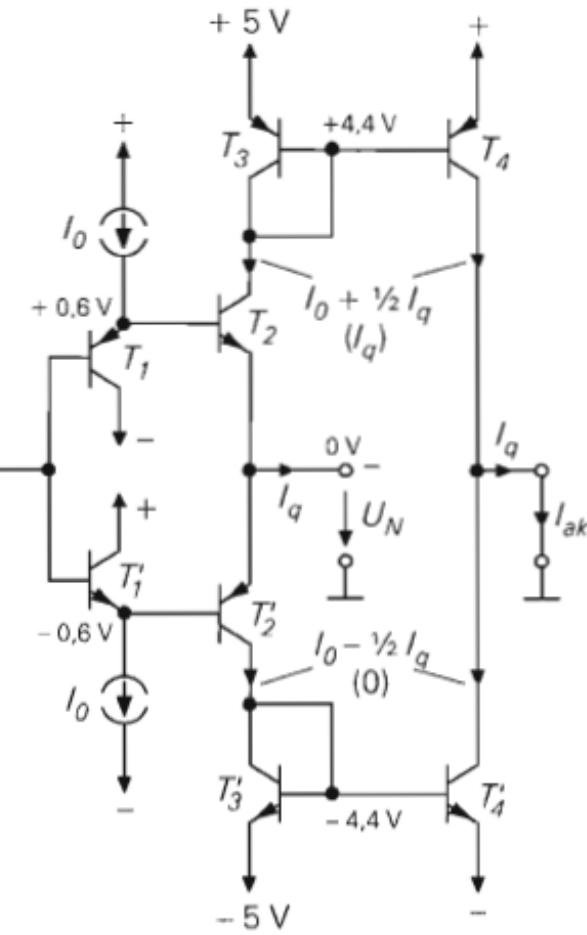
Current amplifier circuit

As compared to CV amplifier: emitter follower at output omitted.

Current gain defined by mirror T_3, T_4



Circuit idea



Realisation, e.g. OPA660

Symbols and model of current amplifier

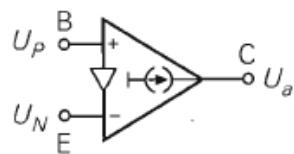
This current amplifier behaves like a transistor:

- **Collector current = emitter current**
- Base input resistance high, emitter input resistance low
- **Collector output resistance high**

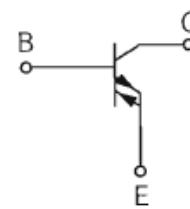
Differences from a simple transistor:

- Collector current has inverted direction
- **$U_{BE} = 0$ (the ‘perfect’ transistor!)**
- Operating point internally defined
- **Emitter and collector currents can flow in both directions**

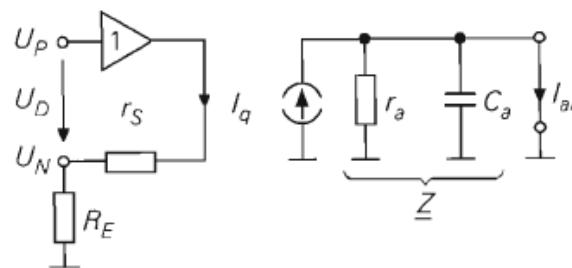
Trade name: *Diamond transistor (Burr Brown)*



a OPV
Schaltsymbol



b Transistor
Schaltsymbol



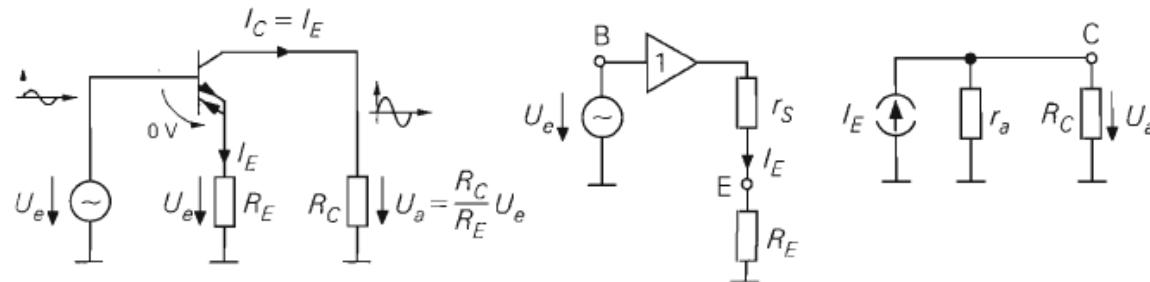
c Modell

$$S = \frac{I_{ak}}{U_D} = \frac{1}{r_s} \quad \text{with external resistance } R_E \text{ at emitter: } S_B = \frac{I_{ak}}{U_P} = \frac{1}{r_s + R_E}, \quad A_B = S_B R = \frac{R}{r_s + R_E}$$

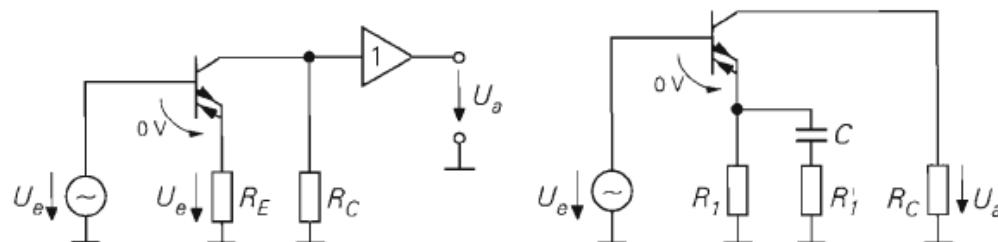
Emitter coupling of current amplifier

Emitter circuit = current feedback at inverting input

Common emitter circuit, and model:



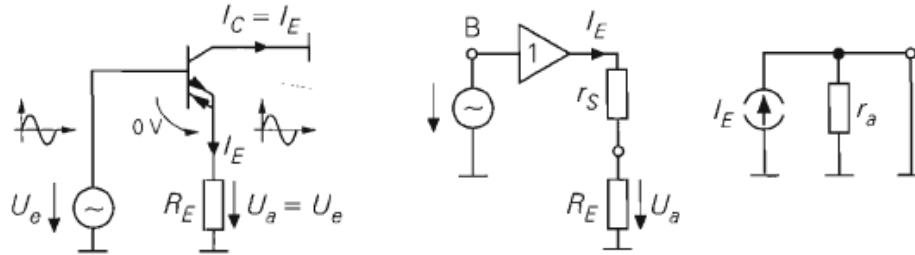
Emitter circuit followed by collector circuit to avoid influence of load on gain.
High frequency gain drop counter-acted by reduction of R_E :



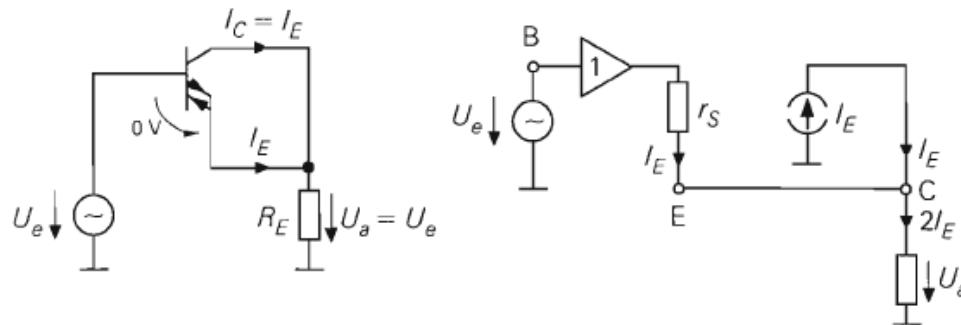
Remark: Develop the gain and impedance relations of circuits on slides 11...20 as exercise.

Collector coupling of current amplifier

Collector circuit = output at emitter, collector grounded (operating point internally fixed)

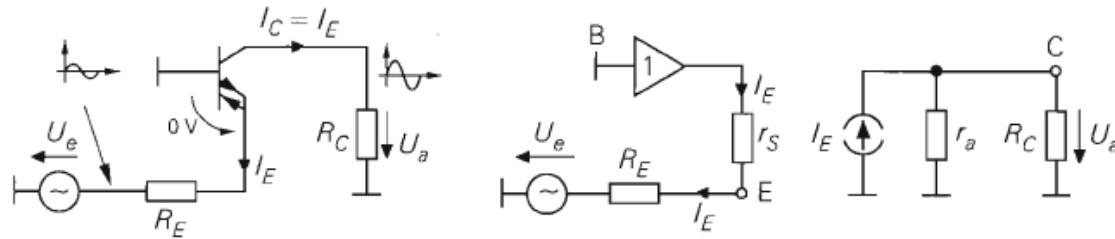


Alternatively, collector and emitter can be connected together to obtain twice the output current:
The output resistance is halved.



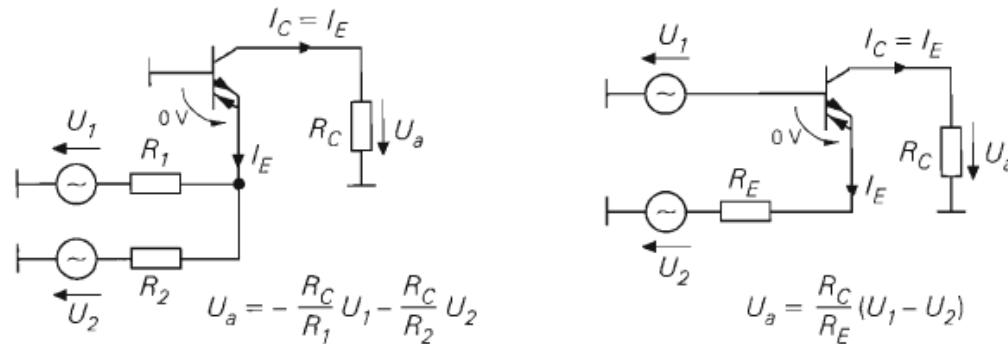
Base coupling of current amplifier

Base circuit = input at emitter, collector is output



Compared to simple transistors, the gain in emitter and base circuits has changed sign.

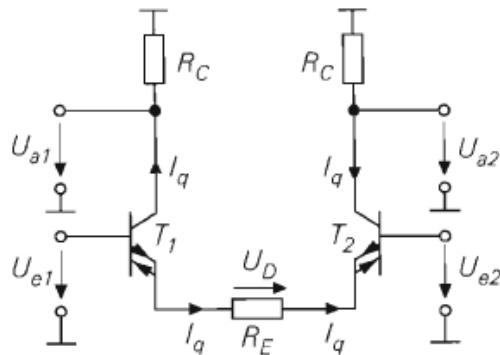
The base circuit can be used for addition and together with the emitter circuit for subtraction:



Difference amplifier with two current amplifiers

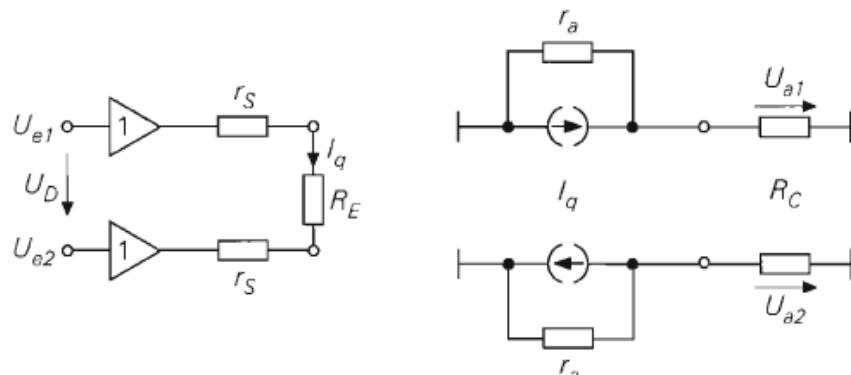
Collector resistances grounded since operating point internally determined.

E.g. MAX435, OPA2662 (duals)



R_E determines the gain.

Model:



Application example: high bandwidth precision rectifier

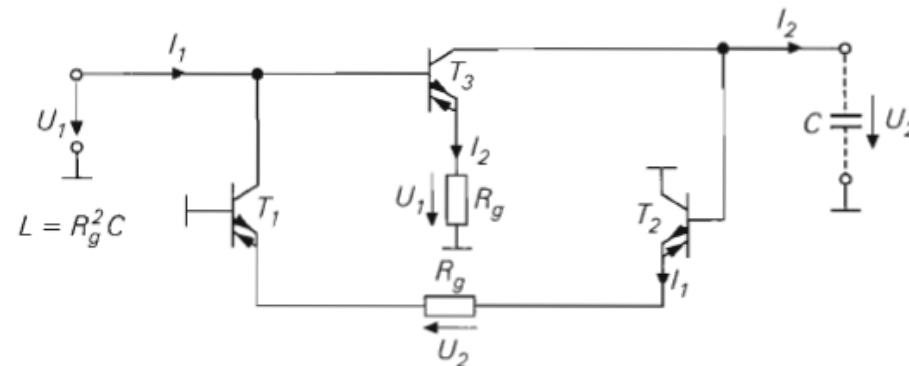
Gyrator with current amplifiers

Gyrator = dual of a transformer

$$I_1 = \frac{1}{R_G} U_2$$

$$I_2 = \frac{1}{R_G} U_1$$

E.g. SHC615



Interesting property: inductance simulation with C at port 2: $L = R_g^2 C$

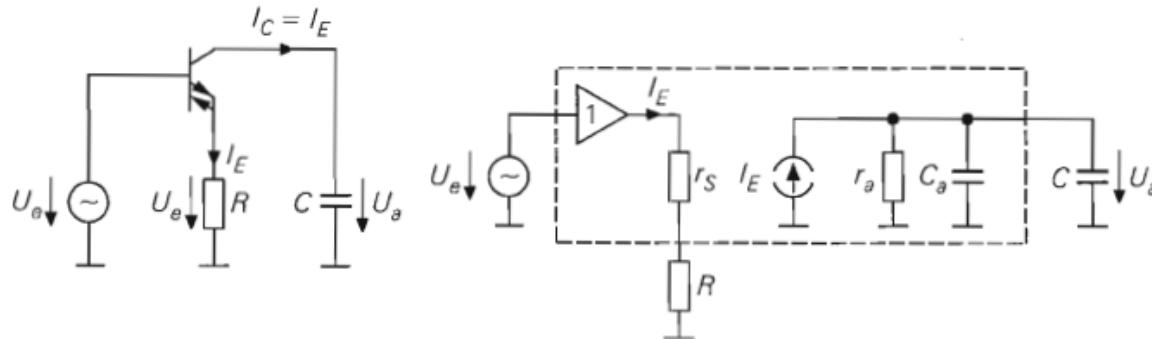
With C at ports 1 and 2, a parallel resonant circuit is realized.

Integrator with current amplifier

Integrator = capacitor fed by current source.

Non-inverting integrator!

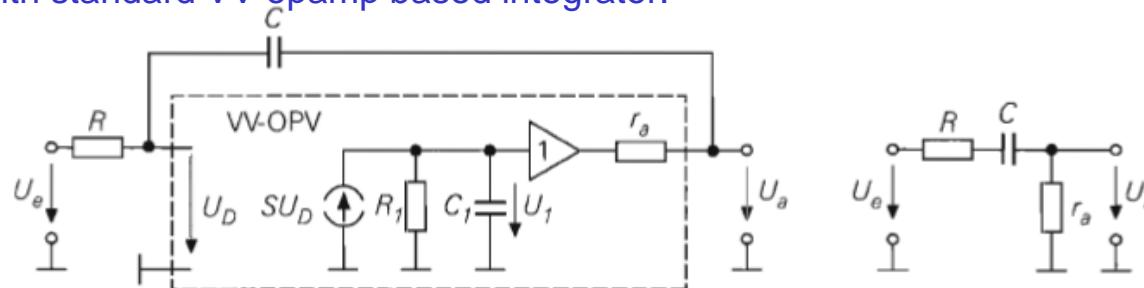
Voltage output should be run through impedance converter.



$r_a(C_a+C)$ represents a lower frequency limit of the integrator.

Upper frequency limit very high.

Comparison with standard VV opamp based integrator:

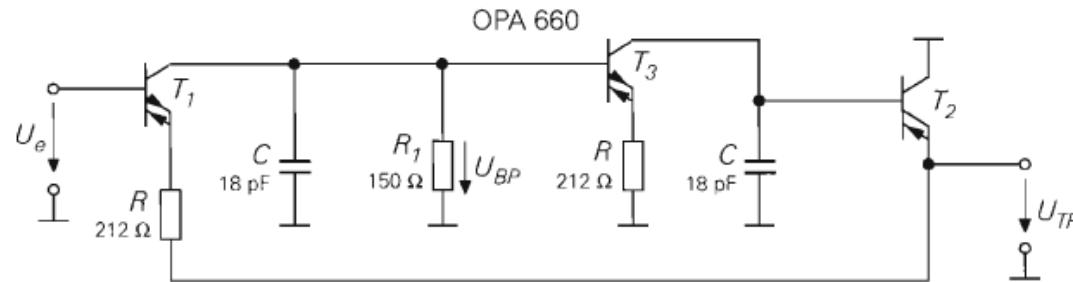


f_T is upper frequency limit.

Second order band-/low- pass with current amplifier

Active high frequency filters based on integrators.

Two integrators followed by an impedance converter form second order stage:



Values are for Butterworth design with $f_g = 30\text{MHz}$

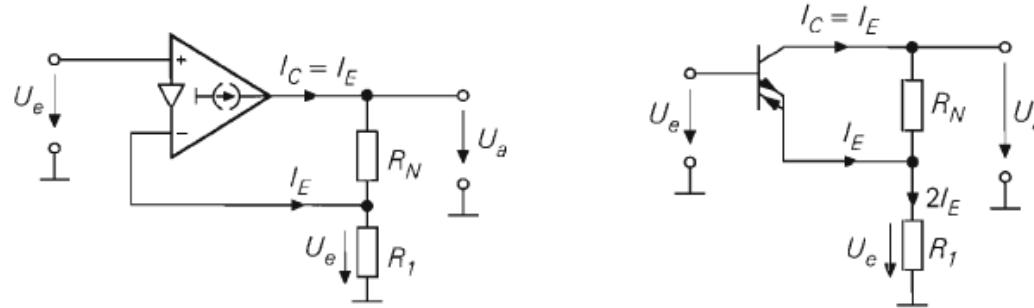
Assuming $r_s = 10\Omega$ and $C_a = 6\text{pF}$.

Operates up to 300MHz.

f_g and quality factor can be set independantly.

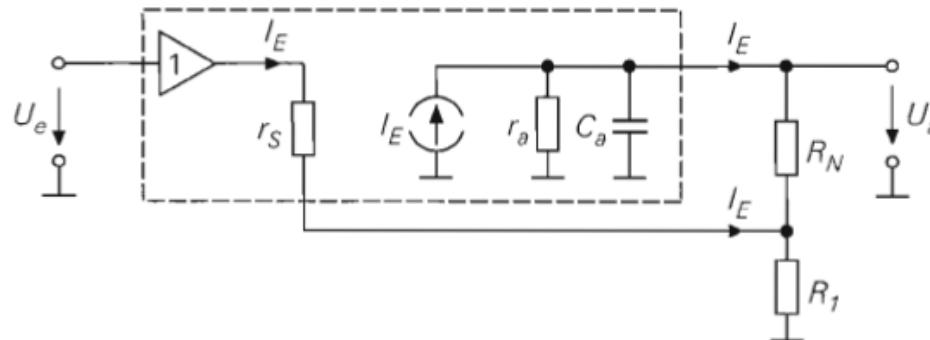
Applications with voltage feedback

Feed back part of the output to inverting input, using voltage divider.



'Direct feedback' since no impedance conversion at out- and inputs.

Corner frequency $\omega_g = 2/(R_N C_a)$



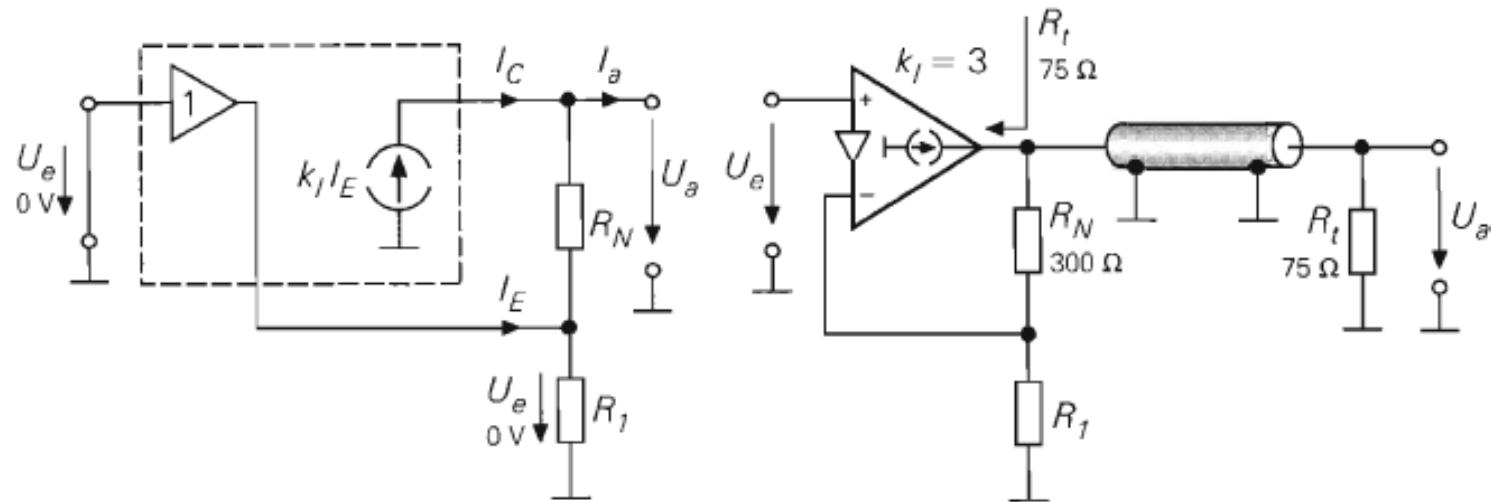
Output resistance $r_a = R_N/(k_i + 1)$ with $k_i = I_C/I_E$

Gain and output resistance can be set from outside \Rightarrow trade name **drive-R-amplifier** (Comlinear)

Active termination

With output resistance determined by R_N .

Reduced power dissipation in R_N , as compared to VC amplifier.



Current amplifier

- Determine the transfer relations of the circuits in slides 11...20
- How does the output resistance of the circuit in slide 20 depend on R_N ? Determine the transfer gain of the same circuit.
- Determine the transfer function describing the dynamic behaviour of the circuit in slide 18.

Low noise 75 Ohm driver

Propose a circuit based on a MAX436 and an OP37 amplifier capable of driving a 75 Ohm load with the noise floor of the output determined by the OP37 amplifier.

Determine the bandwidth of the driver and check its stability with 300pF capacitive load.

If an instability occurs, propose an appropriate circuit modification.

Books

Tietze, Schenk: *Halbleiter-Schaltungstechnik*, Springer 1999 (11th ed.), ISBN 3-540-64192-0

This book was used as a basis for the present presentation, the illustrations are taken from it.

Millman: *Microelectronics: Digital and Analog Circuits and Systems*, McGraw-Hill 1984, ISBN 0-07-066410-2

Chatelain, Dessoulavy: *Électronique*, Traité d'électricité: vol VIII, PPUR 1982, ISBN 2-604-00010-5

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Jung: *OpAmp Application Handbook*, Analog Devices 2005, ISBN 0-750-67844-5

Mancini: *OpAmps for everyone*, Texas Instruments 2002

Contents

- Noise fundamentals
- Noise optimisation

- Exercices
- References

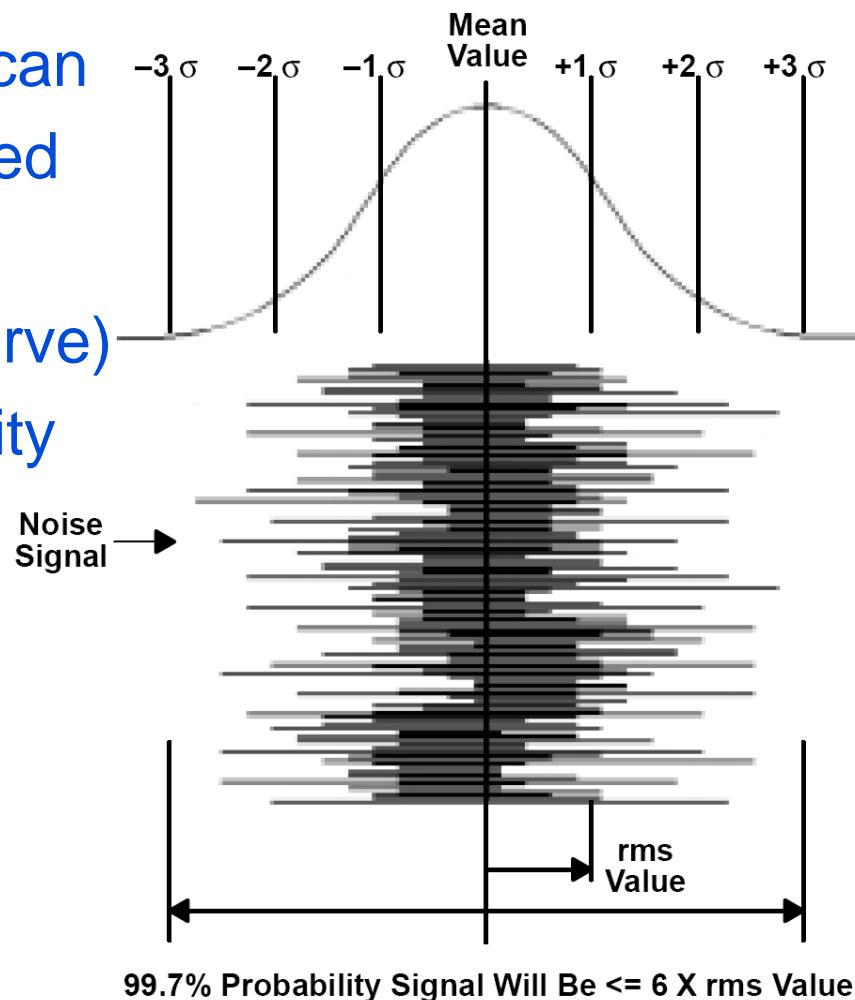
Noise signals

- Are random signals: aperiodic, instantaneous values can never be predicted.
- Can be generated internally in active circuits, e.g. operational amplifiers, in passive components or be injected into a circuit from external sources.
- The signal-to-noise ratio is

$$\frac{S_{(f)}}{N_{(f)}} = \frac{\text{rms signal voltage}}{\text{rms noise voltage}}$$

Noise statistics

- Noise signals can be characterized by histograms (e.g. Gauss curve) or power density spectra (e.g. uniform).



Geometric addition of multiple sources of noise

Independent random signals: rms values do not add linearly but geometrically

$$E_{\text{Totalrms}} = \sqrt{e_{1\text{rms}}^2 + e_{2\text{rms}}^2 + \dots e_{n\text{rms}}^2}$$

Units of spectral density of noise

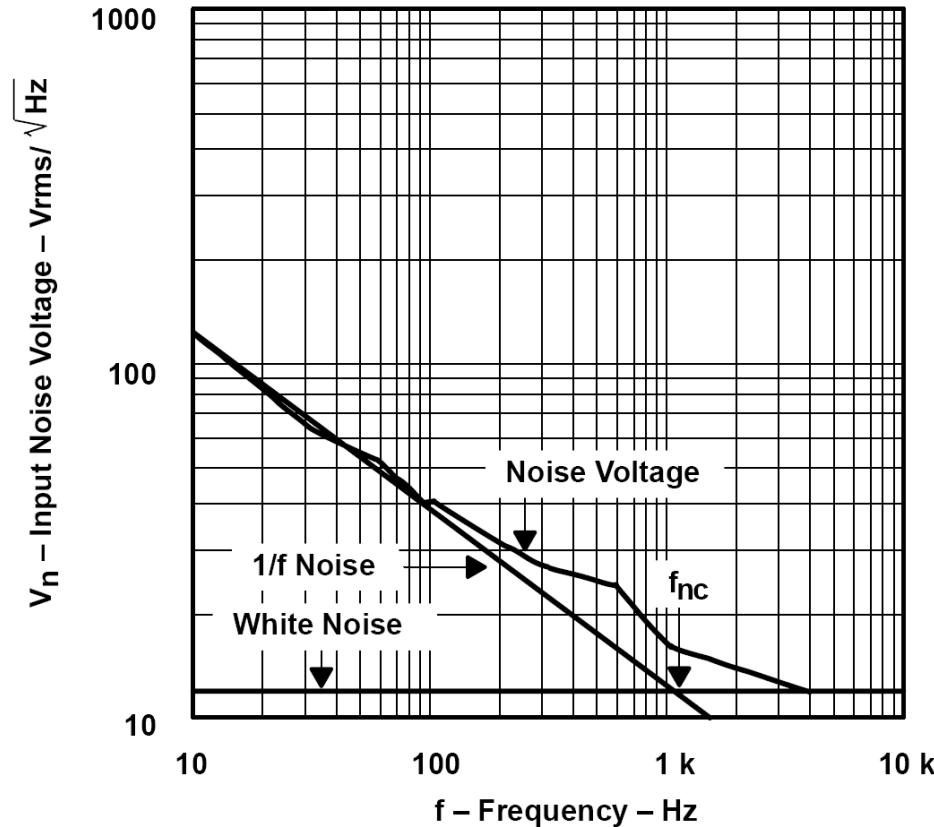
Derived from power spectral density in [V²/Hz] or [A²/Hz], referred to a reference resistor (1Ω by default).

$$\frac{V_{rms}}{\sqrt{Hz}} \quad or \quad \frac{A_{rms}}{\sqrt{Hz}}$$

Corner frequency in operational amplifier noise

Here is an example of an input referred voltage noise spectrum:

It can be roughly decomposed in a uniform part above f_{nc} , and a part increasing with $1/rtf$, below f_{nc} .



Low frequency $1/f$ power spectral density is measured with many natural signals, in particular temperature, and in all semiconductors.

Attention: Total power diverges, which is a paradox.

Noise corner frequency

If datasheet curves are not in logarithmic scale or corner is not pronounced, determine f_{nc}

Example :

For the TLV2772, the figure shows a noise density of $130 \frac{nV}{\sqrt{Hz}}$ at 10Hz.

The datasheet of the TLV2772 shows a white noise density of $12 \frac{nV}{\sqrt{Hz}}$.

On the 1/f noise power curve the product frequency x noise power density is constant:

$$\left[\left(\frac{130nV}{\sqrt{Hz}} \right)^2 - \left(\frac{12nV}{\sqrt{Hz}} \right)^2 \right] \cdot 10Hz = 167560(nV)^2$$

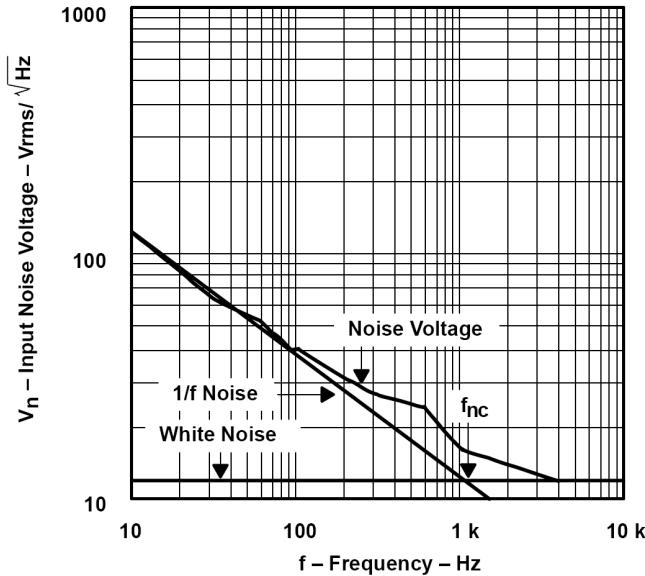
At f_{nc} , the 1/f noise power density is $12nV/\text{rtHz}$:

$$\frac{167560(nV)^2}{\left(\frac{12nV}{\sqrt{Hz}} \right)^2} = 1164 \text{ Hz}$$

Total bandwidth limited noise

Determine the total noise within a given bandwidth, e.g. 10Hz...10kHz

Method: Noise voltage is root of noise power. First integrate power, then determine voltage.



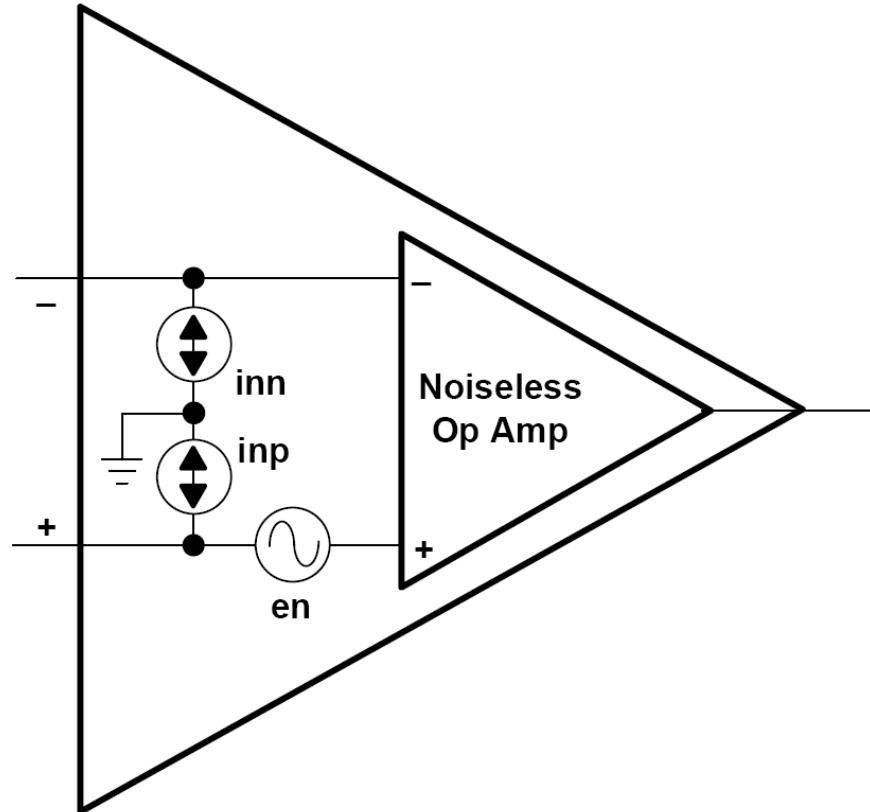
$$E_n = E_{whitenoise} \cdot \sqrt{f_{nc} \cdot \ln\left(\frac{f_{max}}{f_{min}}\right) + (f_{max} - f_{min})}$$

$$E_n = \frac{12\text{nV}}{\sqrt{\text{Hz}}} \cdot \sqrt{1164\text{Hz} \cdot \ln\left(\frac{10^4 \text{Hz}}{10\text{Hz}}\right) + (10^4 \text{Hz} - 10\text{Hz})} = 1.61\mu\text{V} = -116\text{dBV}$$

Operational amplifier input referred noise

Noise sources are added to ideal operational amplifier like bias and offset sources at the inputs.

The effect on the output is computed in analogy to that of bias and offset sources, using superposition.



Attention: Superposition of different noise contributions will be geometric.

Exercice

Noise performance data of OP37

Search for noise performance data in the OP37 datasheet.

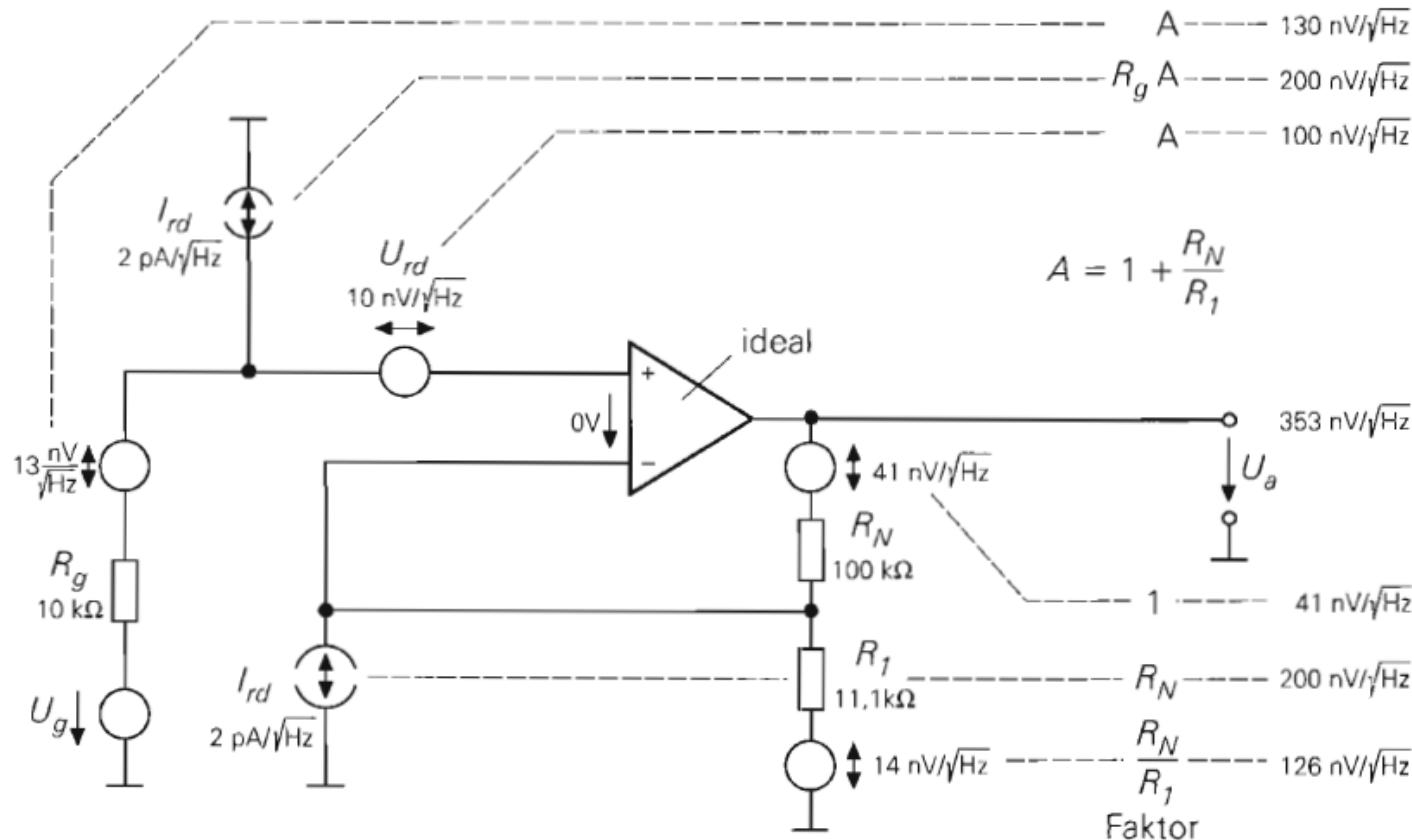
Determine the corner frequencies of voltage and current noise. At which input resistance will voltage and current white noise levels generate equivalent contributions at the output ?

How high will the output noise then be ?

What will the noise corner frequency in this case become ?

Noise sources in a non-inverting amplifier

741 class example:

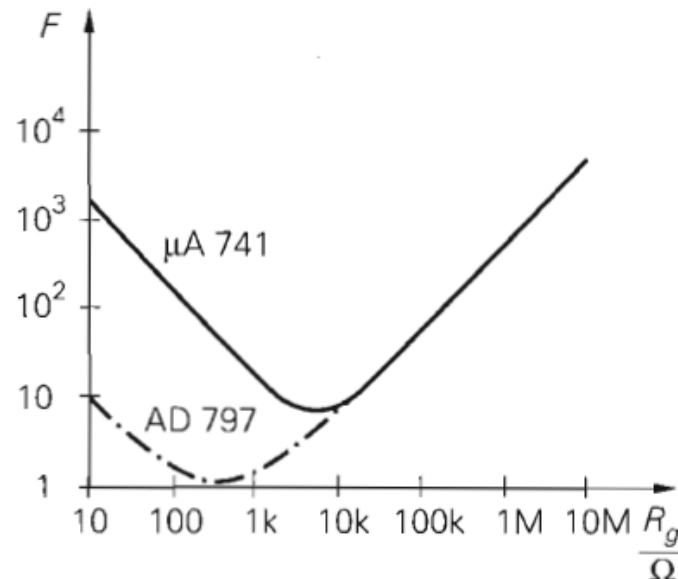
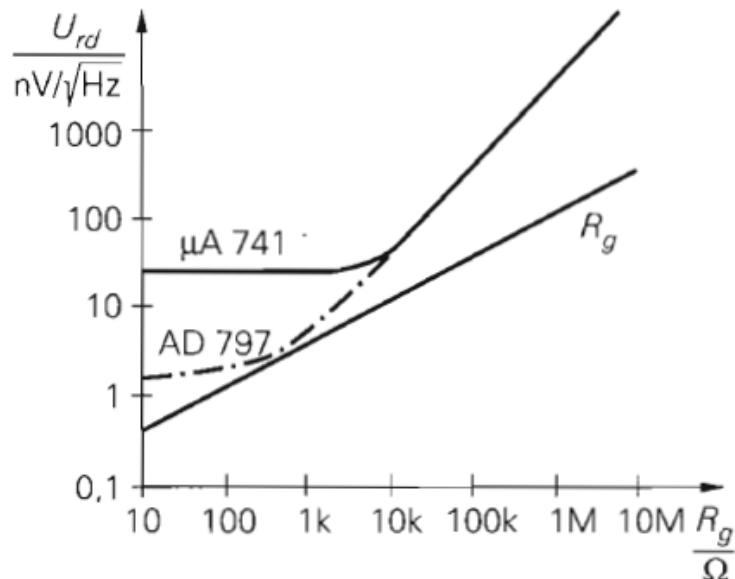


$$\text{Resistor noise: } U_R = \sqrt{4 k T R (f_{\max} - f_{\min})} \quad k = 1.38 \cdot 10^{-23} \text{ J/K} \text{ Boltzmann constant}$$

Noise voltage and noise number

$$F = \left(\frac{\text{Noise voltage at real amplifier output}}{\text{Noise voltage at ideal amplifier output}} \right)^2$$

Function of source resistance:

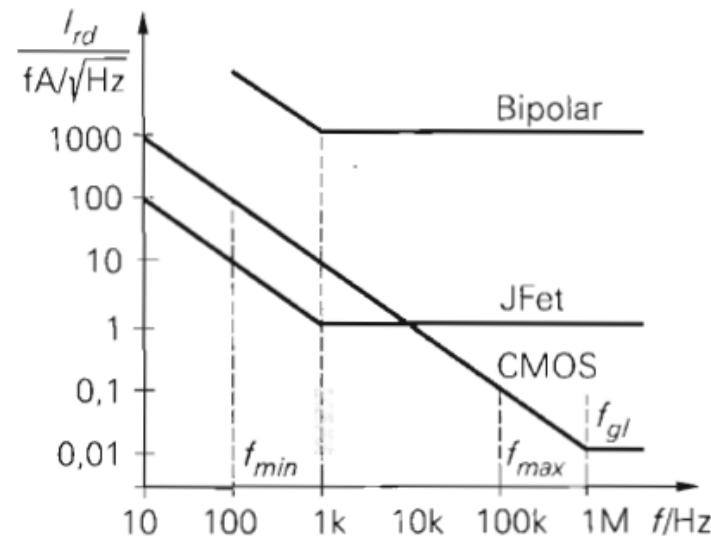
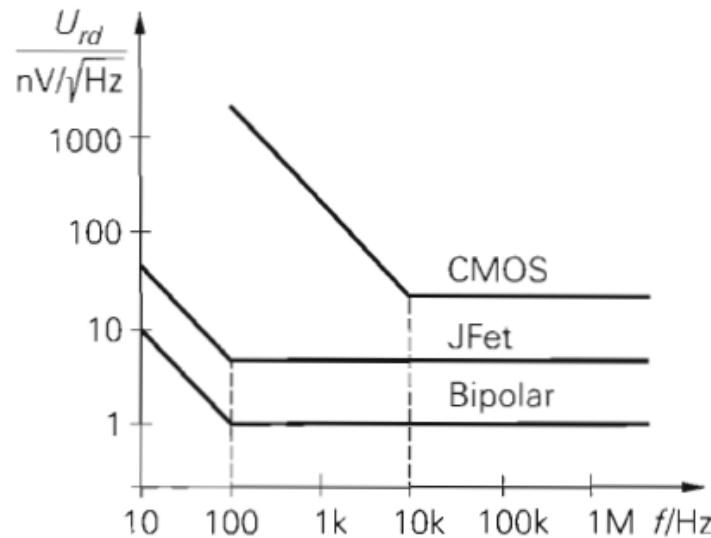


At low R_g , amplifier input referred voltage noise dominates, at high R_g current noise.

Voltage and current noise performances

CMOS circuits tend to have less current but more voltage noise.

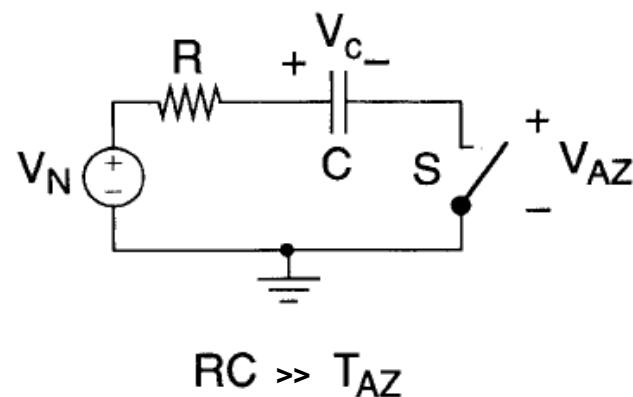
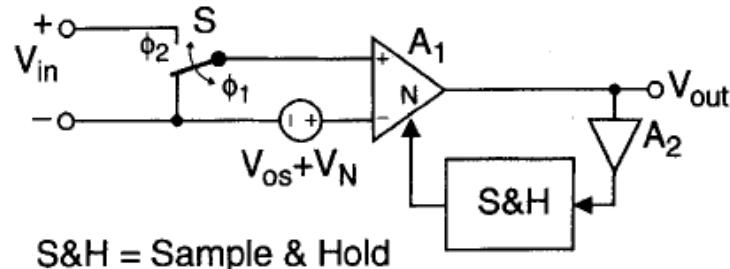
CMOS circuits also tend to have higher noise corner frequencies.



Recall: $n(\text{ano}) = 10^{-9}$, $p(\text{ico}) = 10^{-12}$, $f(\text{emto}) = 10^{-15}$, $a(\text{to}) = 10^{-18}$.

Auto-zero principle

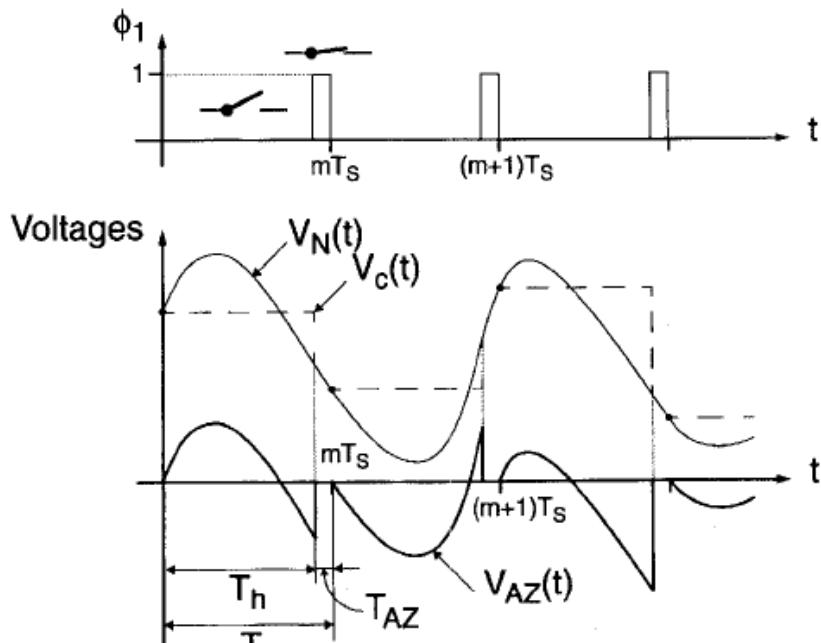
Cancel low frequency noise density increase by auto-measurement of the offset = low frequency noise.
Then subtract measured offset from input.



Usually the measured offset is stored on a capacitor.

Its discharge must be ^(a) much slower than the offset measurement period.

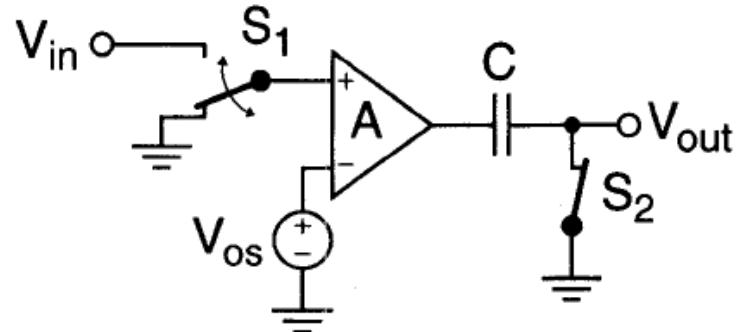
(a) Basic AZ circuit and autozeroed signal: (b) shows voltages in (a).



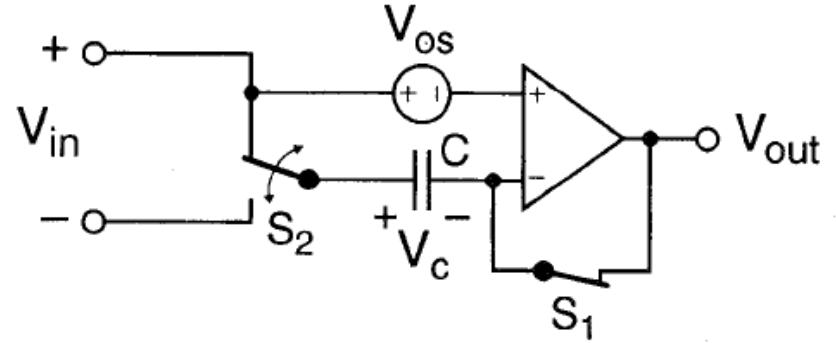
(b)

Auto-zero circuits

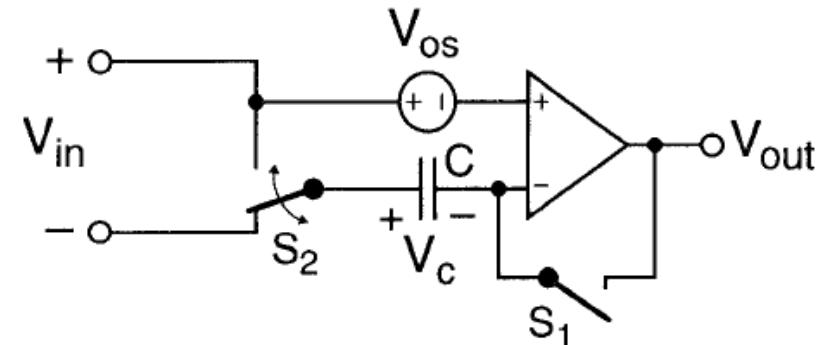
Open-loop cancellation



Closed-loop cancellation



(a)



(b)

Closed-loop-amplifier offset cancellation principle: (a) offset sampling phase (AZ) and (b) amplification phase.

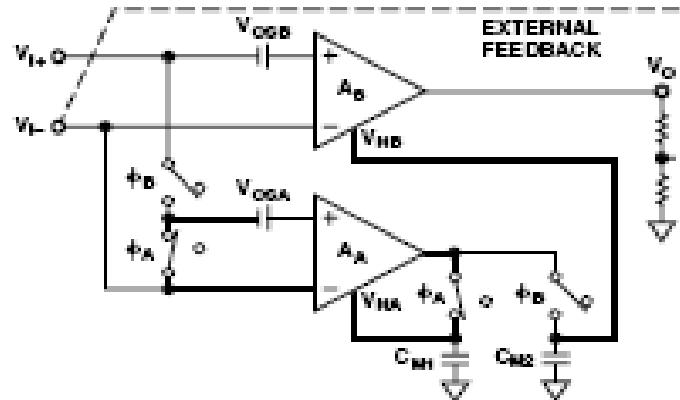
In closed-loop cancellation, the offset is stored on a floating capacitor which is more precise in switched capacitor circuits.

Auto-zero circuit with two amplifiers

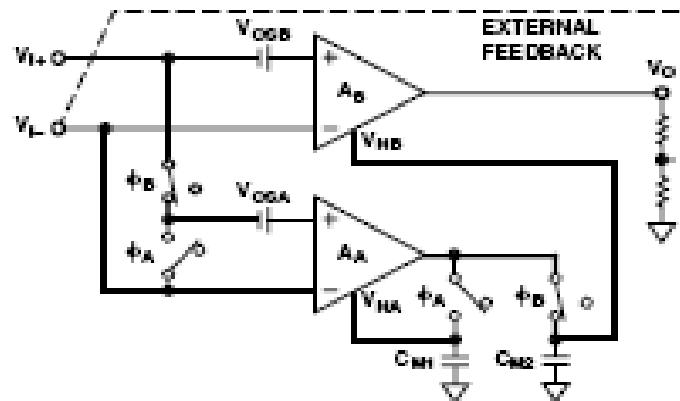
The drawback of auto-zeroing is that during the measurement, the principal function of the circuit is not operating.

Two parallel amplifier stages avoid this problem:

The null amplifier measures 'on-line' the main amplifier offset.



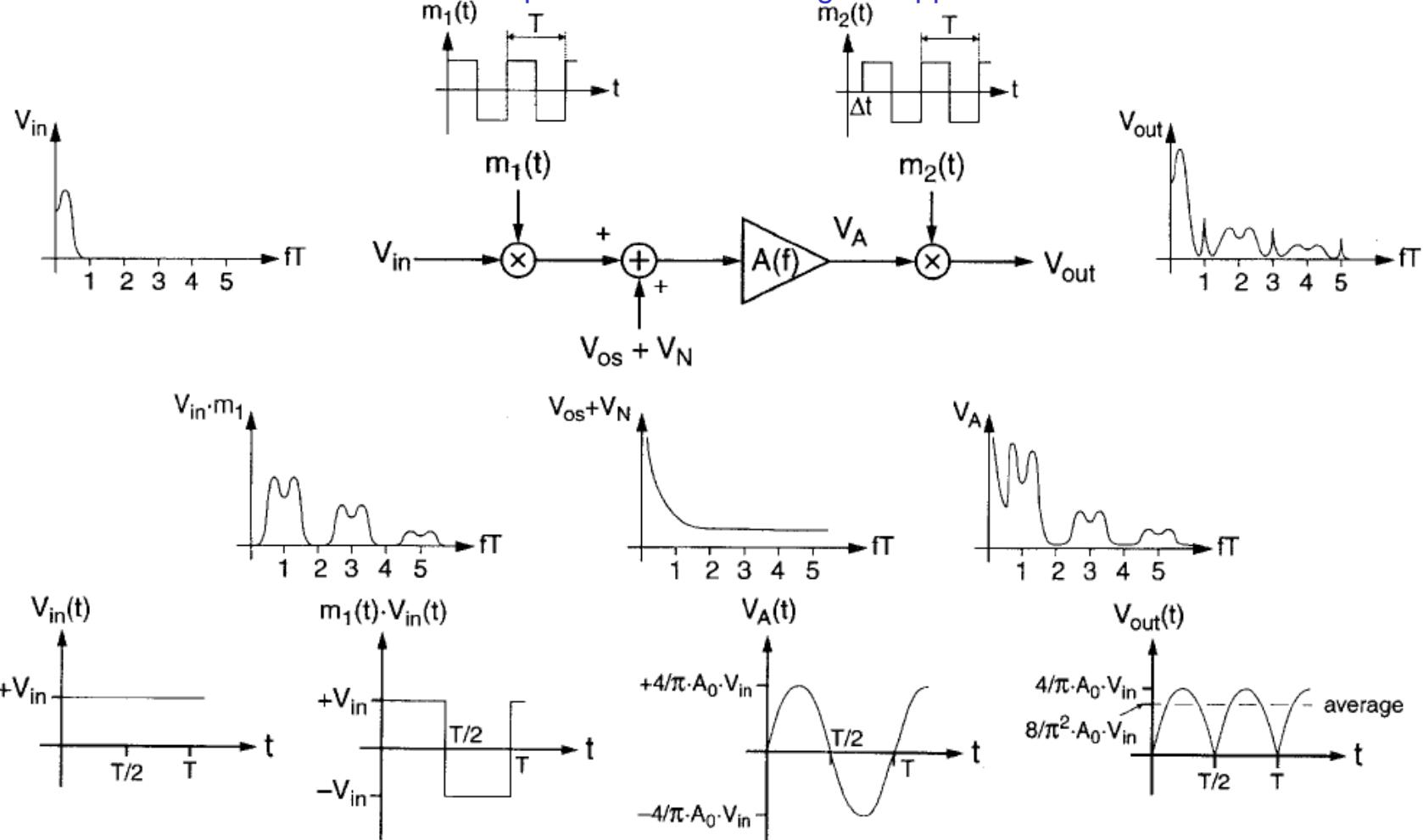
a. Auto-Zero Phase A: null amplifier nulls its own offset.



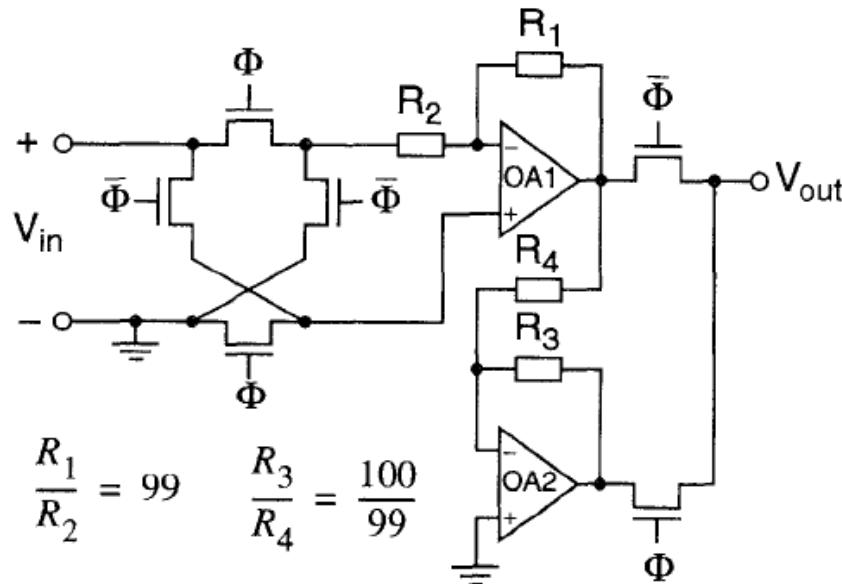
b. Output Phase B: null amplifier nulls the main amplifier offset.

Chopper amplifier principle

Correlated double sampling: The input signal is frequency shifted (modulated), while at the end of the chain the output is demodulated again. Application: in A/D converters.



Chopper amplifier circuit



Chopper amplifier switches are generally FETs.

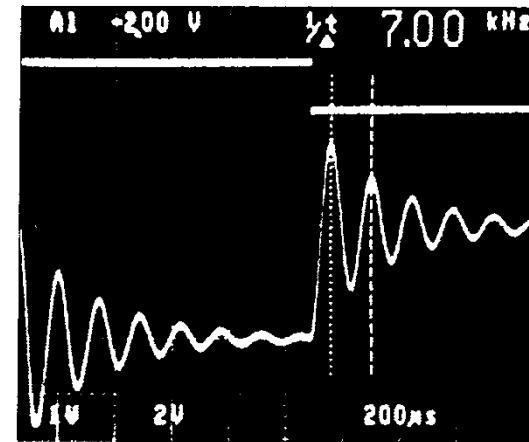
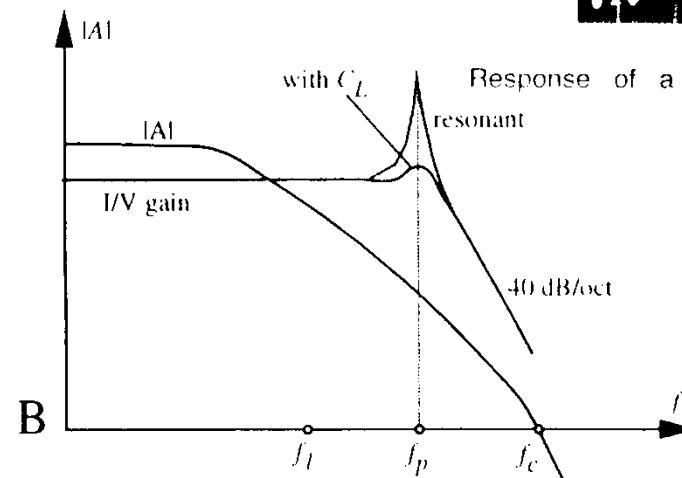
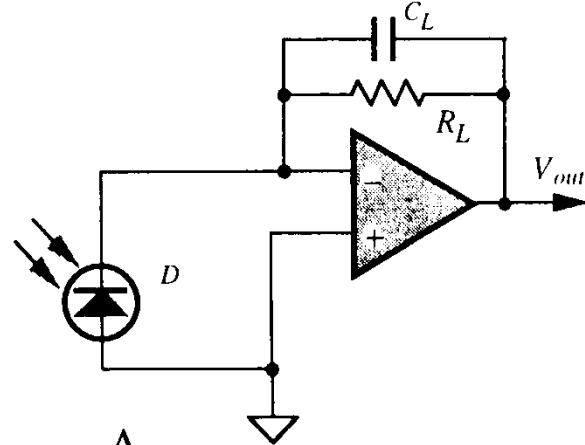
The technique lends itself to use in MOS-FET circuits.

Only two synchronous clocks are used, of opposite phases and with no overlapping.

Exercice:

Noise floor of photodiode current to voltage converter

Determine the transfer function of the circuit below with and without the feedback capacitor C_L . Explain the improvement realized with C_L .



Use of current-to-voltage converter (A) and the frequency characteristics (B).
 Determine the output noise voltage noise density spectrum for an OP37 amplifier, BPW34 photodiode, $R_L = 100\text{k}\Omega$, C_L such that $Q = 1$.

Exercice: TIA bandwidth extension

Consider the datasheets of OP470 (VV type) amplifier and 2N4393 FET transistors.

How can a standard VV amplifier be used in TIA configuration?

Propose a discrete difference amplifier stage in front of the operational amplifier.
The differential pair shall be connected in common source configuration.

Estimate the bandwidth of the circuit without and with
the discrete difference amplifier.

The feedback impedance is 3.3pF in parallel with $5.6\text{M}\Omega$. Suppose $I_{DS0} = 0.1\text{mA}$

Determine the noise floor spectrum at the output for a drain impedance
of first $1\text{k}\Omega$ and then of $1\text{M}\Omega$.

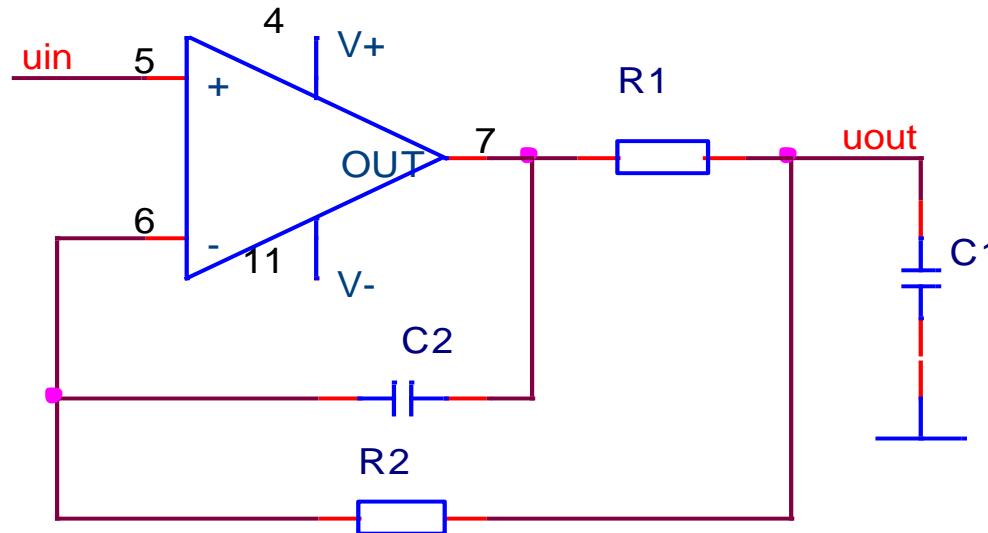
Stabilization of capacitive load

The following circuit represents a voltage follower driving a capacitive load. Determine its transfer function without and with R_1 , R_2 , C_2 . Use a first order model for the operational amplifier.

What is the use of R_2 ?

Suppose an OP37 operational amplifier, and $C_1 = 100\text{nF}$.

Propose values for R_1 , R_2 and C_2 , so as to make sure that the amplifier has $Q = 1$. What bandwidth can be achieved?



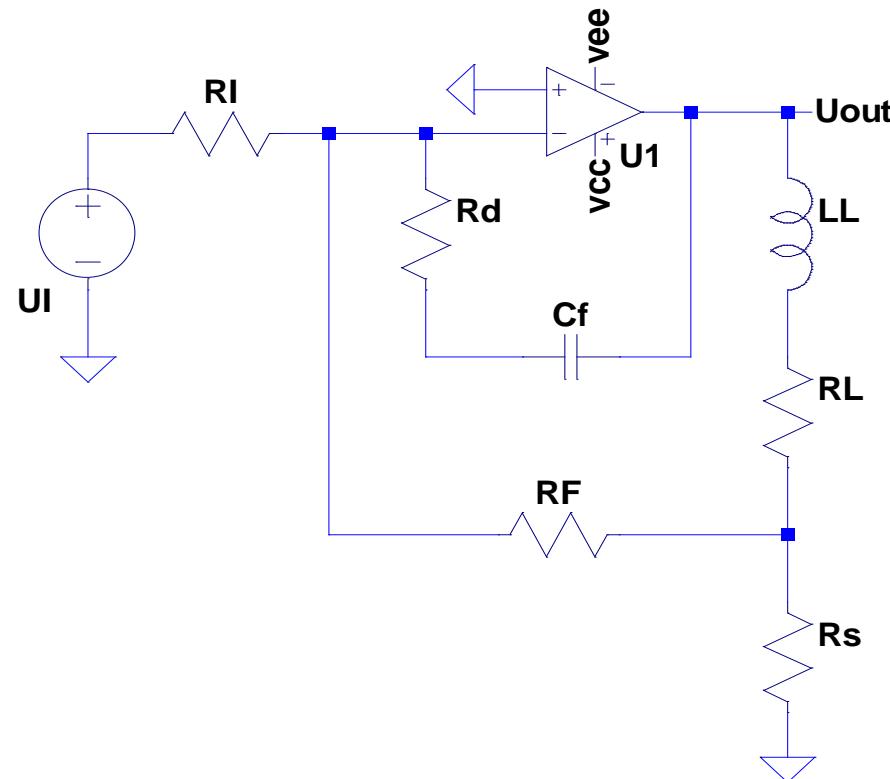
Stabilization of inductive load

The following circuit is a current source driving a voice coil.

Determine its transfer function with and without R_d , C_f . Suppose that all the load current circulates through R_s .

Suppose a PA07 power amplifier, and $L_L = 159\text{mH}$, $R_L = 10\Omega$, $R_s = 1\Omega$, $R_I = 5\text{k}\Omega$, $R_F = 1\text{k}\Omega$.

Propose values for R_d and C_f , so that the amplifier has $Q = 1$.



Books

Tietze, Schenk: *Halbleiter-Schaltungstechnik*, Springer 2012 (14th ed.), ISBN 3-540-64192-0

Millman: *Microelectronics: Digital and Analog Circuits and Systems*, McGraw-Hill 1984, ISBN 0-07-066410-2

Chatelain, Dessoulavy: *Electronique* , Traité d'électricité: vol VIII, PPUR 1982, ISBN 2-604-00010-5

Gray, Meyer: *Analysis and Design of Analog Integrated Circuits*, Wiley 1984 (2nd ed.), ISBN 0-471-81454-7

Jung: *OpAmp Application Handbook*, Analog Devices 2005, ISBN 0-750-67844-5

Mancini: *OpAmps for everyone*, Texas Instruments 2002

Contents

- Principles of DA and AD conversion
- Static performance characteristics of DAC and ADC
- Review of DA converter structures

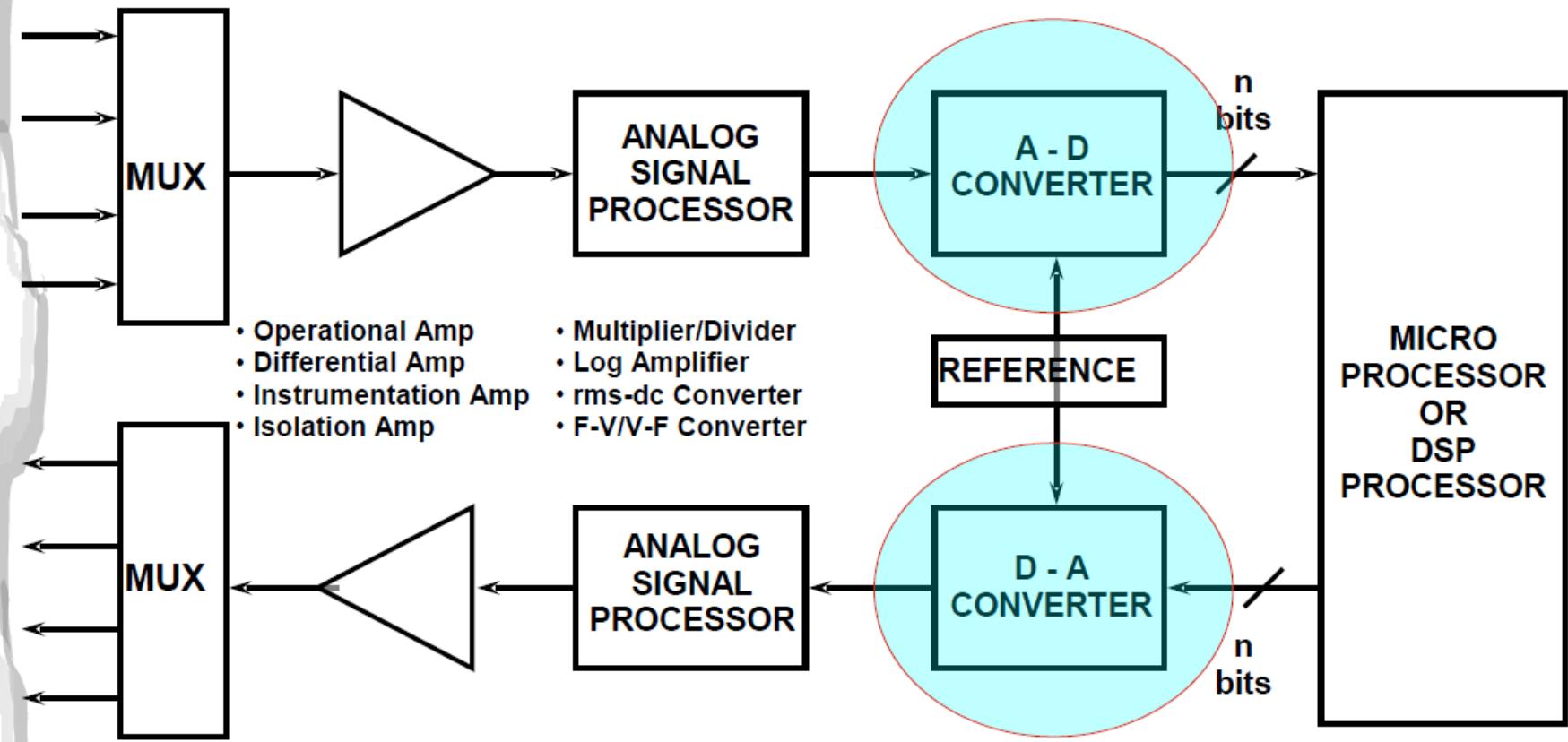
- Exercises
- References

Converter's basics

Physical Domain

↔

Digital Domain



Converter's basics

3

AD & DA Converters are not only circuits but must be seen as a SYSTEM, with two kind of processes :

- ⌘ Quantization of the AMPLITUDE (today)

- ⌘ Quantization of the TIME (next week!)

AMPLITUDE Quantization

* (Analog) Signal Vs (Digital) Number [1.2]

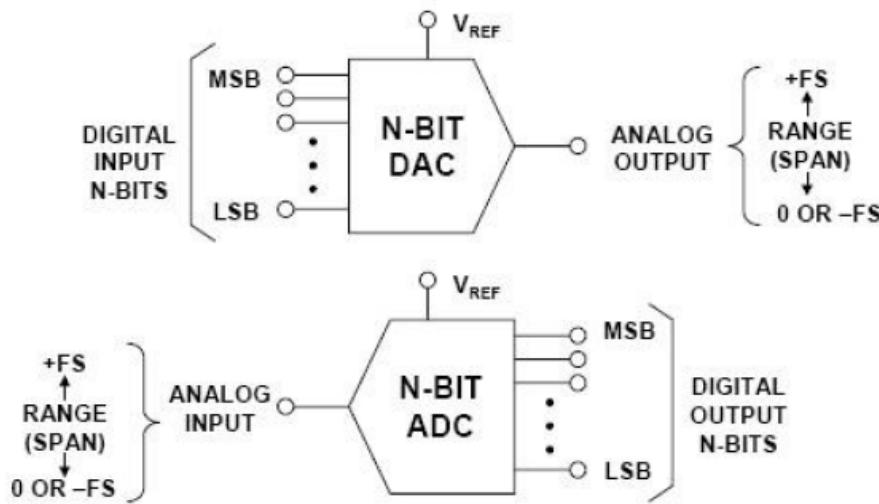


Figure 2.1: Digital-to-Analog Converter (DAC) and Analog-to-Digital Converter (ADC) Input and Output Definitions

Analog Side: Full Scale

- ⌘ Amplitude of the analog domain must meet the **Full Scale** of the converter (FS value)
 - FS is a technological constraint of the converter (Circuit selection!)
- ⌘ FS is related to a **Reference Value** (V_{REF})
- ⌘ « Input Voltage » right understanding!
 - Input Channel single-ended (SE) or differential (Diff) ?
 - Unipolar or bipolar ? Middle value of FS at 0V or $V_{CC}/2$ (or ...)

Analog Side: Dynamic Range

6

- ⌘ The Dynamic Range is the ratio of the larger and the smaller voltage of the INPUT SIGNAL
- ⌘ DR is a primary characteristic of the application, not of the converter!
- ⌘ Converter have to be better than signal's DR, but how much better?

Def. : Resolution

- ⌘ Resolution N is the *number of bits* of the digital number side
- ⌘ Resolution Step is the *analog value* of the interval between two adjacent code values, also called « 1 LSB »
- ⌘ 2^N digital levels (codes) : [0 to $2^N - 1$]
 - $\text{Nbr}_{\text{MAX}} = 2^N - 1$: « 1111111... »
 - By def. « all-1's code » => 1 lsb below FS value

Coding style of numbers



⌘ Number's coding : format of codes are ...

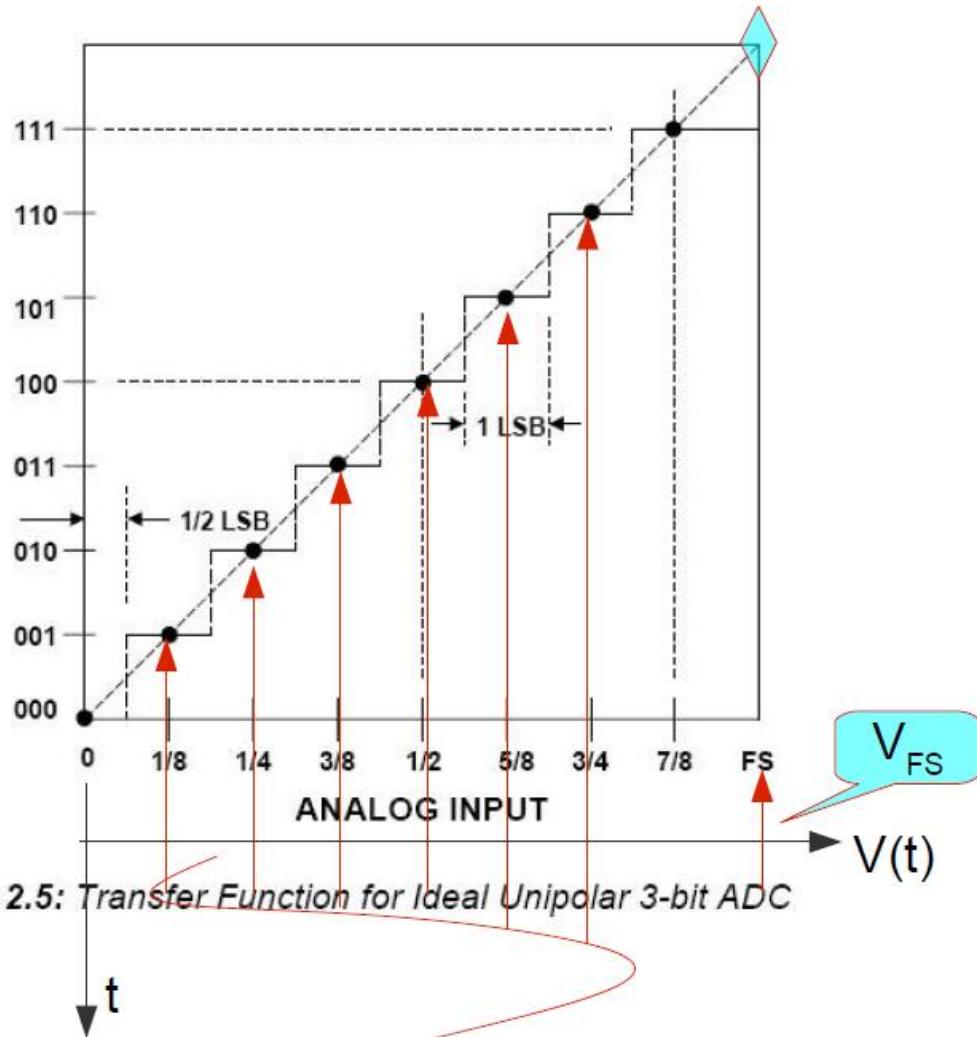
- Straight binary
- (Gray)
- Offset binary
- 2's complement
- (1's complement)
- (sign + magnitude)

Def. : Transfer Function

⌘ Ideal TF

DIGITAL
OUTPUT
(STRAIGHT
BINARY)

$$\text{Code} = \frac{V_{IN}}{V_{FS}} * 2^N - 1$$

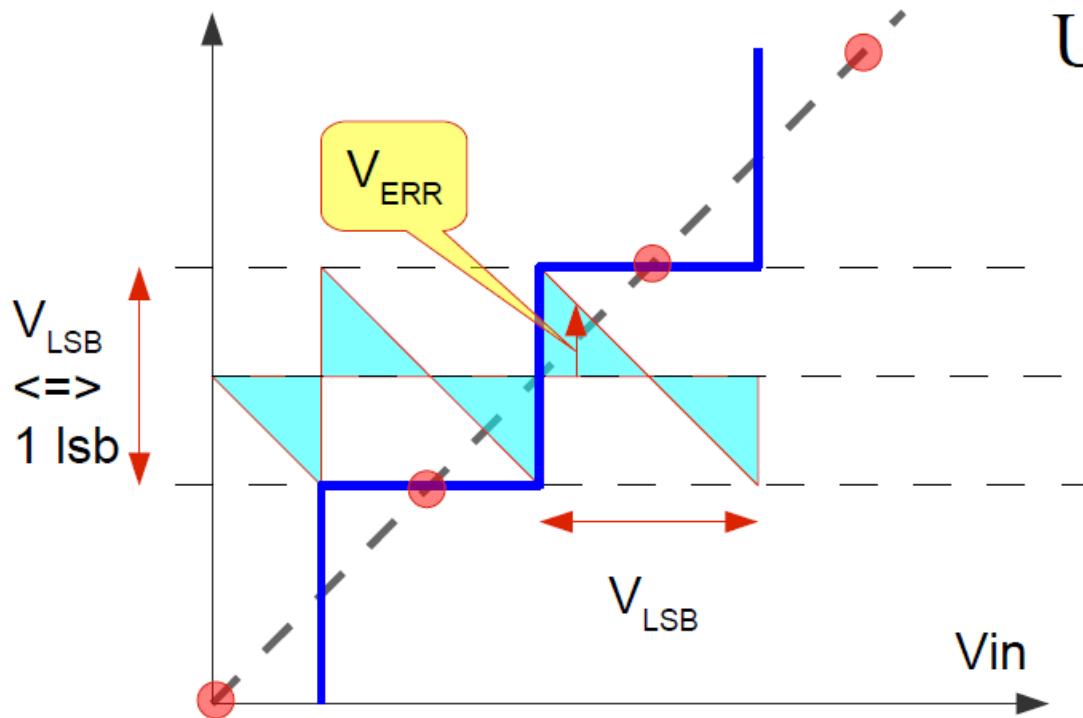


Amplitude quantization error

10

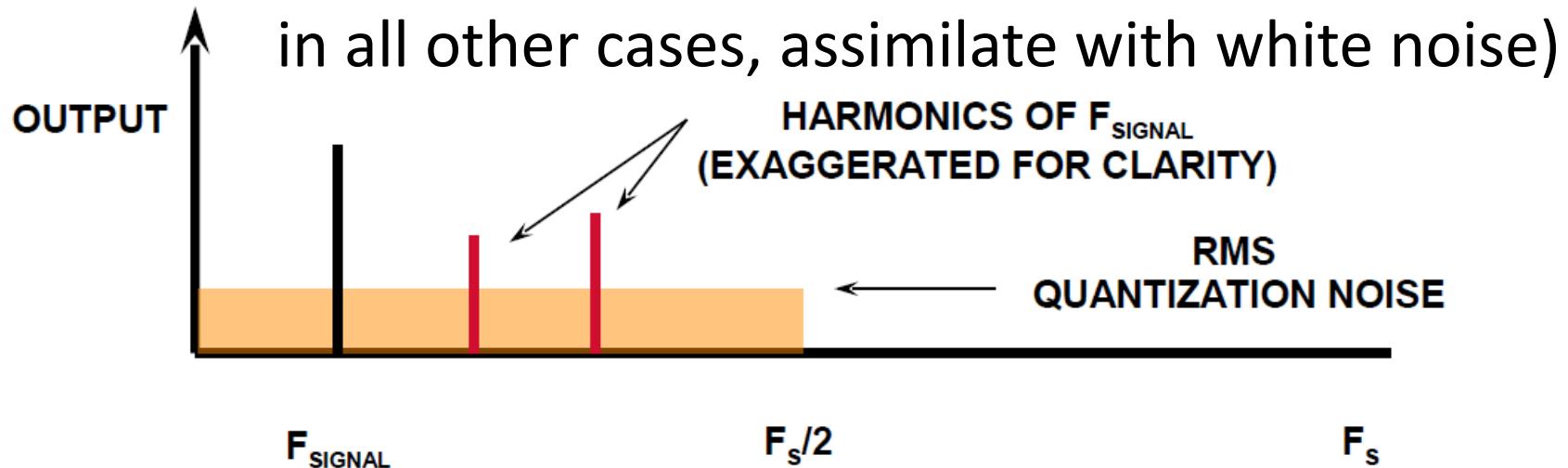
⌘ Power : $E_N = \frac{1}{V_{LSB}} \int_{-q/2}^{q/2} V_{ERR}^2(V_{IN}) dV_{IN} = \frac{V_{LSB}^2}{12}$

$$U_{N(RMS)} = \frac{V_{LSB}}{\sqrt{12}}$$



Amplitude quantization error

- * Quantization error is assumed to be white noise : folded in the base band, the noise level is $(1.76 + N \cdot 6.02) dB$ below the full-scale SINUS power level.
=> quantization is distortion!
(of synchronously sampled, periodic signals,
in all other cases, assimilate with white noise)



Real Transfer Function

⌘ Ideality don't exist in physics !

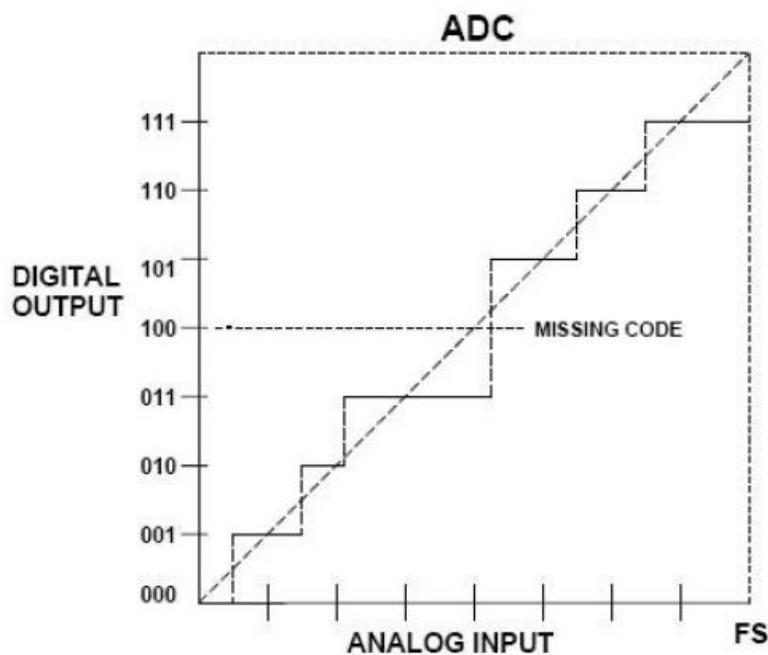
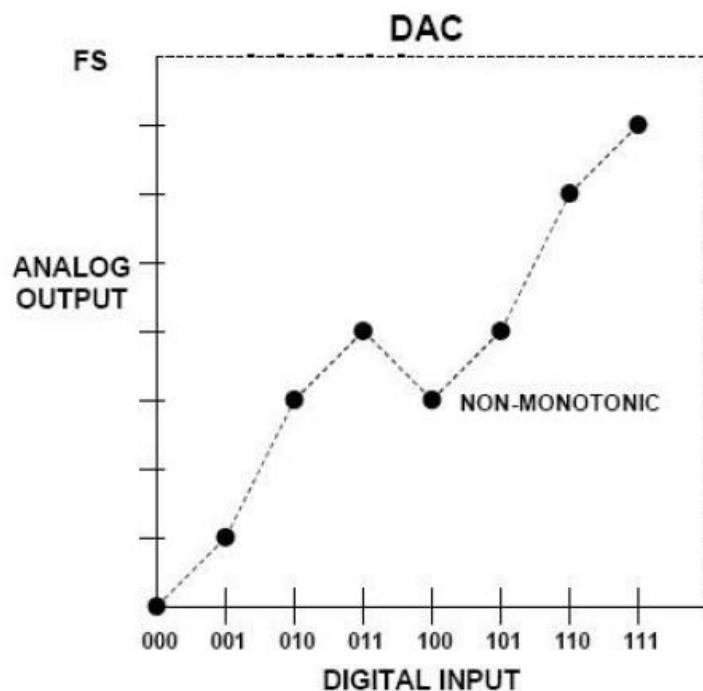


Figure 2.19: Transfer Functions for Non-Ideal 3-Bit DAC and ADC

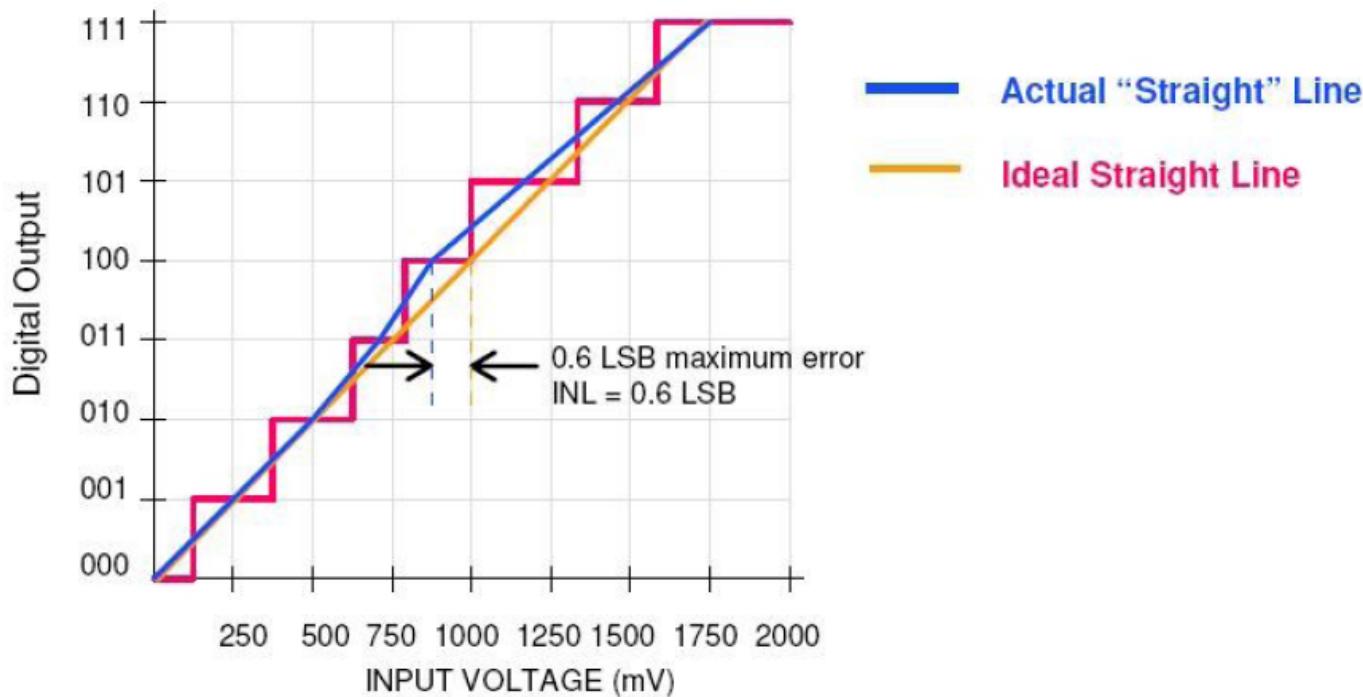
Def. : INL

- ⌘ Integral Non-Linearity : a measure of the distance of the current Transfer line Function to the ideal TF
 - A static parameter
 - Measure on the analog side!
 - Unity : in #LSB or in %FS

| DC ACCURACY | | | | | |
|--|------------|-------------|-------------|---------|---|
| Resolution | 12 | 12 | 12 | Bits | S, B versions, $V_{DD} = (2.35 \text{ V to } 3.6 \text{ V})^4$; A version, $V_{DD} = (2.7 \text{ V to } 3.6 \text{ V})$ |
| Integral Nonlinearity ³ | ± 1 | ± 1.5 | ± 1.5 | LSB max | |
| Differential Nonlinearity ³ | ± 0.75 | ± 0.6 | ± 0.6 | LSB typ | |
| Offset Error ³ | ± 0.75 | $-0.9/+1.5$ | $-0.9/+1.5$ | LSB max | Guaranteed no missed codes to 12 bits |
| Gain Error ³ | ± 0.5 | ± 1.5 | ± 2 | LSB typ | |
| | ± 0.5 | ± 1.5 | ± 2 | LSB max | |
| | | | | LSB typ | |

INL

- ⌘ INL values are « lower » as we choose a best fitting line !
 - Zero-based line
 - Best fitting line



INL

- ⌘ INL is the measure of the overall linearity (also called « precision »)
 - INL's profile is significative of the internal structure of the converter.
- ⌘ INL isn't always needed! (feedback loop systems)
- ⌘

INL example

⌘ AD 7687, Analog Devices

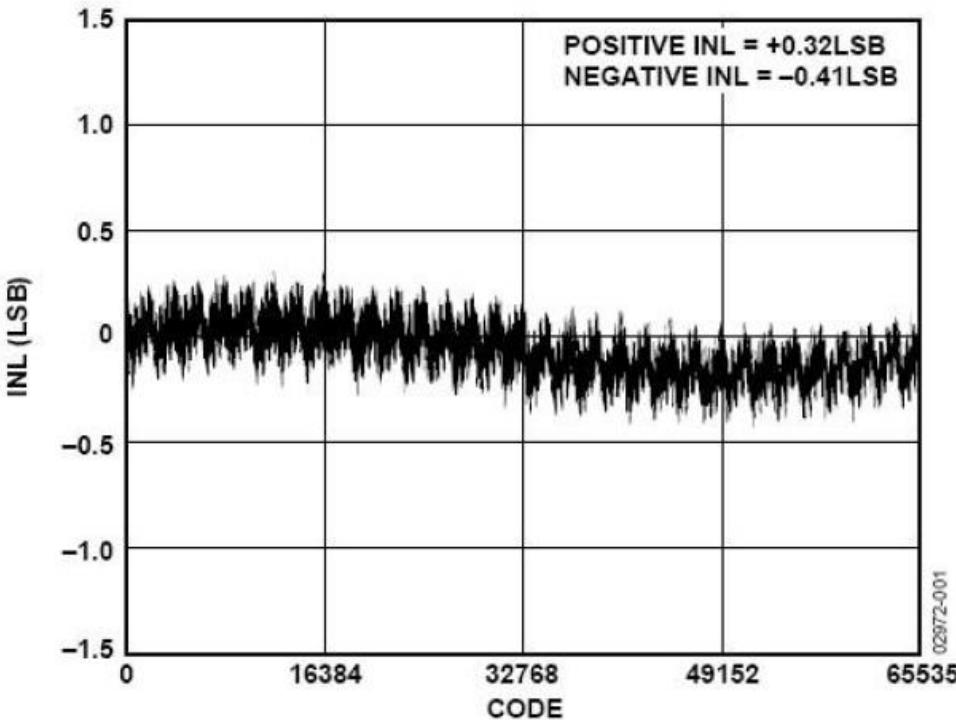


Figure 1. Integral Nonlinearity vs. Code

Def. : DNL

⌘ Differential Non-Linearity : difference of each current step value of the TF from the ideal one

- Measure on the analog side
- Unity : in #LSB or in %FS

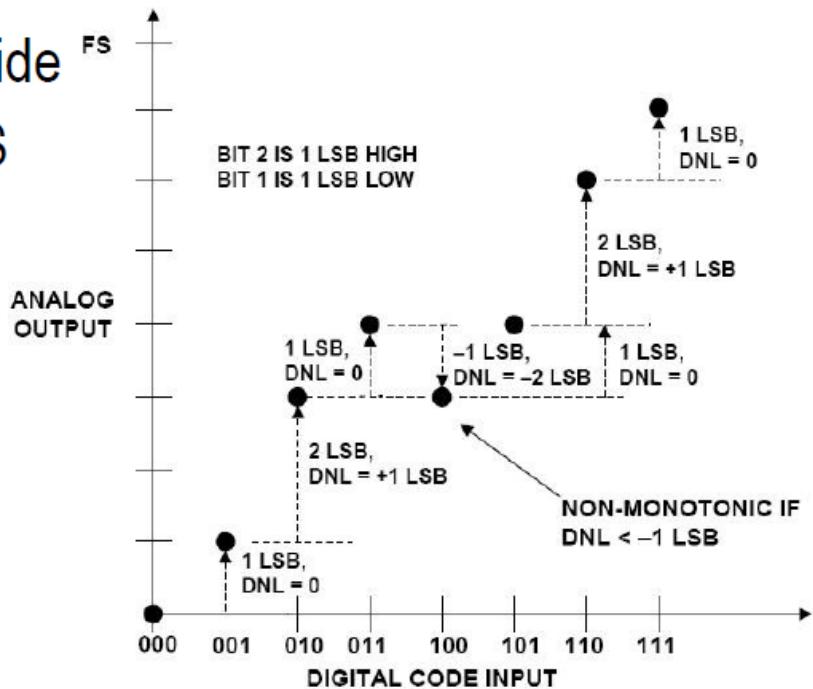
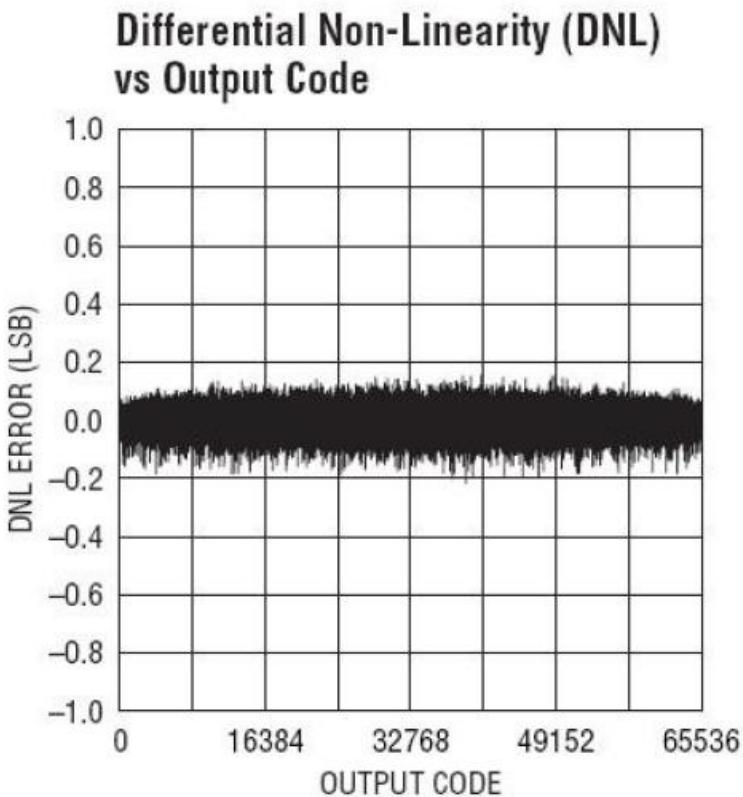
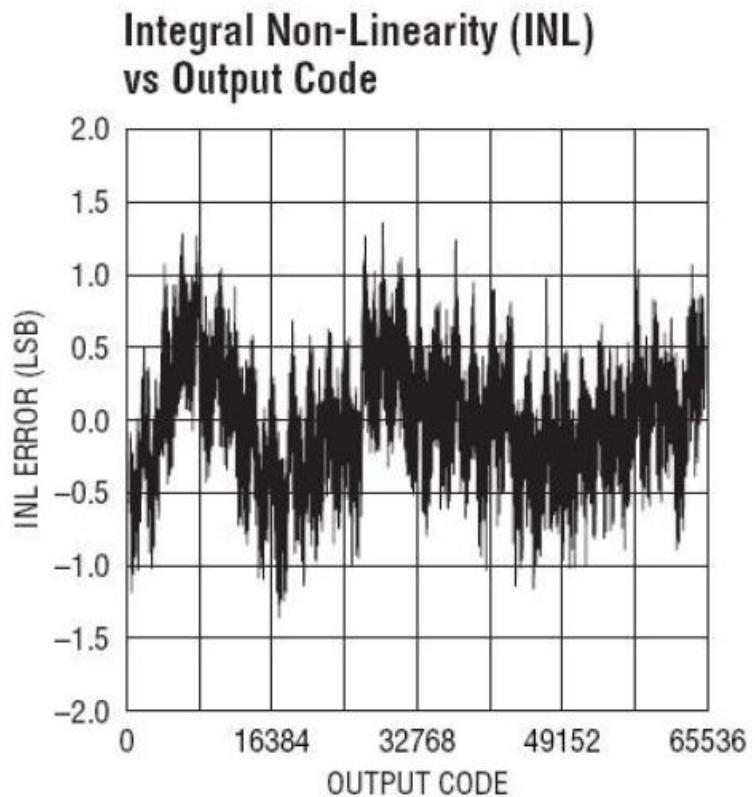


Figure 2.20: Details of DAC Differential Nonlinearity

DNL

- ⌘ DNL > -1 : non-monotonic
- ⌘ DNL > +1 : missing code
- ⌘ DNL is important for :
 - Closed loop systems
 - When small variations most significatives than big DC steps (video, graphics, sensors ...)

DNL example

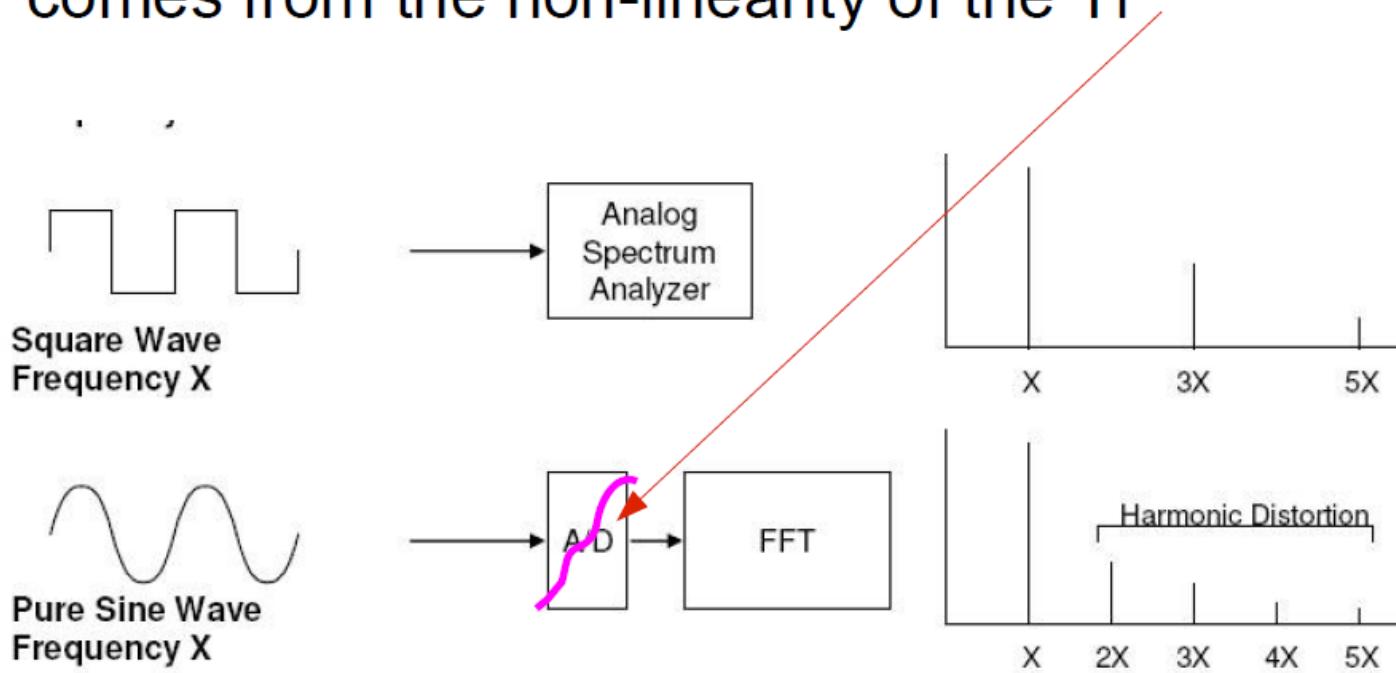


Def. : SNR

- # SNR : Signal over Noise POWER Ratio
- # SNR is one of the expression of the fundamental limitation of the converter
 - => the *SNR of the input signal* is the most useful specification for the choice of the converter's resolution
- # Unit : $\text{SNR}_{\text{dB}} = 10 \cdot \log \left(\frac{\text{signal Power } P_s}{\text{noise Power } P_N} \right)$
- # Or $\text{SNR}_{\text{dB}} = 20 \cdot \log \left(\frac{\text{signal RMS Voltage } U_s}{\text{noise RMS Voltage } U_N} \right)$

Harmonic distortion

- ⌘ 2nd order and 3rd order TF leads to distortion :
 - Pair and unpair harmonics are growing!
 - Distortion is a « dynamic » parameter but comes from the non-linearity of the TF



Total Harmonic Distortion THD

- ⌘ THD is the ratio of 2 RMS values :
 - RMS value of the fundamental sinus
 - RMS value of a given number of harmonics

$$THD = \sqrt{\frac{\sum U_{h2}^2 + U_{h3}^2 + \dots + U_{hn}^2}{U_{sin}^2}}$$

Signal-to-Noise And Distortion SINAD

- ⌘ Distance between a sinus @FS amplitude and (noise + distortion) power is called SINAD

$$\text{SINAD} = 10 \log \frac{A_{\text{SinFS}}^2}{\sum \text{(noise + distortion) power to fs/2}}$$

Effective Number Of Bits ENOB

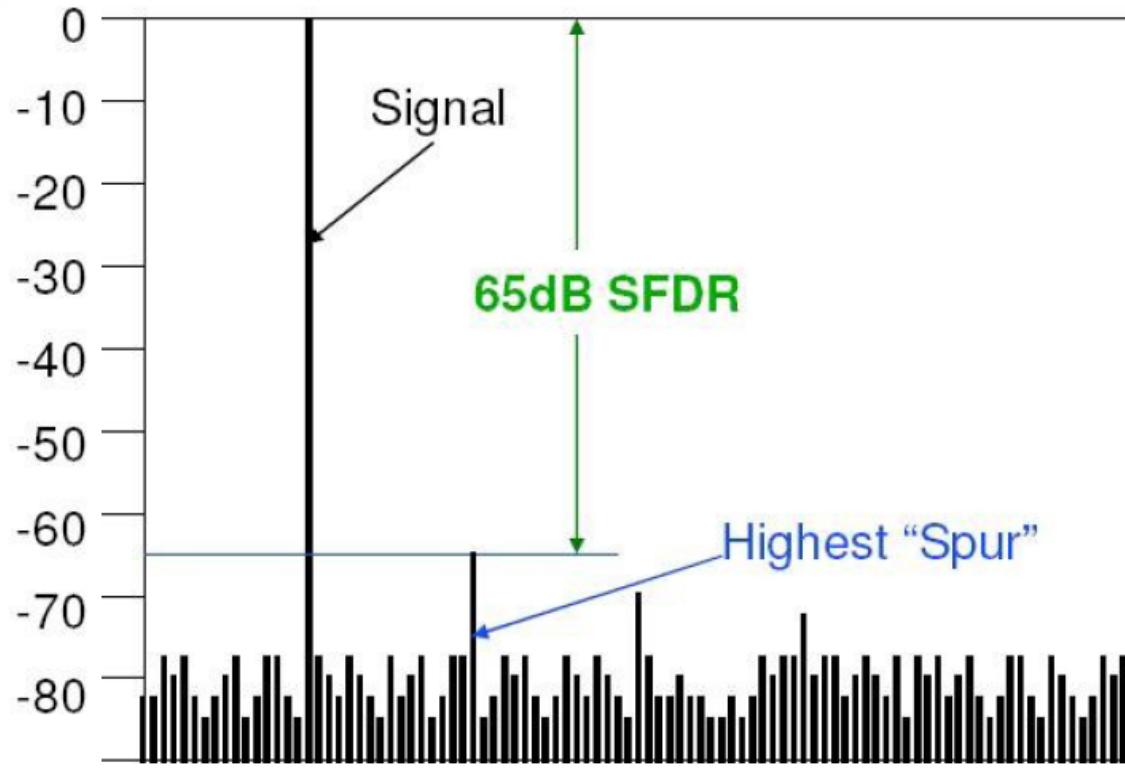


$$\text{ENOB} = \frac{\text{SINAD}_{\text{dB}} - 1.76}{6.02}$$

- ⌘ ENOB says that the ADC is equivalent to this number of bits as far as SINAD is concerned
 - That is, a converter with an ENOB of 7.0 has the same SINAD as a theoretically perfect 7-bit converter.

Spurious Free Dynamic Range SFDR

- ⌘ « Distance » to the highest distortion line



Data sheet analysis

Have a look at the following datasheets,

- DAC8411, MAX542
- AD7687, ADS5463

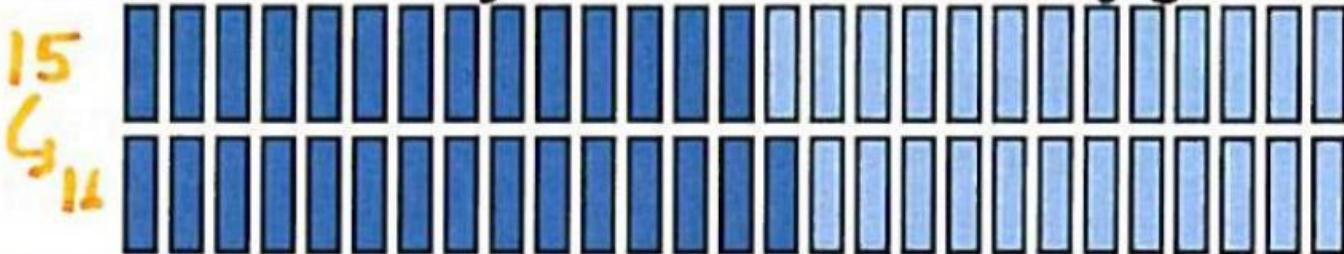
and determine the key performance characteristics: range, resolution, INL, DNL, SNR, THD, SINAD, ENOB, SFDR.

DAC Structures

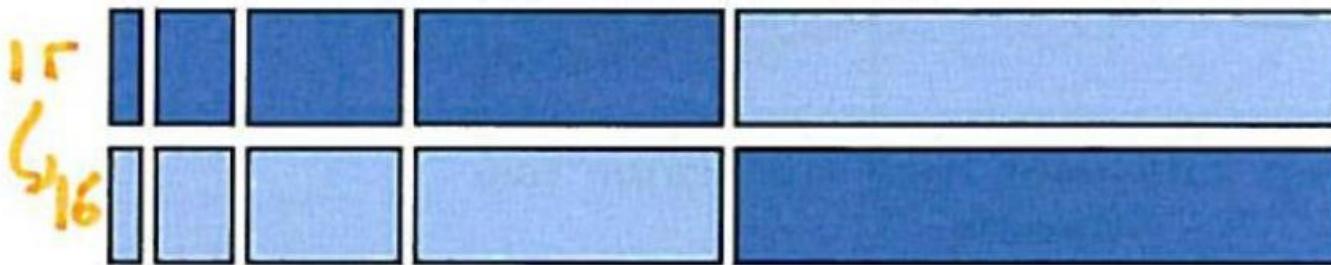
* Unary and binary types

Unary: serie of 2^N times 2^0 (LSB) values

Next value always more: monotonicity guaranteed.

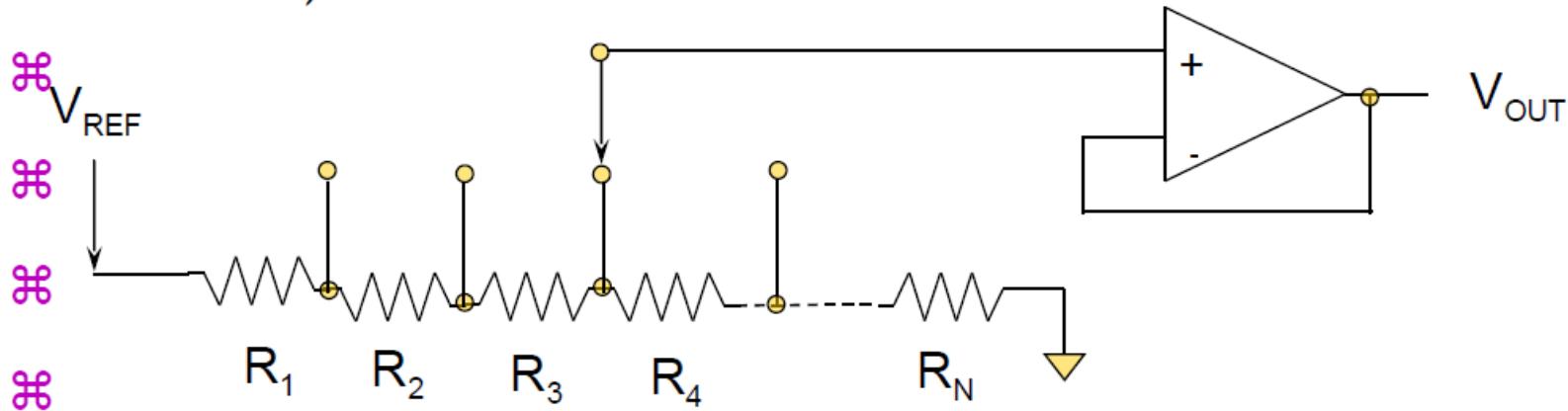


Binary: N different values: $2^0, 2^1, 2^2, 2^3, 2^4 \dots 2^{N-1}$,
small in area, MSB-transition is critical:



Unary Structures

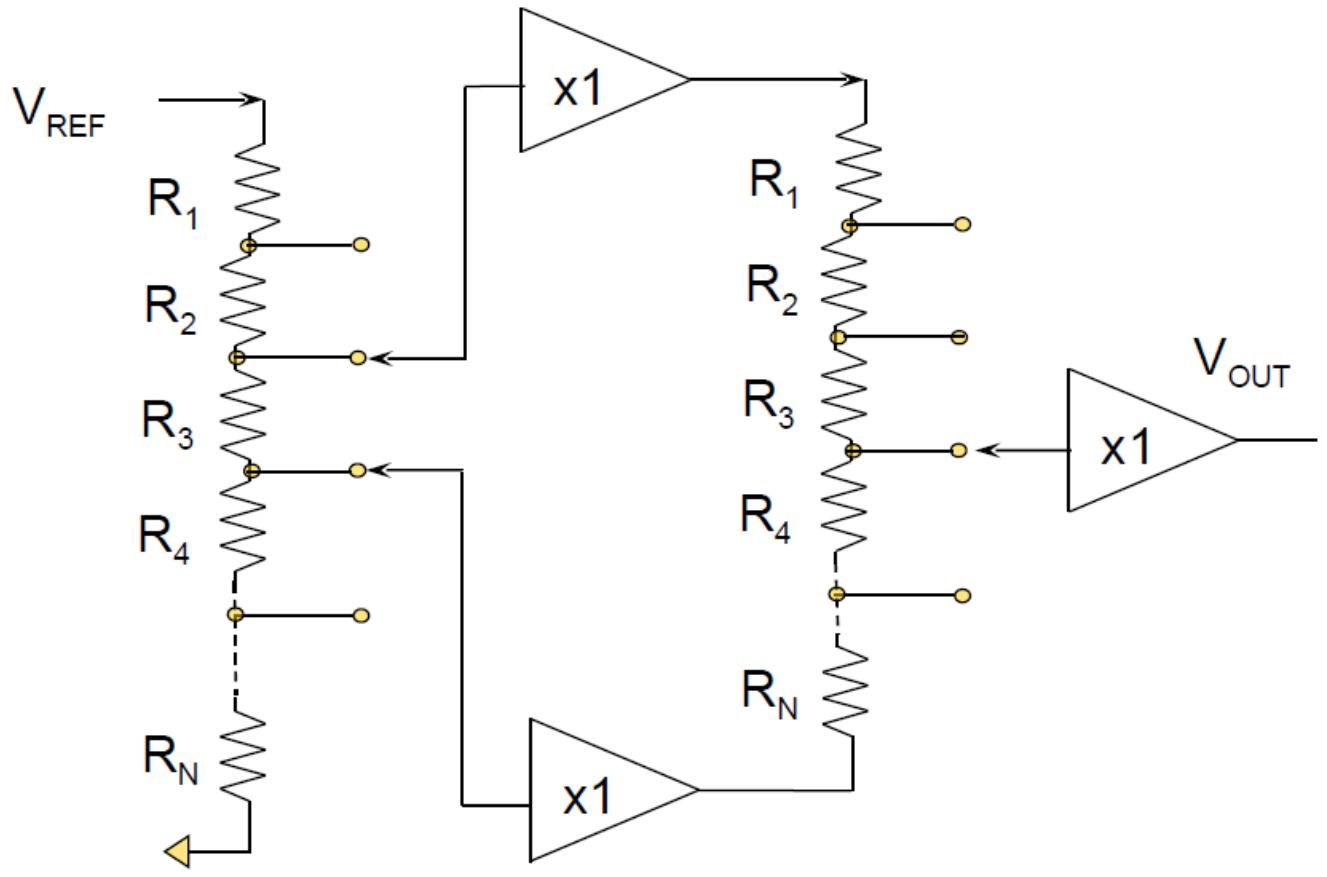
- ⌘ Simple D-A using a resistor chain (Kelvin Divider)



- Not practical for large N (2^N resistors!)
- Output is monotonic guaranteed

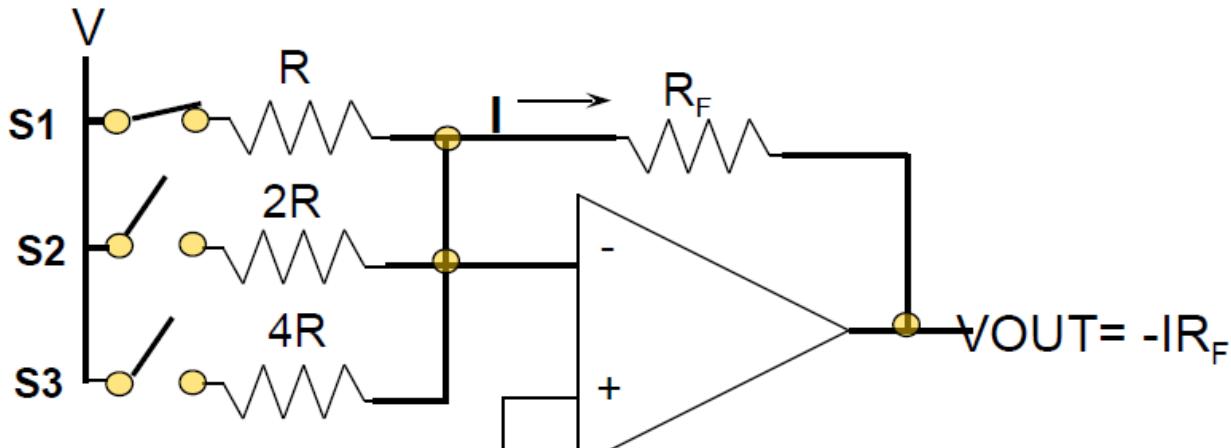
Unary Structures

⌘ Segmented chains



Binary-weighted Structure

- ⌘ A simple low-N U-DAC



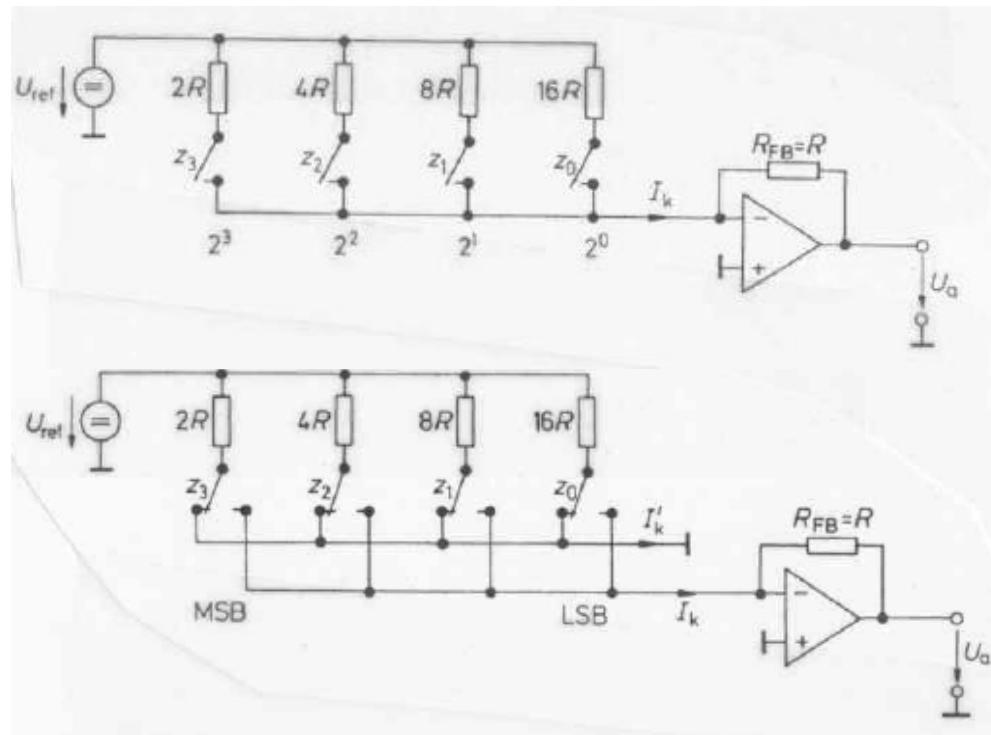
- Matching of the current sources?

Binary weighted structure

The two schematics below show binary weighted structures for DA conversion.
The principal inconvenients of the upper structure are

- The load of U_{ref} is not constant, but depends on z .
- The parasitic capacitances of the switches are (dis)charged when switching.

Explain why the lower schematic solves these problems.

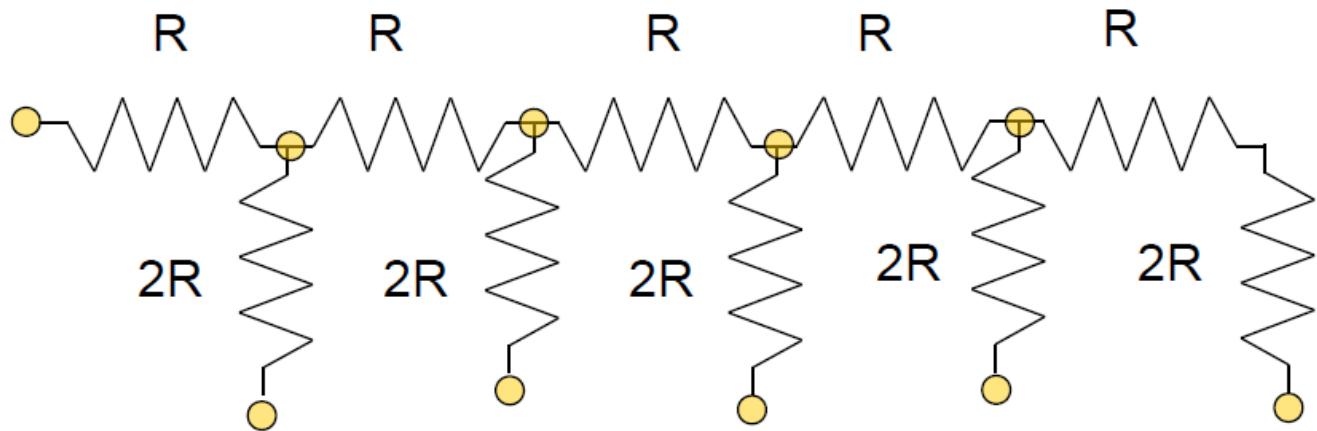


Exercice

Binary-weighted Structure

30

⌘ A simple low-N U-DAC



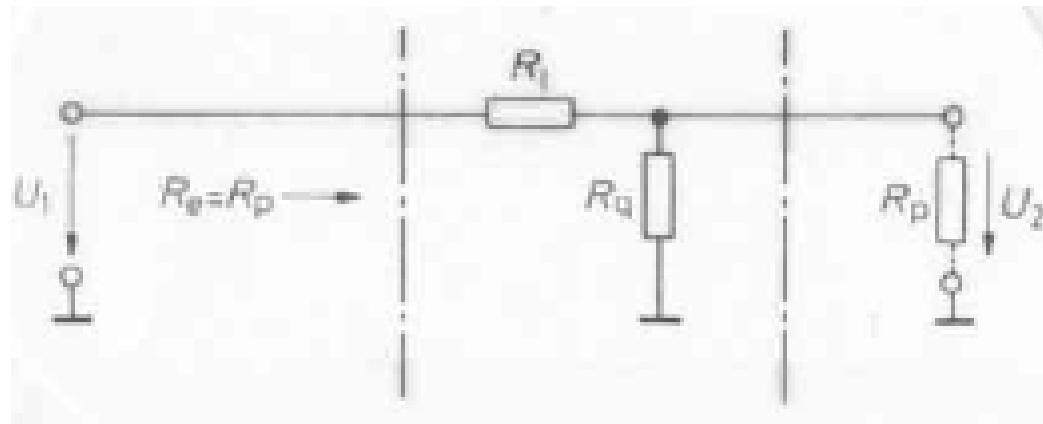
- Matching easier! (only R & 2R values)
- Absolute Value Not Important (typ. 10-20k, +/- 20%)

Generalized ladder network

Draw a schematic of a voltage output 4bit-DAC with an R/2R ladder network, using commutators between two output current rails.

With the help of the circuit shown below, express R_l and R_p as functions of R_q , so that

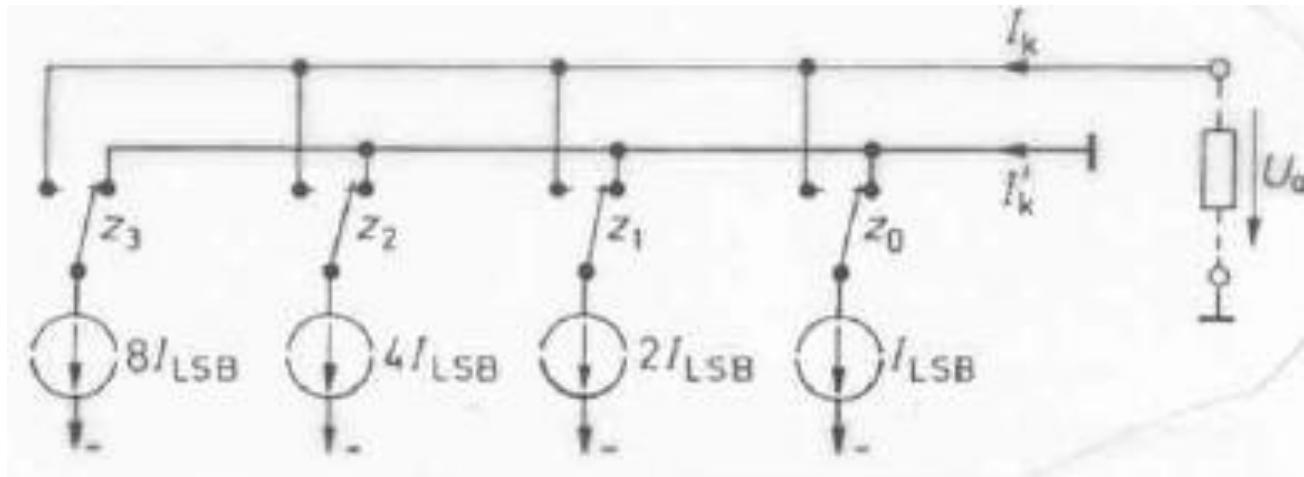
$$U_2/U_1 = \alpha$$



Exercice

Arrays of current sources

Instead of a reference voltage and a set of weighted resistors, a set of weighted current sources can be used for DA conversion as shown below.

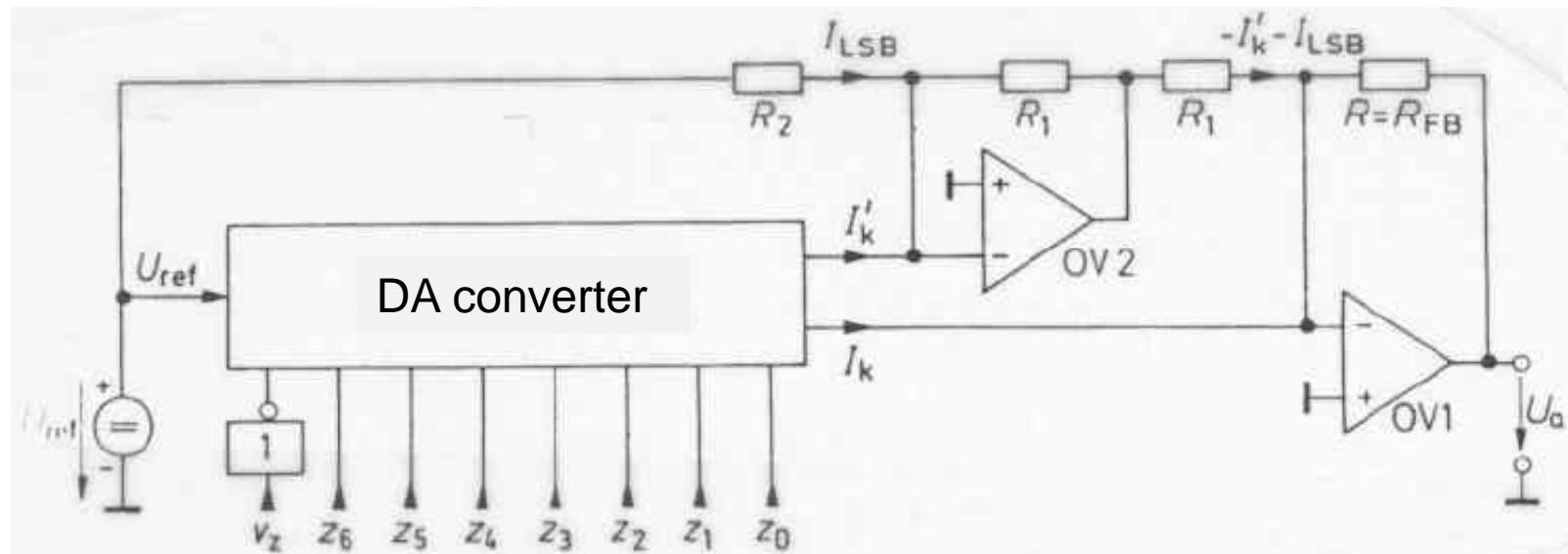


Propose an alternative circuit using a set of current sources of same value and a ladder network for DA conversion.

Exercice

Bipolar output

For the circuit shown below, determine U_a as a function of Z , a signed binary number in 2's complement representation. I_k and I_k' are the two complementary current outputs of the DA converter.

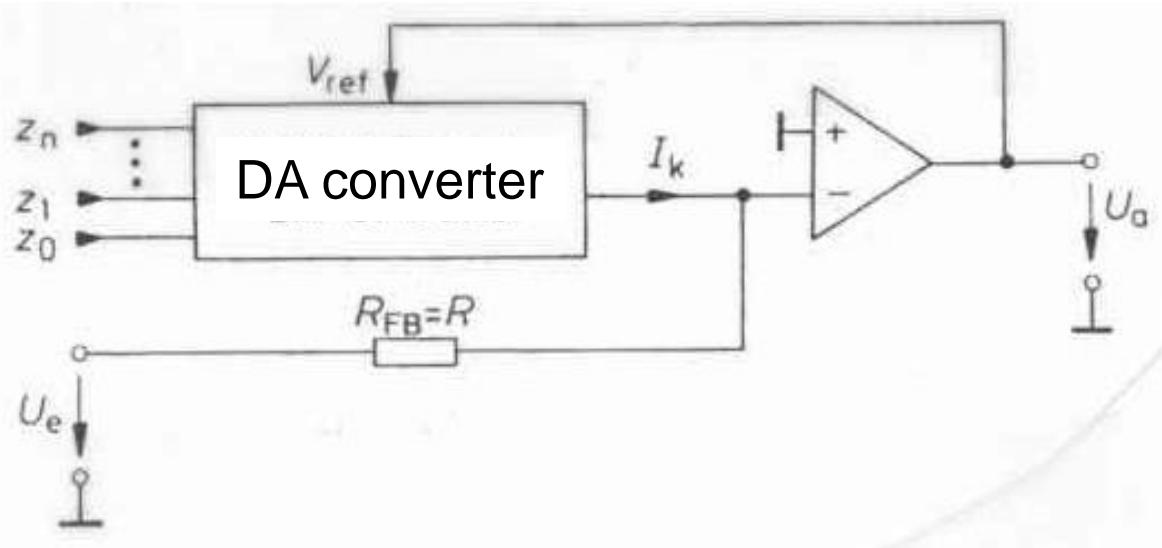


What is the range of U_a ?

Exercice

Multiplication / division

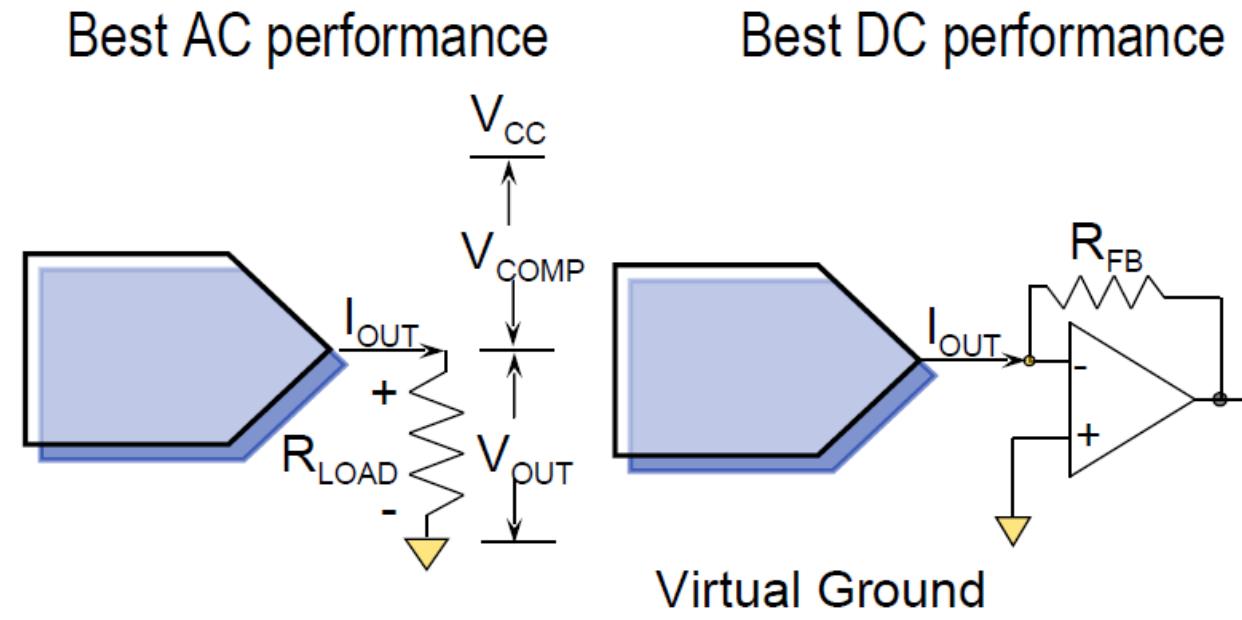
Show that in the circuit below, the output voltage U_a is proportional to U_e/Z .



Exercice

U-I output

- ⌘ Use Voltage-output DAC for DC applications,
Current-output for AC



DAC Summary

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ADC & DAC

⌘ Unary (Resistor String)

- Inherent Monotonicity
- Compact Design Leading to the basis of Multi-Channel DACs
- Difficult to get High performance INL

⌘ Binary (R-2R Ladder)

- Good DC performance
- Suffer from distributed R-C effects and signal-dependant loading in frequency-domain applications
- Multiplying Capability
- Can Operate in Voltage Mode for Single Supply Applications

DAC Summary

⌘ Bipolar Switched Current

- Suffers AC limitations because R-2R is typically required to create LSB currents

⌘ CMOS Switched Current

- Best Choice for frequency-domain applications:
- No R-2R to limit AC performance
- Good matching for DC specifications (calibration sometimes needed)
- Allows for integration with discrete signal processing blocks to ease implementation and improve performance

References

W. Kester (ed.): *Analog-Digital Conversion*, Analog Devices 2004,
ISBN 0-916550-27-3

This reference was used as a basis for the present presentation, a series of illustrations are taken from it.

The book is available for download on the moodle server.

Tietze, Schenk: *Halbleiter-Schaltungstechnik*, Springer 1999 (11th ed.), ISBN 3-540-64192-0

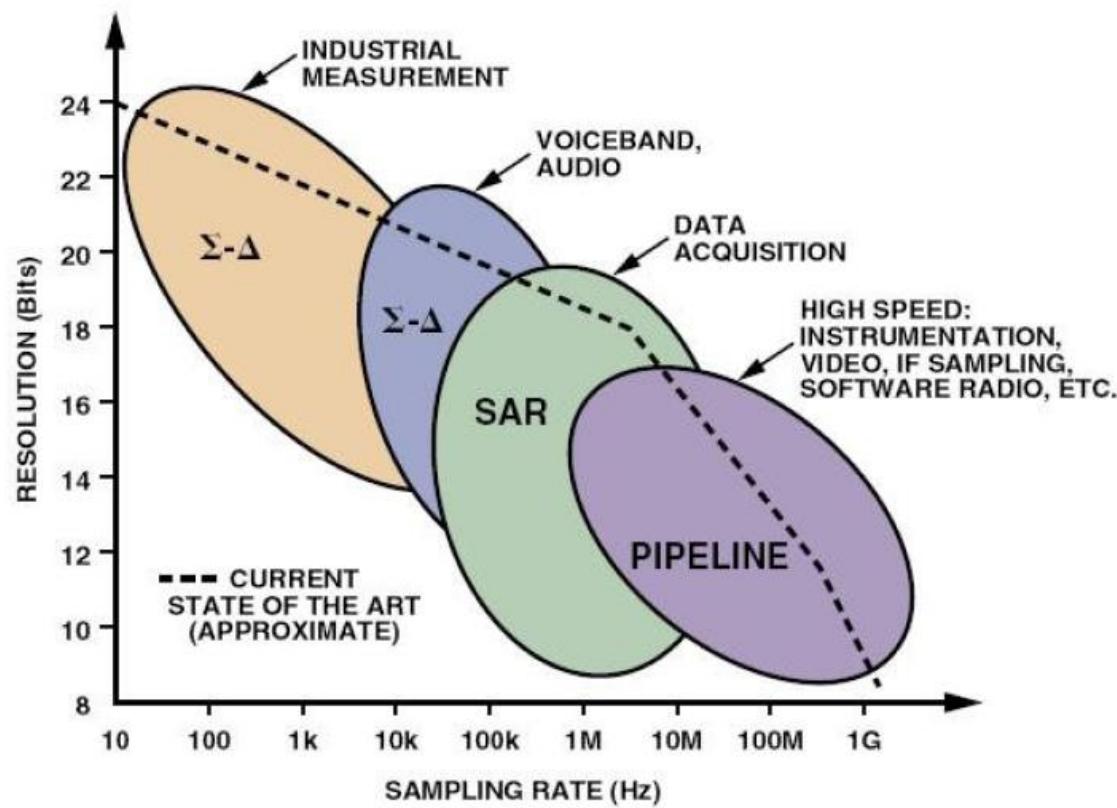
Contents

- A/D converter architectures
- Noise of A/D and D/A conversion
- Power supply
- Input filters and buffers
- Output filters and buffers

- References

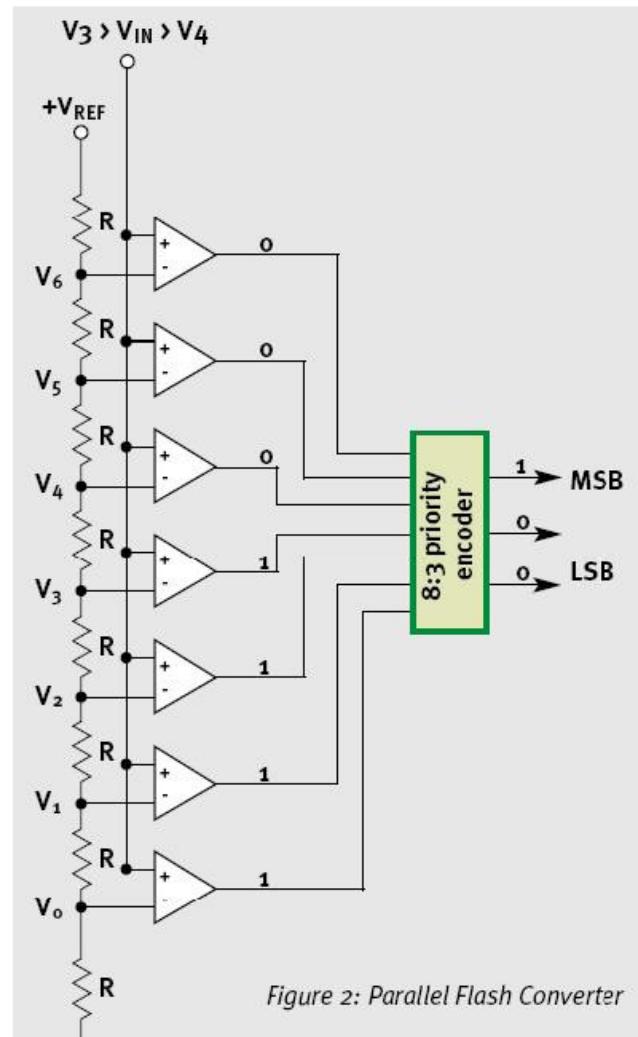
ADC Structures

⌘ Overview



Flash Converter

- ⌘ Structure :
 - 2^N Resistors
 - 2^N Comparators
 - Primary coding is like a thermometer code
 - Need a 2^N -to- N encoder

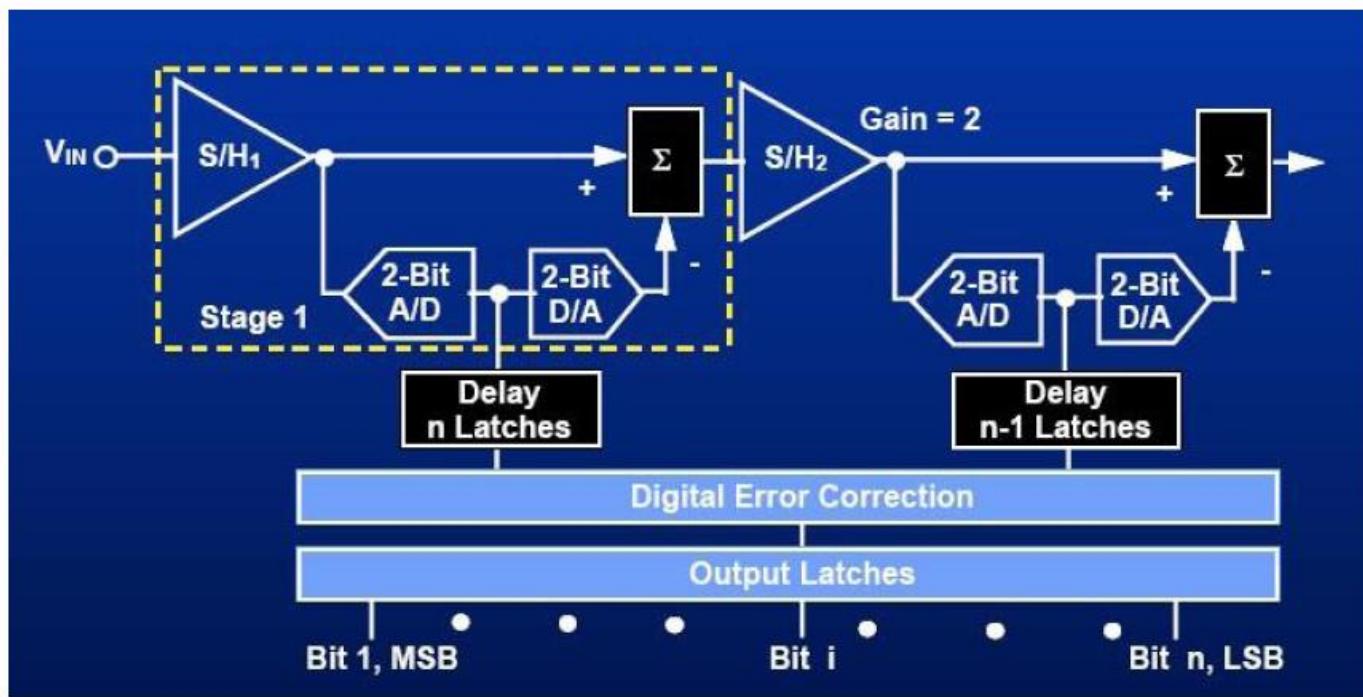


Flash Converter

- ⌘ Resolution : 6-8 bits
 - ⌘ Speed : 100M - 1G sps (one cycle for latches)
 - ⌘ Throughput : idem
 - ⌘ Power : high!
 - ⌘ Applic Domain : very fast sampling
(oscilloscopes, spectrum analyser, ...)
-
- ⌘ Flash conv don't need à S/H amplifier

Pipeline Converter

⌘ Structure



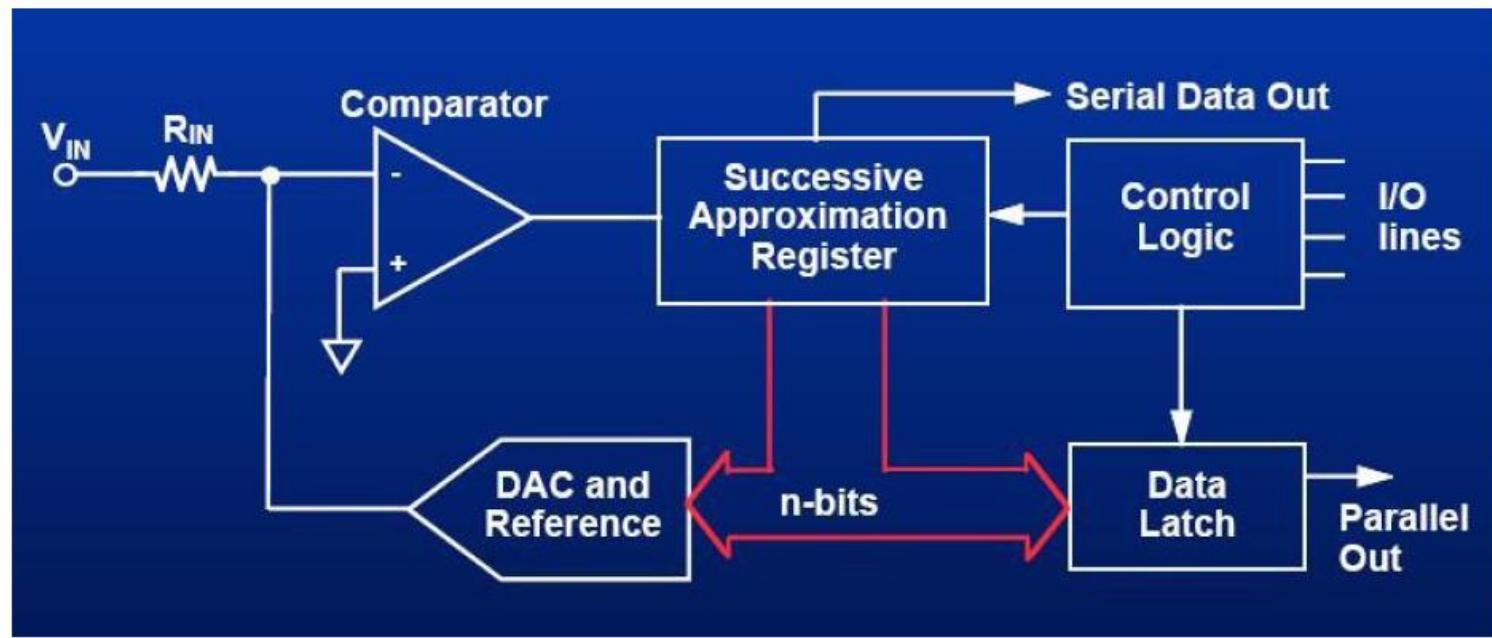
Pipeline Converter

- ⌘ Resolution : 8-12 bits
- ⌘ Speed (Latency) : 1M - 500M sps (3-4 stages X 1 clock cycle)
- ⌘ Throughput : full speed = clock cycle
- ⌘ Power : high
- ⌘ Applic Domain : high speed applic, communications

- ⌘ S/H at each stage

SAR Converter

* Structure



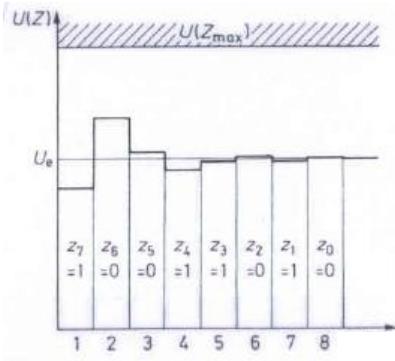
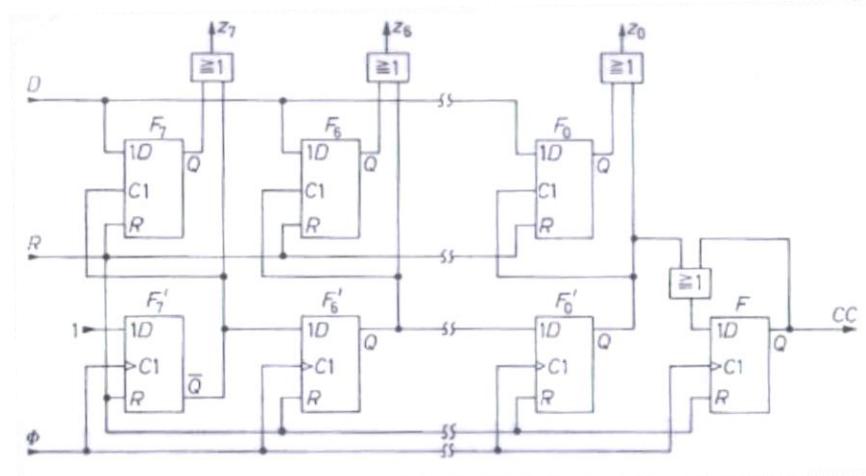
SAR Converter

- ⌘ Resolution : 8-16 bits
- ⌘ Speed (Latency) : 100k - 10M sps (~N cycles latency)
- ⌘ Throughput : 1 sample/~N clk cycles
- ⌘ Power : medium
- ⌘ Applic Domain : industrial domain, suits for multi-channel (i.e analog inputs for uC)

- ⌘ Need a S/H

Successive approximation register

The logic circuit below is a successive approximation register processing the comparator output D and generating the conversion result Z. Describe its operation in time with the help of the conversion example presented below.



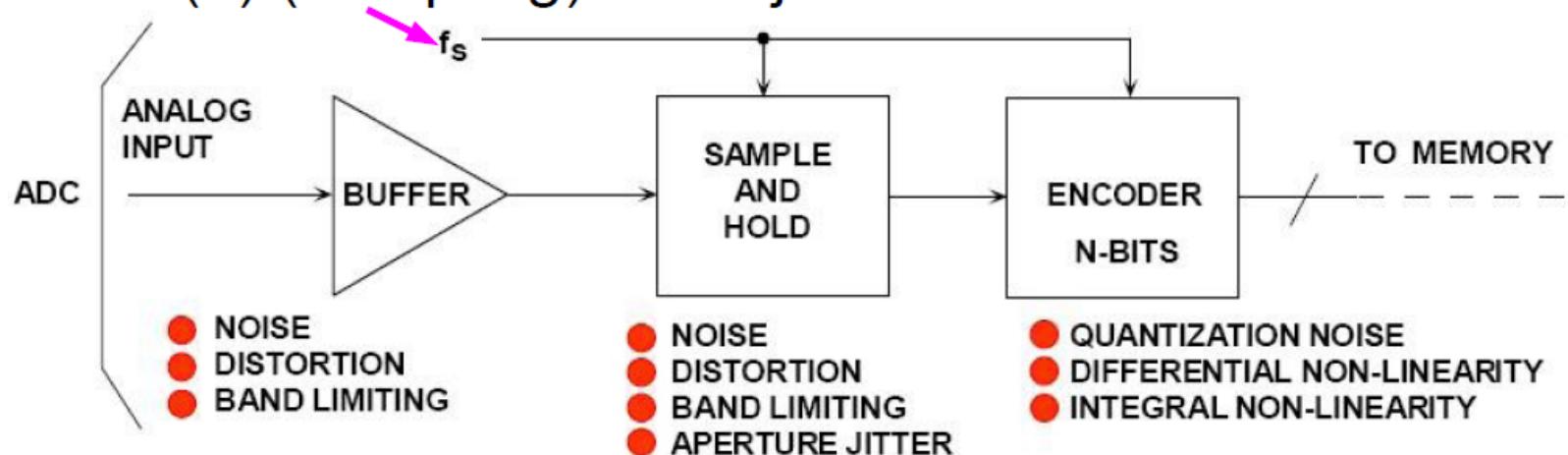
| D | Z_7 | Z_6 | Z_5 | Z_4 | Z_3 | Z_2 | Z_1 | Z_0 |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Z_7 | 1 | | | | | | | 1 |
| Z_6 | | 0 | | | | | | 0 |
| Z_5 | | | 0 | | | | | 0 |
| Z_4 | | | | 1 | | | | 1 |
| Z_3 | | | | | 1 | | | 1 |
| Z_2 | | | | | | 0 | | 0 |
| Z_1 | | | | | | | 1 | 1 |
| Z_0 | | | | | | | | 0 |

| T | R | D | Z_7 | Z_6 | Z_5 | Z_4 | Z_3 | Z_2 | Z_1 | Z_0 | CC |
|-----|-----|-------|-------|-------|-------|-------|-------|-------|-------|-------|----|
| 0 | 1 | D_7 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | D_7 | D_7 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 | D_6 | D_7 | D_6 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | 0 | D_5 | D_7 | D_6 | D_5 | 1 | 0 | 0 | 0 | 0 | 0 |
| 4 | 0 | D_4 | D_7 | D_6 | D_5 | D_4 | 1 | 0 | 0 | 0 | 0 |
| 5 | 0 | D_3 | D_7 | D_6 | D_5 | D_4 | D_3 | 1 | 0 | 0 | 0 |
| 6 | 0 | D_2 | D_7 | D_6 | D_5 | D_4 | D_3 | D_2 | 1 | 0 | 0 |
| 7 | 0 | D_1 | D_7 | D_6 | D_5 | D_4 | D_3 | D_2 | D_1 | 1 | 0 |
| 8 | 0 | D_0 | D_7 | D_6 | D_5 | D_4 | D_3 | D_2 | D_1 | D_0 | 1 |

Noise sources (1)

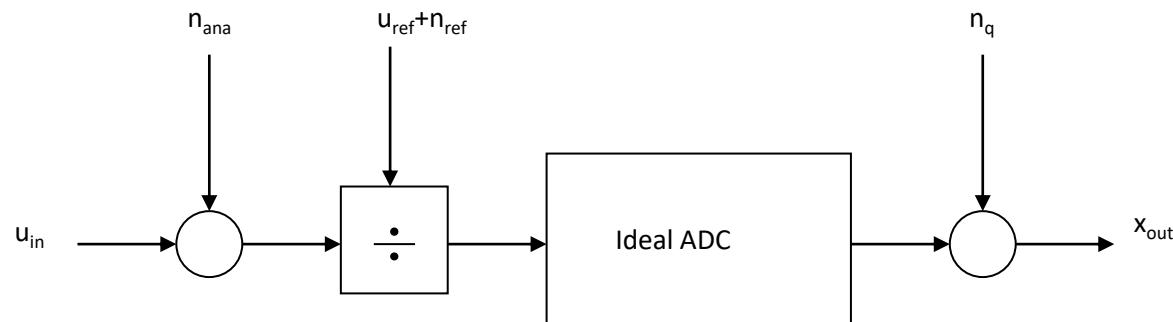
* In an A/D converter, noise comes from many sources:

- (1) quantization noise, (see last week)
- (2) noise generated by the converter itself,
- (3) application circuit noise (**Reference & Power Supply**, **GND** bounce, **LAYOUT** consideration)
- (4) (sampling) clock jitter.



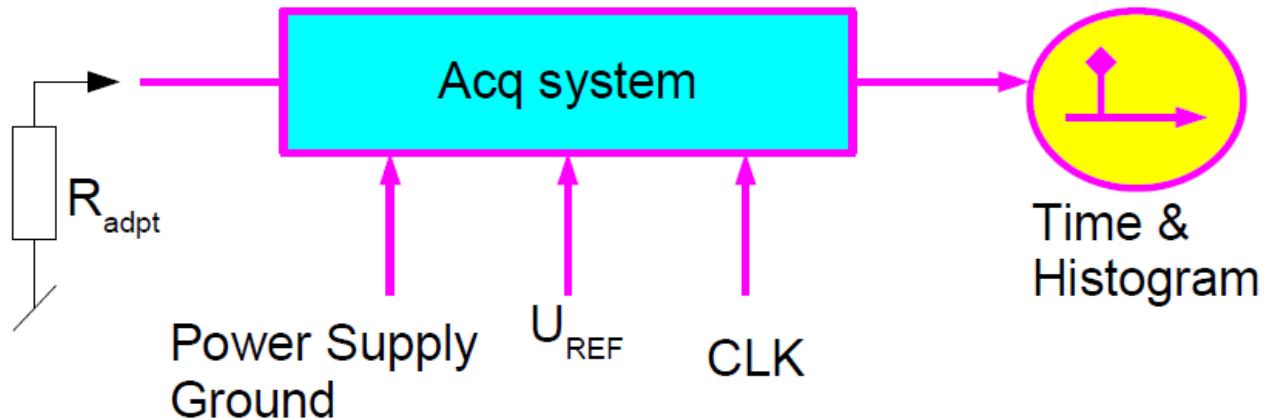
Noise sources (2)

- Analog input circuit noise is *additive*.
- Voltage reference noise is *multiplicative*.
- Quantisation noise is *additive*.



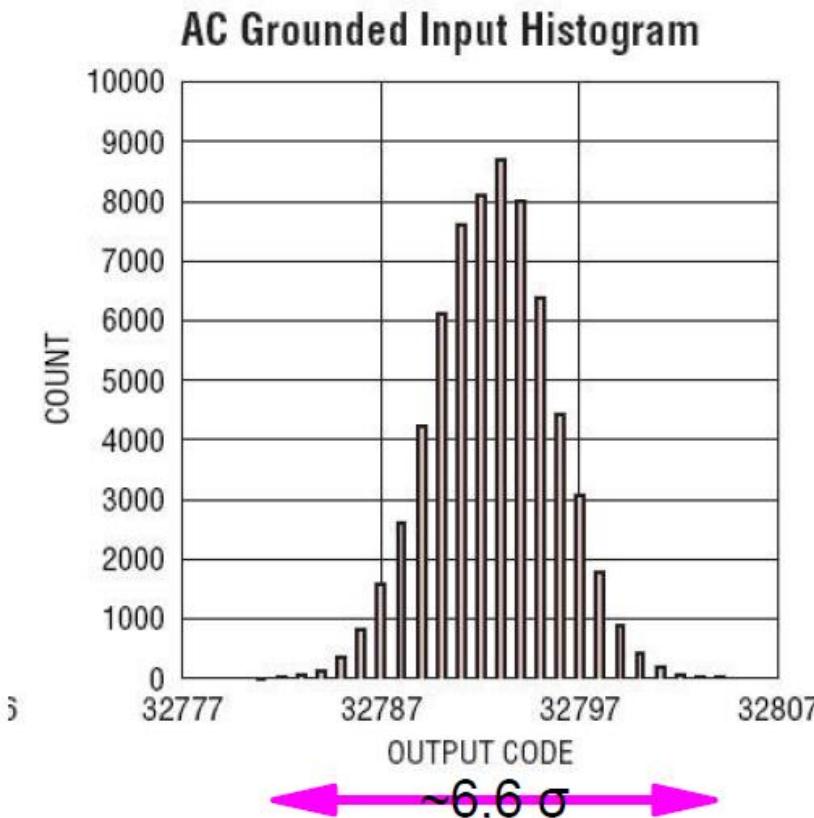
Noise sources (3)

- ⌘ Noise sources have to be decorrelated: White noise can be assumed only in this case.
- ⌘ Many noise are correlated => very difficult to predict the effective behaviour !
- ⌘ Make this test !



Zero Volt test

⌘ AD2274:



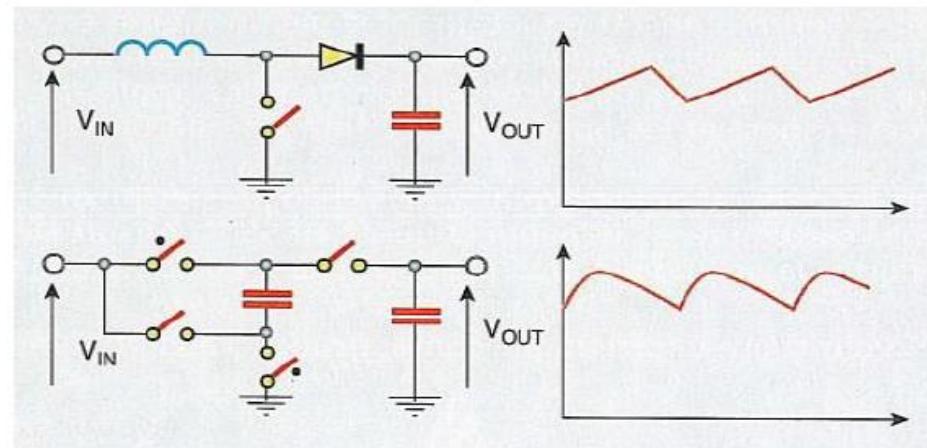
- Evaluate the RMS value of Noise. ($\sigma \approx$)

Voltage reference

- ⌘ Stability of the REFERENCE is crucial for best performance of the Converter.
 - While these voltages appear static, they could be dynamically used in the ADC system.
 - During every conversion the voltages on these pins are sampled and must settle within a fraction of the ADC clock rate, for example.
- ⌘ Ref Voltage Sources are never good enough !
 - They introduces NOISE in the system
 - Quality of the DECOUPLING on the PCB

Power supply

- ⌘ If $\pm 15V$ power supply available, use them!
 - Design much easier (Low-noise amp, mature technologies, availability of the components...)
- ⌘ But portable equipment have only one battery (e.g. 2.7V)
 - => DC/DC boost needed, but Analog circuits don't like it !



Power supply rejection

- ⌘ How much tolerant are ADC to supplies

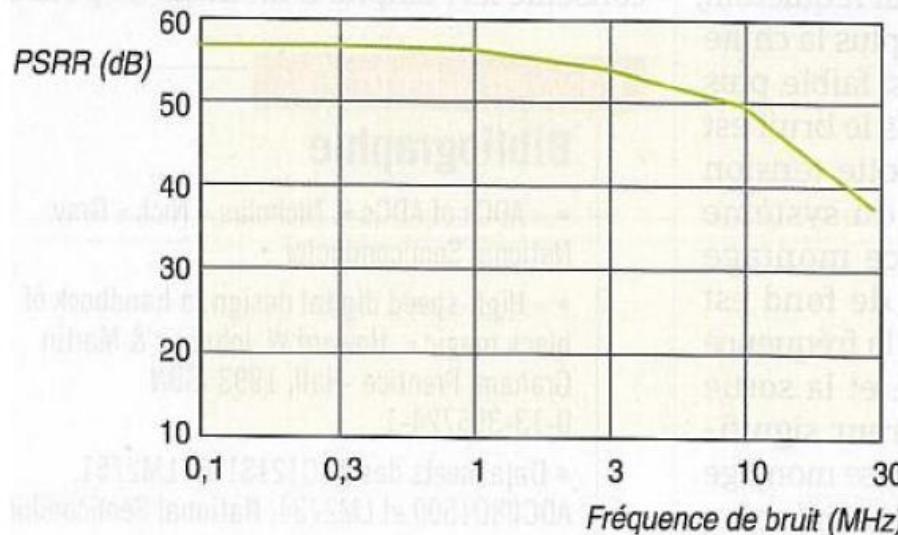
- ⌘ Ideal:

| PSRR | Power-supply rejection ratio | Without 0.1- μ F board supply capacitors, with 100-kHz supply noise | --- | --- | --- | dB |
|------|---------------------------------|---|-----|-----|-----|----|
| | | | 85 | 85 | 85 | |

Taux de réjection de l'alimentation du CAN 12 bits ADC12040.

Pour ce faire, un bruit d'amplitude 200mV est injecté dans
l'alimentation à différentes fréquences.

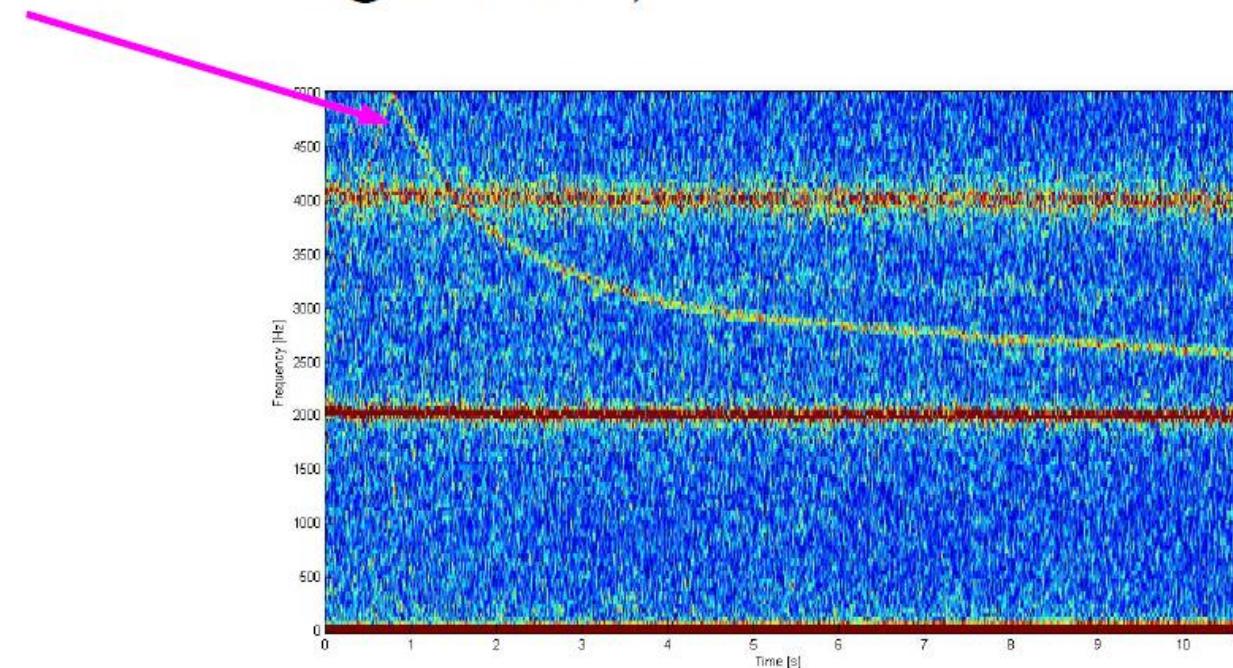
- ⌘ Reality:



- Modern DC/DC switching freq : [500k ... 2MHz]

Power supply scheme (1)

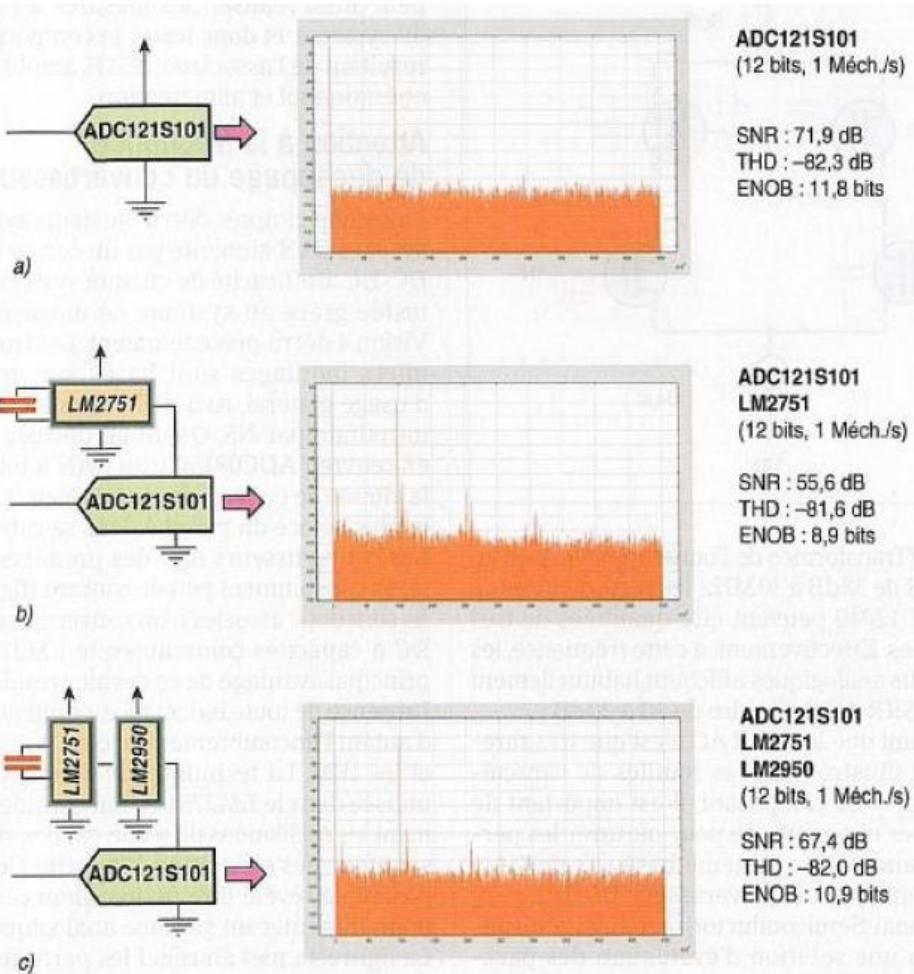
- ⌘ Synchronize DC/DC regulator to the master sampling clock to avoid this (Input grounded test; no LDO after DC/DC regulators):



Power supply scheme (2)

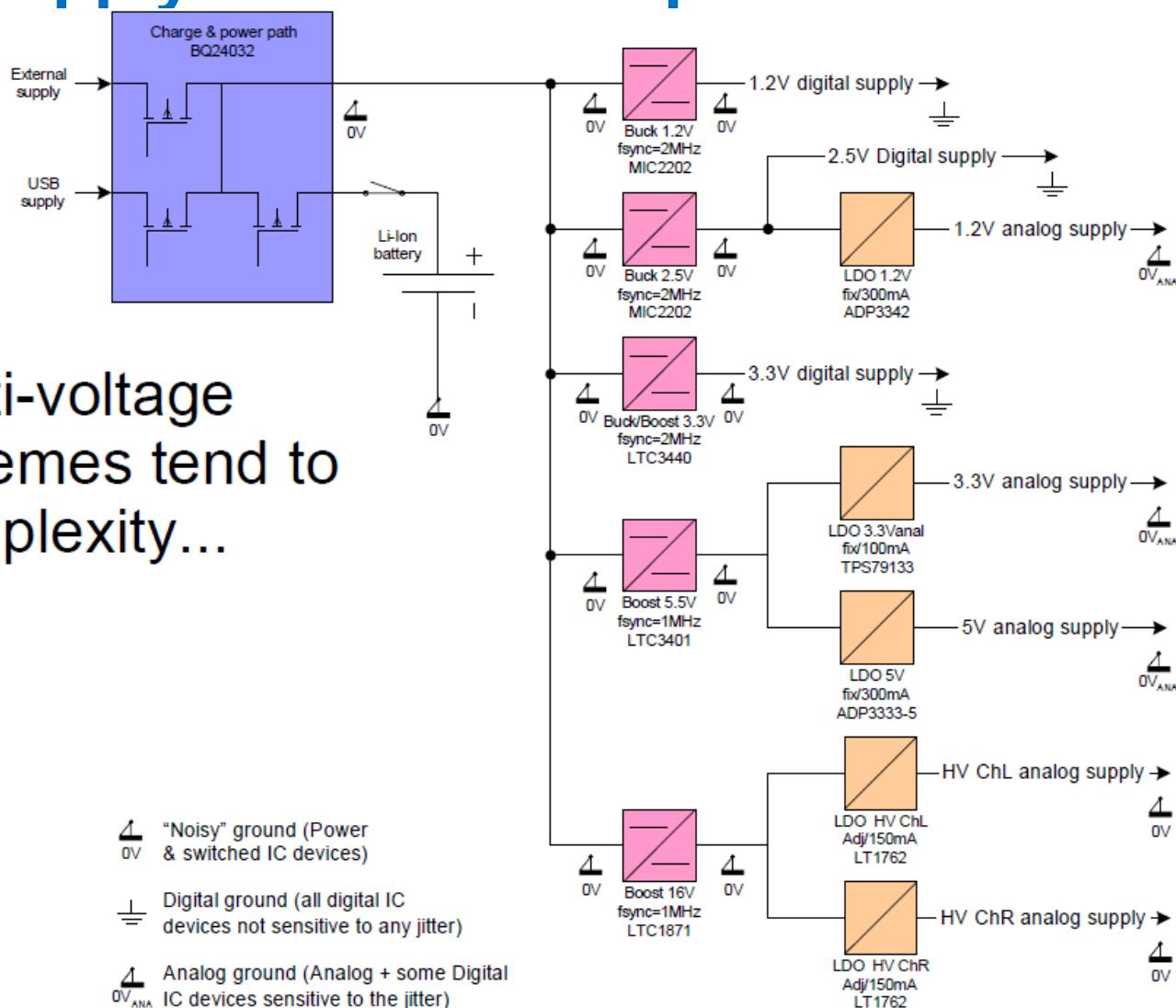
⌘ Analog Power Supply needs LDO !

- 8-10 bits not dramatic
- 12 bits & + : very important



Power supply scheme example

- Multi-voltage schemes tend to complexity...



Input matching (1)

- ⌘ Determine the Nyquist freq and choose an ideal sample frequency. ($1.2 \dots 2 f_{NYQ}$)
- ⌘ Evaluate the feasibility of an Over- / Undersampling process.
 - First selection of the ADC's family
- ⌘ Evaluate the needs & specifications of an antialiasing filter (passive - active, corner freq, order...)
- ⌘ Evaluate the needs & specifications of the voltage matching (attenuator, amplifier, level-shifter,...)

Input matching (2)

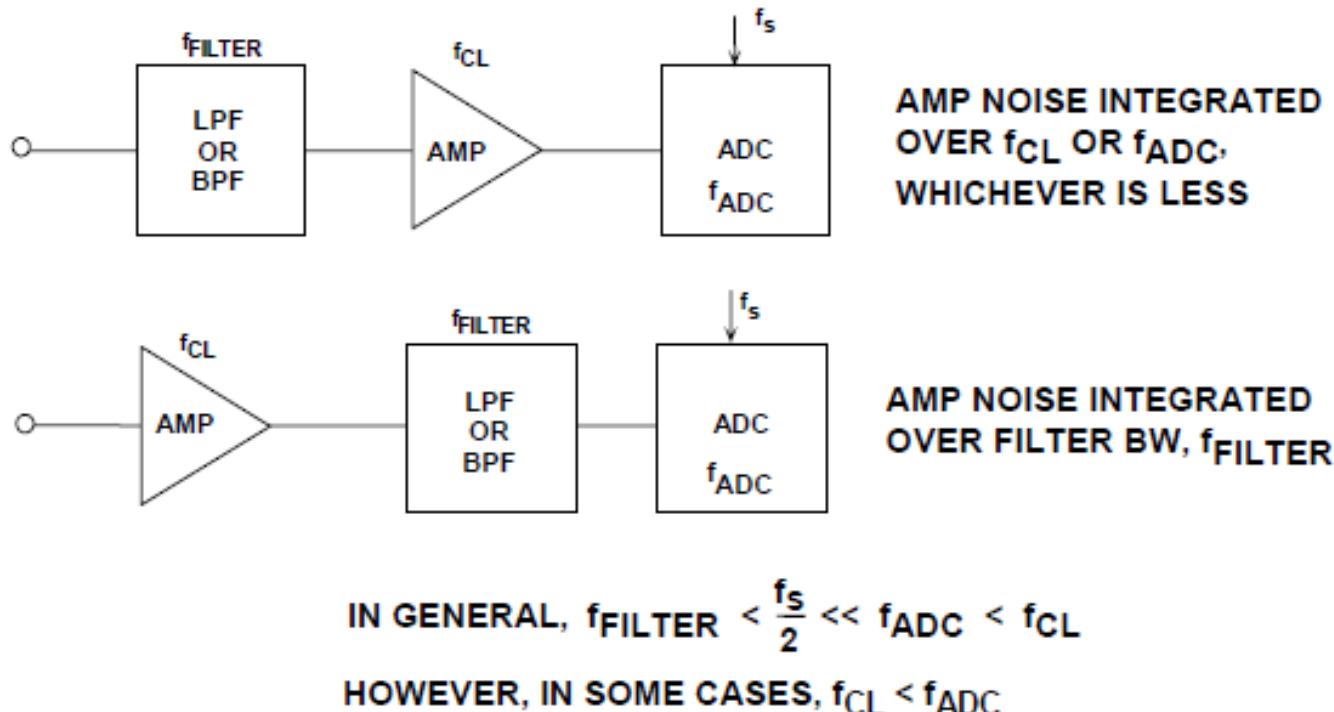


Figure 6.39: Proper Positioning of the Antialiasing Filter Will Reduce the Effects of Op Amp Noise

Single ended and common mode adaptation

⌘ Modern ADC are single supply

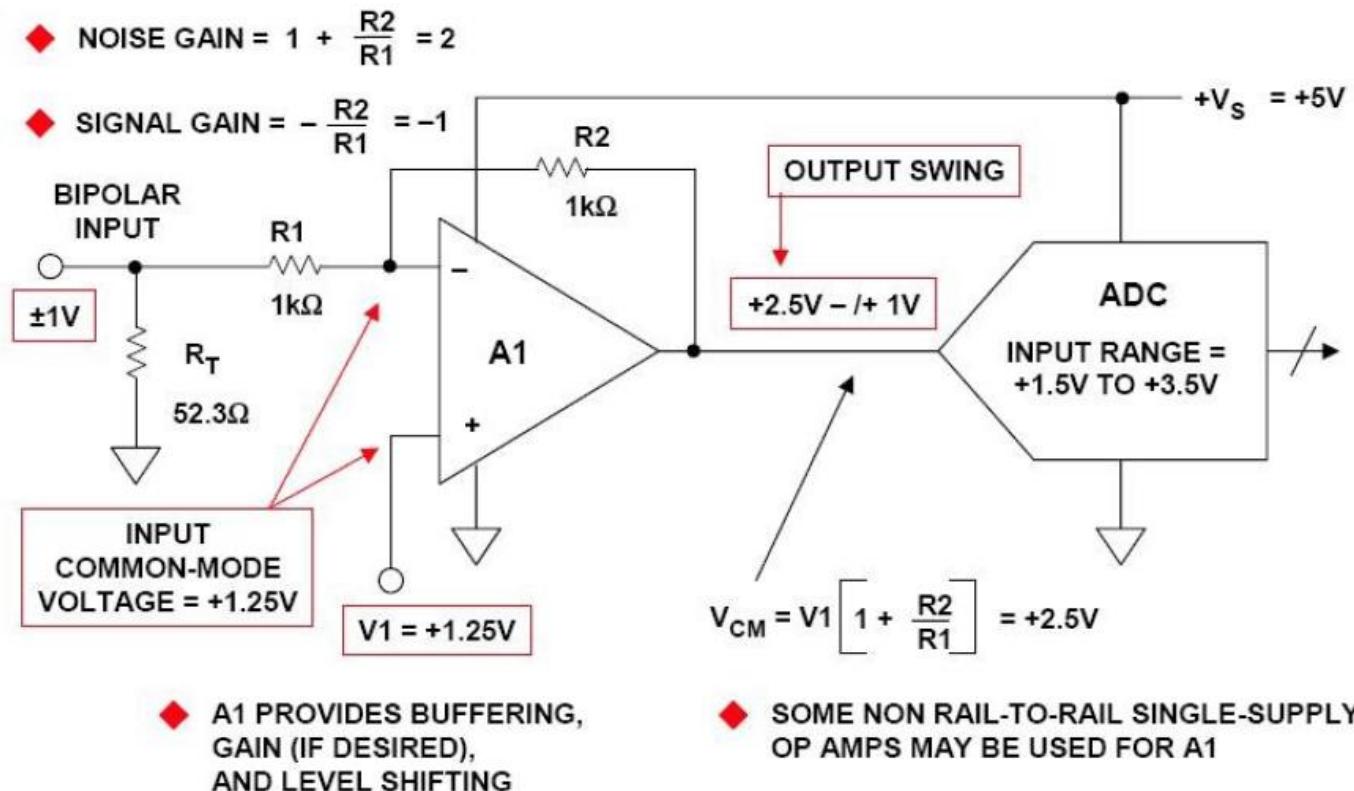


Figure 6.11: Single-Ended Single-Supply DC-Coupled Level Shifter

Single ended to differential (AC) conversion

⌘ Transformer suits HF

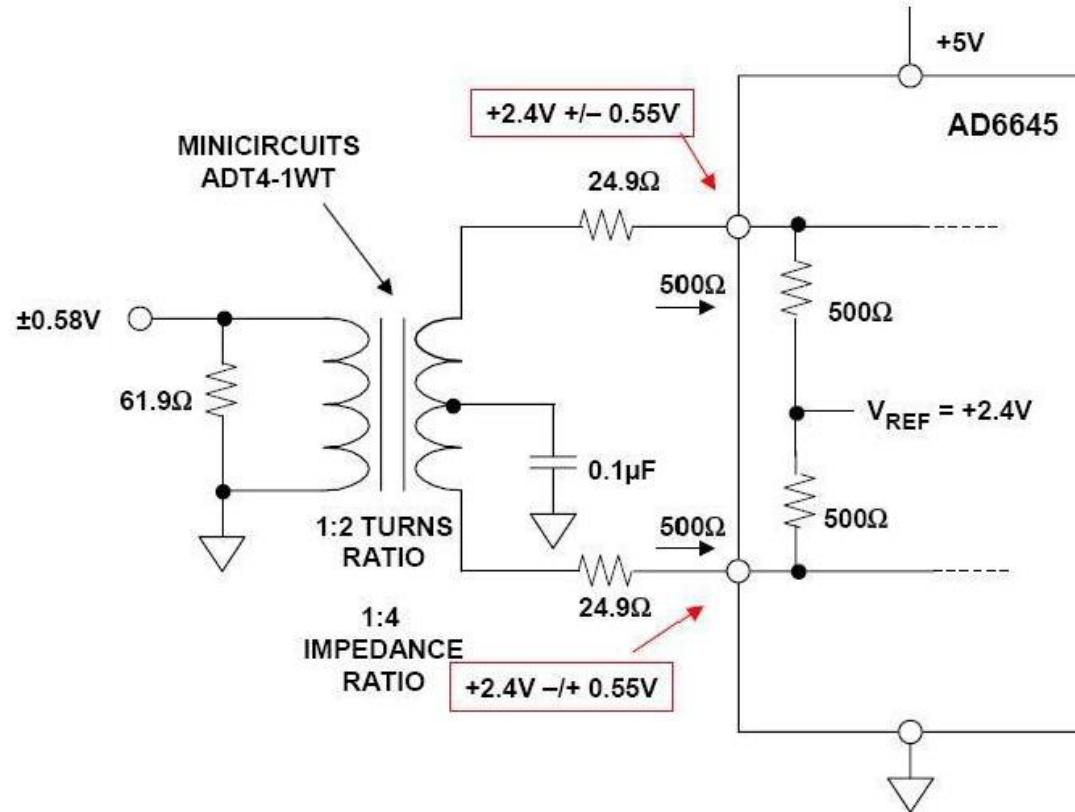


Figure 6.29: Transformer Coupling into the AD6645 14-Bit, 80-/105-MSPS Complementary Bipolar Process ADC

Single ended to differential (DC) conversion

⌘ AO: high BW, high slew-rate, low-noise ...

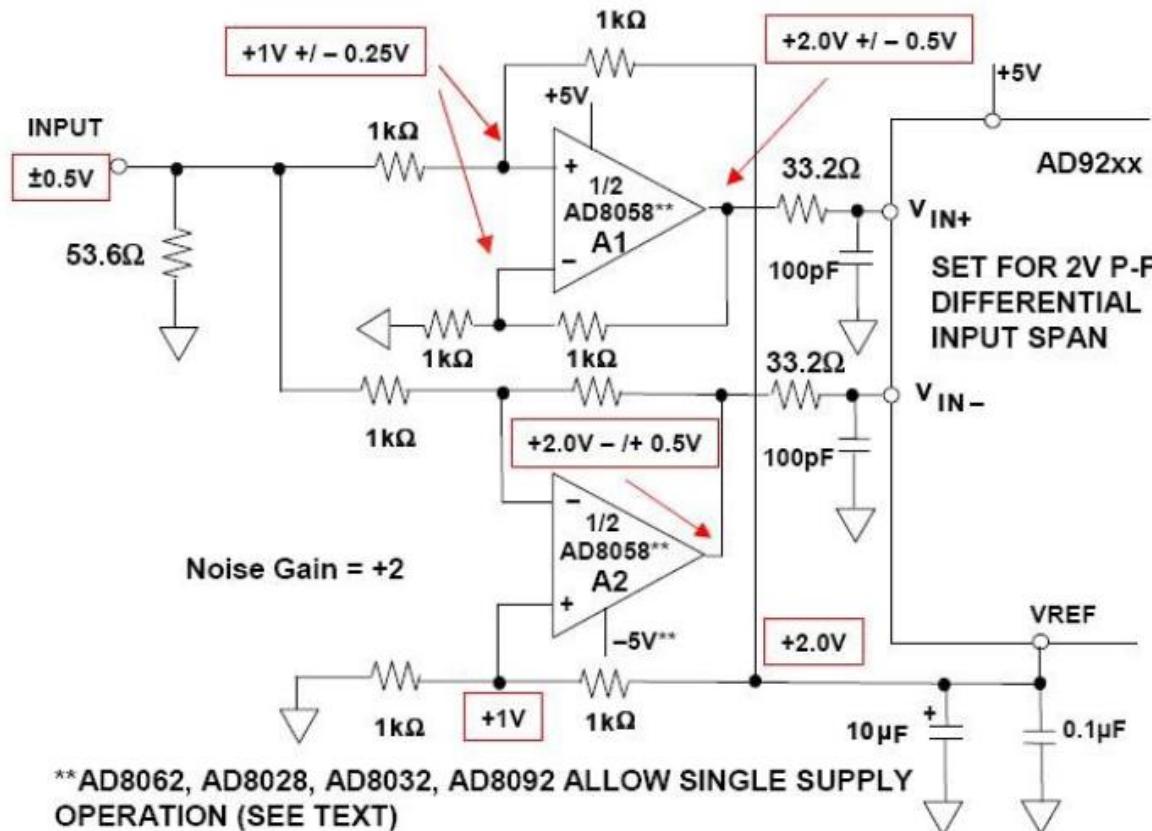
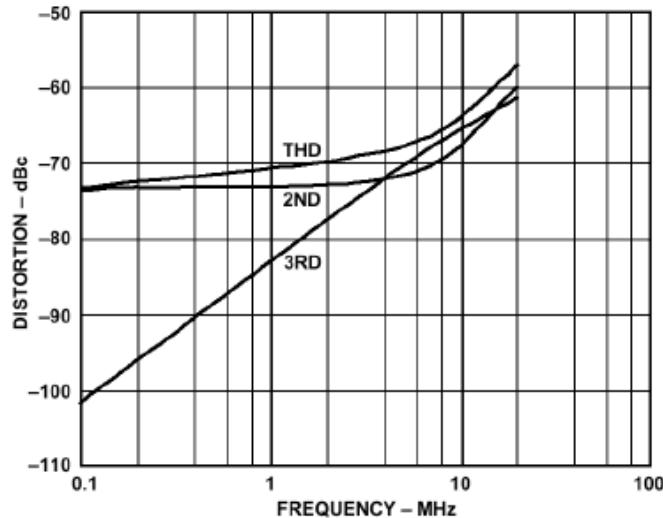
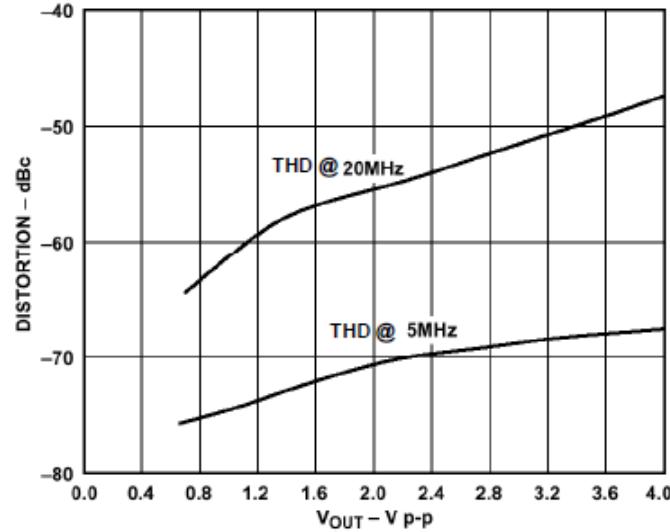


Figure 6.31: Op Amp Single-Ended to Differential DC-Coupled Driver with Level Shifting

Example for buffer distortion performance



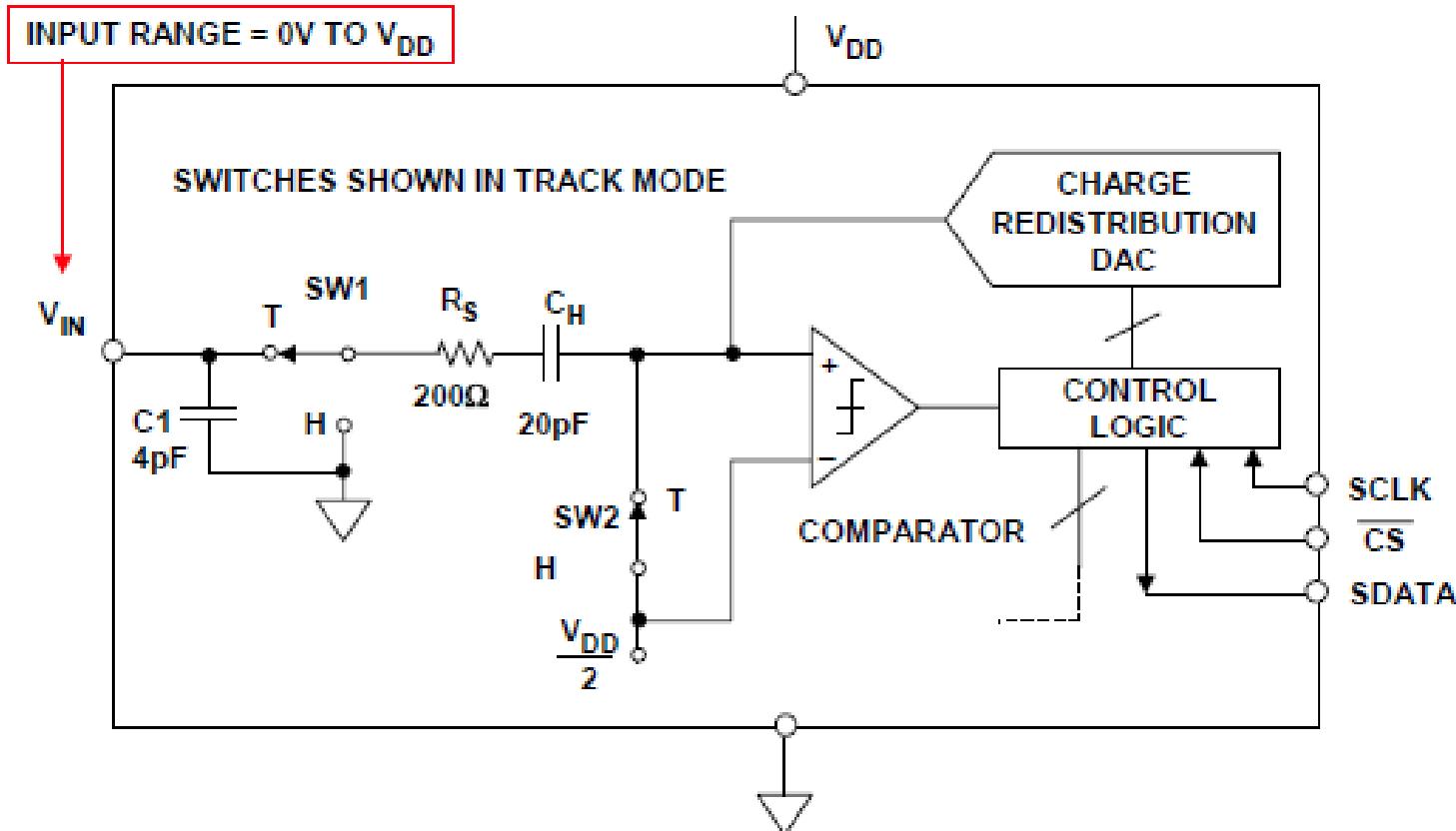
AD8057/AD8058 Op Amp Distortion Versus Frequency
 $G = +1, R_L = 150 \Omega, V_S = \pm 5 V$



AD8057/AD8058 Op Amp Distortion Versus Output Voltage
 $G = +1, R_L = 150 \Omega, V_S = \pm 5 V$

- Beware of distortion increase at high frequencies
- Performance may be better for higher load resistance

SAR ADC input characteristics



- Example: AD7466

Single supply SAR ADC with bipolar input

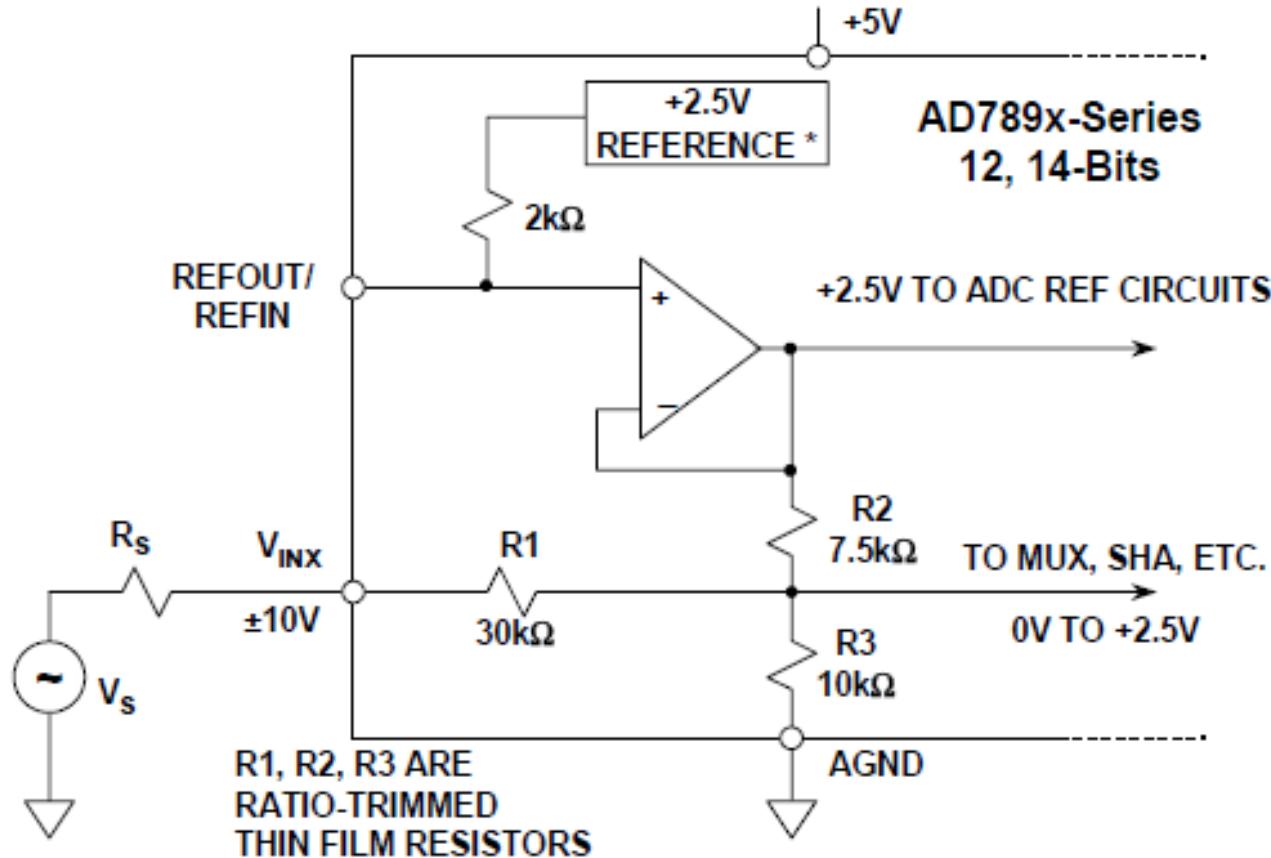
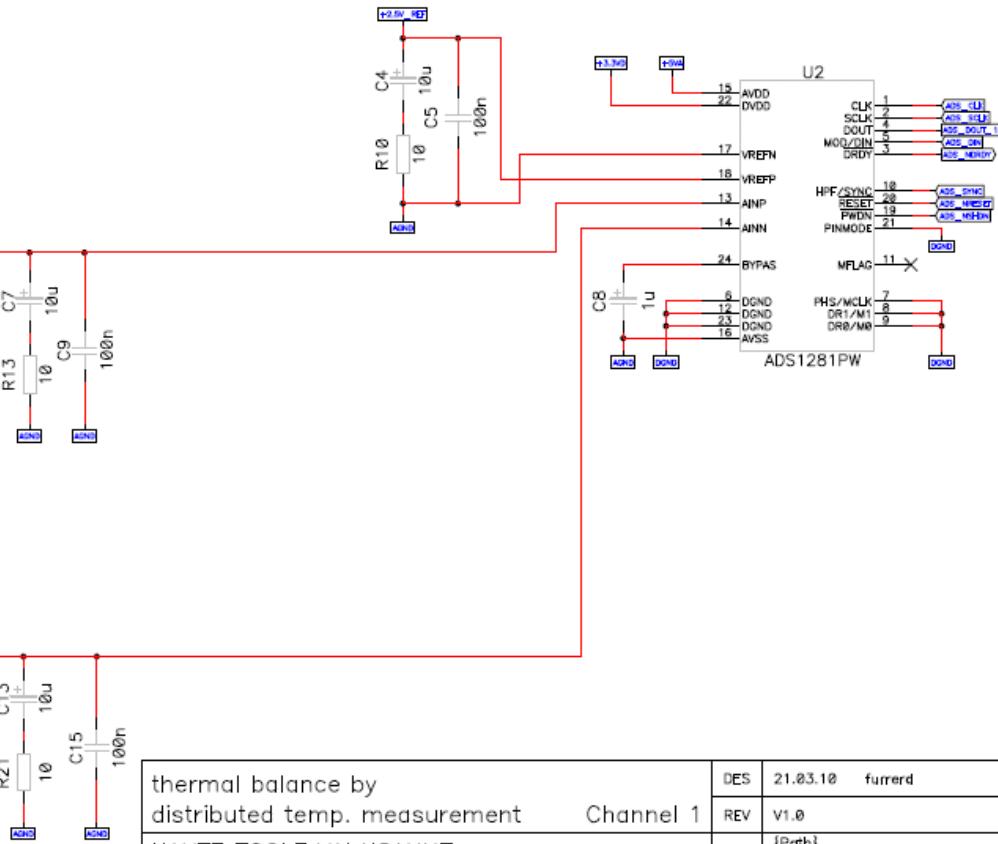
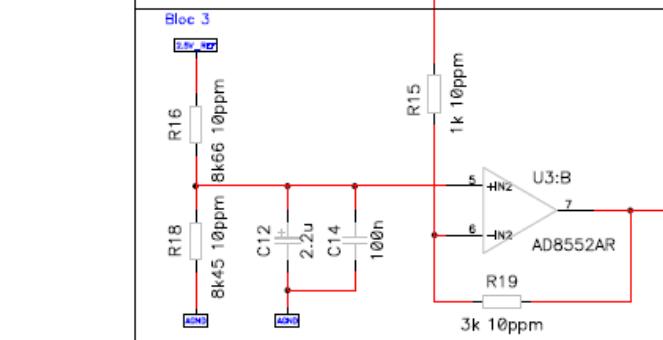
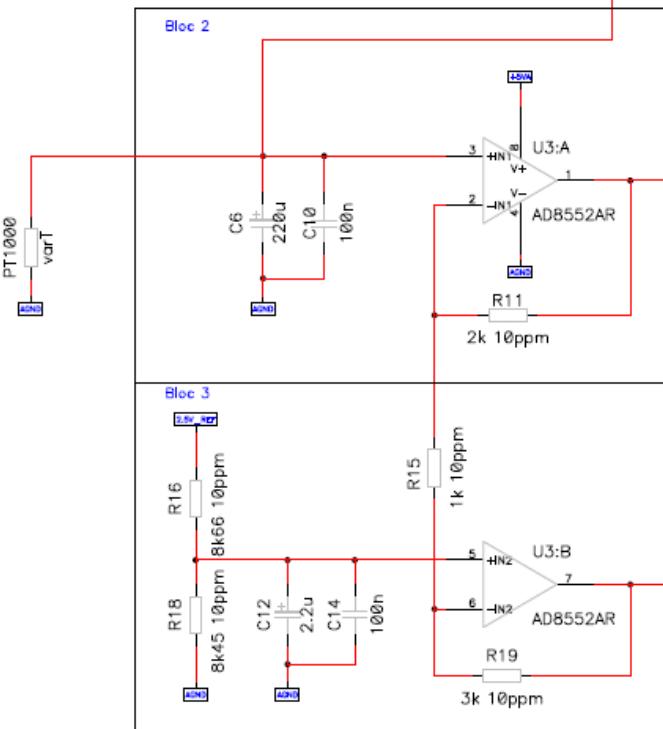
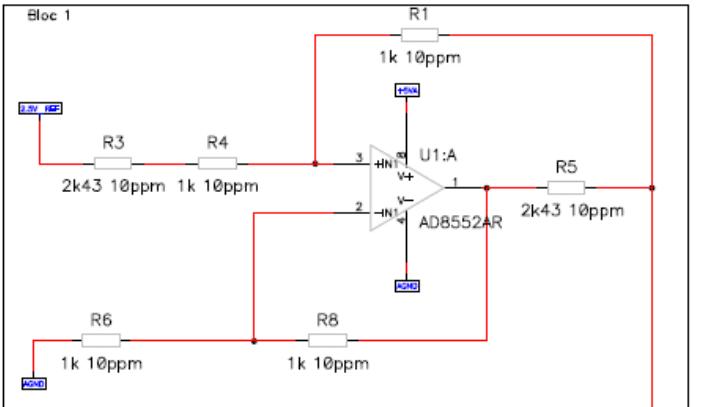


Figure 6.19: Driving Single-Supply Data Acquisition ADCs With Scaled Inputs

- Scaling network at the input

Pt1000 input circuit (1)



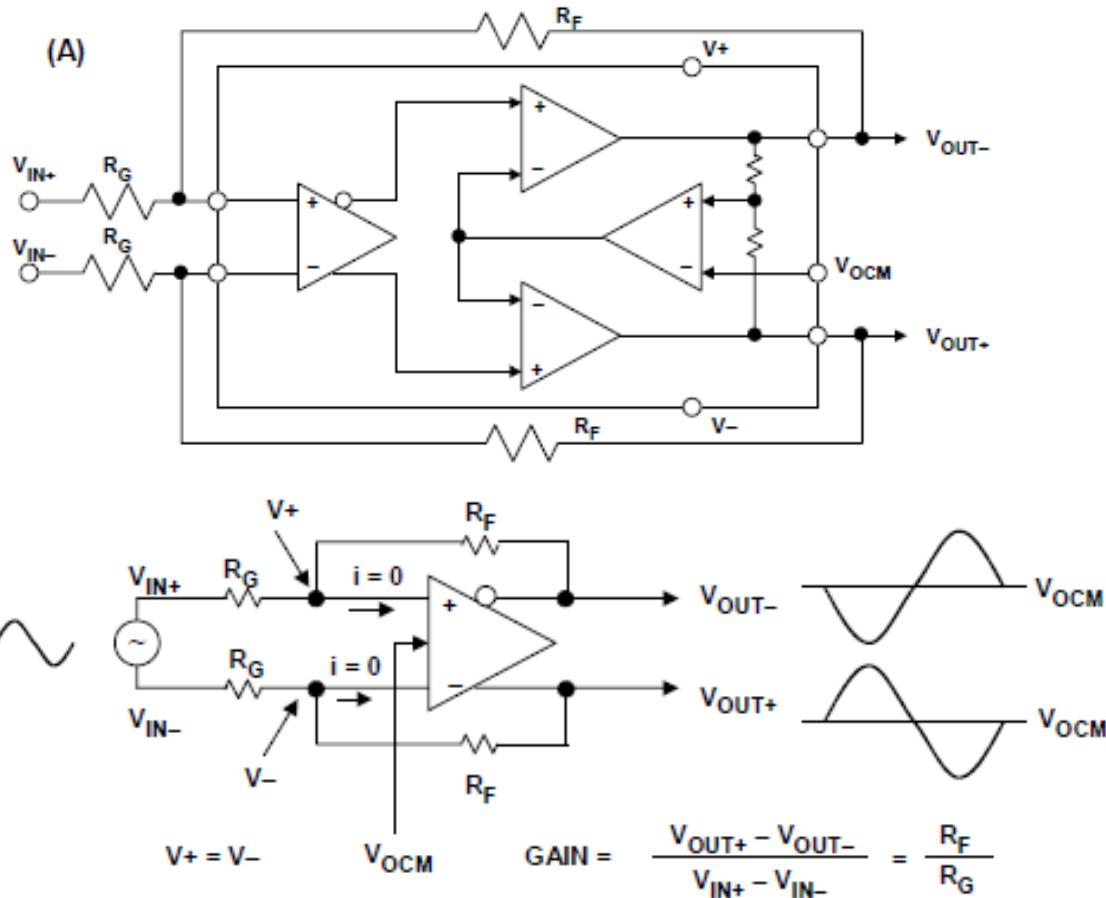
| | | | |
|---|-----------|-----|----------------------------|
| thermal balance by distributed temp. measurement | Channel 1 | DES | 21.03.10 furred |
| | | REV | V1.0 |
| HAUTE ECOLE VALAISANNE | | 1/6 | {Path} therm_bal_v_1.1.sch |

Pt1000 input circuit (2)

The circuit on the slide above acquires a temperature measured by a Pt1000 resistor, through a 24 bits ADC (ADS1281), with the following characteristics : $f_s = 10\text{Hz}$, dynamic range of AINP and AINN : $0 \dots V_{\text{ref}}$, conversion of $V_{\text{AINP}} - V_{\text{AINN}}$ within the range $\pm V_{\text{ref}}$. $V_{\text{ref}} = 2.5\text{V}$ (net $+2.5\text{V_REF}$).

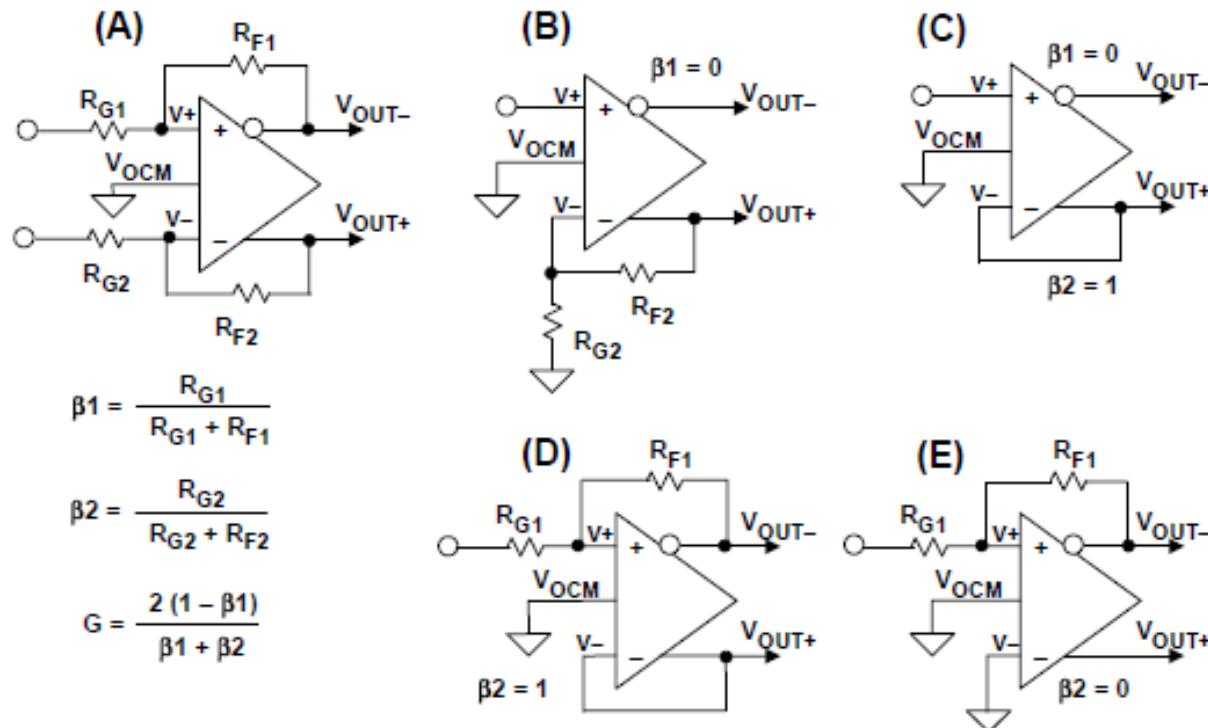
- Describe in words the function of each of the 3 framed blocks.
- Why are resistors R16 and R18 not set to equal values ?
- Determine the temperature measurement range in $^{\circ}\text{C}$ and the circuit sensitivity in $\text{LSB}/^{\circ}\text{C}$, knowing that the resistance of the Pt1000 sensor is 1000Ω at 0°C , increasing by $0.4\%/{^{\circ}\text{C}}$.
- Consider only voltage and current noises of the operational amplifiers AD8552: $40\text{nV}/\text{rtHz}$ and $2\text{fA}/\text{rtHz}$, supposed to be uniform over frequency. What is the spectral density of the current noise in the Pt1000 sensor ? What is the spectral density of the voltage noise at inputs AINP and AINN of the A/D converter ? What is the signal-to-noise ratio between 0 and 5Hz after A/D conversion, taking into account quantization noise and noise in the operational amplifiers ?

Integrated differential amplifier drivers (1)



- ◆ + and – input currents are zero
- ◆ + and – input voltages are equal
- ◆ Output voltages are 180° out of phase and symmetrical about V_{OCM}
- ◆ Gain = R_F/R_G

Integrated differential amplifier drivers (2)



- β_1 : Amount of feedback from V_{out-} to V_+
- β_2 : Amount of feedback from V_{out-} to V_+

Integrated differential amplifier drivers (3)

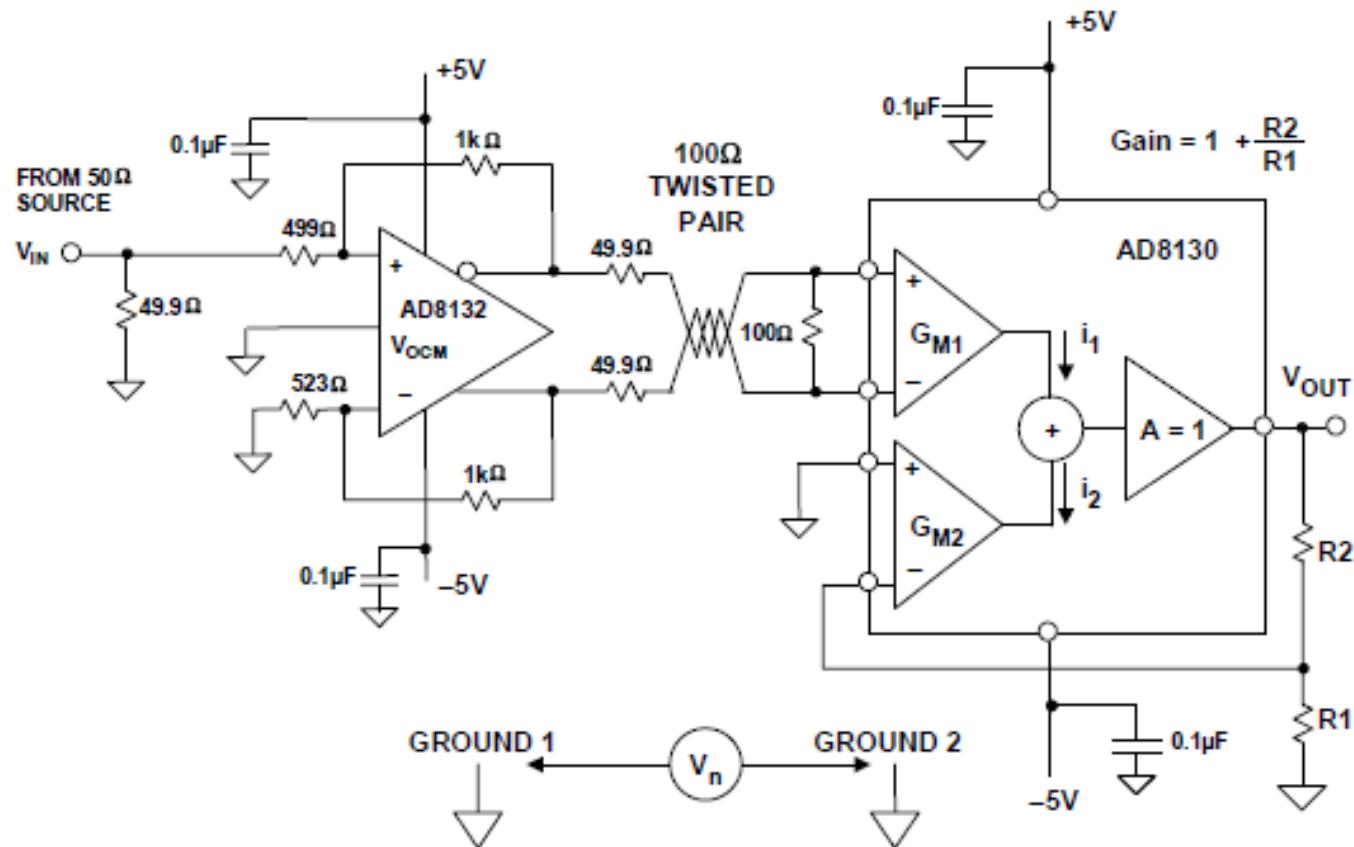
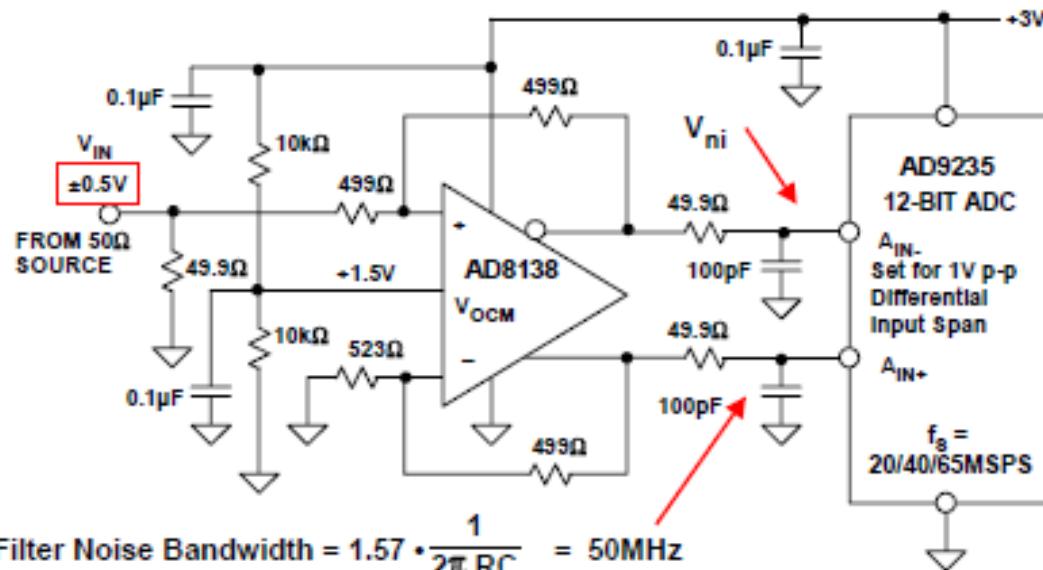


Figure 6.35: High Speed Differential Line Driver,
Line Receiver Applications

Integrated differential amplifier drivers (4)

- Replacement for baluns when direct coupling required



AD8038 DIFF. AMP SPECIFICATIONS

- ◆ Output Voltage Noise = $11.6\text{nV}/\sqrt{\text{Hz}}$
- ◆ Closed-Loop BW = 300MHz
- ◆ Closed-Loop Noise BW = $1.57 \times 300\text{MHz} = 471\text{MHz}$

AD8038 Output Noise Spectral Density = $11.6\text{nV}/\sqrt{\text{Hz}}$ (Including Resistors)

$$V_{ni} = 11.6\text{nV}/\sqrt{\text{Hz}} \cdot \sqrt{50\text{MHz}} = 78.2\mu\text{V rms}$$

AD9235 ADC SPECIFICATIONS

- ◆ Effective Input Noise = $132\mu\text{V rms}$
- ◆ Small Signal Input BW = 500MHz
- ◆ Input Noise BW = $1.57 \times 500\text{MHz} = 785\text{MHz}$

Figure 6.38: Noise Calculations for the AD8138 Differential Op Amp Driving the AD9235 12-Bit, 20-/40-/65-MSPS ADC
Input filters and buffers

Front end bridge connection

- 4 wire Kelvin connection
- Ratiometric conversion

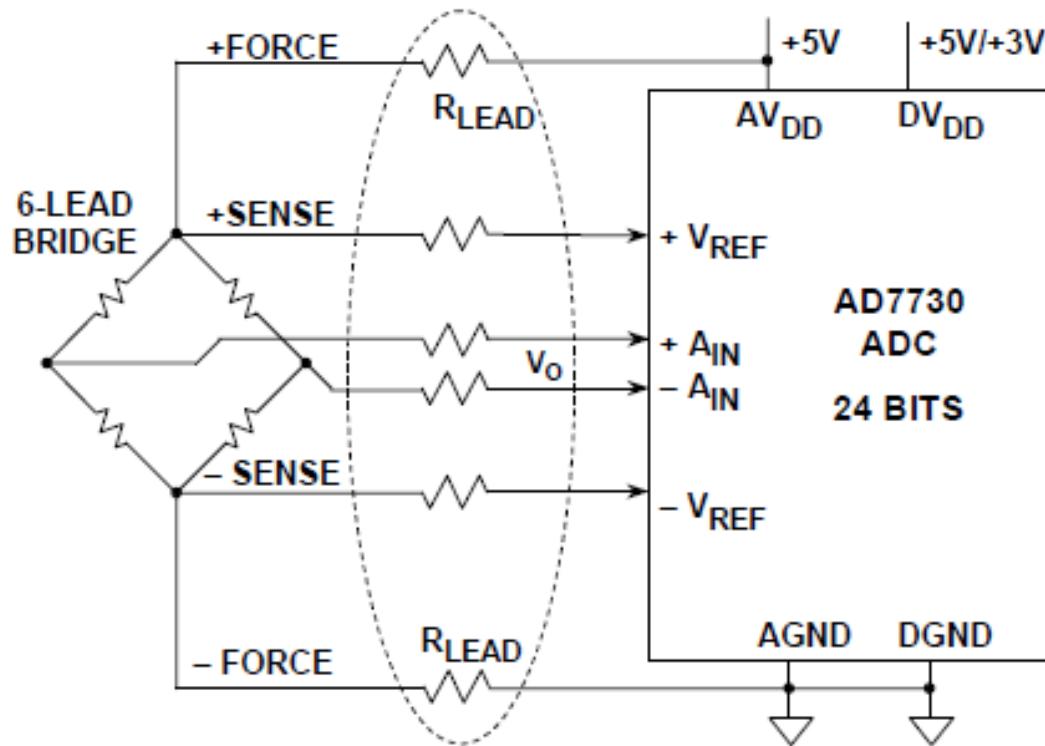


Figure 8.7: AD7730 Bridge Application Showing Ratiometric Operation and Kelvin Sensing

Weigh scale example (1)

- ◆ Full Load: 2 kg
- ◆ Sensitivity: 2 mV/V
- ◆ Excitation: 10 V max

- ◆ Other Features
 - Impedance 350 Ω
 - Total Error 0.025 %
 - Hysteresis 0.025 %
 - Repeatability 0.01%
 - Temperature drift: 10ppm
 - Overload 150%
 - Dimensions
 - Cost (\$200)



TYPICAL LOAD CELLS

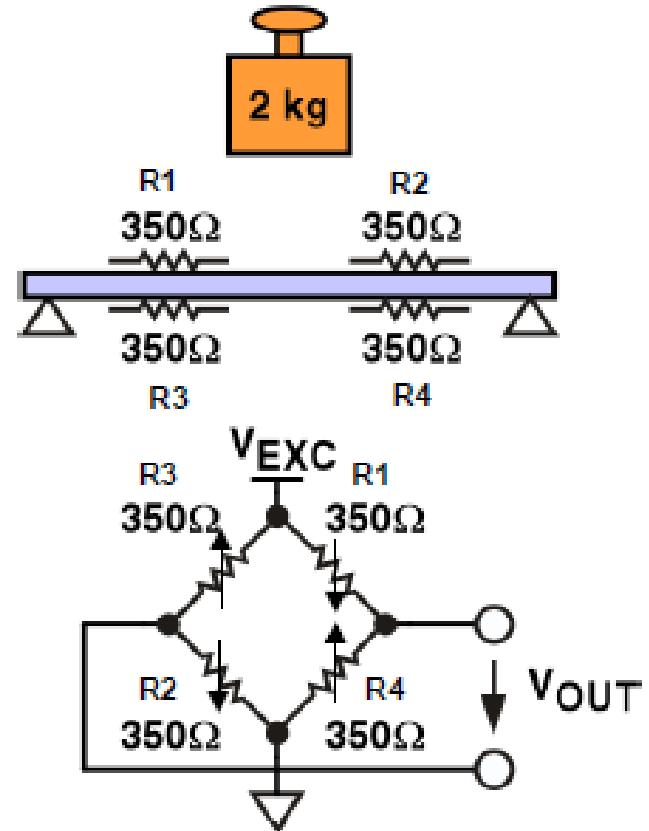


Figure 8.9: Load Cell Characteristics

Weigh scale example (2)

- ◆ Full Load: 2 kg
- ◆ Sensitivity: 2 mV/V
- ◆ Excitation: 5 V

- $V_{FS} = V_{EXC} \times \text{Sensitivity}$
- $V_{FS} = 5V \times 2\text{mV/V} = 10\text{ mV}$
- $V_{CM} = 2.5\text{ V}$

- ◆ Full-Scale Output Voltage: 10 mV
- ◆ Proportional to excitation voltage
- "Ratiometric"

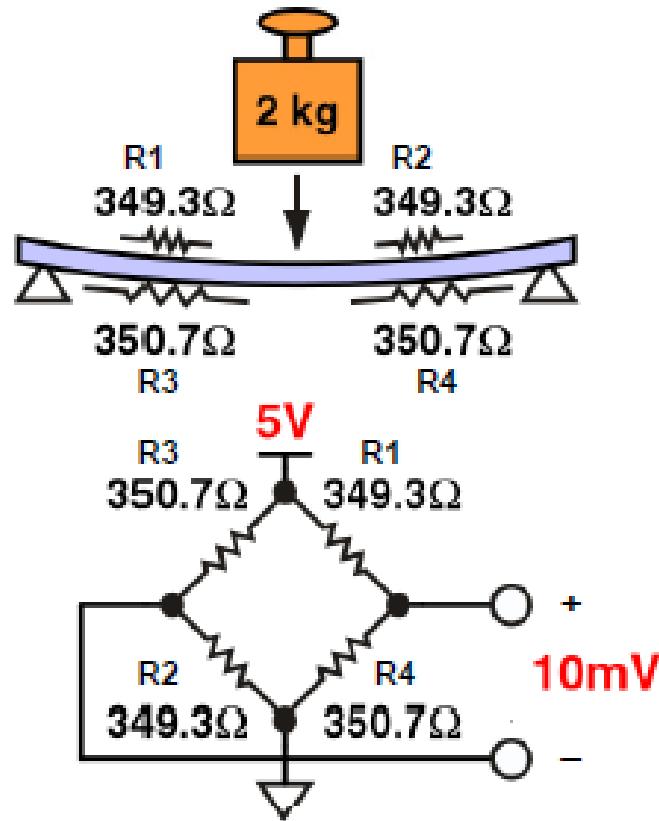


Figure 8.10: Determining Fullscale Output of Load Cell with 5-V Excitation

Weigh scale example (3)

- ◆ Required 0.1 g in 2 kg
 - ◆ # counts = full-scale / resolution
 - ◆ # counts = $2000 \text{ g} / 0.1\text{g} = 20,000$
- 20,000 counts
 - ◆ $V_{FS} = 10\text{mV}$ @ 5V excitation
 - ◆ $V_{P-P} = V_{FS} / \# \text{ counts}$
 - ◆ $V_{P-P} = 10\text{mV} / 20,000 = 0.0005\text{mV}$
- 0.5 μV p-p noise
 - ◆ $V_{RMS} \approx V_{P-P} / 6.6$
 - ◆ $V_{RMS} \approx 0.5\mu\text{V} / 6.6 = 0.075\mu\text{V}$
- 75nV RMS noise
 - ◆ Bits p-p = $\log_{10}(V_{FS} / V_{P-P}) / \log_{10}(2)$
 - ◆ Bits p-p = $\log(10\text{mV} / 0.0005\text{mV}) / 0.3$
- 14.3 bits p-p in 10mV range
(Noise-free bits)
 - ◆ Bits RMS = $\log_{10}(V_{FS} / V_{RMS}) / \log_{10}(2)$
 - ◆ Bits RMS = $\log_{10}(10\text{mV} / 0.000075) / 0.3$
- 17.0 bits RMS in 10mV range
(Effective resolution)

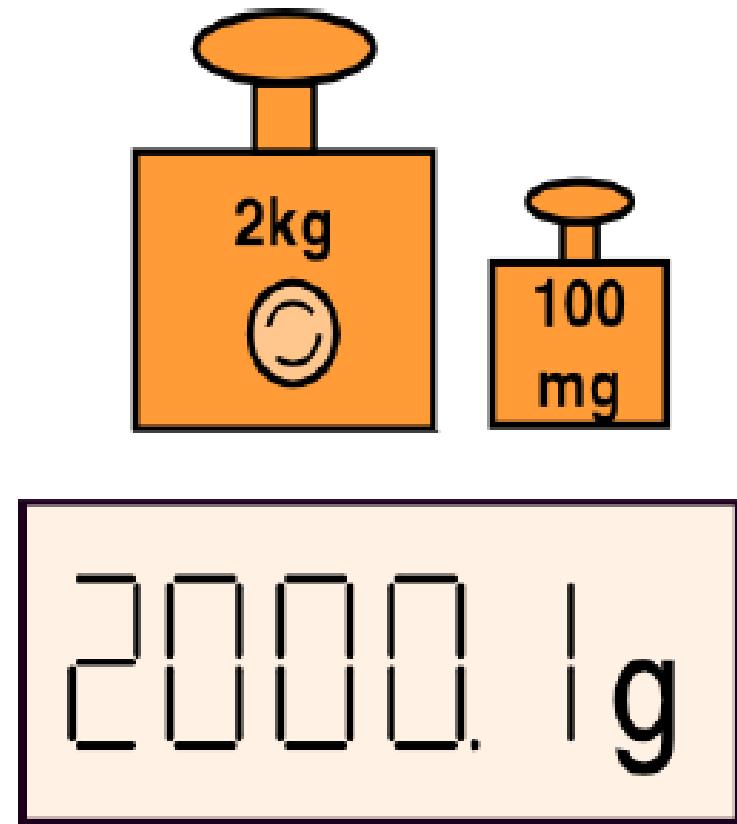


Figure 8.11: Determining Resolution Requirements

Weigh scale example (4)

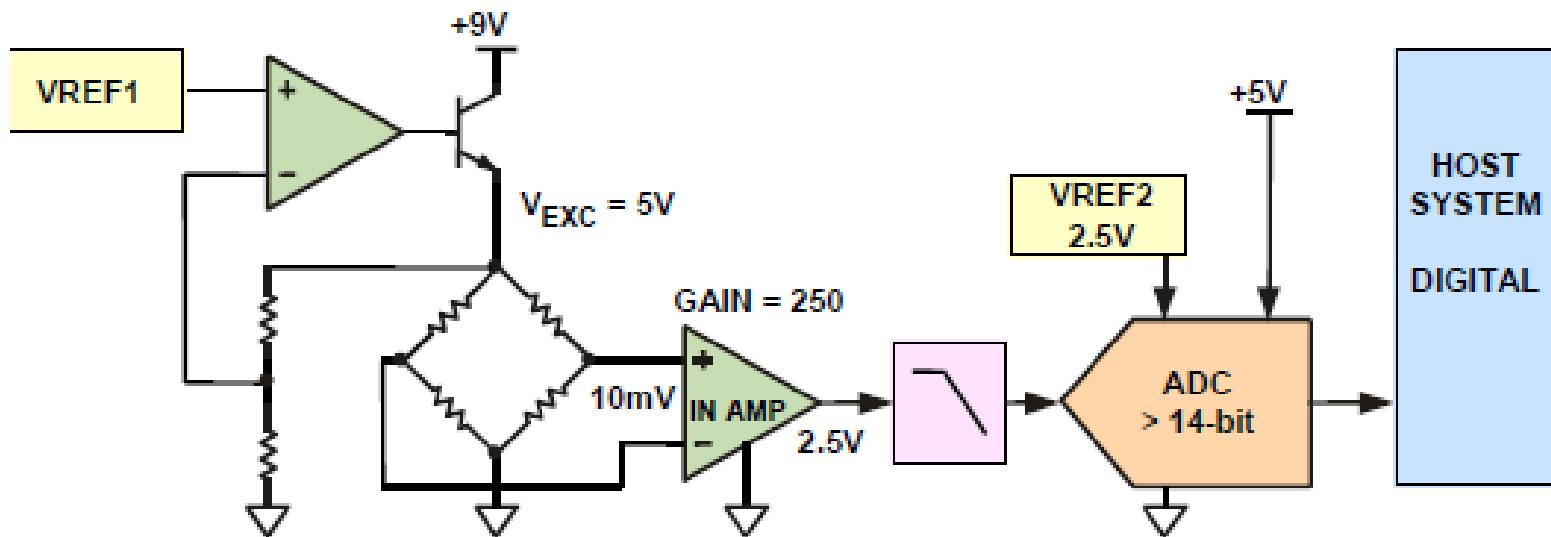
The noise-free code resolution of the ADC is calculated as follows:

$$\text{Noise-Free Code Resolution (Bits)} = \frac{\log_{10}\left(\frac{V_{FS}}{V_{PP}}\right)}{\log_{10}(2)}$$
$$= \frac{\log_{10}\left(\frac{10\text{mV}}{0.5\mu\text{V}}\right)}{\log_{10}(2)} = 14.3 \text{ bits}$$

The effective resolution of the ADC is calculated as follows:

$$\text{Effective Resolution (Bits)} = \frac{\log_{10}\left(\frac{V_{FS}}{V_{PP}/6.6}\right)}{\log_{10}(2)}$$
$$= \frac{\log_{10}\left(\frac{10\text{mV}}{0.5\mu\text{V}/6.6}\right)}{0.3} = 17 \text{ bits.}$$

Weigh scale example (5)

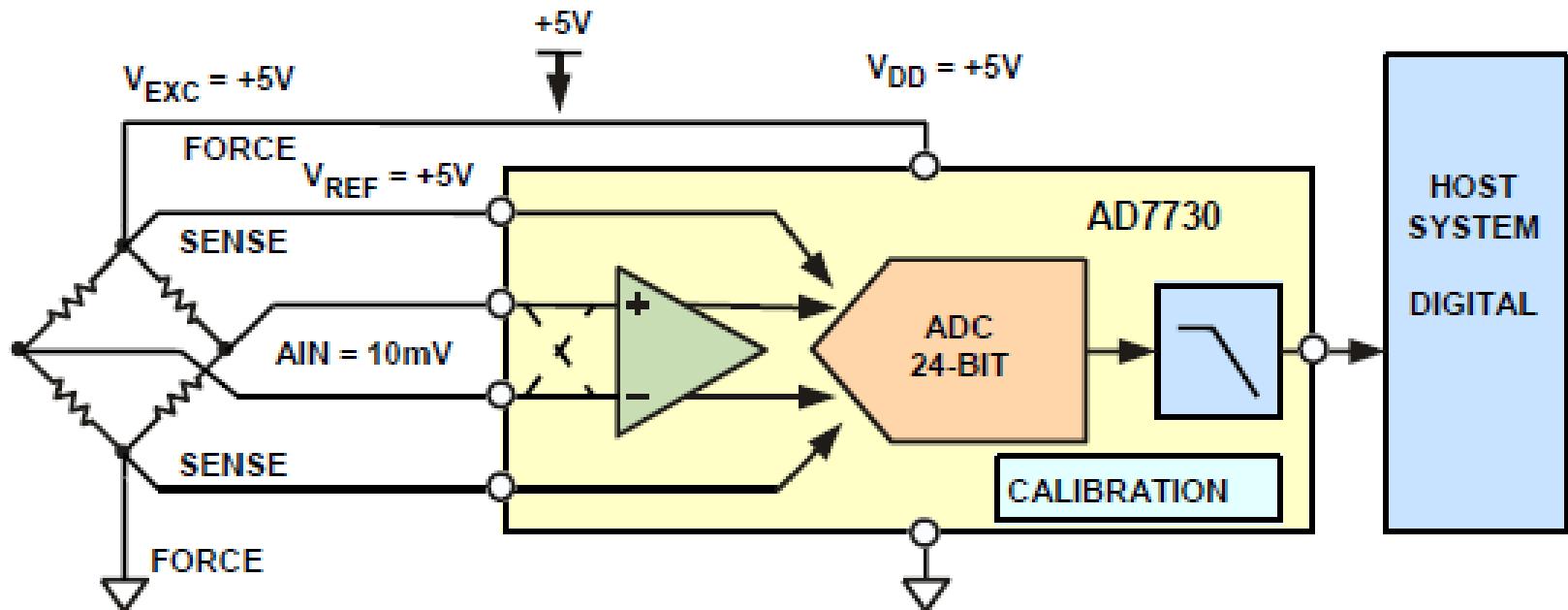


- ◆ Complicated design
- ◆ Low pass filter is needed to keep low noise
 - For example, -3dB @ 10Hz , -60dB @ 50Hz (difficult filter design)
- ◆ Instrumentation amplifier performance is critical
 - Low noise (AD620: $0.28\mu\text{V p-p}$ noise in 0.1Hz to 10Hz BW is approximately 42nV RMS), low offset, low gain error

Figure 8.12: Traditional Approach to Design

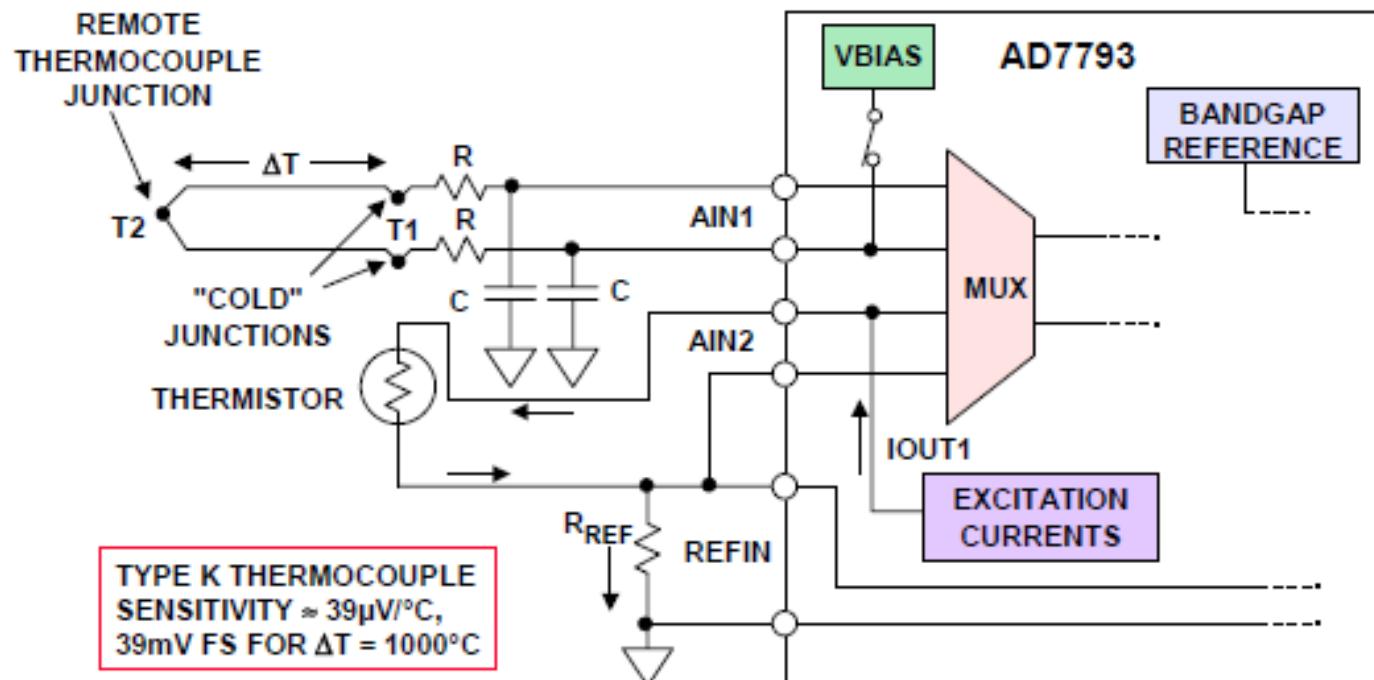
Weigh scale example (6)

- Ratiometric conversion



- ◆ AD7730 was designed for bridge transducers
 - ◆ Chopper, Buffer, PGA, Digital filter, tare DAC, Calibrations, ...
- ◆ Fully Ratiometric, changes on $V_{EXC} = V_{REF}$ eliminated
 - ◆ Load $\approx V_{OUT} / V_{EXC}$, AD7730 Data $\approx V_{IN} / V_{REF}$, $V_{REF} = V_{EXC}$

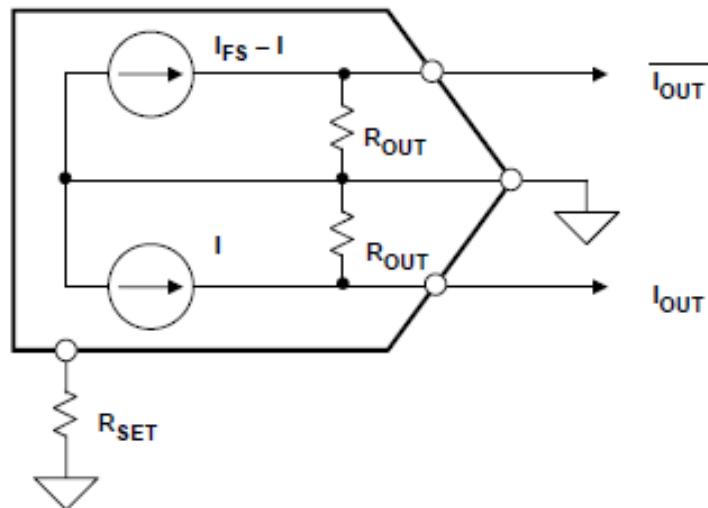
Thermocouple interface



- ◆ Bias voltage generator used to generate a common mode voltage for AIN1
- ◆ Current source provides current to thermistor for cold junction compensation and ratiometric operation using REFIN

Figure 8.19: Thermocouple Design with Cold Junction Compensation using the AD7793

DAC output model



- ◆ I_{FS} 2 - 20mA typical
- ◆ Bipolar or BiCMOS DACs sink current, $R_{OUT} < 500\Omega$
- ◆ CMOS DACs source current, $R_{OUT} > 100k\Omega$
- ◆ Output compliance voltage $< \pm 1V$ for best performance

Figure 6.68: Generalized Model of a High Speed DAC Output such as the AD976x and AD977x Series

Output buffers

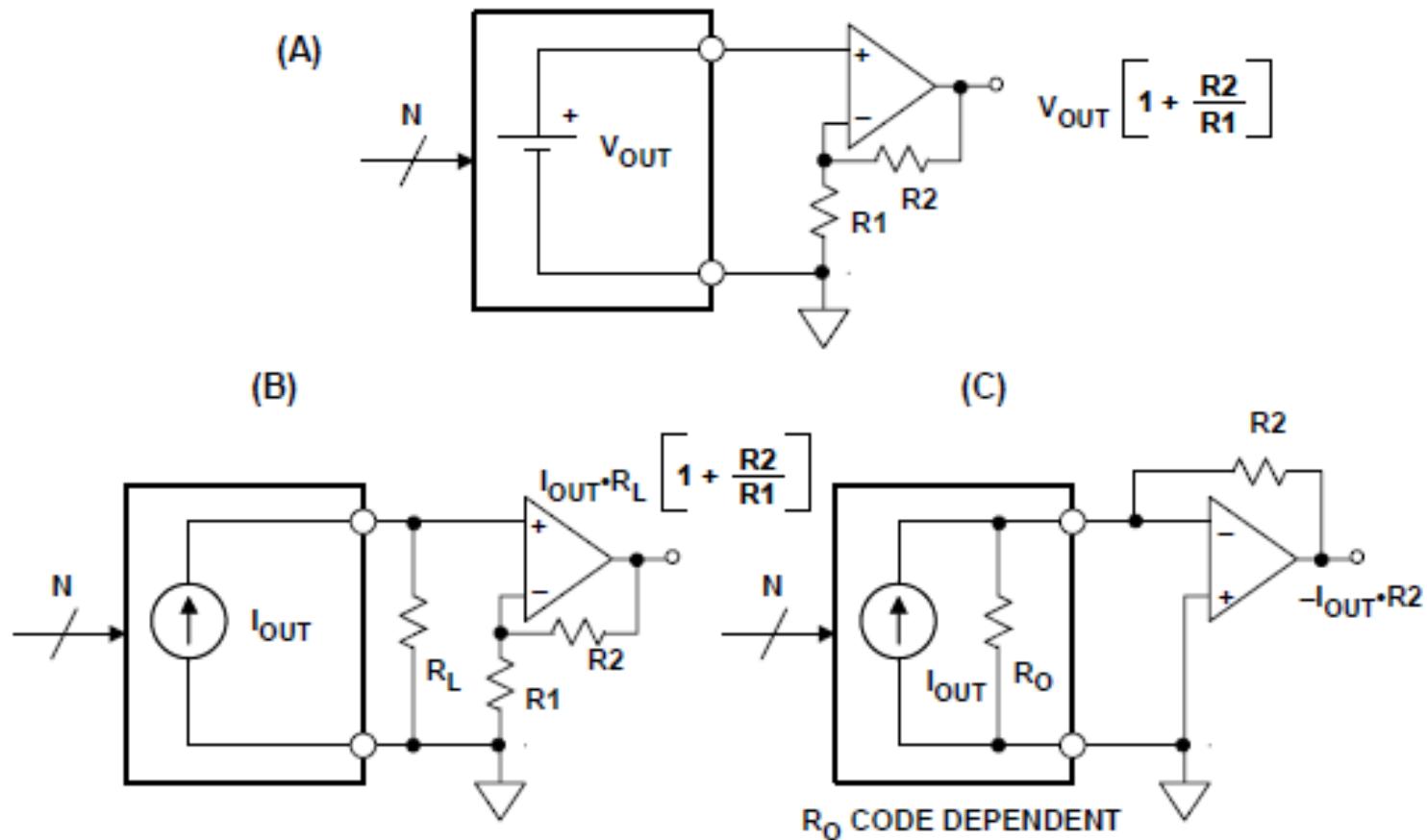


Figure 6.67: Buffering DAC Outputs with Op Amps

AC coupled differential DAC output

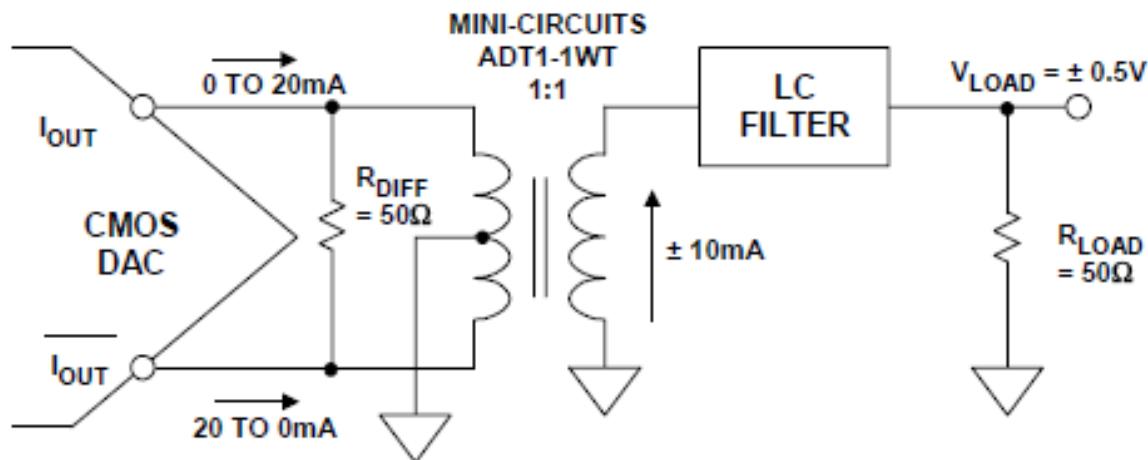
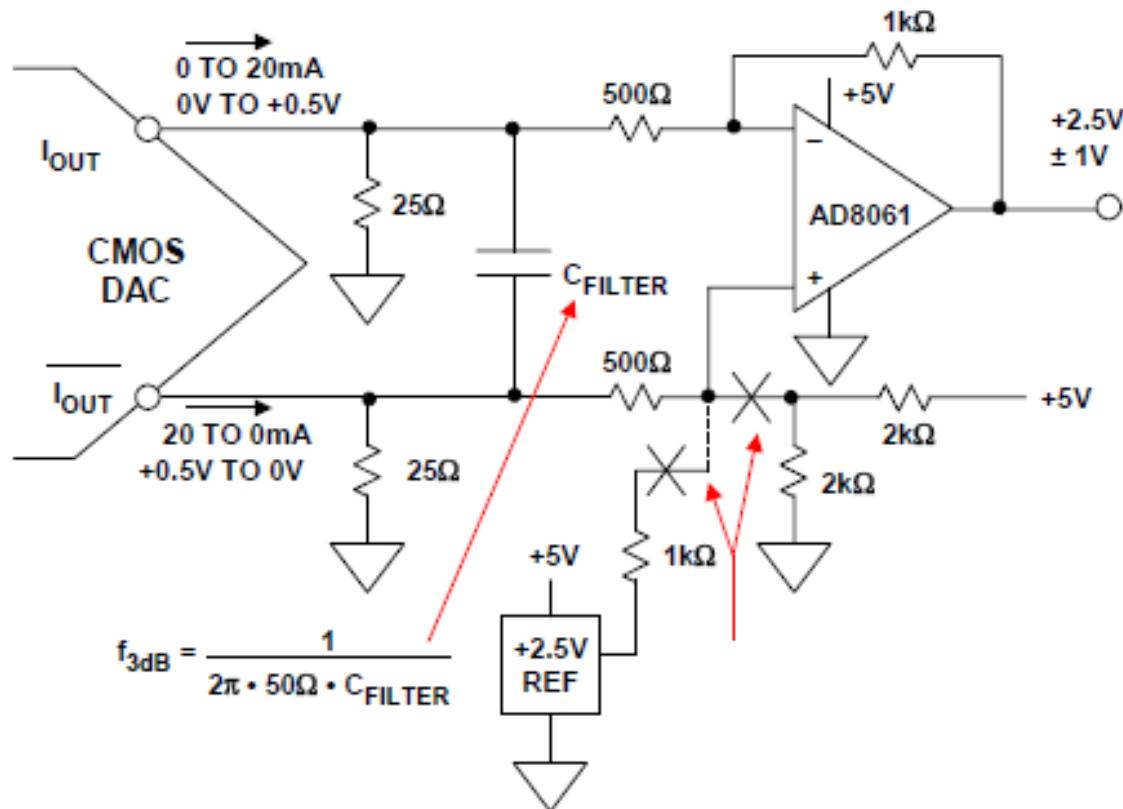


Figure 6.69: Differential Transformer Coupling

DC coupled differential DAC output



Differential DC Coupled Output Using a Single-Supply Op Amp

Output low-pass filtering

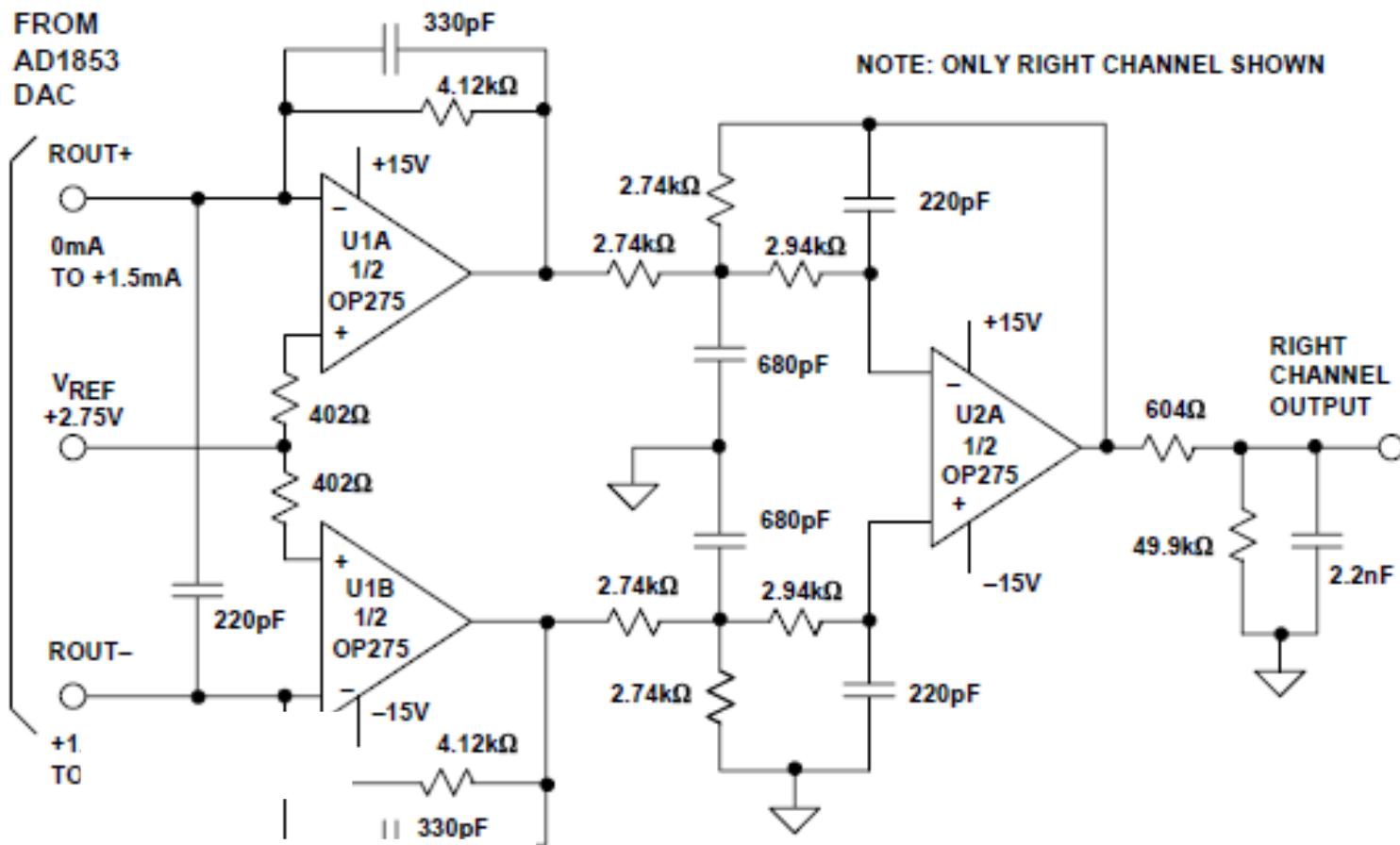


Figure 6.75: A 75-kHz 4-Pole Gaussian Active Filter for Buffering the Output of the AD1853 Stereo DAC

References

W. Kester (ed.): *Analog-Digital Conversion*, Analog Devices 2004,
ISBN 0-916550-27-3

This reference was used as a basis for the present presentation, a series of illustrations are taken from it.

The book is available for download on the moodle server.

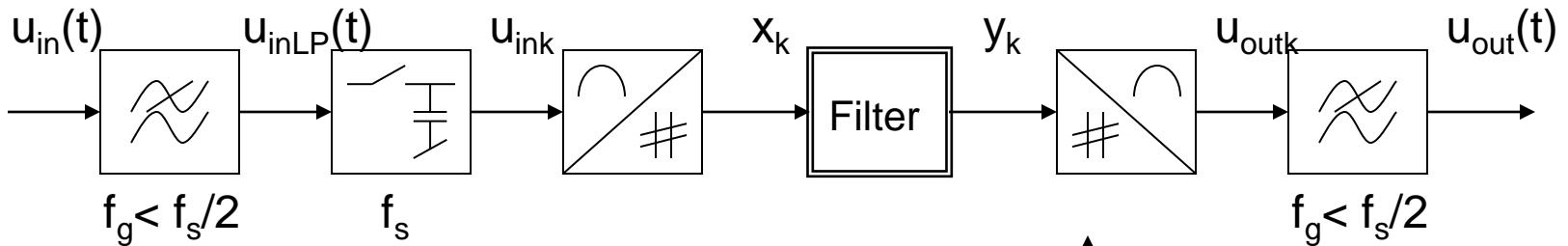
Tietze, Schenk: *Halbleiter-Schaltungstechnik*, Springer 2012 (14th ed.), ISBN 3-540-64192-0

Contents

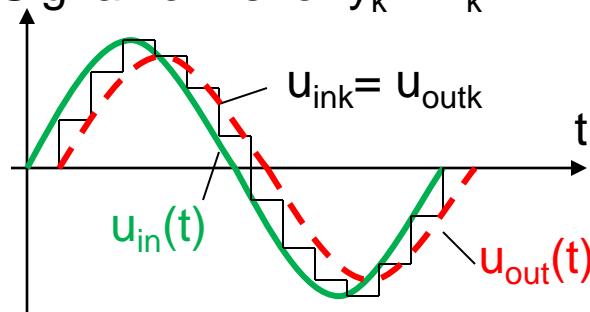
- Discretization in time: sampling
- Delta-sigma conversion
- Switched capacitor circuits
- Higher order, multi-level and cascaded modulators

- Exercises
- References

Signal processing chain

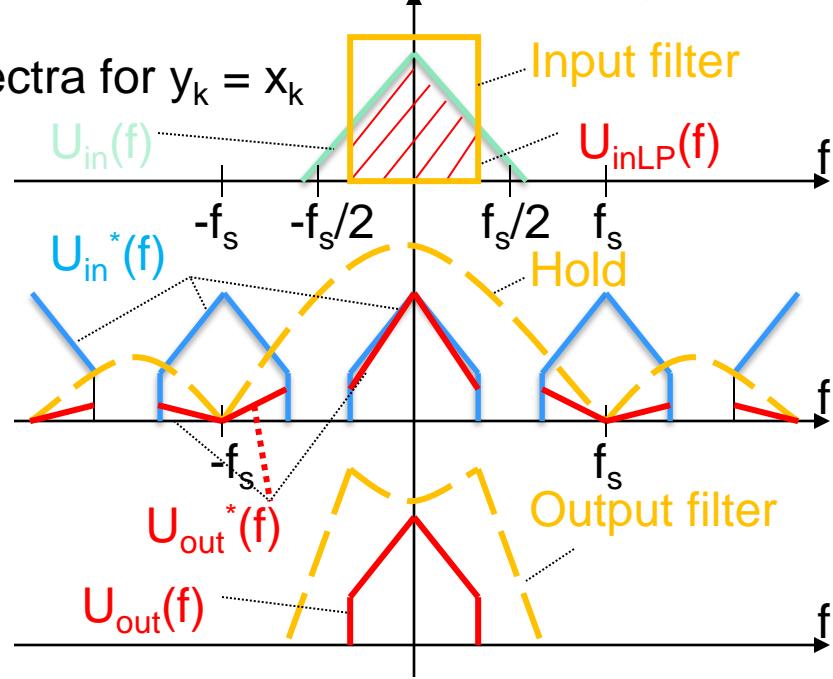


Signal forms for $y_k = x_k$



$$U_{out}^*(jf) = \frac{\sin \frac{\pi f}{f_s}}{\frac{\pi f}{f_s}} \frac{1}{f_s} \sum_{k=0}^{\infty} u_{in}(kT_s) e^{-2\pi j kf/f_s}$$

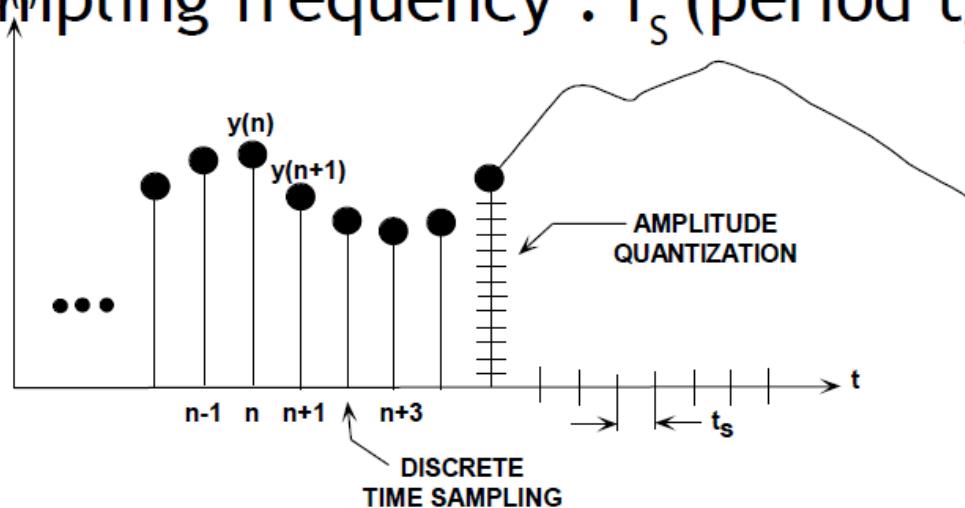
Spectra for $y_k = x_k$



Discretization (quantization) of time

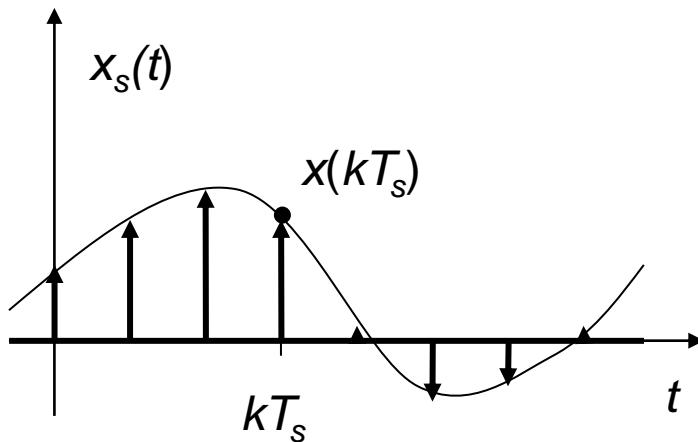
- ⌘ The value of the signal taken at a particular moment : a sample
 - After sampling, the signal is reduced to a suite of amplitude quantified numbers taken at regular time frequency
 - Unregular sampling period not used, only a sampling clock.

⌘ Def.: Sampling frequency : f_s (period t_s)



Ideal regularly sampled signal

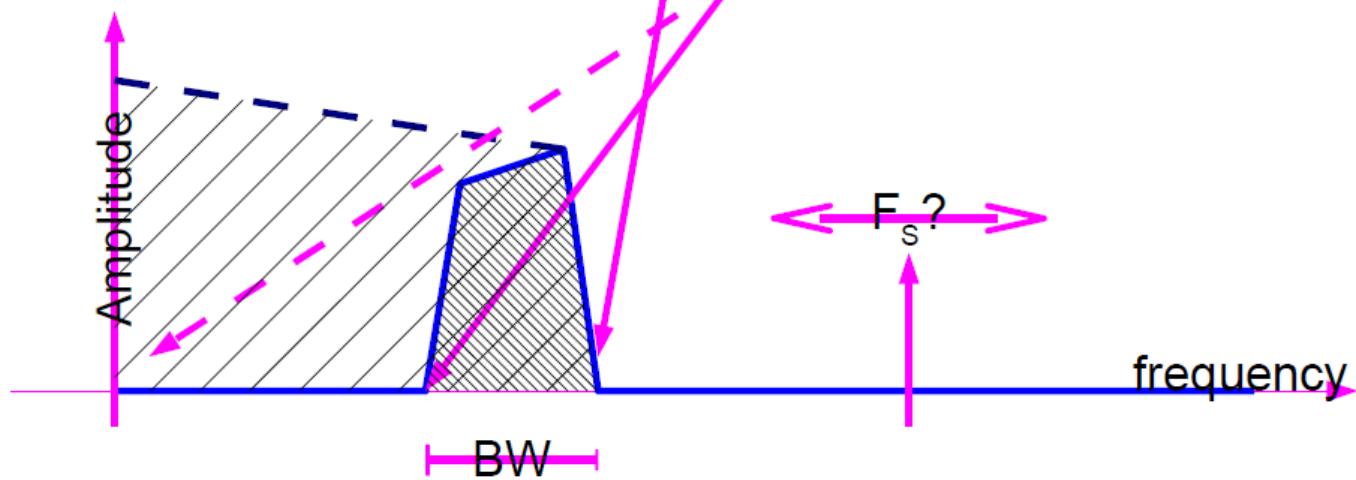
- ⌘ Sampling a signal in the time domain corresponds to a multiplication by a Dirac Sequence (mathematical notation)



$$x_s(t) = \sum_{k=-\infty}^{+\infty} x(kT_s) \cdot \delta(t - kT_s) = x(t) \cdot \sum_{k=-\infty}^{+\infty} \delta(t - kT_s)$$

Nyquist criterion

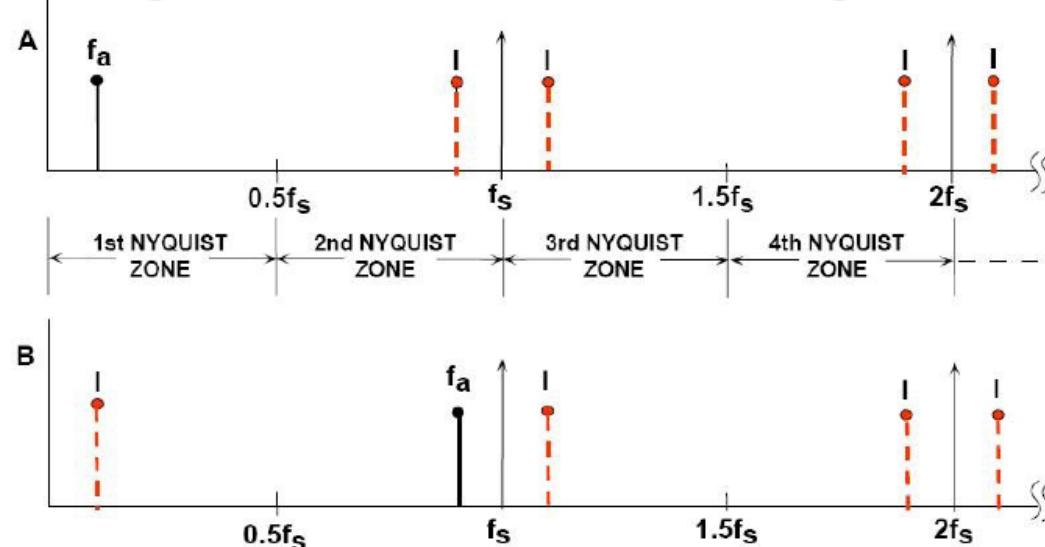
- ⌘ Sampling frequency at least twice the
Signal BANDWITH : $f_s > 2(f_a - f_b)$



- ⌘ A converter used with a $f_s =$ or just $\geq 2f_a$ is assumed to make a « Nyquist conversion »

Aliasing

- ⌘ Sampling a signal causes a repetition of the signal spectrum around f_s and multiples of f_s
 - Repetition in Frequency Domain are called “Aliasing” for an ADC and “Images” for a DAC



Analog Signal f_a Sampled @ f_s Using Ideal Sampler
Has Images (Aliases) at $|\pm Kf_s \pm f_a|$, $K = 1, 2, 3, \dots$

Signal to noise ratio

- ⌘ Quant. Noise RMS is assumed = $V_{\text{LSB}}/\sqrt{12}$
- ⌘ RMS of SinFS = $1/\sqrt{2} \cdot V_{\text{LSB}} \cdot 2^N / 2$

$$\text{SNR} = 20 \log \left(\frac{S_{\text{RMS}}}{N_{\text{RMS}}} \right) = 20 \log \sqrt{\frac{12}{8}} + 20 \log 2^N$$

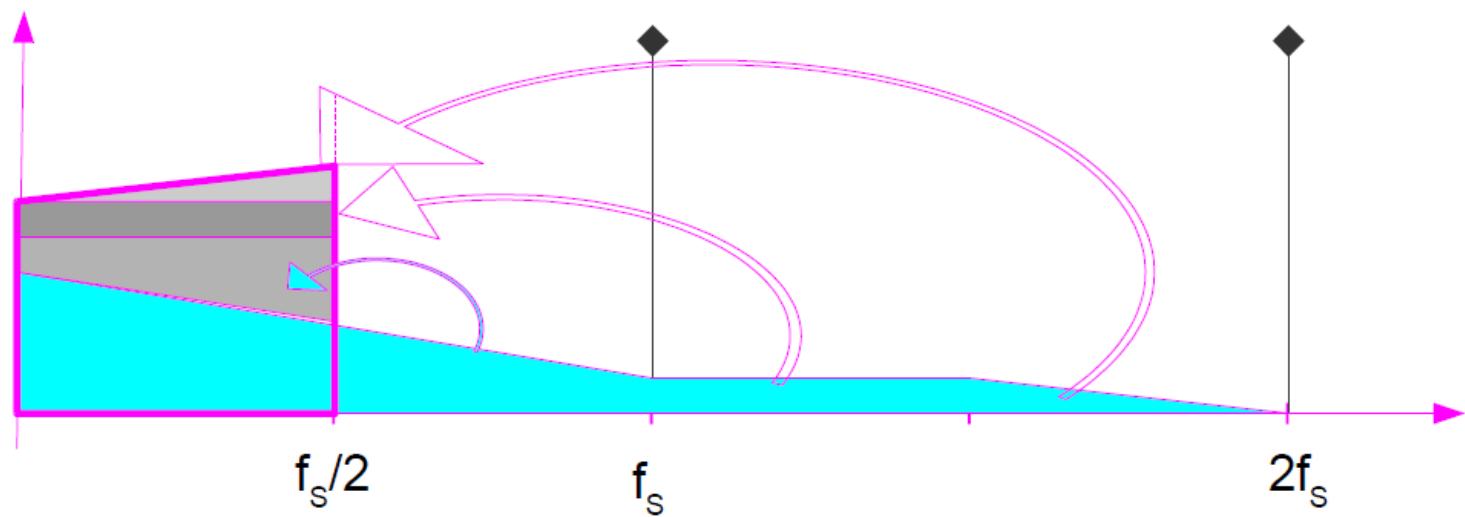
$$\text{SNR} = N \cdot 6.02 \text{ dB} + 1.76 \text{ dB}$$

[fig 2.39]

- ⌘ All quantiz Noise is folded in Nyquist zone 1 (by aliasing !)

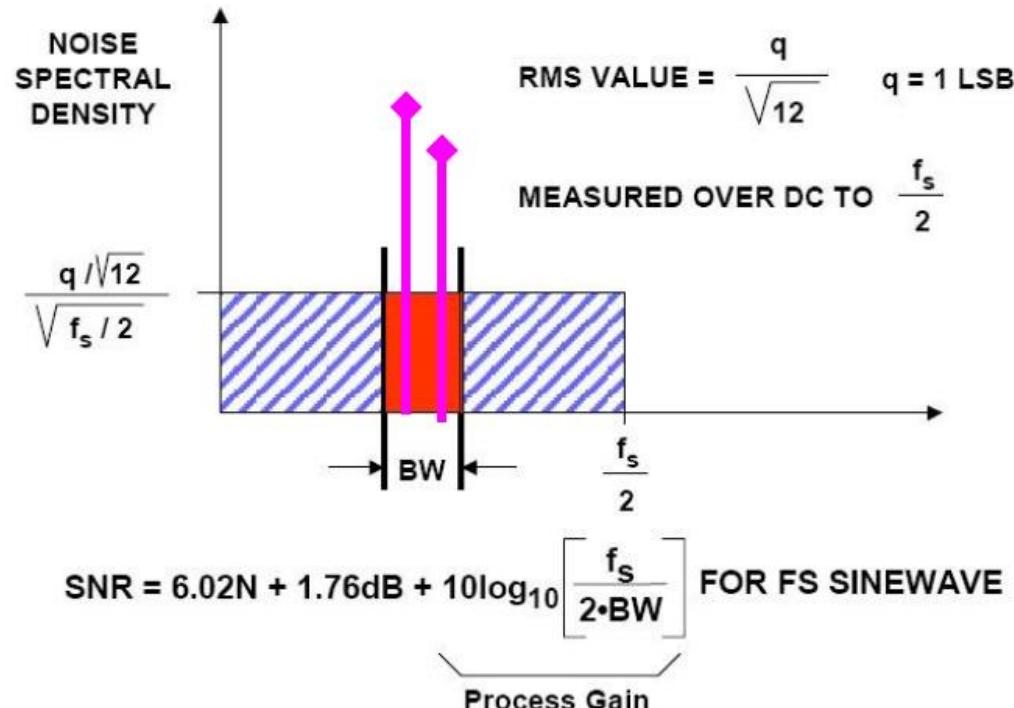
Wide band aliasing

- ⌘ Wide band *noise or signal* will be folded in the « base band » (Nyquist zone 1 : $[0 \dots f_s/2]$)



Process gain

- ⌘ Process gain is the benefit when the signal don't use all the base band $[0 .. f_s/2]$

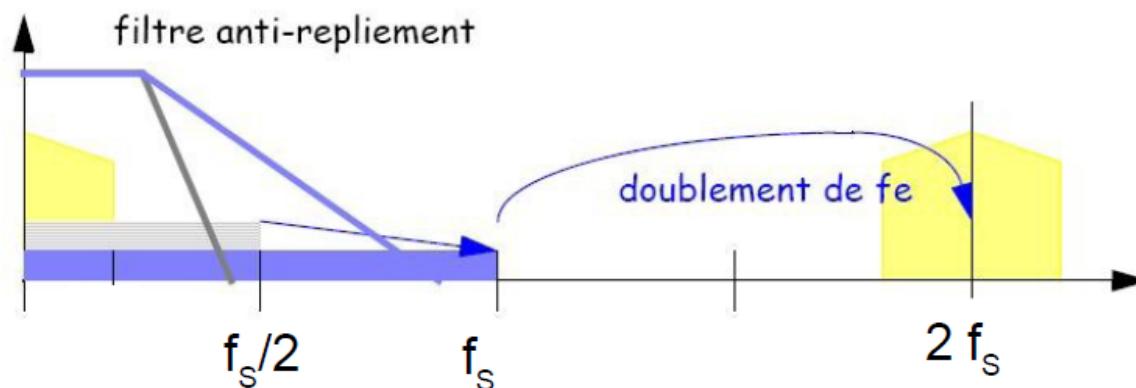


Quantization Noise Spectrum

Oversampling

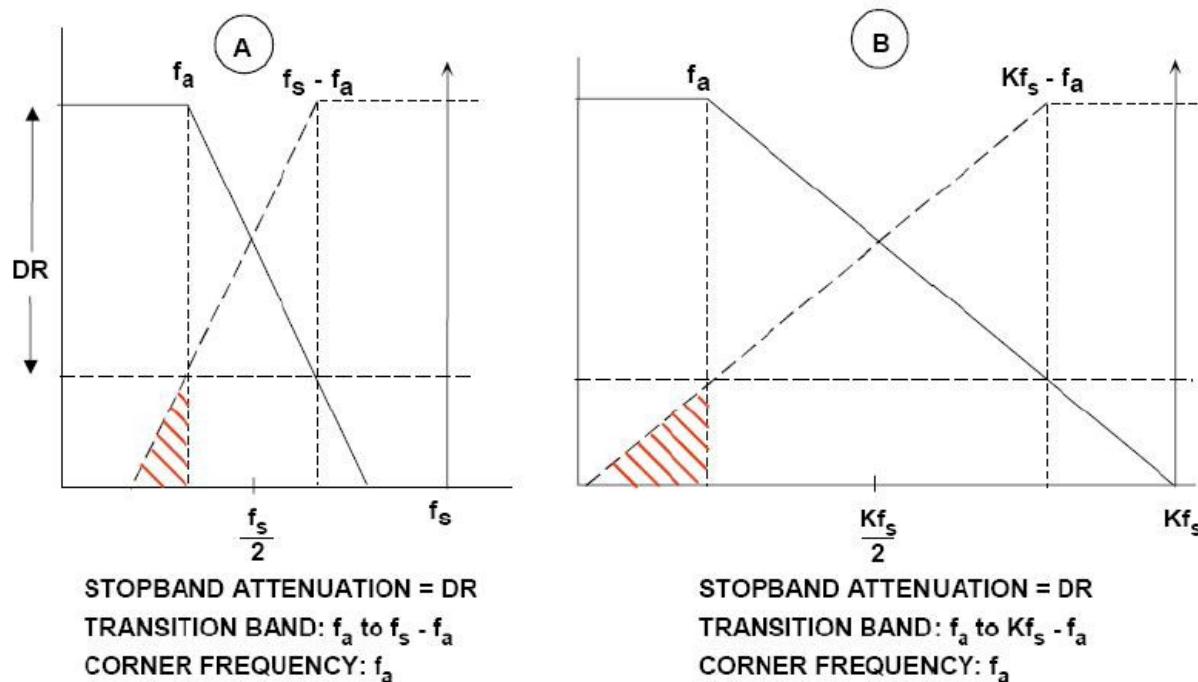
Oversampling is a convenient way to reduce noise - if BW of the signal effectively filtered! -

- Oversampling ratio **OSR** : M time the Nyquist sample frequency ($f_s/2$)
- The SNR of a oversampled system looks like:
$$\text{SNR} = 1.76 + 6N + 10 \cdot \log(\text{OSR})$$
- SNR better of +3dB each time f_s double !



Oversampling

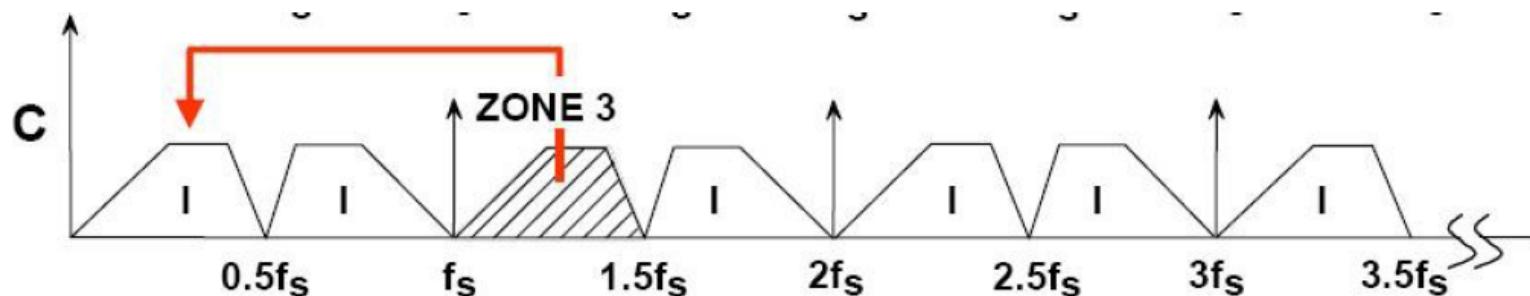
- ⌘ Oversampling is a convenient way to reduce complexity of the antialiasing filter



*Oversampling Relaxes Requirements
on Baseband Antialiasing Filter*

Undersampling

- ⌘ Possible when signal is BW-limited ($\Rightarrow f_S$ can be smaller than f_b)



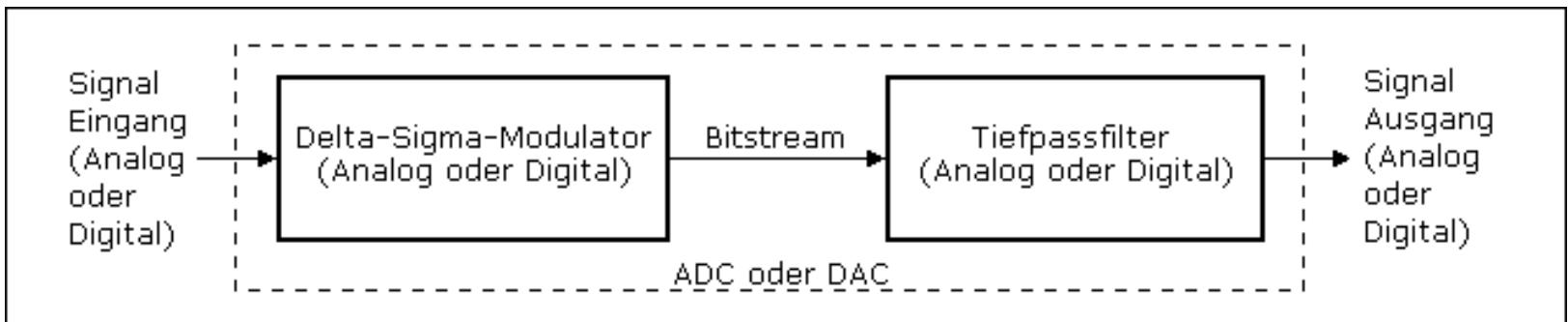
Undersampling and Frequency Translation Between Nyquist Zones

- Usual in communication systems (modulated signals) : undersampling process is *analog to demodulation* !
- But all ADC are not suited for undersampling : Caution analog BW, dynamic performances, etc.

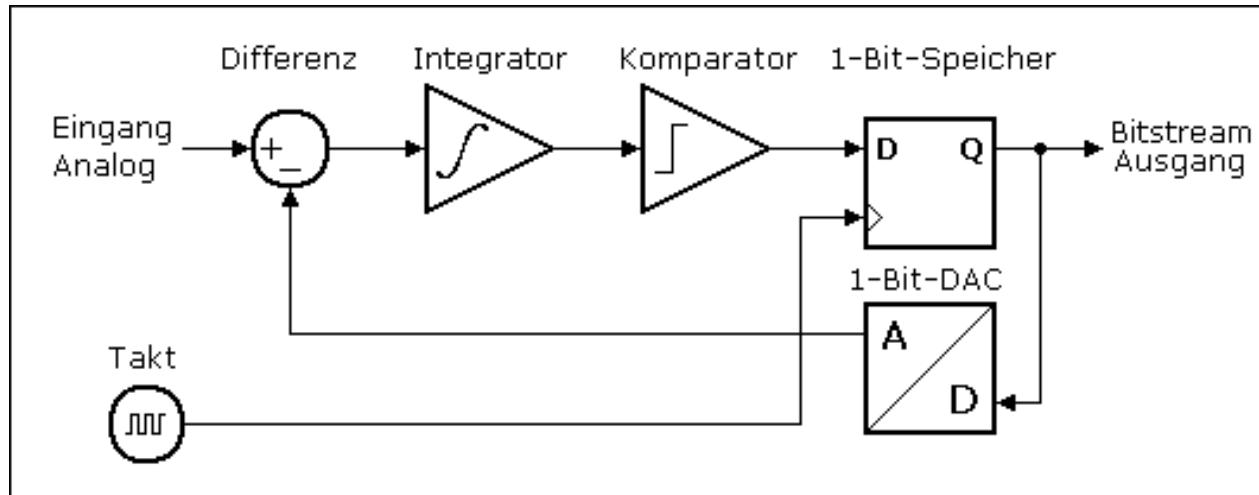
Effect of clock jitter on conversion noise

We have a 20bit audio SAR ADC with a sampling clock rate of $f_s = 48\text{ksps}$. How much rms jitter of the ADC clock signal (suppose $f_{CLK} = 24 \cdot f_s$) can be admitted, so that the conversion error remains below one LSB for sinusoidal full scale input ($\pm 1\text{V}$) signals of frequency $f = 4\text{kHz}$?

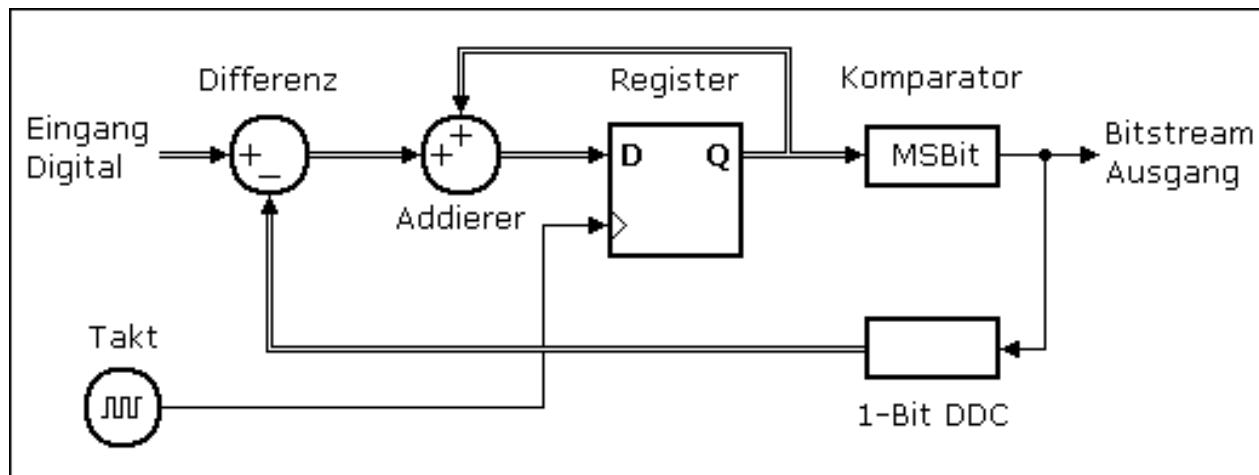
Δ - Σ -Conversion



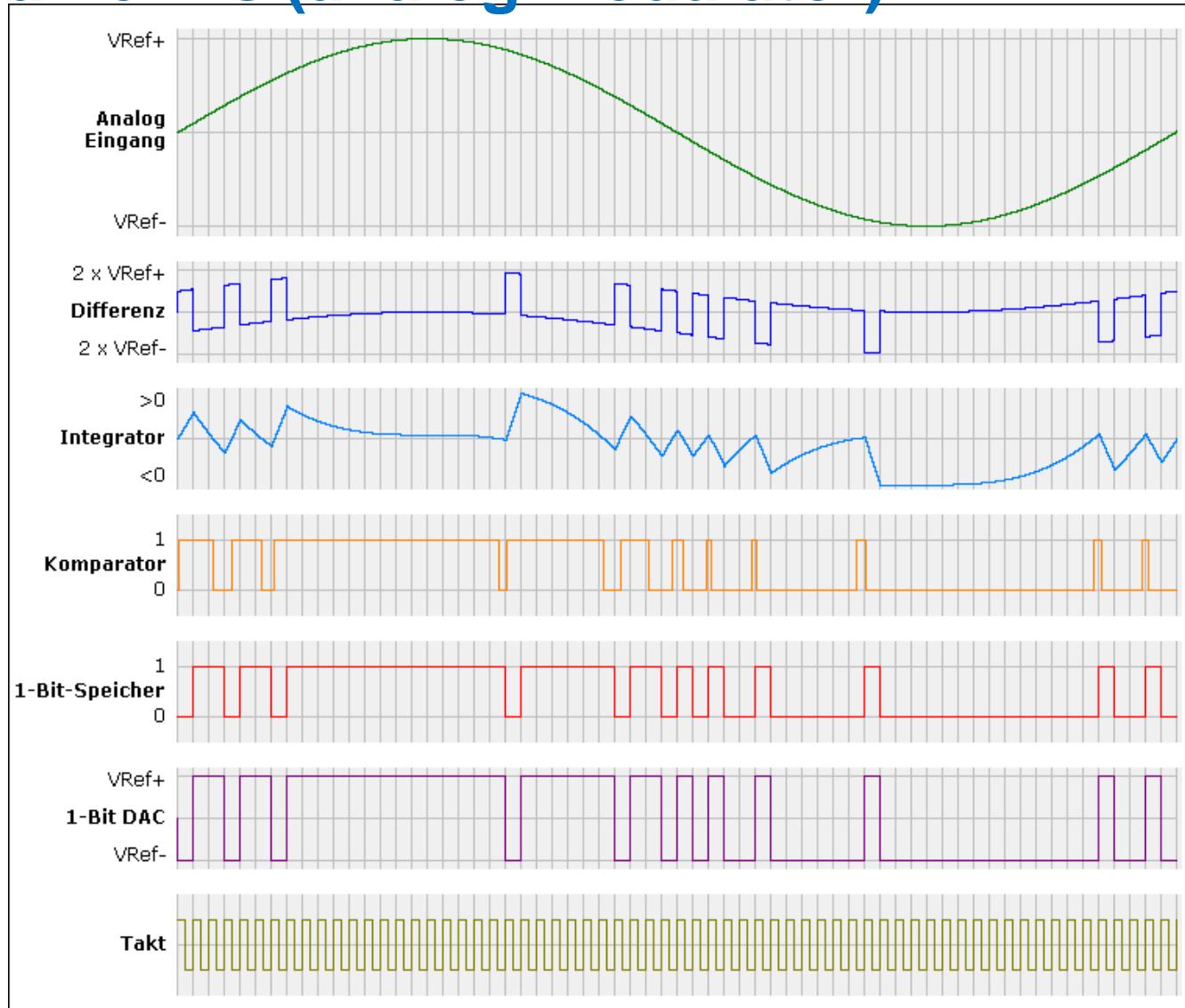
Analog first order modulator



Digital first order modulator

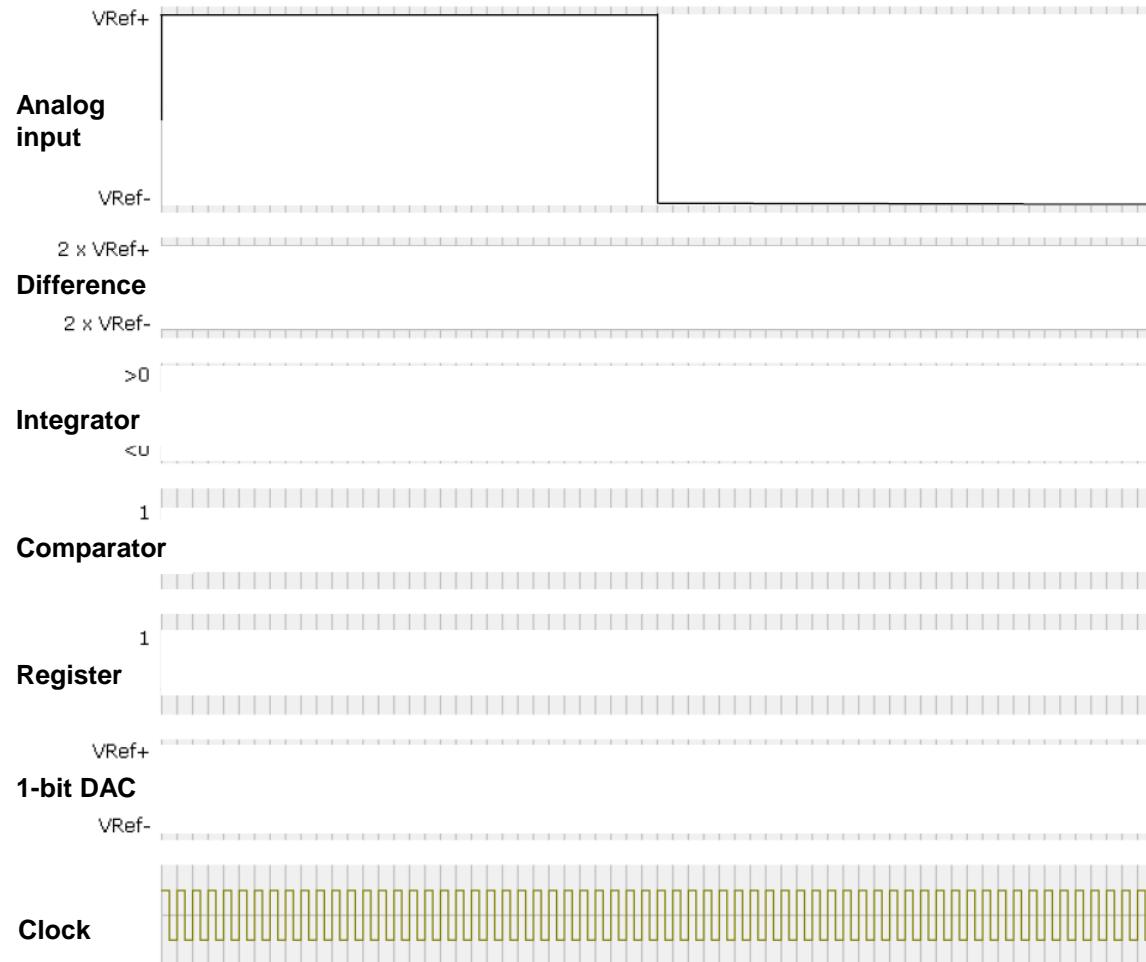


Signal forms (analog modulator)



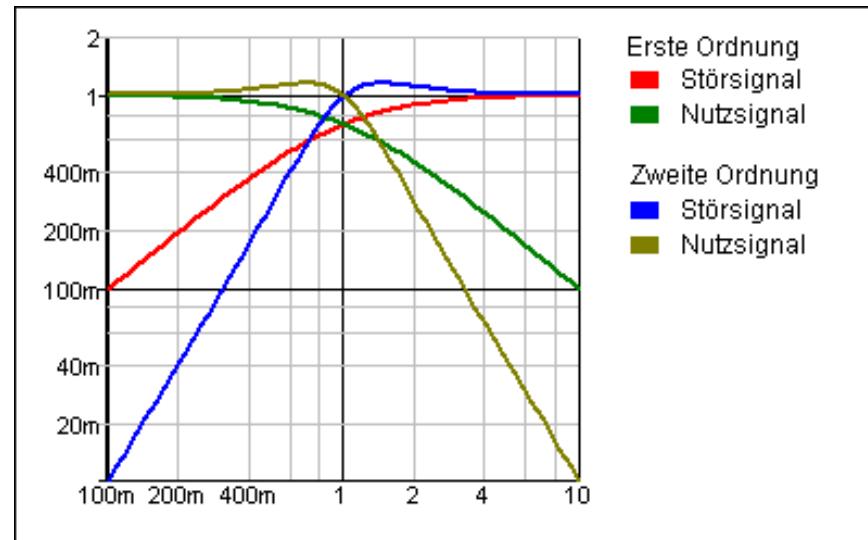
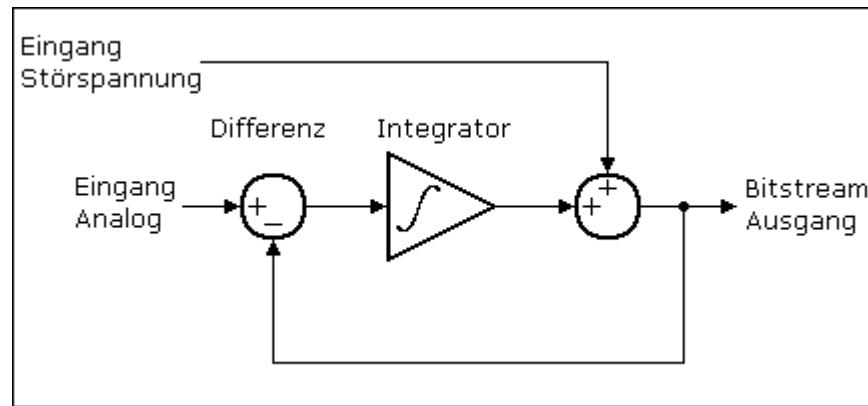
Signal forms

Trace the forms of signals in an analog first order modulator for a rectangular input signal:

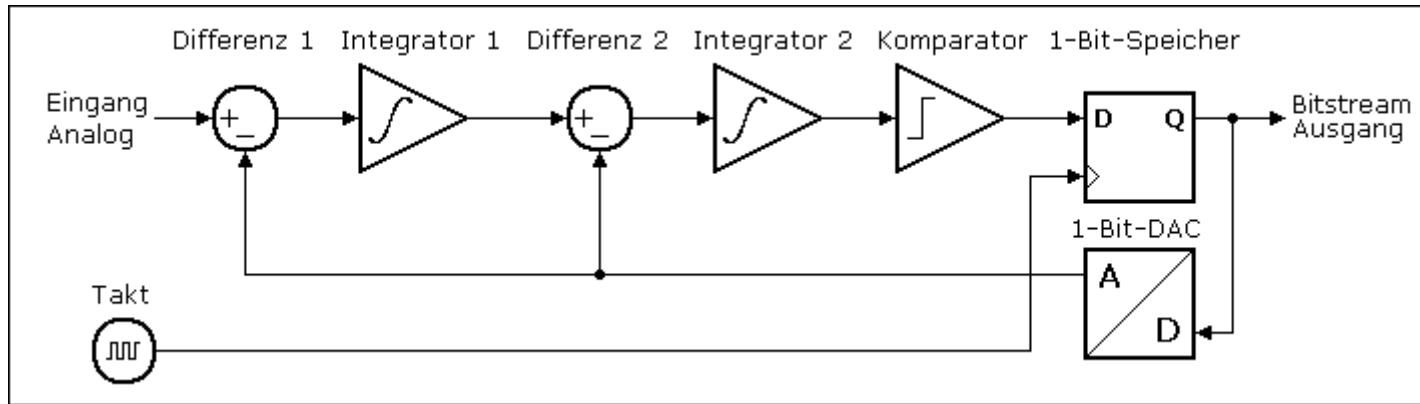


Retrace the
bitstream
after
decimation
by 8.

Dynamic behavior of the modulator

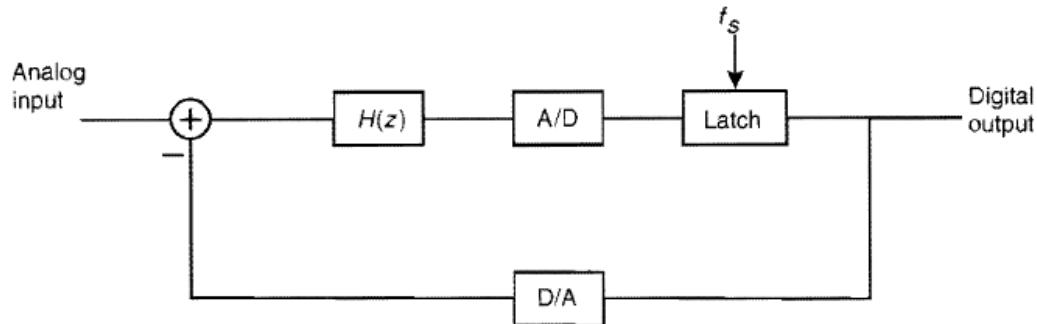


Second order modulator transfer functions

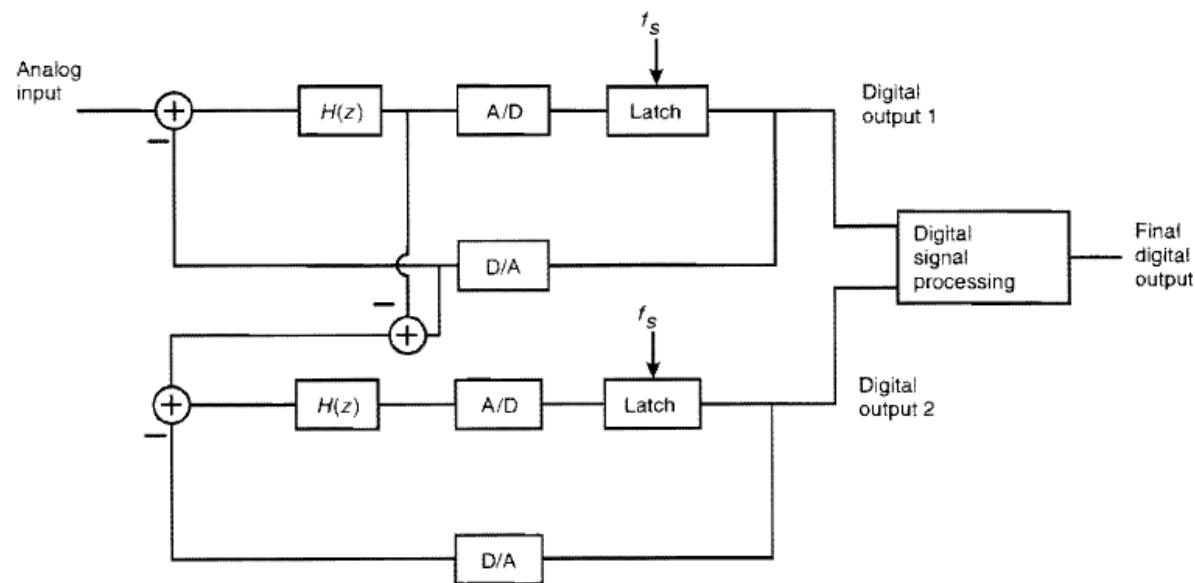


- Determine the equivalent continuous transfer functions of a second order delta-sigma modulator, for the signal and for the noise.
- Represent the corresponding amplitude responses in a Bode diagram.

Cascade of two first order demodulators

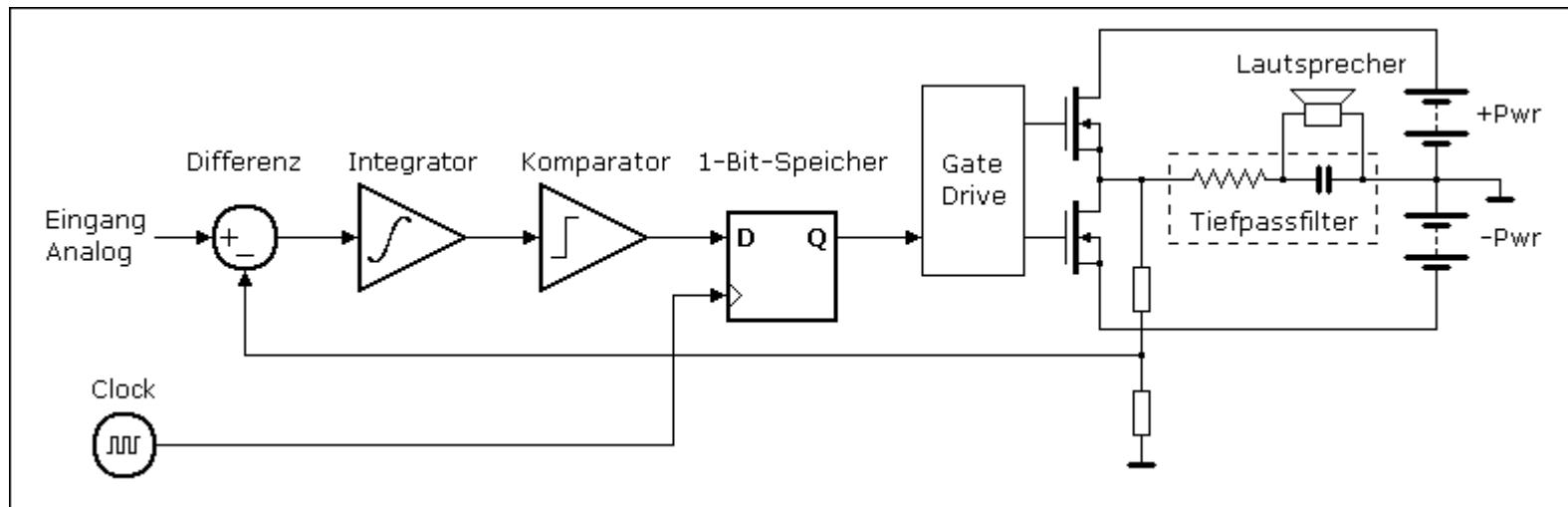


Block diagram of single-loop modulator.



Block diagram of cascaded modulator.

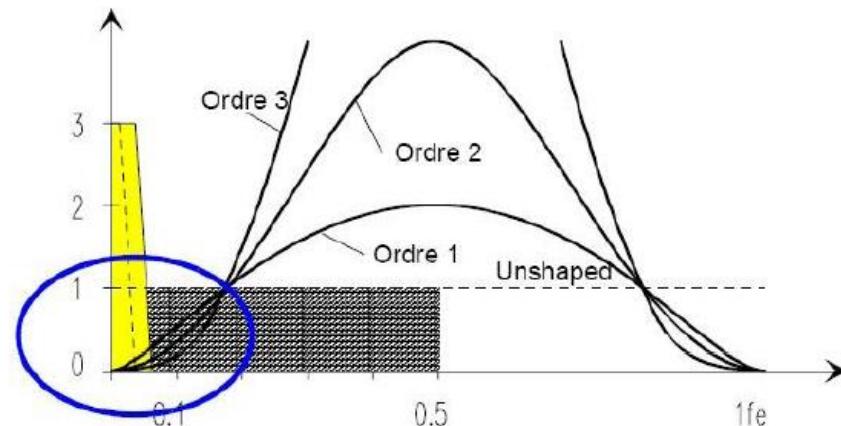
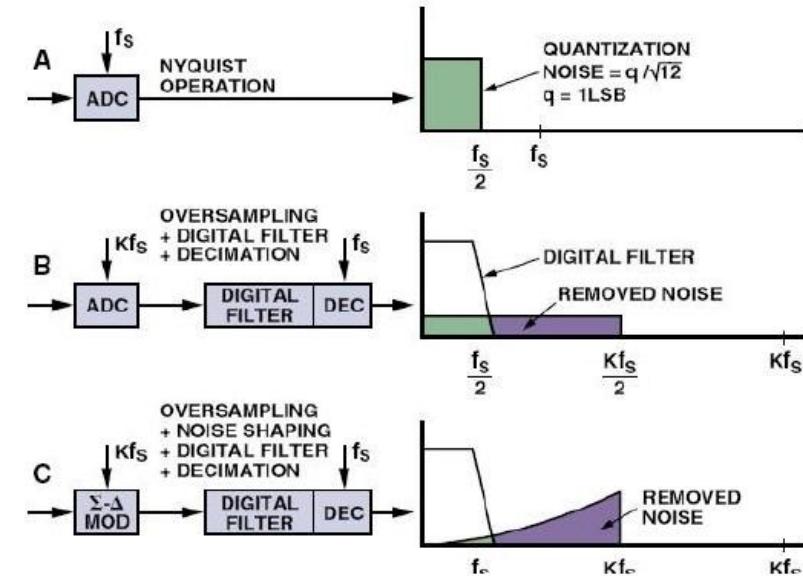
Power amplifier with digital output stage



Oversampling and delta-sigma modulation

⌘ Why S-D converters
are much better than
simple oversampled
systems?

- SD modulation use
Oversampling
(OSR : 32..512...)
and add a
noiseshaping:

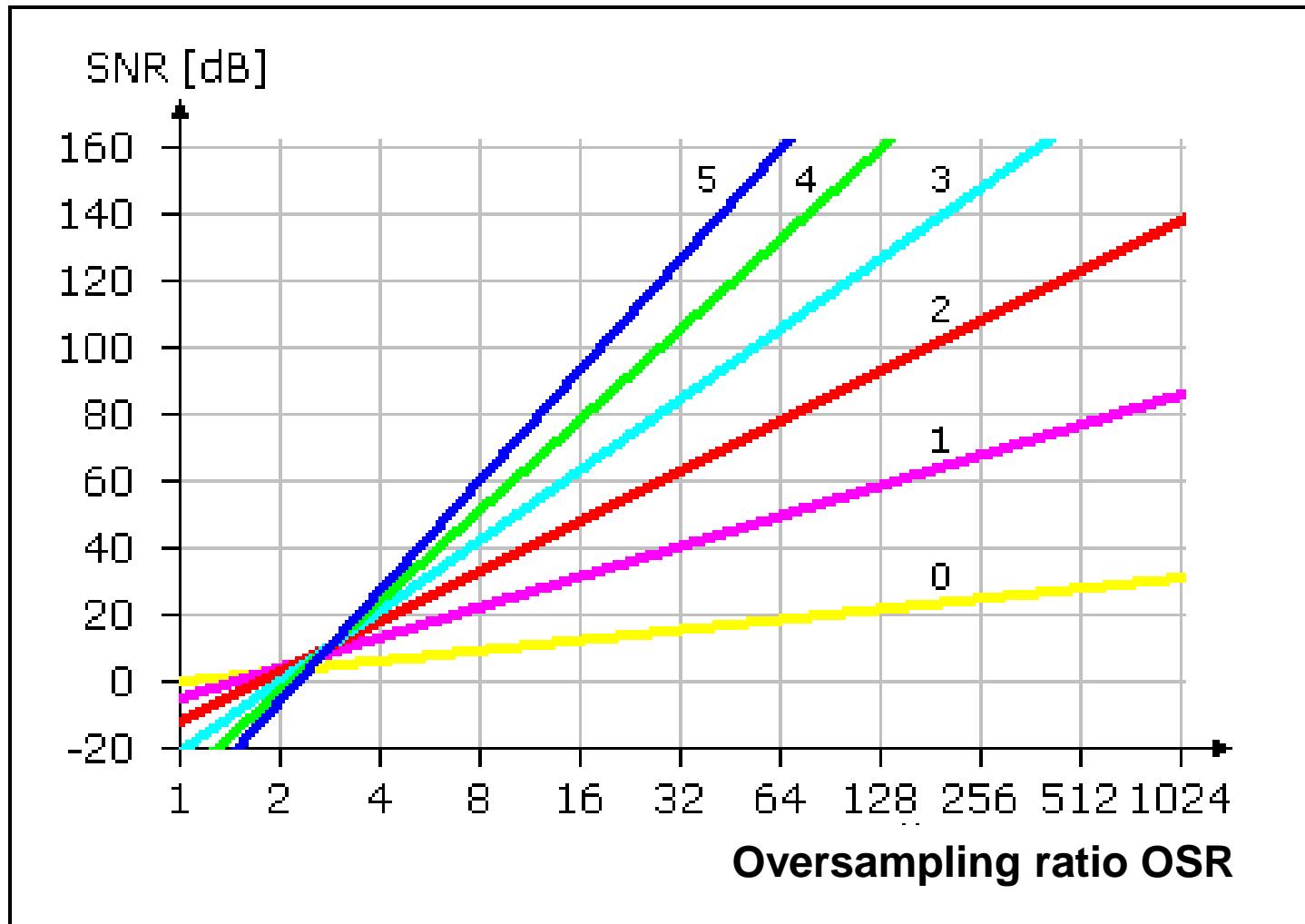


Influence of the order of delta-sigma modulation

⌘ SNR in Function of the order L & OSR :

| Order of modulator | 1 | 2 | 3 | L |
|---|---|---|---|--|
| Transfer $N(z)/E(z)$ | $1 - z^{-1}$ | $(1 - z^{-1})^2$ | $(1 - z^{-1})^3$ | $(1 - z^{-1})^L$ |
| Base band noise n_0 (Δ = quantisation step) | $\frac{\Delta\pi}{6} \sqrt{\left(\frac{1}{OSR}\right)^3}$ | $\frac{\Delta\pi^2}{\sqrt{60}} \sqrt{\left(\frac{1}{OSR}\right)^5}$ | $\frac{\Delta\pi^3}{\sqrt{84}} \sqrt{\left(\frac{1}{OSR}\right)^7}$ | $\frac{\Delta\pi^L}{\sqrt{12(2L+1)}} \sqrt{\left(\frac{1}{OSR}\right)^{2L+1}}$ |
| S/N | $\frac{9}{(2\pi)^2 \left(\frac{1}{OSR}\right)^3}$ | $\frac{15}{(2\pi)^4 \left(\frac{1}{OSR}\right)^5}$ | $\frac{21}{(2\pi)^6 \left(\frac{1}{OSR}\right)^7}$ | $\frac{3(2L+1)}{(2\pi)^{2L} \left(\frac{1}{OSR}\right)^{2L+1}}$ |

Signal to noise ratio versus oversampling ratio

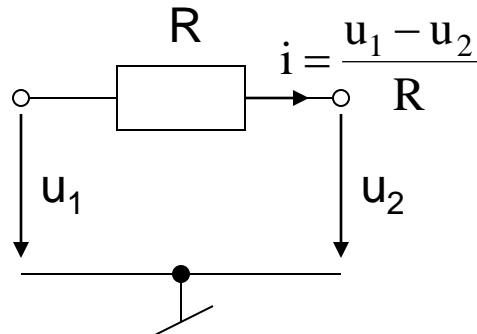


Signal to noise and oversampling ratios

- What is the maximum signal-to-noise ratio of a 16bit ADC? Suppose a sinusoidal input signal, and that the quantisation noise dominates all other noises. The noise is considered as white noise.
- Which resolution, expressed as number of bits (ENOB), can have an ADC with a second order delta-sigma modulator, operating at an oversampling ratio of 128?
- Consider a delta-sigma ADC with ENOB = 16bits and an input signal bandwidth of 1kHz. The oversampling ratio is 128. Which order is required for an analog anti-aliasing filter?

From the resistor to the switched capacitor

In integrated circuits, replacement of area consuming resistors with switched capacitors.



Definition of commutation intervals:

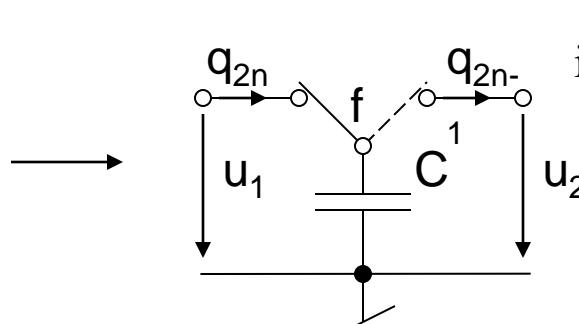
Charge transport

in the even interval:

in the odd interval:

if u_1 and u_2 are constant,

Average of current



even: $2nT-T \leq t \leq 2nT$

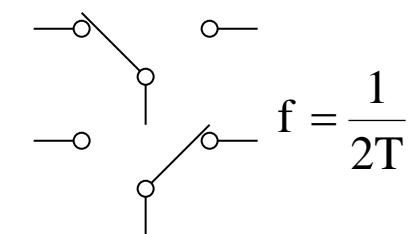
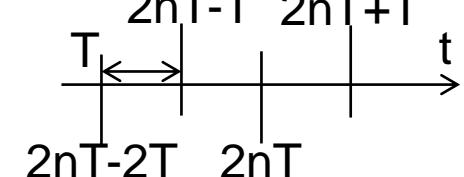
odd: $2nT-2T \leq t \leq 2nT-T$

$$q_{2n} = Cu_1(2nT) - Cu_2(2nT - T)$$

$$q_{2n-1} = Cu_1(2nT - 2T) - Cu_2(2nT - T)$$

$$q_{2n} = q_{2n-1} = q = C(u_1 - u_2)$$

$$I = \frac{q}{2T} = \frac{C}{2T}(u_1 - u_2) = Cf(u_1 - u_2)$$



Integrator with switched capacitor

Analysis method:

- 1) Number nodes (here 1, 2, 3)
- 2) Establish charge equilibria of inner nodes (here only 3)

- even circuit:

$$C(u_2(2nT) - u_3(2nT)) = C(u_2(2nT - T) - u_3(2nT - T)) \\ u_3 \equiv 0 \Rightarrow u_2(2nT) = u_2(2nT - T)$$

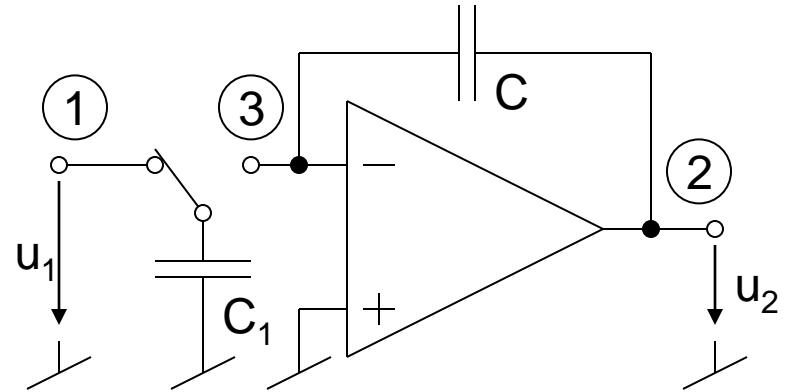
- odd circuit:

$$C(u_2(2nT - T) - u_3(2nT - T)) + C_1(0 - u_3(2nT - T)) = \\ = C(u_2(2nT - 2T) - u_3(2nT - 2T)) + C_1(0 - u_1(2nT - 2T)) \\ u_3 \equiv 0 \Rightarrow Cu_2(2nT - T) = Cu_2(2nT - 2T) - C_1u_1(2nT - 2T)$$

3) Put in relation the start of an odd with the end of an even interval

4) z-transform

$$Cu_2(2nT) = Cu_2(2nT - 2T) - C_1u_1(2nT - 2T) \\ CU_2(z) = CU_2(z)z^{-1} - C_1U_1(z)z^{-1} \Rightarrow \frac{U_2(z)}{U_1(z)} = -\frac{C_1}{C} \frac{1}{z-1}$$



Parasitic capacitances

Parasitic capacitances appear in all circuits.

Circuits that are insensitive to parasitic capacitances, have the following 4 properties:

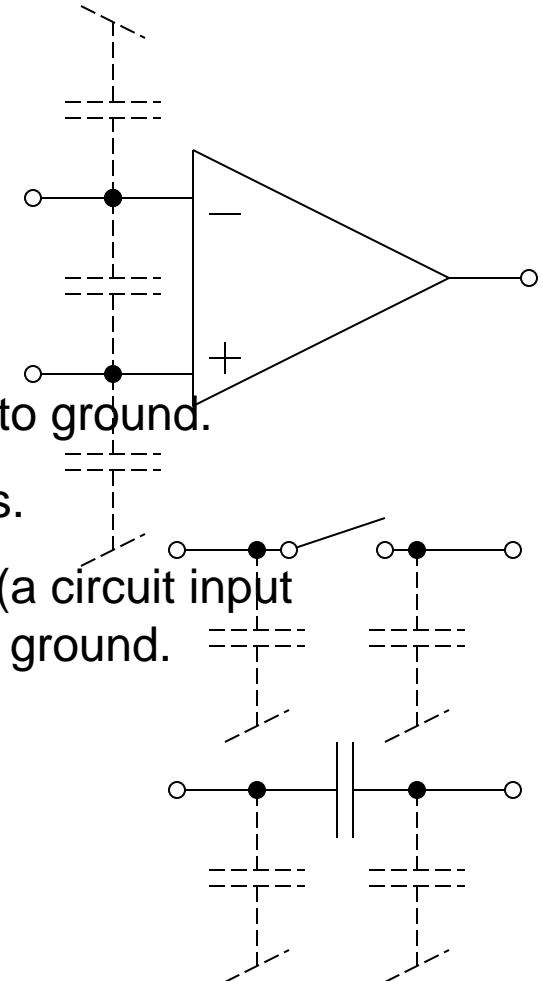
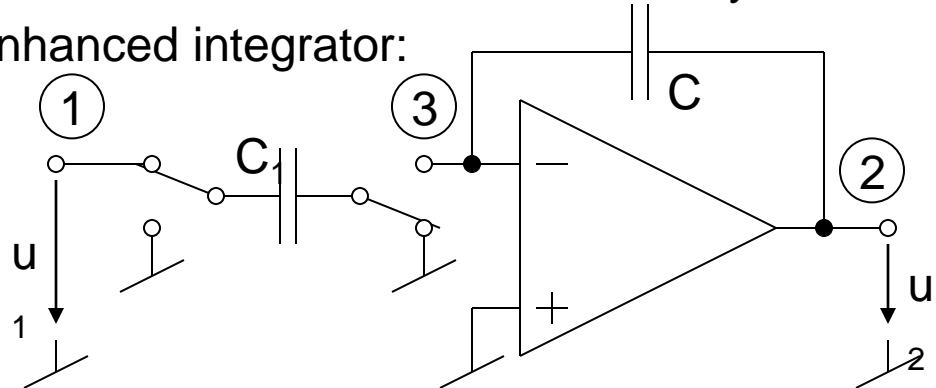
- Operational amplifiers have one input connected to ground.

- There is no node that connects only to capacitors.

- No commutations occur between a voltage node (a circuit input or an output of an operational amplifier) and virtual ground.

- There is no node that connects only to switches.

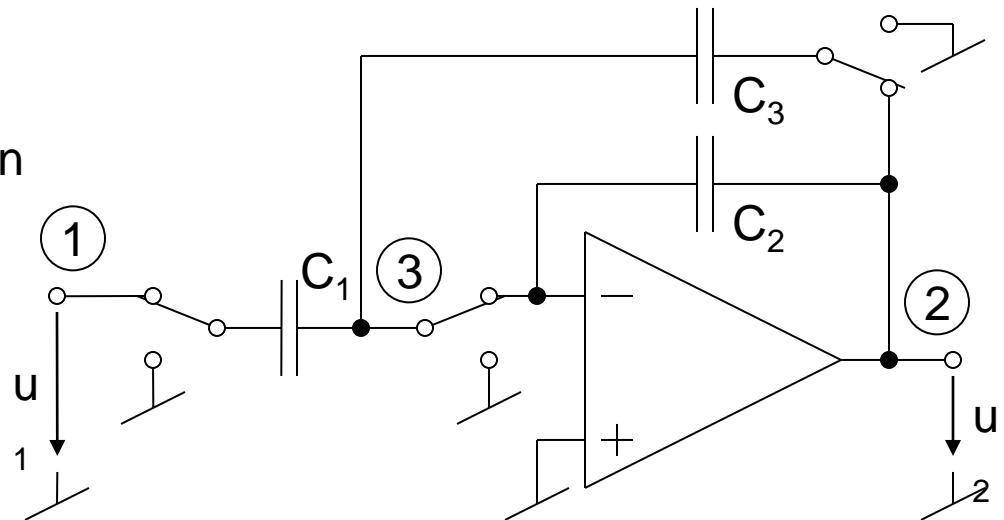
Enhanced integrator:



$$\frac{U_2(z)}{U_1(z)} = + \frac{C_1}{C} \frac{1}{z - 1}$$

First order low pass filter

Position of switches shown
is for the even interval.



- even circuit:

$$\begin{aligned} & C_1(u_{1,2nT} - u_{3,2nT}) + (C_2 + C_3)(u_{2,2nT} - u_{3,2nT}) = \\ & = C_1(0 - u_{3,2nT-T}) + C_2(u_{2,2nT-T} - 0) + C_3(0 - u_{3,2nT-T}) \end{aligned}$$

$$u_{3,2nT} = u_{3,2nT-T} \equiv 0 \Rightarrow C_1 u_{1,2nT} + (C_2 + C_3) u_{2,2nT} = C_2 u_{2,2nT-T}$$

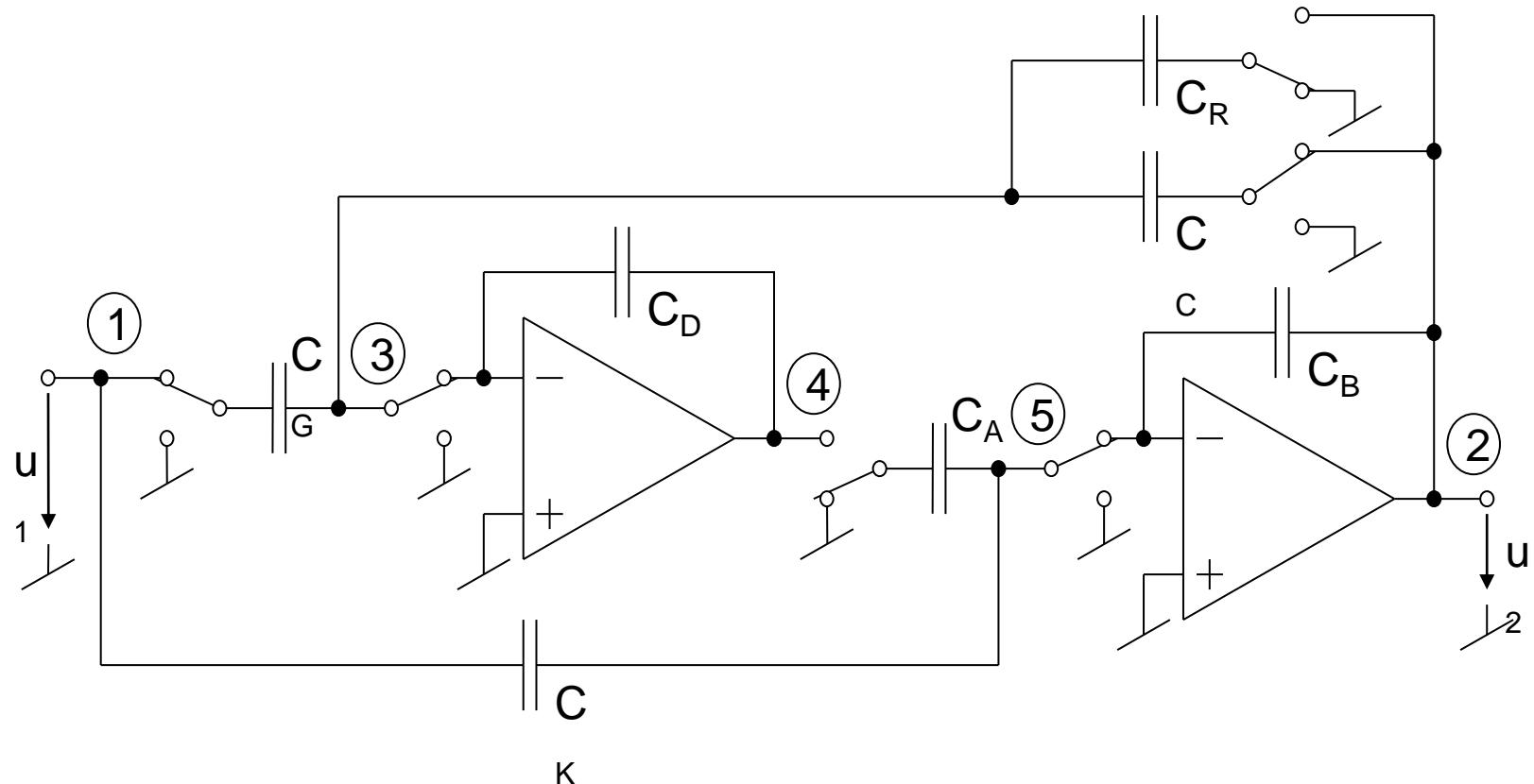
- odd circuit:

$$\begin{aligned} & u_{2,2nT-T} = u_{2,2nT-2T} \\ & C_1 U_1(z) + (C_2 + C_3) U_2(z) = C_2 U_2(z) z^{-1} \end{aligned}$$

- transfer function:

$$\frac{U_2(z)}{U_1(z)} = \frac{C_1}{C_2 z^{-1} - C_2 - C_3}$$

Second order low pass filter (1)



Position of switches shown is for the even interval.

Second order low pass filter (2)

-Even circuit:

Node ③

$$\begin{aligned} C_G(u_{1,2nT} - u_{3,2nT}) + C_D(u_{4,2nT} - u_{3,2nT}) + C_C(u_{2,2nT} - u_{3,2nT}) + C_R(0 - u_{3,2nT}) &= \\ = C_G(0 - u_{3,2nT-T}) + C_D(u_{4,2nT-T} - u_{3,2nT-T}) + C_C(0 - u_{3,2nT-T}) + C_R(u_{2,2nT-T} - 0) \\ u_{3,2nT} = u_{3,2nT-T} \equiv 0 \Rightarrow C_G u_{1,2nT} + C_D u_{4,2nT} + C_C u_{2,2nT} &= C_D u_{4,2nT-T} + C_R u_{2,2nT-T} \end{aligned}$$

Node ⑤

$$\begin{aligned} C_A(0 - u_{5,2nT}) + C_B(u_{2,2nT} - 0) + C_K(u_{1,2nT} - u_{5,2nT}) &= \\ = C_A(u_{4,2nT-T} - 0) + C_B(u_{2,2nT-T} - u_{5,2nT-T}) + C_K(u_{1,2nT-T} - 0) \\ u_{5,2nT} = u_{5,2nT-T} \equiv 0 \Rightarrow C_B u_{2,2nT} + C_K u_{1,2nT} &= C_A u_{4,2nT-T} + C_B u_{2,2nT-T} + C_K u_{1,2nT-T} \end{aligned}$$

- Odd circuit: $u_{2,2nT-T} = u_{2,2nT-2T}$, $u_{4,2nT-T} = u_{4,2nT-2T}$

Assumption: $u_{1,2nT-T} = u_{1,2nT-2T}$ (S & H in front of the filter)

- Transfer function:

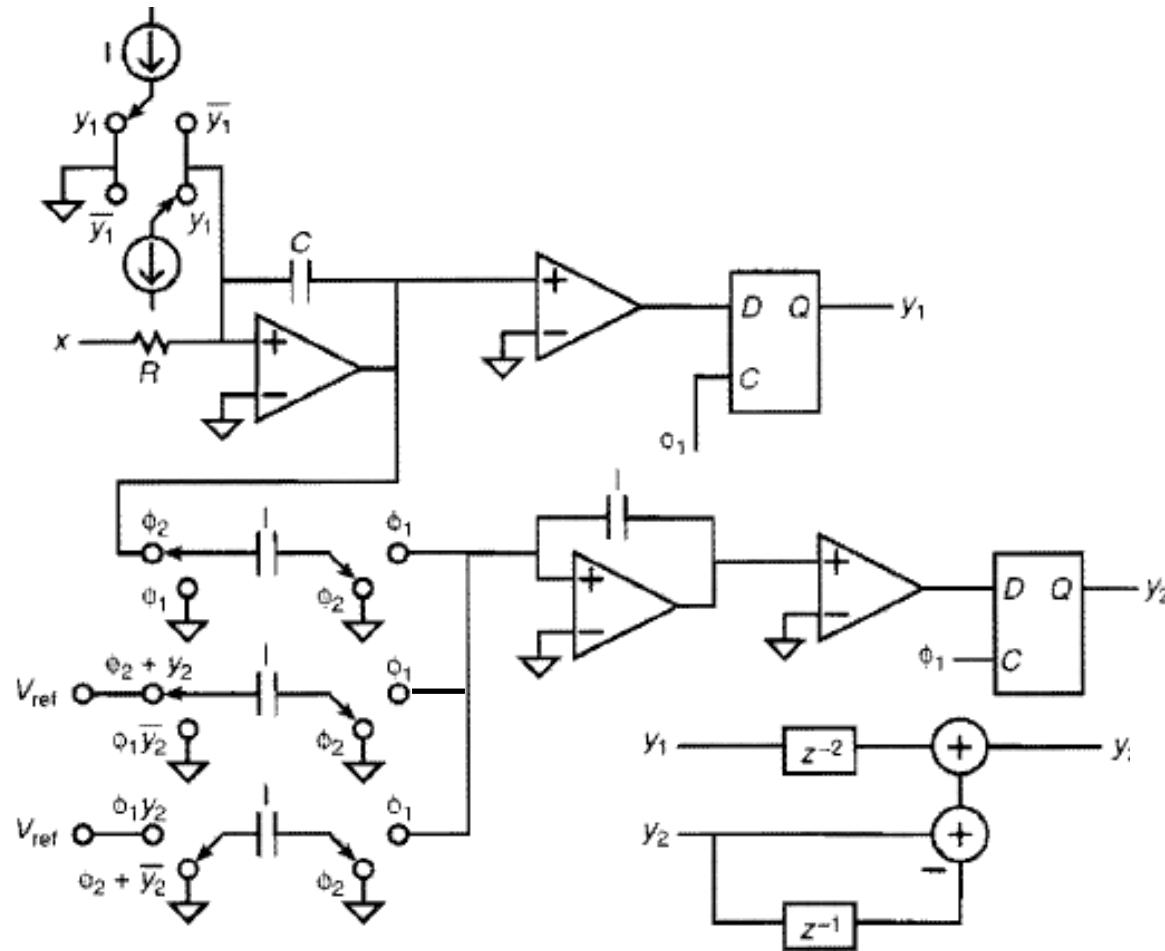
place ⑤ in ③ to
eliminate $u_4 \Rightarrow$

$$\frac{U_2(z)}{U_1(z)} = -\frac{C_K}{C_B} \frac{z^2 + \left(\frac{C_A C_G}{C_D C_K} - 2\right)z + 1}{z^2 + \left(\frac{C_A C_C}{C_B C_D} - 2\right)z + 1 - \frac{C_A C_R}{C_B C_D}}$$

Second order high pass filters

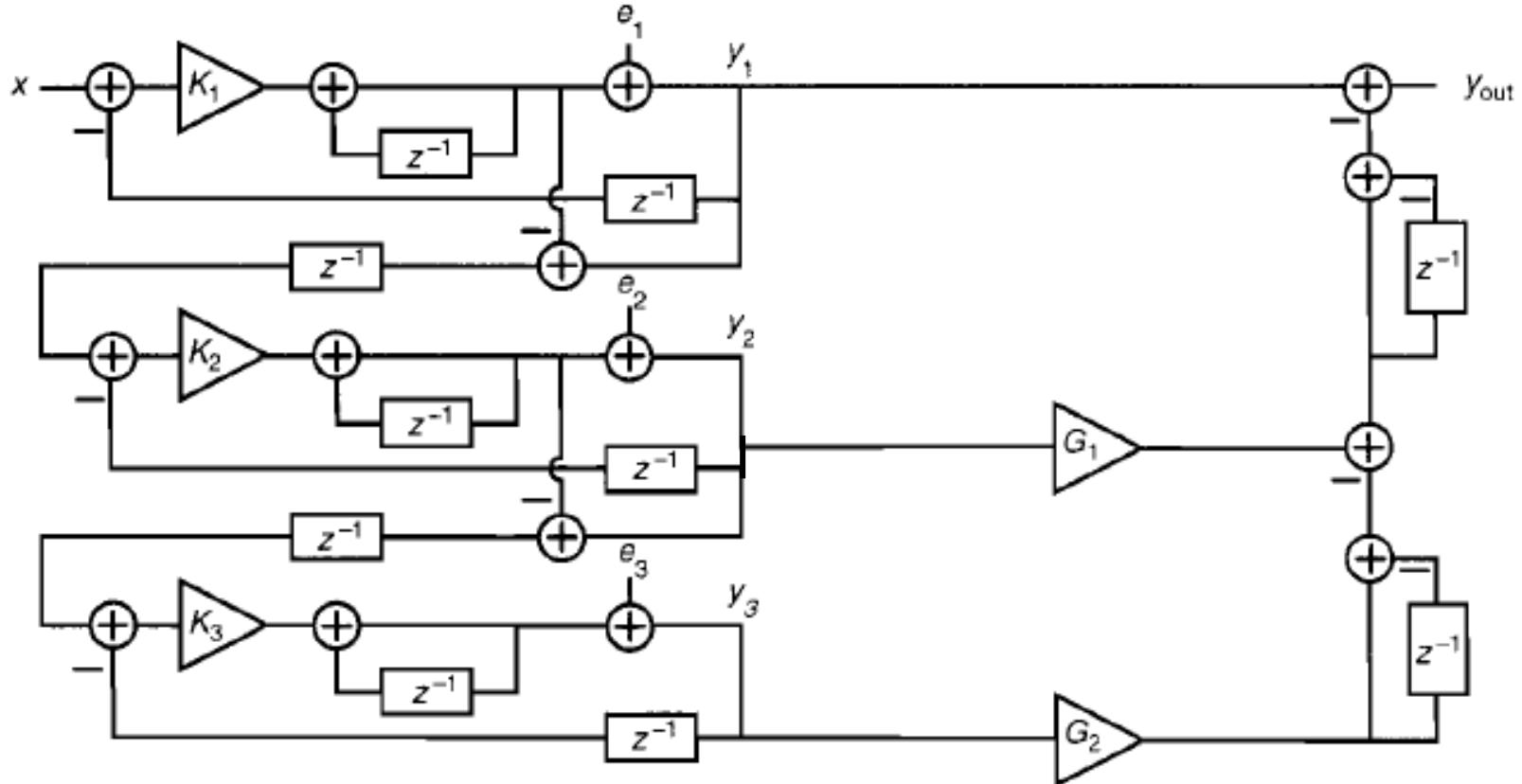
- Propose circuits for second order switched capacitor high-pass filters.

Cascaded second order modulator circuit



A (1-1) cascade, with continuous-time first modulator.

Cascaded third order modulator structure



- Develop the difference equation relating y_{out} to x , to e_1 , e_2 and e_3 .
- Estimate the frequency response of y_{out} excited by x , and the noise spectrum of y_{out} , assuming white noise inputs e_1 , e_2 , e_3 .
- Represent your results in graphs.

Cascaded third order modulator circuit

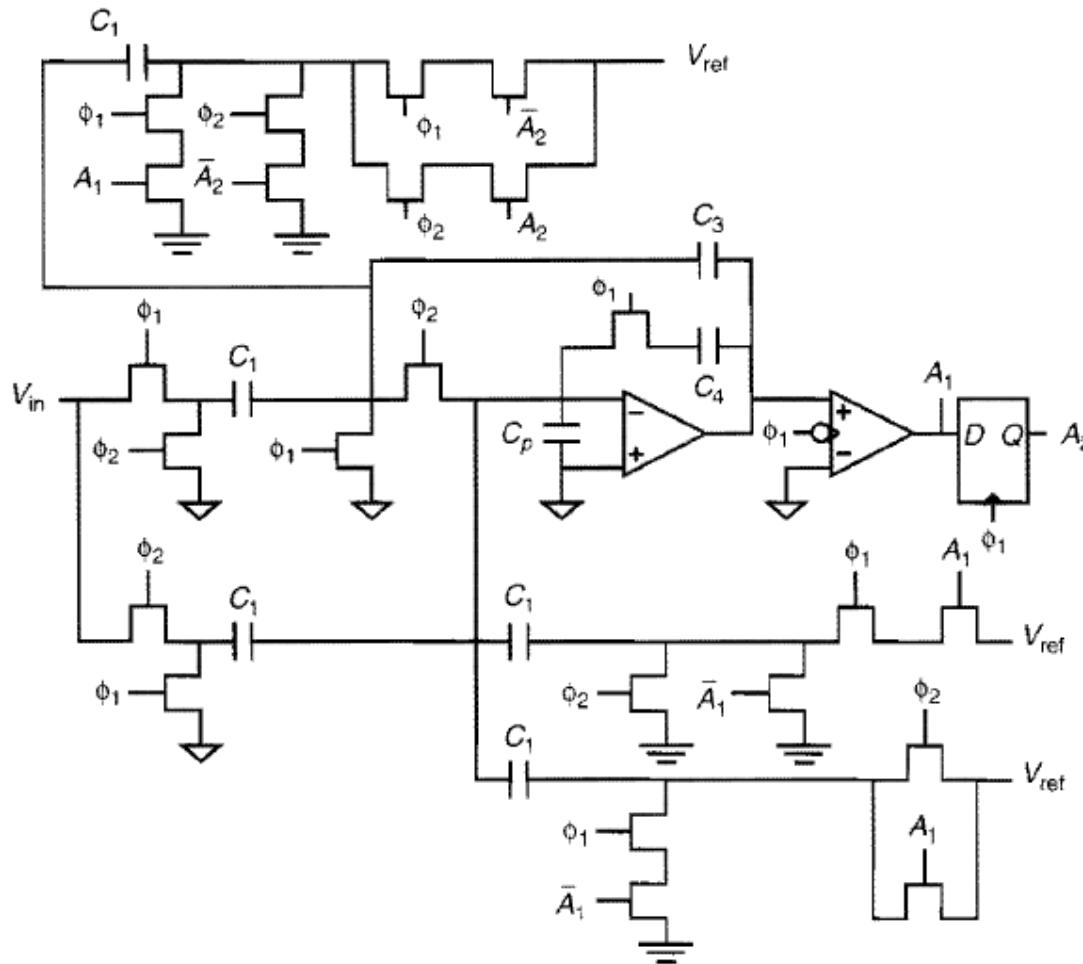


Figure 6.10 First modulator in third-order (1-1-1) cascade.

- Explain the operation of this circuit: Divide it into functional blocks. Draw a chronogram of its operation, with non-overlapping antiphase clocks Φ_1 , Φ_2 , and signals A_1 , A_2 and their inverses.

References

U. Beis: *Eine Einführung in Delta-Sigma-Wandler*,
http://www.beis.de/Elektronik/DeltaSigma/DeltaSigma_D.html

This reference was used as a basis for the present presentation, several illustrations are taken from it.

R. Schreier, G. C. Temes: *Understanding Delta-Sigma Data Converters*, IEEE Press 2004, ISBN 0-4714-6585-2

R. Norsworthy, R. Schreier, G. C. Temes: *Delta-Sigma Data Converters*, IEEE Press 1996, ISBN 0-7803-1045-4

Tietze, Schenk: *Halbleiter-Schaltungstechnik*, Springer 2010 (13th ed.), ISBN 3-540-64192-0

Chapitre 1

Digital Timing Analysis MA-AdvEIDes

Pietro Buccella

A. A. 2021/22



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Objectives

Objectives of the lesson:

- Know the different timing parameters of logic circuits
- Understand the concepts and arithmetic behind digital logic circuitry timing analysis
- Calculate the maximum operating clock frequency of a digital circuit
- Use LTspice® software to perform timing analysis of simple logic gates

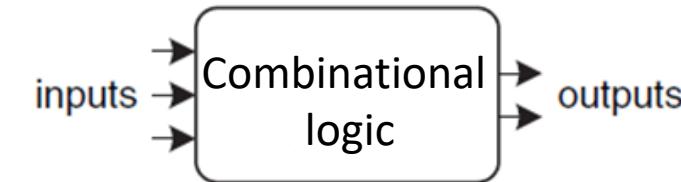
Contents

- Logic Circuits: Combinational and Sequential
- Transient Behaviour of Logic Circuits
- Timing Parameters for Combinational Logic
- Timing Parameters for Synchronous Sequential Logic
- Timing Analysis of Synchronous Sequential Logic: Setup and Hold Time Constraints
- Timing Analysis – Inside a Component (FPGA/ASIC)
- Delays – where do they come from
- Exercises

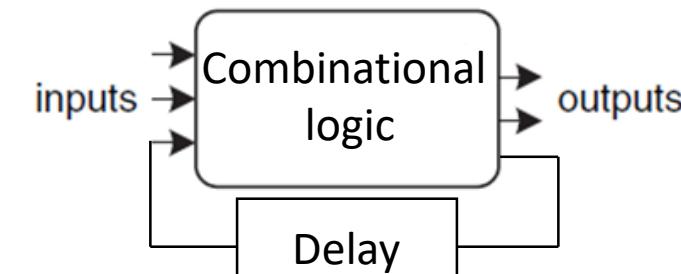
Logic Circuits

- **Combinational logic:** The outputs depend only on current input values
- **Sequential logic:** The outputs depend on both current and prior input values → Combinational logic + Memory elements
- **Sequential logic:** Synchronous Sequential and Asynchronous Sequential Circuits
- Asynchronous circuits: An un-clocked flip flop or time delay element acts as memory element
- Synchronous circuits: A clocked flip flop acts as memory element; the status of memory element is affected only at the active edge of clock, if input is changed

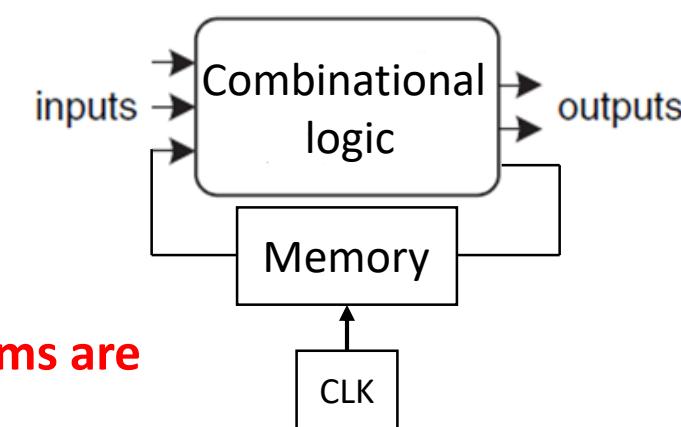
Combinational
logic



Asynchronous
logic



Synchronous
logic

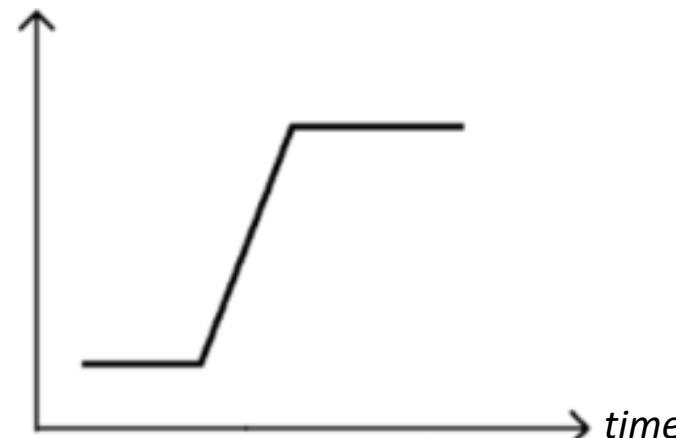


Virtually all digital sequential systems are
synchronous

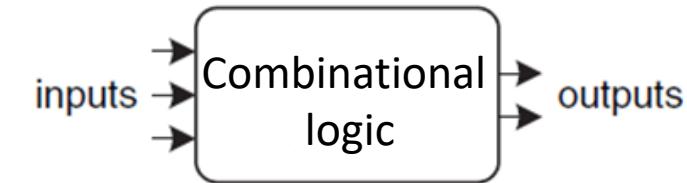
Transient Behaviour of Logic Circuits

How do signal of digital circuits evolve from one value to the next?

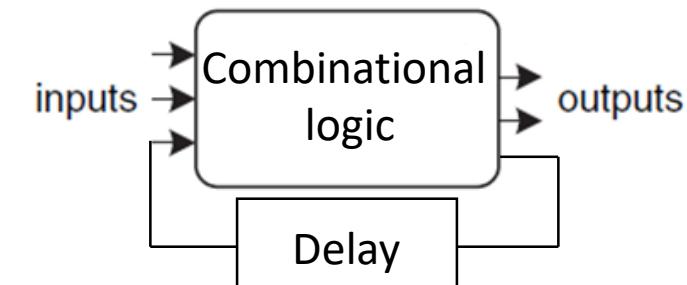
- *Ideal case: a logic signal varies between a low and a high signal level in monotonic ramp*



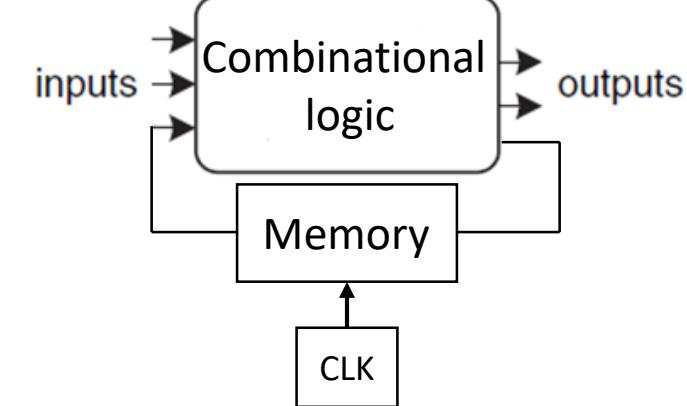
Combinational logic



Asynchronous logic



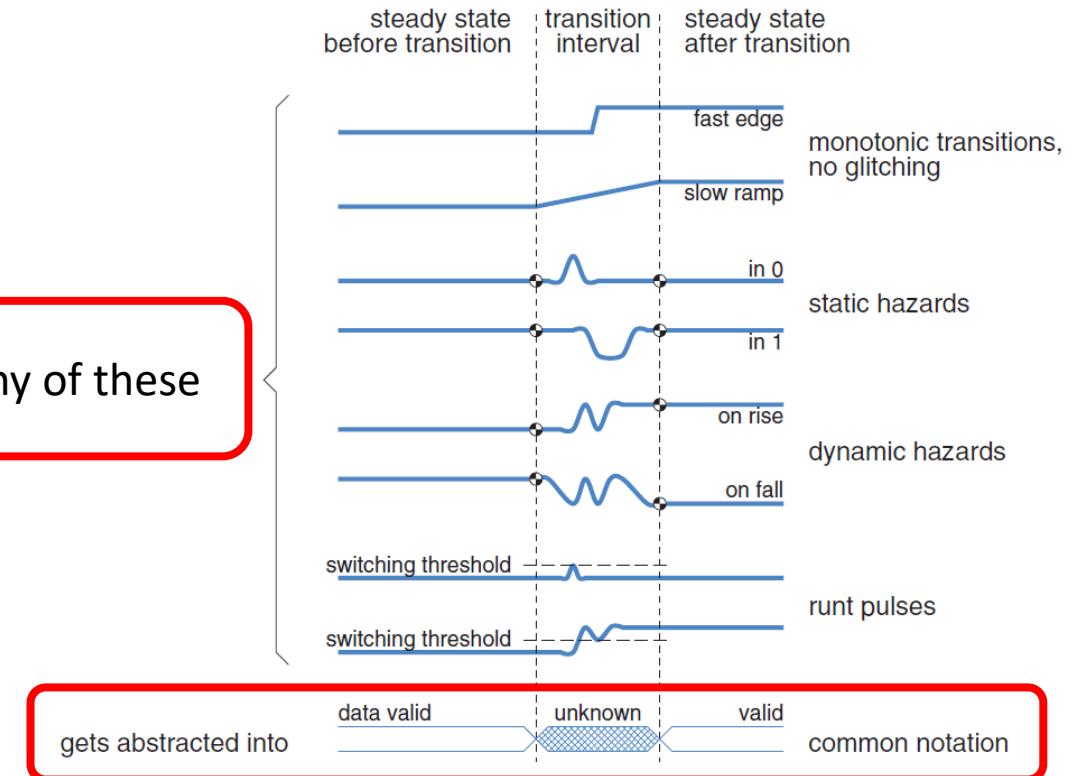
Synchronous logic



Transient Behaviour of Logic Circuits

How do the outputs of digital circuits evolve from one value to the next?

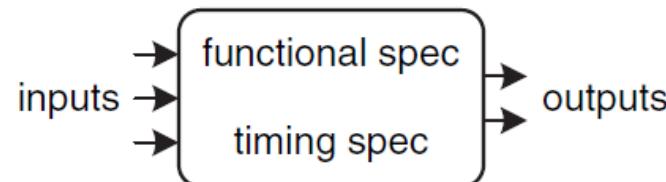
- *Real case* → Any of these



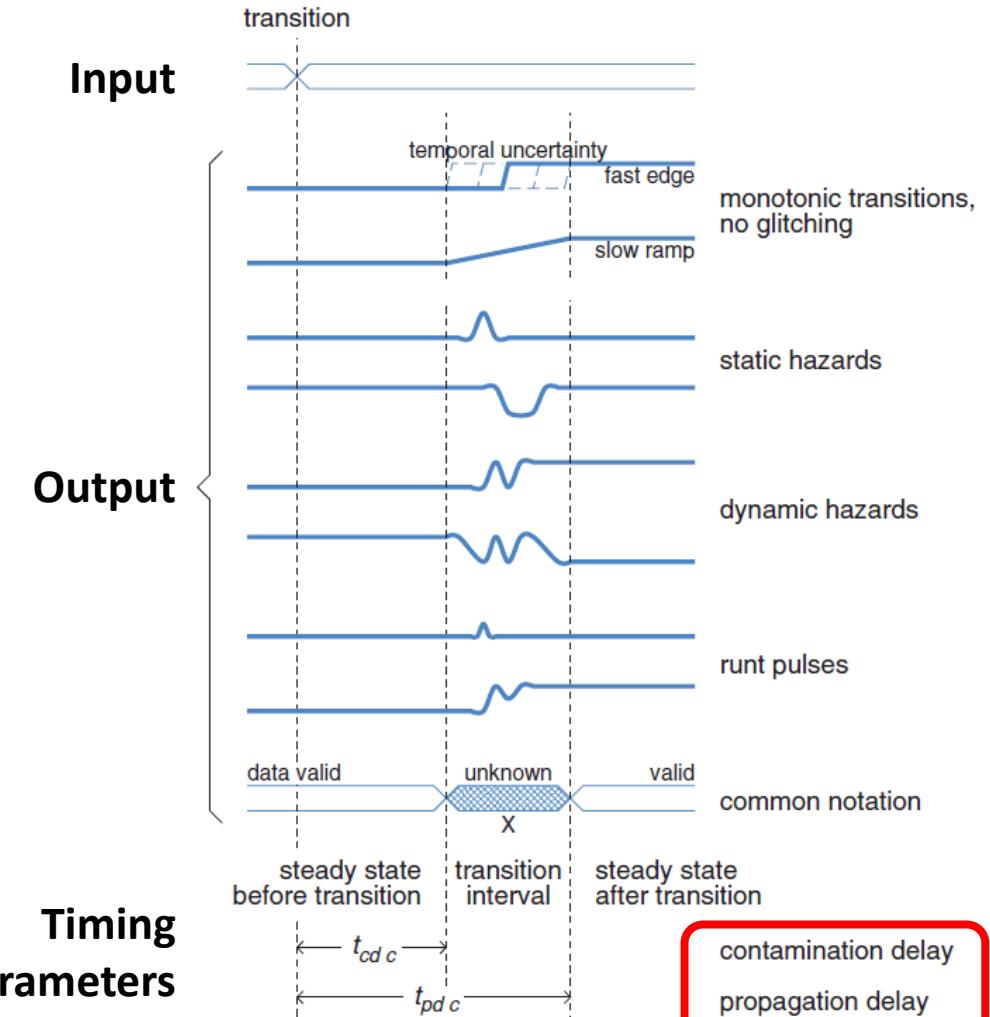
Transient Behaviour of Logic Circuits

How long transient phenomena persist at the output of a digital circuit in response to a change at one of the circuit's inputs?

- it takes a pair of **Timing Parameters** :
 - Contamination delay: t_{cd}
 - Propagation delay: t_{pd}



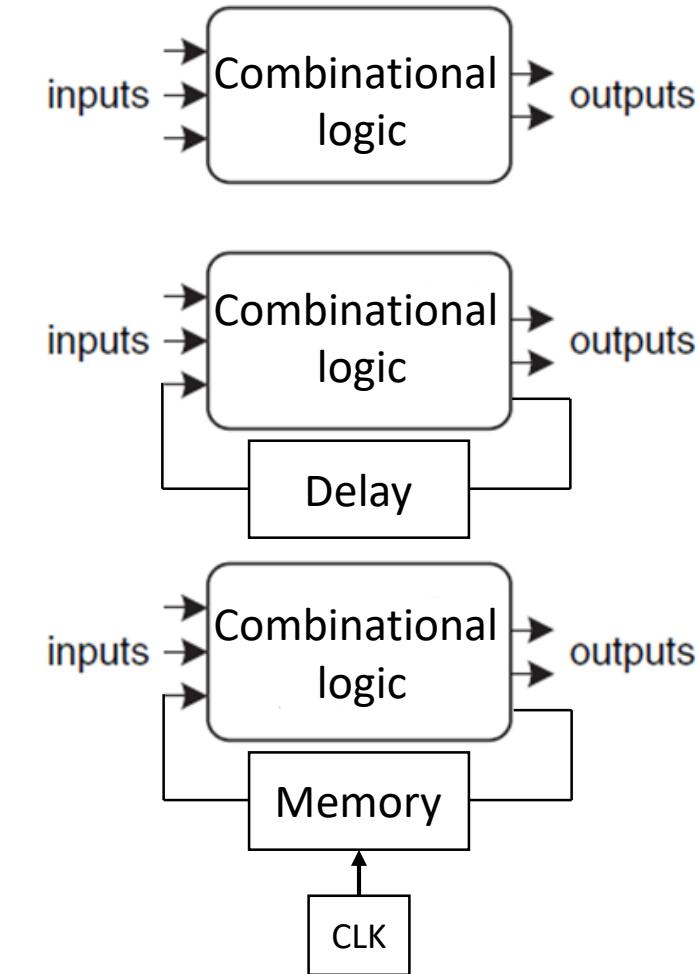
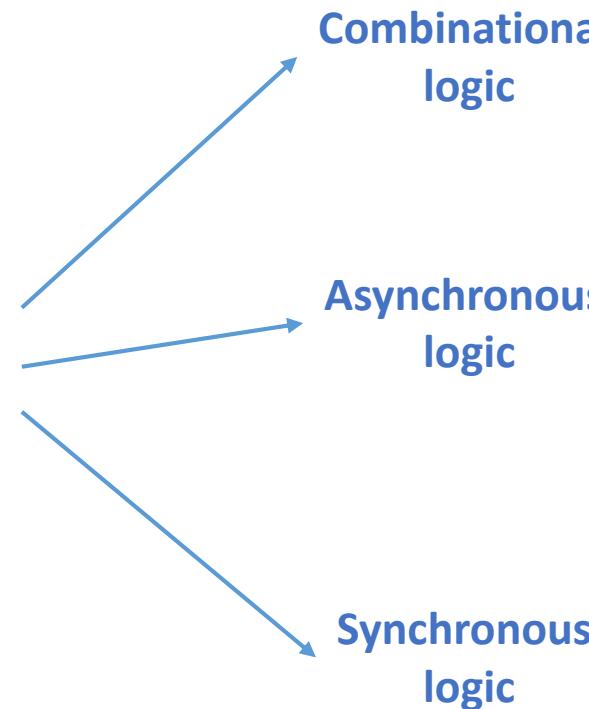
Timing parameters



Transient Behaviour of Logic Circuits

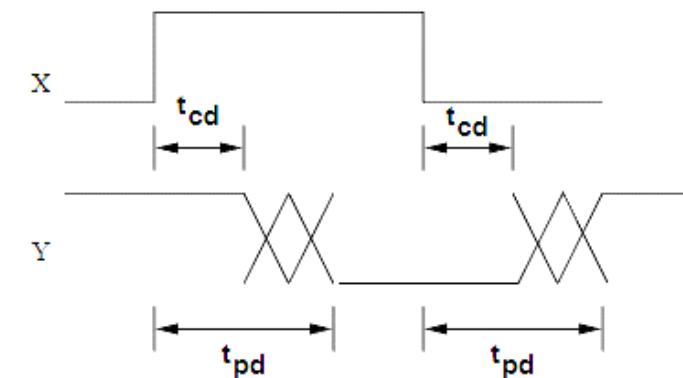
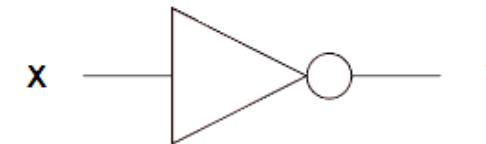
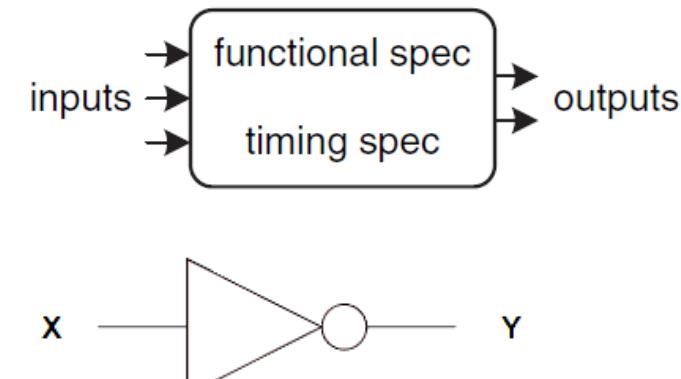
Timing Parameters :

- Contamination delay: t_{cd}
- Propagation delay: t_{pd}



Timing Parameters for Combinational Logic

- When a binary value is applied at the input to a combinational circuit, the change at the circuit output is not instantaneous
- Input-to-output delay in combinational circuits is expressed with two parameters, t_{pd} and t_{cd}

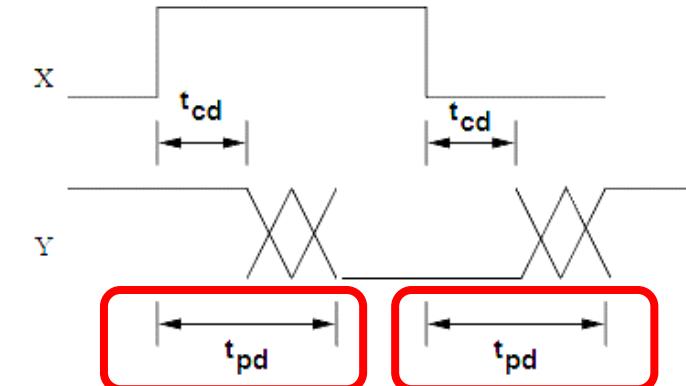
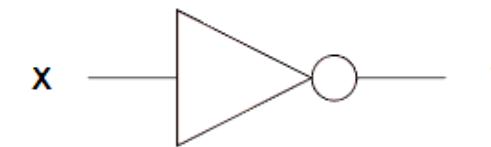


Timing Parameters for Combinational Logic

Propagation Delay t_{pd}

- amount of time needed for a change in a logic input to drive a permanent change at an output

For combinational logic no output changes in response to an input change after t_{pd} time passed

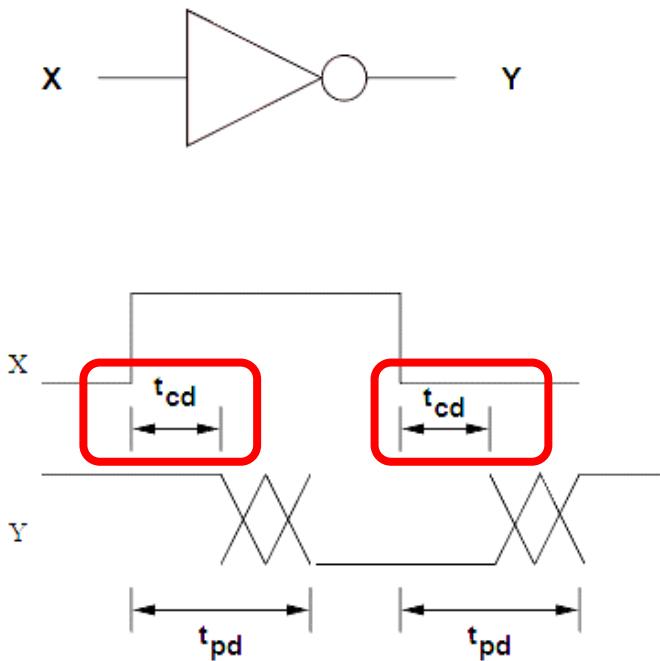


Timing Parameters for Combinational Logic

Contamination Delay t_{cd} :

- amount of time required for a change in a logic input to drive an initial change in an output

Combinational logic is guaranteed not to show any output change in response to an input change before t_{cd} time units have passed



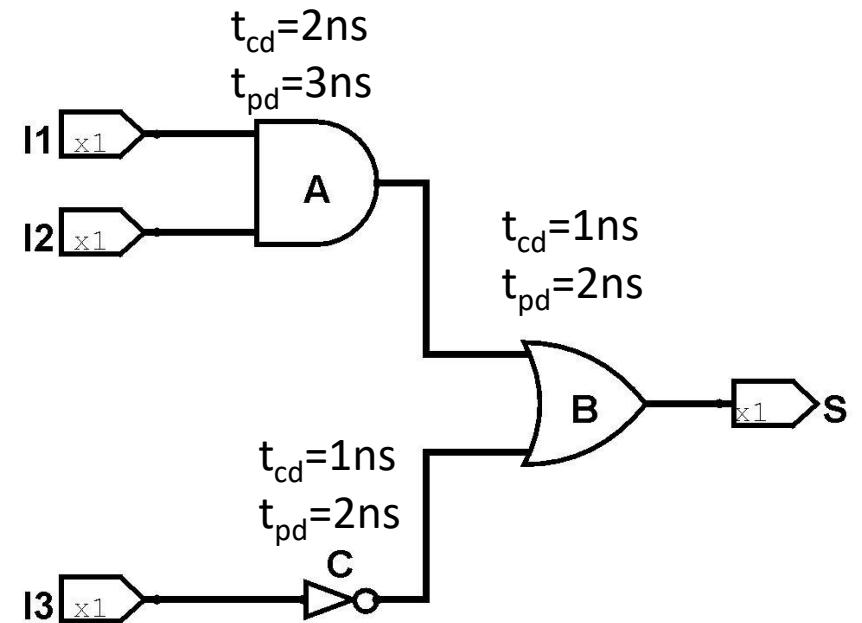
Timing of Combinational Logic : exercise 1

1. Determine the total t_{pd} of such combinational circuit:

- identify the longest path
- $t_{pd} =$

2. Determine the total t_{cd} of such combinational circuit:

- identify the shortest path
- $t_{cd} =$



Timing Parameters for Synchronous Sequential Logic: Clock Signal

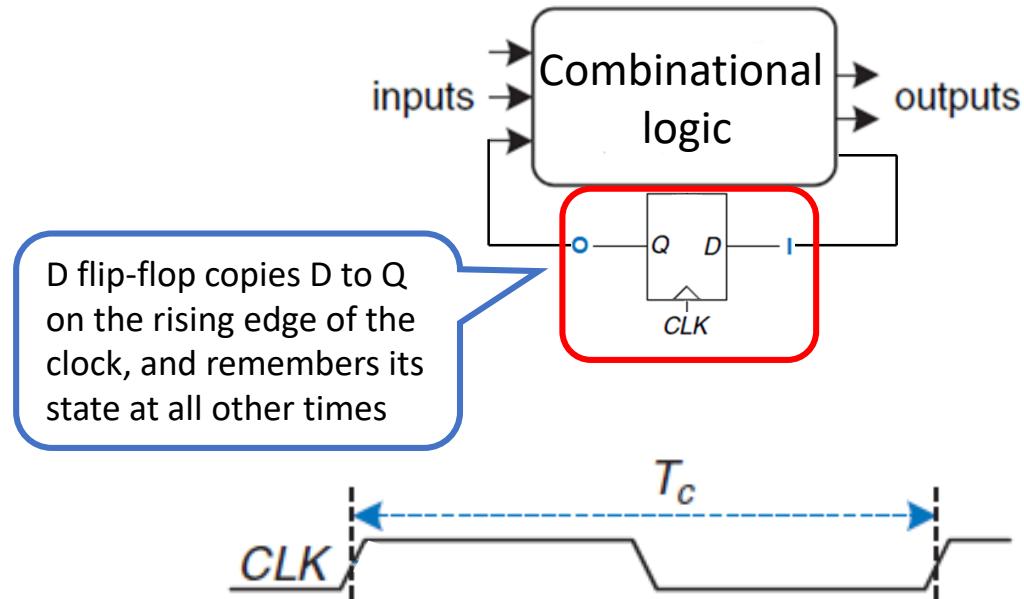
Synchronous circuits: A flip flop acts as memory element, such as the edge-triggered D flip flop controlled by the **clock signal**, CLK

Clock signal is a periodic square wave between logic high ("1") and logic low ("0")

- The amount of time between rising clock edges: **clock period**, T_c
- The inverse of the clock period ($1/T_c$) is the **clock frequency**, f_c .

f_c measures how often the data is transferred into edge-triggered flip flops:

↑clock frequency → data stored more quickly → sequential circuit generates results at a faster rate



Timing Parameters for Synchronous Sequential Logic: D Flip-Flop

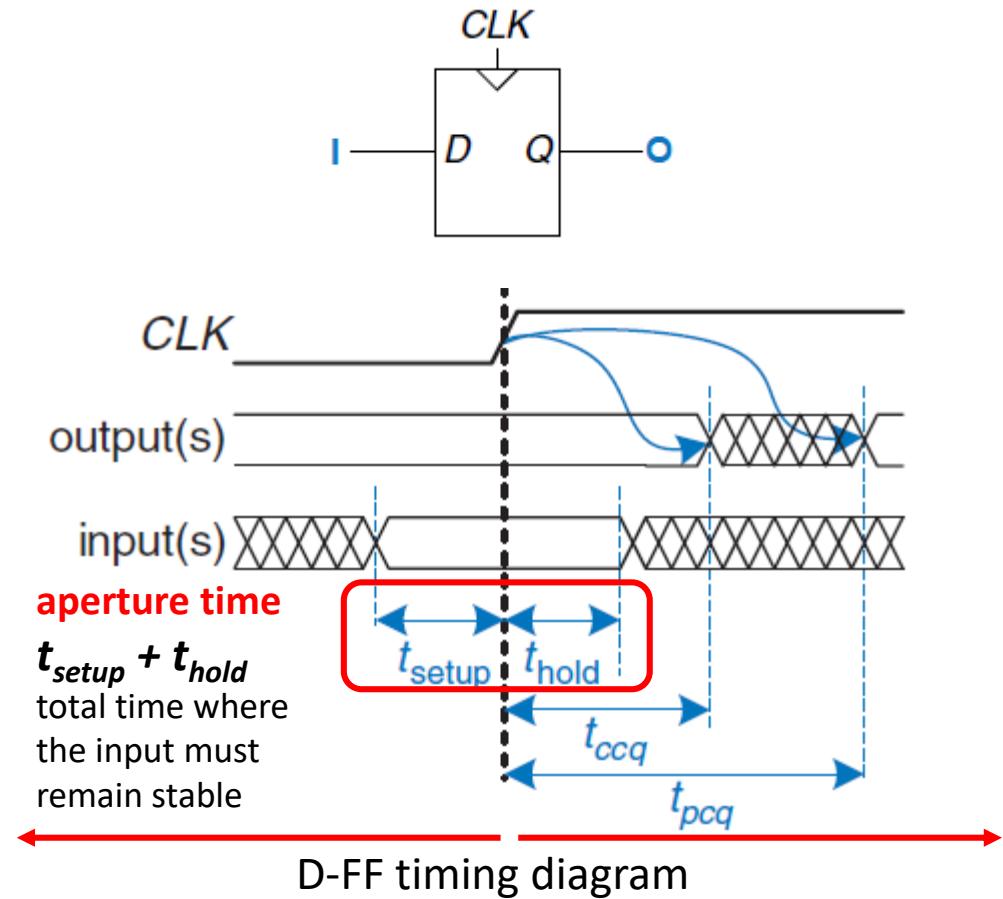
Requirement, flip-flop signals must be sampled while they are not changing:

Before clock rising edge:

- the input must have stabilized at least some **setup time**, t_{setup}

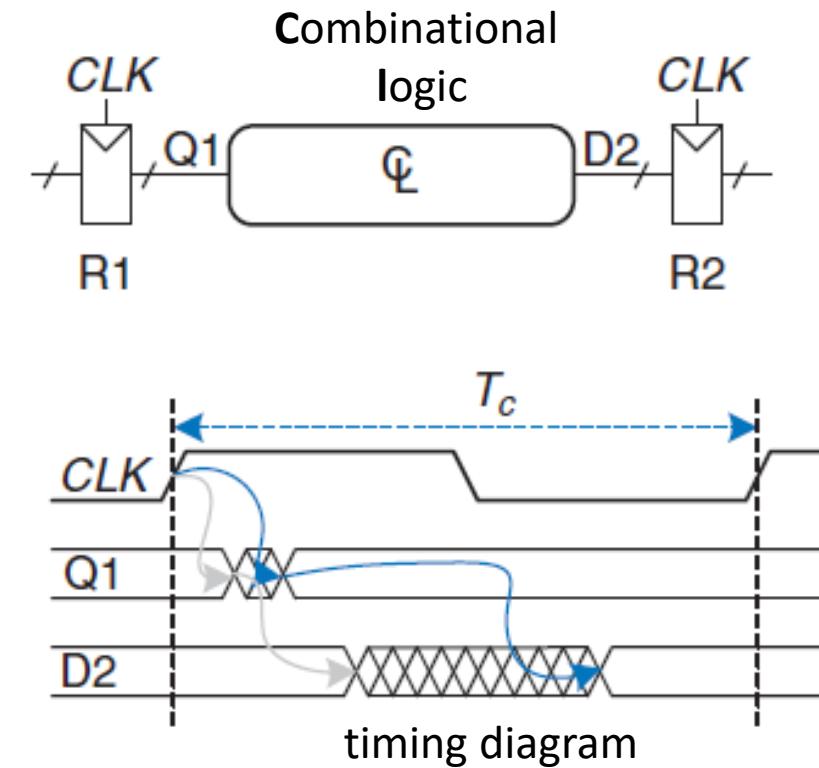
After clock rising edge:

- the input must remain stable for at least some **hold time**, t_{hold}
- the output may start to change after the **clock-to-Q contamination delay**, t_{ccq}
- the output must definitely settle to the final value within the **clock to-Q propagation delay**, t_{pcq}

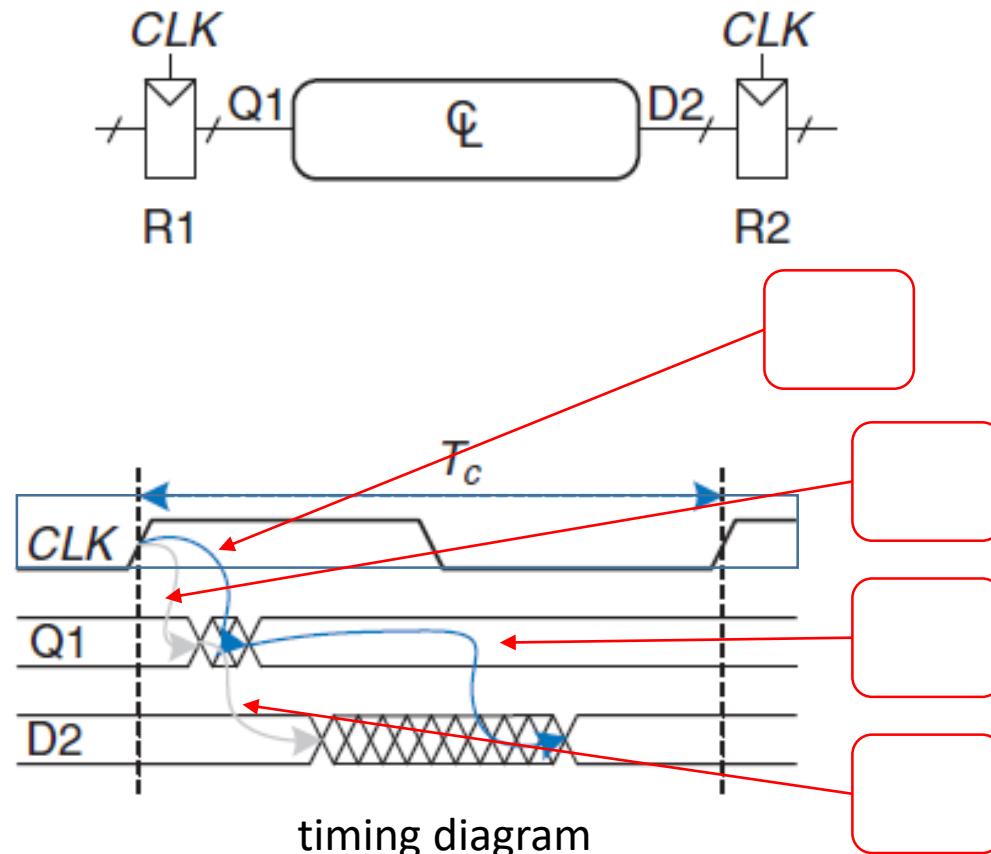


Timing of Synchronous Sequential Logic

- Each calculation cycle starts immediately after an active clock edge and ends with the next one
- On the rising edge of the clock, register R1 generates the output Q1
- Q1 enters the combinational logic generating D2, the input to register R2



Timing of Synchronous Sequential Logic

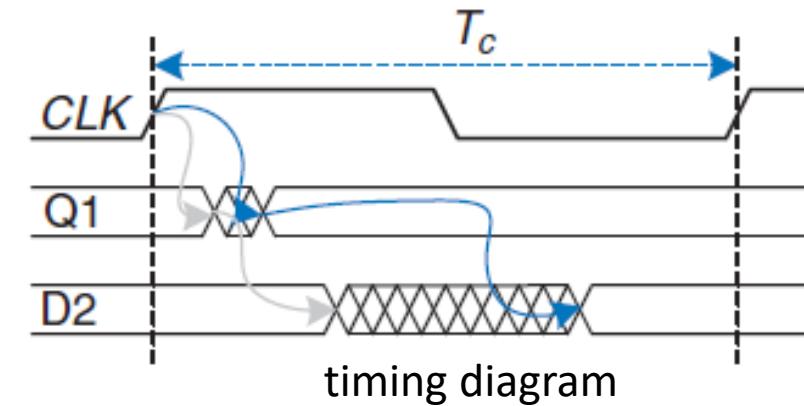
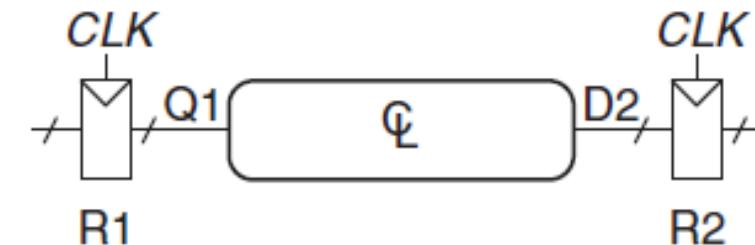


| Term | Name |
|--------------------|---|
| t_{pd} | Logic Propagation Delay |
| t_{cd} | Logic Contamination Delay |
| t_{pcq} | Latch/Flop Clock-to- <i>Q</i> Propagation Delay |
| t_{ccq} | Latch/Flop Clock-to- <i>Q</i> Contamination Delay |
| t_{setup} | Latch/Flop Setup Time |
| t_{hold} | Latch/Flop Hold Time |

Timing of Synchronous Sequential Logic

Gray arrows represent the **contamination delay** through R1 and the combinational logic

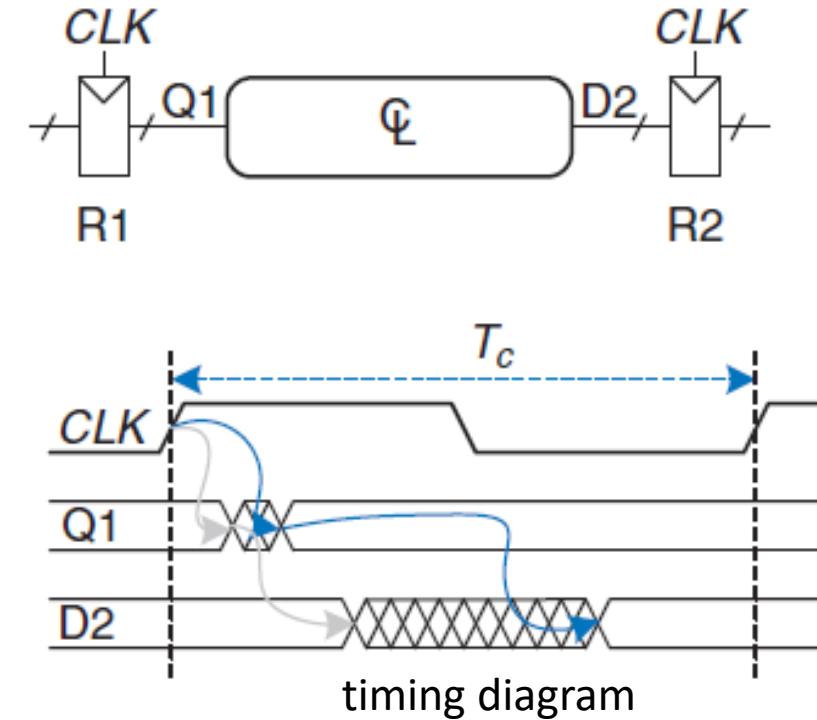
Blue arrows represent the **propagation delay** through R1 and the combinational logic



Timing Analysis of Synchronous Sequential Logic

Problem: given a generic path in a synchronous sequential circuit, calculate the **maximum clock frequency** that can be applied

Procedure: analyse the timing constraints with respect to the setup and hold time of the second register R2



Timing Analysis of Synchronous Sequential Logic: Setup Time Constraint

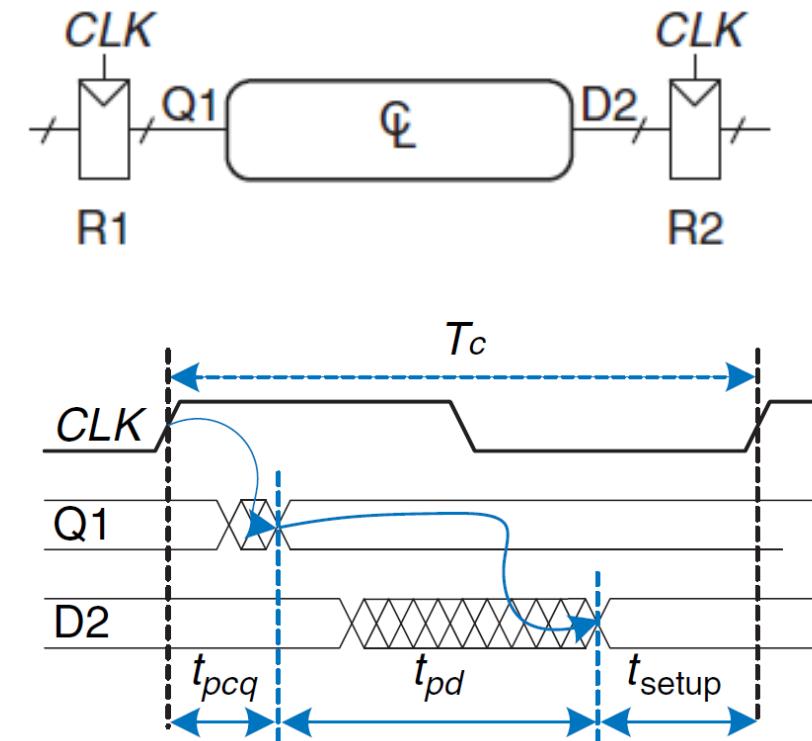
Analysis of the timing constraints with respect to the setup time of the second register R2

- use of timing diagram with only the maximum delay through the path
- to satisfy the setup time of R2, D2 must settle no later than the setup time before the next CLK edge:

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$

If the equation is solved for the maximum propagation delay through the combinational logic:

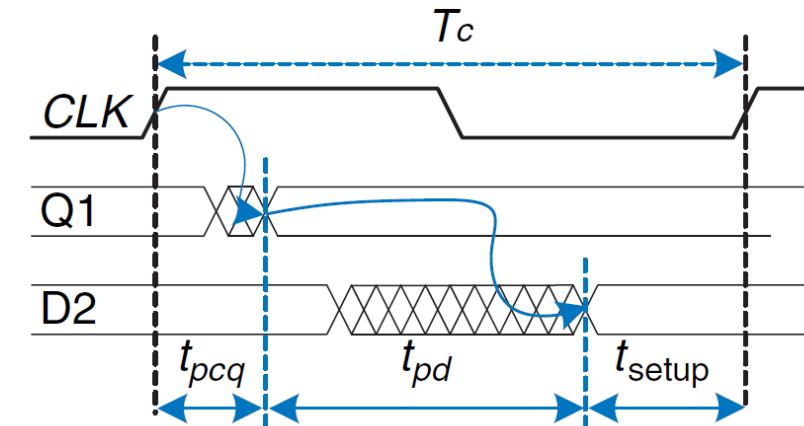
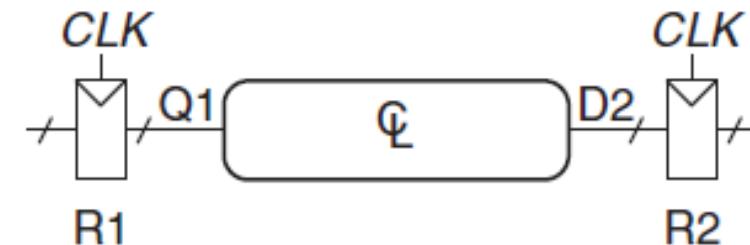
$$t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}})$$



Timing Analysis of Synchronous Sequential Logic: Setup Time Constraint

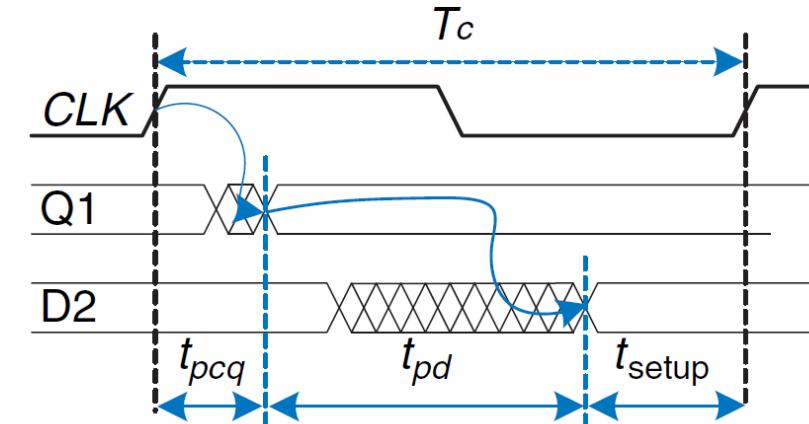
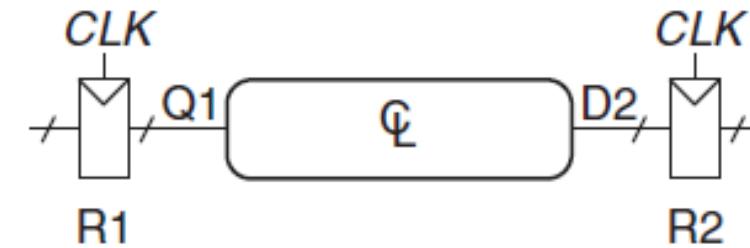
$$t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}})$$

- **setup time constraint** or max-delay constraint, because it depends on the setup time
- it limits the maximum delay through combinational logic



Timing Analysis of Synchronous Sequential Logic: Setup Time Constraint

- If the propagation delay t_{pd} through the combinational logic is too high, R2 may sample an incorrect result and the circuit will malfunction
- Solution: increase the clock period or redesign the combinational logic for a shorter propagation delay t_{pd}



Timing Analysis of Synchronous Sequential Logic: Hold Time Constraint

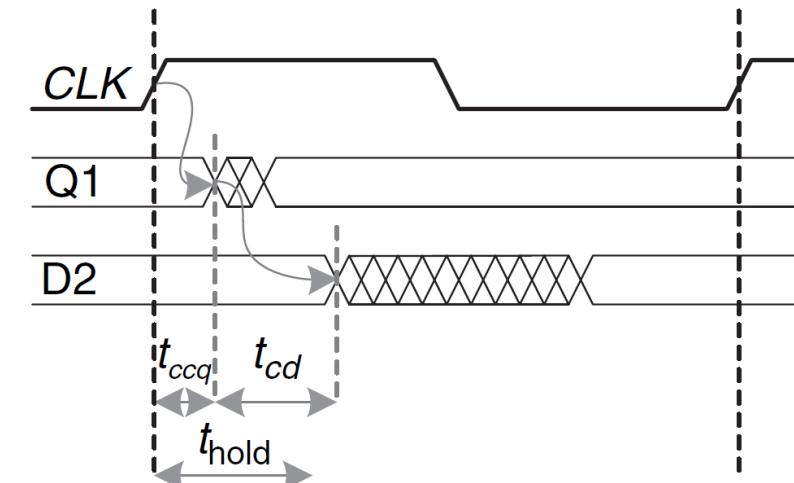
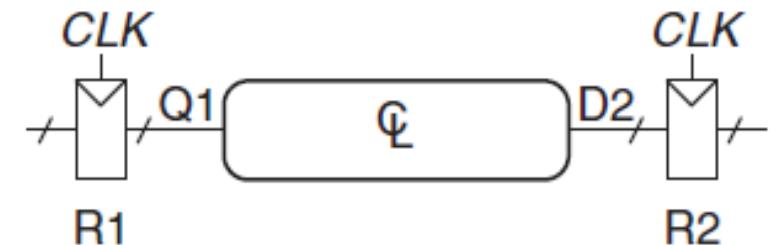
Analysis of the timing constraints with **respect to the hold time** of the second register R2

- use of timing diagram with only the minimum delay through the path
- to satisfy the hold time of R2, its input, D2, must not change until some time, t_{hold} , after the rising edge of CLK

$$t_{ccq} + t_{cd} \geq t_{hold}$$

- if the equation is solved for the minimum contamination delay through the combinational logic:

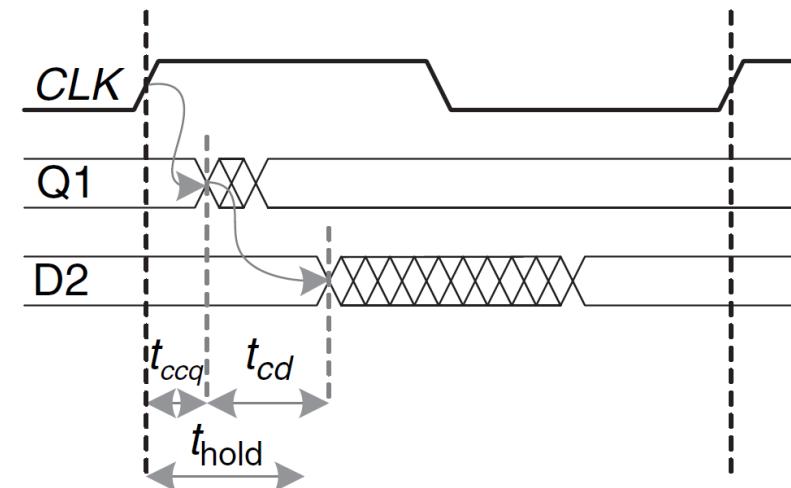
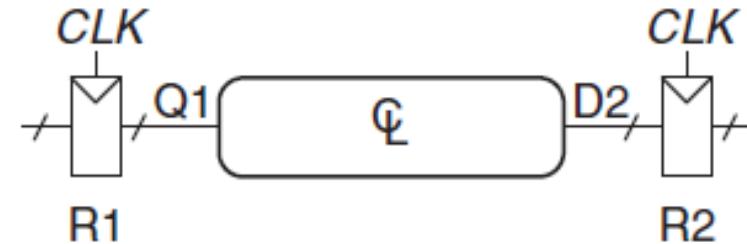
$$t_{cd} \geq t_{hold} - t_{ccq}$$



Timing Analysis of Synchronous Sequential Logic: Hold Time Constraint

$$t_{cd} \geq t_{\text{hold}} - t_{ccq}$$

- **hold time constraint** or min-delay constraint, because it depends on the hold time
- it limits the minimum delay through combinational logic

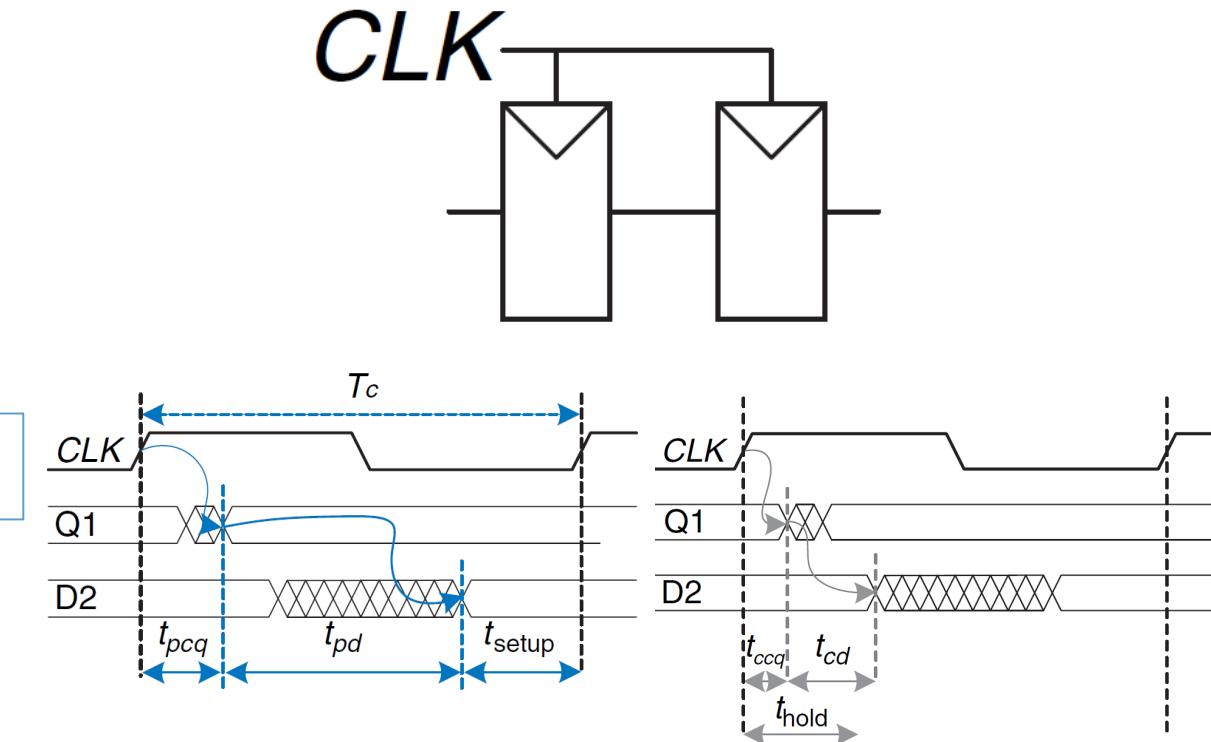


Timing Analysis of Synchronous Sequential Logic: Cascading flip-flops

Analysis of a *cascaded* arrangement of two D-FF, are there hold time problems?

In such a case there is no combinational logic between flip-flops

- hold time constraint:
 $t_{cd}=0 \rightarrow t_{hold} \leq t_{ccq}$
- a reliable flip-flop must have a t_{hold} shorter than its t_{ccq}
- often, flip-flops are designed with $t_{hold} = 0$



Timing Analysis of Synchronous Sequential Logic: exercise 2

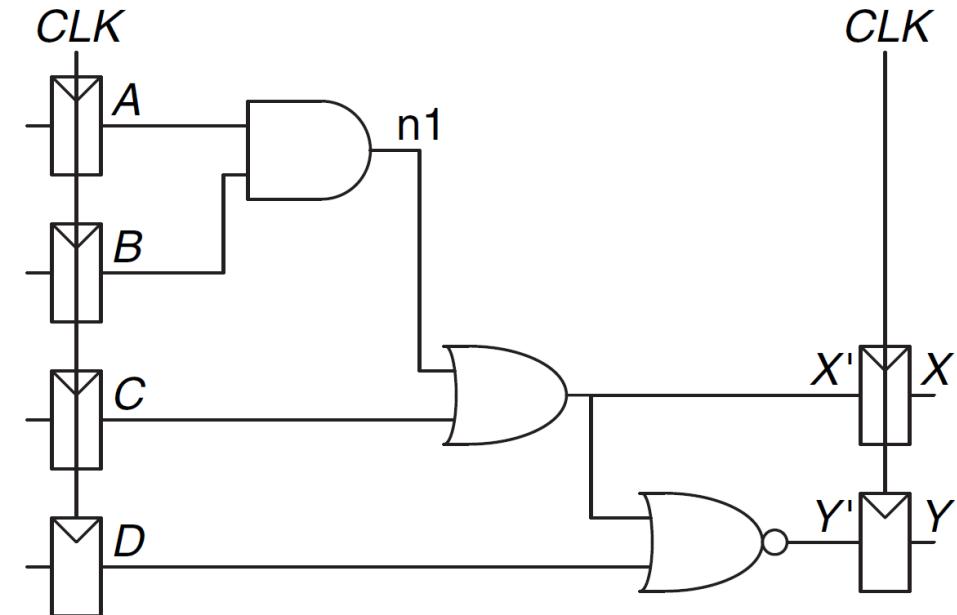
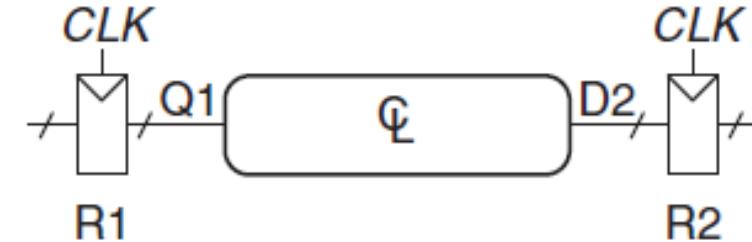
Timing analysis: determine the maximum clock frequency and whether any hold time violations could occur

DFF:

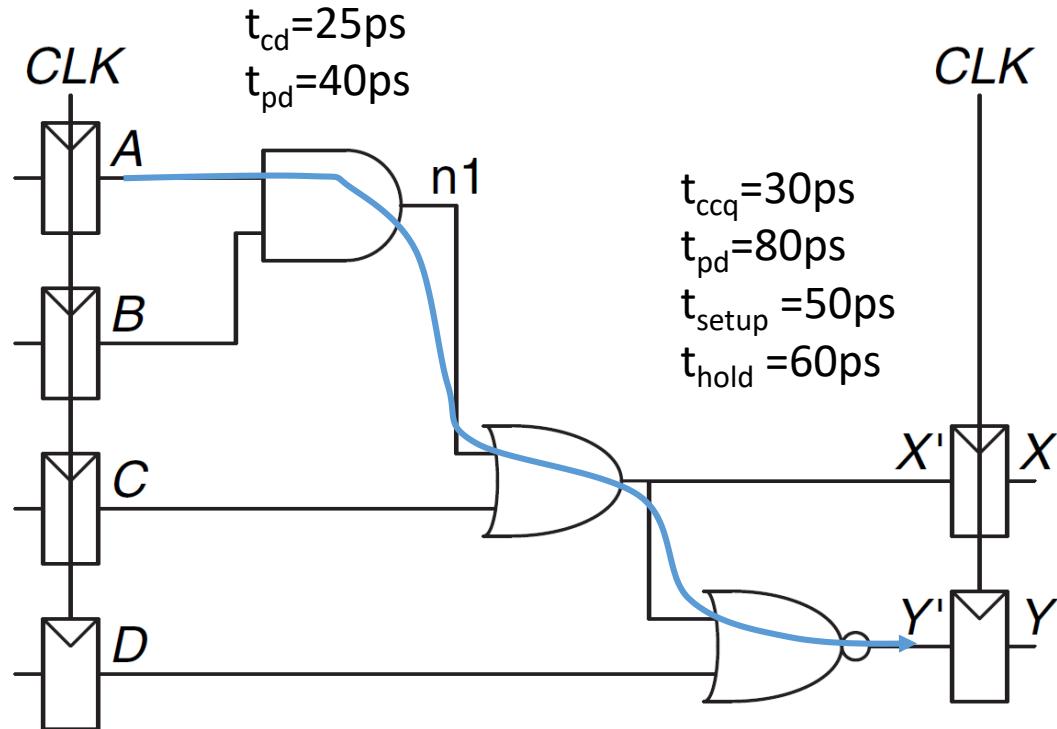
- clock-to-Q contamination delay of 30 ps
- propagation delay of 80 ps
- setup time of 50 ps
- hold time of 60 ps

Logic gates:

- propagation delay of 40 ps
- contamination delay of 25 ps

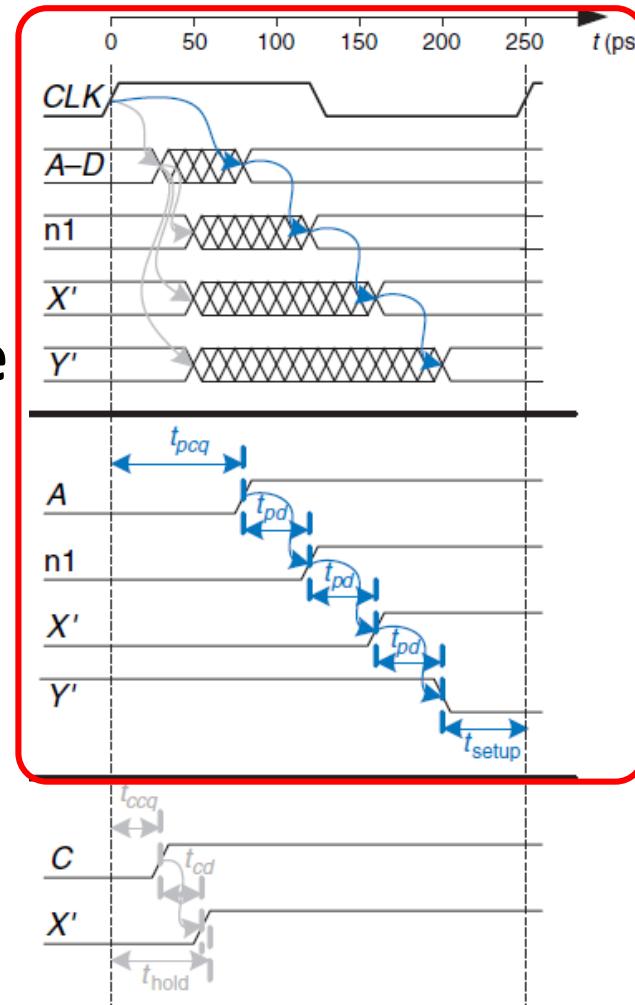


Timing Analysis of Synchronous Sequential Logic: exercise 2



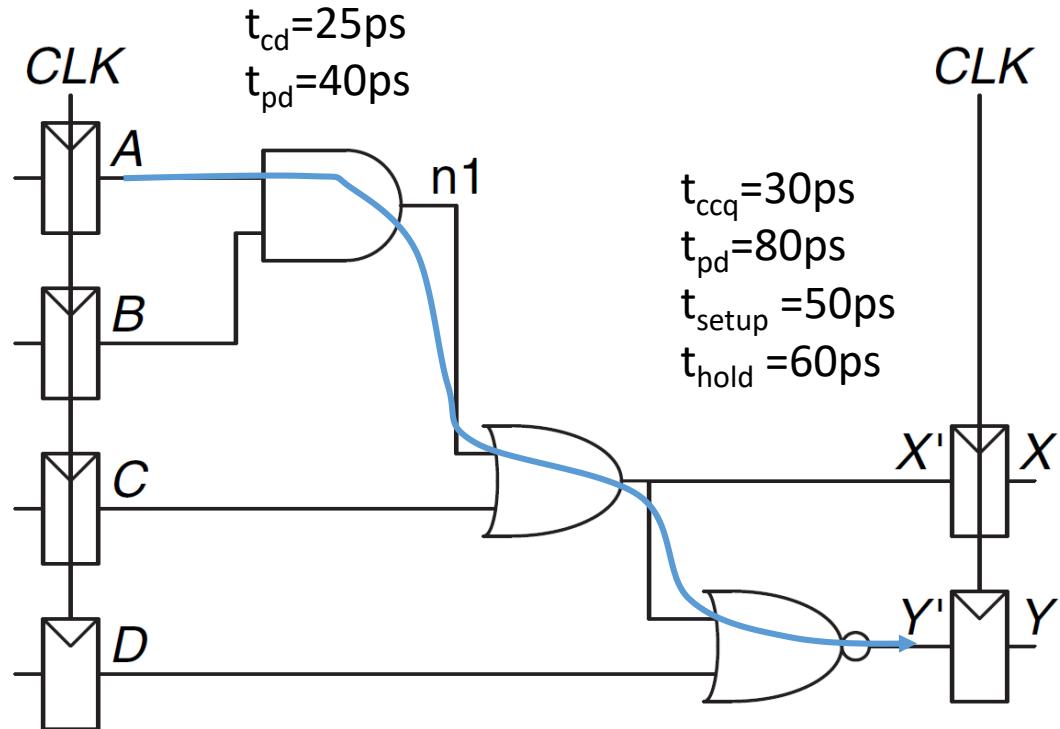
**Setup Time
Constraint**

**Hold Time
Constraint**



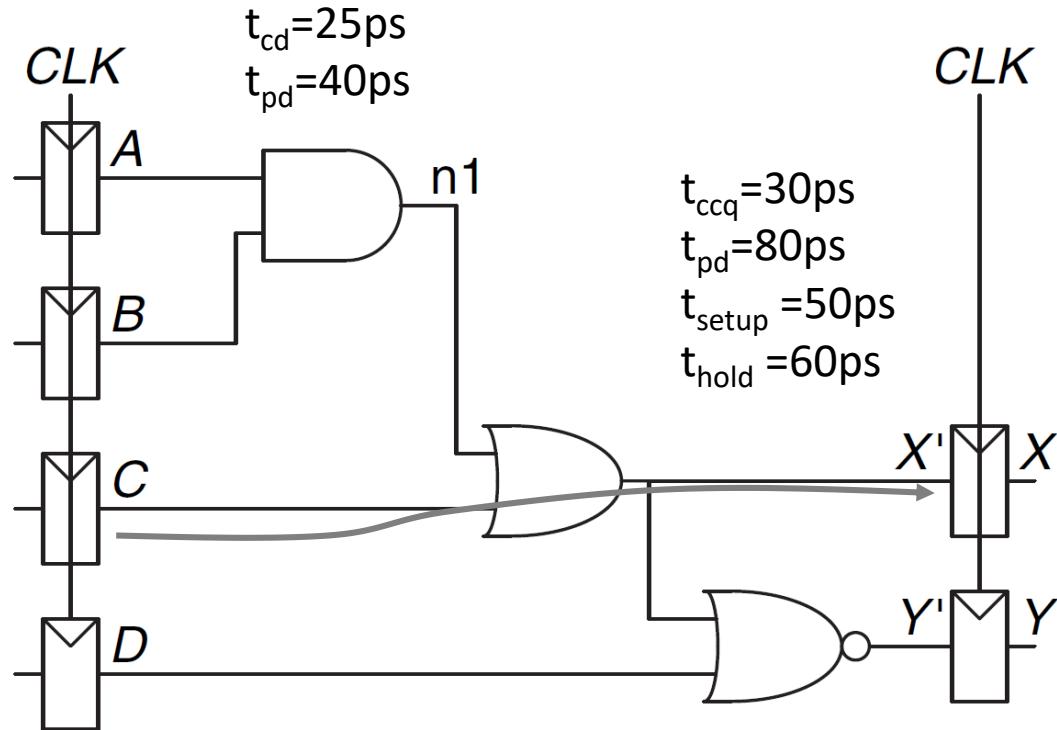
Timing Analysis of Synchronous Sequential Logic: exercise 2

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$



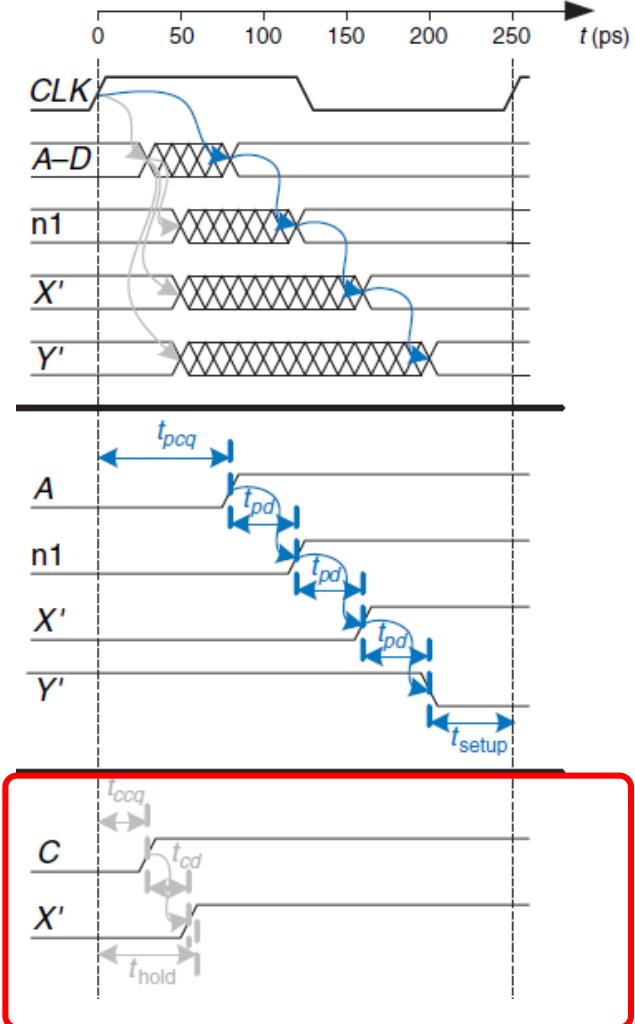
Maximum clock frequency
Setup Time Constraint: find the longest path

Timing Analysis of Synchronous Sequential Logic: exercise 2



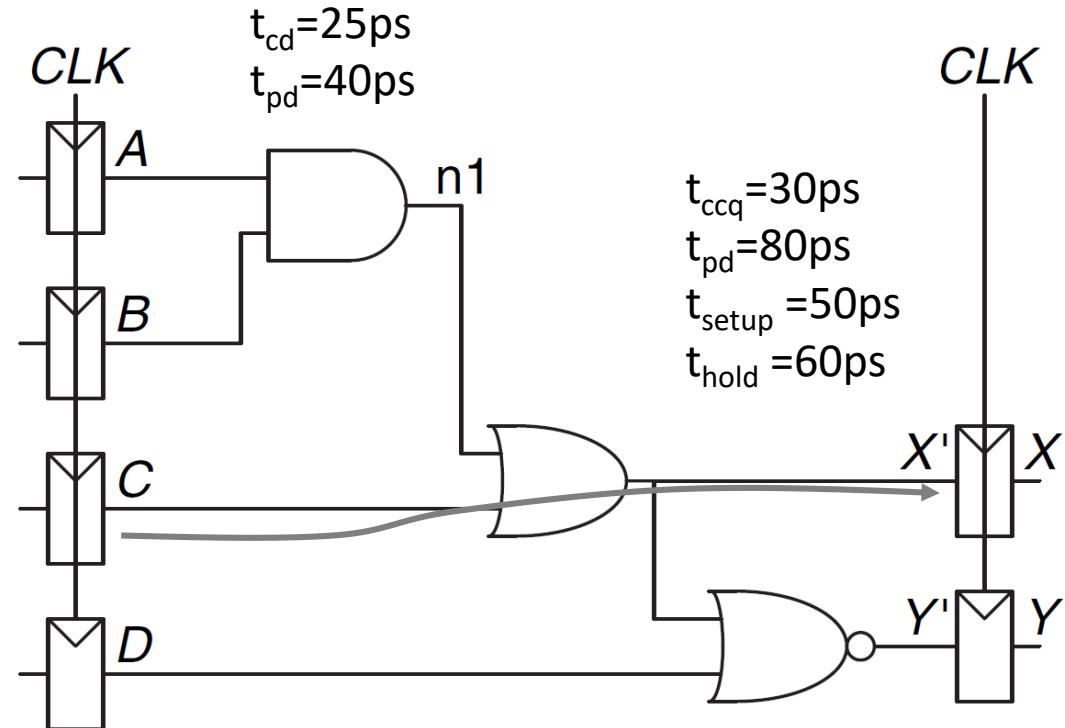
Setup Time
Constraint

Hold Time
Constraint



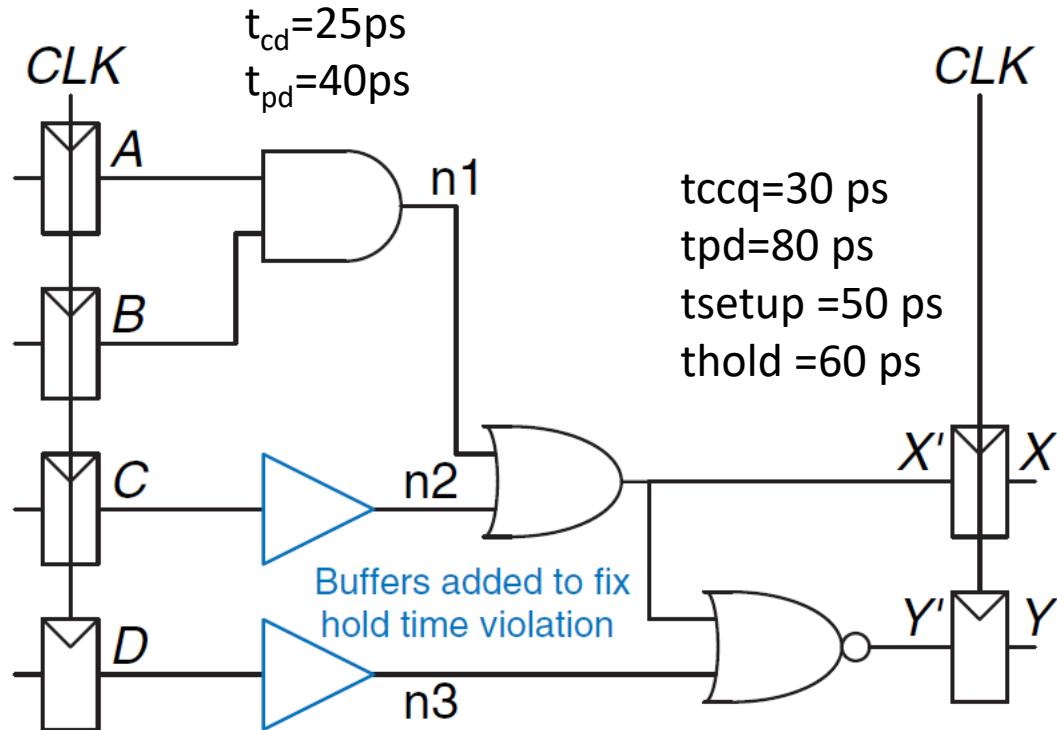
Timing Analysis of Synchronous Sequential Logic: exercise 2

$$t_{ccq} + t_{cd} \geq t_{hold}$$



Hold Time Constraint: find the shorter path

Timing Analysis of Synchronous Sequential Logic: exercise 2



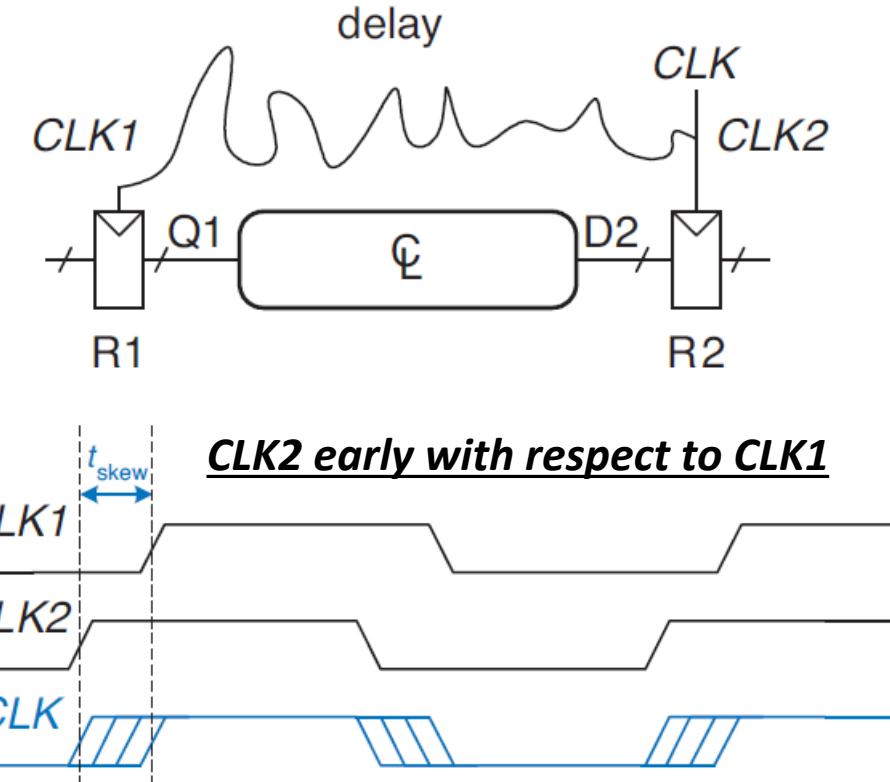
Hold time violations fix: add buffers to slow down short paths
If the buffers have the same delays as other gates, **determine**:

- the maximum clock frequency
- whether any hold time problems could occur

Clock Skew

What happens if the clock does not reach all registers at exactly the same time?

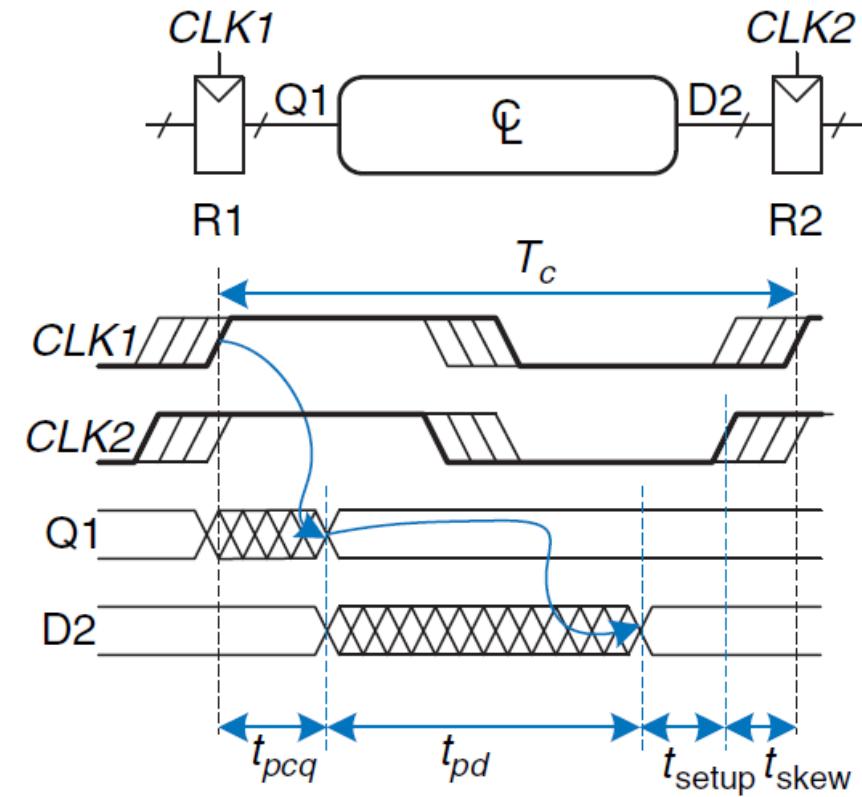
- Clock skew, t_{skew} : variation in clock edges
- When doing the timing analysis, consider the worst-case scenario to ensure the circuit works under all circumstances



Timing Analysis with Clock Skew

Skew is added to the timing diagram:

- heavy clock line indicates the latest time at which the clock signal might reach any register
- hashed lines show that the clock might arrive upto t_{skew} earlier



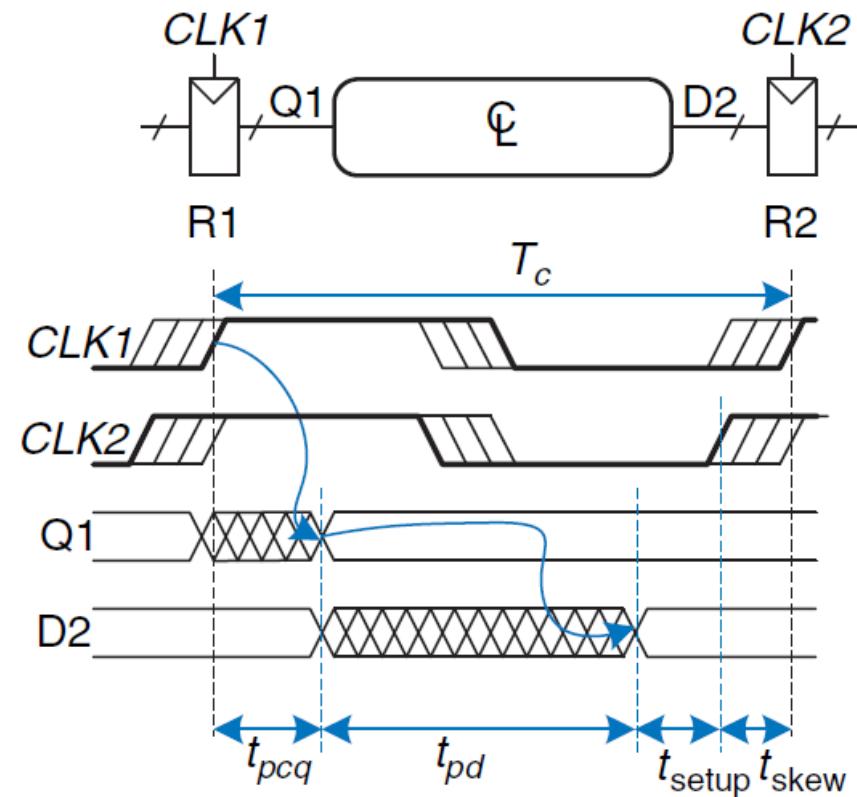
Timing Analysis with Clock Skew: Setup Time Constraint

Consider R1 receives the latest skewed clock and R2 receives the earliest:

- data has a limited time to propagate between registers and must setup before R2 samples it

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}} + t_{\text{skew}}$$

$$t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}} + t_{\text{skew}})$$



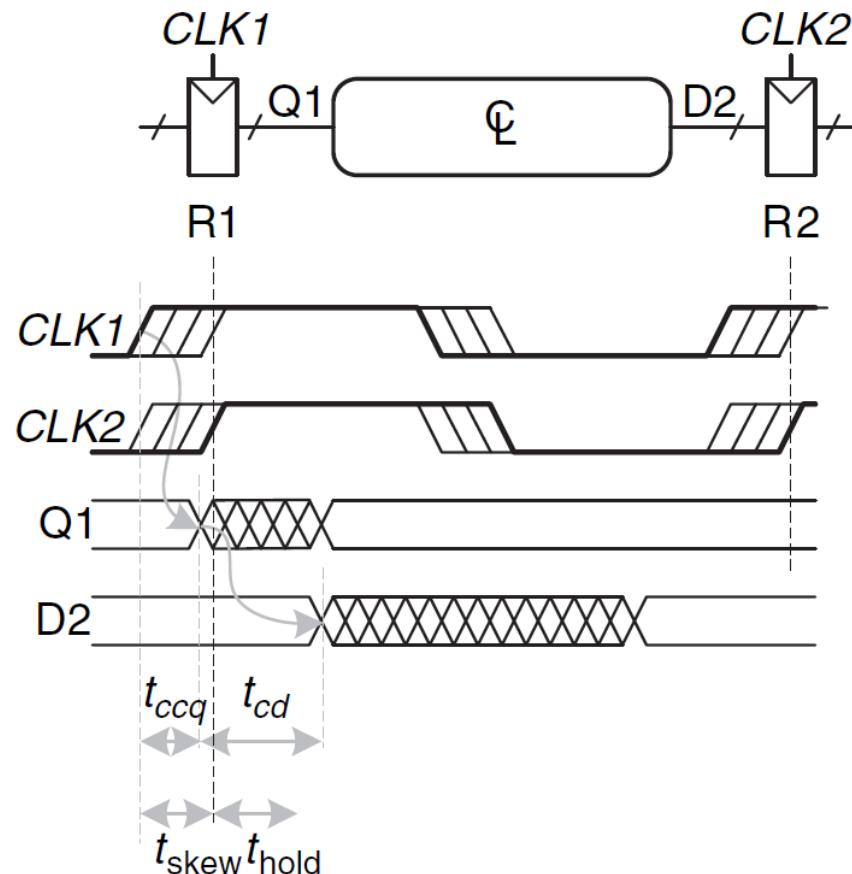
Timing Analysis with Clock Skew: Hold Time Constraint

In the worst case, R1 receives an early skewed clock, CLK1, and R2 receives a late skewed clock, CLK2

- data flows through register and combinatorial logic, but should not arrive until a hold time after the late clock

$$t_{ccq} + t_{cd} \geq t_{hold} + t_{skew}$$

$$t_{cd} \geq t_{hold} + t_{skew} - t_{ccq}$$



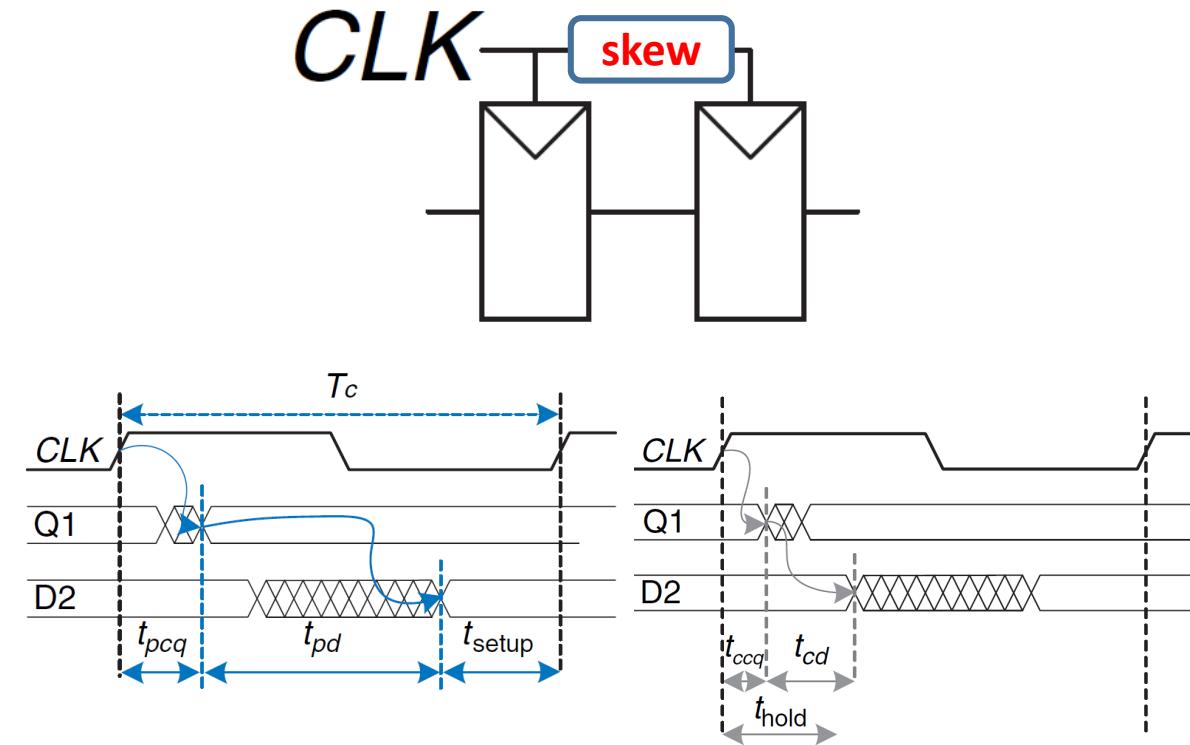
Timing Analysis with Clock Skew: Cascading flip-flops

Analysis of a *cascaded* arrangement of two D-FF with clock skew, are there hold time problems?

- Even if $t_{\text{hold}} = 0$, a pair of back-to-back flip-flops can violate the equation:

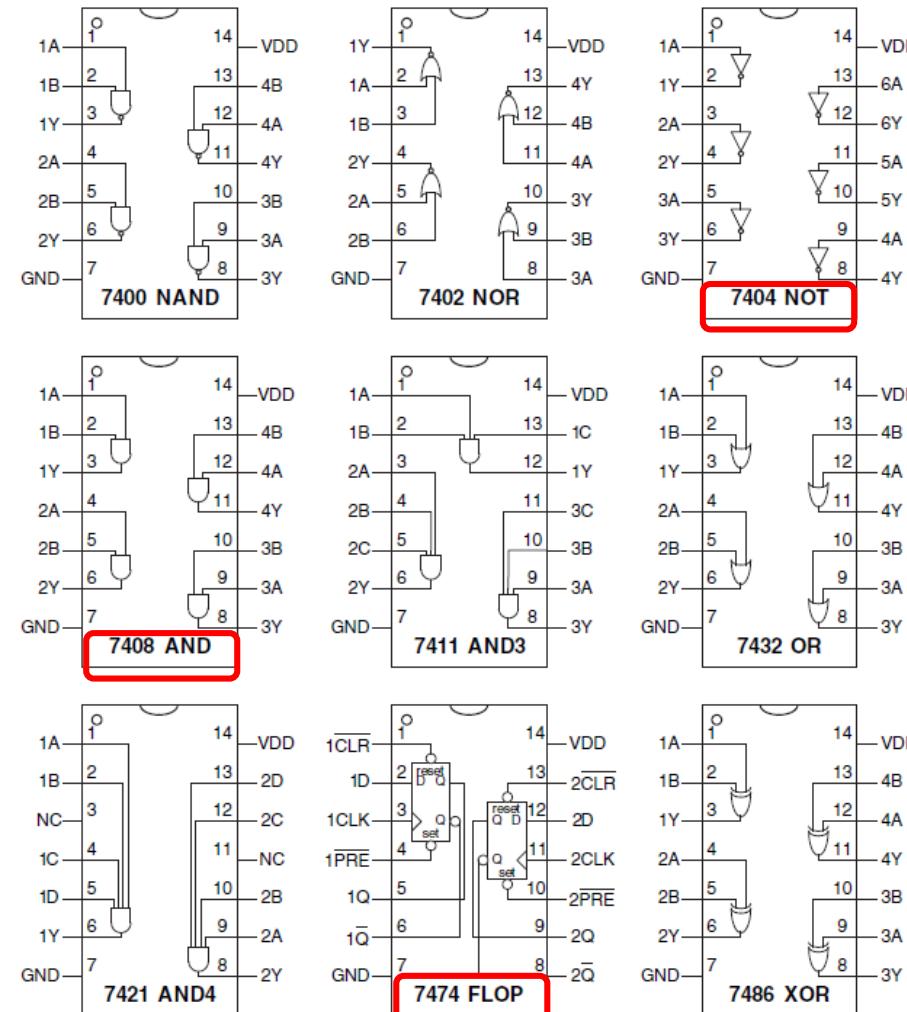
$$t_{\text{ccq}} \geq t_{\text{skew}}$$

- If $t_{\text{ccq}} < t_{\text{skew}}$, flip-flops can intentionally designed to be particularly slow (large tccq)



Timing Analysis of Synchronous Sequential Logic: 74xx LOGIC

- 74xx-series logic: chips, each containing few logic gates, for example:
- 7404: six NOT gates
- 7408: four AND gates
- 7474: two flip-flops



Timing Analysis of Synchronous Sequential Logic: 74xx LOGIC

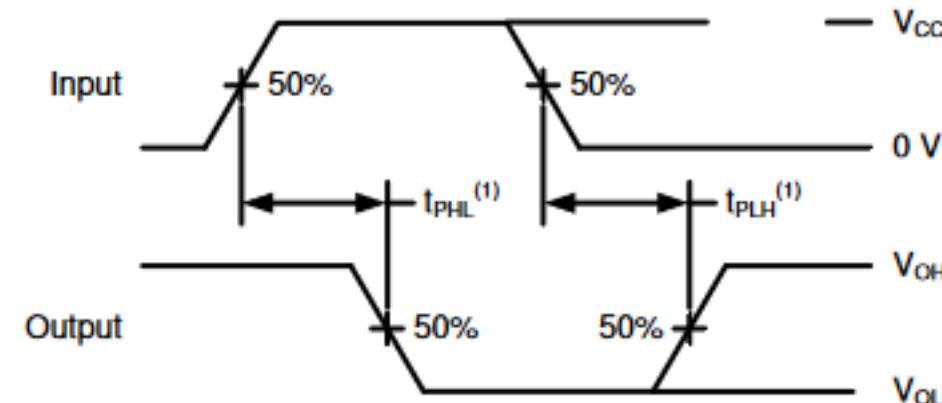
SNx4HC04 Hex Inverters

- The propagation delay, t_{pd} , is measured from when the input passes through $0.5V_{CC}$ to when the output passes through $0.5V_{CC}$
- If V_{CC} is nominally 2V and the chip drives a capacitance of less than 50 pF, the propagation delay will not exceed 95ns (and typically will be much faster)
- The maximum between t_{PLH} and t_{PHL} is used for t_{pd}

6.8 Switching Characteristics - 54

over operating free-air temperature range; typical values measured at $TA = 25^\circ\text{C}$ (unless otherwise noted).

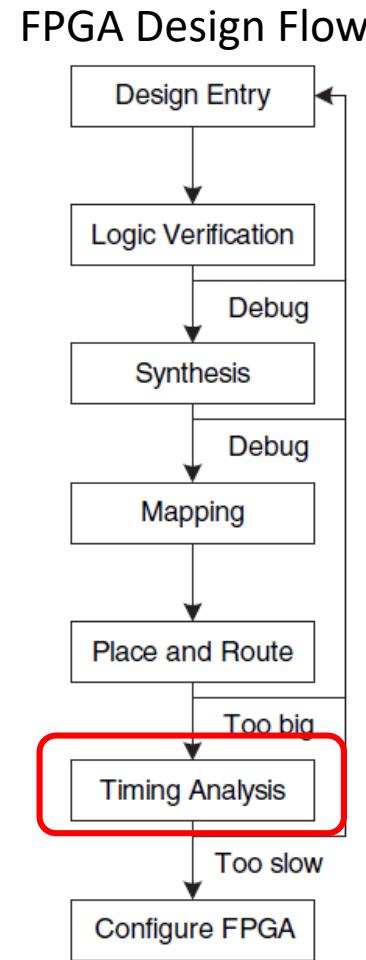
| PARAMETER | FROM | TO | V_{CC} | Operating free-air temperature (T_A) | | | | | | | | | UNIT | |
|-------------------------------|------|----|----------|--|-----|-----|---------------|-----|-----|----------------|-----|-----|------|--|
| | | | | 25°C | | | −40°C to 85°C | | | −55°C to 125°C | | | | |
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | |
| t_{pd} Propagation delay | A | Y | 2 V | 45 | 95 | | 120 | | 125 | | | | ns | |
| | | | 4.5 V | 9 | 19 | | 24 | | 29 | | | | | |
| | | | 6 V | 8 | 16 | | 20 | | 25 | | | | | |



Timing Analysis of Synchronous Sequential Logic: FPGA

FPGA, Field Programmable Gate Array: array of reconfigurable gates

- Using software programming tools, both combinational and sequential logic designs can be implemented on FPGAs
- Modern FPGAs integrate other features such as multipliers, high-speed I/Os, analog-to-digital converters, large RAM arrays and processors



Design Entry: design specified with a hardware description language (HDL)

Logic Verification: The design is then simulated to verify that the logic is correct

Logic synthesis: converts the HDL into Boolean functions

Mapping: FPGA tool maps the functions onto the Logic Elements (LEs) of a specific chip

Place and route tool determines which functions go in which lookup tables and how they are wired together

Timing Analysis: compares the timing constraints against the actual circuit delays and reports any errors

Configuration: a file is generated specifying the contents of all the (Logic Elements)LEs and the programming of all the wires on the FPGA

Timing Analysis of Synchronous Sequential Logic: FPGA, exercise 3

A design is implemented as a FSM (Finite State Machine) on a FPGA having the timing characteristics shown beside

1. If the FSM has to run at 100 MHz, what is the maximum number of Logic Elements on the critical path?
2. What is the fastest speed at which her FSM could possibly run?

- **FPGA Timings**

| name | value (ps) |
|---------------------------------|------------|
| t_{pcq} | 199 |
| t_{setup} | 76 |
| t_{hold} | 0 |
| t_{pd} (per LE) | 381 |
| t_{wire} (between LEs) | 246 |

Timing Analysis of Synchronous Sequential Logic: FPGA, exercise 3

1. If the FSM has to run at 100 MHz, what is the maximum number of LEs on the critical path?

At 100 MHz, T_c , is 10 ns

- minimum combinational propagation delay, t_{pd} , at this cycle time:

- **FPGA Timings**

| name | value (ps) |
|---------------------------------|------------|
| t_{pcq} | 199 |
| t_{setup} | 76 |
| t_{hold} | 0 |
| t_{pd} (per LE) | 381 |
| t_{wire} (between LEs) | 246 |

Timing Analysis of Synchronous Sequential Logic: FPGA, exercise 3

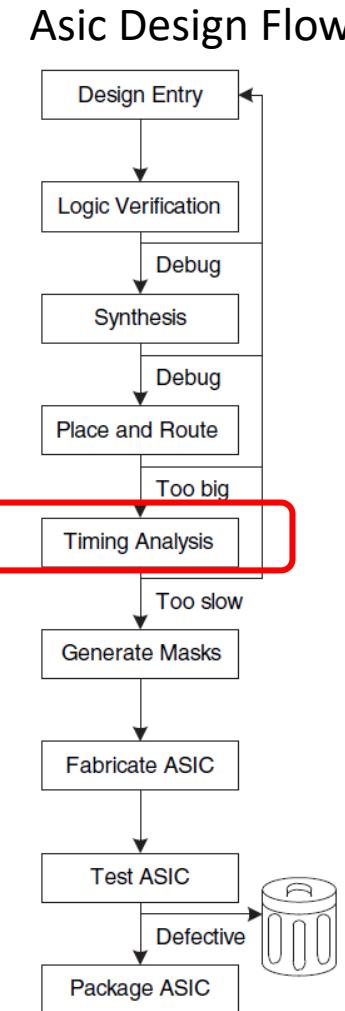
- 2. What is the fastest speed at which her FSM could possibly run?
- The fastest speed is when using a single LE for the next state logic

- **FPGA Timings**

| name | value (ps) |
|---------------------------------|------------|
| t_{pcq} | 199 |
| t_{setup} | 76 |
| t_{hold} | 0 |
| t_{pd} (per LE) | 381 |
| t_{wire} (between LEs) | 246 |

Timing Analysis of Synchronous Sequential Logic: ASIC

- Application-specific integrated circuits (ASICs) are chips designed for a particular purpose
- Examples of ASICs: graphics accelerators, network interface chips, and cell phone chips
- ASIC are hardwired for a specific function
 - several times faster than an FPGA
 - occupies an order of magnitude less chip area than an FPGA with the same function
 - higher cost for production



Design Entry: design specified with a hardware description language (HDL)

Logic Verification: The design is then simulated to verify that the logic is correct

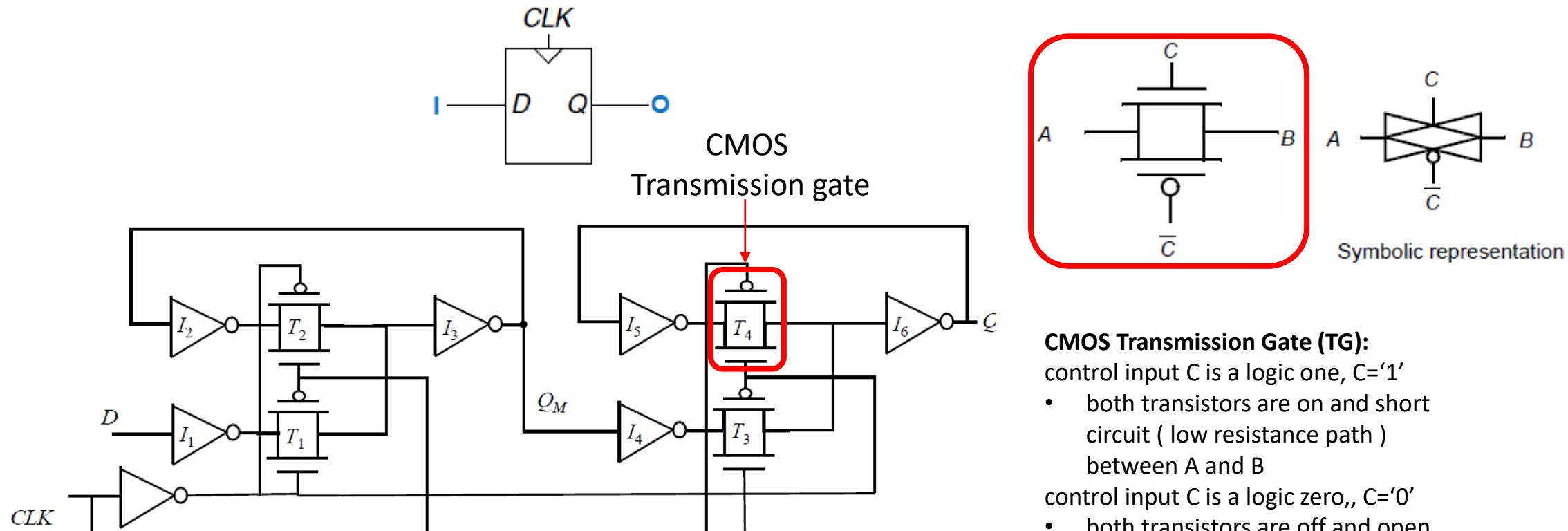
Logic synthesis: converts the HDL into a netlist consisting of logic gates and connections between the gates;

Place and route: the gates in this netlist are placed, and the wires are routed between gates.

Timing Analysis: compares the timing constraints against the actual circuit delays and reports any errors

Mask generation: masks are generated and used to fabricate the ASIC

Timing Analysis of Multiplexer-based Master-Slave Registers

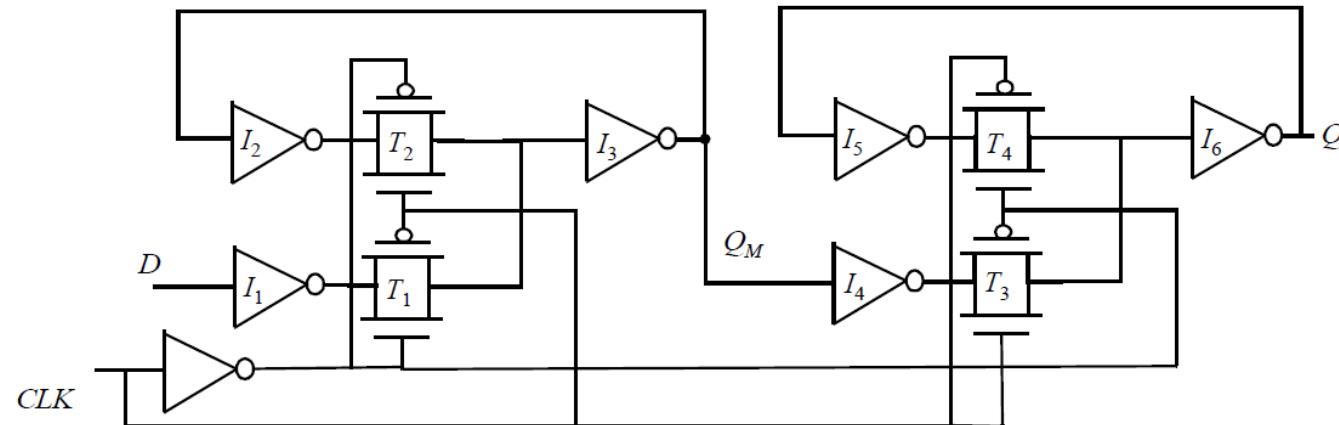


Timing Analysis of Multiplexer-based Master-Slave Registers

Study of factors that affect timing parameters: set-up time, hold time and propagation delay

Assumptions:

- propagation delay of inverters is t_{pd_inv}
- propagation delay of the transmission gate is t_{pd_tx}
- contamination delay is 0
- inverter delay to derive CLK_b from CLK has a delay equal to 0



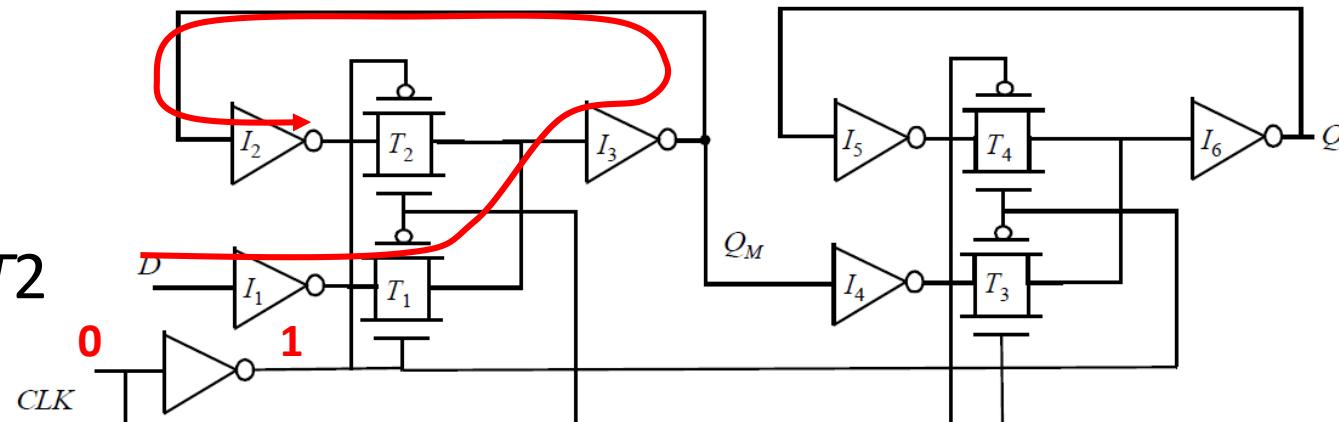
Timing Analysis of Multiplexer-based Master-Slave Registers

Set-up time: the input D must have stabilized at least some *set-up time* before the rising edge of the clock

The input *D* has to propagate through *I*/₁, *T*/₁, *I*/₃ and *I*/₂ before the rising edge of the clock to ensure that the node voltages on both terminals of the transmission gate *T*/₂ are at the same value

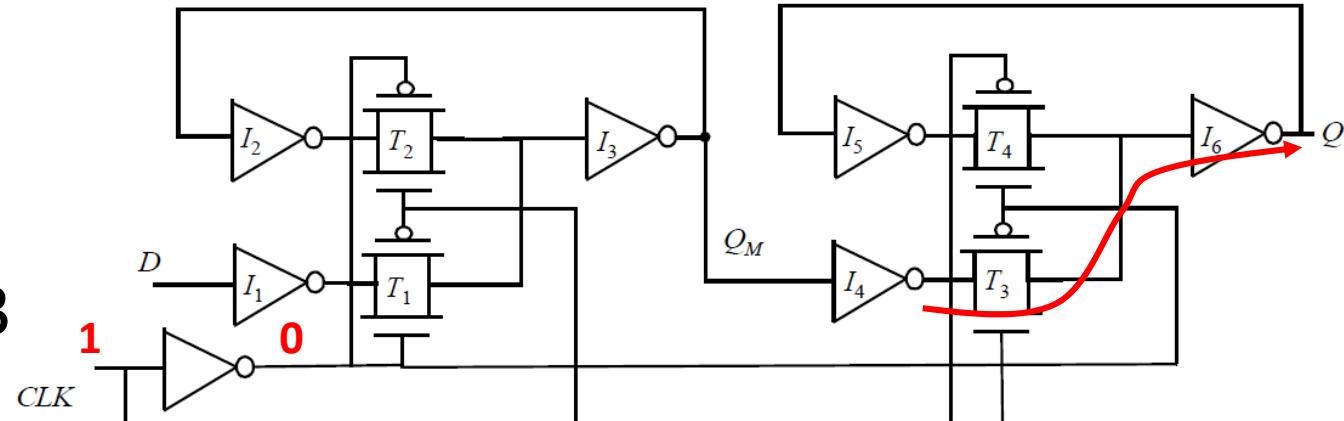
Otherwise, it is possible for the cross-coupled pair *I*/₂ and *I*/₃ to settle to an incorrect value

$$t_{\text{setup}} = 3 * t_{\text{pd_inv}} + t_{\text{pd_tx}}$$



Timing Analysis of Multiplexer-based Master-Slave Registers

- *propagation delay* : time for the value of Q_M to propagate to the output Q
- the output of I_4 is valid before the rising edge of clock
- delay t_{cq} is the delay through T_3 and I_6

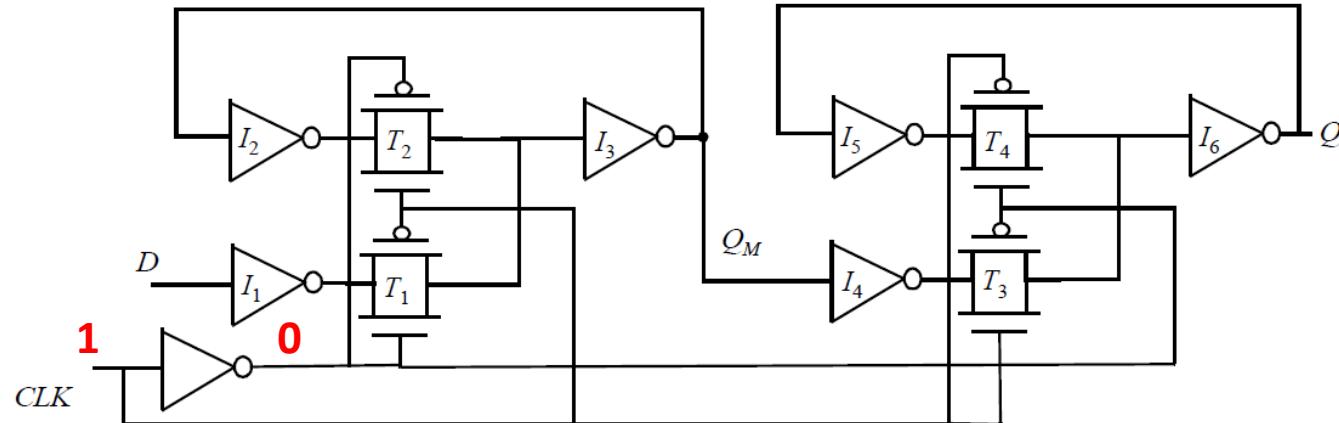


$$t_{pcq} = t_{pd_tx} + t_{pd_inv}$$

Timing Analysis of Multiplexer-based Master-Slave Registers

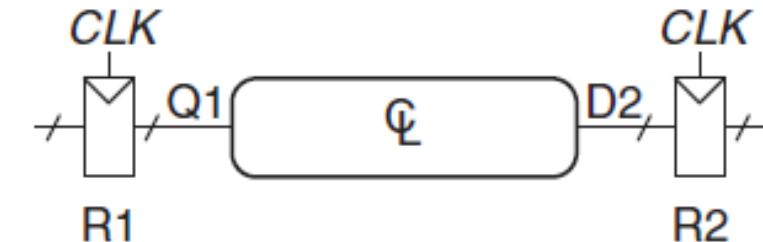
- *hold time* : the input must remain stable for at least some **hold time** after the rising edge of the clock
- the transmission gate T_1 turns off when clock goes high
- any changes in the D -input after clock rising are not seen by the input

$$t_{hold} = 0$$



Timing of Synchronous Sequential Logic: Summary

- The maximum delay constraint limits the number of consecutive gates on the critical path of a high-speed circuits
- Setup and hold time constraints dictate the maximum and minimum delays of the combinational logic between flip-flops in sequential circuits
- Modern flip-flops are usually designed so that the minimum delay through the combinational logic is 0
- Clock skew effectively increases both the setup time and the hold time.



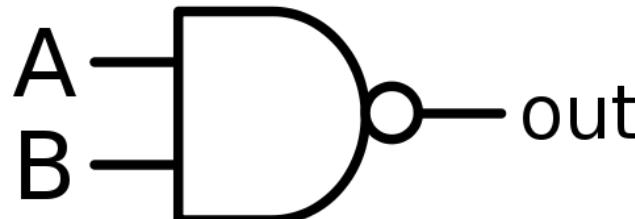
| Term | Name |
|--------------------|---|
| t_{pd} | Logic Propagation Delay |
| t_{cd} | Logic Contamination Delay |
| t_{pcq} | Latch/Flop Clock-to-Q Propagation Delay |
| t_{ccq} | Latch/Flop Clock-to-Q Contamination Delay |
| t_{setup} | Latch/Flop Setup Time |
| t_{hold} | Latch/Flop Hold Time |

Exercises

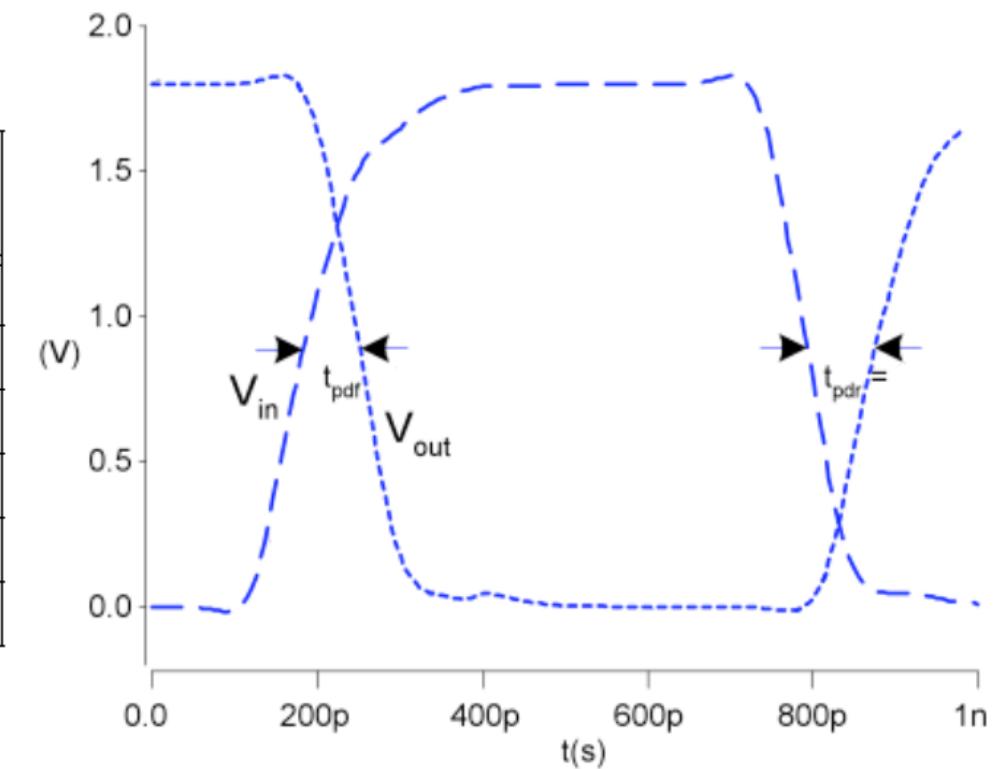
Timing Analysis using LTspice

Timing Analysis using LTspice : exercise 1

Obtain the t_{pd} time of a NAND2 gate using LTspice



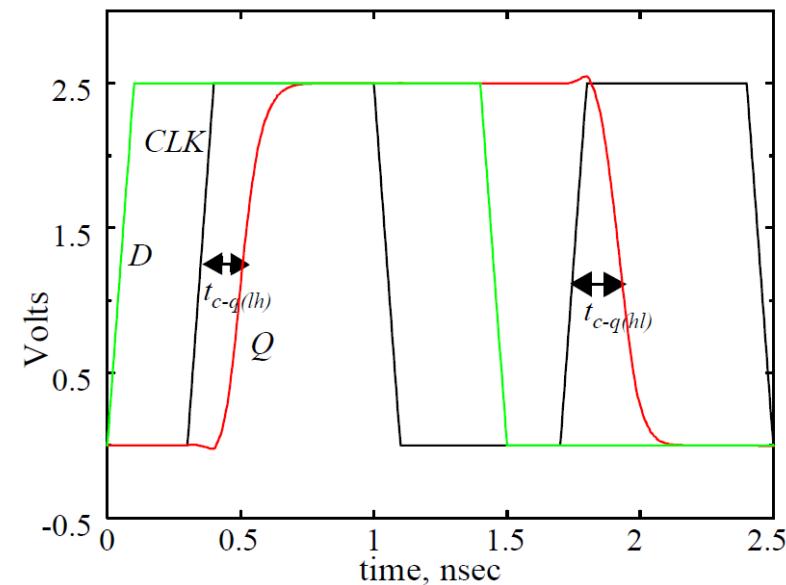
| Input Data Pattern | Delay |
|------------------------------|-------|
| $A = B = 0 \rightarrow 1$ | |
| $A = 1, B = 0 \rightarrow 1$ | |
| $A = 0 \rightarrow 1, B = 1$ | |
| $A=B=1\rightarrow 0$ | |
| $A=1, B = 1 \rightarrow 0$ | |
| $A= 1 \rightarrow 0, B = 1$ | |



Timing Analysis using LTspice : exercise 2

Obtain the propagation delay of the D-FF using LTspice, assume that:

- a load of a single inverter is connected at each D-FF output
- the D-FF is initially in reset state



Simulation of *propagation delay*.

Timing Analysis using LTspice : exercise 3

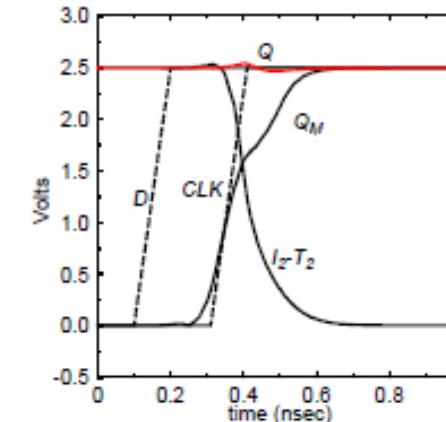
Obtain the set-up time, t_{setup} , of the D-FF using LTspice :

- progressively skew the input D with respect to the clock edge until the circuit fails

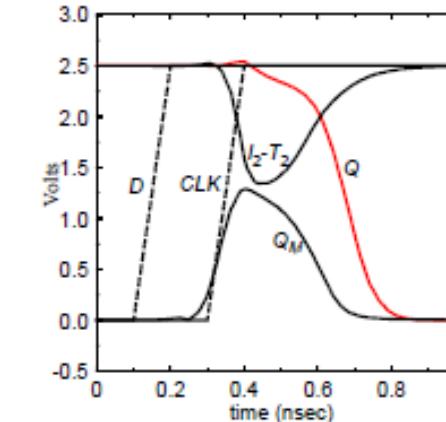
Assume that:

- a load of a single inverter is connected at each D-FF output

No set-up time violation!



Set-up time violation!



Timing Analysis using LTspice : exercise 4

Obtain the hold time, t_{hold} , of the D-FF using LTspice :

- progressively skew the D input edge relative to the clock signal till the circuit stop functioning (for this design, the *hold time* is 0 - i.e., the inputs can be changed on the clock edge)

References

- David Harris and Sarah Harris. 2007. Digital Design and Computer Architecture. Morgan Kaufmann Publishers Inc., San Francisco, CA, USA.
- Neil Weste and David Harris. 2010. CMOS VLSI Design: A Circuits and Systems Perspective (4th. ed.). Addison-Wesley Publishing Company, USA.
- Rabaey, J. M.; Chandrakasan, A. & Nikolic, B. (2004), Digital integrated circuits- A design perspective , Prentice Hall .
- R. Jacob Baker. 2010. CMOS Circuit Design, Layout, and Simulation (3rd. ed.). Wiley-IEEE Press.

Chapitre 2

Delay Models

Used For Digital Timing Analysis

MA-AdvEIDes

Pietro Buccella

A. A. 2021/22



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Objectives

Objectives of the lesson:

- Knowledge of models for propagation delay calculation of CMOS gates
- Application of delay model to simple CMOS logic gates
- Use logical effort method to predict the best number of stages in a multistage networks

Contents

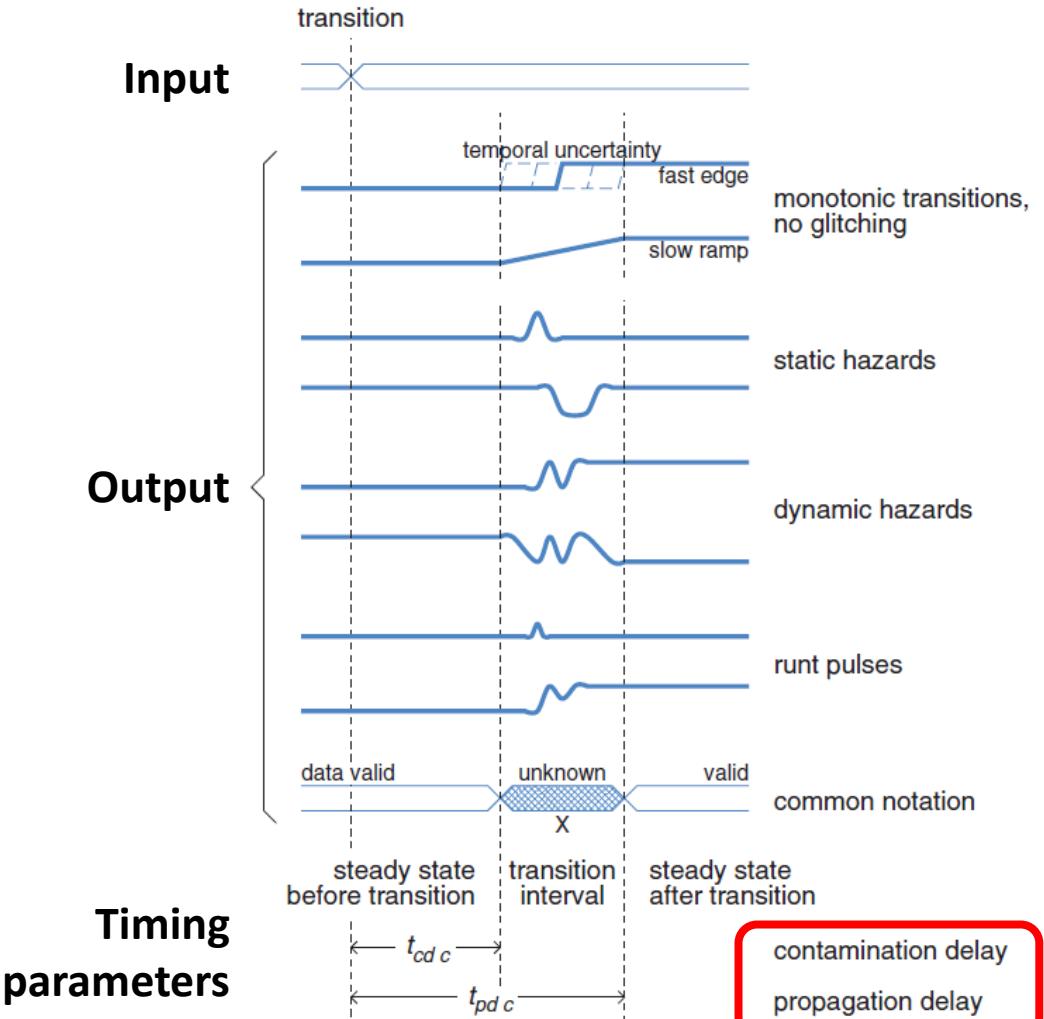
- Logic circuits: equivalent RC model
- Elmore delay
- Linear delay model of logic gates
- Delay in multistage networks
- Best number of stages

Transient Behaviour of Logic Circuits

How long transient phenomena persist at the output of a digital circuit in response to a change at one of the circuit's inputs?

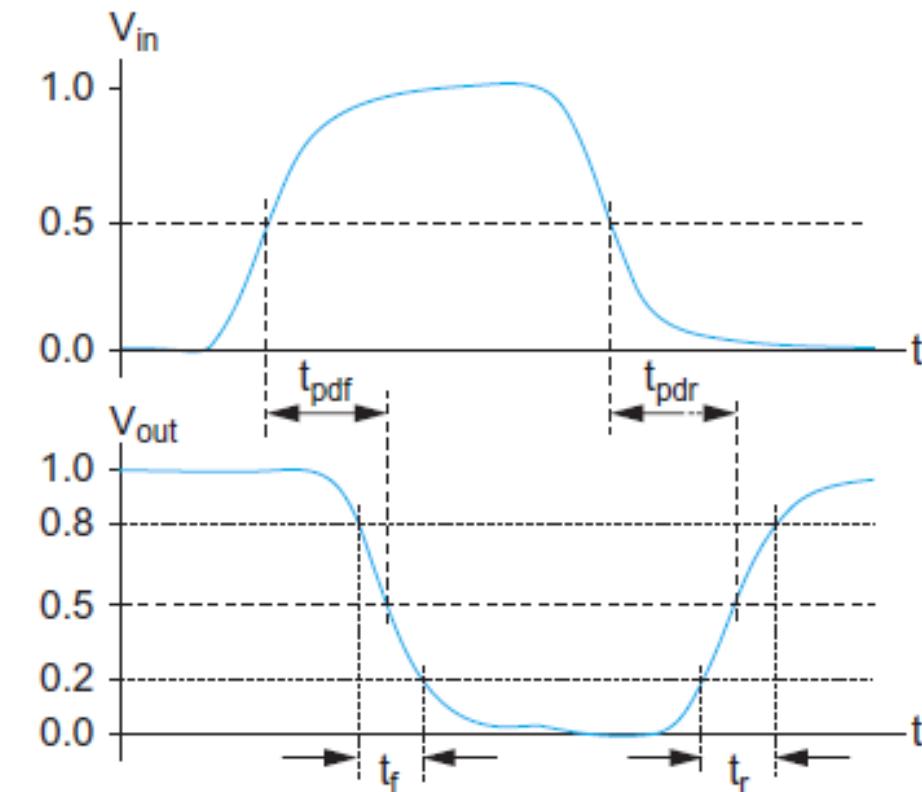
Two Timing Parameters :

- the output will retain its old value for at least the **contamination delay t_{cd}** and take on its new value in at most the **propagation delay t_{pd}**



Transient Behaviour of Logic Circuits

- *Contamination delay, t_{cd}* : **minimum time** from the input crossing 50% to the output crossing 50%
- *Propagation delay, t_{pd}* : **maximum time** from the input crossing 50% to the output crossing 50%
- *Rise time, tr* : time for a waveform to rise from 20% to 80% of its steady-state value
- *Fall time, tf* : time for a waveform to fall from 80% to 20% of its steady-state value
- *Edge rate, $trf = (tr + tf)/2$*

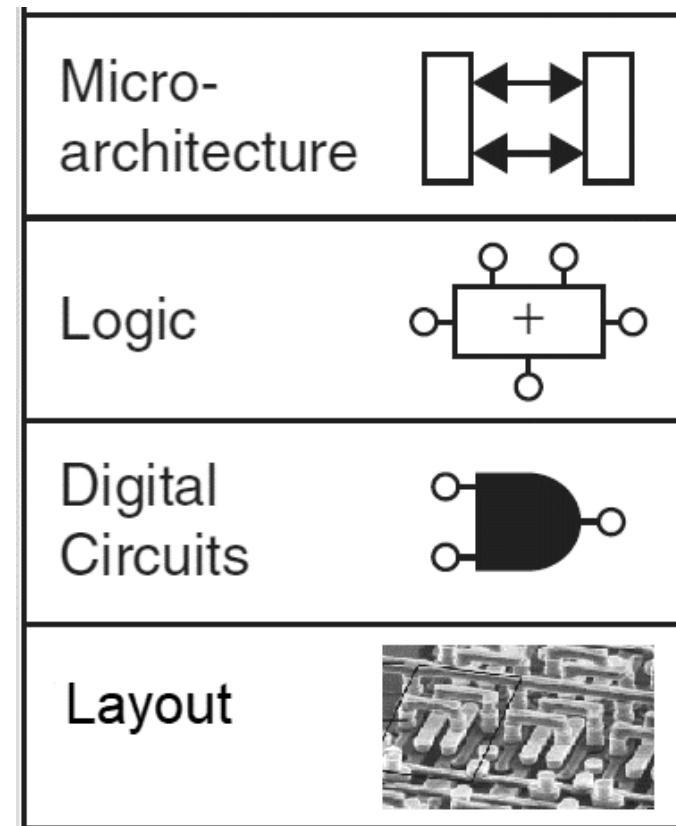


Timing Optimization

There are a number of critical paths that limit the operating speed of a system

Critical paths can be affected at four main levels:

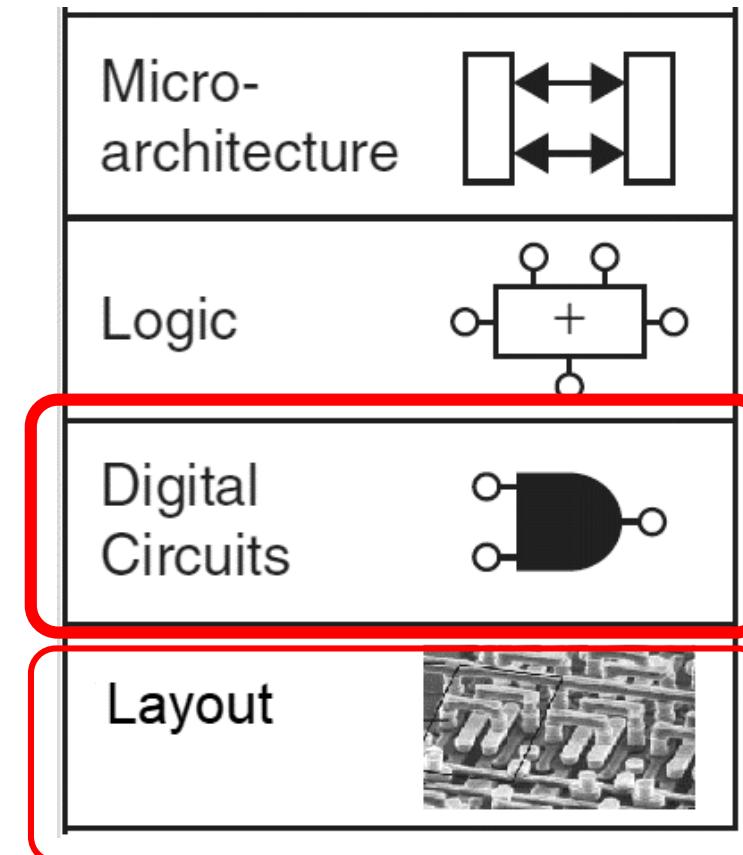
- The microarchitectural level
- The logic level
- The circuit level
- The layout level



Timing Optimization

Delay is dependent on:

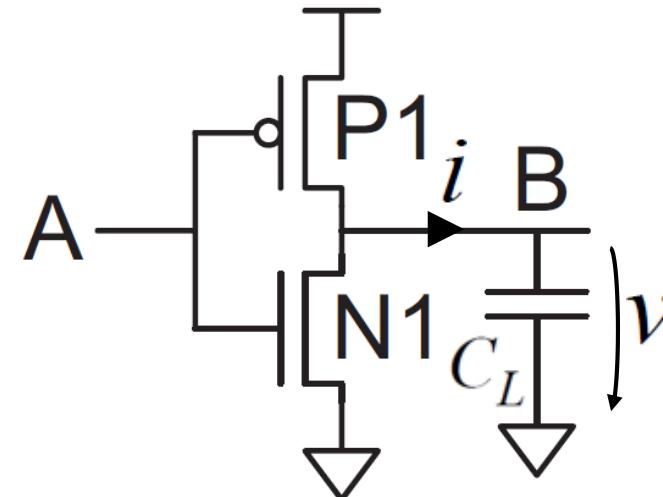
- Algorithms, number of pipeline stages, the number of execution units, size of memories
- Functional blocks, number of stages of gates in the clock cycle, the fan-in and fan-out of the gates
- Transistor sizes or styles of CMOS logic
- Layout, wire lengths and parasitic capacitance can dominate delay



Transient Response Calculation

Delay Computation in Digital Gates:

1. Build physical model of the circuit
2. Write differential equation of output voltage as a function of input voltage and time
3. The solution is the *transient response*
4. Delay is the time when the output reaches $VDD/2$



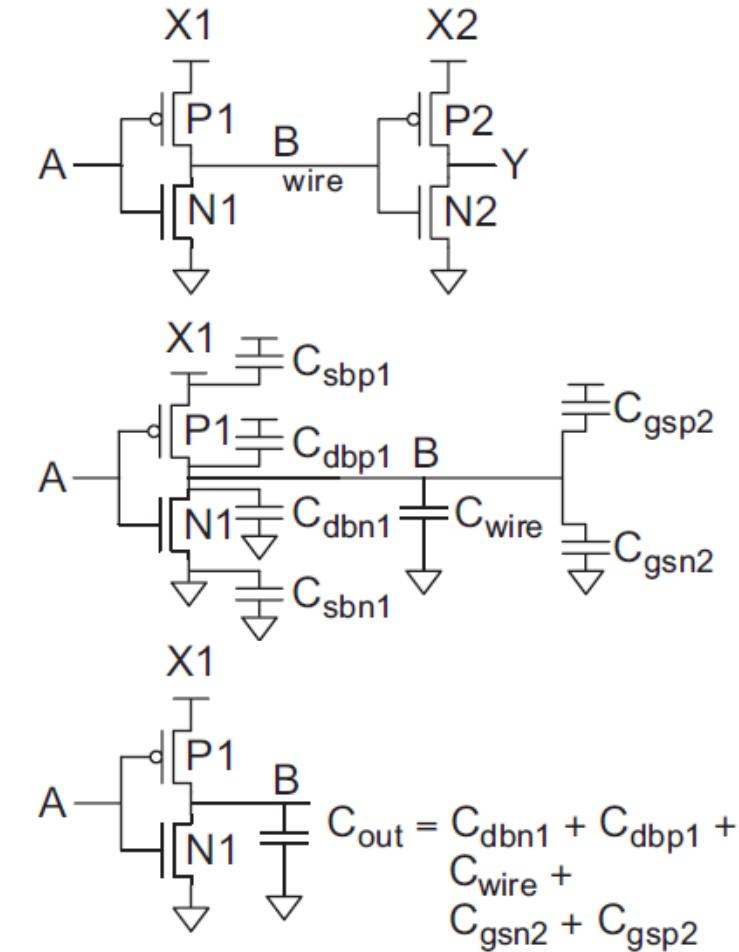
$$t_p = \int_{v_1}^{v_2} \frac{C_L(v)}{i(v)} dv$$

Transient Response of an Inverter

Logic Circuit: inverter X_1 driving another inverter X_2

An ***ideal voltage step*** from 0 to V_{DD} with zero rise/fall time is applied to node A

- How compute the propagation delay t_{pd} , from the input step until node B crosses $V_{DD}/2$?



Transient Response of an Inverter

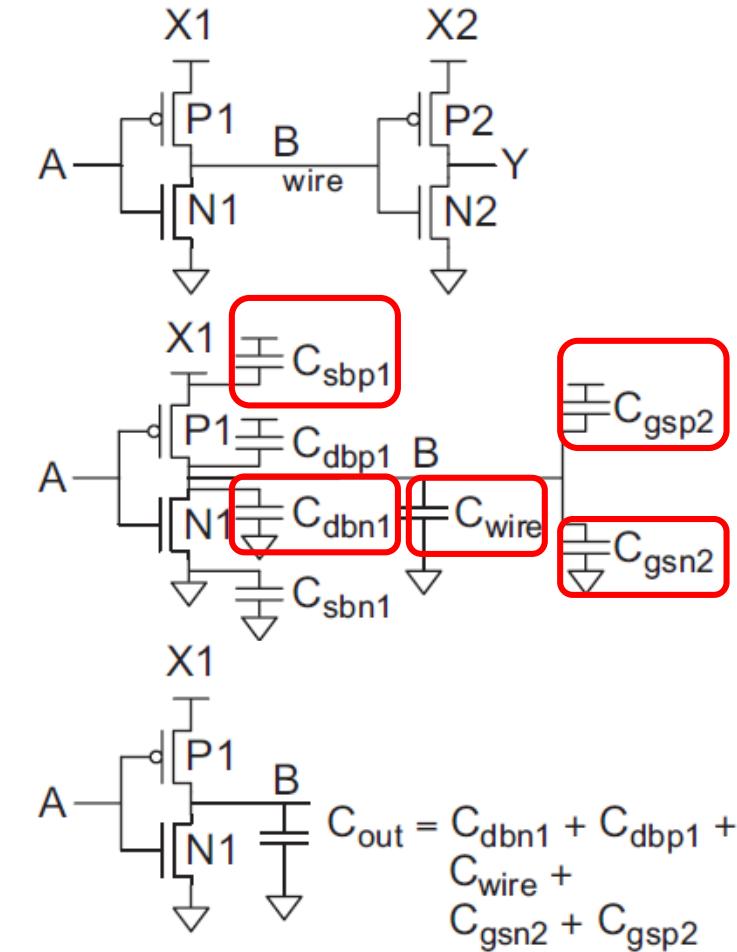
Delay Computation:

1. Build physical model of the circuit

C_{db} and C_{sb} : diffusion capacitances between the drain and body and source and body

C_{gs} : gate capacitance

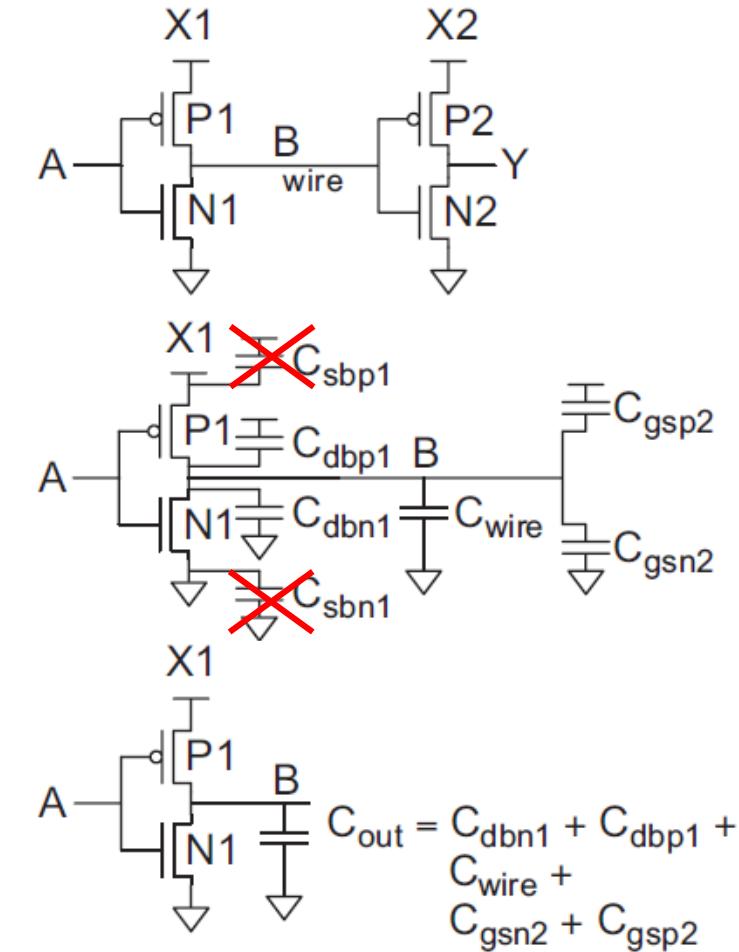
C_{wire} : wire capacitance



Transient Response of an Inverter

Delay Computation:

1. Build physical model of the circuit
 - C_{gs1} and C_d of transistors in $X2$ do not contribute to the switching capacitance: not connected to node B
 - C_{sbn1} and C_{sbp1} do not contribute to the switching capacitance: both terminals tied to constant voltages
 - All the capacitances are lumped into a single load capacitance C_{out}



Transient Response of an Inverter

Delay Computation:

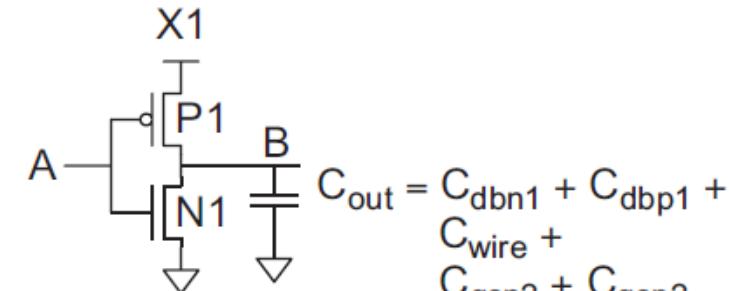
2. Write differential equation of output voltage as a function of input voltage and time

- **Before** the ideal voltage step:

$A = 0$; $N1$ is OFF; $P1$ is ON $\rightarrow B = VDD$

- After the ideal voltage step:

$A = 1$; $N1$ turns ON and $P1$ turns OFF and B drops toward 0



Transient Response of an Inverter

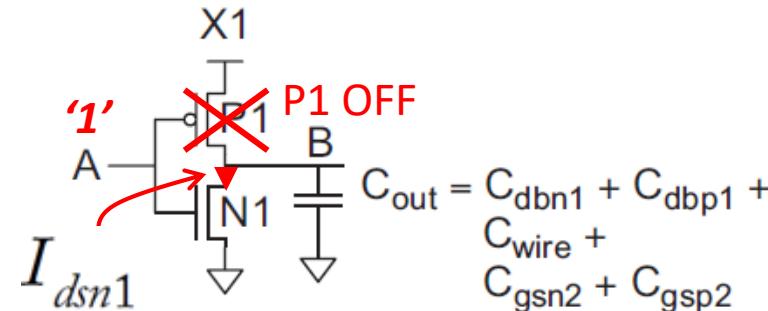
Delay Computation:

2. Write differential equation of output voltage as a function of input voltage and time

- **After** the ideal voltage step:

$A = 1$; $N1$ turns ON and $P1$ turns OFF and B drops toward 0

The current I_{DSN1} discharges C_{out} and depends on whether $N1$ is in linear or saturation regime



The rate of change VB depends on the output capacitance and on the current through $N1$

$$C_{out} \frac{dV_B}{dt} = -I_{dsn1}$$

Transient Response of an Inverter

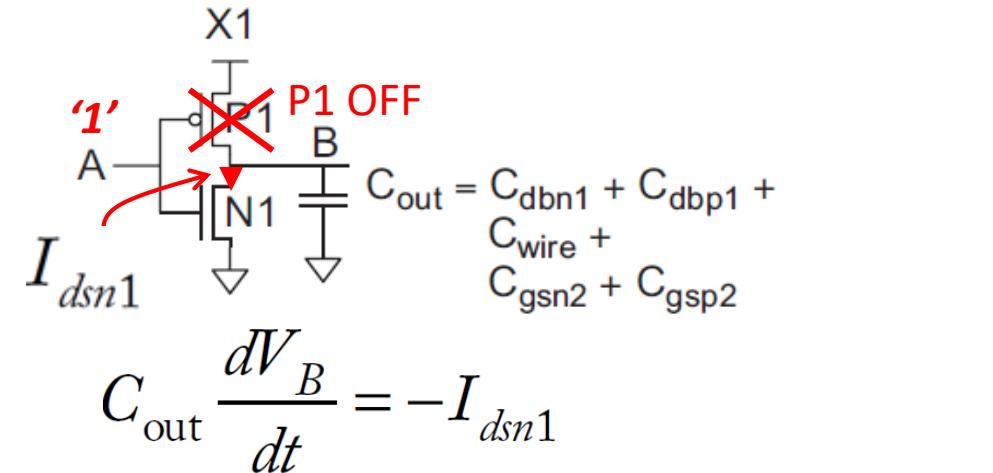
Delay Computation:

2. Write differential equation of output voltage as a function of input voltage and time

After the ideal voltage step :

$A = 1; V_{gsn1} = V_{DD} \rightarrow N1$ turns ON

Initially, $V_{dsn1} = V_B = V_{DD}$
 $\rightarrow V_B > V_{DD} - V_t$
 $\rightarrow N1$ is in saturation



$$\frac{dV_B}{dt} = -\frac{\beta}{C_{out}} \left\{ \begin{array}{ll} \frac{(V_{DD} - V_t)^2}{2} & \text{saturation} \\ \left(V_{DD} - V_t - \frac{V_B}{2} \right) V_B & V_B < V_{DD} - V_t \end{array} \right.$$

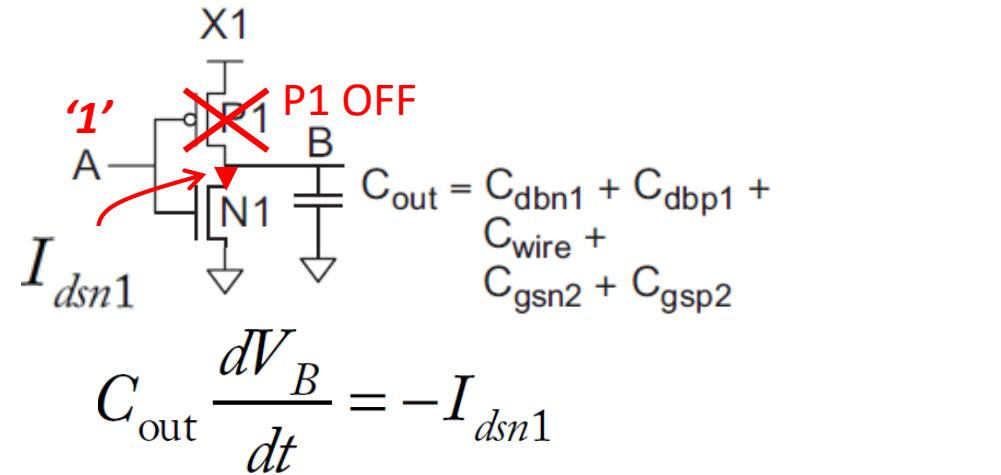
Transient Response of an Inverter

Delay Computation:

2. Write differential equation of output voltage as a function of input voltage and time

As V_B falls below $V_{DD} - V_t$

→ $N1$ enters the linear regime



$$\frac{dV_B}{dt} = -\frac{\beta}{C_{out}}$$

$\frac{(V_{DD} - V_t)^2}{2}$

saturation
 $V_B > V_{DD} - V_t$

$\left(V_{DD} - V_t - \frac{V_B}{2} \right) V_B$

linear
 $V_B < V_{DD} - V_t$

Transient Response of an Inverter

Delay Computation:

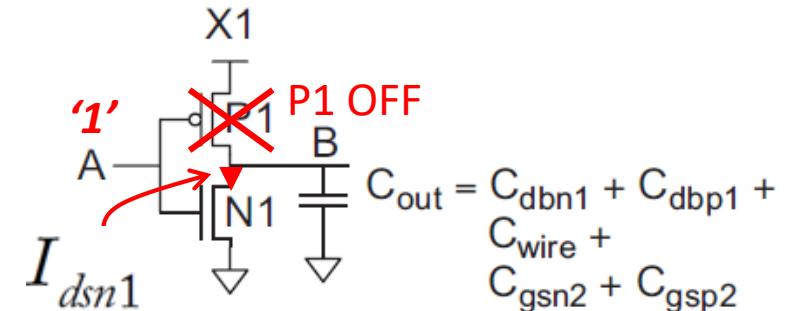
- Write differential equation of output voltage as a function of input voltage and time

- Saturation**

I_{DSN1} is constant and V_B drops linearly until it reaches $VDD - V_t$

- Linear regime**

differential equation nonlinear,
response computed numerically



$$C_{\text{out}} \frac{dV_B}{dt} = -I_{dsn1}$$

$$\frac{dV_B}{dt} = -\frac{\beta}{C_{\text{out}}} \left\{ \begin{array}{ll} \frac{(V_{DD} - V_t)^2}{2} & \text{saturation} \\ \left(V_{DD} - V_t - \frac{V_B}{2} \right) V_B & \text{linear} \end{array} \right.$$

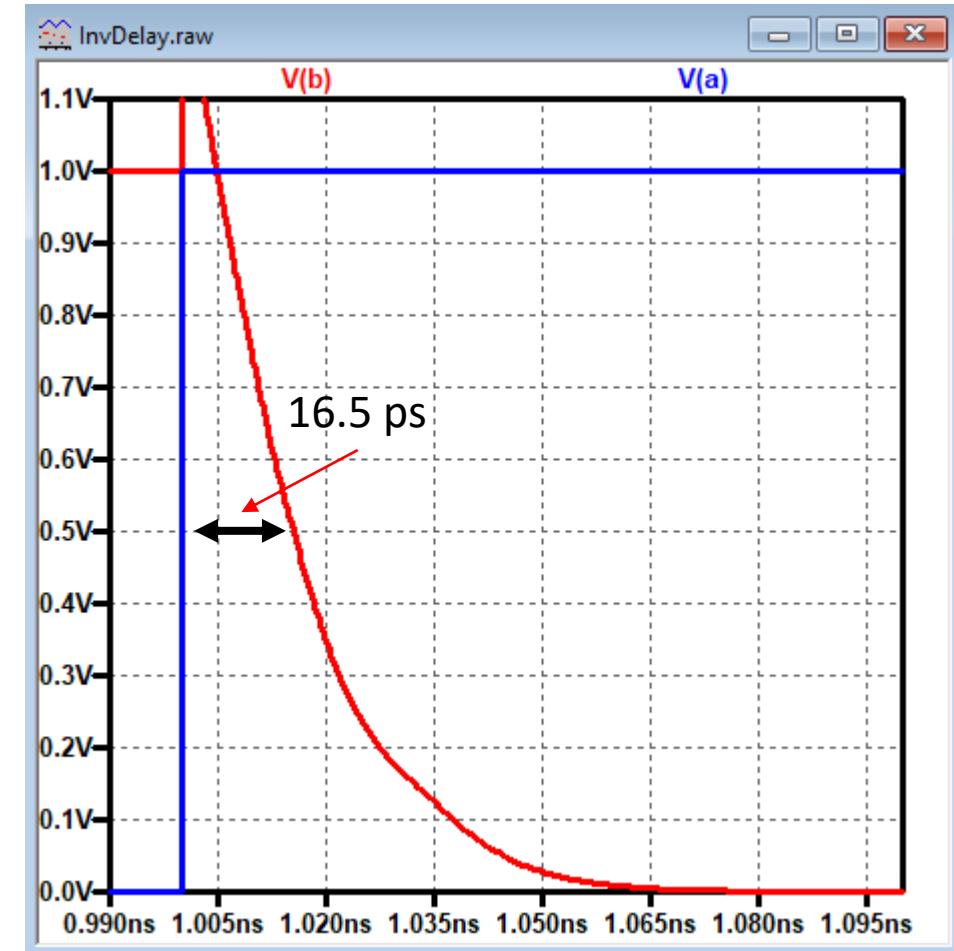
Transient Response of an Inverter

Example: Plot of the response of an inverter to a **rising step** input

The blue line indicates the input voltage $V(A)$, rising at 0.1ps

The red blue line indicates the output voltage, $V(B)$:

- initially it follows a straight line, as the saturated transistor N1 behaves as a constant current source
- Then curves as it approaches 0 and the transistor N1 enters the linear regime



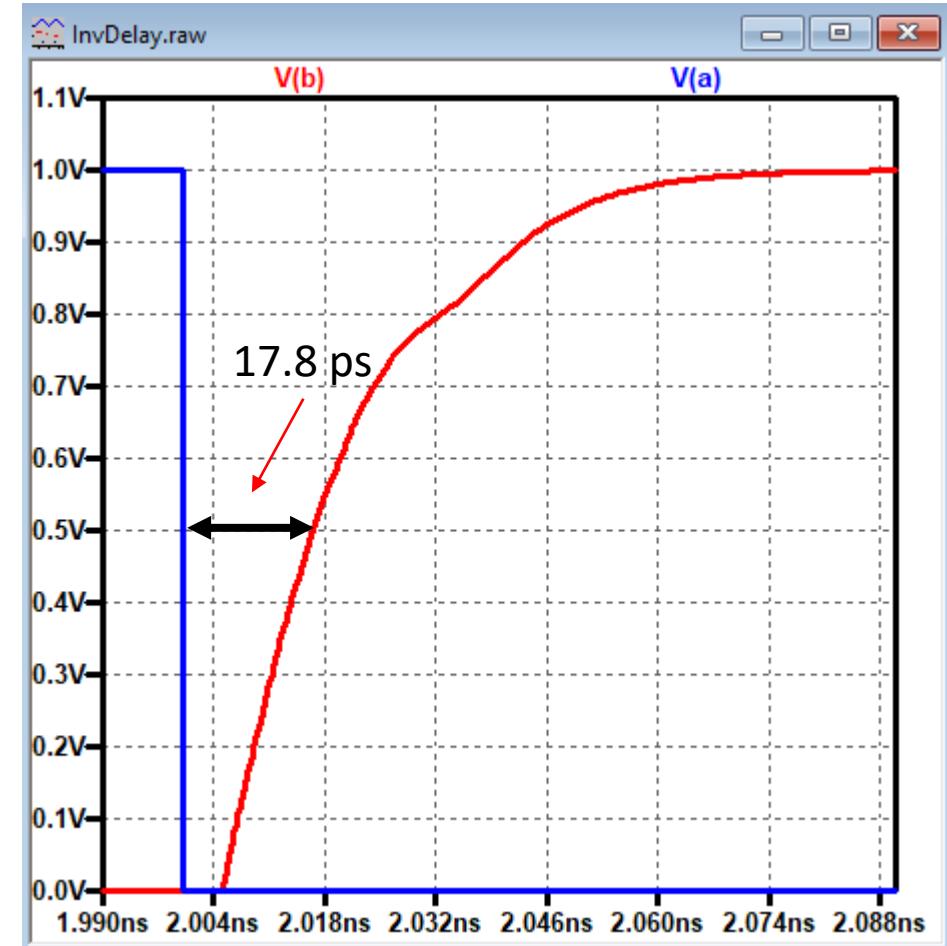
Transient Response of an Inverter

Example: Plot of the response of an inverter to a **falling step** input

The blue line indicates the input voltage $V(A)$, falling at 0.1ps

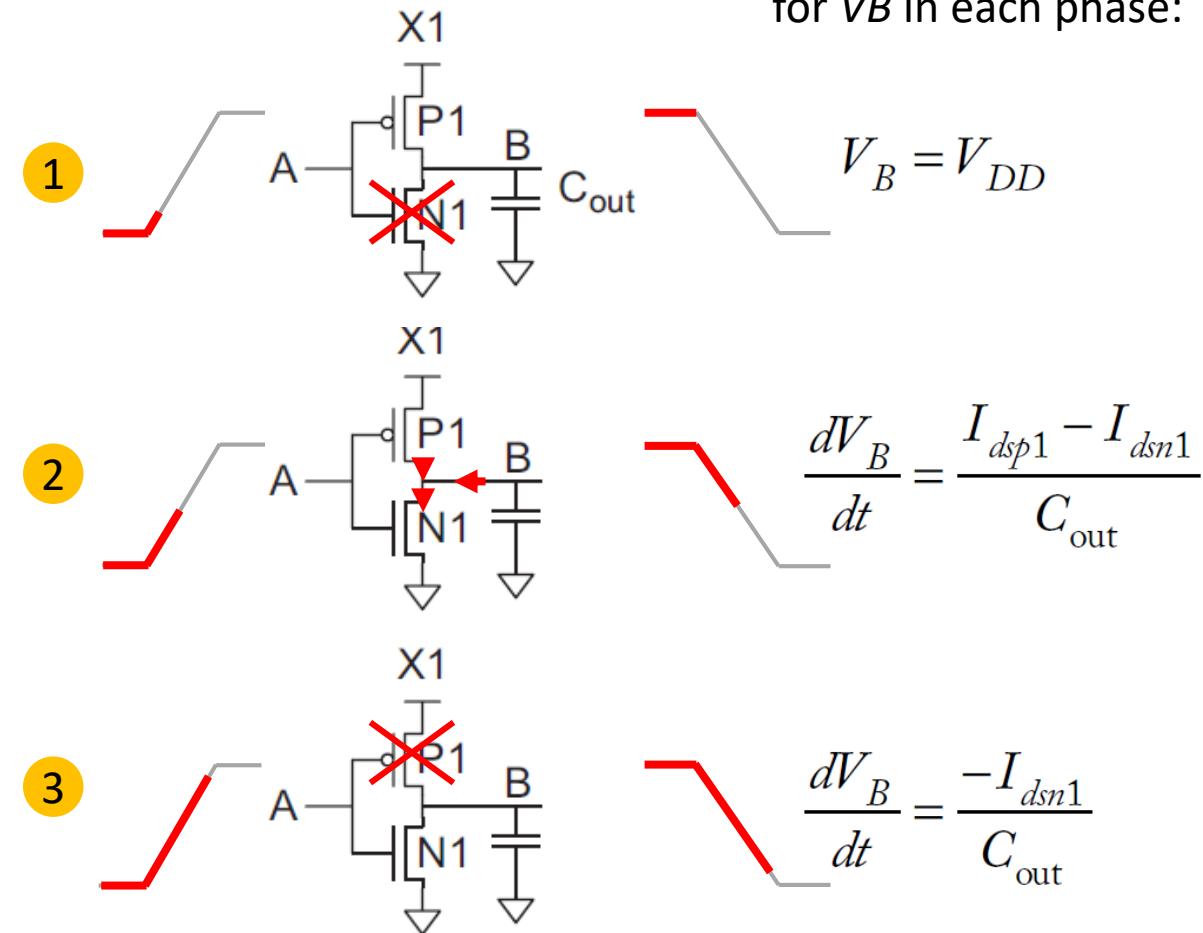
The red blue line indicates the output voltage, $V(B)$:

- initially it follows a straight line, as the saturated transistor P1 behaves as a constant current source
- Then curves as it approaches 0 and the transistor P1 enters the linear regime



Transient Response of an Inverter

- In a real circuit, the input has a **non-zero rise/fall time**
- Three phases:
 1. When A starts to rise, $P1$ is ON and $N1$ remains OFF and B remains at V_{DD}
 2. When A reaches V_{tn} , $P1$ is still ON, $N1$ turns ON and starts to gradually pull B down
 3. When A gets close enough to VDD , $P1$ turns OFF and B falls to 0

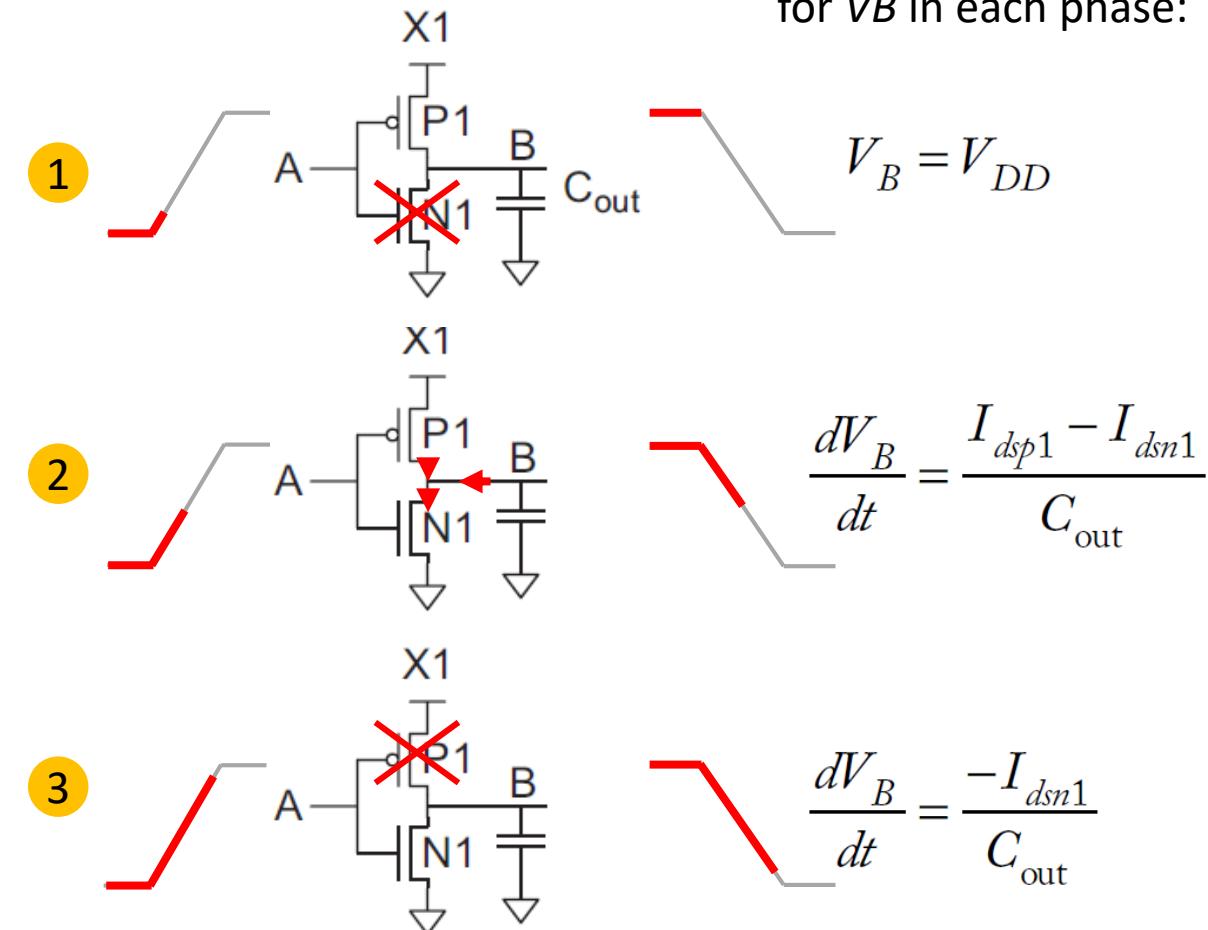


Transient Response of an Inverter

- In a real circuit, the input has a **non-zero rise/fall time**

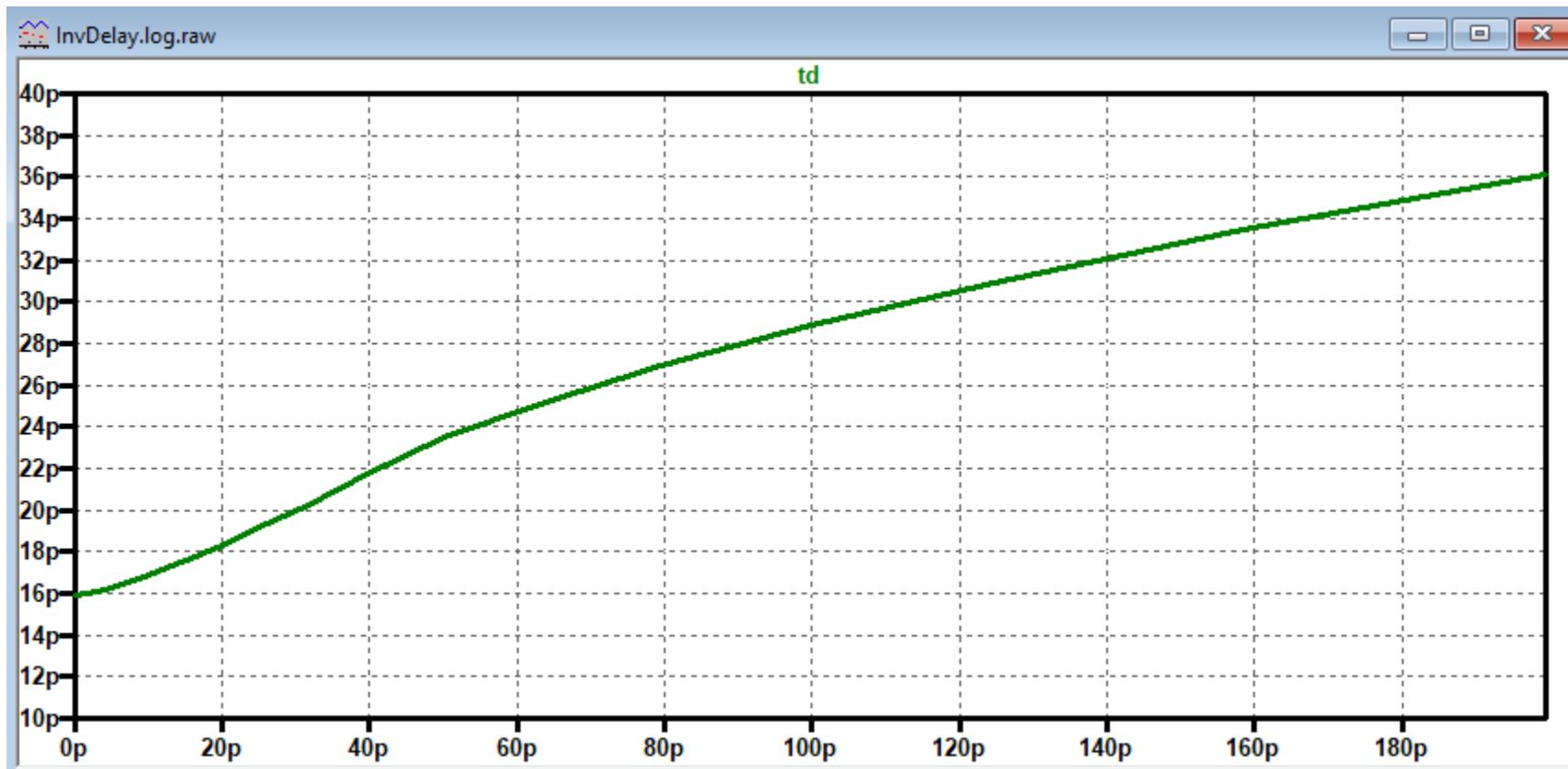
The currents could be estimated using transistor current model

Key observation: the propagation delay increases with **non-zero rise/fall time** because $N1/P1$ is not fully ON right away and because it must struggle with $P1/N1$ in Phase 2



Transient Response of an Inverter

- Plot of average inverter propagation delay vs. input rise time.



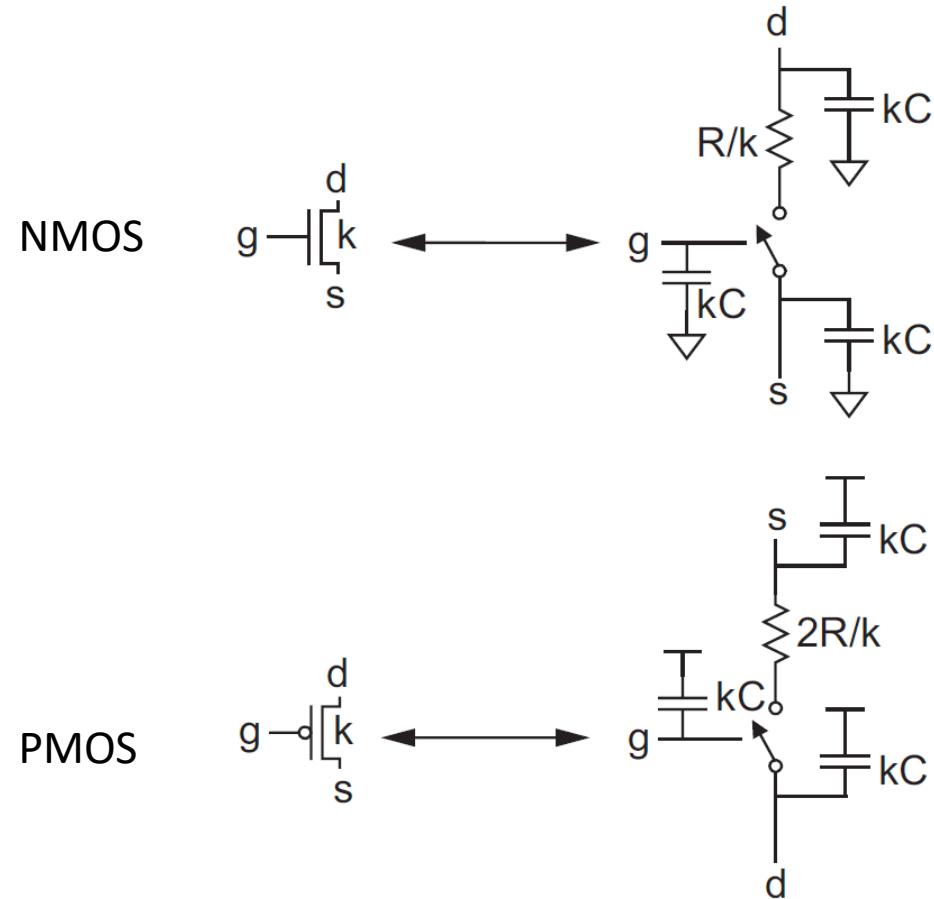
Transient Response of an Inverter

- The physical modelling give good insight on delay
 - delay increases with the output capacitance and decreases with the driver current
- However, equations are nonlinear to solve in closed form
 - simulators solve numerically delay equations and give accurate predictions of delay but offer less insight
- Need of a simpler delay model that offers more insight and tolerable accuracy

RC Delay Model

Nonlinear transistor I-V and C-V characteristics as an average resistance and capacitance over the switching interval

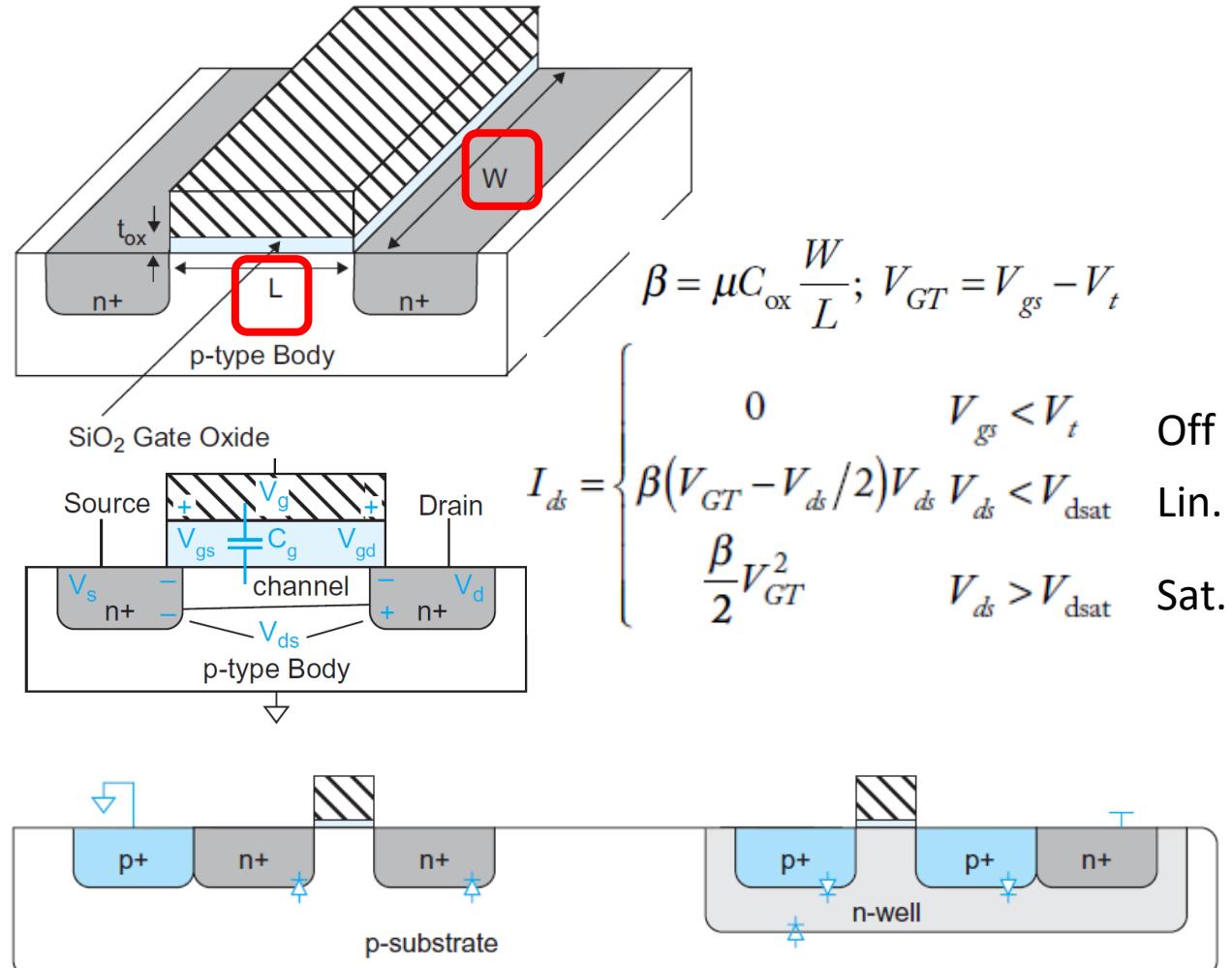
- transistor as a switch in series with a resistor with *effective resistance* + Gate and Diffusion Capacitances



RC Delay Model: Effective Resistance

Effective resistance R is referred to the unit nMOS transistor

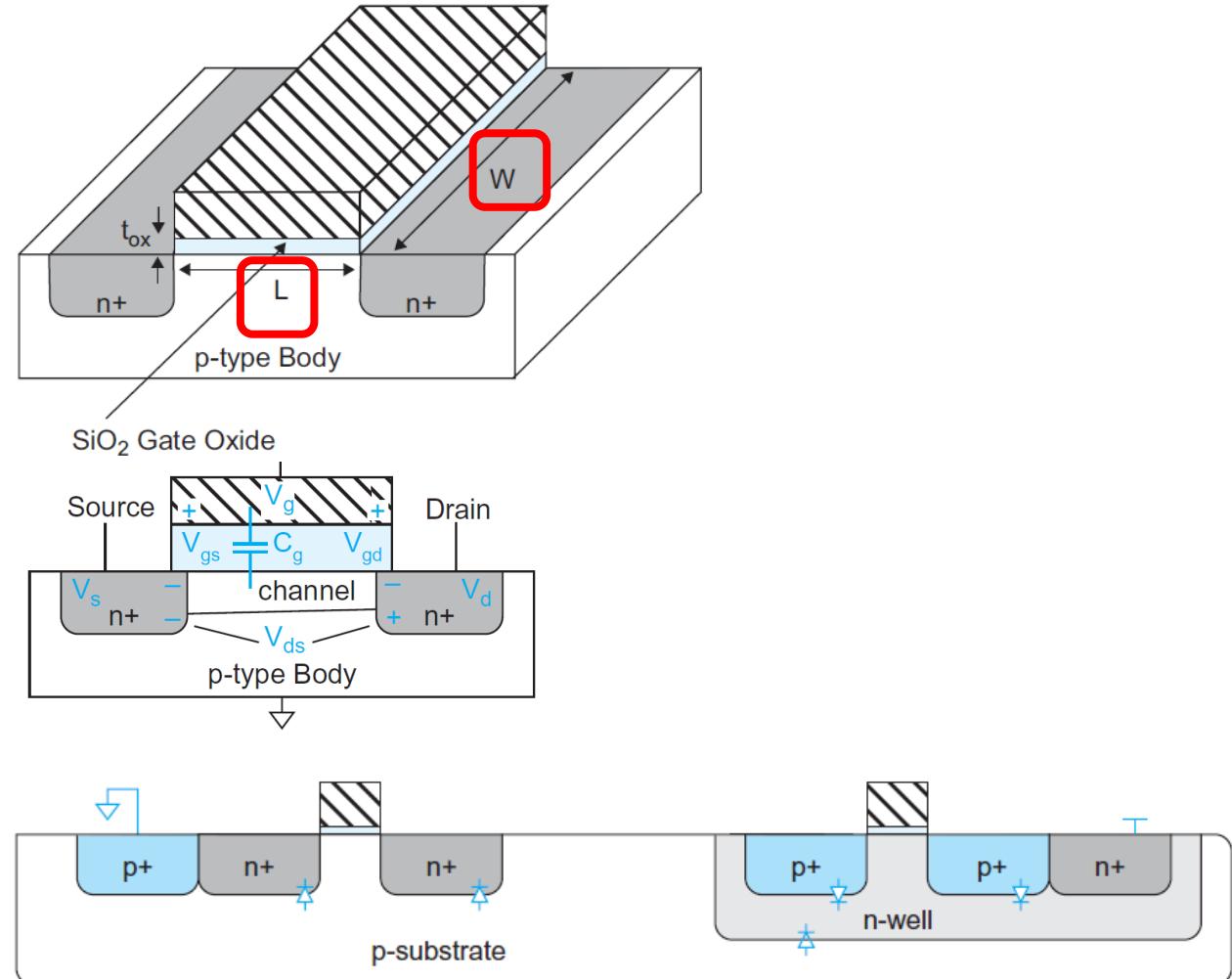
- unit transistor size: minimum length and minimum width
- an nMOS transistor of k times unit width delivers k times as much current → resistance = R/k



Note: Most transistors used in logic are of minimum length for greater speed and lower dynamic power consumption

RC Delay Model: Gate and Diffusion Capacitance

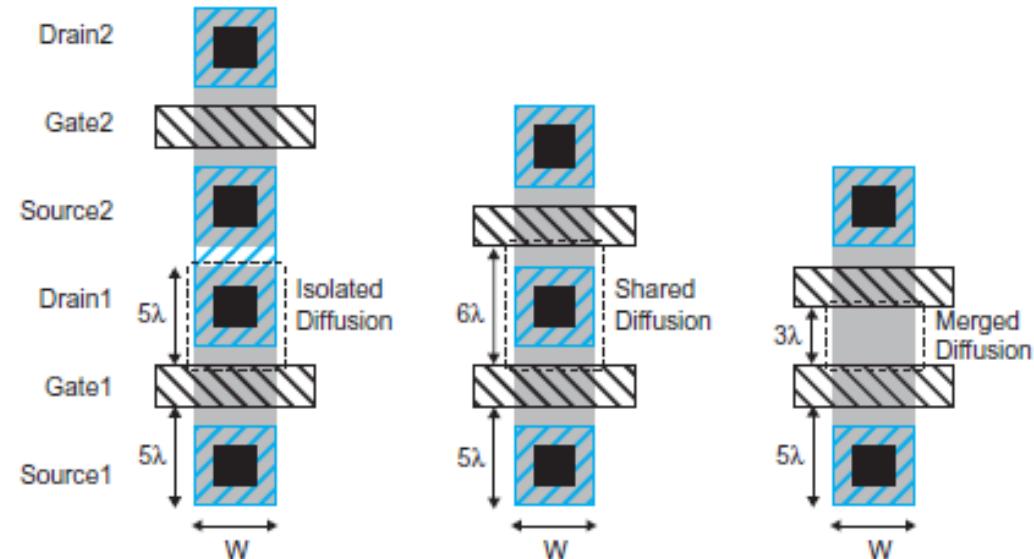
- C to be the gate capacitance of a unit transistor of NMOS
 - A transistor of k times unit width has capacitance kC
 - Increasing channel length increases gate capacitance proportionally
- Diffusion capacitance depends on the size of the source/drain region
 - Wider transistors have proportionally greater diffusion capacitance
 - Increasing channel length does not affect diffusion capacitance



RC Delay Model: Gate and Diffusion Capacitance

- For hand estimation, diffusion capacitances C_{sb} and C_{db} of contacted source and drain regions are comparable to the gate capacitance

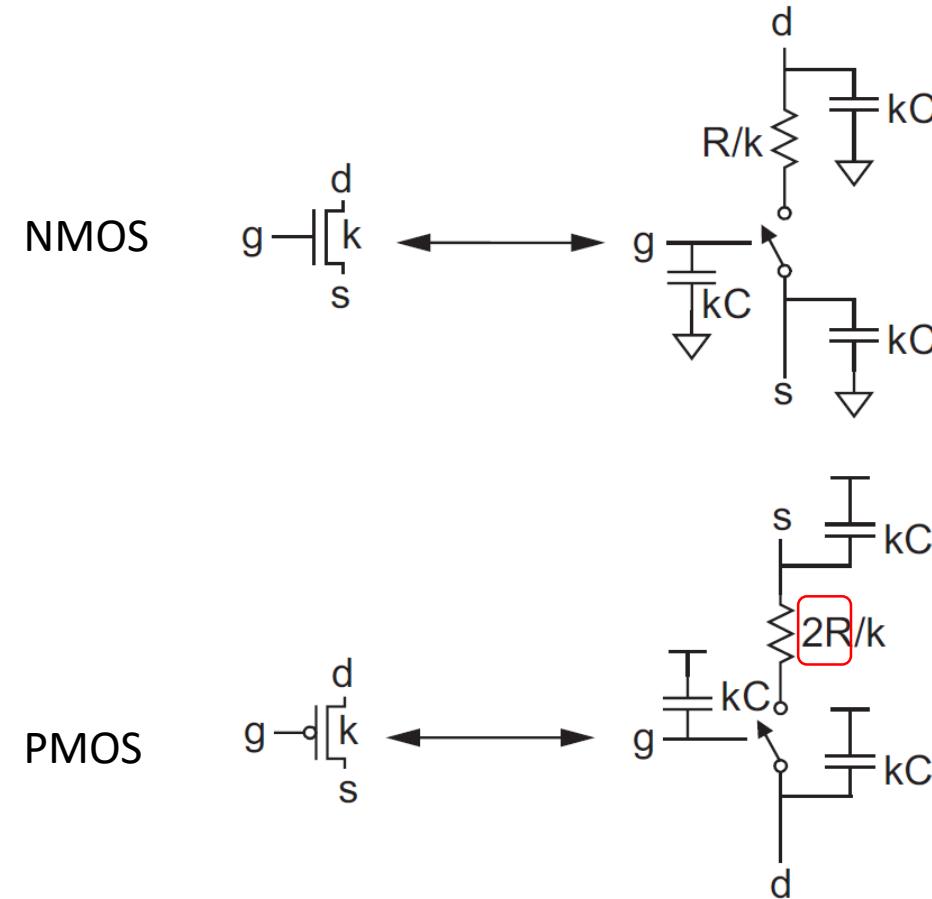
$$C_g = C_{\text{ox}} WL$$



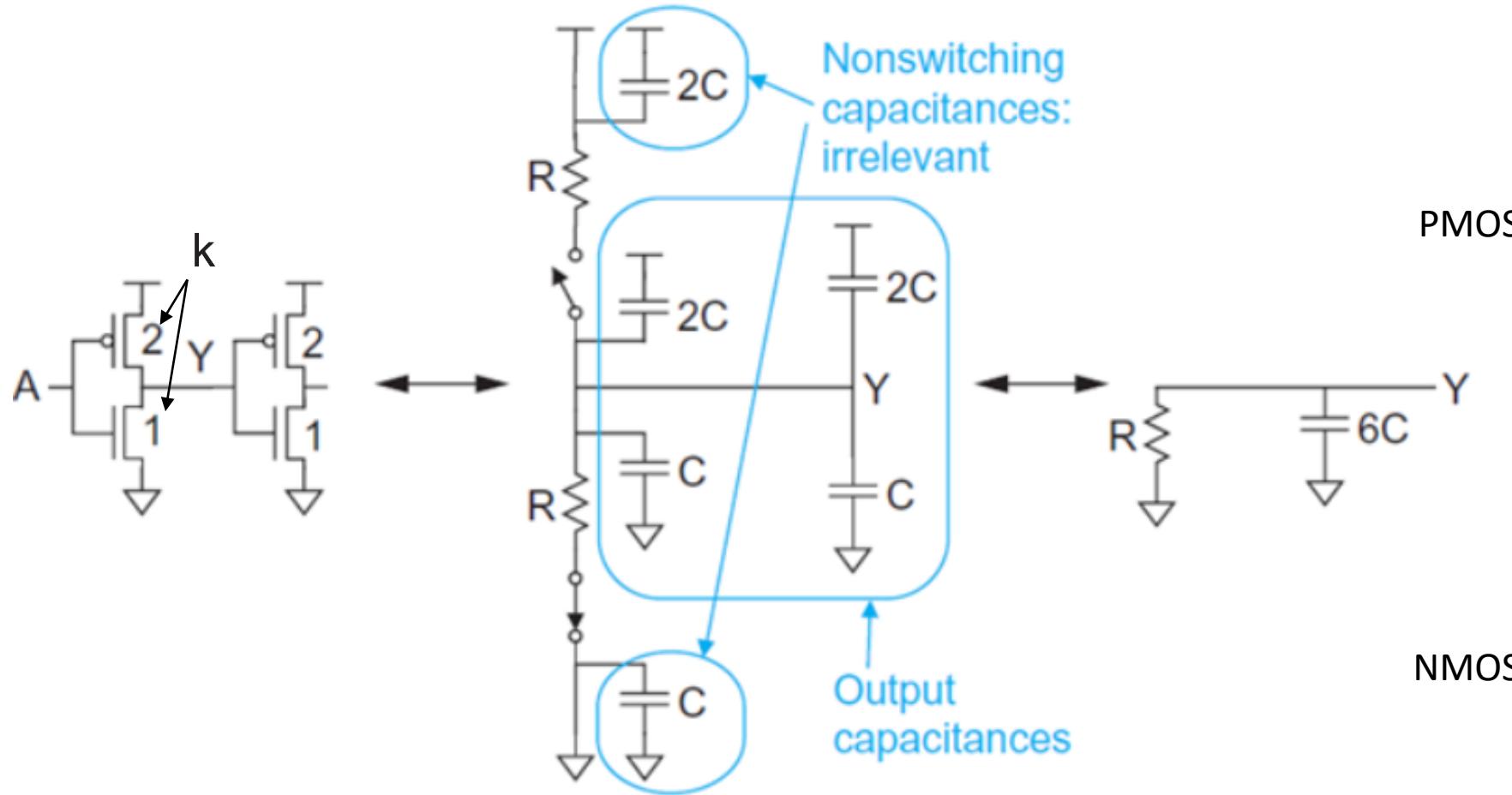
Equivalent RC Circuits

Equivalent RC circuit models for nMOS and pMOS transistors of width k

- the pMOS transistor has approximately **twice the resistance** of the nMOS transistor because holes have lower mobility than electrons



Equivalent RC circuit for an Inverter



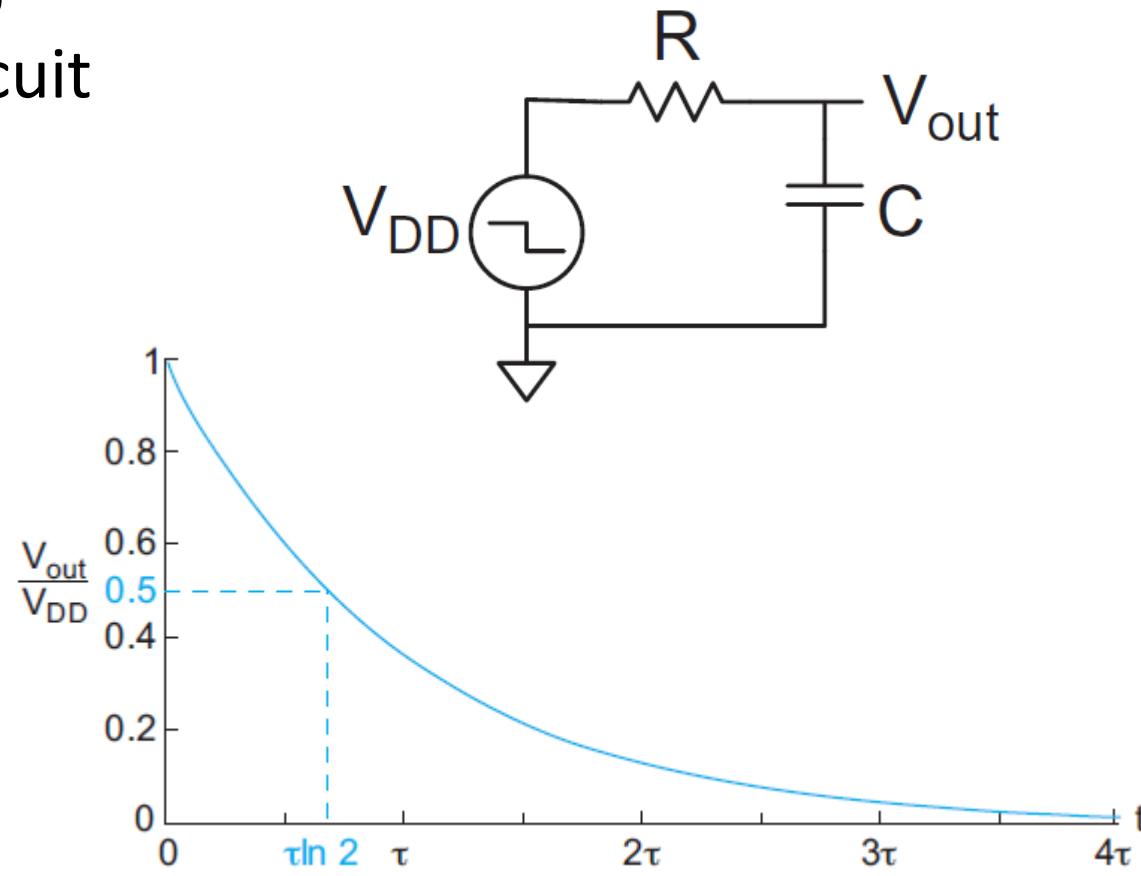
Transient Response for an Inverter

- RC model to estimate the step response of the first-order circuit
- The propagation delay is the time at which V_{out} reaches $V_{DD} / 2$

$$V_{out}(t) = V_{DD} e^{-t/\tau}$$

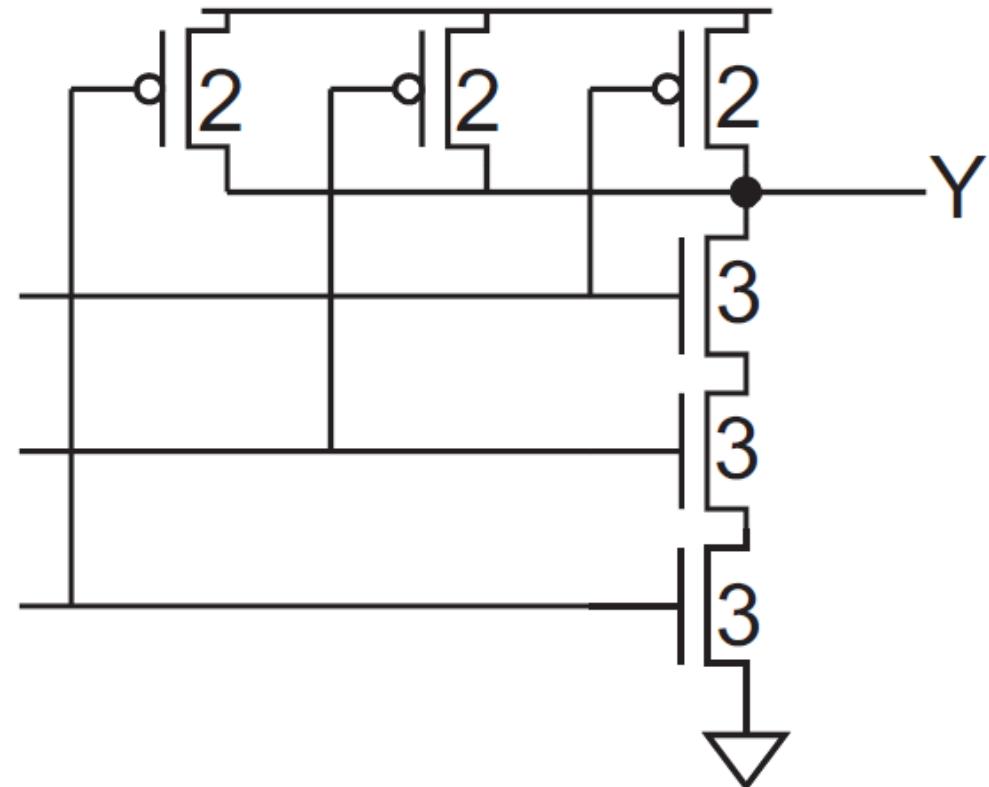
$$\tau = RC$$

$$t_{pd} = RC \ln 2$$



Propagation Delay of Complementary CMOS Gates

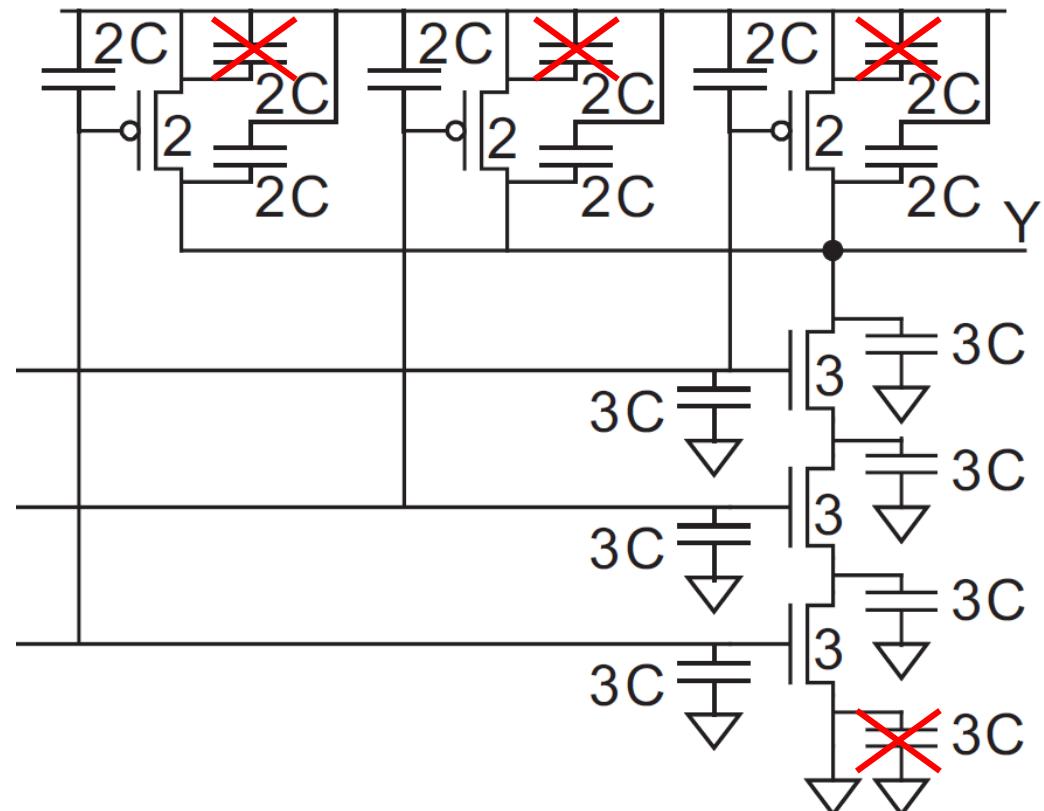
- NAND3 gate with effective rise and fall resistance equal to that of a unit inverter (R)
- three nMOS transistors in series
 - each with resistance $R/3$: the series combination has resistance R
- three pMOS transistors in parallel
 - each with twice unit width: when only one is ON it has resistance R



Propagation Delay of Complementary CMOS Gates

NAND3 gate with capacitances

- Each input presents five units of gate capacitance to whatever circuit drives that input
- pMOS source diffusions capacitors have both terminals shorted together so they are irrelevant to circuit operation

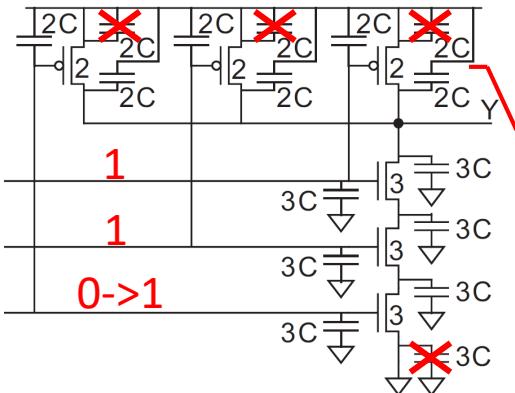


Propagation Delay of Complementary CMOS Gates

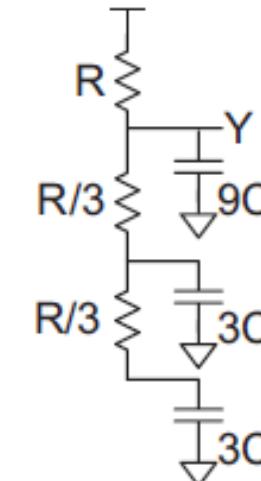
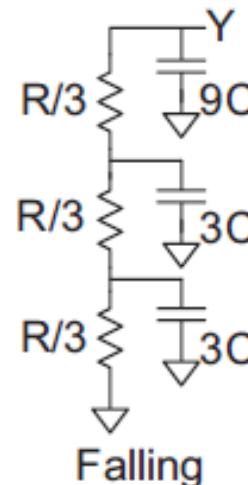
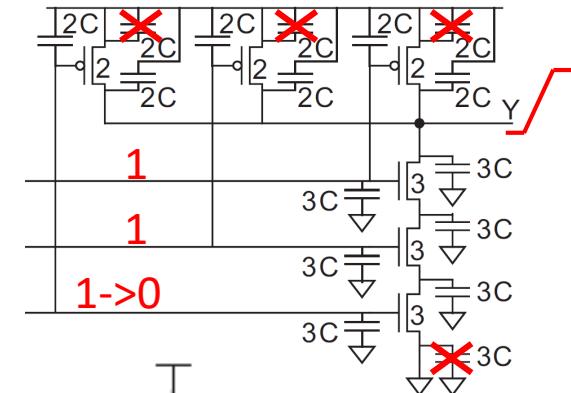
NAND3 gate: equivalent RC model

- worst case falling
 - the upper two inputs are 1 and the bottom one rises to 1
- worst case rising
 - the upper two inputs are 1 and the bottom one falls to 0
 - the output pulls up through a single pMOS transistor

worst case falling



worst case rising

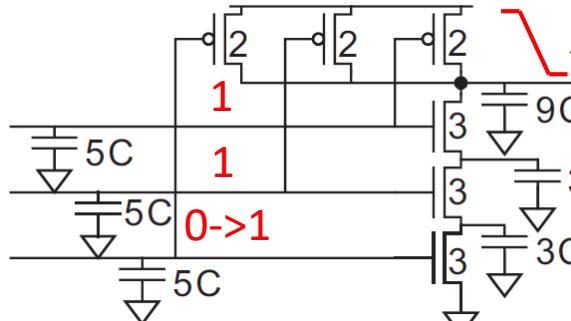


Propagation Delay of Complementary CMOS Gates

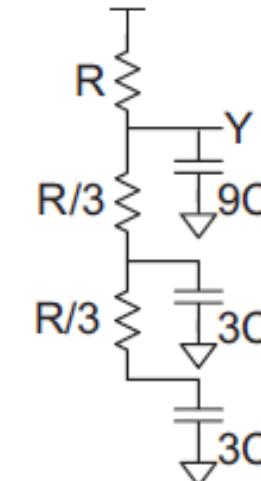
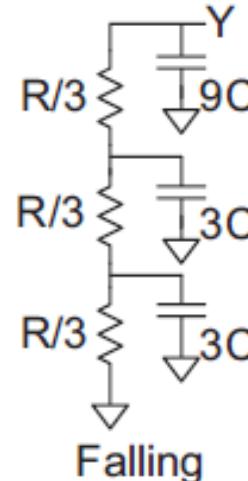
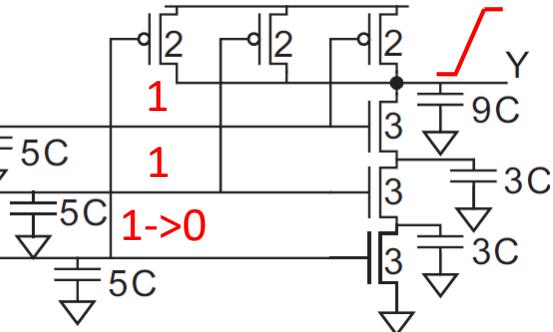
NAND3 gate: equivalent RC model

- Delay? second-order RC system
- complex problem that prevents the simplification of a CMOS circuit into an equivalent RC network!

worst case falling



worst case rising

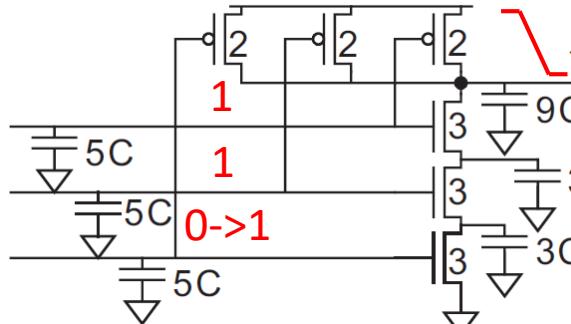


Propagation Delay of Complementary CMOS Gates

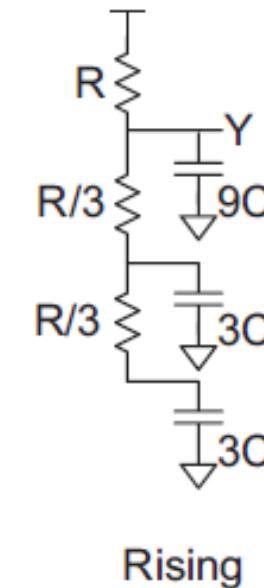
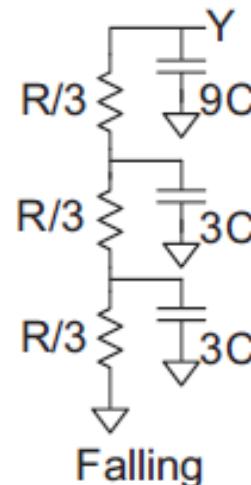
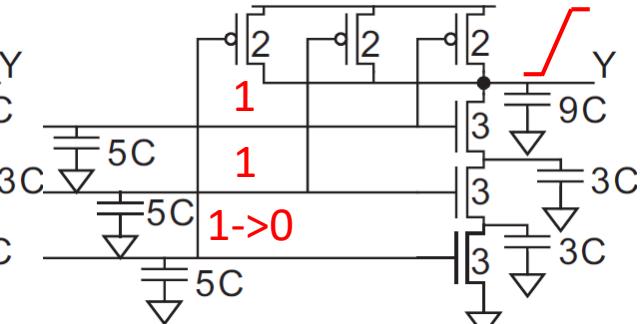
NAND3 gate: equivalent RC model

- Delay? Elmore Delay Model
- The equivalent RC circuit is an *RC tree*, i.e., an RC circuit with no loops

worst case falling



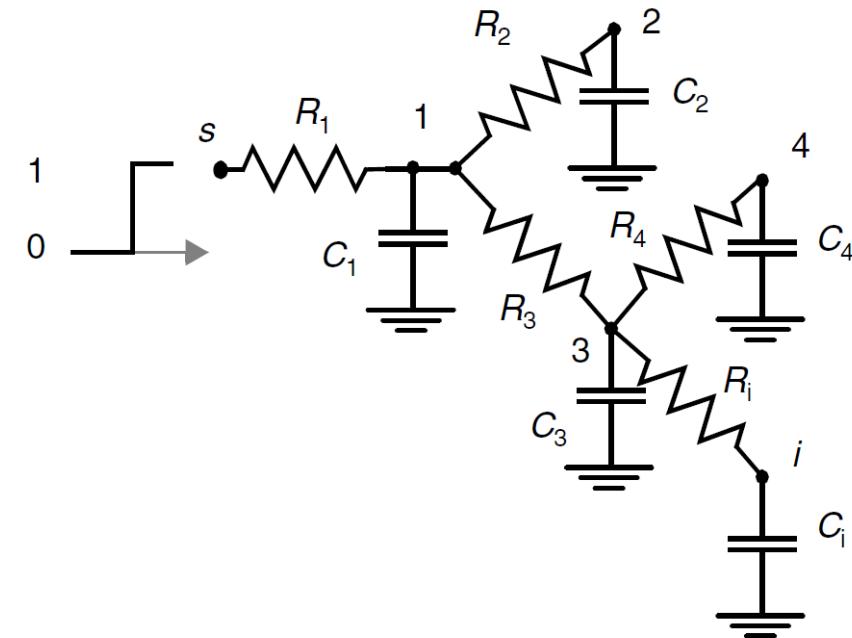
worst case rising



Elmore Delay Model

RC tree network, properties:

- the network has a single input node (s)
- all the capacitors are between a node and the ground
- the network does not contain any resistive loops (which makes it a tree)



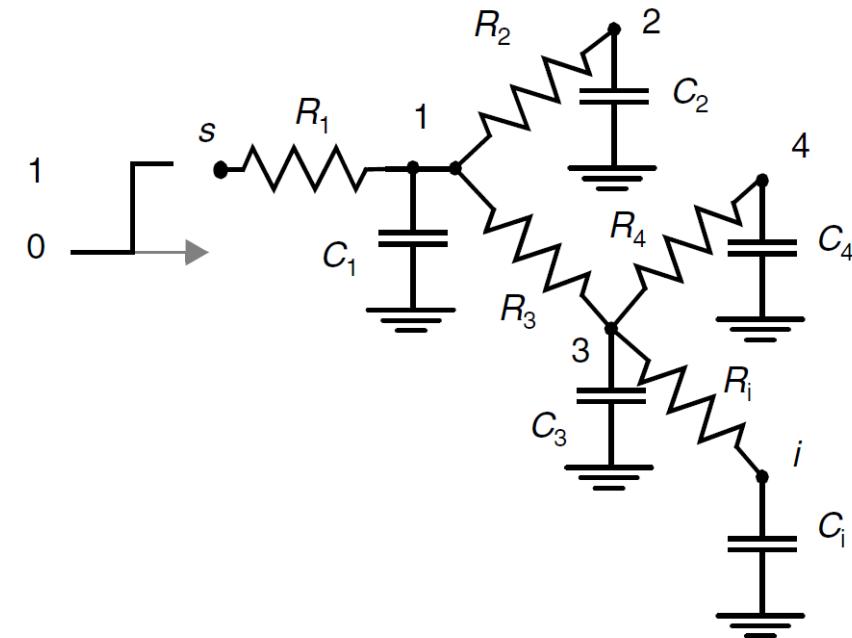
Elmore Delay Model

RC tree network, properties:

there exists a unique resistive path between the source node s and any node i of the network

The total resistance along this path is called the *path resistance* R_{ii}

- resistance between the node s and node 4 equals $R_{s4} = R_1 + R_3 + R_4$
- *shared path resistance* R_{ik} , which represents the resistance shared among the paths from the root node s to nodes k and i
- $R_{i4} = R_1 + R_3$ while $R_{i2} = R_1$.

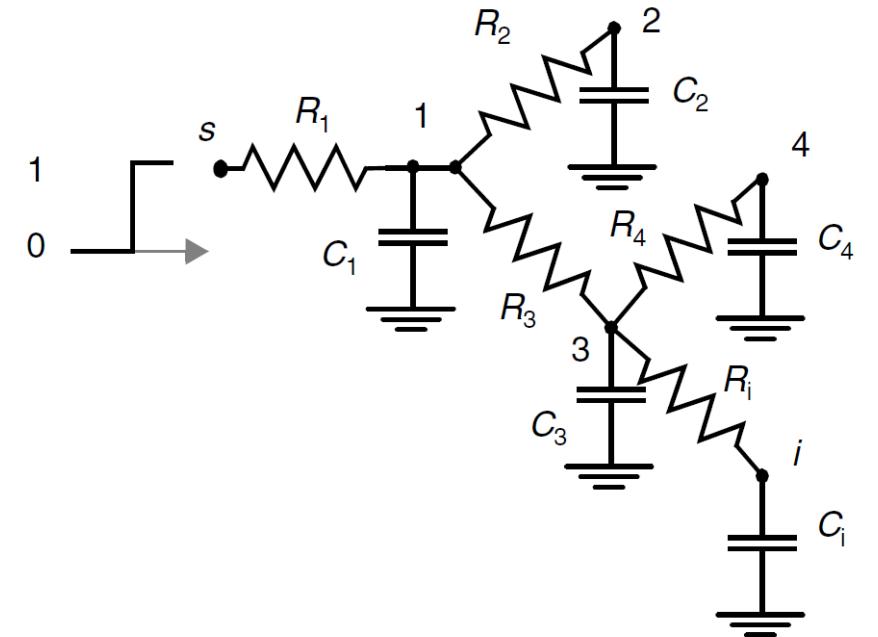


Elmore Delay Model

- Assumption: each of the N nodes of the network is initially discharged to GND
- A step input is applied at node s at time $t = 0$
- The Elmore delay at node i is given by the following expression:

$$\tau_{Di} = \sum_{k=1}^N C_k R_{ik}$$

$$\tau_{Di} = R_1 C_1 + R_1 C_2 + (R_1 + R_3) C_3 + (R_1 + R_3) C_4 + (R_1 + R_3 + R_i) C_i$$



Propagation Delay of Complementary CMOS Gates

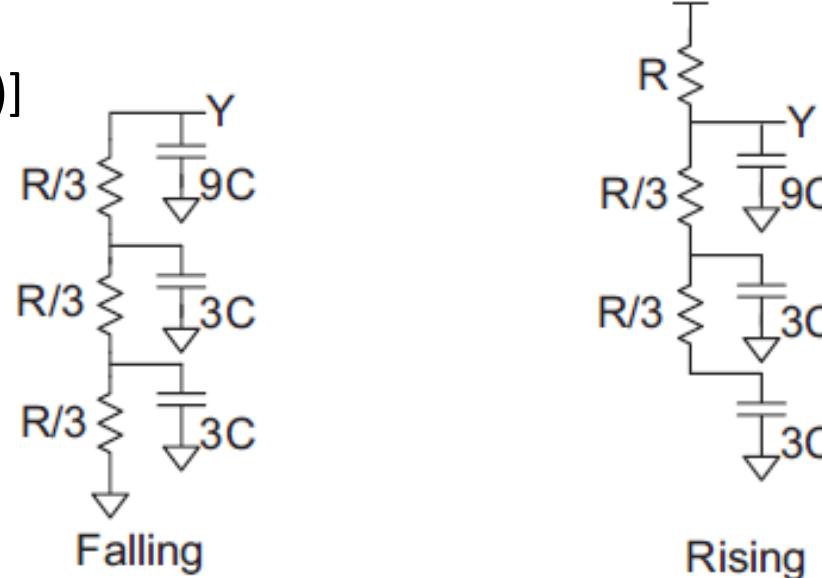
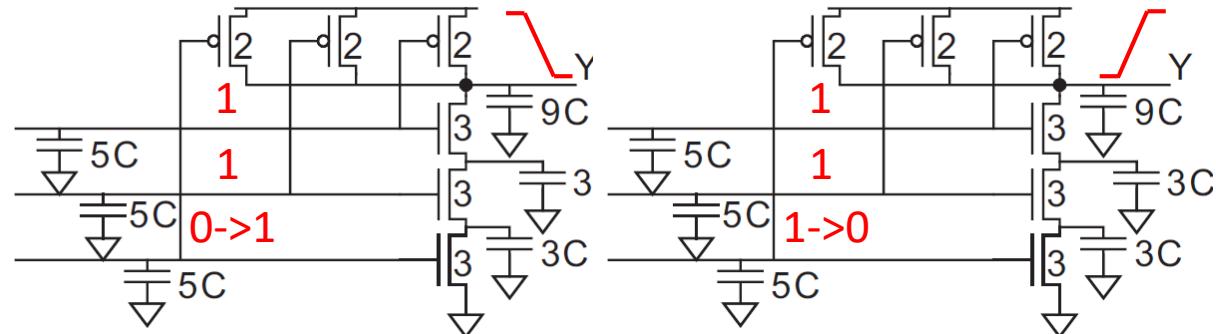
NAND3 gate: implementing Elmore Delay Model

worst case:

$$t_{pdf} = \ln 2 [(3C)(R/3) + (3C)(R/3+R/3) + (9C)(R/3+R/3+R/3)] \\ = \ln 2 (12RC)$$

$$t_{pdr} = \ln 2 [(3C)(R) + (3C)(R) + (9C)(R)] \\ = \ln 2 (15RC)$$

Output not loaded
worst case falling **worst case rising**



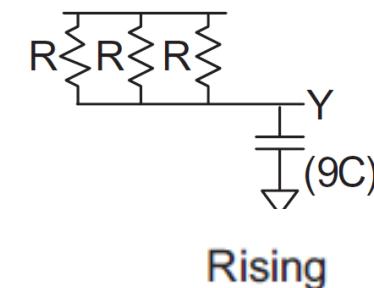
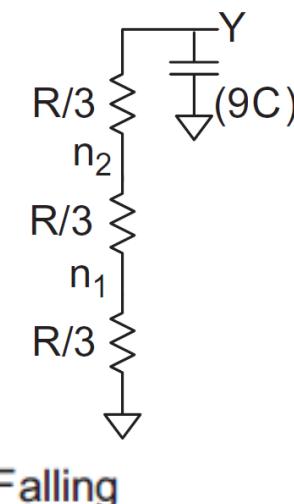
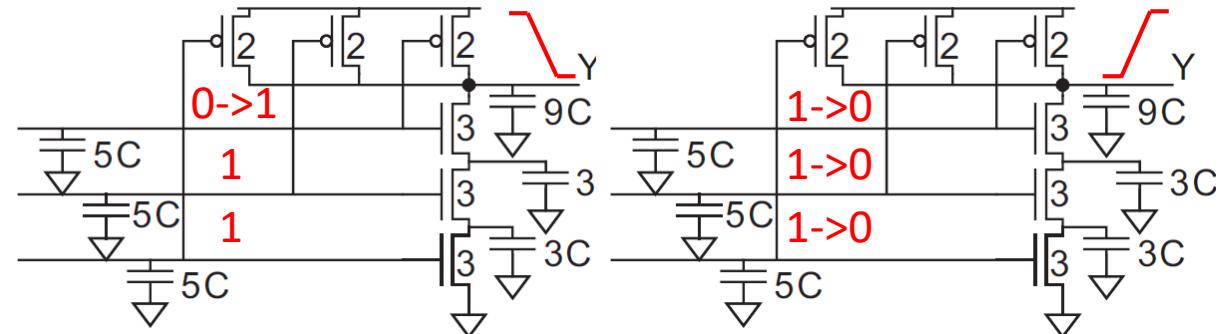
Propagation Delay of Complementary CMOS Gates

NAND3 gate: implementing Elmore Delay Model
 best case: contamination delays

$$t_{cdf} = \ln 2 [(9C)(R/3 + R/3 + R/3)] = \ln 2 (9RC)$$

$$t_{cdr} = \ln 2 [(9C)(R/3)] = \ln 2 (3RC)$$

Output not loaded
worst case falling **worst case rising**



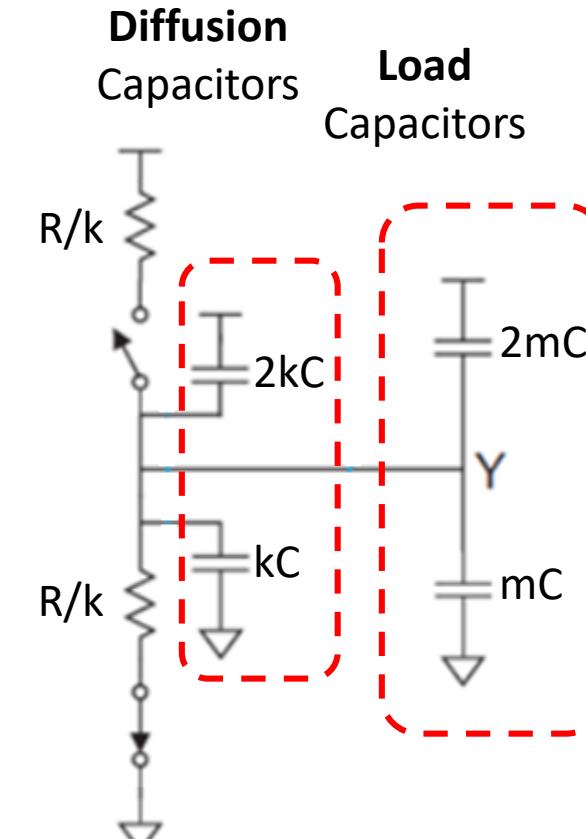
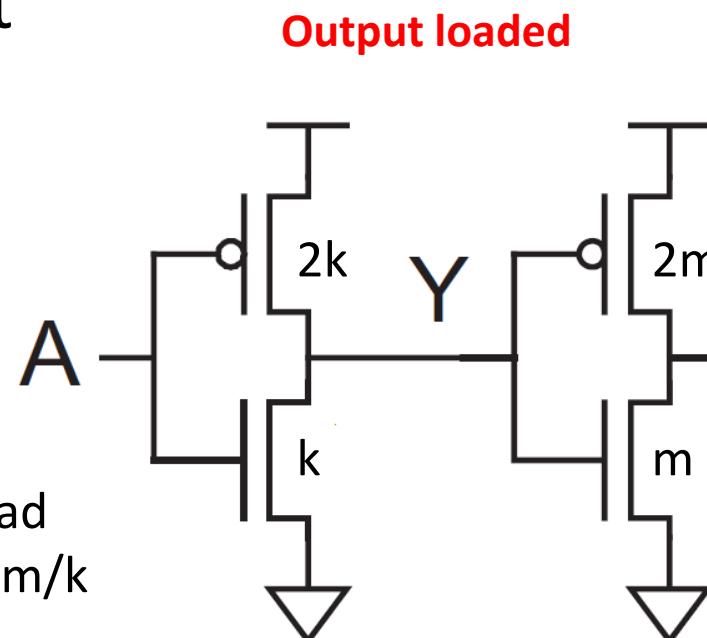
Propagation Delay of an Inverter

- Inverter driving m identical unit inverters

$$t_{pdf} = t_{pdr} = \ln 2(3k + 3m)(C)(R/k) \\ = \ln 2(3 + 3m/k)(RC)$$

fanout or electrical effort h=ratio between load capacitance 3m and input capacitance 3k: $h=m/k$

$$t_{pdf} = t_{pdr} = \ln 2(3k + 3m)(C)(R/k) \\ = \ln 2(1+h)(3RC) = (1+h)\tau \text{ with } \tau = \ln 2 * 3RC$$



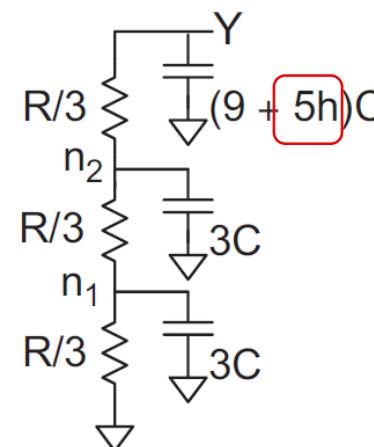
Propagation Delay of Complementary CMOS Gates

NAND3 gate driving h identical
NAND3 gates

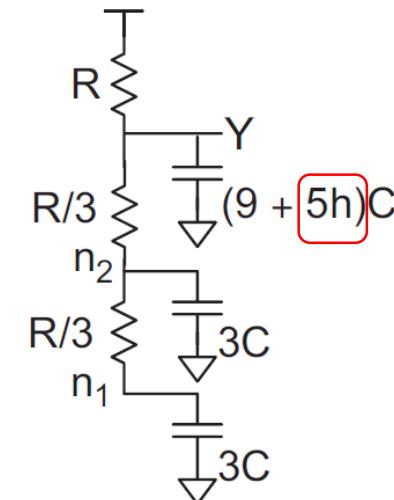
worst case:

$$\begin{aligned} t_{pd़} &= \ln 2[(3C)(R/3) + (3C)(R/3+R/3) + (9C+5hC)(R/3+R/3+R/3)] \\ &= \ln 2(12+5h)RC = \ln 2(4+5/3h)3RC = (4+5/3h)\tau \end{aligned}$$

$$\begin{aligned} t_{pd़r} &= \ln 2[(3C)(R) + (3C)(R) + (9C+5hC)(R)] = \\ &= \ln 2(15+5h)RC = (5+5/3h)\tau \end{aligned}$$



Falling



Rising

Propagation Delay of Complementary CMOS Gates

NAND3 gate driving h identical NAND3 gates

Normalized delay $t_{pd}/\tau = d = (p + f)$ consists of two components:

1. *p: parasitic delay*

- time for a gate to drive its own internal diffusion capacitance
- ideally independent of the gate size, increasing the width of the transistors decreases the resistance but increases the capacitance

2. *f: effort delay, it depends on:*

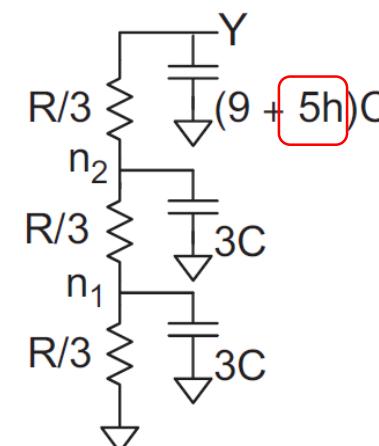
- electrical effort* h , ratio of external load capacitance to input capacitance and thus changes with transistor widths
- logical effort* the gate g , ratio of the input capacitance of the gate to the input capacitance of an inverter that can deliver the same output current

$$t_{pdf}/\tau = (4+5/3h)$$

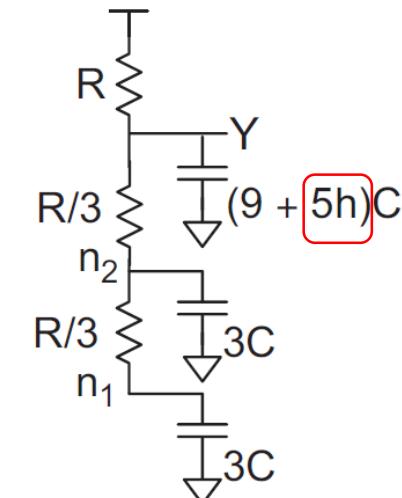
$$d = (p+gh)$$

$$t_{pdr}/\tau = (5+5/3h)$$

NAND3: parasitic delay of 5 and a logical effort of $5/3$



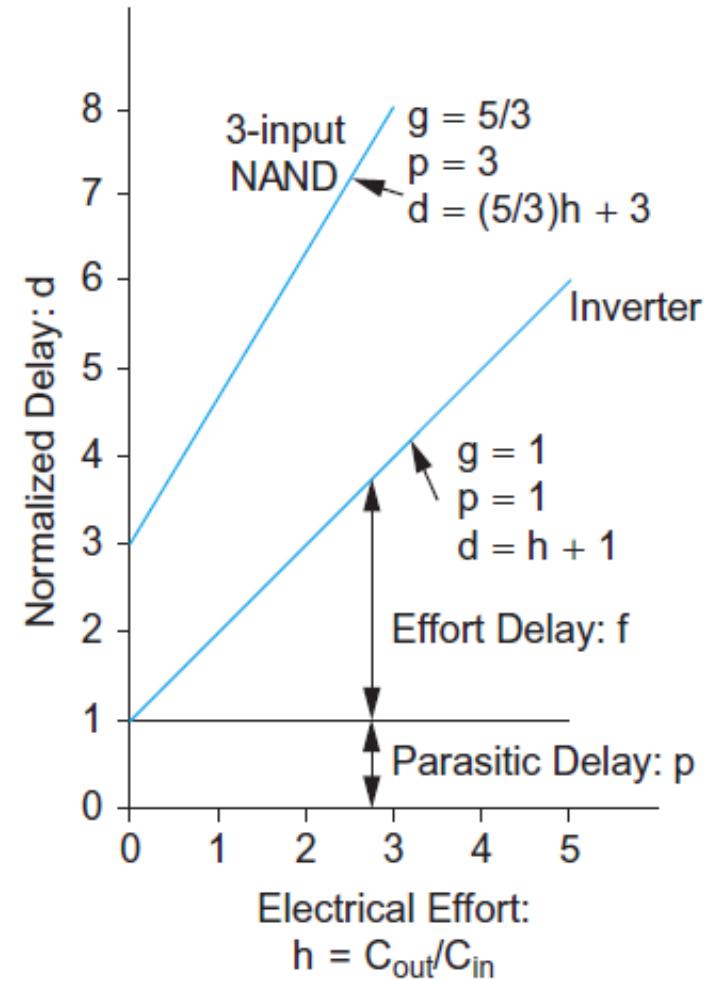
Falling



Rising

Linear Delay Model

- Linear delay model of a logic gate $d = (p+gh)$ plotted as a function of the fanout (electrical effort h) for an inverter and for a NAND3 gate
- The slope of the line is the *logical effort* g , its intercept is the *parasitic delay* p
- We can adjust the delay by
 - adjusting the effective fanout (by transistor sizing)
 - choosing a logic gate with a different logical effort



Common Gates Parameters

Parasitic Delay

| Gate Type | Number of Inputs | | | | |
|-----------------------|------------------|---|---|---|------|
| | 1 | 2 | 3 | 4 | n |
| inverter | 1 | | | | |
| NAND | | 2 | 3 | 4 | n |
| NOR | | 2 | 3 | 4 | n |
| tristate, multiplexer | 2 | 4 | 6 | 8 | $2n$ |

Logical Effort

- NANDs are better than NORs
- Gates with few inputs are better than gates with many

| Gate Type | Number of Inputs | | | | |
|-----------------------|------------------|------|----------|--------------|--------------|
| | 1 | 2 | 3 | 4 | n |
| inverter | 1 | | | | |
| NAND | | 4/3 | 5/3 | 6/3 | $(n + 2)/3$ |
| NOR | | 5/3 | 7/3 | 9/3 | $(2n + 1)/3$ |
| tristate, multiplexer | 2 | 2 | 2 | 2 | 2 |
| XOR, XNOR | | 4, 4 | 6, 12, 6 | 8, 16, 16, 8 | |

Delay of a Multistage Network

- How to choose the fastest circuit topology and gate sizes for a specific logic function ?
- How to estimate the delay of the design?
- **Logical Effort method** for best topology and number of stages of logic for a function

Delay of a Multistage Network

Logical Effort Method

- G : path logical effort

$$G = \prod g_i$$

- H : path electrical effort
- path effort F

$$H = \frac{C_{\text{out(path)}}}{C_{\text{in(path)}}}$$

Is $F=GH$? NO in branching paths

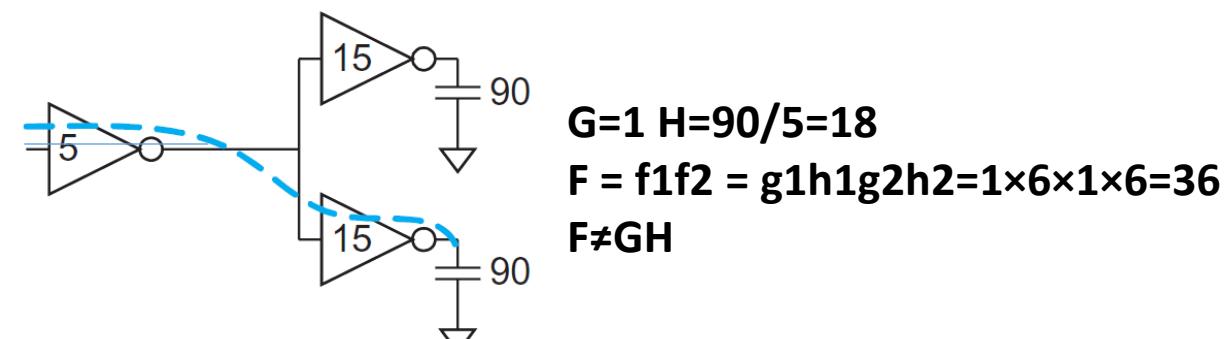
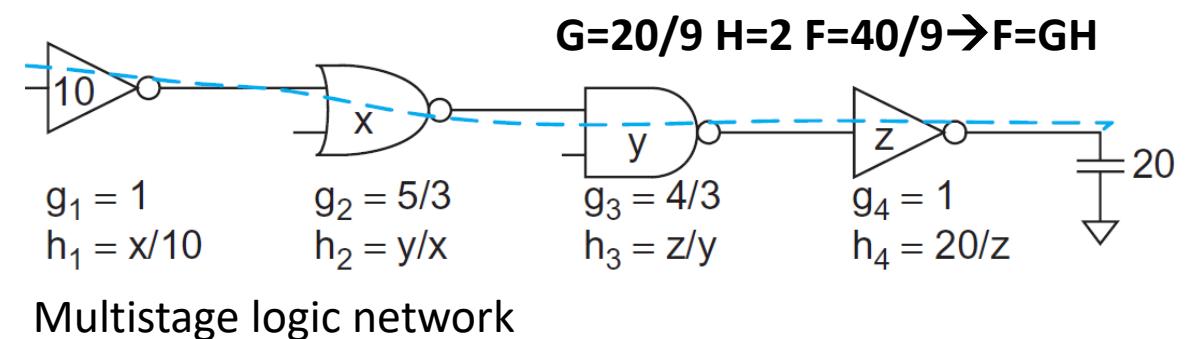
$$F = \prod f_i = \prod g_i h_i$$

- b : branching effort
- B path branching effort

$$b = \frac{C_{\text{onpath}} + C_{\text{offpath}}}{C_{\text{onpath}}}$$

$$B = \prod b_i$$

$$F = GBH$$



Network with two-way branch

Delay of a Multistage Network

- *path delay D*

$$D = \sum d_i = D_F + P$$

- *path effort delay D_F*

$$D_F = \sum f_i$$

- *path parasitic delay P*

$$P = \sum p_i$$

- The product of the stage efforts is F , independent of gate sizes
- The path effort delay D_F is the sum of the stage efforts
- The sum of a set of numbers whose product is constant is minimized by choosing all the numbers to be equal
- The path delay is minimised when each stage sustains the same effort

Delay of a Multistage Network

- If a path has N stages and each sustains the same effort, that effort must be:

$$\hat{f} = g_i b_i = F^{1/N}$$

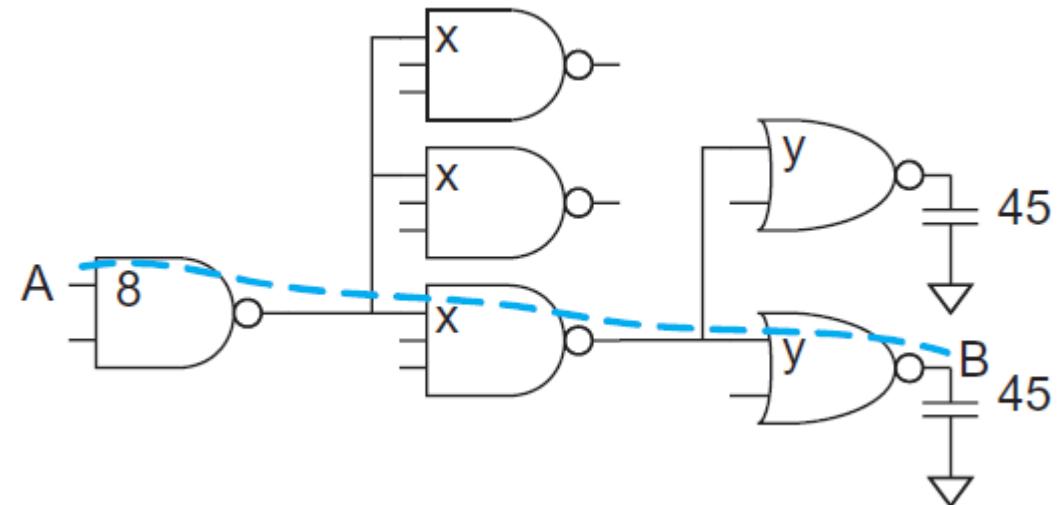
- The minimum possible delay of an N -stage path with path effort F and path parasitic delay P is:

$$D = NF^{1/N} + P$$

- The minimum delay of the path can be estimated knowing only the number of stages N , path effort F , and parasitic delays P without the need to assign transistor sizes

Delay of a Multistage Network: Exercise

- Estimate the minimum delay of the path from A to B
- choose transistor sizes to achieve this delay.
- The initial NAND2 gate may present a load of 8 of transistor width on the input and the output load is equivalent to 45 of transistor width

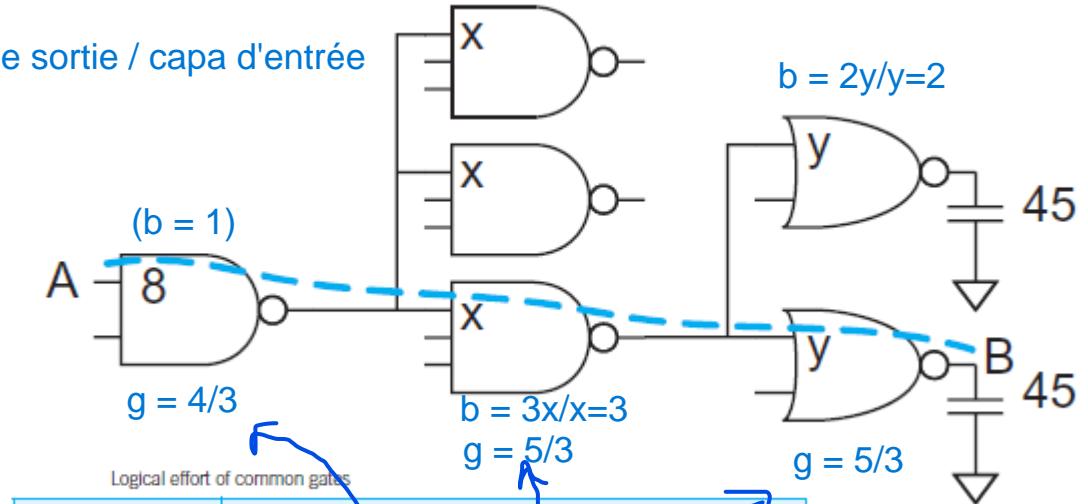


Delay of a Multistage Network: Exercise

multiplication de tous les g

- path logical effort $G = (4/3) \times (5/3) \times (5/3) = 100/27$
- path electrical effort $H = 45/8$ capa de sortie / capa d'entrée
- path branching effort $B = 3 \times 2 = 6$
- path effort $F = BGH = 125$
- best stage effort ($N=3$)
 $f = \sqrt[3]{125} = 5$
- path parasitic delay $P = 2+3+2 = 7$
- minimum path delay $D = 3 \times 5 + 7 = 22$ in units of τ

| Gate Type | Number of Inputs | | | | |
|-----------------------|------------------|---|---|---|------|
| | 1 | 2 | 3 | 4 | n |
| inverter | 1 | | | | |
| NAND | | 2 | 3 | 4 | n |
| NOR | | 2 | 3 | 4 | n |
| tristate, multiplexer | 2 | 4 | 6 | 8 | $2n$ |



| Gate Type | Number of inputs | | | | |
|-----------------------|------------------|------|----------|--------------|--------------|
| | 1 | 2 | 3 | n | |
| inverter | 1 | | | | |
| NAND | | 4/3 | 5/3 | 6/3 | ($n+2$)/3 |
| NOR | | 5/3 | 7/3 | 9/3 | (2 $n+1$)/3 |
| tristate, multiplexer | 2 | 2 | 2 | 2 | 2 |
| XOR, XNOR | | 4, 4 | 6, 12, 6 | 8, 16, 16, 8 | |

Delay of a Multistage Network: Exercise

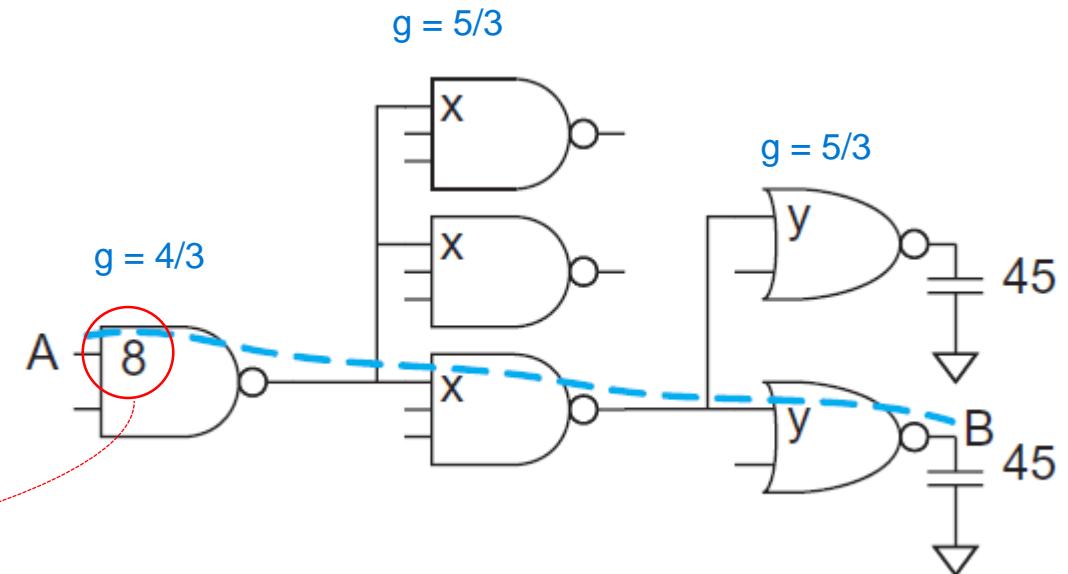
- Using capacitance transformation formula:

$$C_{\text{in}_i} = \frac{C_{\text{out}_i} \times g_i}{\hat{f}}$$

$$\bullet y = C_{\text{in}_3} = 45 \times (5/3) / 5 = 15$$

$$\bullet x = C_{\text{in}_2} = (15+15) \times (5/3) / 5 = 10$$

$$\bullet 8 = (10+10+10) \times (4/3) / 5$$

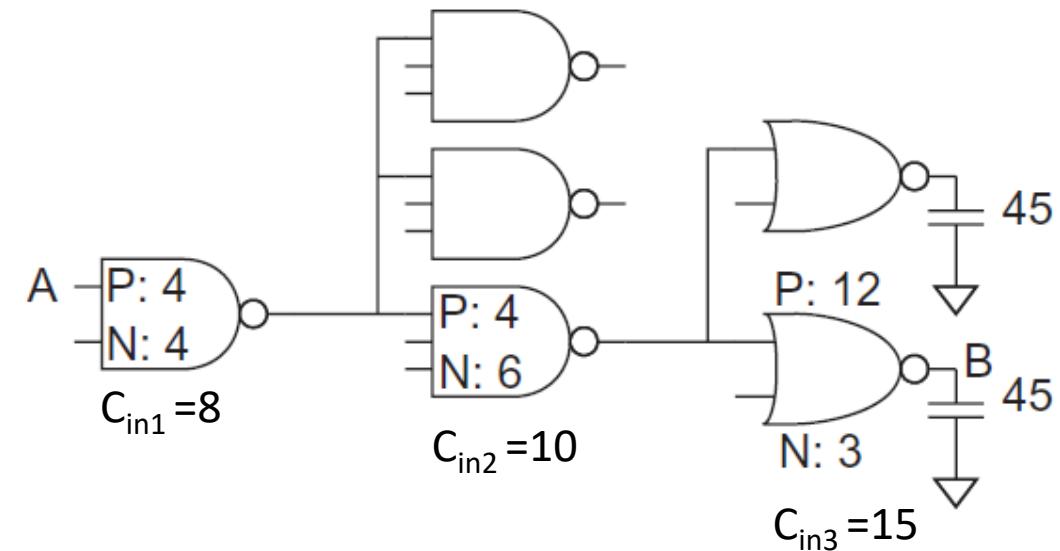


Delay of a Multistage Network: Exercise

- The transistor sizes chosen to give the desired amount of input capacitance while achieving equal rise and fall delays:

P N

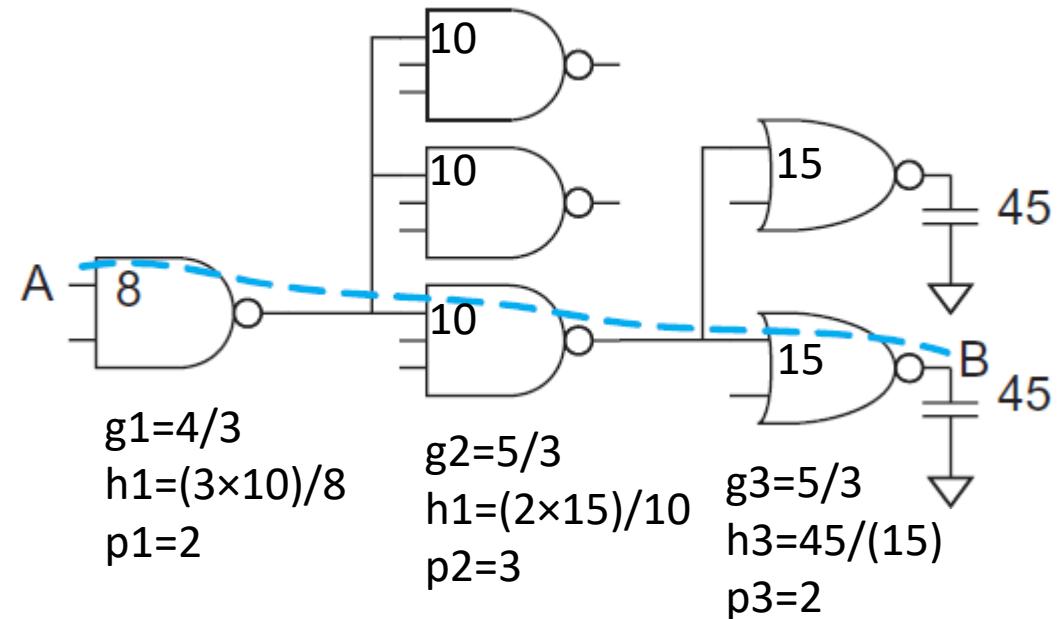
- Basic NAND2: $C_{in} = 2C + 2C$
- Basic NAND3: $C_{in} = 2C + 3C$
- Basic NOR2: $C_{in} = 4C + 1C$



Delay of a Multistage Network: Exercise

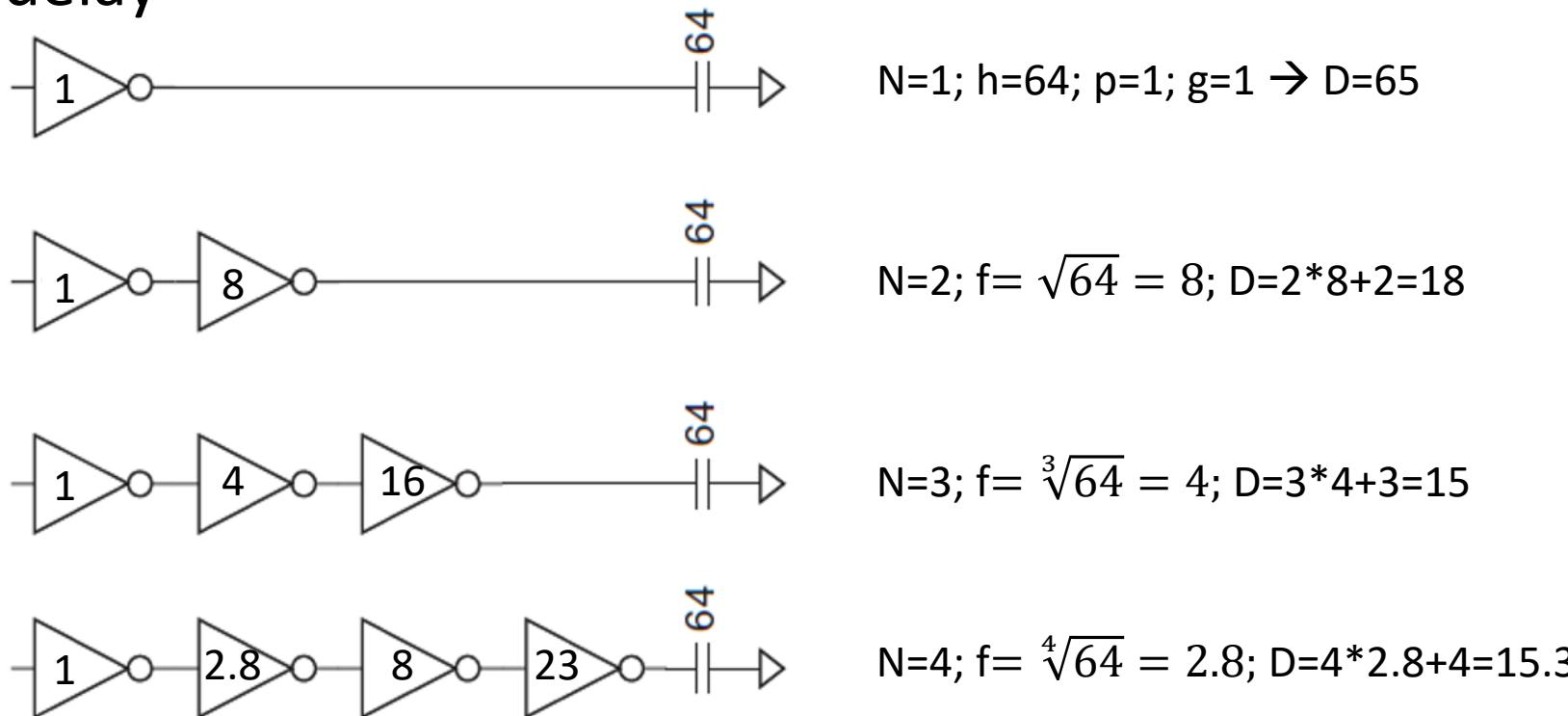
Path delay verification:

- $D = (g_1 \times h_1 + p_1) + (g_2 \times h_2 + p_2) + (g_3 \times h_3 + p_3) = 22 \tau$



Choosing the Best Number of Stages: Exercise

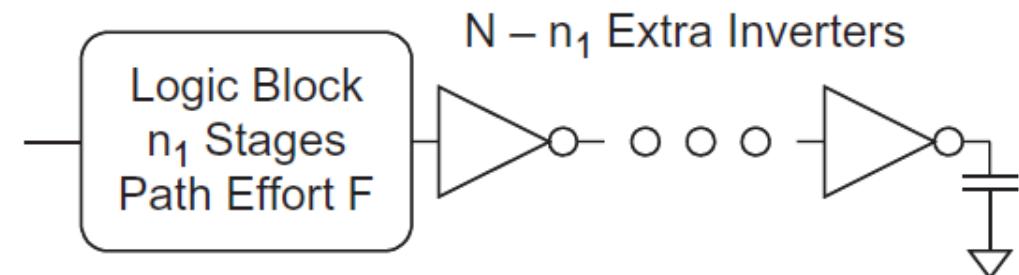
- A signal generated from a unit-sized inverter must drive 64 unit-sized inverters, calculate the optimal number of stages for minimizing the delay



- 3-stage design is the fastest
- For an even number of inversions (same polarity), the two- or four-stage designs are promising. Four-stage design is slightly faster, but the two-stage design requires significantly less area

Choosing the Best Number of Stages

- In general, it is always possible to add inverters to the end of a path without changing its function (save possibly for polarity)
- how many should be added for least delay?
- Logic path has n_1 stages and a path effort of F
- Consider adding $N - n_1$ inverters to the end to bring the path to N stages
- The extra inverters do not change the path logical effort but do add parasitic delay
- Delay of the new path is



$$D = NF^{1/N} + \sum_{i=1}^{n_1} p_i + (N - n_1) p_{\text{inv}}$$

Choosing the Best Number of Stages

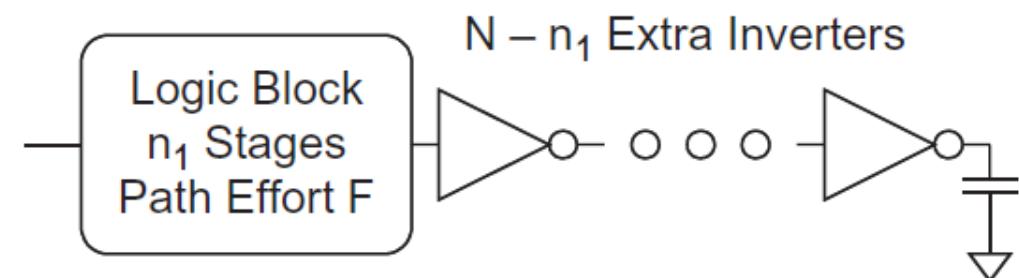
- Delay of the new path is

$$D = NF^{1/N} + \sum_{i=1}^{n_1} p_i + (N - n_1) p_{\text{inv}}$$

$$\hat{N} = \log_{\rho} F$$

- Differentiating with respect to N and setting to 0 to find the best number of stages \hat{N}

$$\begin{aligned} \frac{\partial D}{\partial N} &= -F^{1/N} \ln F^{1/N} + F^{1/N} + p_{\text{inv}} = 0 \\ \Rightarrow p_{\text{inv}} + \rho(1 - \ln \rho) &= 0 \quad \rho = F^{1/\hat{N}} \end{aligned}$$



- Solving numerically, when $p_{\text{inv}} = 1$, $\rho = 3.5$
- A path achieves least delay by using $\hat{N} = \log_{\rho} F$ stages

Summary

The method of Logical Effort is applied with the following steps:

1. Compute the path effort: $F = GBH$
2. Estimate the best number of stages: $\hat{N} = \log_4 F$
3. Sketch a path using: \hat{N} stages
4. Estimate the minimum delay: $D = \hat{N}F^{1/\hat{N}} + P$
5. Determine the best stage effort: $\hat{f} = F^{1/\hat{N}}$
6. Starting at the end, work backward to find sizes: $C_{\text{in}_i} = \frac{C_{\text{out}_i} \times g_i}{\hat{f}}$

TABLE 4.5 Summary of Logical Effort notation

| Term | Stage Expression | Path Expression |
|-------------------|--|--|
| number of stages | 1 | N |
| logical effort | g (see Table 4.2) | $G = \prod g_i$ |
| electrical effort | $b = \frac{C_{\text{out}}}{C_{\text{in}}}$ | $H = \frac{C_{\text{out(path)}}}{C_{\text{in(path)}}}$ |
| branching effort | $b = \frac{C_{\text{onpath}} + C_{\text{offpath}}}{C_{\text{onpath}}}$ | $B = \prod b_i$ |
| effort | $f = gb$ | $F = GBH$ |
| effort delay | f | $D_F = \sum f_i$ |
| parasitic delay | p (see Table 4.3) | $P = \sum p_i$ |
| delay | $d = f + p$ | $D = \sum d_i = D_F + P$ |

Summary

- The propagation delay of the CMOS inverter is determined by the time it takes to charge and discharge the load capacitor CL through the PMOS and NMOS transistors, respectively
- Getting c_l as small as possible is crucial to the realization of high-performance CMOS circuits
- Logic gates are modelled as RC networks
- The Elmore delay model estimates the delay of the network
- The gate delay consists of a parasitic delay (accounting for the gate driving its own internal parasitic capacitance) plus an effort delay (accounting for the gate driving an external load)
- The effort delay depends on the electrical effort (the ratio of load capacitance to input capacitance, also called *fanout*) and the logical effort (which characterizes the current driving capability of the gate relative to an inverter with equal input capacitance)
- The method of logical effort builds on this linear delay model to help us quickly estimate the delay of entire paths based on the effort and parasitic delay of the path

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