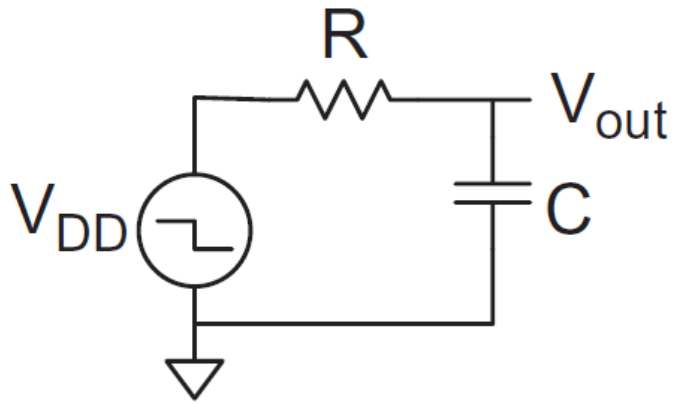
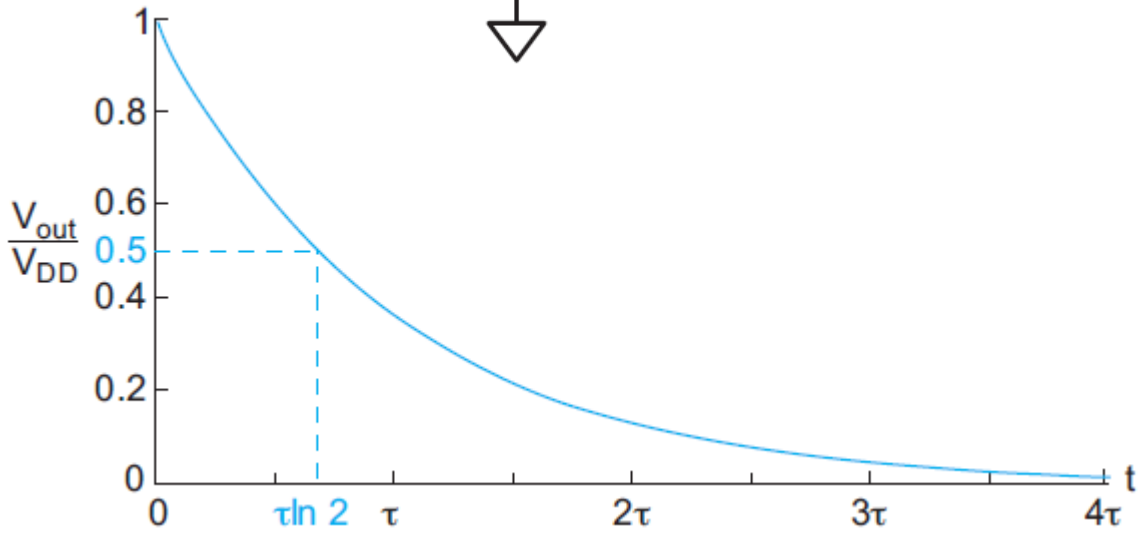
Transient Response for an Inverter

- RC model to estimate the step response of the first-order circuit
- The propagation delay is the time at which *V*out reaches *VDD* /2





$$V_{\text{out}}(t) = V_{DD} e^{-t/\tau}$$

$$\tau = RC$$

$$\boxed{t_{pd} = RC \ln 2}$$

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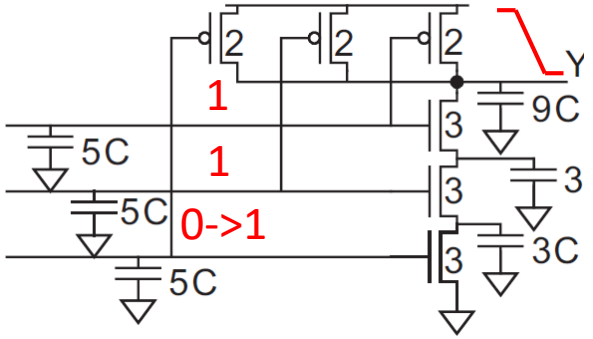
Propagation Delay of Complementary CMOS Gates

NAND3 gate: implementing Elmore Delay Model

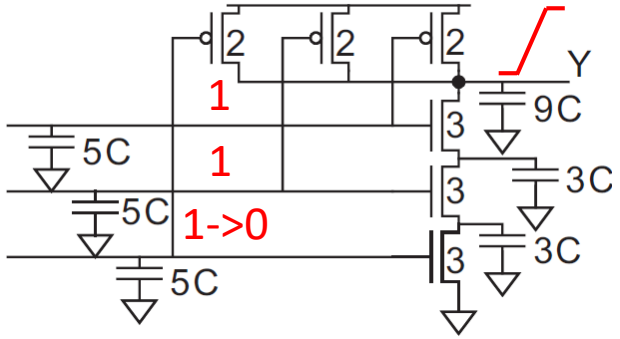
worst case:

Output not loaded

worst case falling

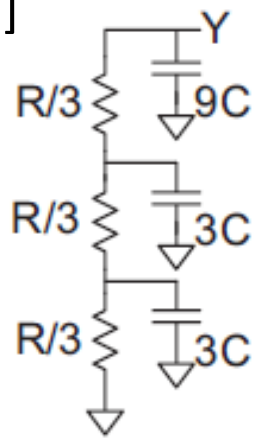


worst case rising

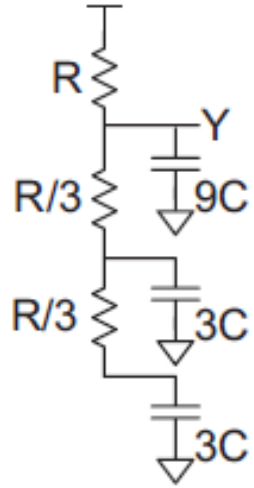


t_{pdf}=ln2[(3C)(R/3)+(3C)(R/3+R/3)+(9C)(R/3+R/3+R/3)]
=ln2(12RC)

t_{pdr}=ln2[(3C)(R)+(3C)(R)+(9C)(R)]
=ln2(15RC)



Falling



Rising

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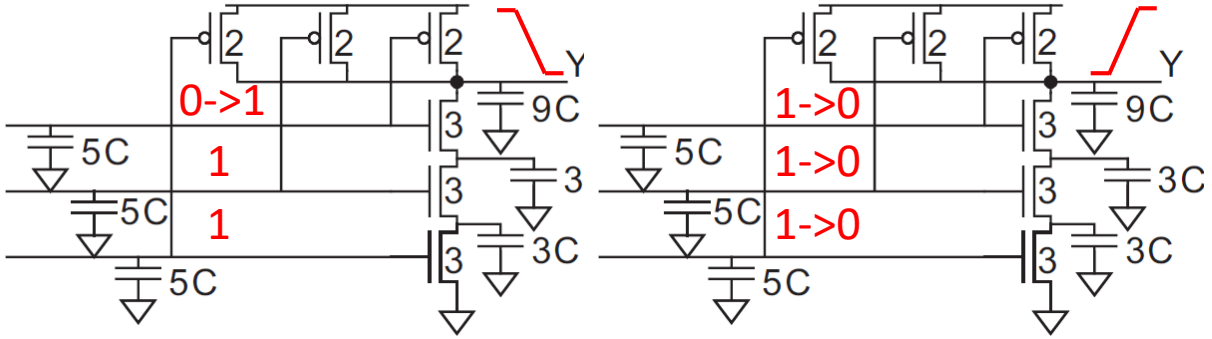
Propagation Delay of Complementary CMOS Gates

NAND3 gate: implementing Elmore Delay Model

best case: contamination delays

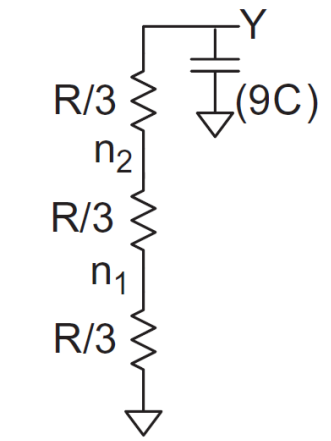
Output not loaded

worst case falling **worst case rising**

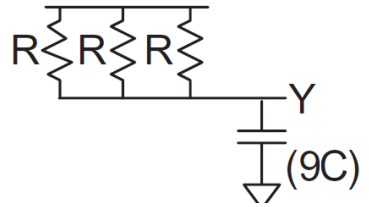


$t_{cdf}=\ln 2[(9C)(R/3+R/3+R/3)]=\ln 2(9RC)$

$t_{cdr}=\ln 2[(9C)(R/3)]=\ln 2(3RC)$



Falling



Rising

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Delay of a Multistage Network Logical Effort Method

- *G : path logical effort* $G = \prod g_i$
- *H : path electrical effort path effort F* $H = \frac{C_{out(path)}}{C_{in(path)}}$

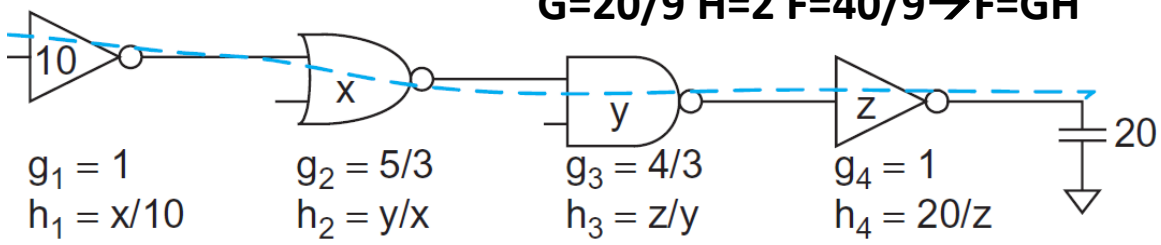
$F = \prod f_i = \prod g_i h_i$

Is *F=GH? NO* in branching paths

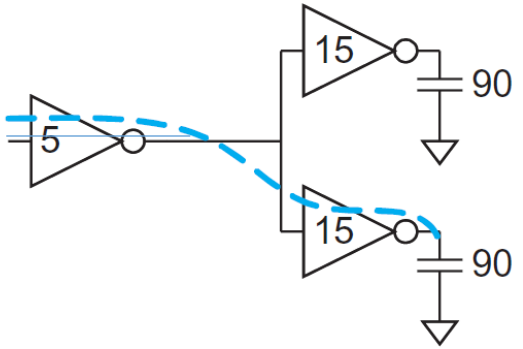
- *b : branching effort* $b = \frac{C_{onpath} + C_{offpath}}{C_{onpath}}$
- B *path branching effort* $B = \prod b_i$

$F = GBH$

G=20/9 H=2 F=40/9→F=GH



Multistage logic network



G=1 H=90/5=18
F = f1f2 = g1h1g2h2=1×6×1×6=36
F≠GH

Network with two-way branch

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Delay of a Multistage Network: Exercise

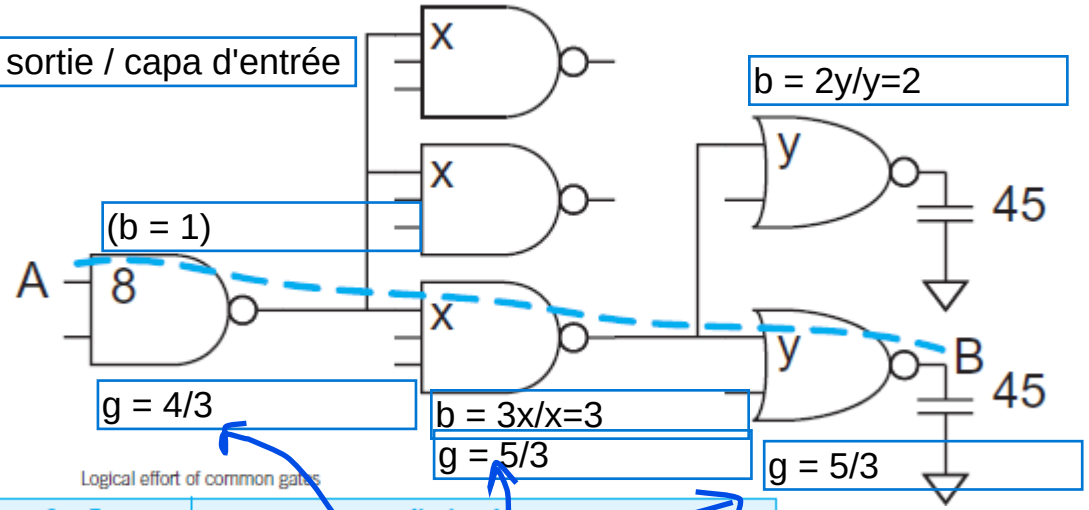
multiplication de tous les g

- *path logical effort* G=(4/3)×(5/3)×(5/3)=100/27
- *path electrical effort H* = 45/8
- *path branching effort B*=3×2=6
- *path effort F=BGH*=125
- *best stage effort* (N=3) $f = \sqrt[3]{125} = 5$
- *path parasitic delay P*=2+3+2=7
- minimum path delay *D*= 3×5+7= 22 in units of τ

Parasitic delay of common gates

Gate Type	Number of Inputs				
	1	2	3	4	*n*
inverter	1				
NAND		2	3	4	*n*
NOR		2	3	4	*n*
tristate, multiplexer	2	4	6	8	2*n*

capa de sortie / capa d'entrée



Logical effort of common gates

Gate Type	Number of Inputs				
	1	2	3	4	*n*
inverter	1				
NAND		4/3	5/3	6/3	(*n* + 2)/3
NOR		5/3	7/3	9/3	(2*n* + 1)/3
tristate, multiplexer	2	2	2	2	2
XOR, XNOR		4, 4	6, 12, 6	8, 16, 16, 8	

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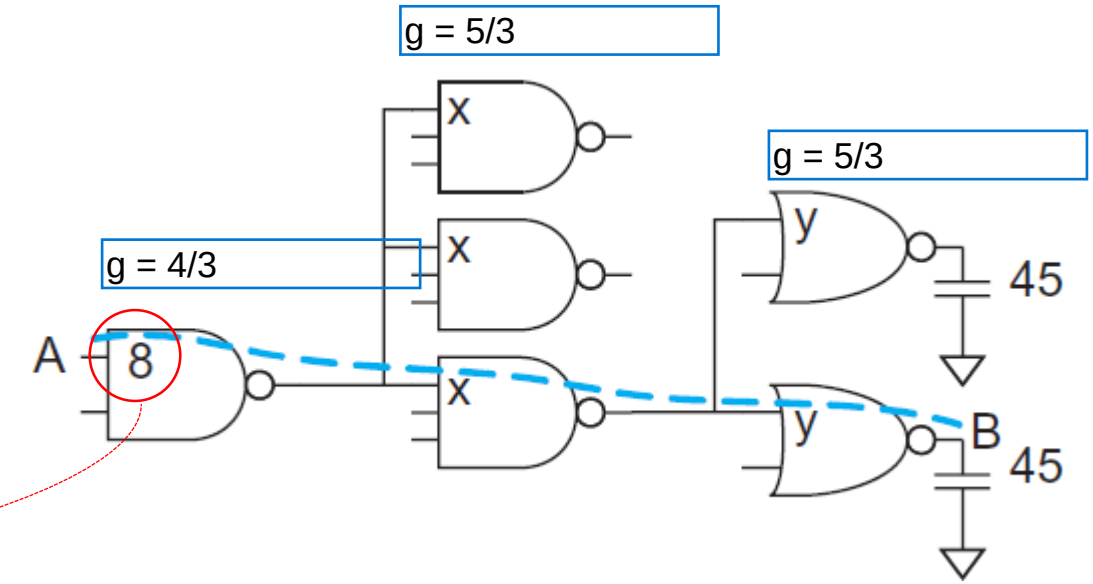
Delay of a Multistage Network: Exercise

- *Using capacitance transformation* formula: $$C_{\text{in}_i} = \frac{C_{\text{out}_i} \times g_i}{\hat{f}}$$
- $y = C_{in3} = 45 \times (5/3)/5 = 15$
- $x = C_{in2} = (15+15) \times (5/3)/5 = 10$
- $8 = (10+10+10) \times (4/3)/5$



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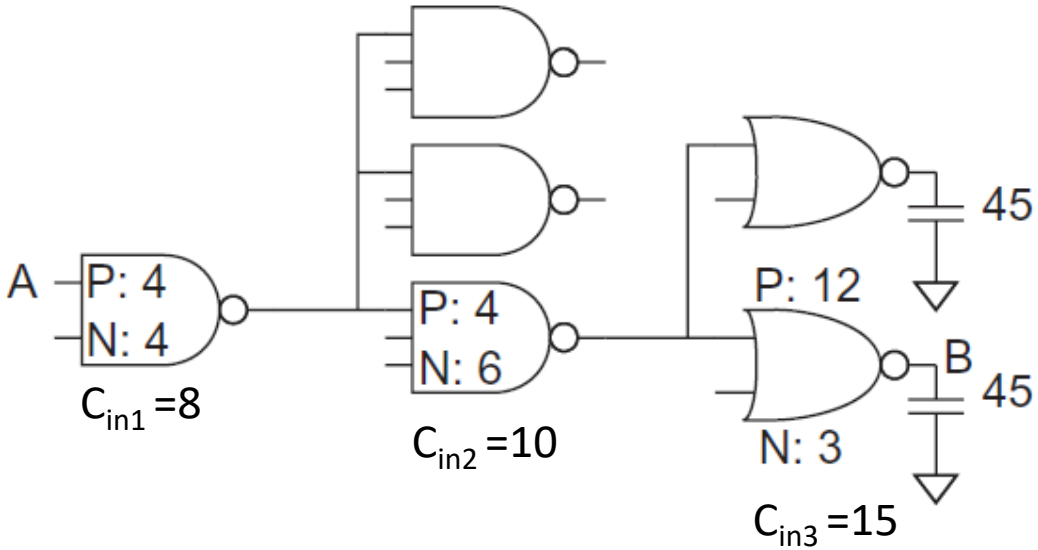
Delay of a Multistage Network: Exercise

- The transistor sizes chosen to give the desired amount of input capacitance while achieving equal rise and fall delays:

  P N

- Basic NAND2: Cin =2C+2C
- Basic NAND3: Cin =2C+3C
- Basic NOR2: Cin =4C+1C



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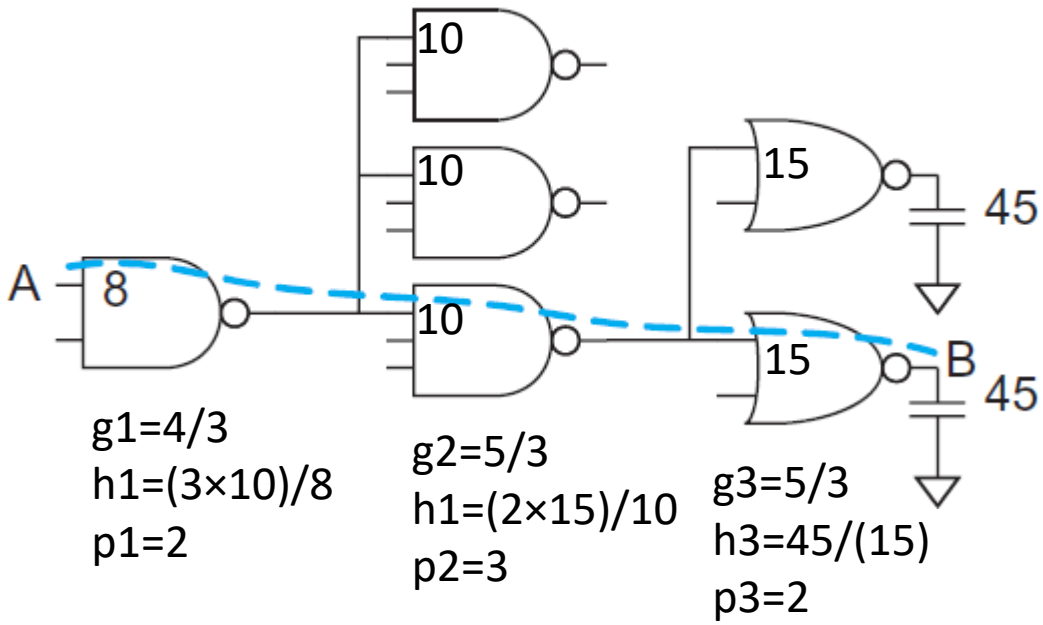
Delay of a Multistage Network: Exercise

Path delay verification:

- D=(g1×h1+p1)+(g2×h2+p2)+(g3×h3+p3)=22 τ



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