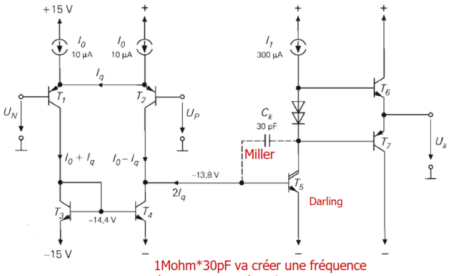
1 ADC / DAC

Petite puissance :
Haute vitesse :
Operational amplifier:



1Mohm*30pF va créer une fréquence decoupure pour le gain

$$U_1 = -2I_qR_1 = -2R_1\frac{U_D}{2r_S} = -\frac{1M\Omega}{2.5k\Omega}U_D = -400\cdot U_D$$

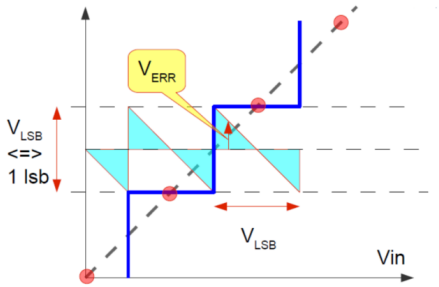
$$U_2 = -S_2U_1R_2 = -5\frac{mA}{V}\cdot 100k\Omega\cdot U_1 = -500\cdot U_1$$

$$A_D = (-400)\cdot(-500) = 2\cdot 10^5$$

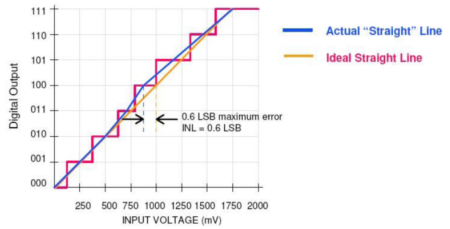
$f_0 = \frac{1}{2\pi R_1 C_k}\cdot\frac{r_{s5}}{R_2}$

ADC

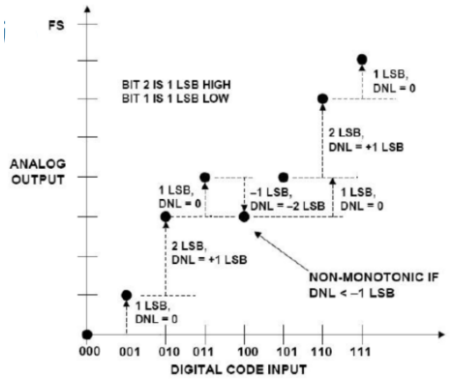
Quantization of the amplitude Resolution N is the number of bits
Resolution step is the analog value of the interval between two codes (1LSB)
$Code = \frac{V_{in}}{V_{FS}}\cdot(2^N-1)$
Quantification de l'erreur:
Power : $E_N = \frac{1}{V_{LSB}}\int_{-q/2}^{q/2} V_{ERR}^2(V_{iN})dV_{IN} = \frac{V_{LSB}^2}{12}$
$U_N = \frac{V_{LSB}}{\sqrt{12}}$



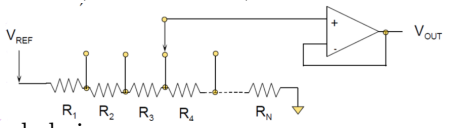
INL (Integral non linearity): différence entre la valeur actuelle et la valeur idéale



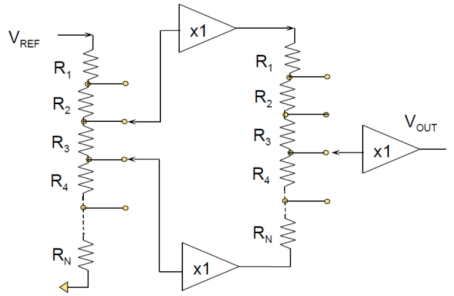
DNL : différence entre entre le step actuel et le step idéal
DNL ¿ -1 : non monotonic
DNL ¿ +1 : missing code



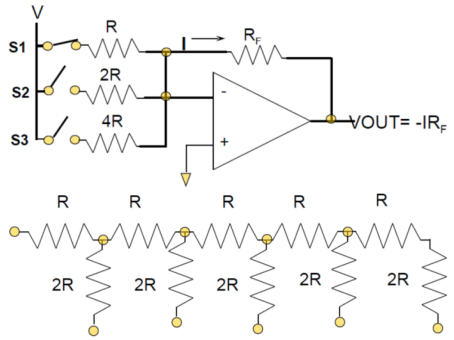
SNR(signal over noise power ratio):
$SNR_{dB} = 10\cdot log(\frac{signal\ power\ P_S}{noise\ power\ P_N})$
$SNR_{dB} = 20\cdot log(\frac{signal\ RMS\ voltage\ U_S}{noise\ RMS\ voltage\ U_N})$
THD (Total Harmonic distorsion): ratio entre deux valeurs RMS
$THD = \sqrt{\frac{\sum U_{h2}^2+U_{h3}^2+\ldots+U_{hn}^2}{U_{Sin}^2}}$
(résultat entre 0 et 1)
SINAD (signal to noise and distorsion):
$SINAD = 10\cdot log\frac{A_{SinFS}^2}{\sum(noise+distortion)power\ to\ fs/2}$ ENOB
(Effective number of bits):
$ENOB = \frac{SINAD_{dB}-1.76}{6.02}$
Structure unary : série of 2^N times 2^0 values
Resistor chain (kelvin divider)



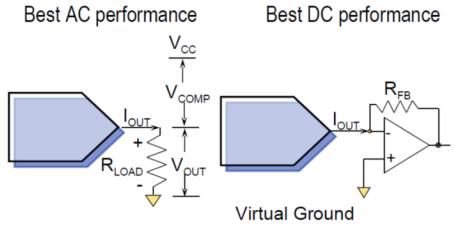
Segmented chains:



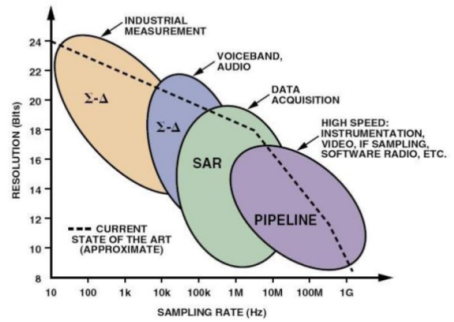
Structure binary : N different values$(2^0, 2^1, 2^2, 2^3 \ldots 2^{N-1})$
Binary-weighted structure



U-I output:



ADC structures :



Flash converter: 2^N resistors and 2^N comparators. Speed between 100M and 1G sps. No S/H neeeded.

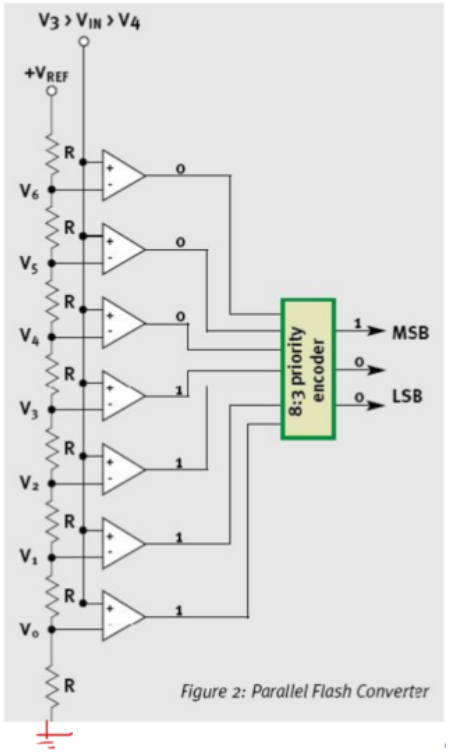
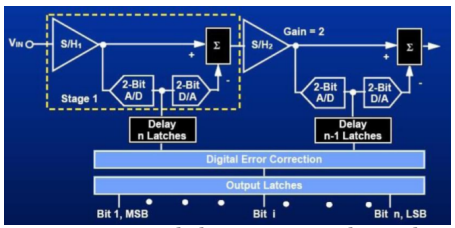
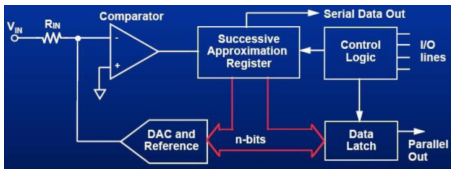


Figure 2: Parallel Flash Converter

Pipeline converter: chaque étage représente un bit. Speed between 1M and 500M sps. S/H needed at each stage.

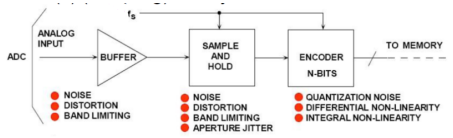


SAR converter: speed between 100k and 10M sps. Need S/H.



Noise sources:

- quantization noise
- noise generated by the converter itself
- application circuit noise (reference & power supply, GND bounce, layout considerations)
- Clock jitter (sampling)



Analog input circuit noise is additive. Voltage reference noise is multiplicative. Quantisation noise is additive. Single ended and common mode:

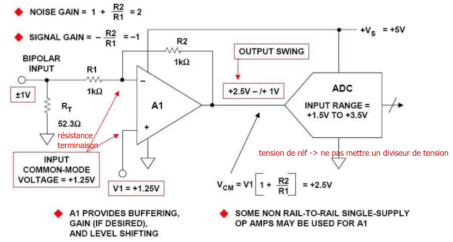
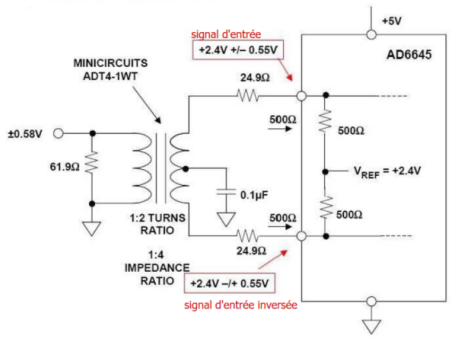


Figure 6.11: Single-Ended Single-Supply DC-Coupled Level Shifter

Single ended to differential (AC) conversion :



Single ended to differential (DC) conversion :

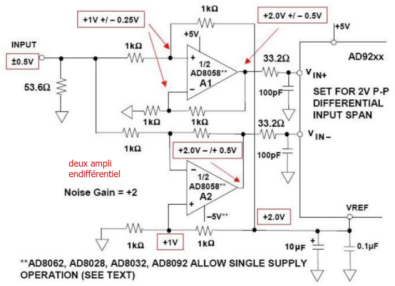


Figure 6.31: Op Amp Single-Ended to Differential DC-Coupled Driver with Level Shifting

1.1 Discrétisation

Valeur du signal continu pris à des temps précis (sample) Après l'échantillonnage, la valeur est quantifiée sur une valeur de 2^n

1.1.1 Idéal

$$x_s(t) = \sum_{k=-\infty}^{+\infty} x(kT_s)\cdot\delta(t-kT_s) = x(t)\cdot\sum_{k=-\infty}^{+\infty}\delta(t-kT_s) \quad (1)$$

1.1.2 Critère de Nyquist

$f_s > 2(f_a - f_b)$ avec f_a limite haute de la BW du signal et f_b limite basse de la BW

1.2 Aliasing

L'échantillonnage d'un signal provoque une répétition du spectre du signal autour de f_s et de multiples de f_s.

1.3 Signal Noise Ratio

- Bruit de quantification RMS $N_{RMS} = \frac{V_{LSB}}{\sqrt{12}}$
- Tension sinus FullScale $S_{RMS}\frac{V_{LSB}}{\sqrt{2}}\cdot\frac{2^N}{2}$
- $SNR = 20log(\frac{S_{RMS}}{N_{RMS}}) = 20log(\sqrt{\frac{12}{8}}) + 20log(2^N)$
- En dB $SNR = 6.02N + 1.76$

1.4 Process gain

C'est lorsque l'on utilise pas toute la bande de 0 à $f_s/2$ le gain pour un sinus FullScale est le suivant.

$$SNR = 6.02N + 1.76 + 10log(\frac{f_s}{2 \cdot BW}) \qquad (2)$$

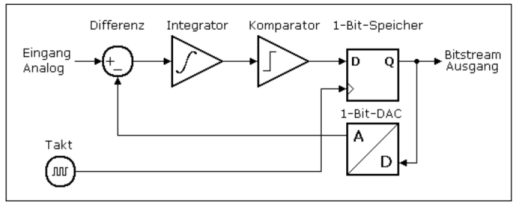
1.5 Sur-échantillonnage

$$SNR = 6.02N + 1.76 + 10log(OSR) \qquad (3)$$

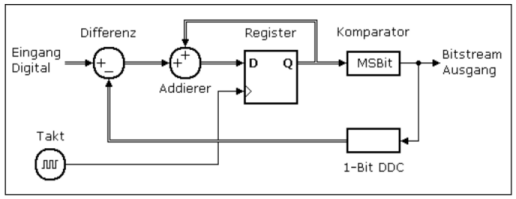
Meilleur de 3dB à chaque fois que la f_s double.

1.6 Conversion Sigma-Delta

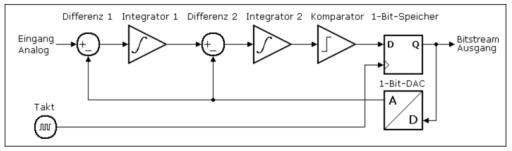
Modulateur de premier ordre



Analogique



Digital



Modulateur du deuxième ordre

1.6.1 Sur-échantillonnage pour SD