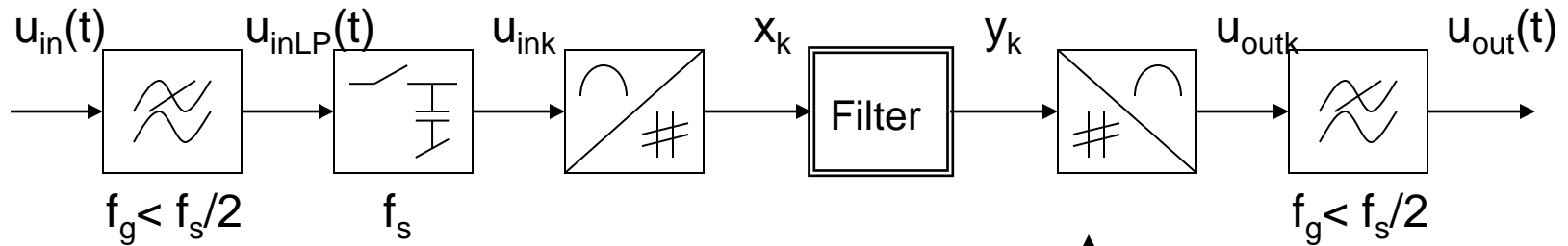


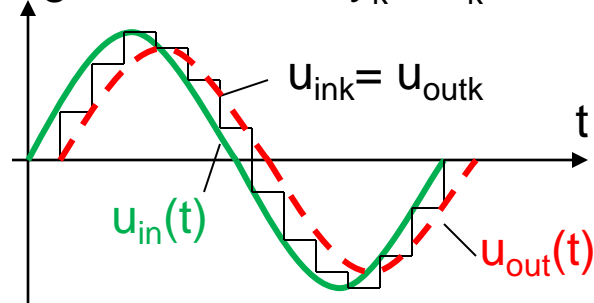
# Contents

- Discretization in time: sampling
  - Delta-sigma conversion
  - Switched capacitor circuits
  - Higher order, multi-level and cascaded modulators
- 
- Exercises
  - References

# Signal processing chain

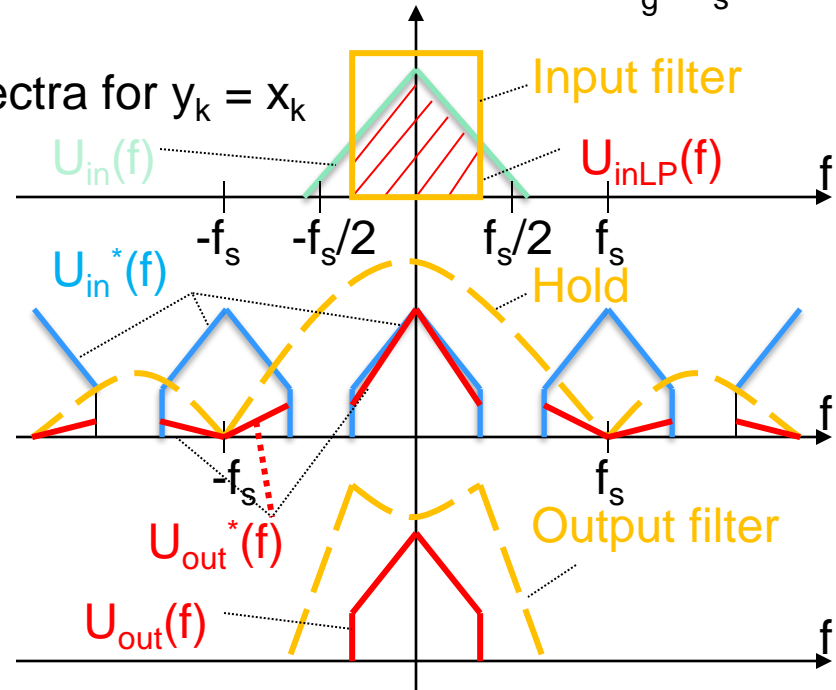


Signal forms for  $y_k = x_k$



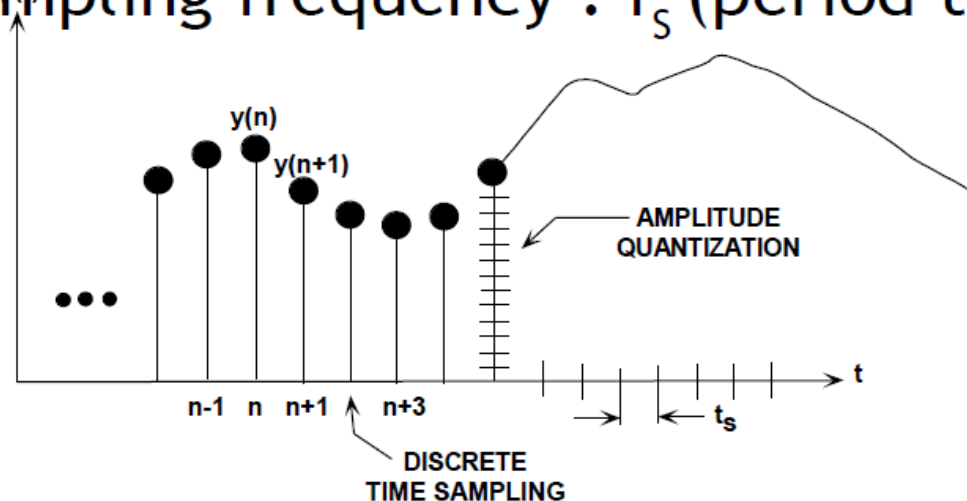
$$U_{out}^*(jf) = \frac{\sin \frac{\pi f}{f_s}}{\frac{\pi f}{f_s}} \frac{1}{f_s} \sum_{k=0}^{\infty} u_{in}(kT_s) e^{-2\pi jkf/f_s}$$

Spectra for  $y_k = x_k$



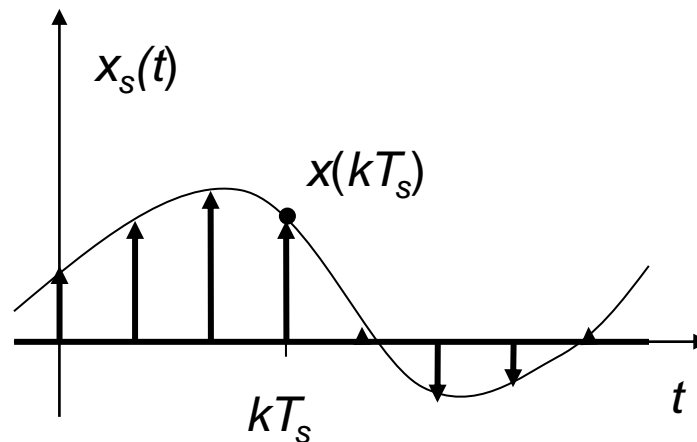
# Discretization (quantization) of time

- ⌘ The value of the signal taken at a particular moment : a sample
  - After sampling, the signal is reduce to a suite of amplitude quantified numbers taken at regular time frequency
    - Unregular sampling period not used, only a sampling clock.
- ⌘ Def.: Sampling frequency :  $f_s$  (period  $t_s$ )



# Ideal regularly sampled signal

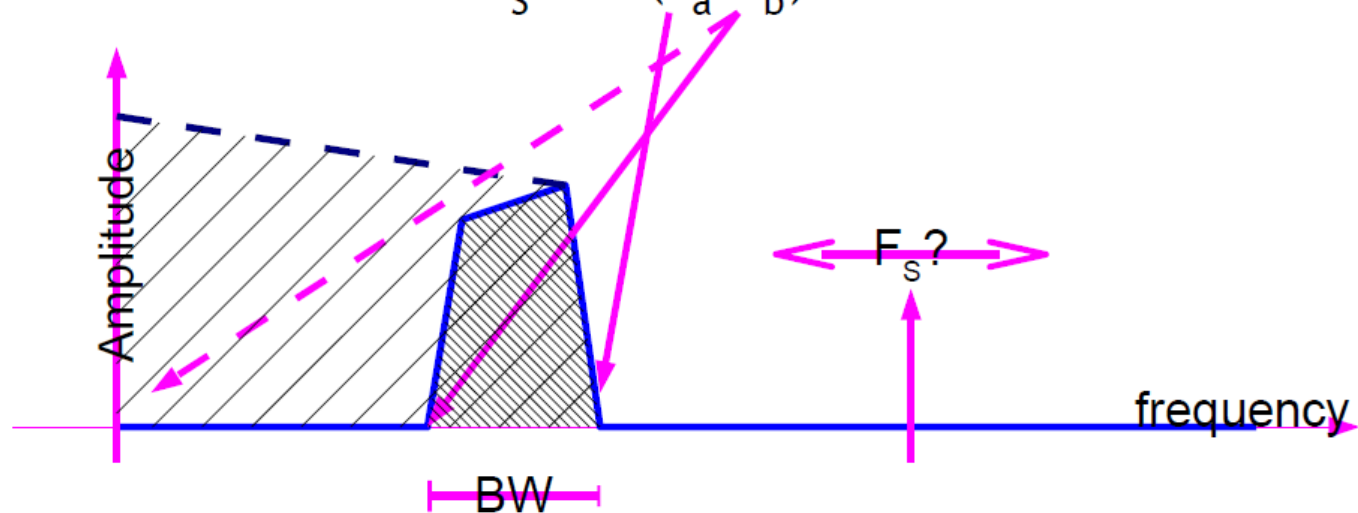
- ⌘ Sampling a signal in the time domain corresponds to a multiplication by a Dirac Sequence (mathematical notation)



$$x_s(t) = \sum_{k=-\infty}^{+\infty} x(kT_s) \cdot \delta(t - kT_s) = x(t) \cdot \sum_{k=-\infty}^{+\infty} \delta(t - kT_s)$$

# Nyquist criterion

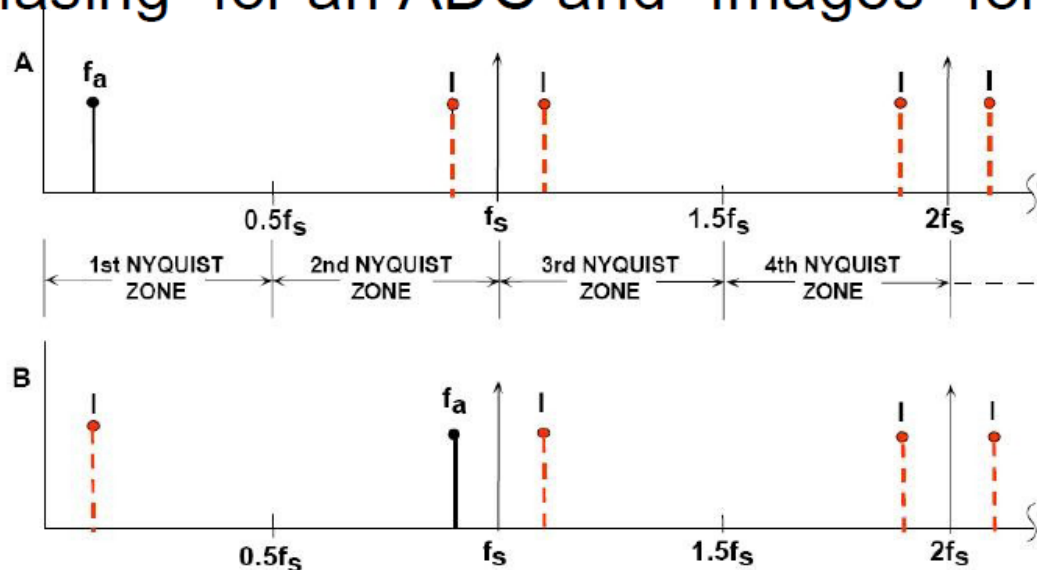
- ⌘ Sampling frequency at least twice the *Signal BANDWIDTH* :  $f_s > 2(f_a - f_b)$



- ⌘ A converter used with a  $f_s =$  or just  $\geq 2f_a$  is assumed to make a « Nyquist conversion »

# Aliasing

- ⌘ Sampling a signal causes a repetition of the signal spectrum around  $f_s$  and multiples of  $f_s$
- Repetition in Frequency Domain are called “Aliasing” for an ADC and “Images” for a DAC



Analog Signal  $f_a$  Sampled @  $f_s$  Using Ideal Sampler  
Has Images (Aliases) at  $|\pm Kf_s \pm f_a|$ ,  $K = 1, 2, 3, \dots$

# Signal to noise ratio

⌘ Quant. Noise RMS is assumed =  $V_{\text{LSB}}/\sqrt{12}$

⌘ RMS of SinFS =  $1/\sqrt{2} \cdot V_{\text{LSB}} \cdot 2^N/2$

$$\text{SNR} = 20 \log \left( \frac{S_{\text{RMS}}}{N_{\text{RMS}}} \right) = 20 \log \sqrt{\frac{12}{8}} + 20 \log 2^N$$

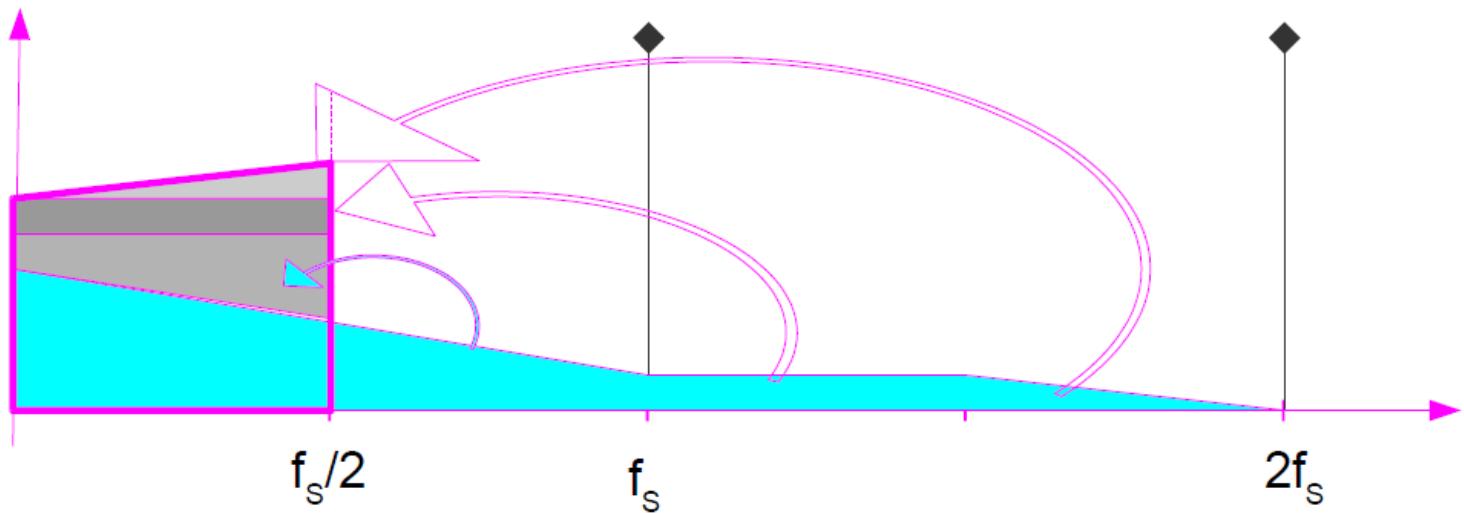
$$\text{SNR} = N \cdot 6.02 \text{ dB} + 1.76 \text{ dB}$$

[fig 2.39]

⌘ All quantiz Noise is folded in Nyquist zone 1 (by aliasing !)

# Wide band aliasing

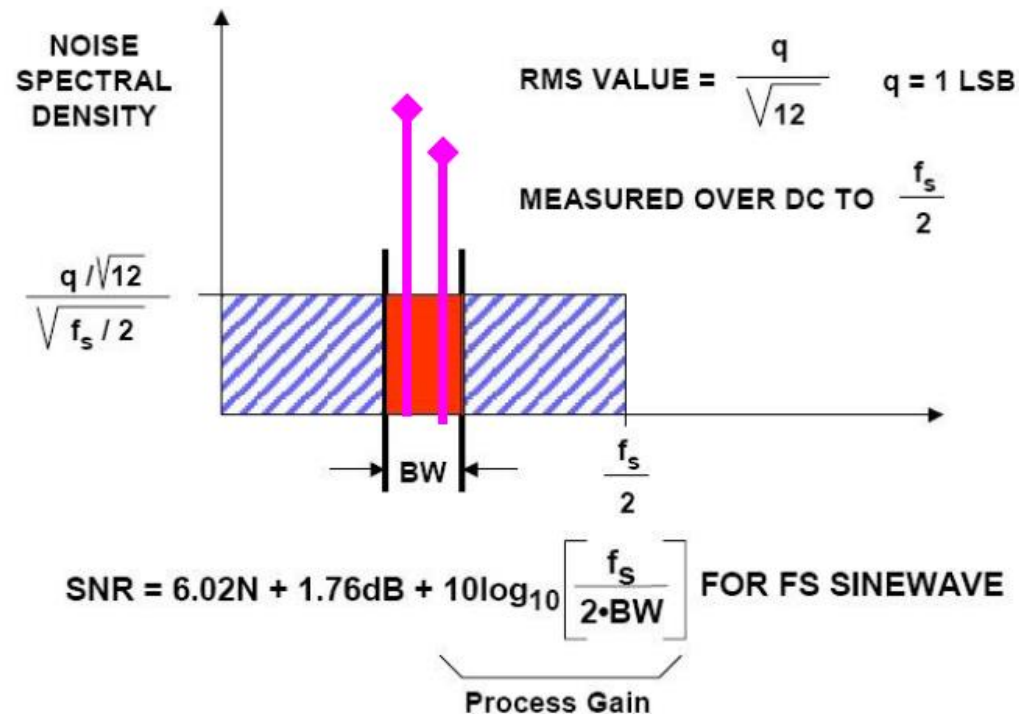
- ⌘ Wide band *noise or signal* will be folded in the « base band » (Nyquist zone 1 :  $[0 \dots f_s/2]$ )





# Process gain

- ⌘ Process gain is the benefit when the signal don't use all the base band  $[0 \dots f_s/2]$



*Quantization Noise Spectrum*

# Oversampling

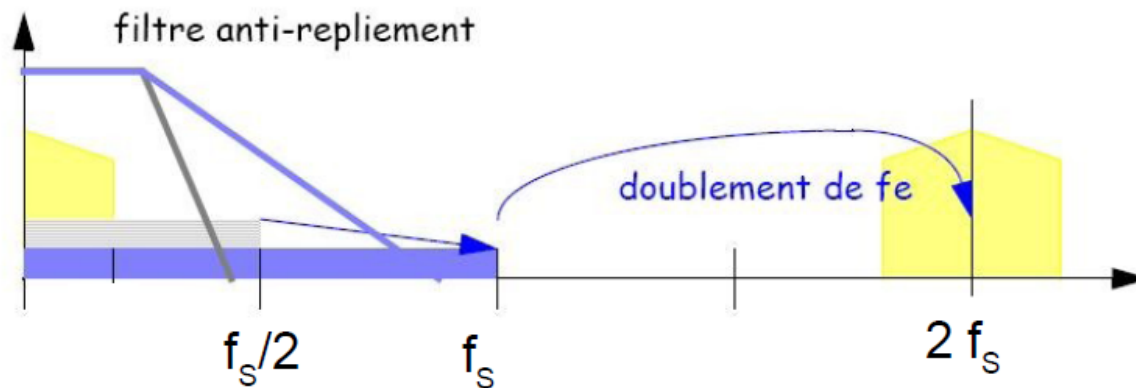
Oversampling is a convenient way to reduce noise - if BW of the signal effectively filtered! -

- Oversampling ratio **OSR** : M time the Nyquist sample frequency ( $f_s/2$ )

- The SNR of a oversampled system looks like:

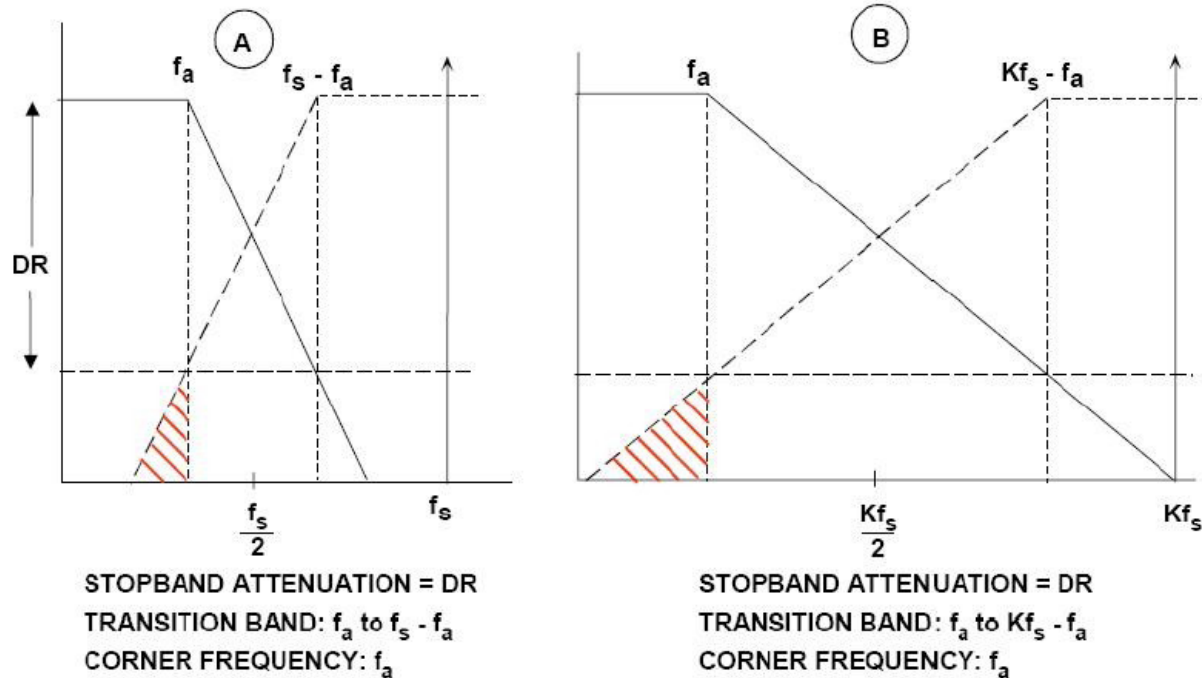
$$\text{SNR} = 1.76 + 6N + 10 \cdot \log(\text{OSR})$$

- SNR better of +3dB each time  $f_s$  double !



# Oversampling

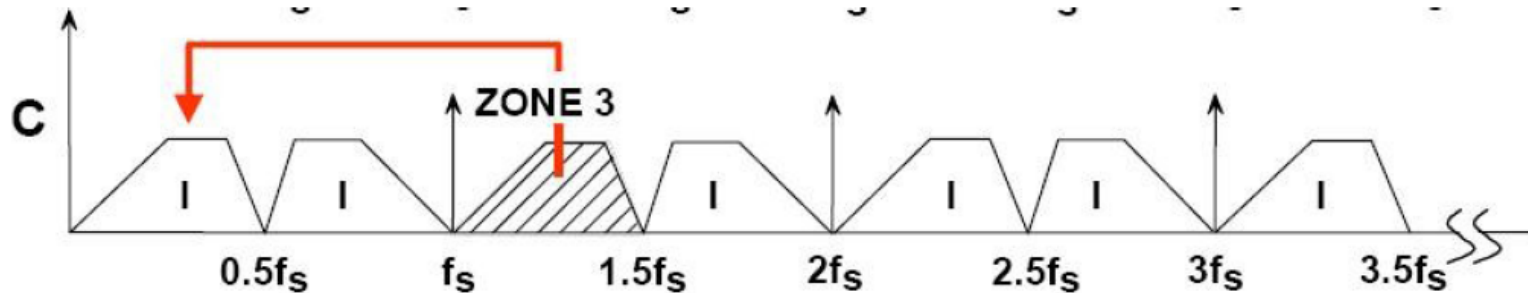
- ⌘ Oversampling is a convenient way to reduce complexity of the antialiasing filter



*Oversampling Relaxes Requirements  
on Baseband Antialiasing Filter*

# Undersampling

⌘ Possible when signal is BW-limited ( $\Rightarrow f_s$  can be smaller than  $f_b$ )



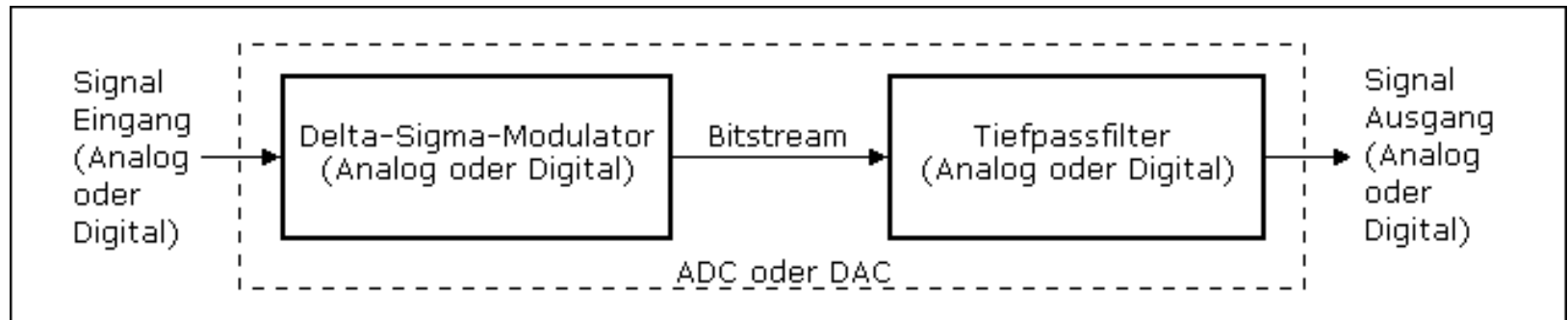
*Undersampling and Frequency Translation Between Nyquist Zones*

- Usual in communication systems (modulated signals) : undersampling process is *analog to demodulation* !
- But all ADC are not suited for undersampling : Caution analog BW, dynamic performances, etc.

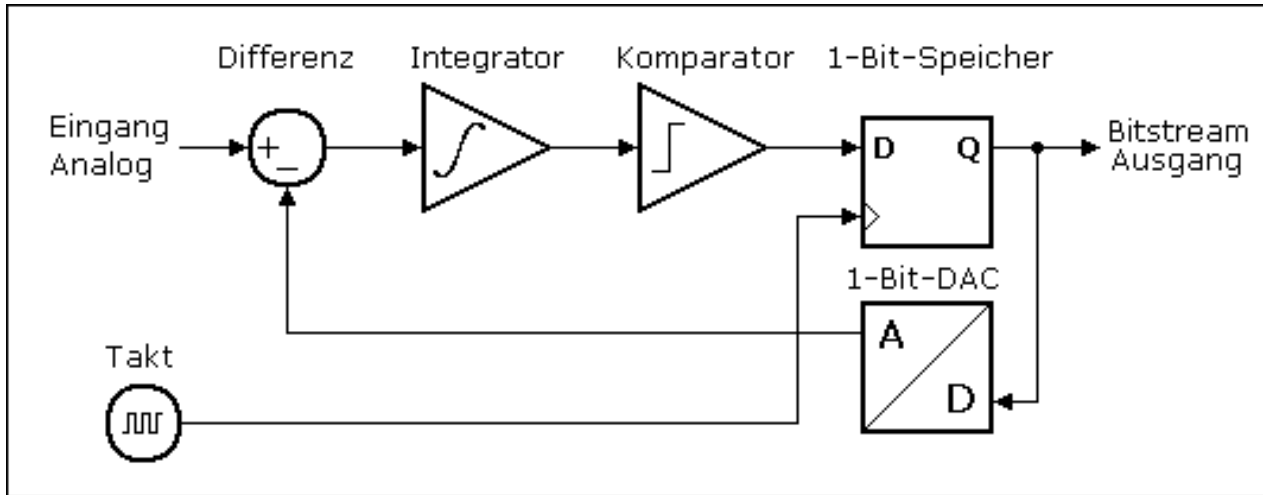
# Effect of clock jitter on conversion noise

We have a 20bit audio SAR ADC with a sampling clock rate of  $f_s = 48\text{ksps}$ . How much rms jitter of the ADC clock signal (suppose  $f_{\text{CLK}} = 24 \cdot f_s$ ) can be admitted, so that the conversion error remains below one LSB for sinusoidal full scale input ( $\pm 1\text{V}$ ) signals of frequency  $f = 4\text{kHz}$ ?

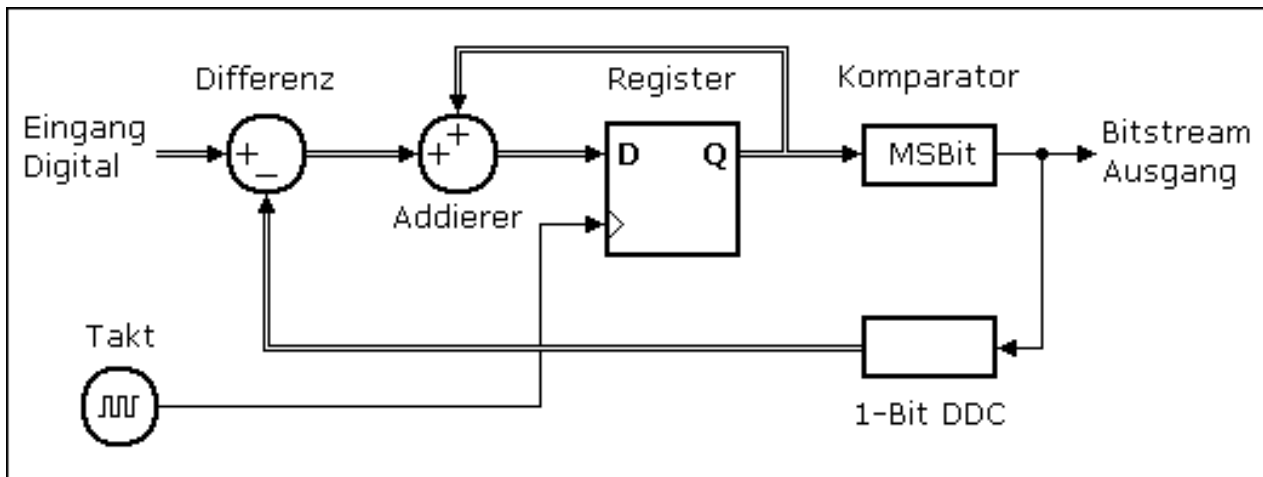
# $\Delta$ - $\Sigma$ -Conversion



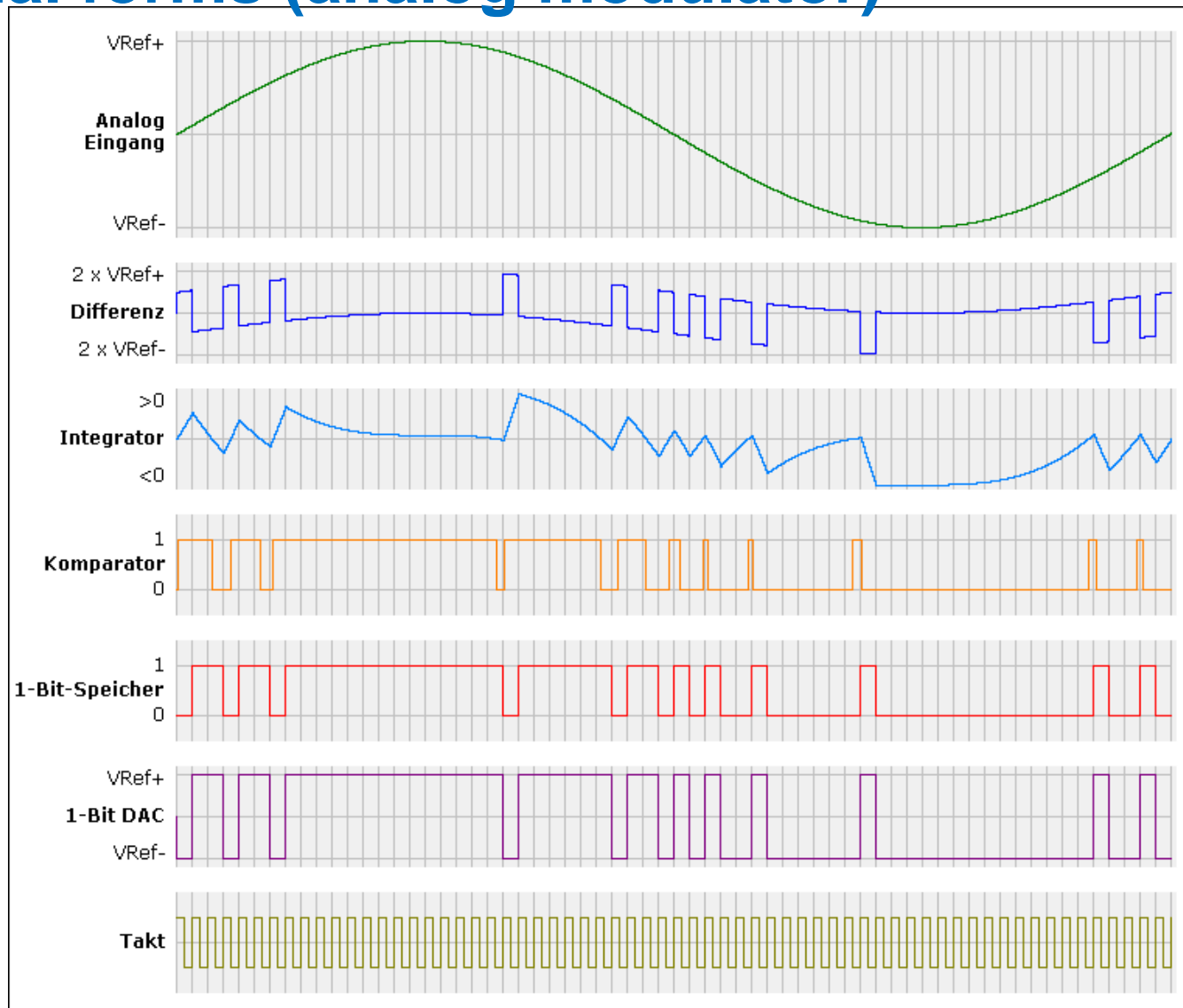
# Analog first order modulator



# Digital first order modulator



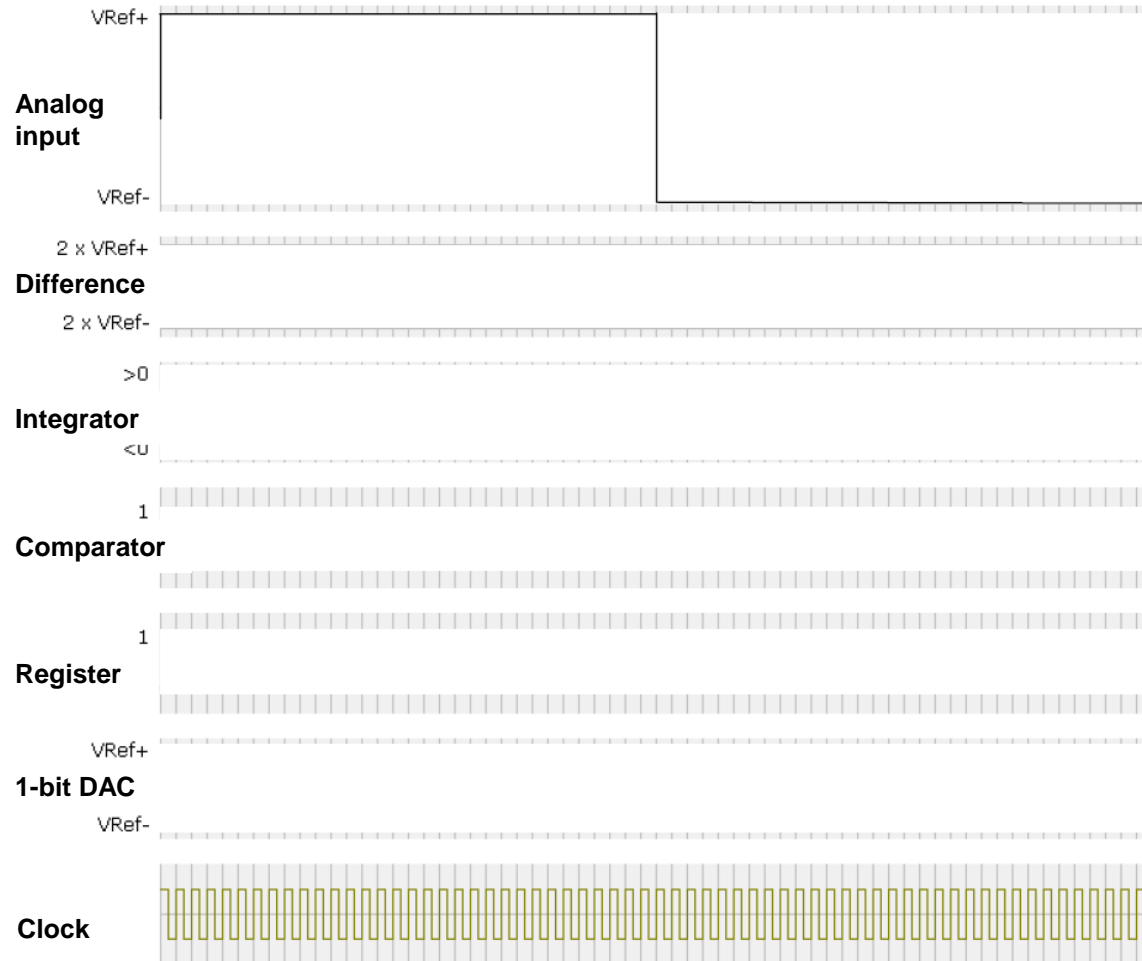
# Signal forms (analog modulator)





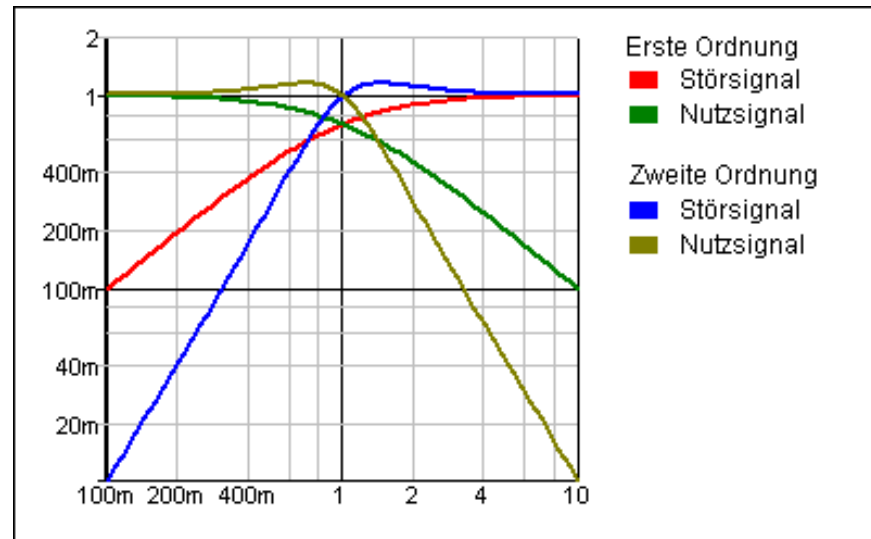
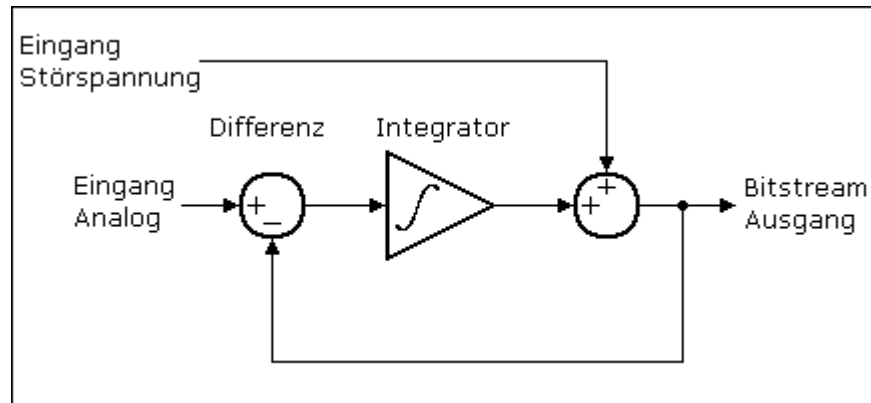
# Signal forms

Trace the forms of signals in an analog first order modulator for a rectangular input signal:

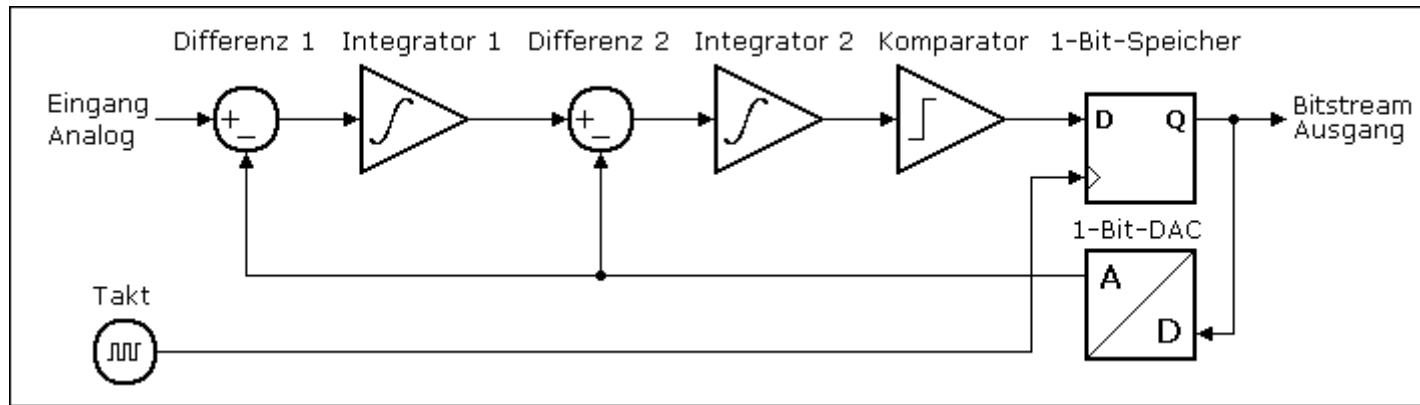


Retrace the bitstream after decimation by 8.

# Dynamic behavior of the modulator

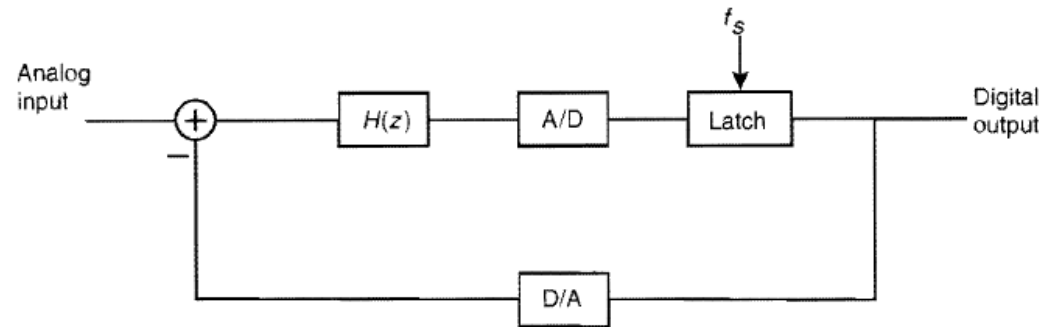


# Second order modulator transfer functions

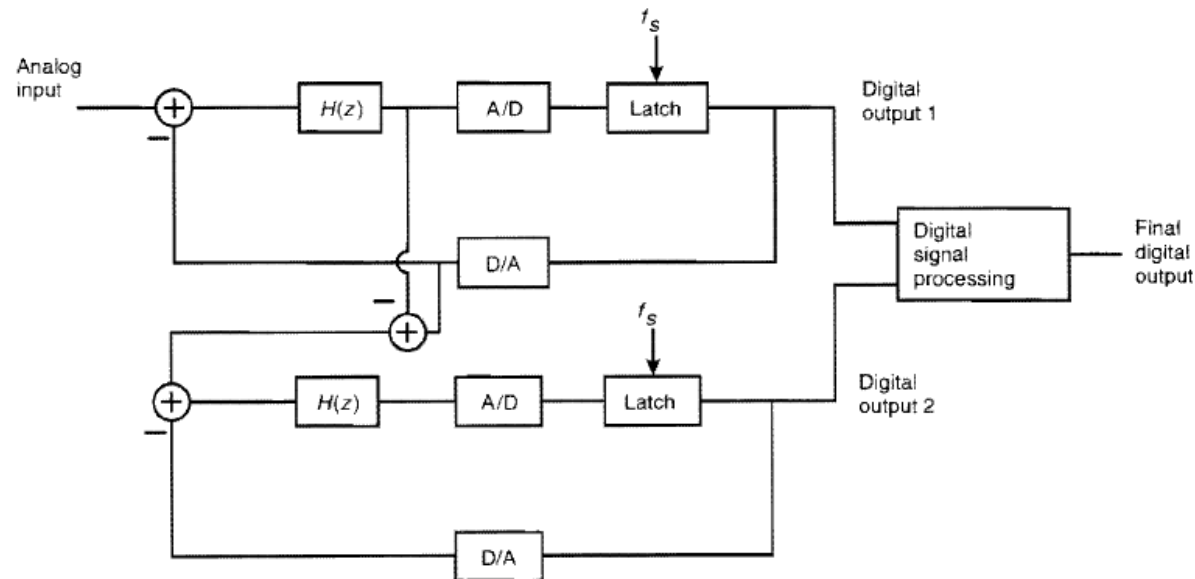


- Determine the equivalent continuous transfer functions of a second order delta-sigma modulator, for the signal and for the noise.
- Represent the corresponding amplitude responses in a Bode diagram.

# Cascade of two first order demodulators

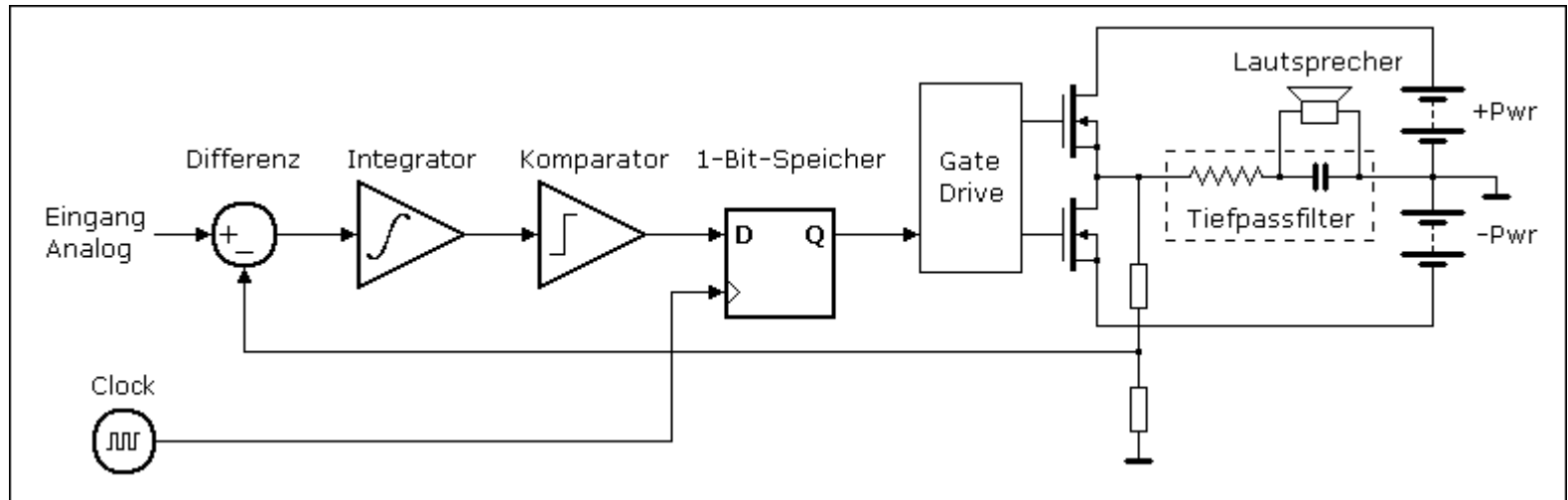


Block diagram of single-loop modulator.



Block diagram of cascaded modulator.

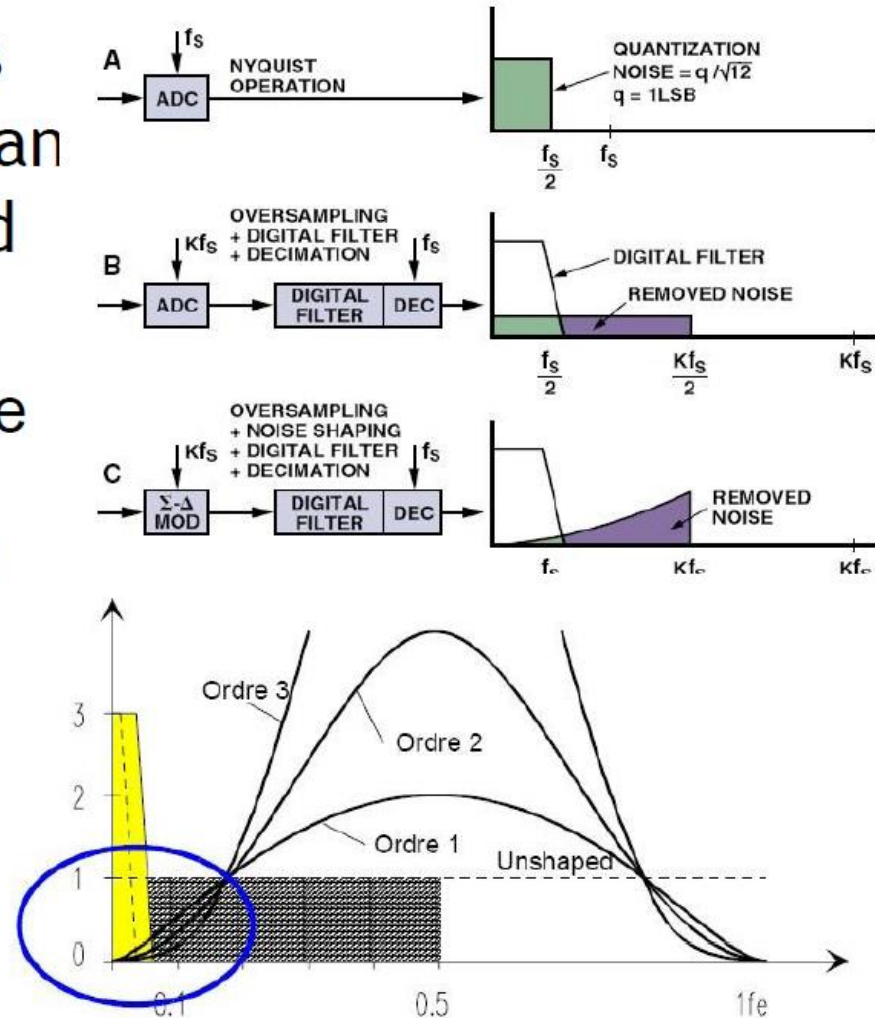
# Power amplifier with digital output stage



# Oversampling and delta-sigma modulation

⌘ Why S-D converters are much better than simple oversampled systems?

- SD modulation use Oversampling (OSR : 32..512...) and add a noiseshaping:

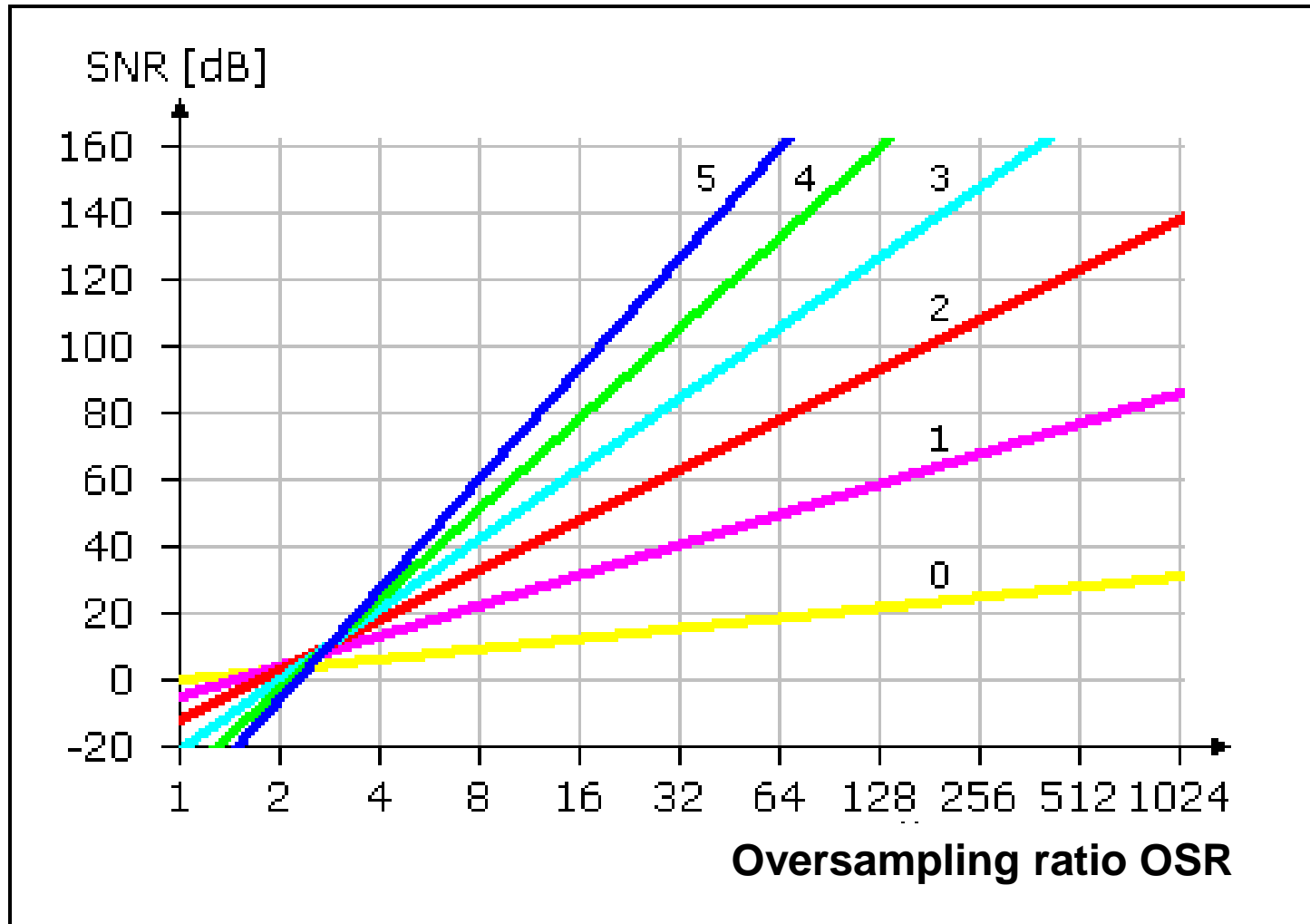


# Influence of the order of delta-sigma modulation

⌘ SNR in Function of the order L & OSR :

Order of modulator	1	2	3	L
Transfer N(z)/E(z)	$1 - z^{-1}$	$(1 - z^{-1})^2$	$(1 - z^{-1})^3$	$(1 - z^{-1})^L$
Base band noise $n_0$ ( $\Delta$ = quantisation step)	$\frac{\Delta\pi}{6} \sqrt{\left(\frac{1}{\text{OSR}}\right)^3}$	$\frac{\Delta\pi^2}{\sqrt{60}} \sqrt{\left(\frac{1}{\text{OSR}}\right)^5}$	$\frac{\Delta\pi^3}{\sqrt{84}} \sqrt{\left(\frac{1}{\text{OSR}}\right)^7}$	$\frac{\Delta\pi^L}{\sqrt{12(2L+1)}} \sqrt{\left(\frac{1}{\text{OSR}}\right)^{2L+1}}$
S/N	$\frac{9}{(2\pi)^2 \left(\frac{1}{\text{OSR}}\right)^3}$	$\frac{15}{(2\pi)^4 \left(\frac{1}{\text{OSR}}\right)^5}$	$\frac{21}{(2\pi)^6 \left(\frac{1}{\text{OSR}}\right)^7}$	$\frac{3(2L+1)}{(2\pi)^{2L} \left(\frac{1}{\text{OSR}}\right)^{2L+1}}$

# Signal to noise ratio versus oversampling ratio



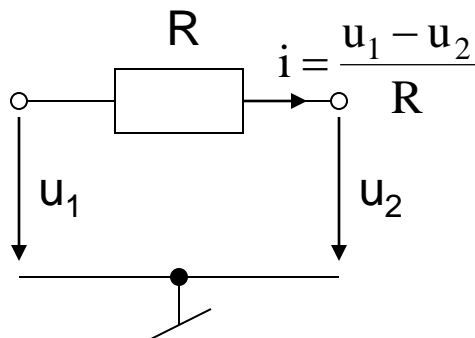


# Signal to noise and oversampling ratios

- What is the maximum signal-to-noise ratio of a 16bit ADC? Suppose a sinusoidal input signal, and that the quantisation noise dominates all other noises. The noise is considered as white noise.
- Which resolution, expressed as number of bits (ENOB), can have an ADC with a second order delta-sigma modulator, operating at an oversampling ratio of 128?
- Consider a delta-sigma ADC with ENOB = 16bits and an input signal bandwidth of 1kHz. The oversampling ratio is 128. Which order is required for an analog anti-aliasing filter?

# From the resistor to the switched capacitor

In integrated circuits, replacement of area consuming resistors with switched capacitors.



Definition of commutation intervals:

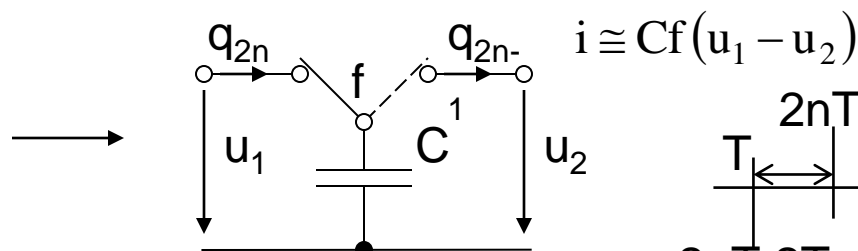
Charge transport

in the even interval:

in the odd interval:

if  $u_1$  and  $u_2$  are constant,

Average of current



even:  $2nT - T \leq t \leq 2nT$

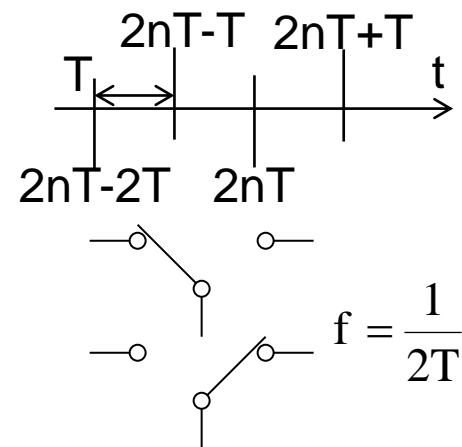
odd:  $2nT - 2T \leq t \leq 2nT - T$

$$q_{2n} = Cu_1(2nT) - Cu_2(2nT - T)$$

$$q_{2n-1} = Cu_1(2nT - 2T) - Cu_2(2nT - T)$$

$$q_{2n} = q_{2n-1} = q = C(u_1 - u_2)$$

$$I = \frac{q}{2T} = \frac{C}{2T}(u_1 - u_2) = Cf(u_1 - u_2)$$

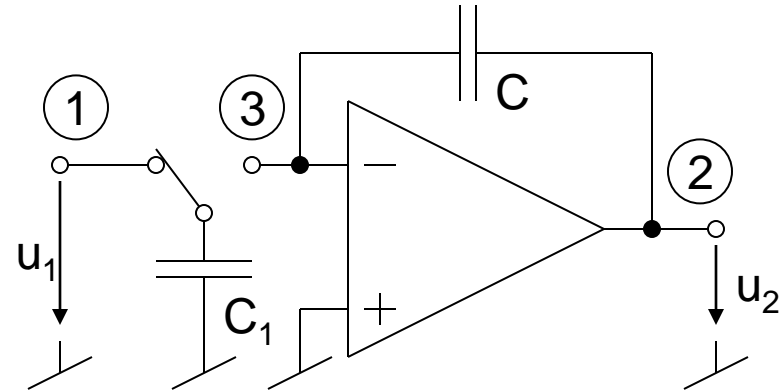


# Integrator with switched capacitor

Analysis method:

1) Number nodes (here 1, 2, 3)

2) Establish charge equilibria of inner nodes (here only 3)



- even circuit:

$$C(u_2(2nT) - u_3(2nT)) = C(u_2(2nT - T) - u_3(2nT - T))$$

$$u_3 \equiv 0 \Rightarrow u_2(2nT) = u_2(2nT - T)$$

- odd circuit:

$$\begin{aligned} C(u_2(2nT - T) - u_3(2nT - T)) + C_1(0 - u_3(2nT - T)) = \\ = C(u_2(2nT - 2T) - u_3(2nT - 2T)) + C_1(0 - u_1(2nT - 2T)) \end{aligned}$$

$$u_3 \equiv 0 \Rightarrow Cu_2(2nT - T) = Cu_2(2nT - 2T) - C_1u_1(2nT - 2T)$$

3) Put in relation the start of an odd with the end of an even interval

$$Cu_2(2nT) = Cu_2(2nT - 2T) - C_1u_1(2nT - 2T)$$

4) z-transform

$$CU_2(z) = CU_2(z)z^{-1} - C_1U_1(z)z^{-1} \Rightarrow \frac{U_2(z)}{U_1(z)} = -\frac{C_1}{C} \frac{1}{z-1}$$

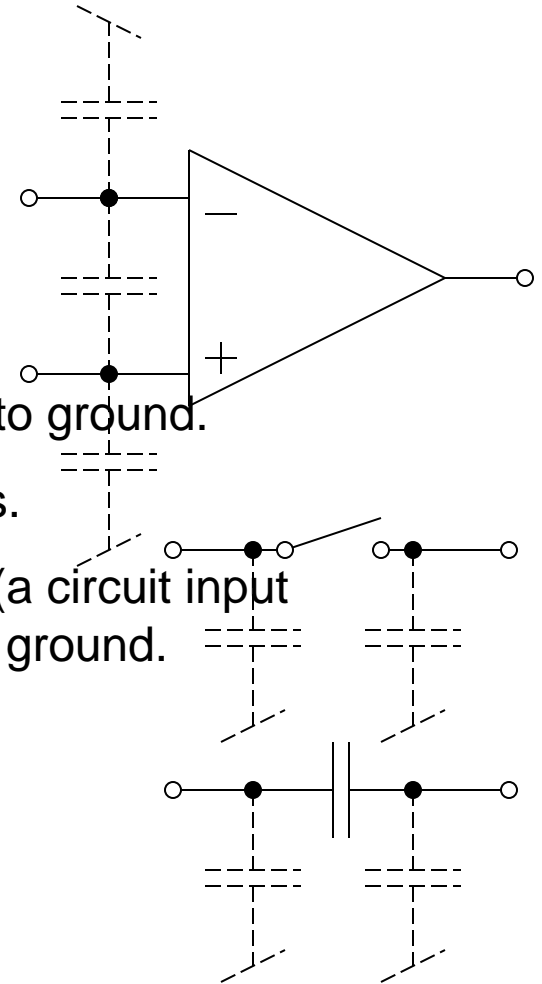
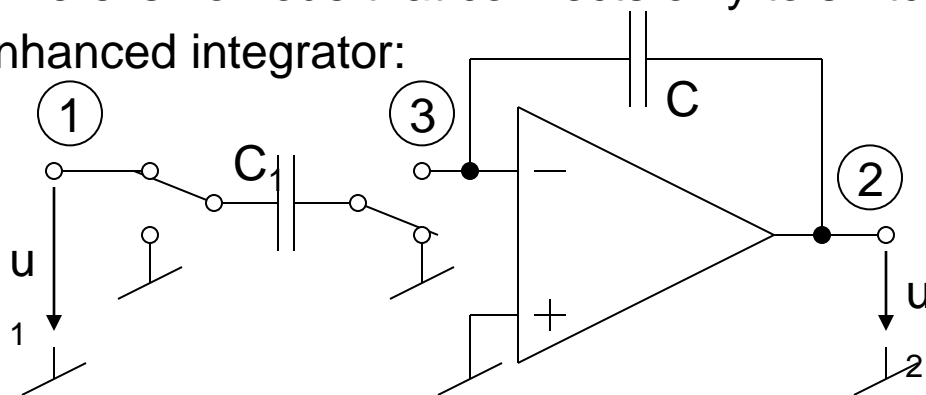
# Parasitic capacitances

Parasitic capacitances appear in all circuits.

Circuits that are insensitive to parasitic capacitances, have the following 4 properties:

- Operational amplifiers have one input connected to ground.
- There is no node that connects only to capacitors.
- No commutations occur between a voltage node (a circuit input or an output of an operational amplifier) and virtual ground.
- There is no node that connects only to switches.

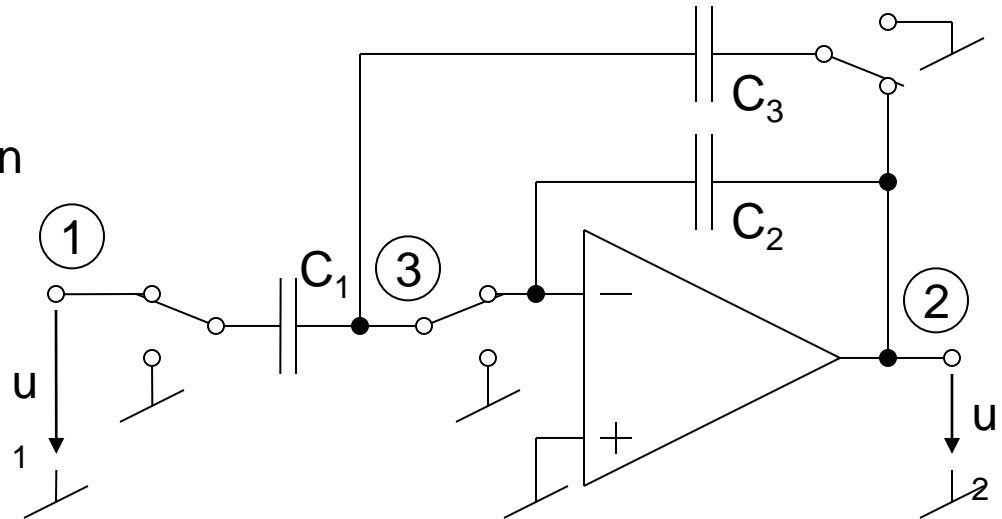
Enhanced integrator:



$$\frac{U_2(z)}{U_1(z)} = + \frac{C_1}{C} \frac{1}{z-1}$$

# First order low pass filter

Position of switches shown is for the even interval.



- even circuit:

$$C_1(u_{1,2nT} - u_{3,2nT}) + (C_2 + C_3)(u_{2,2nT} - u_{3,2nT}) =$$

$$= C_1(0 - u_{3,2nT-T}) + C_2(u_{2,2nT-T} - 0) + C_3(0 - u_{3,2nT-T})$$

$$u_{3,2nT} = u_{3,2nT-T} \equiv 0 \Rightarrow C_1 u_{1,2nT} + (C_2 + C_3) u_{2,2nT} = C_2 u_{2,2nT-T}$$

- odd circuit:

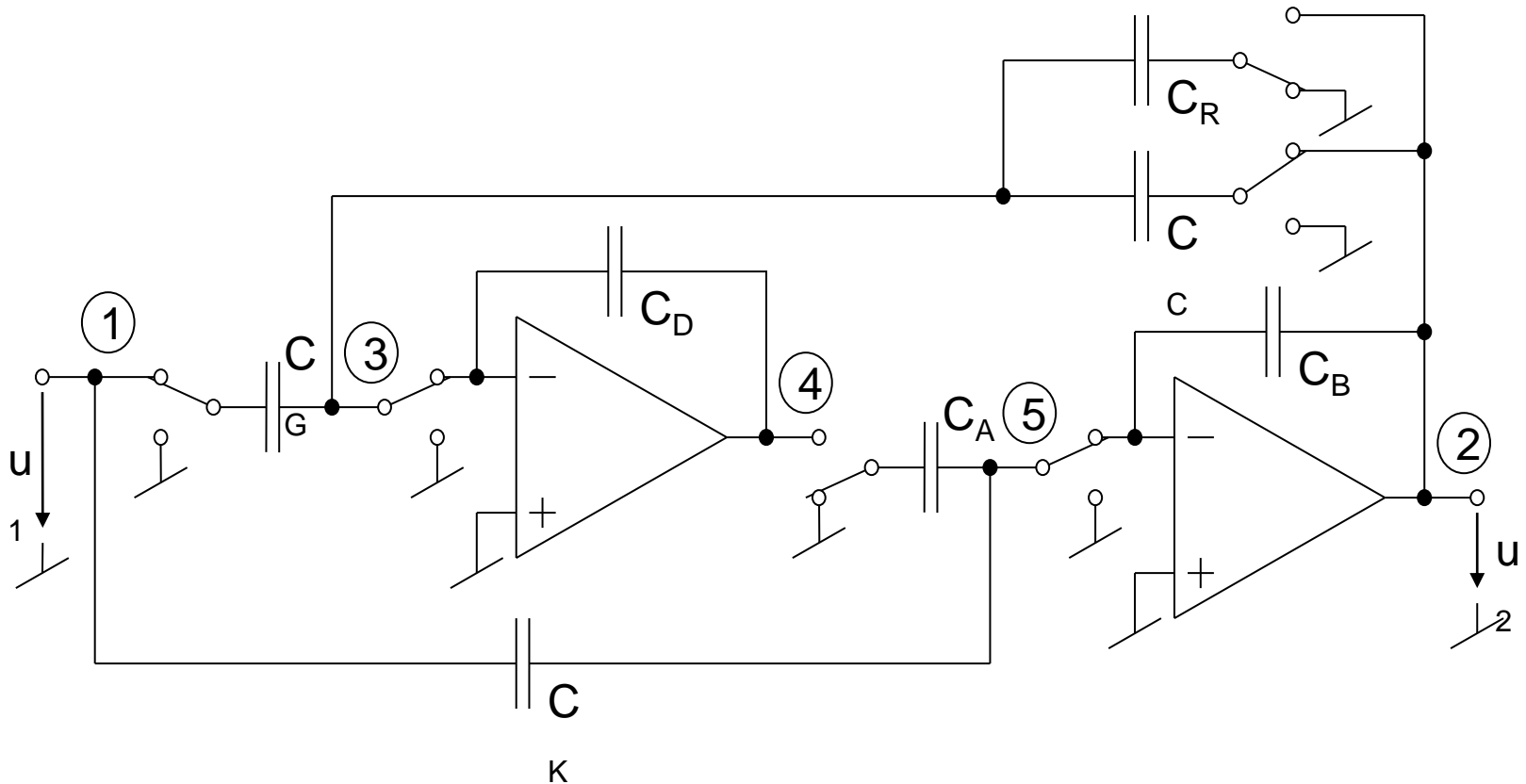
$$u_{2,2nT-T} = u_{2,2nT-2T}$$

$$C_1 U_1(z) + (C_2 + C_3) U_2(z) = C_2 U_2(z) z^{-1}$$

- transfer function:

$$\frac{U_2(z)}{U_1(z)} = \frac{C_1}{C_2 z^{-1} - C_2 - C_3}$$

## Second order low pass filter (1)



Position of switches shown is for the even interval.

## Second order low pass filter (2)

-Even circuit:

Node ③

$$\begin{aligned}
 & C_G(u_{1,2nT} - u_{3,2nT}) + C_D(u_{4,2nT} - u_{3,2nT}) + C_C(u_{2,2nT} - u_{3,2nT}) + C_R(0 - u_{3,2nT}) = \\
 & = C_G(0 - u_{3,2nT-T}) + C_D(u_{4,2nT-T} - u_{3,2nT-T}) + C_C(0 - u_{3,2nT-T}) + C_R(u_{2,2nT-T} - 0) \\
 & u_{3,2nT} = u_{3,2nT-T} \equiv 0 \Rightarrow C_G u_{1,2nT} + C_D u_{4,2nT} + C_C u_{2,2nT} = C_D u_{4,2nT-T} + C_R u_{2,2nT-T}
 \end{aligned}$$

Node ⑤

$$\begin{aligned}
 & C_A(0 - u_{5,2nT}) + C_B(u_{2,2nT} - 0) + C_K(u_{1,2nT} - u_{5,2nT}) = \\
 & = C_A(u_{4,2nT-T} - 0) + C_B(u_{2,2nT-T} - u_{5,2nT-T}) + C_K(u_{1,2nT-T} - 0) \\
 & u_{5,2nT} = u_{5,2nT-T} \equiv 0 \Rightarrow C_B u_{2,2nT} + C_K u_{1,2nT} = C_A u_{4,2nT-T} + C_B u_{2,2nT-T} + C_K u_{1,2nT-T}
 \end{aligned}$$

- Odd circuit:  $u_{2,2nT-T} = u_{2,2nT-2T}$ ,  $u_{4,2nT-T} = u_{4,2nT-2T}$

Assumption:  $u_{1,2nT-T} = u_{1,2nT-2T}$  (S & H in front of the filter)

- Transfer function:

place ⑤ in ③ to  
eliminate  $u_4 \Rightarrow$

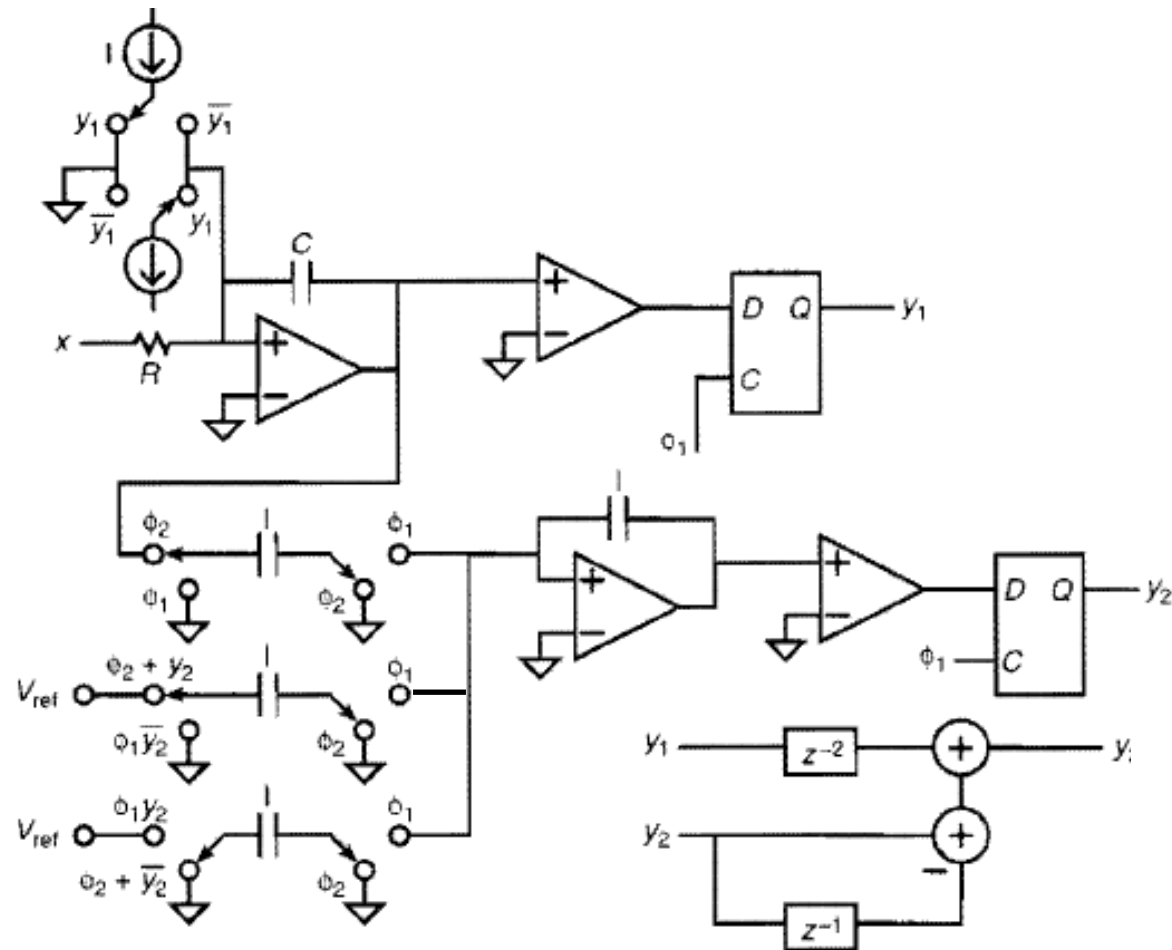
$$\frac{U_2(z)}{U_1(z)} = -\frac{C_K}{C_B} \frac{z^2 + \left( \frac{C_A C_G}{C_D C_K} - 2 \right) z + 1}{z^2 + \left( \frac{C_A C_C}{C_B C_D} - 2 \right) z + 1 - \frac{C_A C_R}{C_B C_D}}$$

# Second order high pass filters

- Propose circuits for second order switched capacitor high-pass filters.

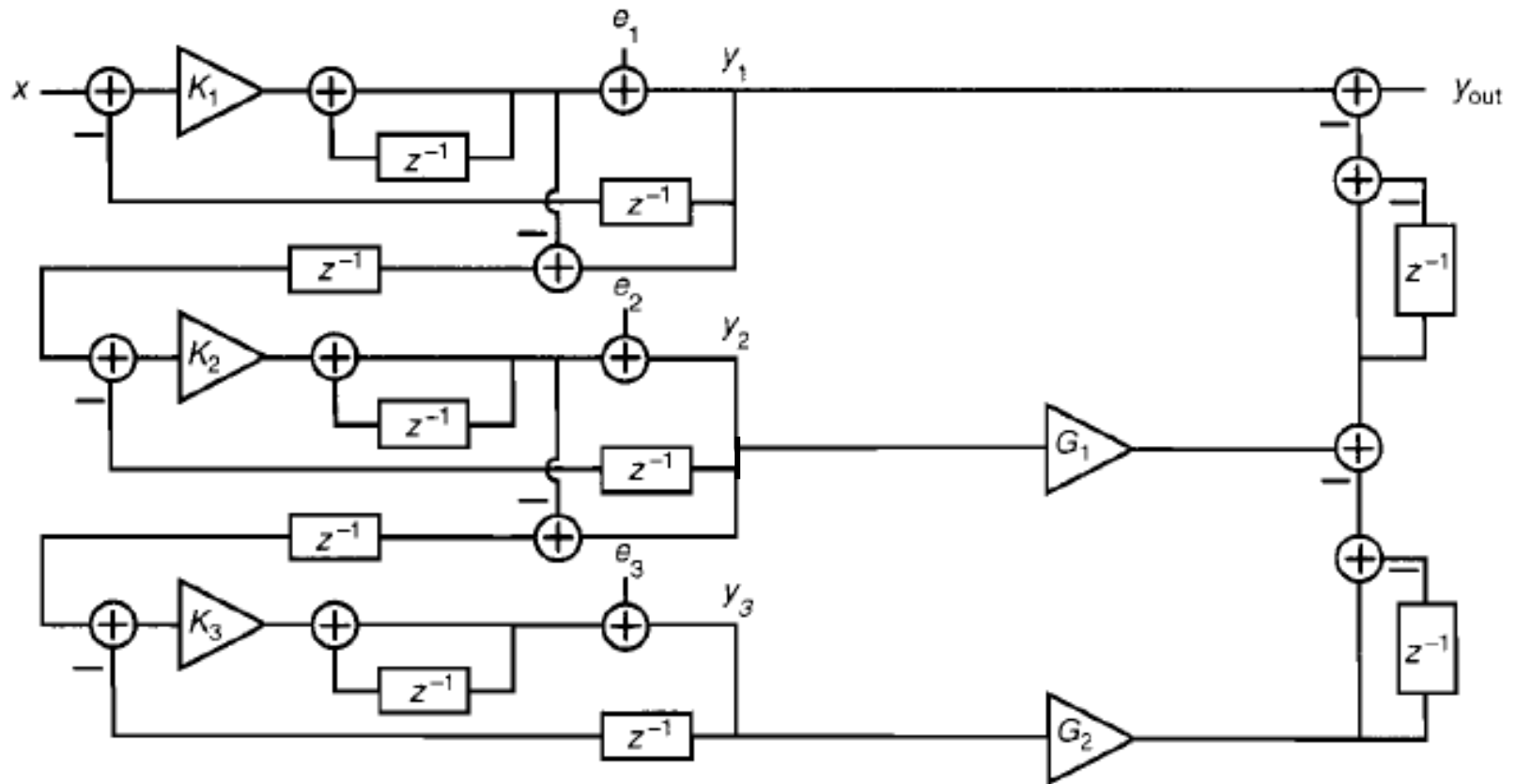


# Cascaded second order modulator circuit



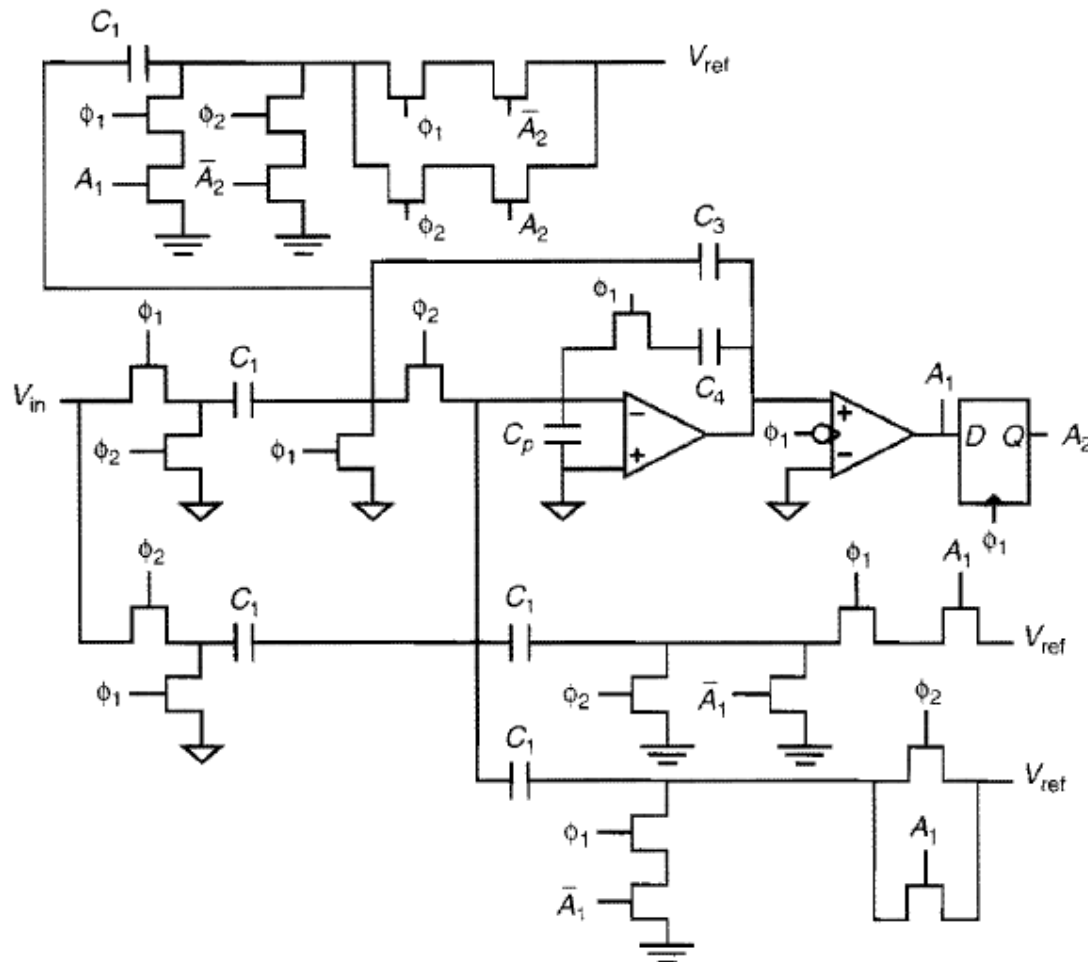
A (1-1) cascade, with continuous-time first modulator.

# Cascaded third order modulator structure



- Develop the difference equation relating  $y_{out}$  to  $x$ , to  $e_1$ ,  $e_2$  and  $e_3$ .
- Estimate the frequency response of  $y_{out}$  excited by  $x$ , and the noise spectrum of  $y_{out}$ , assuming white noise inputs  $e_1$ ,  $e_2$ ,  $e_3$ .
- Represent your results in graphs.

# Cascaded third order modulator circuit



**Figure 6.10** First modulator in third-order (1-1-1) cascade.

- Explain the operation of this circuit: Divide it into functional blocks. Draw a chronogram of its operation, with non-overlapping antiphase clocks  $\Phi_1$ ,  $\Phi_2$ , and signals  $A_1$ ,  $A_2$  and their inverses.

# References

U. Beis: *Eine Einführung in Delta-Sigma-Wandler* ,  
[http://www.beis.de/Elektronik/DeltaSigma/DeltaSigma\\_D.html](http://www.beis.de/Elektronik/DeltaSigma/DeltaSigma_D.html)

**This reference was used as a basis for the present presentation, several illustrations are taken from it.**

R. Schreier, G. C. Temes: *Understanding Delta-Sigma Data Converters*, IEEE Press 2004, ISBN 0-4714-6585-2

R. Norsworthy, R. Schreier, G. C. Temes: *Delta-Sigma Data Converters*, IEEE Press 1996, ISBN 0-7803-1045-4

Tietze, Schenk: *Halbleiter-Schaltungstechnik*, Springer 2010 (13<sup>th</sup> ed.), ISBN 3-540-64192-0