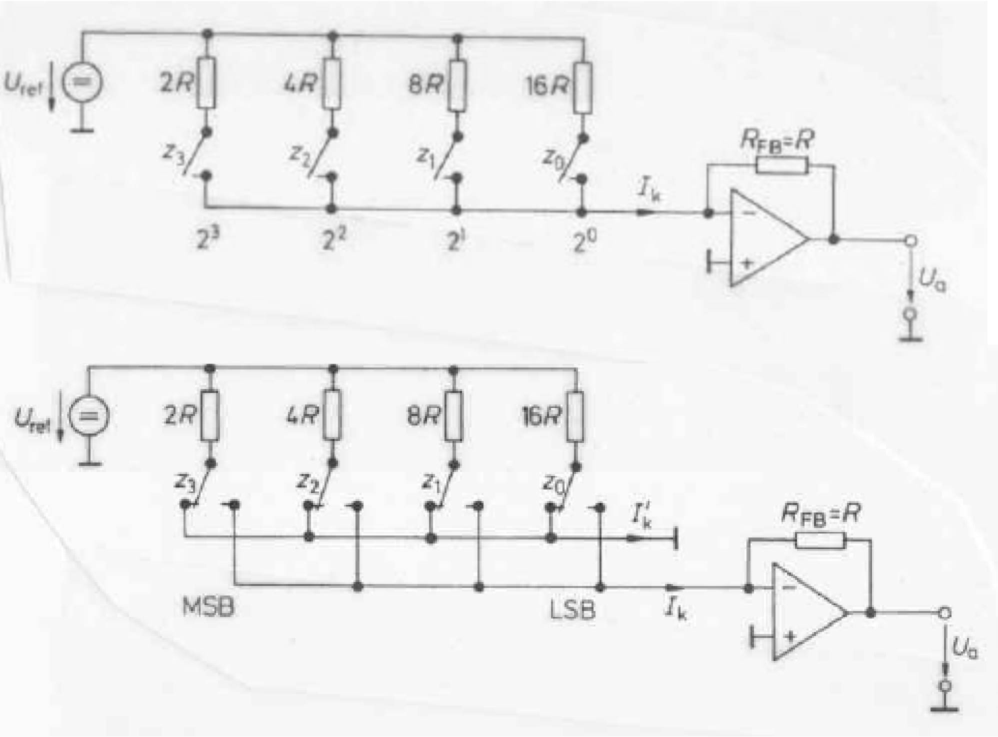
Binary weighted structure

The two schematics below show binary weigthed structures for DA conversion. The principal inconvenients of the upper structure are

- The load of Uref is not constant, but depends on z.
- The parasitic capacitances of the switches are (dis)charged when switching.

Explain why the lower schematic solves these problems.



Exercice

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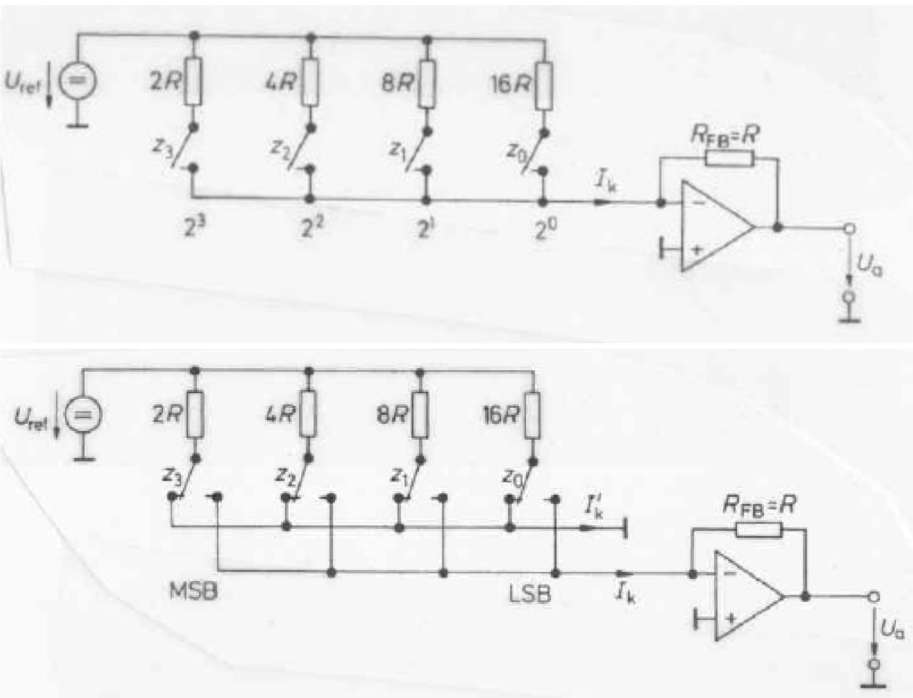


- The load of Uref is always the same, independantly of the switch positions, since current always flows into one of two collector rails.
- The connections of any switch are always at the same potential, so that no charging / discharging of stray capacitances occurs.

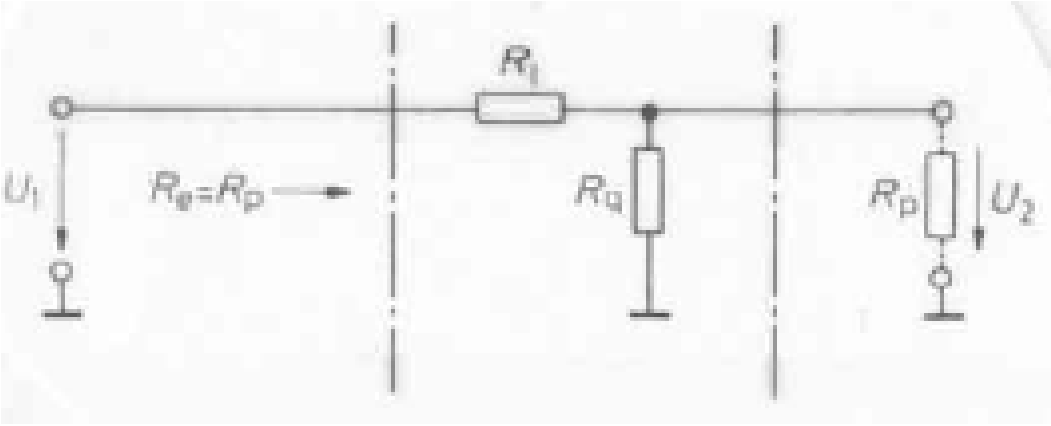
Exercice

Generalized ladder network

Draw a schematic of a voltage output 4bit-DAC with an R/2R ladder network, using commutators between two output current rails.

With the help of the circuit shown below, express R_l and R_p as functions of R_q, so that

$$U_2/U_1 = \alpha$$



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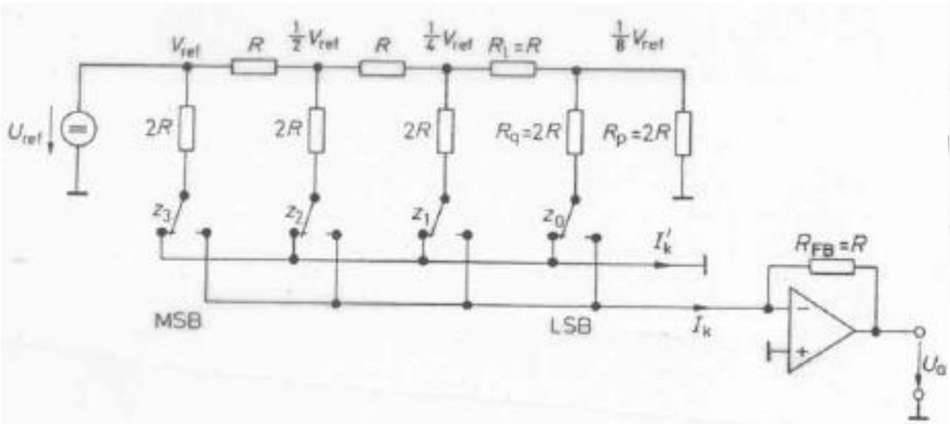
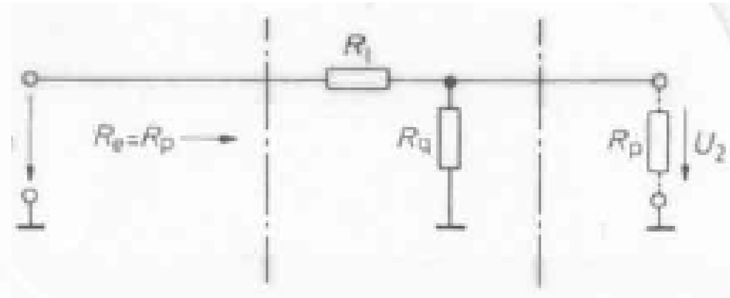




With the help of the circuit shown above, express R_l and R_p as functions of R_q, so that $\alpha = U_2 / U_1$

$$R_e = R_p = R_l + \frac{R_p R_q}{R_p + R_q} \quad \Rightarrow \quad R_l = \frac{R_p^2}{R_p + R_q}$$

$$\alpha = \frac{U_2}{U_1} = \frac{R_q}{R_p + R_q} \quad \Rightarrow \quad R_p = R_q\left(\frac{1}{\alpha} - 1\right)$$

$$R_l = \alpha\left(\frac{1}{\alpha} - 1\right)^2 R_q = \frac{(1-\alpha)^2}{\alpha} R_q$$

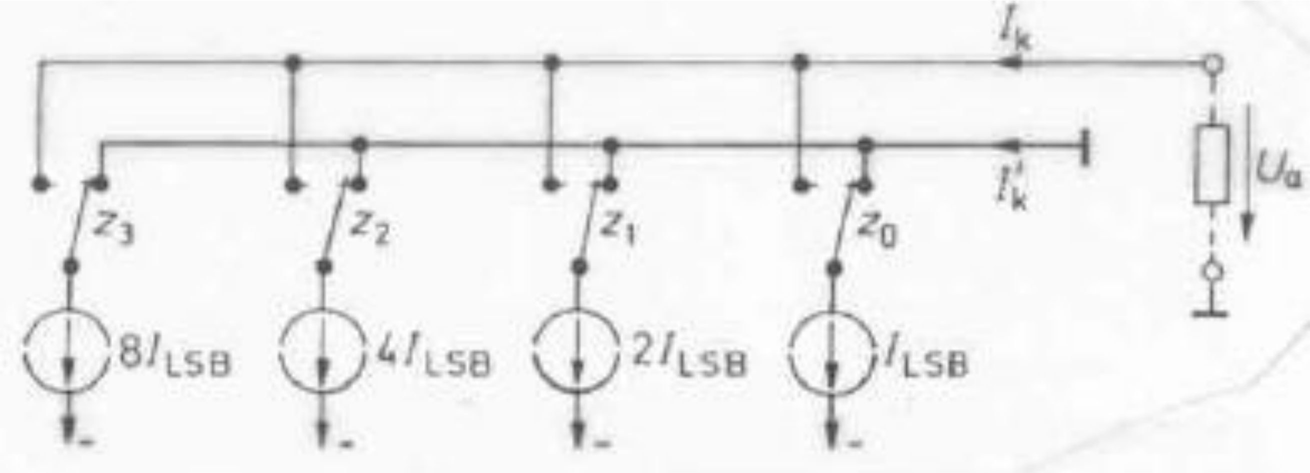
In particular, for α = 0.5:

$R_p = R_q = 2\ R_l$

Exercice

Arrays of current sources

Instead of a reference voltage and a set of weighted resistors, a set of weighted current sources can be used for DA converion as shown below.

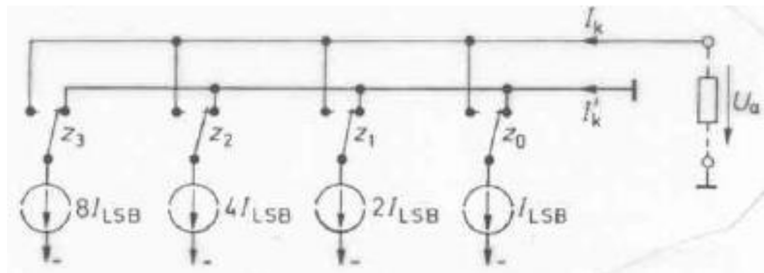


Propose an alternative circuit using a set of current sources of same value and a ladder network for DA conversion.

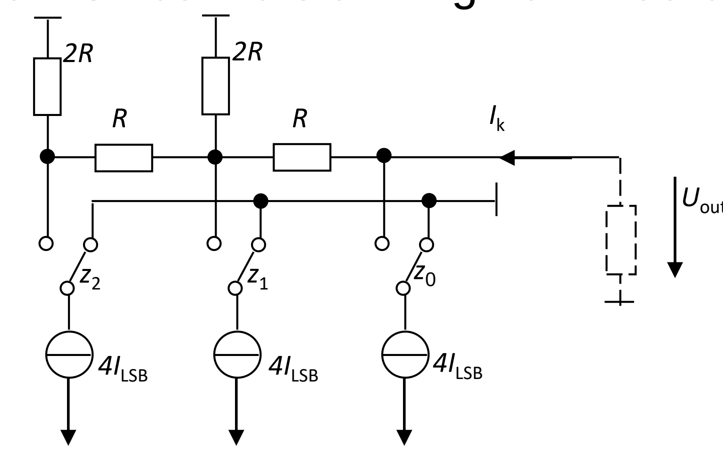
Exercice

Arrays of current sources

Instead of a reference voltage and a set of weighted resistors, a set of weighted current sources can be used for D/A converion as shown below.



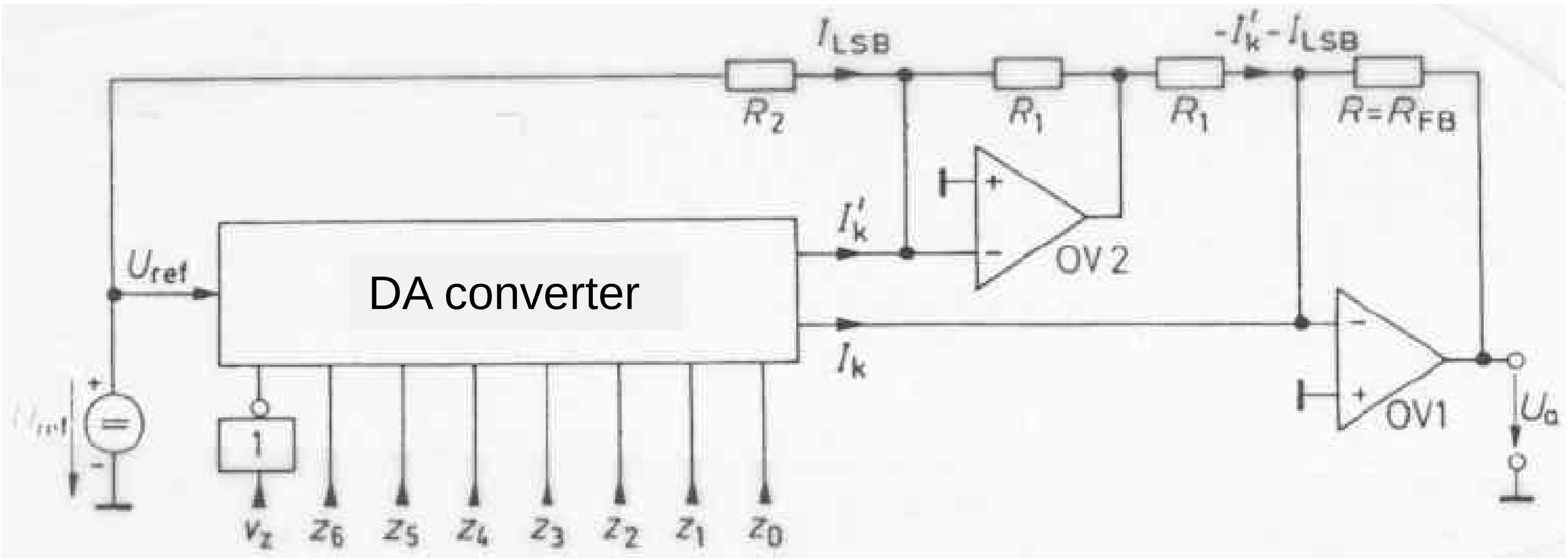
Propose an alternative circuit using a set of current sources of same value and a ladder network for D/A conversion. E.g. for three bits:



Exercice

Bipolar output

For the circuit shown below, determine U_a as a function of Z, a signed binary number in 2's complement representation. I_k and I_k' are the two complementary current outputs of the DA converter.

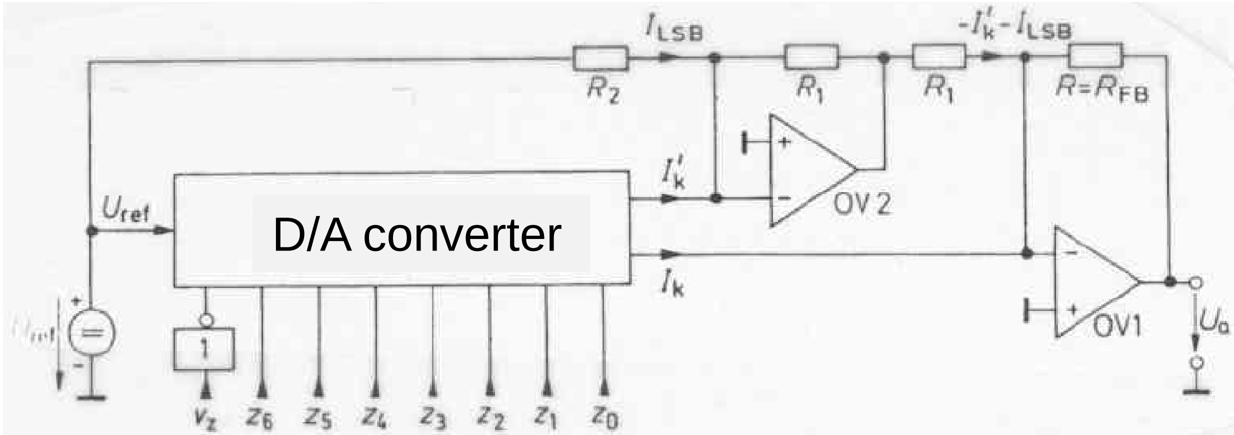


What is the range of U_a?

Exercice

Bipolar output

For the circuit shown below, determine U_a as a function of Z, a signed binary number in 2's complement representation. Ik and Ik' are the two complementary current outputs of the D/A converter.



$$-2^{n-1} < Z = \left[v_z, z_{n-1}, \cdots, z_0\right] < 2^{n-1} - 1$$

$$I_k = \frac{U_{ref}}{R}\frac{Z + 2^{n-1}}{2^n}, \quad I'_k = \frac{U_{ref}}{R}\left(1 - \frac{1}{2^n}\right) - I_k = \frac{U_{ref}}{R}\frac{2^{n-1} - Z - 1}{2^n}$$

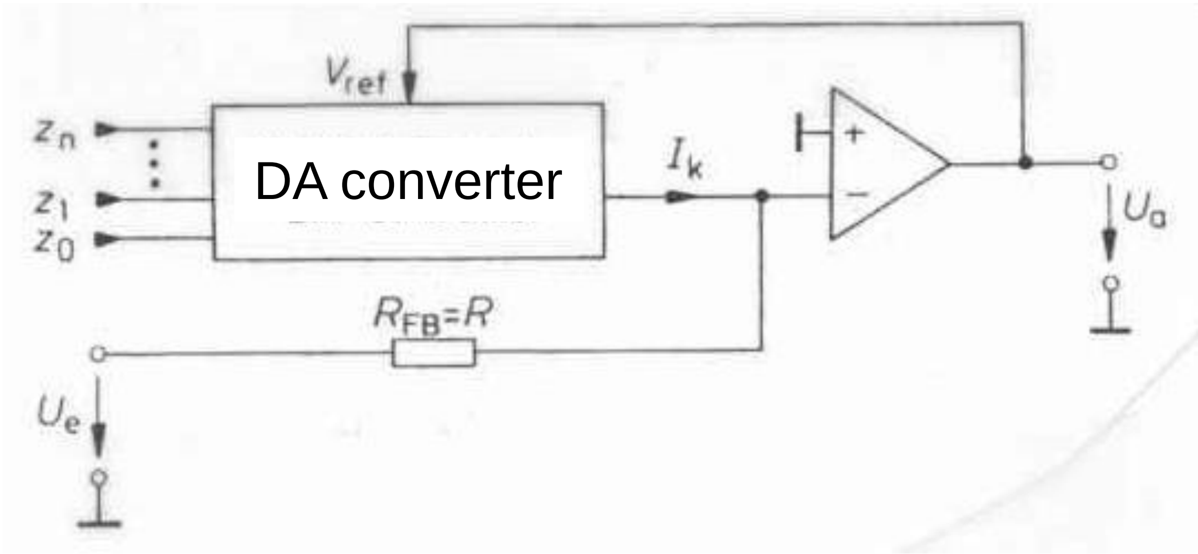
$$R_2 = \frac{R}{2^n} \quad \Rightarrow \quad I_{LSB} = \frac{U_{ref}}{2^n R}$$

$$U_a = \left(I'_k + I_{LSB} - I_k\right)R = U_{ref}\frac{2^{n-1} - Z - 1 + 1 - Z - 2^{n-1}}{2^n} = -U_{ref}\frac{Z}{2^{n-1}}$$

Exercice

Multiplication / division

Show that in the circuit below, the output voltage U_a is proportional to U_e/Z.



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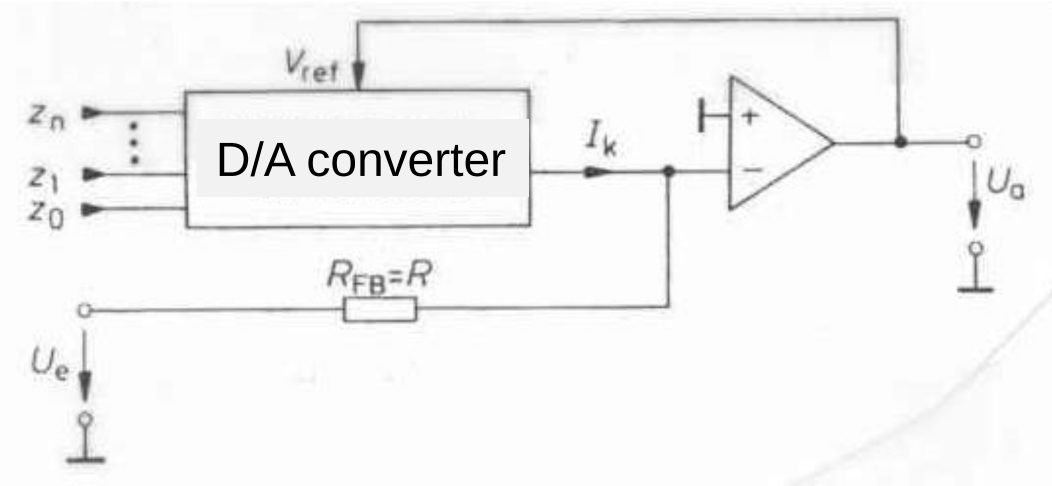
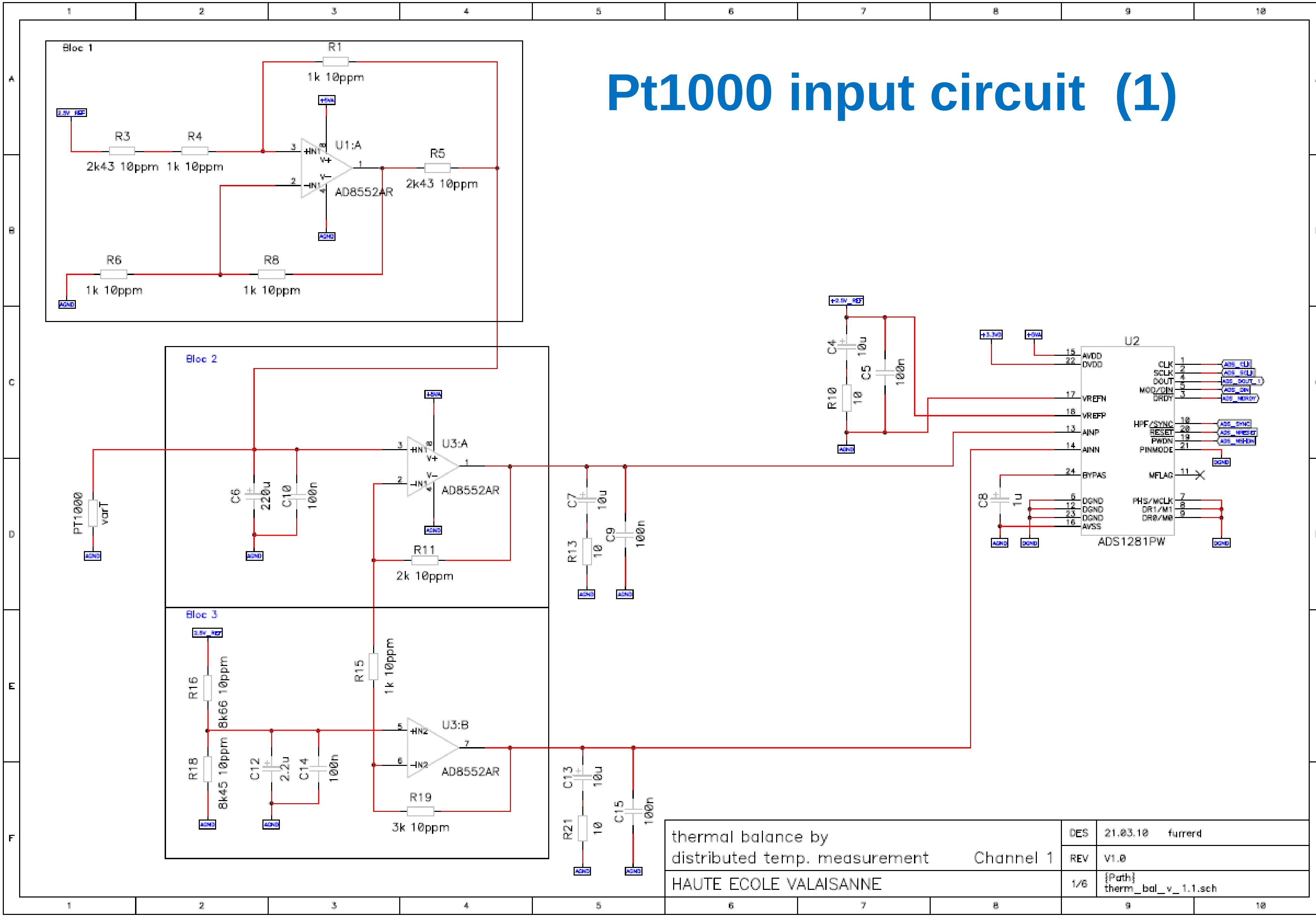


$$I_k = \frac{V_{ref}}{R}\frac{Z}{2^n} = \frac{U_a}{R}\frac{Z}{2^n} = -\frac{U_e}{R_{FB}} = -\frac{U_e}{R} \quad \Rightarrow \quad U_a = -U_e\frac{2^n}{Z}$$

Exercice

Pt1000 input circuit (1)



Exercice

Pt1000 input circuit (2)

The circuit on the slide above acquires a temperature measured by a Pt1000 resistor, through a 24 bits ADC (ADS1281), with the following characteristics : f_s = 10Hz, dynamic range of AINP and AINN : 0…V_{ref}, conversion of V_{AINP}-V_{AINN} within the range ±V_{ref}. V_{ref} = 2.5V (net +2.5V_REF).

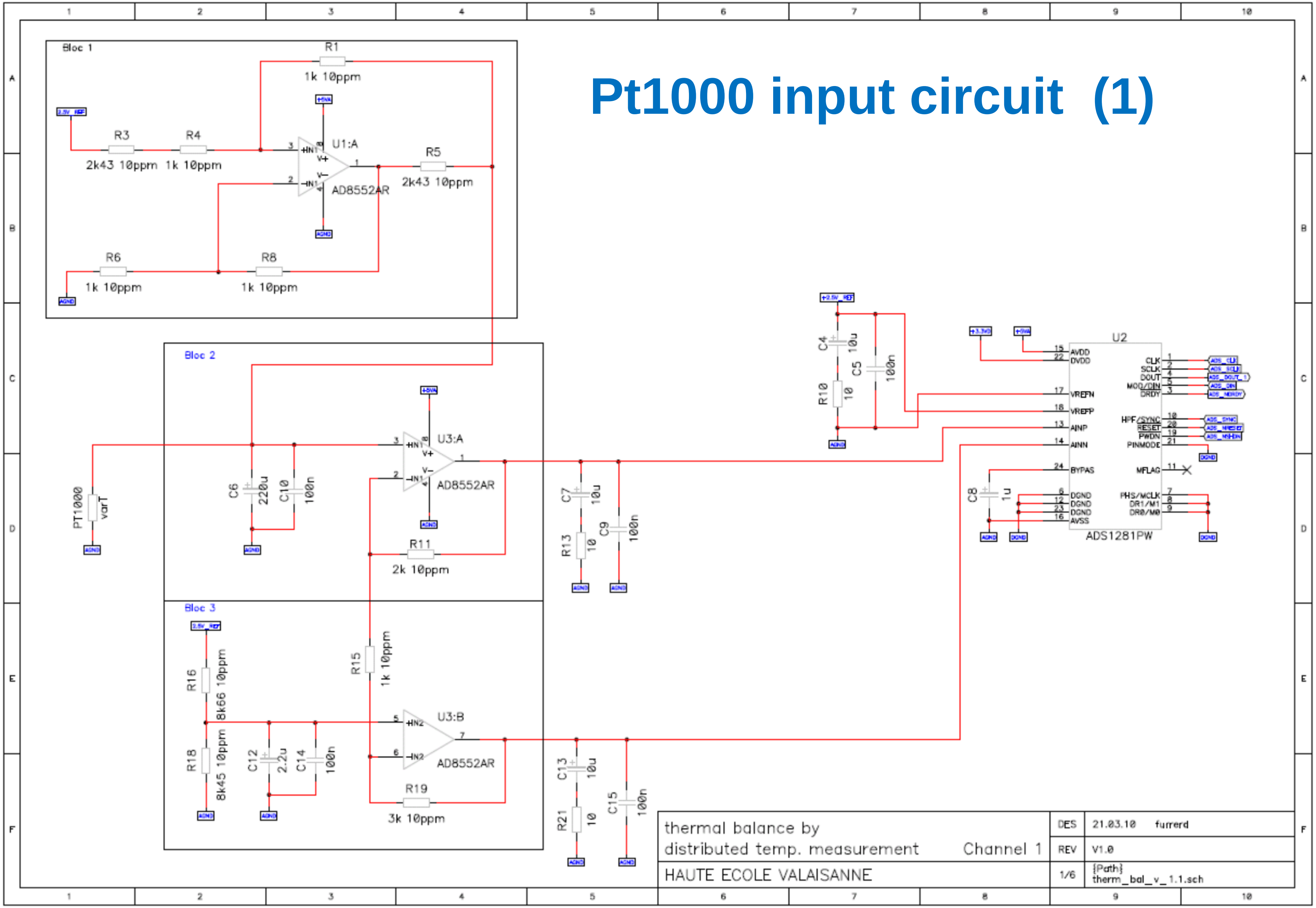
➢ Describe in words the function of each of the 3 framed blocks.

➢ Why are resistors R16 and R18 not set to equal values ?

➢ Determine the temperature measurement range in °C and the circuit sensitivity in LSB/°C, knowing that the resistance of the Pt1000 sensor is 1000Ω at 0°C, increasing by 0.4%/°C.

➢ Consider only voltage and current noises of the operational amplifiers AD8552: 40nV/rtHz and 2fA/rtHz, supposed to be uniform over frequency. What is the spectral density of the current noise in the Pt1000 sensor ? What is the spectral density of the voltage noise at inputs AINP and AINN of the A/D converter ? What is the signal-to-noise ratio between 0 and 5Hz after A/D conversion, taking into account quantization noise and noise in the operational amplifiers ?

Pt1000 input circuit (1)



Pt1000 input circuit (2)

The circuit on the slide above acquires a temperature measured by a Pt1000 resistor, through a 24 bits ADC (ADS1281), with the following characteristics : f_s = 10Hz, dynamic range of AINP and AINN : 0…V_{ref}, conversion of V_{AINP}-V_{AINN} within the range ±V_{ref}. V_{ref} = 2.5V (net +2.5V_REF).

- Describe in words the function of each of the 3 framed blocks.

$U_i = U_o * R_6 / (R_6 + R_8) = U_o / 2$
$I_P = (V_{ref} - U_i) / (R_3 + R_4)$
$I_{out} = I_{R5} + I_P = (U_o – (U_i – R_1 I_P)) / R_5 + I_P = (U_o / 2 + R_1 I_P) / R_5 + I_P$
$I_{out} = U_o / (2 R_5) + I_P (R_1 + R_5) / R_5 = U_o / (2 R_5) + (V_{ref} - U_i) / R_5 = V_{ref} / R_5$
=1.03mA
Block 1 : constant current source

$U_{iB} = V_{ref} * R_{18} / (R_{16} + R_{18}) = 1.235V$
$U_{iA} = U_{PT1000}$
$U_{AINP} = 3 U_{Pt1000} – 2 U_{iB}$
Block 2 : Range adaptation for input AINP of the ADC.
$U_{AINN} = 4 U_{iB} - 3 U_{Pt1000}$
Block 3 : Generation of inverted signal for input AINN of the ADC.

Pt1000 input circuit (3)

➢ Why are resistors R16 and R18 not set to equal values ?
This is to avoid saturation of inputs AINP and AINN close to full scale values.

➢ Determine the temperature measurement range in °C and the circuit sensitivity in LSB/°C, knowing that the resistance of the Pt1000 sensor is 1000Ω at 0°C, increasing by 0.4%/°C.

$U_{AINP} = 0$ for $U_{Pt1000} = 2\,U_{iB} / 3 = 0.823V \Rightarrow R_{Pt1000} = 800\Omega$, $T_{min} = -50°C$

$U_{AINN} = 0$ for $U_{Pt1000} = 4\,U_{iB} / 3 = 1.646V \Rightarrow R_{Pt1000} = 1600\Omega$, $T_{max} = 150°C$

Measurement range from -50°C to +150°C

$U_{AINNmax} = U_{AINPmax} = 2U_{iB} = 2.470V$

Sensitivity $= 2^{24} * (U_{AINNmax} + U_{AINPmax}) / (2V_{ref}) / (T_{max} - T_{min}) = 82'879$ LSB/°C

Pt1000 input circuit (4)

➢ Consider only voltage and current noises of the operational amplifiers AD8552: 40nV/rtHz and 2fA/rtHz, supposed to be uniform over frequency. What is the spectral density of the current noise in the Pt1000 sensor ? What is the spectral density of the voltage noise at inputs AINP and AINN of the A/D converter ? What is the signal-to-noise ratio between 0 and 5Hz after A/D conversion, taking into account quantization noise and noise in the operational amplifiers ?

Spectral current noise density in the Pt1000 sensor:

$I_{nPu} = (U_n - U_i) / (R_3 + R_4)$

$I_{noutu} = (2U_i – (U_i - U_n – R_1 I_{nPu})) / R_5 + I_{nPu} = 2U_n / R_5 = 32.9$pA/rtHz

I_{nouti} is negligible, since at least one order of magnitude smaller than I_{noutu}.

$I_{nout} = I_{noutu} = 32.9$pA/rtHz in the Pt1000.

The voltage noise of U3:A is amplified like U_{Pt1000}, the one of U3:B like U_{iB}.
Current noises are again negligible, given the level of resistors present.

Spectal density of noise contributed by U3:A

$U_{nAINP} – U_{nAINN} = 6U_n = 240$nV/rtHz

Spectral density of noise contributed by U3:B

$U_{nAINP} – U_{nAINN} = 6U_n = 240$nV/rtHz

Pt1000 input circuit (5)

Spectral density of noise contributed by the current source (e.g. in centre of range, $R_{Pt1000} = 1200\Omega$)
$U_{nAINP} - U_{nAINN} = 6R_{Pt1000}I_{nout} = 237nV/rtHz$

Spectral density of total analog noise :
$U_{nAINP} - U_{nAINN} = sqrt(240^2 + 240^2 + 237^2)$ [nV/rtHz] = 414nV/rtHz
Within the frequency band 0…5Hz :
$(U_{nAINP} - U_{nAINN})_{rms} = 926nV$

1LSB corresponds to $2*2.5V/2^{24} = 298nV$, equivalent spectral density of quantization noise : $U_{LSB}/sqrt(12) = 86nV/rtHz$

Spectral density of total noise :
$U_{nAINP} - U_{nAINN} = sqrt(240^2 + 240^2 + 237^2 + 86^2)$ [nV/rtHz] = 423nV/rtHz
Within the frequency band 0…5Hz :
$(U_{nAINP} - U_{nAINN})_{rms} = 945nV$

SNR = 20 log10 $(V_{ref}/sqrt(2) / (U_{nAINP} - U_{nAINN})_{rms})$ = 125dB

Effect of clock jitter on conversion noise

We have a 20bit audio SAR ADC with a sampling clock rate of f_s = 48ksps. How much rms jitter of the ADC clock signal (suppose $f_{CLK} = 24 \cdot f_s$) can be admitted, so that the conversion error remains below one LSB for sinusoidal full scale input (±1V) signals of frequency f = 4kHz?

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Largest error at zero crossing of sine oscillation, since slope is maximum there:

$$\left.\frac{du}{dt}\right|_{t=0} = \hat{U}\omega$$

Amplitude error resulting from sampling instant uncertainty Δt_A :

$$\Delta u = \hat{U} 2\pi f \Delta t_A$$

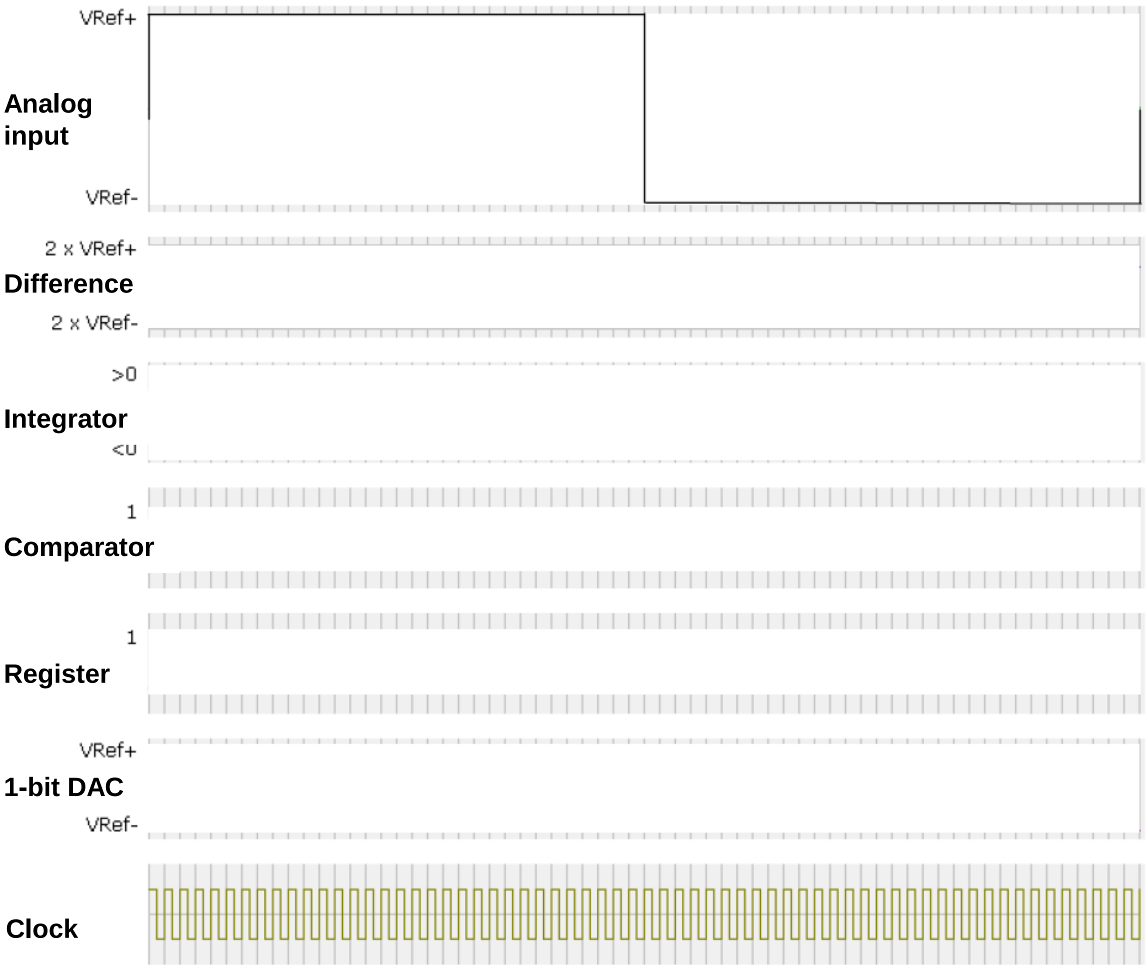
The amplitude of the sine signal is half of the input range U_{max}, so :

$$\hat{U} \le \frac{U_{FS}}{2}, \quad \mathrm{U}_{\mathrm{LSB}} = \frac{\mathrm{U}_{\mathrm{FS}}}{2^{\mathrm{n}}} \quad \Rightarrow \quad \Delta t_{A,pk-pk} \le \frac{1}{2^n \pi f}, \quad \Delta t_{A,rms} \le \frac{1}{6.6 \cdot 2^n \pi f}$$

With given nnumeric values, $\Delta t_{A,rms}$ < 11.5psec.

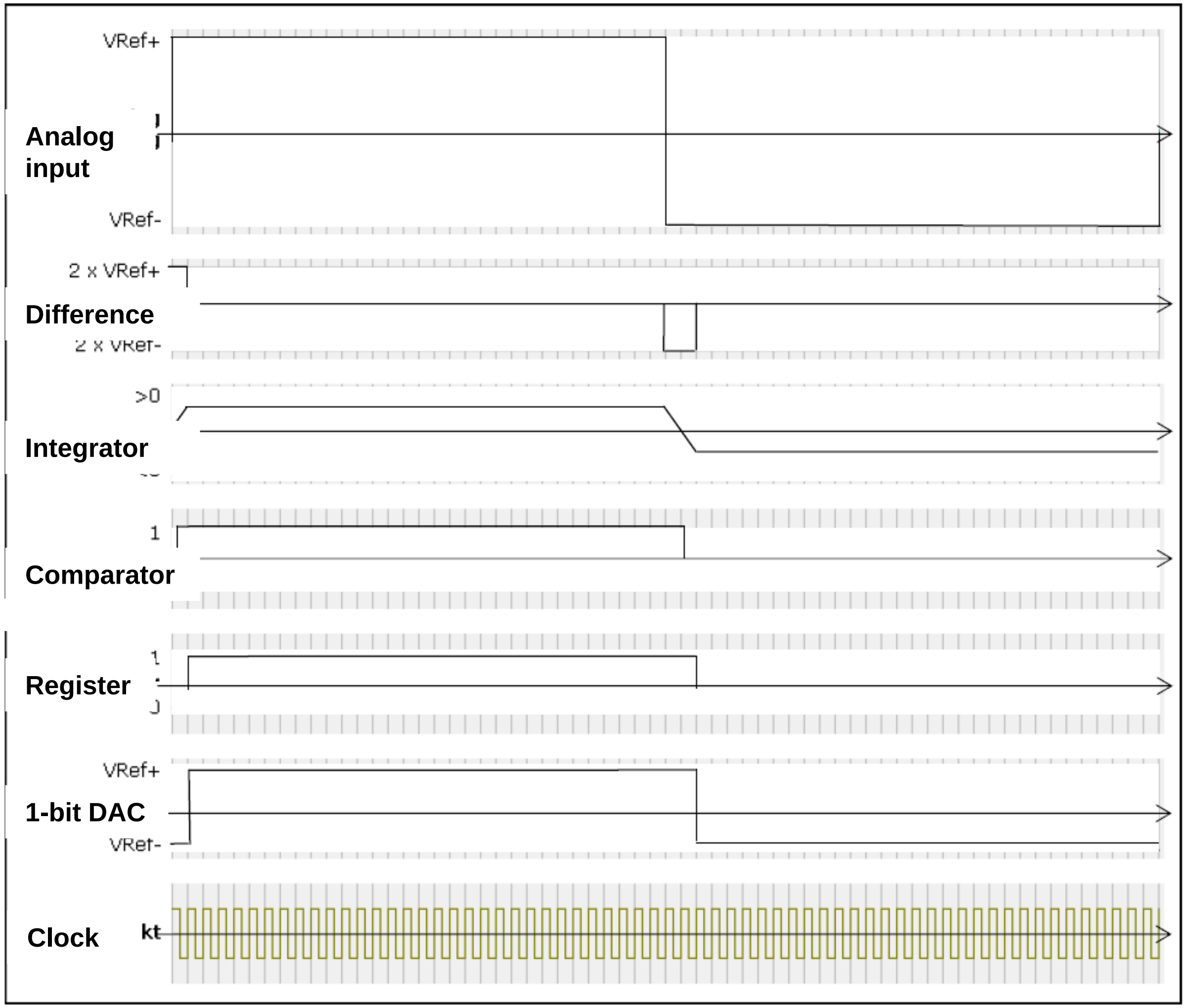
Signal forms

Trace the forms of signals in an analog first order modulator for a rectangular input signal:

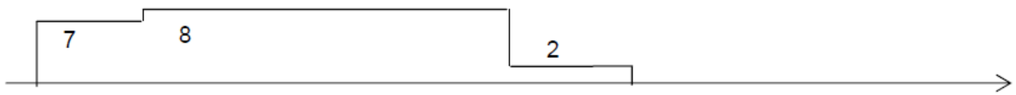


Retrace the bitstream after decimation by 8.

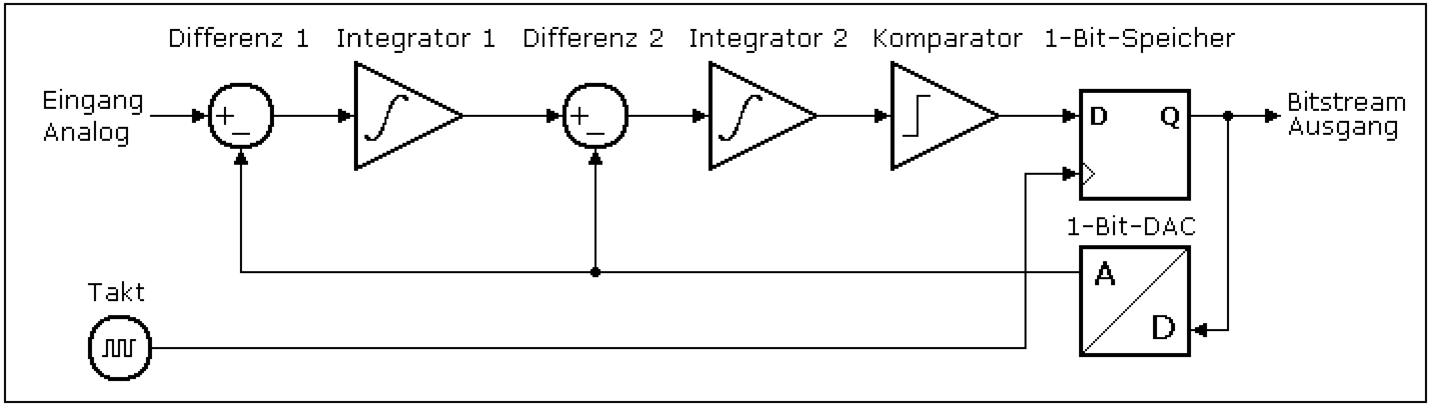
Signal forms



Bitstream after decimation by 8:



Second order modulator transfer functions



- Determine the equivalent continuous transfer functions of a second order delta-sigma modulator, for the signal and for the noise.
- Represent the corresponding amplitude responses in a Bode diagram.

Second order modulator transfer functions

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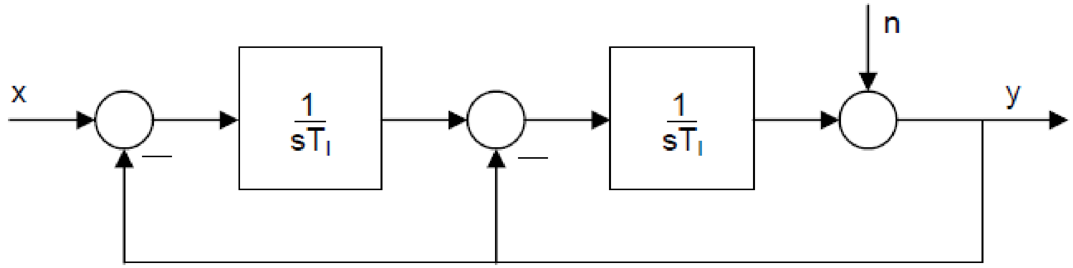
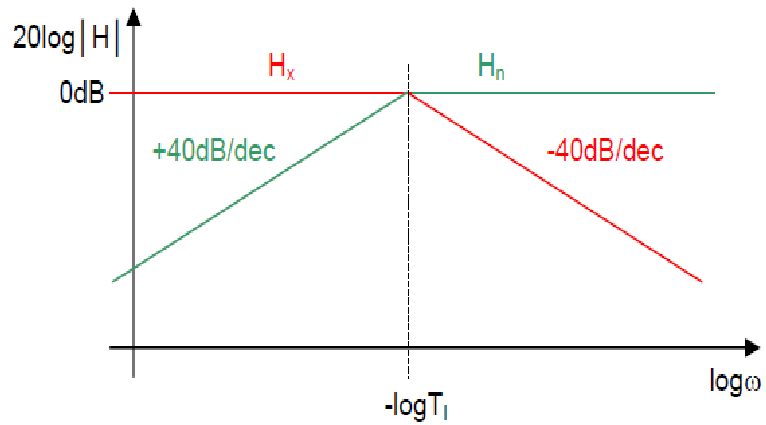


$$y = n + \frac{1}{sT_I}\left(-y + \frac{1}{sT_I}(x-y)\right)$$

$$y\left(s^2T_I^2 + sT_I + 1\right) = ns^2T_I^2 + x$$

Signal transfer: $$H_x = \frac{y}{x} = \frac{1}{1 + sT_I + s^2T_I^2}$$

Noise transfer: $$H_n = \frac{y}{x} = \frac{s^2T_I^2}{1 + sT_I + s^2T_I^2}$$



Signal to noise and oversampling ratios

- What is the maximum signal-to-noise ratio of a 16bit ADC? Suppose a sinusoidal input signal, and that the quantisation noise dominates all other noises. The noise is considered as white noise.
- Which resolution, expressed as number of bits (ENOB), can have an ADC with a second order delta-sigma modulator, operating at an oversampling ratio of 128?
- Consider a delta-sigma ADC with ENOB = 16bits and an input signal bandwidth of 1kHz. The oversampling ratio is 128. Which order is required for an analog anti-aliasing filter?

Signal to noise and oversampling ratios (2)

- Consider a delta-sigma ADC with 16bit resolution and an input signal bandwidth of 1kHz. The oversampling ratio is 128. Which order is required for an analog anti-aliasing filter?

  A maximum attenuation of -SNR = -98dB ≅ 80'000 is required at $f > 128\, f_{c,Antialias}$.
  E.g. for a Butterworth filter, the order *n* is given by

$$H^2_{Anitalias} = \frac{1}{1+\left(\frac{f}{f_{c,Antialias}}\right)^{2n}} \quad \Rightarrow \quad n = \frac{\log\left(\frac{1}{H^2_{Anitalias}} - 1\right)}{2\log\left(\frac{f}{f_{c,Antialias}}\right)} \approx 2.3 \quad \Rightarrow \quad n = 3$$

Second order high pass filters

- Propose circuits for second order switched capacitor high-pass filters.

Second order high pass filters

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