



MASTER OF SCIENCE  
IN ENGINEERING

# ADVANCED ELECTRONIC DESIGN

EMC, signal integrity, grounding and power supply routing,  
decoupling, transmission lines, simulation tools

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# Topics of this series of 3 lessons

## PCB Design

- Lesson 1:
  - Introduction
  - Partitioning, filtering
  - Shielding
  - Image planes
  - Continuous vs split GND concepts
  - Mixed signal circuits
- Lesson 2:
  - Decoupling
  - Transmission lines
  - Guard rings
  - Crosstalk, Ground bounce
  - Differential signalling
  - Terminations
  - Clock distribution: clock skew and clock jitter
- Lesson 3:
  - Place & route strategy
  - Components selection
  - Layer stackups
  - Multicard systems, backplanes
  - Enclosures, connectors and cables
  - ESD + Burst protection
  - 2-layer PCBs
  - Design for testability
  - Prototyping

# Decoupling

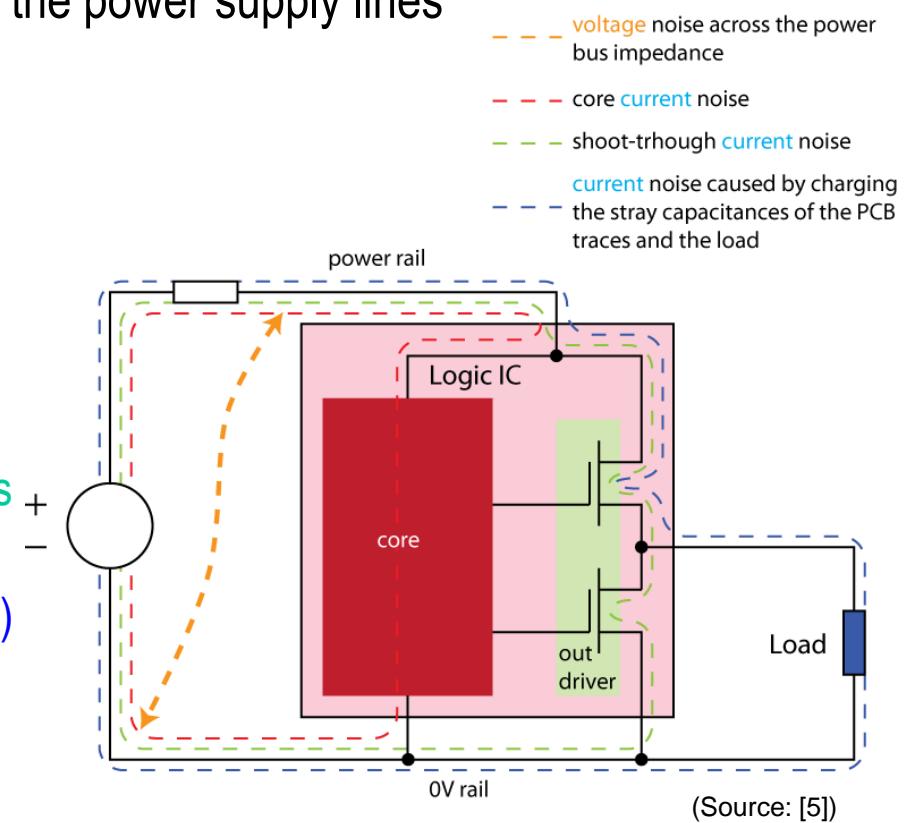
## What is decoupling and why do we need it?

We need to reduce the fluctuations on the power supply lines

- to reduce emissions
- to guarantee correct circuit operation

The fluctuations in the power line  
are due to:

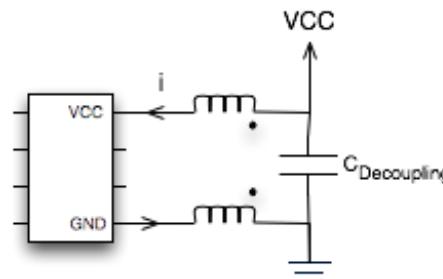
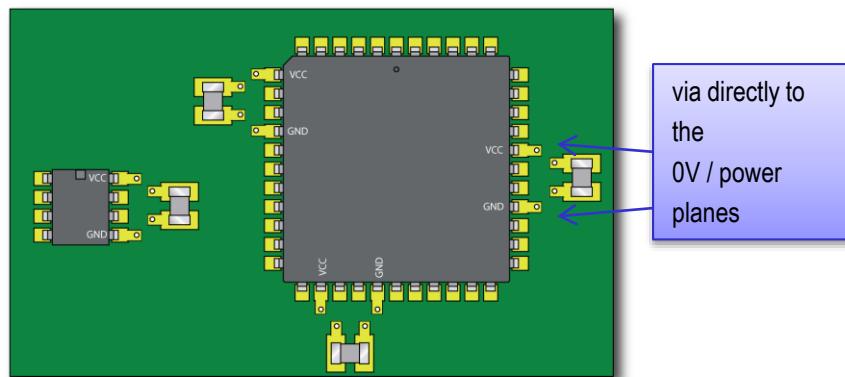
- internal switching noise of the ICs
- vertical shoot-through of output drivers
- high charging/discharging currents of capacitive loads (PCB trace, IC inputs)
- Noisy currents emit magnetic fields
- Noisy voltages emit electric fields



# Decoupling

## To reduce emissions from the power supply circuits

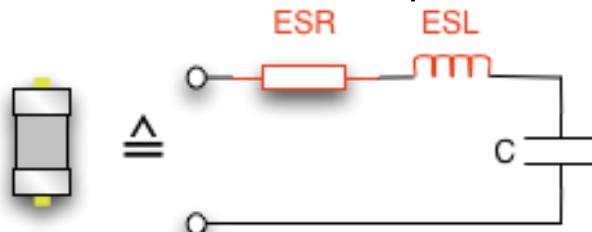
- reduce the amplitude of the voltage fluctuations
  - place decoupling (bypass) capacitors ("decaps") between VCC and GND
  - add one for every power pin of every IC (and even some more...)
- reduce current loop areas
  - reduce connection length between ICs and decoupling capacitors
  - in multilayer PCBs, place 0V and VCC planes adjacent (near)
  - take benefit from mutual inductance in the connection lines to the decap to reduce their voltage drop (impedance) (this is best achieved in multilayer PCBs with GND+VCC layers)



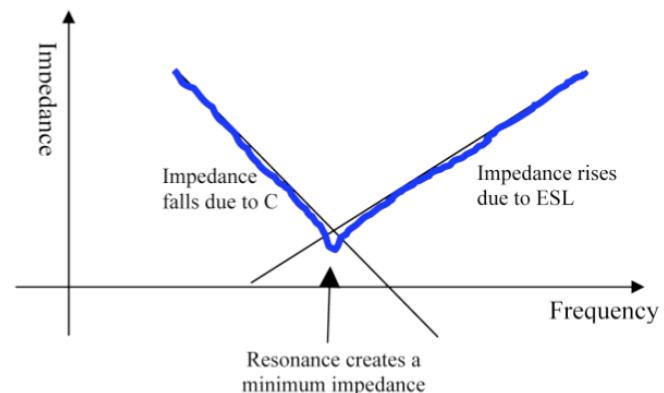
# Decoupling

## Capacitor series resonance

- equivalent circuit of a capacitor:



- ESL + C form a series resonant circuit:  $\omega_{res.} = \frac{1}{\sqrt{LC}}$   
→ increasing C reduces  $\omega_{res.}$  !
- above  $\omega_{resonance}$  the capacitor behaves like an inductor!
- ESL depends on the capacitor case type and size
- minimize PCB trace length (inductance) to decoupling capacitors as this adds to the ESL
- in multilayer PCB's, keep GND and VCC layers at a short distance to the top (component layer) to reduce via lengths (L, loop areas)



# Decoupling

## Capacitor series resonance

- examples of **series resonant frequency** of capacitors:

$$f_{res.} = \frac{1}{2\pi\sqrt{LC}}$$

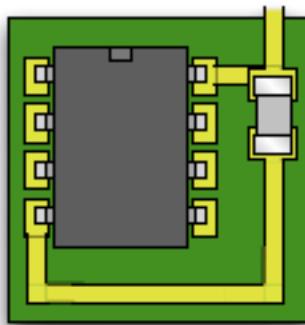
Capacitor value	THT case (6mm leads) ESL ≈ 3.75 nH	SMD 0805 case ESL ≈ 1 nH
1.0 µF	2.6 MHz	5 MHz
100 nF	8.2 MHz	16 MHz
10 nF	26 MHz	50 MHz
1 nF	82 MHz	159 MHz
100 pF	260 MHz	503 MHz

- rule of thumb: 1 cm of thin wire (0.5mm Ø) or 0.25 mm wide PCB trace has an L of 7...10 nH  
**=> use smaller components, with shorter leads**

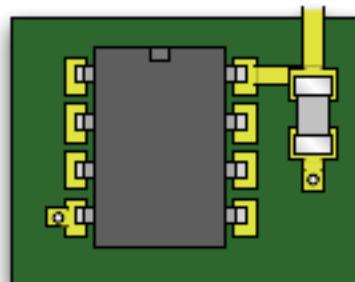
# Decoupling

## Also reduce external wiring length

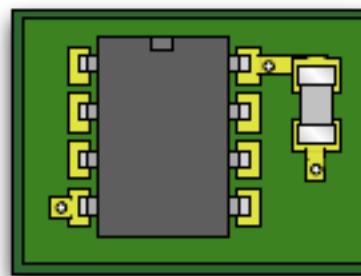
- reduce additional L due to PCB traces that add to the capacitor's ESL
- reduce area of the loop formed by the capacitor and the IC
- examples of positioning and routing of a decoupling capacitor:



BAD



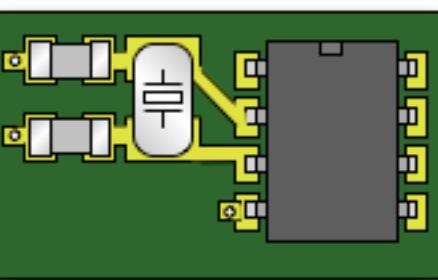
GOOD



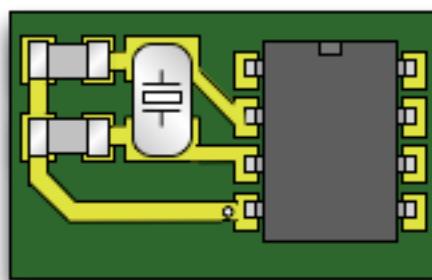
# Oscillator circuits

**Similar considerations apply as with decoupling**

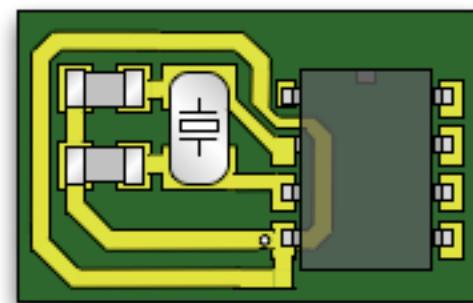
- reduce the area of the oscillator circuit
- keep connections short
- keep noise from GND layer out of the oscillator circuit



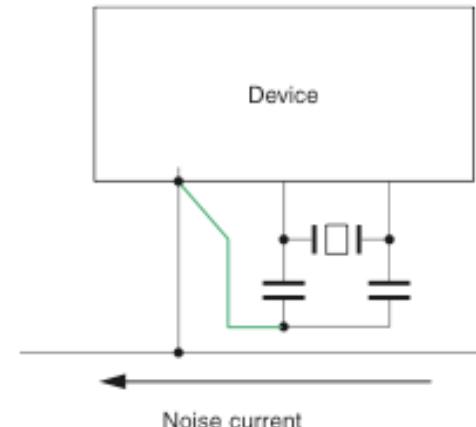
FAIR



GOOD



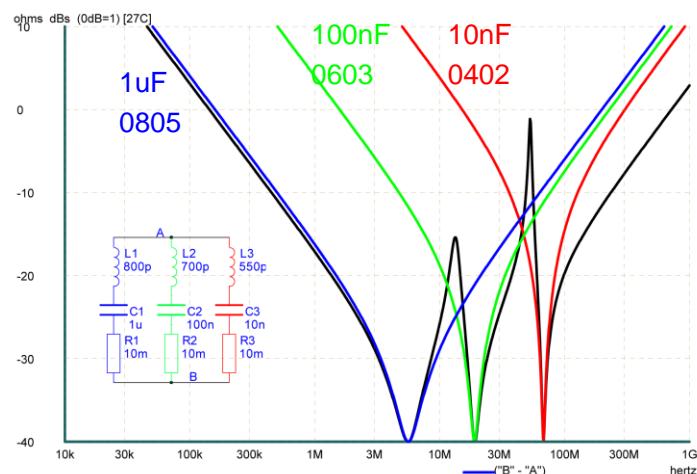
BEST



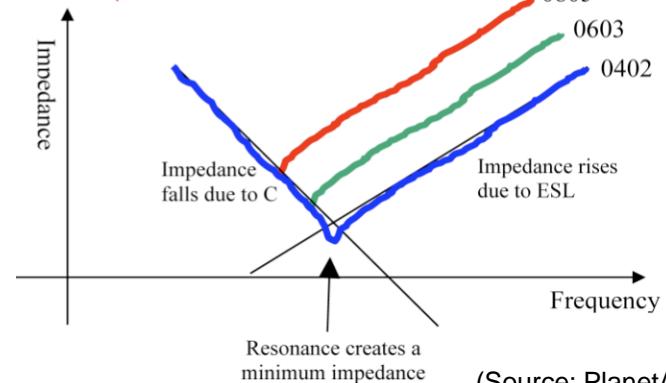
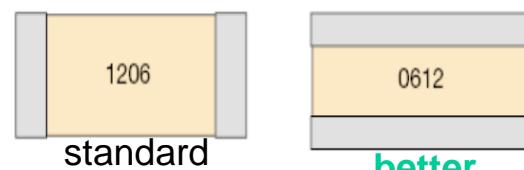
# Decoupling

## How to choose a decoupling capacitor

- use MLCC (multilayer ceramic) capacitors: X7R, Z5U:
  - low loss
  - compact size
- use the smallest possible SMD case
  - lower equivalent series inductance (ESL)
  - special cases with low ESL are available:
- commonly used values: 100nF, 10nF, 1nF



Ceramic (EIA Class II) Capacitor Code					
Letter Symbol	Low Temp. Requirement	Number Symbol	High Temp. Requirement	Letter Symbol	Max. ΔC over ΔT
Z	+10°C	2	+45°C	A	+/- 1.0%
		4	+65°C	B	+/- 1.5%
Y	-30°C	5	+85°C	C	+/- 2.2%
				D	+/- 3.3%
X	-55°C	6	+105°C	E	+/- 4.7%
		7	+125°C	F	+/- 7.5%
				P	+/- 10.0%
				R	+/- 15.0%
				S	+/- 22.0%
				T	+22% / -33%
				U	+22% / -56%
				V	+22% / -82%

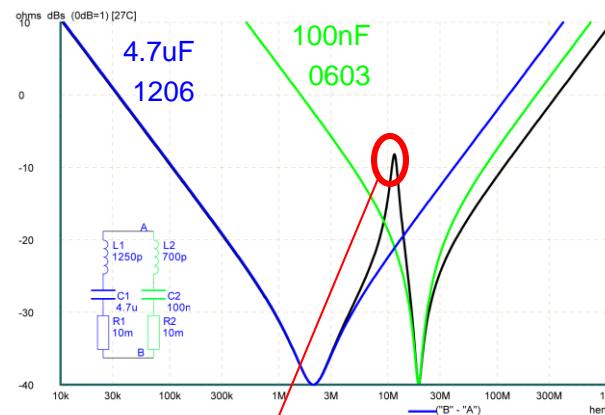


(Source: PlanetAnalog.com)

# Decoupling

## Paralleling decoupling capacitors

- the idea: above its  $\omega_{\text{res}}$ , a single capacitor has an increasing Z  
=> reduce this Z at higher frequencies with a smaller C in parallel



- the risk: parallel resonance: the equivalent circuit is now of 4<sup>th</sup> order and  $Z_{\text{TOT}}(\omega)$  has 2 zeros and 3 poles. Network theory says that they alternate on the frequency axis. Therefore, between the series resonance of each single capacitor we have a frequency where Z becomes **very high**.

# Parallel decoupling capacitors

## how to mitigate parallel resonance:

- use capacitors with higher ESR (or add a small series R): this extra loss adds more damping to the parallel resonance (less Q)
  - NPO and COG dielectrics (used in high frequency capacitors) have very low losses and are therefore not a good choice for decoupling
- when paralleling capacitors, use all capacitors of the same capacitance
- put a great number of capacitors in parallel, with closely spaced series resonance frequencies

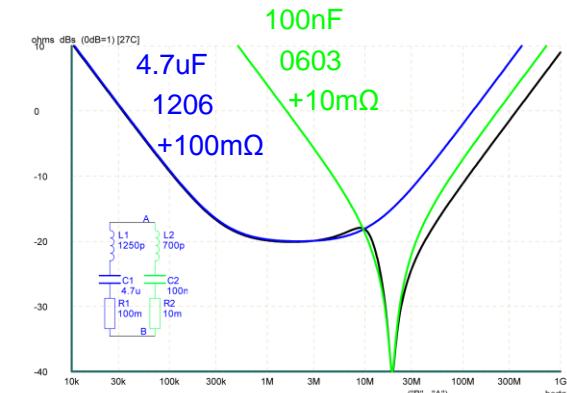


Figure 5L Example of using ten identical 10nF decaps in parallel  
(assuming they share the small power plane of a layout similar to Figure 5F)

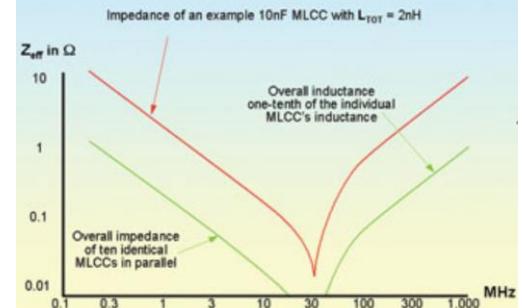
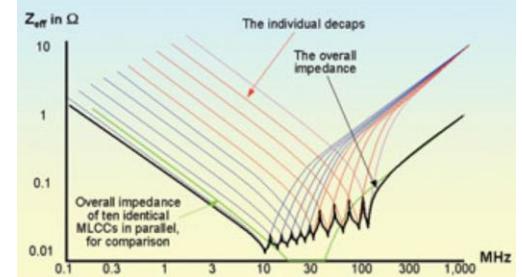


Figure 5N Example of ten parallel decaps with different values  
100, 56, 33, 27, 15, 10, 5.6, 3.3, 1.8 and 1nF, each with L<sub>TOT</sub> = 2nF  
(assuming they share the small power plane of a layout similar to Figure 5F)

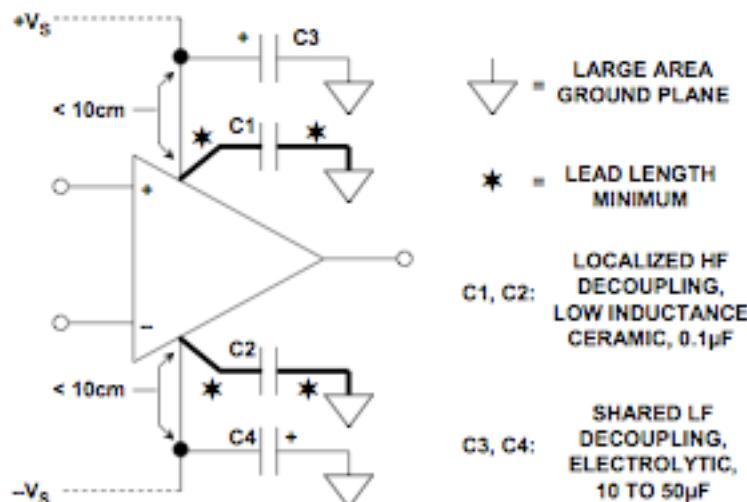


(Sources: PlanetAnalog and [5])

# Parallel decoupling capacitors

still recommended in analog circuits:

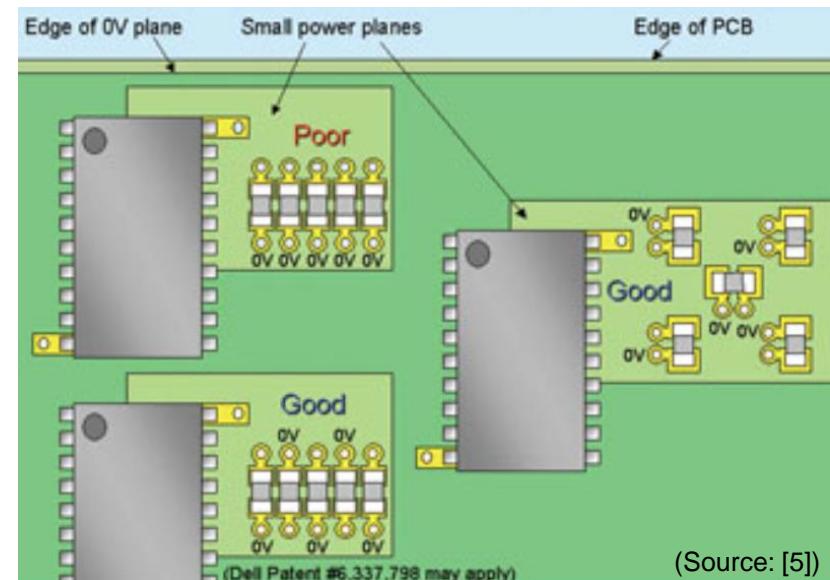
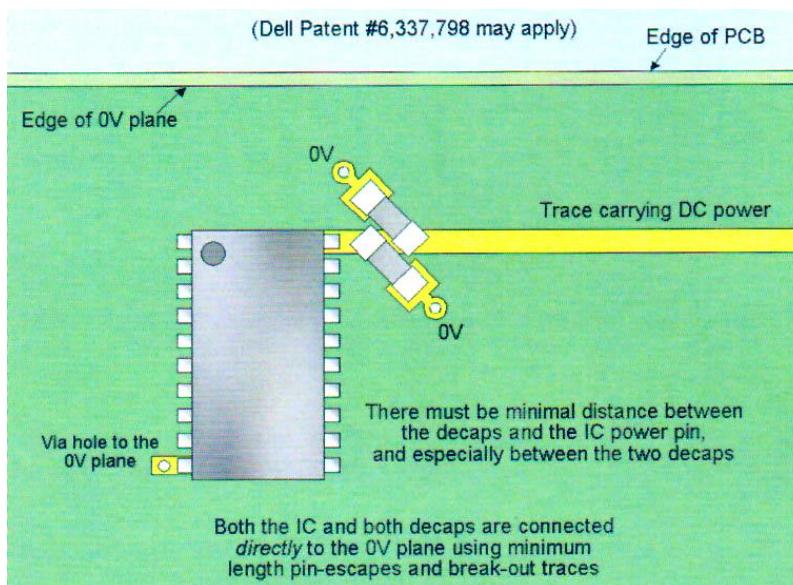
- circuits operating at frequencies below a few MHz are not affected by high frequency parallel resonances
- use the combination of:
  - a large C ( $10\mu F \dots 50\mu F$ ) to decouple noise introduced by the power supply (PSRR)
  - a smaller C ( $100nF$ ) as a return path for higher frequency noise generated by the IC is recommended by analog IC manufacturers [1]:



# Decoupling

## Parallel decoupling capacitor placement

- if possible, take advantage of magnetic flux cancellation that reduces ESL when placing multiple capacitors very close to each other with **opposite** current flow

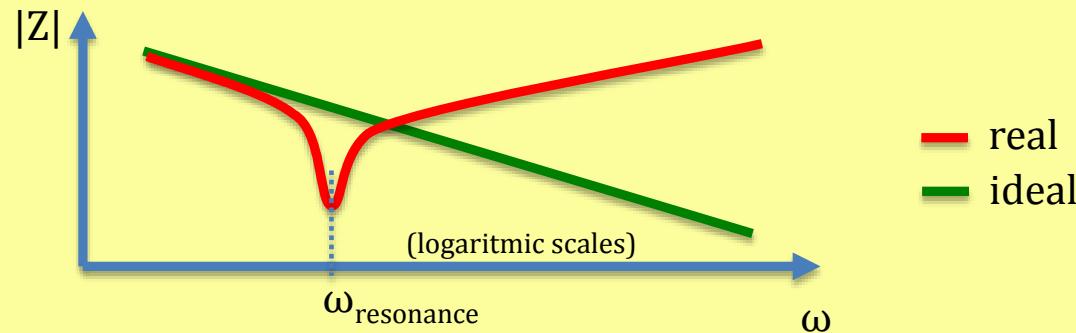


## Quiz time

1. Draw the frequency response  $Z(\omega)$  of:

- an ideal capacitor
- a real capacitor

Answer:



2. Explain the reason of this difference

Answer:

A real capacitor has parasitic elements, such as a series inductance and a series resistance. The capacitance and its series inductance form a resonant circuit. At the series resonance frequency,  $|Z|$  reaches its minimum value. At frequencies above the resonance, the impedance of the inductance prevails. Here the real capacitor acts as an inductor.

# Decoupling

## Intrinsic capacitance between GND and VCC planes of a PCB

- in multilayer PCBs, placing the VCC and GND planes adjacent and very close ( $d < 100\mu m$ ) produces a good intrinsic decoupling capacitance
- $C = \epsilon_0 \epsilon_r \frac{A}{d}$       (*example : FR4 with  $d = 100\mu m$   $\rightarrow C \approx 37 pF/cm^2$* )

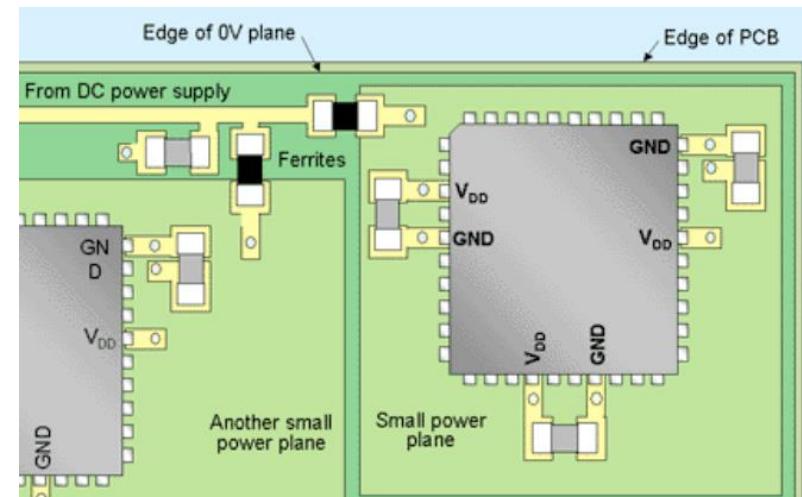
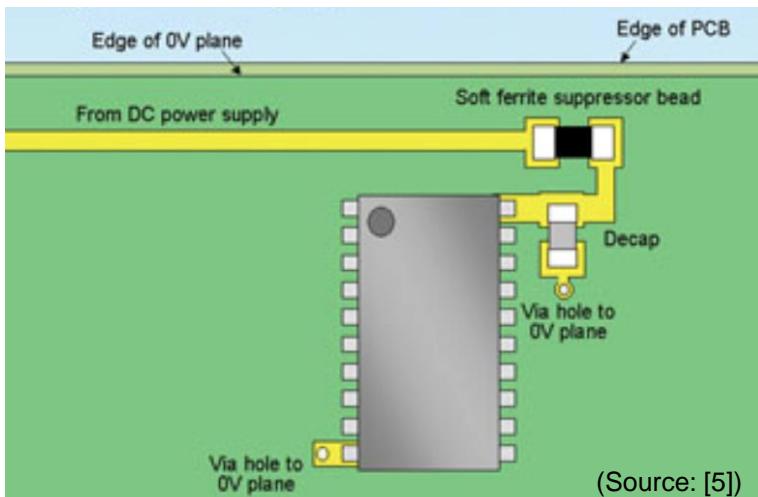
## Avoid the risk of resonance of the VCC-GND cavity

- reducing the distance between VCC and GND planes (modify stackup) reduces their cavity's Q
- resize the VCC area so that resonant frequencies along its length L and its width W do not overlap.  $\Rightarrow$  Choose  $L/W = \text{irrational number}$ .
- spread many decoupling capacitors all over the PCB (spaced at  $\leq \lambda/4$  of the highest frequency of concern)
- partition the VCC plane into smaller planes, connected through  $\pi$ -filters  
 $\Rightarrow$  shift plane resonance to higher (uncritical) frequencies
- if multiple reference planes of the same type (GND or VCC) exist, contact them with many vias (spaced at  $< \lambda/10$  of the highest frequency of concern)
- add some damping (R, series R-C or capacitors with higher ESR) between GND and VCC

# Decoupling

## Ferrite beads or RF suppressors on VCC

- can help further suppress VCC noise from ICs
- useful when VCC is already partitioned
- L or  $\pi$  filters can be implemented with ferrite beads
- T filters can be implemented with pass-through filters
- do not use normal inductors (resonant circuit!)





# Transmission lines

## A PCB trace is *not* an ideal conductor (1)

- a piece of PCB trace with a length  $z$  has a resistance:

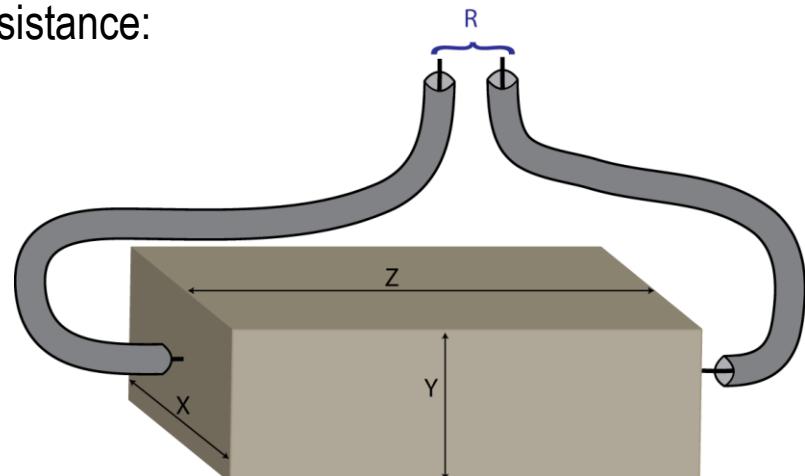
$$R = \rho \frac{Z}{X \cdot Y} \quad (\rho: \text{resistivity } [\Omega\text{m}])$$

- example:

$$Y = 35 \mu\text{m}, \quad X = 0.254 \text{ mm (10 mils)}$$

$$\rho = 0.0175 \Omega \frac{\text{mm}^2}{\text{m}} \quad (\text{copper})$$

$$\Rightarrow R = 19 \text{ m}\Omega/\text{cm}$$

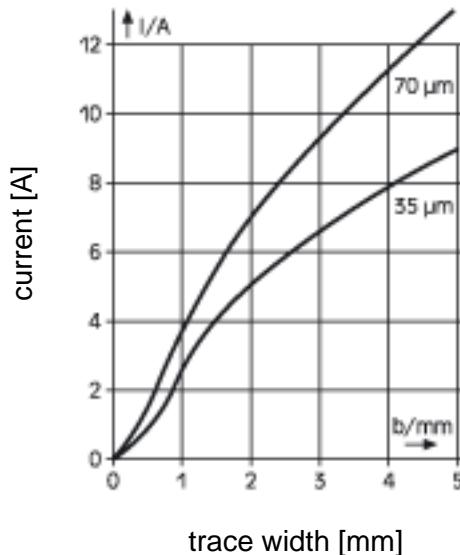


- when driving low impedance loads, the trace  $R$  forms with this load a resistive voltage divider. This can be critical for precision analog circuits.

# Transmission lines

## A PCB trace is *not* an ideal conductor (2)

- current flow produces a temperature rise. Trace widths must be dimensioned accordingly!
- **example:** typical recommended trace widths, for  $Y = 35\mu\text{m}$  and  $70 \mu\text{m}$ , for a max temperature rise of  $60^\circ\text{C}$



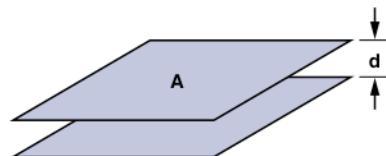
(Source: [www.db-electronic.com](http://www.db-electronic.com))

# Transmission lines

## Intrinsic capacitance *(already seen)*

- the capacitance formed by two copper areas on adjacent PCB layers is:

$$C = \epsilon_0 \epsilon_r \frac{A}{d} \quad (\text{example : FR4 with } d = 100\mu\text{m} \rightarrow C \approx 37 \text{ pF/cm}^2)$$



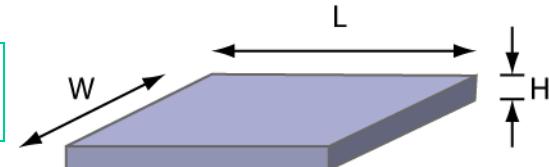
# Transmission lines

## Inductance

- a PCB trace has a self inductance L.

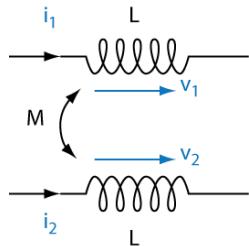
Approximate formula for a copper strip of length L *when no GND plane is present underneath:*

$$\text{inductance} = 0.0002L \left[ \ln \frac{2L}{W+H} + 0.2235 \left( \frac{W+H}{L} \right) + 0.5 \right] \quad (\text{in } [\mu\text{H}])$$



- two parallel PCB traces have a mutual inductance M.

This is the case for a signal trace and its return path in the adjacent GND layer



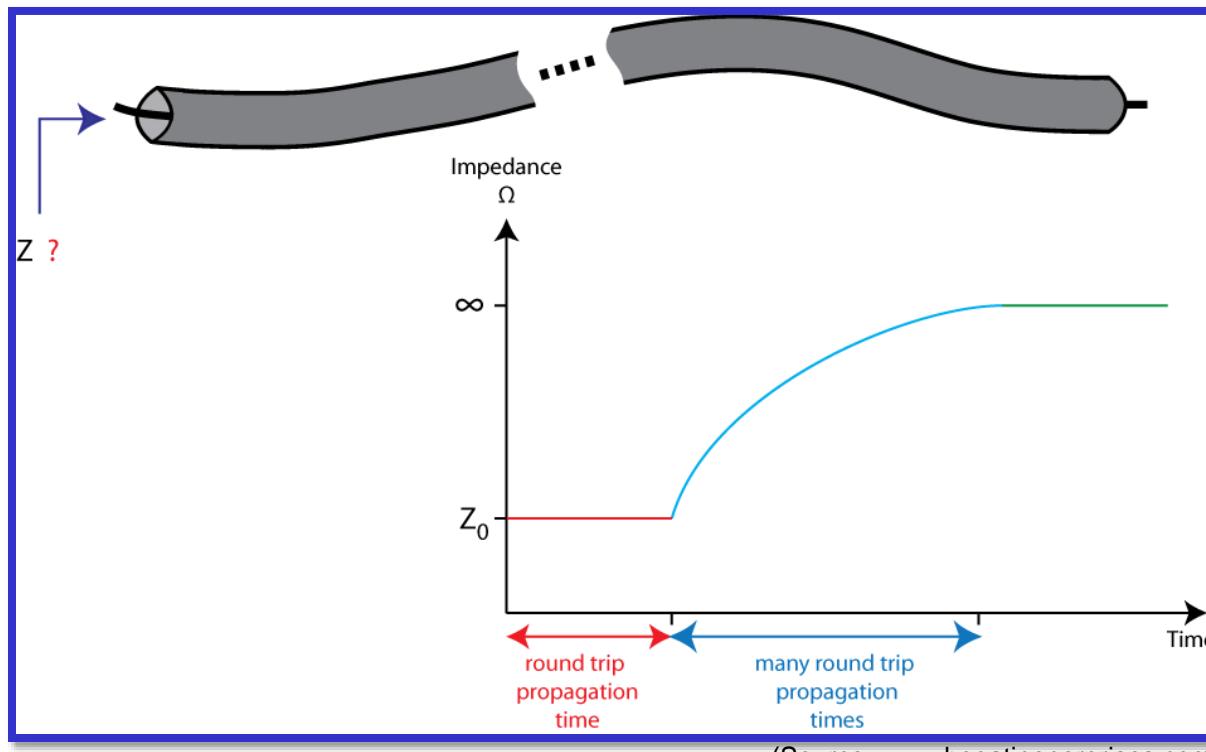
$$\begin{aligned} V_1 &= L \frac{di_1}{dt} + M \frac{di_2}{dt} \\ V_2 &= L \frac{di_2}{dt} + M \frac{di_1}{dt} \end{aligned}$$

- if  $i_1 = -i_2$  then  $V_1 = -V_2 = (L - M) \frac{di}{dt}$ . The term  $(L - M)$  is called **mutual partial inductance**.
- if the mutual coupling is good (reference plane carrying the return current is very close to the signal trace) then  $(L - M)$  is very small and  $\Delta V$  due to inductance is very small.
- this is **another good reason** for using continuous reference planes adjacent to each signal plane!

# Transmission lines

**What is the characteristic impedance  $Z_0$  of a transmission line?**

- it is the impedance measured at one end of the line before the signal makes a round trip in the line
- if the line's length is  $\infty$  we will measure  $Z_0$  forever

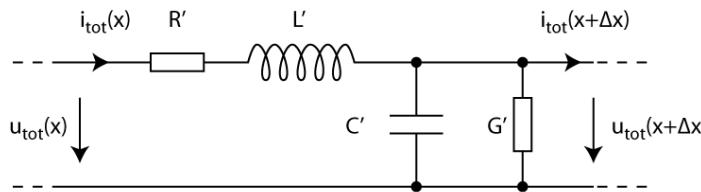


(Source: [www.bogatinenerprises.com](http://www.bogatinenerprises.com))

# Transmission lines

## Every PCB trace is a transmission line (1)

- equivalent schematic:



( $R'$ ,  $L'$ ,  $C'$  and  $G'$  are the values per unit length)

- the differential equations for  $u_{tot}(x)$ ,  $i_{tot}(x)$ ,  $u_{tot}(x+\Delta x)$ ,  $i_{tot}(x+\Delta x)$  are called "Telegrapher's equations"
- Their solution results in two signals that can propagate in the two directions:  
 $\rightarrow (u_a, i_a)$  and  $\leftarrow (u_b, i_b)$ .  
(e.g.: *forward and reflected signal*)  
For each one, the relationship between  $u$  and  $i$  is:

$$\frac{|u_a|}{|i_a|} = \frac{|u_b|}{|i_b|} = Z_0$$

# Transmission lines

## Every PCB trace is a transmission line (2)

- Important properties:

$$\text{Characteristic impedance : } Z_0 \approx \sqrt{\frac{L'}{C'}}$$

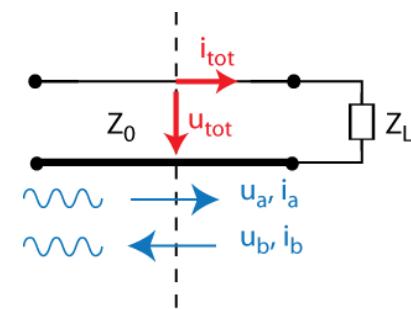
$$\text{Propagation velocity : } v_{ph} = \frac{c}{\sqrt{\epsilon_r \mu_r}} \approx \frac{1}{\sqrt{L' C'}}$$

- when a signal is sent into a transmission line, and before the reflected signal returns we see only  $u_a, i_a$ .
- $Z_0$  is the impedance that we would measure at the beginning of a line with length  $\infty$  or more in general, when no reflected signal  $\leftarrow$  exists ( $u_b, i_b = 0$ )
- in order to avoid reflections at the end of a transmission line, the load impedance  $Z_L$  must be equal to the line's  $Z_0$

- at any point in the line, we know that:

$$u_b(x) = u_a(x) + u_s(x)$$

$$i_b(x) = i_a(x) - i_s(x)$$





# Transmission lines

## Signal reflection (1)

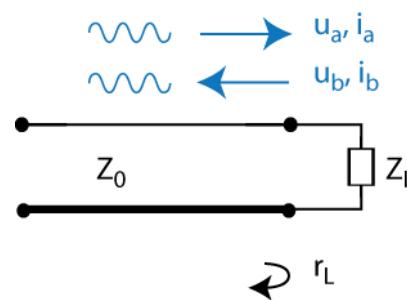
- When  $Z_L \neq Z_0$  we have a reflection.
- We define the reflection coefficient  $r$ :

$$r_{(complex)} = \frac{u_b}{u_a}$$

- Relationship between  $Z_L$ ,  $Z_0$  and  $r$ :

$$r_L = \frac{Z_L - Z_0}{Z_L + Z_0}$$

$$\underline{Z}_L = Z_0 \frac{1 + r_L}{1 - r_L}$$



## Quiz time

**3. Calculate the reflection factor at the end of a  $100\Omega$  line terminated with a  $1\text{k}\Omega$  load**

*Answer:*

$$r = \frac{Z_L - Z_0}{Z_L + Z_0}$$

*with  $Z_0 = 100\Omega$  and  $Z_L = 1\text{k}\Omega$  we have :*

$$r = \frac{1000 - 100}{1000 + 100} = \frac{900}{1100} = 0.82 \text{ (real)}$$

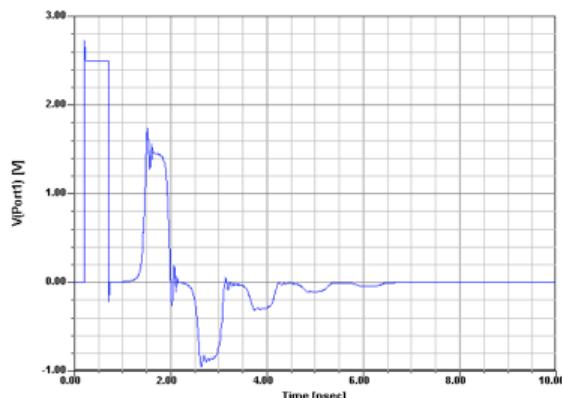
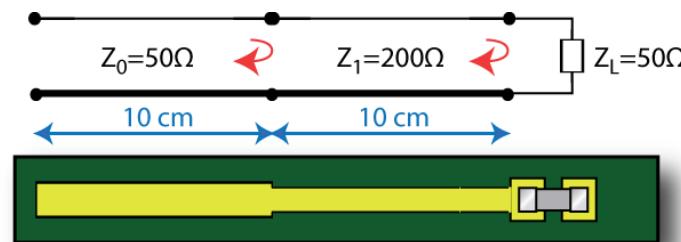
# Transmission lines

## Signal reflection (2)

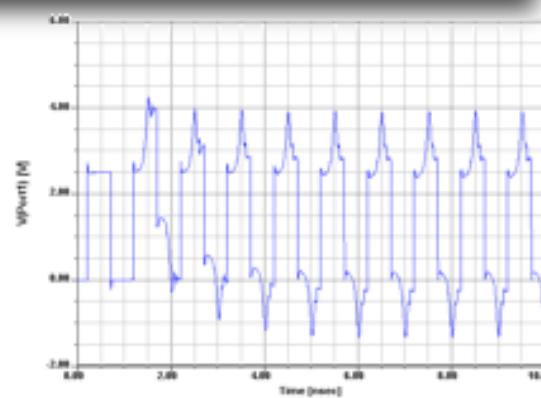
- A junction between two transmission lines with different characteristic impedances also generates reflections:
- Examples of signal reflections seen **here**:



$$r_{junction} = \frac{Z_1 - Z_0}{Z_1 + Z_0}$$



single 0.5 ns pulse



square wave with 0.5 ns pulses

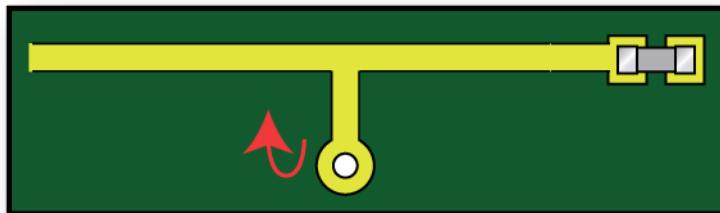
- Be careful with trace width changes, connectors, etc!

(Source: [22])

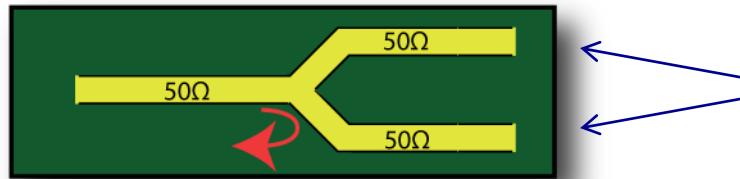
# Transmission lines

## Traces, stubs and splits

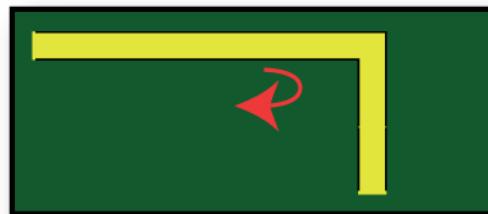
- An unloaded ( $Z=\infty$ ) trace generates reflections ( $r = +1$ ):



- Splitting a trace in two (or more) can generate reflections:



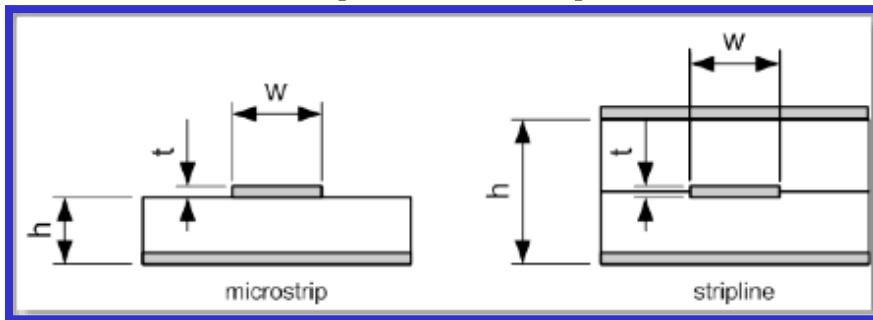
- Sharp corners generate reflections:



(Source: [22])

# Transmission lines

## Microstrip and stripline



typical values $Z_0$ :	$w=3, h=1.6$ [mm]	$w=0.65, h=1.6$ [mm]
Microstrip (in FR4)	50 Ω	98 Ω
Stripline (in FR4)	<20 Ω	50 Ω

- Microstrip: a signal trace runs over a continuous GND plane:

$$Z_0 \approx \frac{87}{\sqrt{\epsilon_r + 1.41}} \cdot \ln\left(\frac{5.98h}{0.8w + t}\right) \quad [\Omega]$$

$$v_{ph} \approx \frac{1}{1.017\sqrt{0.457 \cdot \epsilon_r + 0.67}} \quad [ft/ns]$$

- Stripline: a signal trace is "sandwiched" between two GND planes:

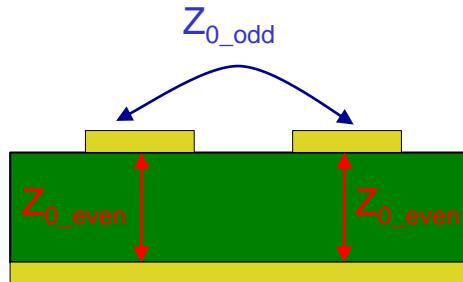
$$Z_0 \approx \frac{60}{\sqrt{\epsilon_r}} \cdot \ln\left(\frac{4h}{0.67\pi w \cdot \left(0.8 + \frac{t}{w}\right)}\right) \quad [\Omega]$$

$$v_{ph} \approx \frac{1}{1.017 \cdot \sqrt{\epsilon_r}} \quad [ft/ns]$$

(Source: [22])

# Transmission lines

## Differential lines



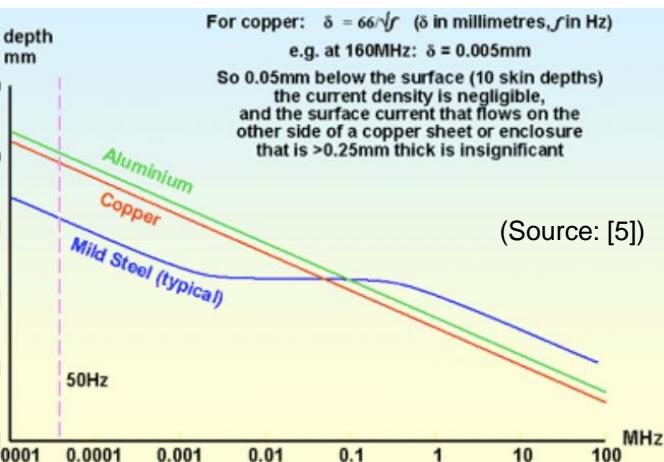
- Actually we can have two different  $Z_0$ 's, depending on how the two traces are driven: common mode or differential mode
- Example
  - $Z_{0\_even}$  is for common mode signals: the value is similar to that of a single microstrip line and is independent from the distance between the traces
  - $Z_{0\_odd}$  is for differential mode signals. Its value increases with increasing distance between the two traces
- Example:  $Z_{0\_even} = 50 \Omega$ ,  $Z_{0\_odd} = 100 \Omega$
- use numeric simulation tools to determine the two  $Z_0$ 's

# Transmission lines

## Skin effect

- As a consequence of Maxwell's equations, AC current tends to distribute on the outer region of a conductor.
- Def: skin depth  $\delta$  is the depth into the conductor by which the current density has decreased to  $1/e$  of what it was ( $\sim 37\%$ )

$$\delta = \sqrt{\frac{2}{\omega \mu_0 \mu_r \sigma}}$$



where:

$\omega$ : frequency ( $2\pi f$ )

$\mu_0, \mu_r$ : permeability

$\sigma$ : conductivity [ $\Omega^{-1}\text{m}^{-1}$ ] ( $=5.82 \times 10^7$  for copper)

- since the AC current uses a smaller conductor section,  $R$  increases due to the skin effect:

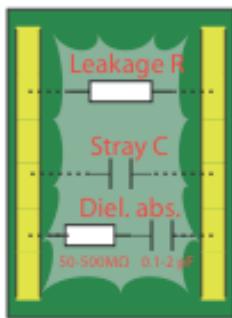
$$R \sim \sqrt{\omega}$$

- Example:

f	1 kHz	1 MHz	10 MHz	100 MHz
$\delta[\text{mm}]$	2.1	0.06	0.02	0.006

# Parasitic PCB effects

*...depend from PCB materials, environmental factors (humidity, dirt, salts),  
PCB layout and assembly*



## Static (affect DC operation of the circuit)

- Leakage resistance
  - even a 10nA leakage current can disrupt operation of a high impedance analog circuit

## Dynamic (affect AC operation of the circuit)

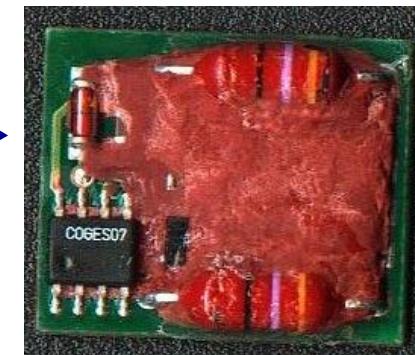
- Stray capacitance (between traces, component cases and leads)
  - can "detune" precision filters or oscillators
- Dielectric absorption (same as in capacitors, 0.1-2.0pF in series with 50-500MΩ)
  - can affect circuit settling time, S/H circuits, active filters
- High frequency losses
  - can affect high-Q circuit and produce signal attenuations



# Parasitic PCB effects

## Workarounds

- PCB layout
- component mounting (THT leads folding)
- PCB and components coating (resin) →  
against atmospheric agents



- use of superior PCB materials (alumina, Rogers<sup>©</sup>, Taconic<sup>©</sup>, Arlon<sup>©</sup>) [...Link](#)
- guard rings

## Quiz time

### 4. Resistive losses on a conductor

- do not change with frequency
- are higher at higher frequencies
- are higher at lower frequencies

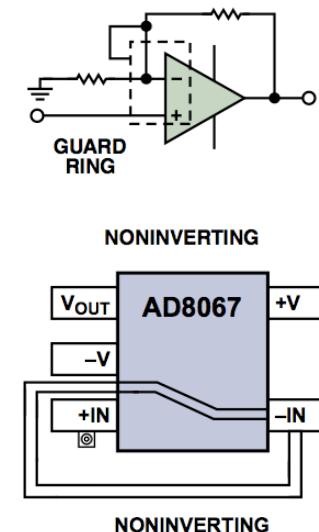
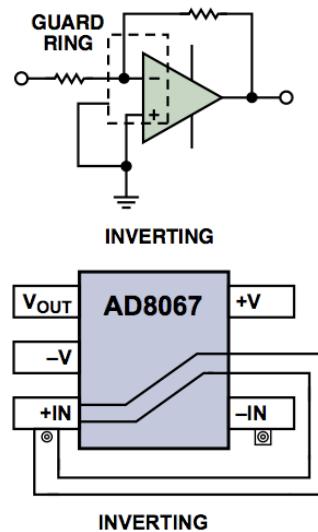
### 5. A stub is ...

- a test point
- a connector
- an unterminated transmission line
- a branch transmission line

# Parasitic PCB effects

## Guard rings against parasitic effects (analog circuits)

- *the idea:* Completely surround sensitive nodes with conductors that can readily sink stray currents, and maintain the guard conductors at the exact potential of the sensitive node
- *example* Inverting amplifier
- *example* Non-inverting amplifier



- in THT circuits, repeat the guard ring on *all* layers
- *never* leave guard rings *floating*!

(Source: [1], [2])



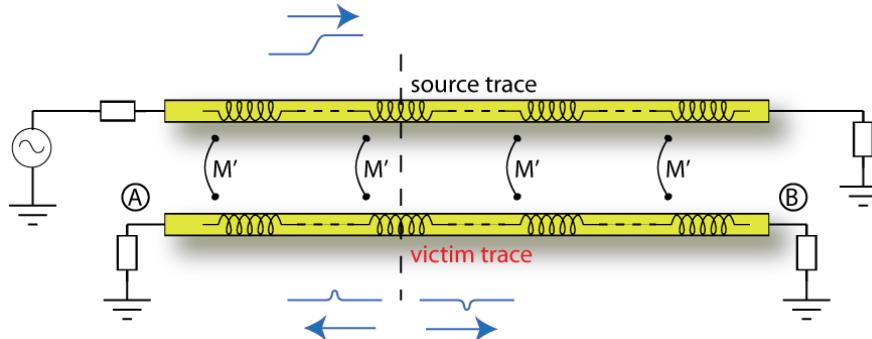
# Crosstalk

## What is it?

- Crosstalk is the unintended interference between nearby signal traces
- There are several reasons for crosstalk between two (or more) signal traces:
  - inductive coupling
  - capacitive coupling
  - sharing of a common signal return path with non-zero impedance

# Crosstalk

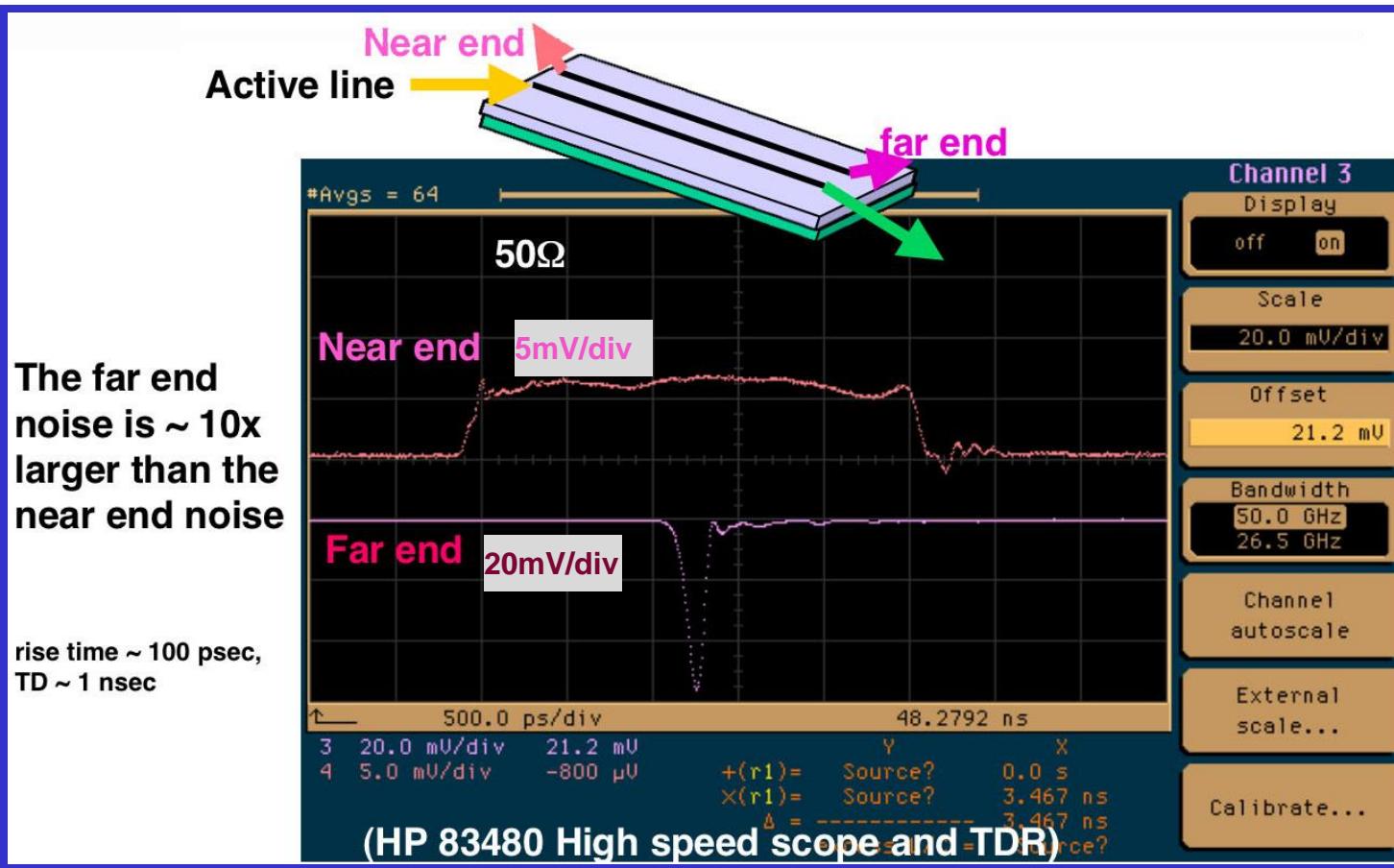
## Inductive coupling



- the magnetic field lines generated by the source trace induce a voltage on the victim trace
- $u_{victim} = M \frac{di_{source}}{dt}$
- on the victim trace, the coupled signal propagates in both directions with opposite polarity
- in the victim trace, the "pulses" contributed by each single coupling point arrive at the same time at the far end (B), while they arrive at different times at the near end (A).
- therefore, in B we see a sharp pulse with strong amplitude, whereas in A we see a broad pulse

# Crosstalk

## Inductive coupling



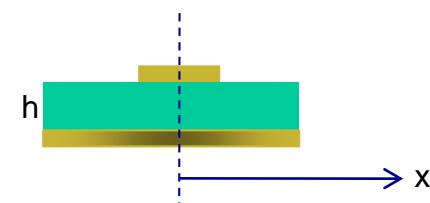
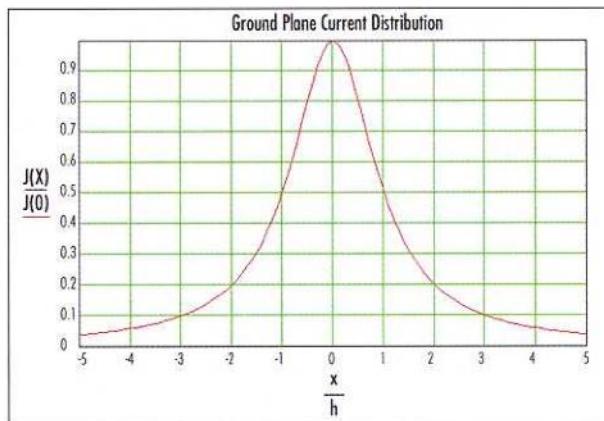
(Source: Agilent)

# Crosstalk

## Inductive coupling – estimation of the inductive crosstalk

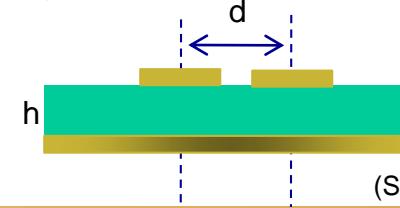
- we have seen (*Image Planes*) that the current distribution in the GND layer underneath a signal trace has the following distribution:

$$J(x) = \frac{I_0}{\pi h} \cdot \frac{1}{1 + \left(\frac{x}{h}\right)^2}$$



- The magnetic field decreases accordingly, therefore, for a parallel trace at distance  $d$  we can expect that the inductive cross coupling is proportional to:

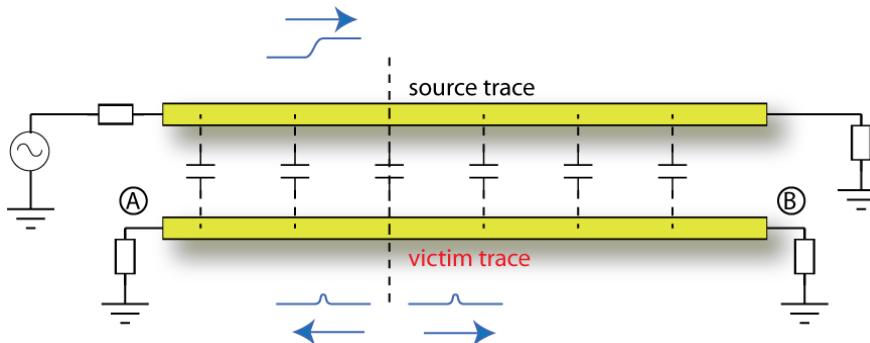
$$\frac{1}{1 + \left(\frac{d}{h}\right)^2}$$



(Source: [6], [19])

# Crosstalk

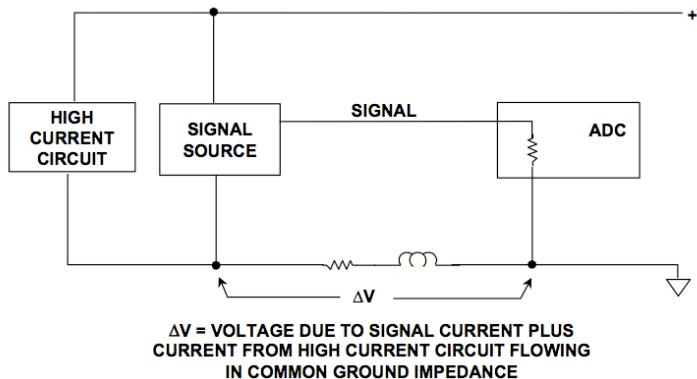
## Capacitive coupling



- on the victim trace, the coupled signal propagates in both directions with the same polarity
- in the victim trace, the "pulses" contributed by each single coupling point arrive at the same time at the far end (B), while they arrive at different times at the near end (A).
- therefore, in B we see a sharp pulse with strong amplitude, whereas in A we see a broad pulse
- when a solid reference plane is present, inductive and capacitive crosstalk voltages are roughly of the same amplitude. Therefore, at the far end they tend to cancel (opposite polarity) and at the near end they add up
- we must provide good termination in A to avoid that the coupled signal gets reflected back into the victim trace
- when a solid reference plane is missing, inductive crosstalk prevails

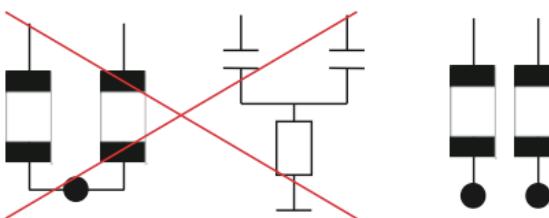
# Crosstalk

**Crosstalk due to a common signal return path with non-zero impedance**



- ground noise (e.g. from high speed logic) can translate to output voltage noise of other circuits if they share a common return path with  $Z \neq 0$
- => use uninterrupted GND planes!
- => avoid sharing the same GND via by more than one component

( $C_{\text{decoupling}}$ , IC GND, etc)





# Crosstalk

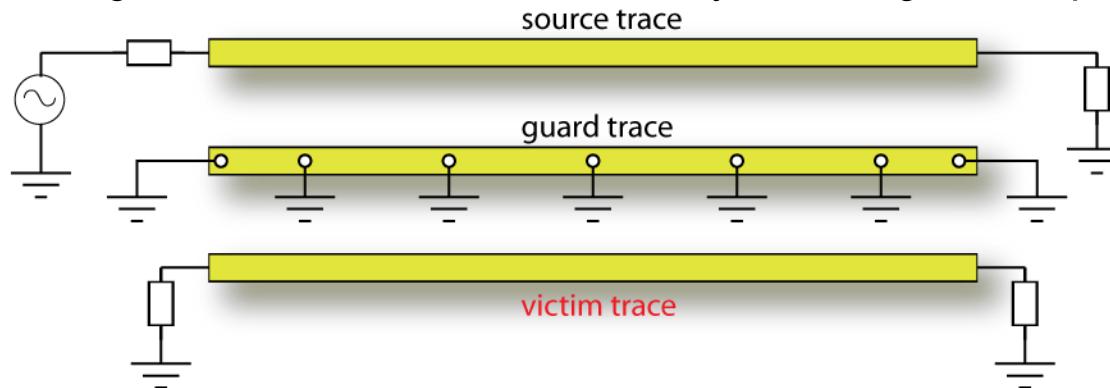
## How to reduce it:

- do not run traces parallel over long distances
- minimize the length of all interconnects
- use a continuous reference plane adjacent to each signal layer (reduce coupling between signal layers and reduce impedance of the signal return path)
- reduce the number of layer changes and reduce the impedance of traces
- use the slowest possible signal edges (choice of the logic family)
- provide proper termination of the signal traces at both ends
- use differential signaling
- use lower signaling voltage (e.g. LVDS)
- in connectors, add a separate return (GND) pin for every signal
- use stripline technology for very critical nets (e.g. high speed clocks)
- use guard traces

# Crosstalk

## Guard traces to reduce crosstalk:

- may be useful to reduce **inductive coupling** as currents induced in the guard trace tend to compensate the magnetic field generated by the source trace
- this technique was seen more frequently on 2-layer PCBs without GND plane
- however in multilayer PCBs, compared to the effectiveness of a continuous reference plane adjacent (at a short distance) to every signal plane, a guard trace adds little benefit against inductive coupling.
- a grounded guard trace can act as a faraday shield against capacitive coupling



- **never** leave a guard trace floating!

## Quiz time

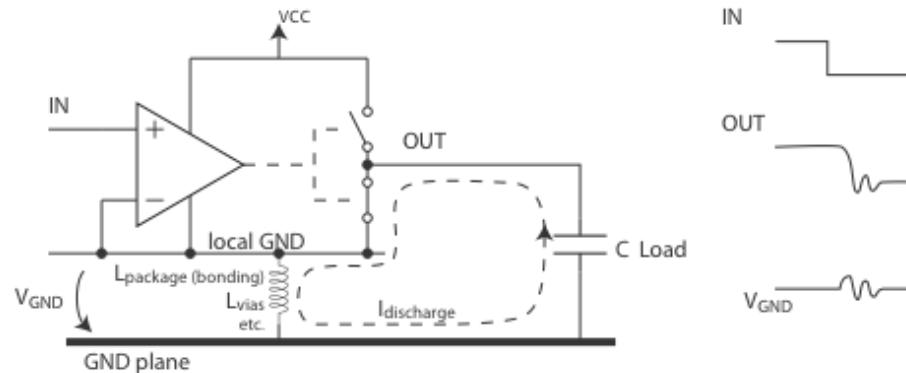
### 6. The inductive crosstalk between two adjacent signal traces

- increases with the distance
- decreases with the square of the distance
- decreases with the distance
- other

# Ground bounce

is a similar problem and can be the origin of crosstalk:

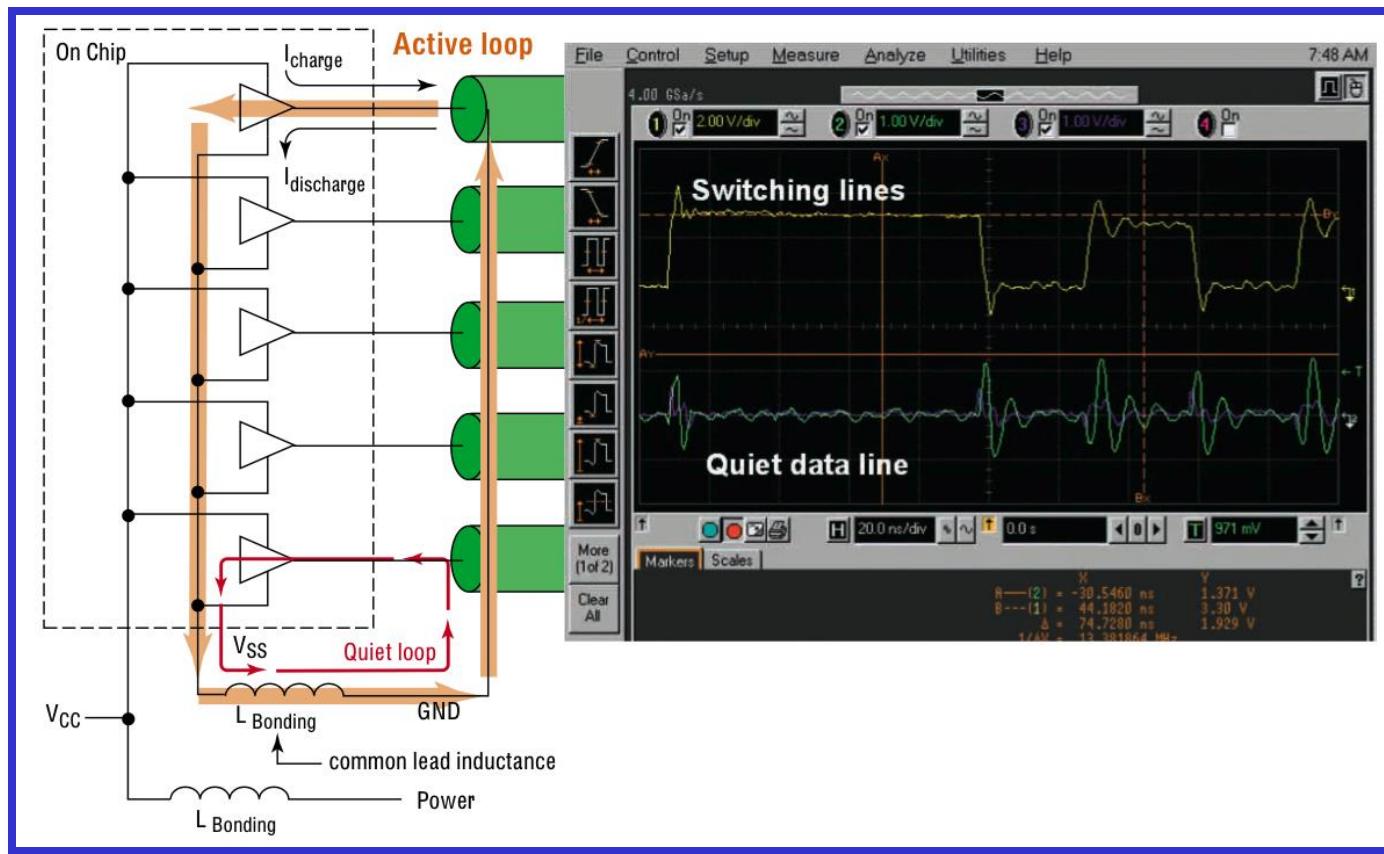
- single gate:



- multiple output drivers, input buffers sharing the same "local GND":
  - **outputs** that should not change show "ground bounces" when other outputs switch
  - **input** buffers see a input change due to ground bounce, even if the input signal is not changing (critical for clock circuits!)
  - the problem can extend to multiple ICs, if they share the same local GND or the same via to the main GND plane, etc.

# Ground bounce

Ground bounce and crosstalk in action:



(Source: Agilent)

# Ground bounce

## How to reduce it:

- reduce output slew rate, use slower logic family or one with slew rate control
- use IC cases with smaller L (SMD, BGA) and more GND pins
- do not share the same via to connect multiple ICs to the GND plane
- reduce impedance of connections to the GND plane (e.g. multiple vias)



# Differential signaling

**advantages from the signal integrity point of view:**

- can tolerate much common mode noise (if noise affects equally both lines of a differential pair, it cancels completely in the differential receiver)
- are insensitive to GND noise and non-zero GND impedance
- they have a controlled impedance, which facilitates finding an adequate termination (reduction of signal reflections)
- they generate less emissions (noise) in case of a non optimal (continuous) GND plane, because current return path is not travelling through GND.
- the same noise margin can be achieved with half the voltage swing of a single ended signaling solution (better immunity / less emissions)
- **do not** run a trace very close to a differential pair, as this could unbalance the pair and void some of its advantages!

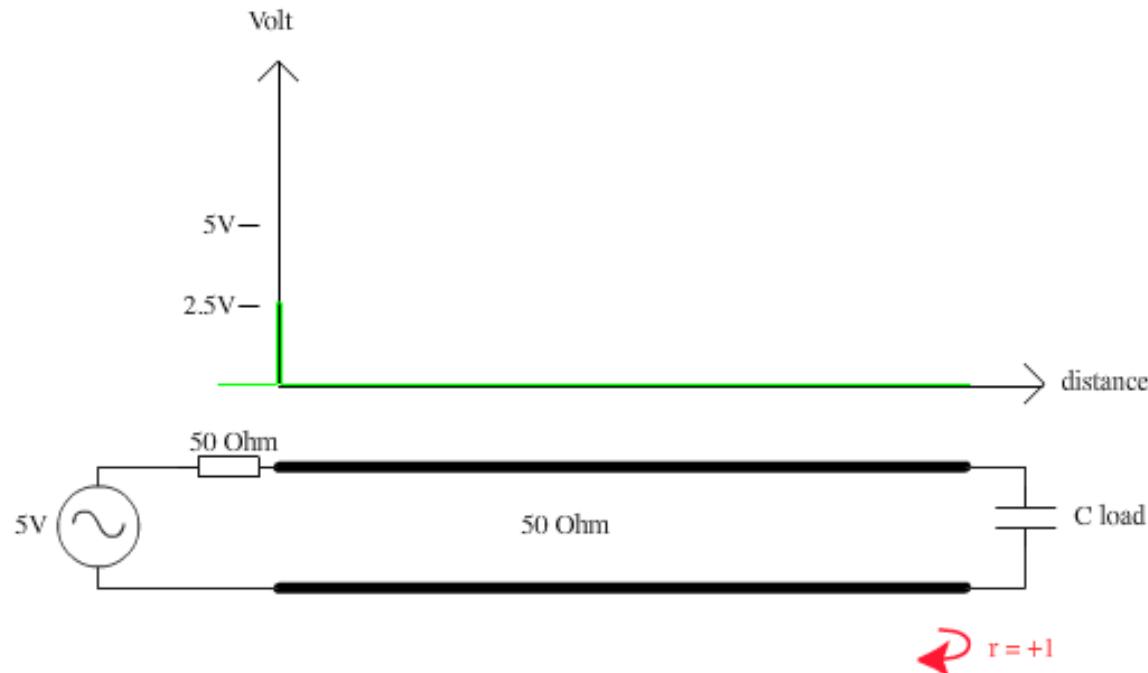
# Transmission lines

## Terminations

- **the purpose:** provide a load impedance at the end of a transmission line that is equal to its  $Z_0$ , as this will result in **no reflections ( $r = 0$ )**  
(signal reflections can severely compromise the functionality in digital systems)
- extend the possibility to use fast signal rise/fall times also on longer connections
- types of termination:
  - series
  - parallel (including Thevenin)

# Transmission lines

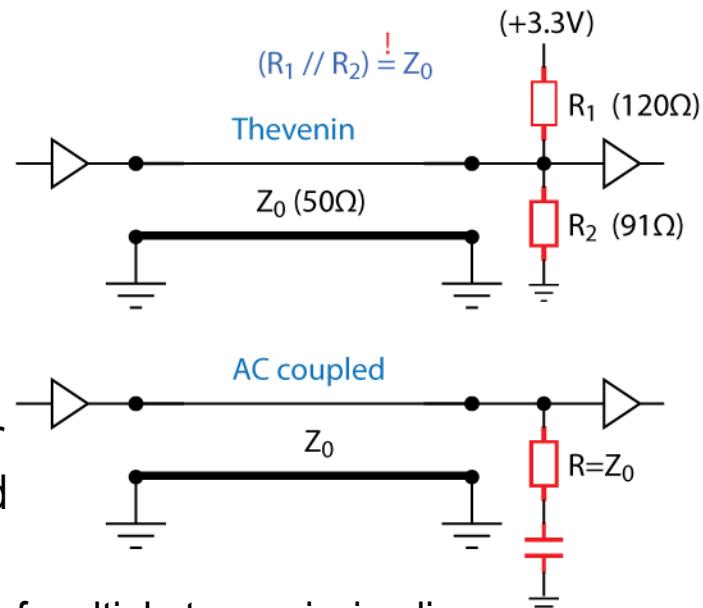
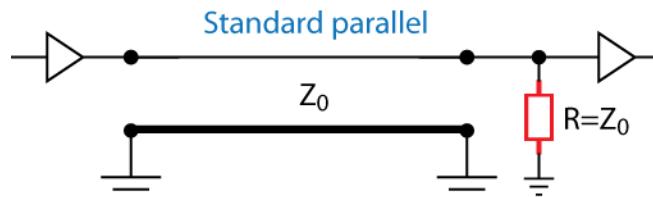
## Series termination explained



(Source: [22])

# Transmission lines

## Parallel terminations

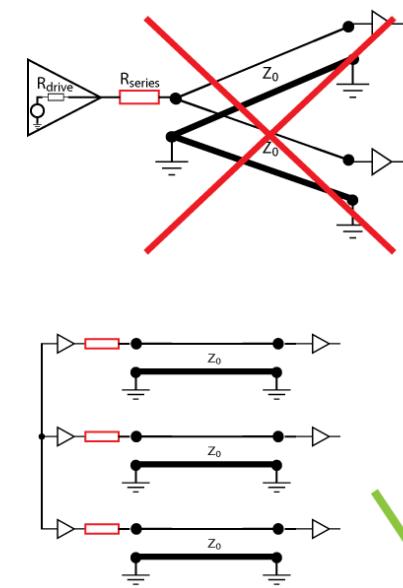
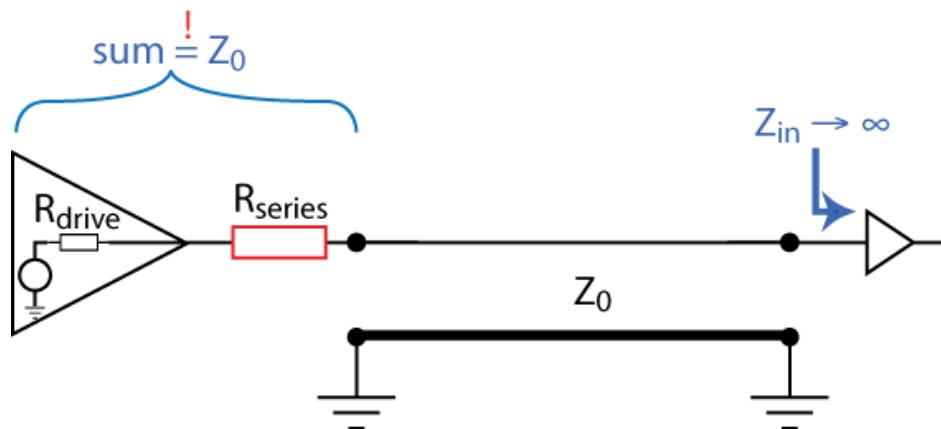


- Thevenin termination: choose  $R_1$ ,  $R_2$  so that their center point voltage is halfway from logic high and low levels
- beware from crosstalk in the terminating network of multiple transmission lines:
  - keep resistors at adequate distance
  - do not share GND vias for multiple termination networks
- place termination network *after* the *last* receiver IC
- place terminations at both ends if the line is bidirectional
- can be used for multidrop bus topologies (e.g. RS485)
- disadvantage: static power consumption (except for "AC coupled" version and in reduced extent in "Thevenin" version)
- disadvantage: reduced noise margin if driver can not source all the required current

# Transmission lines

## Series terminations

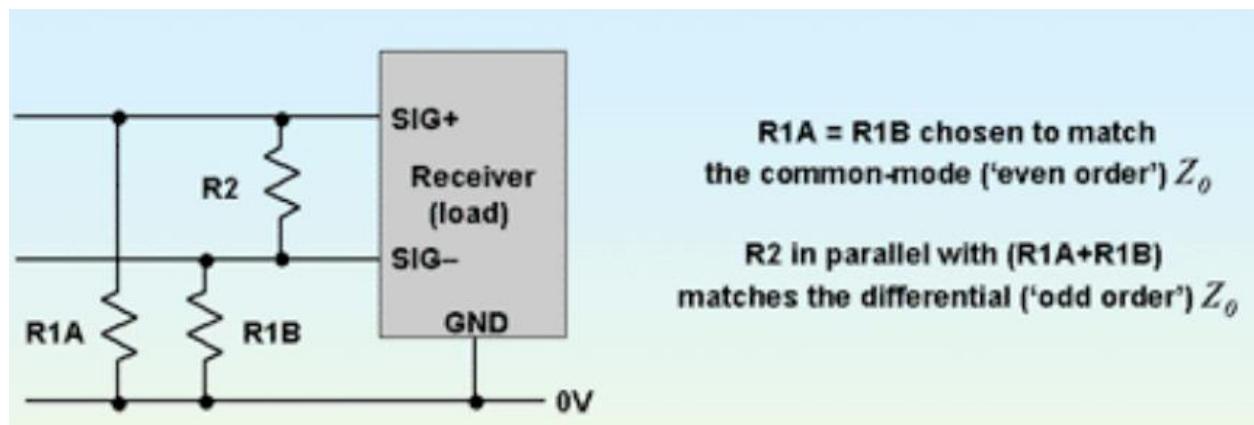
- for point-to-point (1 driver – 1 receiver) connections only
- low power dissipation
- for loads with high  $Z$  only (e.g. CMOS inputs)
- driver IC should have same  $R_{drive}$  for  $V_{OH}$  and  $V_{OL}$
- slightly reduces signal slew rate, at the benefit of better signal integrity
- place  $R_{series}$  very close to the driver IC
- place a series termination at both ends of the line, if it is a bidirectional one



# Transmission lines

## Terminations for differential lines

- Remember?: Differential lines actually have two types of  $Z_0$ :  $Z_{0\_even}$  and  $Z_{0\_odd}$
- We should try to terminate both of them (even in case of a pure differential signal, due to parasitic effects etc we are likely to have some common mode voltage)
- Example of parallel termination ([5]):



## Quiz time

### 7. What is ground bounce and how can it be reduced?

Answer:

Ground bounce happens when an IC with a non ideal (non zero impedance) connection to GND draws a high current spike, for instance when switching a capacitive load. When flowing through the non ideal GND connection of the IC, this current produces a voltage drop here. The "internal" GND of the IC experiences a voltage shift which can be observed also on other outputs that should stay quiet. Both the impedance of a via and that of the IC's internal bonding can contribute to this effect.

### 8. A series termination is obtained with:

- a series resistor at the end of the line
- a series resistor at the beginning of the line
- a resistive voltage divider at the end of the line



# Transmission lines

## When do transmission line effects become important

(crosstalk, signal reflections, need for terminations, etc)

Remember

- rule of thumb: transmission line effects must be taken into consideration if the round trip ( $\Rightarrow$ ) propagation time over a line exceeds the signal's rise/fall time
- Typical values:

Logic family	Rise / Fall time approx.	is transmission line starting from ..
74HC	13-15 ns	117 cm
74LS	9.5 ns	85.5 cm
74ALS	2-10 ns	18 cm
74ACT	2-5 ns	18 cm
74F	1.5 ns	10.5 cm
CPLD/FPGA	0.5 ns	< 5 cm

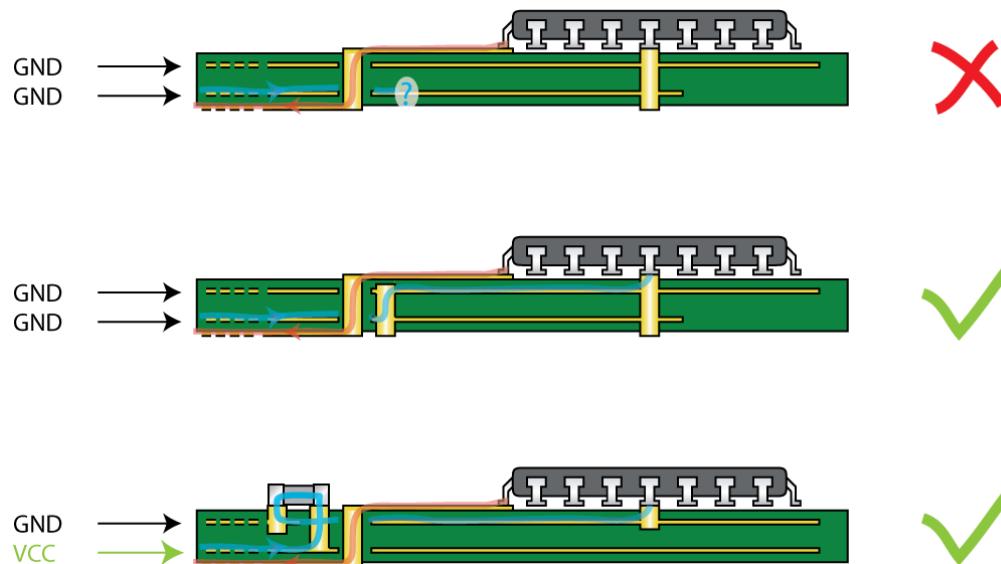
(assuming: microstrip, FR4 ( $\epsilon_r = 4.6$ ), 0.36 ns/cm propag. speed)

(Source: [11])

# Transmission lines

## Vias

- Rule #1: try to avoid changing layer with high speed signals whenever possible
- Rule #2: if a via can't be avoided, don't forget to assure an uninterrupted return path
- A via represents a discontinuity in the transmission line (capacitance to GND/VCC planes it crosses, series inductance) and can be a source of concern



# Clock distribution

- Clock nets are usually carrying high frequency signals. Therefore, transmission line effects arise. It is important to apply all the precautions already seen against signal reflections, ringing, crosstalk, etc.

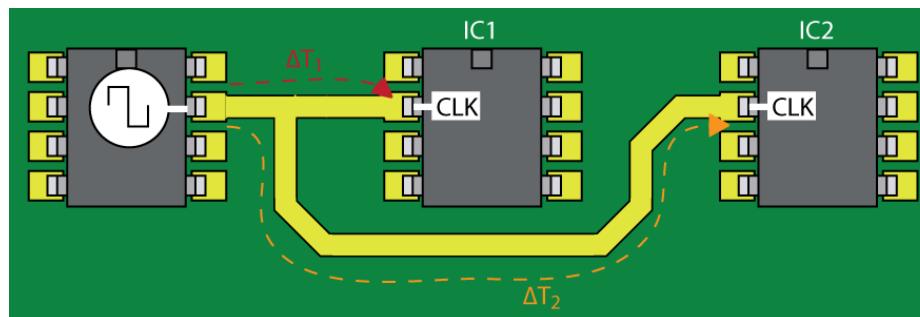
*In the next slides we will deal with some special issues related to clock distribution:*

- **Clock skew**
- **Clock jitter**

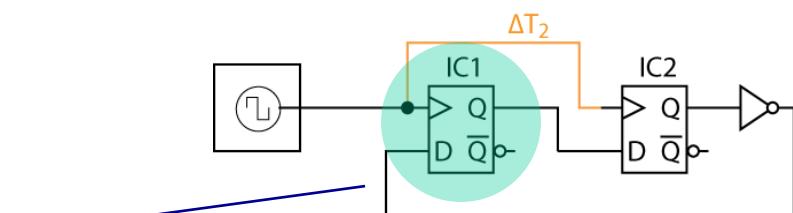
# Clock distribution

## Clock skew

- ... refers to a situation where the clock signal to a synchronous logic circuit does not arrive at the same time to all IC's clock inputs



- Example:

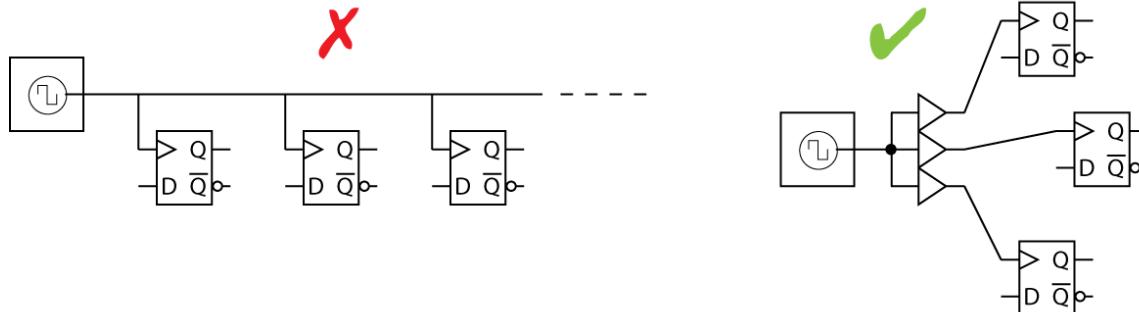


$$t_{SU(CLK)} = T_{CLK} - \Delta T_2 - t_{CKQV(FF)} - t_{P(BUF)}$$

# Clock distribution

## Clock skew – how to prevent it:

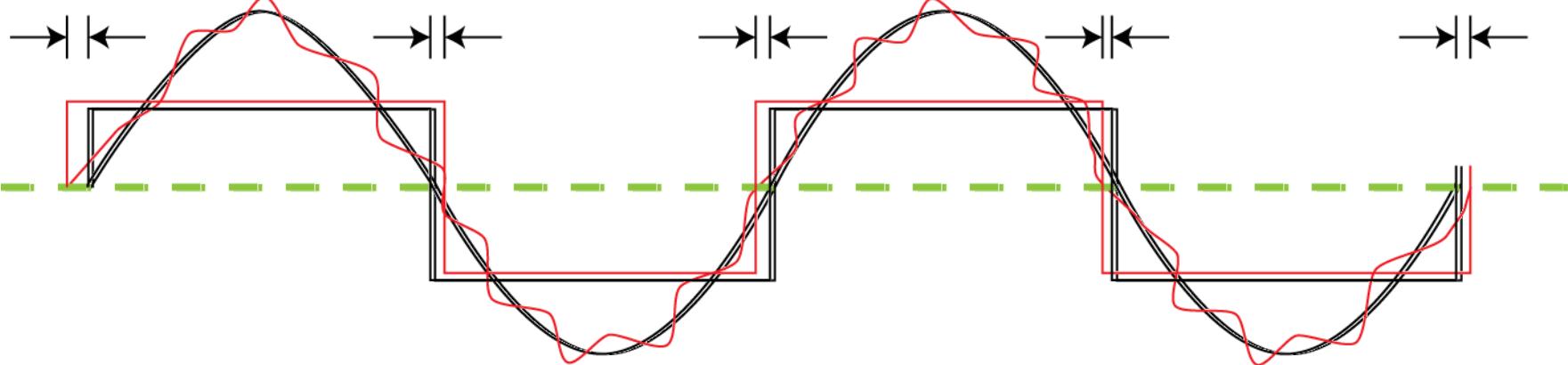
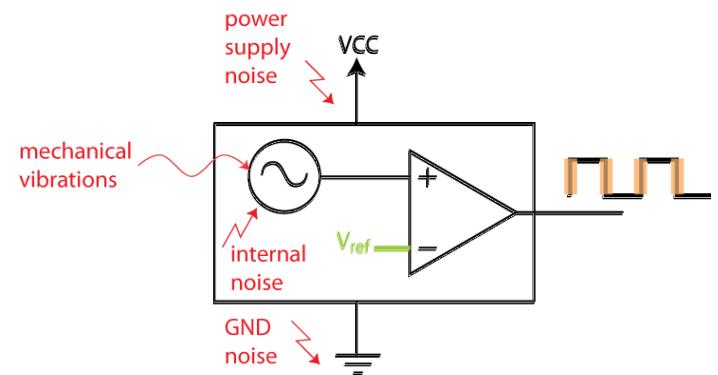
- place all clock inputs in close proximity
- place the clock source at the center and distribute the clock with a "star" topology, consisting of all equal length (terminated) PCB traces.
- if the load becomes excessive for the clock source, there are commercially available clock buffers with multiple outputs having minimum skew
- use PLL based clock retiming circuits (phase adjusting)
- do not use multidrop topology for clock distribution



# Clock distribution

## Clock jitter

- are small variations of a clock oscillator's output transitions from their ideal positions



# Clock distribution

## Clock jitter – how to prevent it

- Clock jitter should be addressed with the same approach as signal integrity problems
- reduce noise sources and their coupling
- apply circuit partitioning, shielding
- prevent crosstalk ([see](#))
- provide good signal return paths
- do not share GND connections between components, ICs
- increase immunity against GND noise by using differential clock lines or isolation techniques  
([see](#) "Mixed Signal Circuits-sampling clock circuits")

## Exercise

### 9. Discuss some advantages and disadvantages of series vs. parallel termination methods

*Answer:*

Series terminations have the advantage of generating less power dissipation (if the logic signal does not switch too often). Their disadvantage is that they should be used only in point-to-point (1:1) connections (and not in 1:n connections).

The advantage of parallel terminations (at the end of the line) is that the level switching (high-to-low or viceversa) waveform observed at any point of the line is made of one single step (this is not the case with series terminations: remember the animation shown during the lesson for series terminations, slide n 48 of this lesson). Therefore parallel terminations are better recommended for multidrop applications (=situations with more than one "receiver" distributed throughout the line, e.g. RS-485). The disadvantage of parallel terminations is their power dissipation, even if the signals are static (not changing).

## Exercise

*Questions related to the circuit & simulation of slide page 48:*

### 10. What happens if we add a $50\Omega$ load at the end of the line?

*Answer:*

Doing so we end up having a combination of series and parallel termination. The  $50\Omega$  load removes reflections at the end of the line since it is matched to the line's impedance. Therefore, we will not see the voltage step from 2.5V to 5V. The final voltage on the line is therefore only 2.5V, which could be insufficient to be recognized as a logic "1" by a 5V CMOS gate.

### 11. What happens if we increase the driver's $R_{series}$ ?

*Answer:*

Since  $R_{series}$  forms a resistive voltage divider with the line's  $Z_0$ , the voltage of the incident signal wave travelling down the line will be smaller. Due to the reflection at the end of the line, the final voltage will be twice that value. We must check if this is still sufficient for the input requirements of the component attached at the end of the line.

# Bibliography

- [1] Analog Devices, I. *Op Amp Applications Handbook*. (Newnes/Elsevier, A cura di)
- [2] Analog Devices, I. *The Data Conversion Hanbook*. (Newnes/Elsevier, A cura di)
- [3] Armstrong, K. (s.d.). *Design techniques for EMC - Part 5a - PCB design and layout*.
- [4] Armstrong, K. (s.d.). *Design techniques for EMC - Part 5b - PCB design and layout*.
- [5] EMC Information Centre ([www.compliance-club.com](http://www.compliance-club.com))
- [6] Johnson, H. W., & Graham, M. *High-speed digital design: a handbook of black magic*. (N. Englewood Cliffs, A cura di)
- [7] Lacoste, R. (2008, October). Cable shielding experiments. *Circuit Cellar* .
- [8] Montrose, M. I. (s.d.). *20-H\_rule*.
- [9] Montrose, M. I. (s.d.). *Decoupling capacitor placement*.
- [10] Montrose, M. I. (s.d.). *Decoupling capacitors*.
- [11] Montrose, M. I. *EMC and the Printed Circuit Board - Design Theory and Layout made simple*. (I. Press, A cura di)
- [12] Montrose, M. I. (s.d.). *Heatsink\_Dilemma*.
- [13] Montrose, M. I. (s.d.). *Image\_Planes*.
- [14] Montrose, M. I. (s.d.). *PCB suppression concepts for EMC*.
- [15] Montrose, M. I. *Printed Circuit Board Design Techniques for EMC Compliance*. (I. Press, A cura di)
- [16] Montrose, M. I. (s.d.). *Right angle trace corners*.
- [17] Montrose, M. I. (s.d.). *Termination and trace lengths*.
- [18] NEC. (s.d.). *PCB-Design for Improved EMC*.
- [19] Ott, H. W. (2001, June). Partitioning and Layout of a Mixed-Signal PCB. *Printed Circuit Design* .
- [20] Ott, H. W., German, R. F., & Clayton, P. R. (1990). Effect of an Image Plane on PCB Radiation. In IEEE (A cura di), *IEEE International Symposium on Electromagnetic Compatibility*. Washington DC.
- [21] SMSC. (s.d.). *Avoid PCB Plane Cuts*.
- [22] R. Monleone, *High Frequency Design Course* (SUPSI)
- [23] Eric Bogatin, *Signal Integrity-Problems & Solutions* ([www.bogatinenterprises.com](http://www.bogatinenterprises.com))
- [24] Ott, H.W., *Electromagnetic Compatibility Engineering* (Wiley)