	A	B	C	D	E	F	G	H
1	Date	Version	Release Note					
2	2018.12.13	V1.3	Updated the function 5 of XPD_DCDC to ANT_SWITCH_BIT0, type O					
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	A	B	C	D
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3		1.INST_NAME indicate the IO_MUX REGISTER defined in eagle_soc.h□for example MTDI_U refers to PERIPHS_IO_MUX_MTDI_U		
4		2.PAD NAME accords with the pin name in schematic		
5		3.FUNCTION says the multifunction of each pin pad		
6		func number 1-5 in this table correspond to FUNCTION 0-4 in SDK		
7		e.g.□set MTDI to GPIO12		
8		[1]#define FUNC_GPIO12 3 //defined in eagle_soc.h		
9		[2]PIN_FUNC_SELECT(PERIPHS_IO_MUX_MTDI_U,FUNC_GPIO12);		
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	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R
1	PAD Name	Inst Name	Pull down	Function1	Type	Function2	Type	Function3	Type	Function4	Type	Function5	Type	At Reset	After Reset	Sleep		
2	MTDI	MTDI_U	Pull up	MTDI	I	I2SI_DATA	I/O/T	HSPIQ MISO	I/O/T	GPIO12	I/O/T	U0DTR	O	oe=0, wpu	wpu	oe=0		
3	MTCK	MTCK_U	Pull up	MTCK	I	I2SI_BCK	I/O/T	HSPID MOSI	I/O/T	GPIO13	I/O/T	U0CTS	I	oe=0, wpu	wpu	oe=0		
4	MTMS	MTMS_U	Pull up	MTMS	I	I2SI_WS	I/O/T	HSPICLK	I/O/T	GPIO14	I/O/T	U0DSR	I	oe=0, wpu	wpu	oe=0		
5	MTDO	MTDO_U	Pull up	MTDO	O/T	I2SO_BCK	I/O/T	HSPICS	I/O/T	GPIO15	I/O/T	U0RTS	O	oe=0, wpu	wpu	oe=0		
6	U0RXD	U0RXD_U	Pull up	U0RXD	I	I2SO_DATA	I/O/T		O	GPIO3	I/O/T	CLK_XTAL	O	oe=0, wpu	wpu	oe=0		
7	U0TXD	U0TXD_U	Pull up	U0TXD	O	SPICS1	I/O/T		O	GPIO1	I/O/T	CLK_RTC	O	oe=0, wpu	wpu	oe=0		
8	SDIO_CLK	SD_CLK_U	Pull up	SD_CLK	I	SPICLK	I/O/T		O	GPIO6	I/O/T	U1CTS	I	oe=0		oe=0		
9	SDIO_DATA_0	SD_DATA0_U	Pull up	SD_DATA0	I/O/T	SPIQ	I/O/T		O	GPIO7	I/O/T	U1TXD	O	oe=0		oe=0		
10	SDIO_DATA_1	SD_DATA1_U	Pull up	SD_DATA1	I/O/T	SPID	I/O/T		O	GPIO8	I/O/T	U1RXD	I	oe=0		oe=0		
11	SDIO_DATA_2	SD_DATA2_U	Pull up	SD_DATA2	I/O/T	SPIHD	I/O/T		O	GPIO9	I/O/T	HSPIHD	I/O/T	oe=0		oe=0		
12	SDIO_DATA_3	SD_DATA3_U	Pull up	SD_DATA3	I/O/T	SPIWP	I/O/T		O	GPIO10	I/O/T	HSPIWP	I/O/T	oe=0		oe=0		
13	SDIO_CMD	SD_CMD_U	Pull up	SD_CMD	I/O/T	SPICS0	I/O/T		O	GPIO11	I/O/T	U1RTS	O	oe=0		oe=0		
14	GPIO0	GPIO0_U	Pull up	GPIO0	I/O/T	SPICS2	I/O/T		O		I/O/T	CLK_OUT	O	oe=0, wpu	wpu	oe=0		
15	GPIO2	GPIO2_U	Pull up	GPIO2	I/O/T	I2SO_WS	I/O/T	U1TXD	O		I/O/T	U0TXD	O	oe=0, wpu	wpu	oe=0		
16	GPIO4	GPIO4_U	Pull up	GPIO4	I/O/T	CLK_XTAL	O							oe=0		oe=0		
17	GPIO5	GPIO5_U	Pull up	GPIO5	I/O/T	CLK_RTC	O							oe=0		oe=0		
18																		
19	XPD_DCDC	XPD_DCDC	Pull down	XPD_DCDC	O	RTC_GPIO0	I/O/T	EXT_WAKEUP	I	DEEPSLEEP	O	ANT_SWITCH_BIT0	O	oe=1,wpd	oe=1,wpd	oe=1		
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	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1	Num	Pin	Address	Bit[8]	Bit[7]	Bit[6]	Bit[5:4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	GPIO pin			
2				Function Select[2]	Pullup	Rsvd	Function Select[1:0]	Sleep Pullup	Rsvd	Sleep Sel	Sleep OE				
3	1	MTDI	0x60000804	0	1	0	0	0	0	0	0	GPIO12			
4	2	MTCK	0x60000808	0	1	0	0	0	0	0	0	GPIO13			
5	3	MTMS	0x6000080C	0	1	0	0	0	0	0	0	GPIO14			
6	4	MTDO	0x60000810	0	1	0	0	0	0	0	0	GPIO15			
7	5	U0RXD	0x60000814	0	1	0	0	0	0	0	0	GPIO3			
8	6	U0TXD	0x60000818	0	1	0	0	0	0	0	0	GPIO1			
9	7	SDIO_CLK	0x6000081C	0	0	0	0	0	0	0	0	GPIO6			
10	8	SDIO_DATA_0	0x60000820	0	0	0	0	0	0	0	0	GPIO7			
11	9	SDIO_DATA_1	0x60000824	0	0	0	0	0	0	0	0	GPIO8			
12	10	SDIO_DATA_2	0x60000828	0	0	0	0	0	0	0	0	GPIO9			
13	11	SDIO_DATA_3	0x6000082C	0	0	0	0	0	0	0	0	GPIO10			
14	12	SDIO_CMD	0x60000830	0	0	0	0	0	0	0	0	GPIO11			
15	13	GPIO0	0x60000834	0	1	0	0	0	0	0	0	GPIO0	after reset, the default is function5 to export the clock		
16	14	GPIO2	0x60000838	0	1	0	0	0	0	0	0	GPIO2	after reset, the default is function5 to export U0TXD		
17	15	GPIO4	0x6000083C	1	0	0	0	0	0	0	0	GPIO4			
18	16	GPIO5	0x60000840	1	0	0	0	0	0	0	0	GPIO5			
19															
20															
21						Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1:0]				
22						Function Select[2]	Sleep Pulldown	Rsvd	Pulldown	Rsvd	Function Select[1:0]				
23	17	XPD_DCDC	0x600007A0			0	0	0	0	0	0	RTC_GPIO0			
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2	U0TXD	Strapping to chip_test_mode	1: normal mode; 0: chip_test_mode			
3						
4	MTDO	Strapping to STRAPPING_GPIO2 for SW boot_sel [2]				
5	GPIO0	Strapping to STRAPPING_GPIO1 for SW boot_sel [1]				
6	GPIO2	Strapping to STRAPPING_GPIO0 for SW boot_sel [0]				
7						
8	SDIO_DATA_3	Strapping to STRAPPING_GPIO[15] for SW sdio_boot_sel [2]				
9	SDIO_DATA_2	Strapping to STRAPPING_GPIO[14] for SW sdio_boot_sel [1]				
10	SDIO_DATA_0	Strapping to STRAPPING_GPIO[13] for SW sdio_boot_sel [0]				
11						
12	Boot_sel	SD_sel != 3'b010	SD_sel == 3'b010			
13	7	SDIO HighSpeed V2 IO	Uart1 Booting			
14	6	SDIO LowSpeed V1 IO	Uart1 Booting			
15	5	SDIO HighSpeed V1 IO	Uart1 Booting			
16	4	SDIO LowSpeed V2 IO	Uart1 Booting			
17	3	FLASH BOOT				
18	2	Jump Boot				
19	1	UART Boot				
20	0	Remapping				
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22						
23	GPIO0	after reset, the default is function5 to export the clock				
24	GPIO2	U0TXD signal can be output through GPIO2 pad besides U0TXD pad				
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