Meta Large Language Model Compiler: Foundation Models of Compiler Optimization

Arxiv

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INLINING OPTIMIZATIONS CAN BE SURPRISING 2

```
Struct Loop_Slow() {
   Struct s = new();
   for(int i = 0; i < 1000; i++)
       s = Add(s);
   return s;
static Struct Add(Struct v) {
   var a = v.A + v.A;
   return new(a, a);
```

```
Struct Loop_Fast() {
   Struct s = new();
   for(int i = 0; i < 1000; i++)
        s = Add(s,0);
   return s;
static Struct Add(Struct v, int x) {
   var a = v.A + v.A;
   return new(a, a);
```

	The state of the s	StdDev	
	0.1069 us	0.0893 us	

Compilation Pipeline

Source Code (*.c, *.cpp)

Abstract Syntax Tree

Intermediate Representation

Binary

Intermediate Representation

```
define dso_local i32 @main() #0 {
  call void @srand(i32 2019) #4
  br label %1
1:
                                                  ; preds = %5, %0
 %2 = phi i32 [ 0, %0 ], [ %9, %5 ]
 %3 = icmp slt i32 %2, 10
  br i1 %3, label %5, label %4
4:
                                                  ; preds = %1
  ret i32 0
5:
                                                  ; preds = %1
 %6 = call i32 @rand() #4
 %7 = srem i32 %6, 3
 \%8 = \text{call i32 (i8*, ...) } @printf(i8* getelementptr inbounds ([4 x i8], [4 x i8]* @.str, i64 0, i64 0), i32
%7)
 %9 = add nsw i32 %2, 1
  br label %1
```

LLM Compiler

Training LLMs is resource-intensive

 LLM Compiler, openly available pre-trained models designed for code optimization tasks.

- Two models
 - LLM Compiler (7B, 13B)
 - LLM Compiler FTD (7B, 13B)

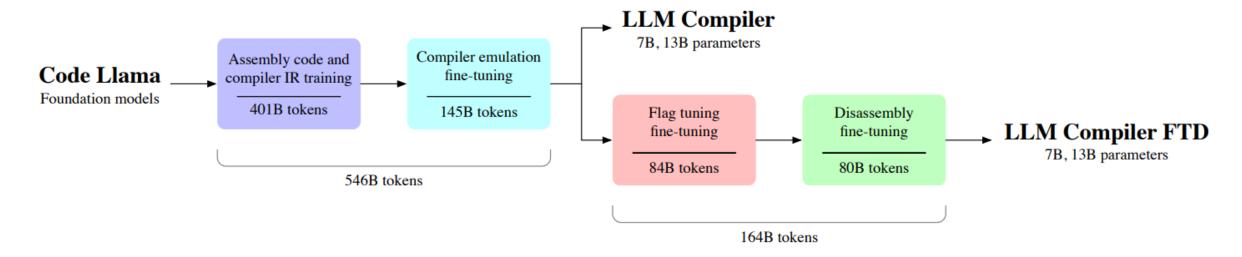


Figure 1: LLM COMPILER models are specialized from CODE LLAMA by training on 546 billion tokens of compiler-centric data in two stages. In the first stage the models are trained predominantly on unlabelled compiler IRs and assembly code. In the next stage the models are instruction fine-tuned to predict the output and effect of optimizations. LLM COMPILER FTD models are then further fine-tuned on 164 billion tokens of downstream flag tuning and disassembly task datasets, for a total of 710 billion training tokens. During each of the four stages of training, 15% of data from the previous tasks is retained.

Dataset

- Coding LLMs are typically trained with
 - Largely high level source language (Python)
 - Assembly (small)
 - Compiler IR (really small)
 - Compiler Centric Dataset needed

Dataset	Sampling prop.	Epochs	Disk size				
IR and assembly pretraining (401 billion tokens)							
Code	85.00%	1.000	$872~\mathrm{GB}$				
Natural language related to code	e 14.00%	0.019	$942~\mathrm{GB}$				
Natural language	1.00%	0.001	$938~\mathrm{GB}$				
Compiler emulation (additional 145 billion tokens)							
Compiler emulation	85.00%	1.702	$175~\mathrm{GB}$				
Code	13.00%	0.055	$872~\mathrm{GB}$				
Natural language related to code	e 1.80%	0.001	$942~\mathrm{GB}$				
Natural language	0.20%	$6.9\mathrm{e}{-5}$	$938~\mathrm{GB}$				
Flag tuning fine-tuning (additional 84 billion tokens)							
Flag tuning	85.00%	1.700	$103~\mathrm{GB}$				
Compiler emulation	11.73%	0.136	$175~\mathrm{GB}$				
Code	2.84%	0.007	$872~\mathrm{GB}$				
Natural language related to code	e 0.40%	$1.1e{-4}$	$942~\mathrm{GB}$				
Natural language	0.03%	8.8e-6	$938~\mathrm{GB}$				
Disassembly fine-tuning (additional 80 billion tokens)							
Disassembly	85.00%	1.707	88 GB				
Flag tuning	4.68%	0.089	$103~\mathrm{GB}$				
Compiler emulation	8.07%	0.089	$175~\mathrm{GB}$				
Code	1.96%	0.004	$872~\mathrm{GB}$				
Natural language related to code	e 0.27%	7.5e - 5	$942~\mathrm{GB}$				
Natural language	0.03%	5.7e-6	$938~\mathrm{GB}$				

 ${\bf Table\ 1:\ Training\ datasets\ used.}$

Training Tasks

Compiler emulation (fine tuning)

Flag tuning (fine tuning)

Disassembly (fine tuning)

Compiler Emulation

- Emulate Compiler
 - Emit Optimized IR
 - Emit Assembly

- Dataset
 - 1~50 optimization passes applied
 - Pass chosen randomly

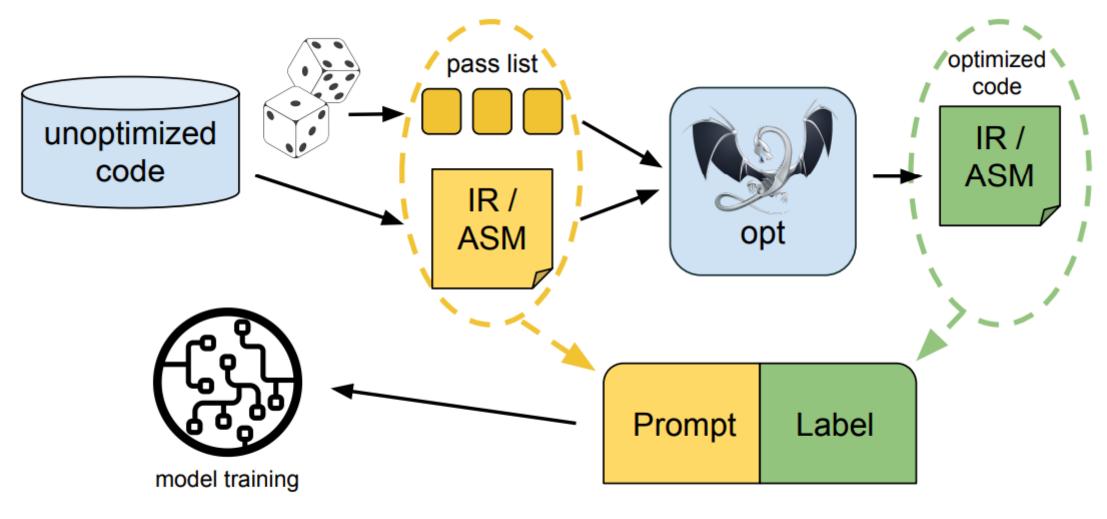


Figure 2: To give the model an understanding of how compiler optimizations work, we use *compiler emulation*. Unoptimized code samples and random pass lists are given to opt to generate optimized code (IR or assembly). Pass list and input code are taken together as prompt while the generated output code is used as label.

B.1 Compiler emulation prompts

Prompt:

```
[INST] Give the LLVM-IR for the following code when optimized using opt -p 'module(default<0z>)':
<code>; ModuleID = '<stdin>'
source_filename = "-"
target datalayout = "e-m:e-p270:32:32-p271:32:32-p272:64:64-i64:64-f80:128-n8:16:32:64-S128"
target triple = "x86_64-unknown-linux-gnu"
; Function Attrs: minsize nounwind optsize uwtable
define dso_local i32 @add_two(i32 noundef %0, i32 noundef %1) #0 {
 %3 = alloca i32, align 4
 %4 = alloca i32, align 4
  store i32 %0, ptr %3, align 4, !tbaa !5
  store i32 %1, ptr %4, align 4, !tbaa !5
 %5 = load i32, ptr %3, align 4, !tbaa !5
  %6 = load i32, ptr %4, align 4, !tbaa !5
 %7 = add nsw i32 %5, %6
 ret i32 %7
attributes #0 = { minsize nounwind optsize uwtable "min-legal-vector-width"="0" "no-trapping-math"="true"
→ "stack-protector-buffer-size"="8" "target-cpu"="x86-64" "target-features"="+cmov,+cx8,+fxsr,+mmx,+sse
\hookrightarrow,+sse2,+x87" "tune-cpu"="generic" }
!llvm.module.flags = !{!0, !1, !2, !3}
!11vm.ident = !{!4}
!0 = !\{i32\ 1, !"wchar_size", i32\ 4\}
!1 = !{i32 8, !"PIC Level", i32 2}
!2 = !{i32 7, !"PIE Level", i32 2}
!3 = !{i32 7, !"uwtable", i32 2}
!4 = !{!"clang version 17.0.6 (git@github.com:fairinternal/CodeGen.git
→b05db9bbf7a92019267416c1bb9996fe6134e3f1)"}
!5 = !\{!6, !6, i64 0\}
!6 = !{!"int", !7, i64 0}
!7 = !{!"omnipotent char", !8, i64 0}
!8 = !{!"Simple C/C++ TBAA"}
</code>
The input code has instruction count 8 and binary size 65 bytes. [/INST]
```

```
The LLVM-IR will have instruction count 2 and binary sise 53 bytes:
<code>: ModuleID = '<stdin>'
source_filename = "-"
target datalayout = "e-m:e-p270:32:32-p271:32:32-p272:64:64-i64:64-f80:128-n8:16:32:64-S128"
target triple = "x86_64-unknown-linux-gnu"
; Function Attrs: minsize mustprogress nofree norecurse nosync nounwind optsize willreturn memory(none)

→uwtable

define dso_local i32 @add_two(i32 noundef %0, i32 noundef %1) local_unnamed_addr #0 {
 %3 = add nsw i32 %1, %0
 ret i32 %3
attributes #0 = { minsize mustprogress nofree norecurse nosync nounwind optsize willreturn memory(none)
→uwtable "min-legal-vector-width"="0" "no-trapping-math"="true" "stack-protector-buffer-size"="8" "

→ target - cpu "= "x86 - 64" "target - features "= "+ cmov , + cx8 , + fxsr , + mmx , + sse , + sse2 , + x87" "tune - cpu "= "generic" }

!llvm.module.flags = !{!0, !1, !2, !3}
!11vm.ident = !{!4}
!0 = !\{i32 1, !"wchar_size", i32 4\}
!1 = !{i32 8, !"PIC Level", i32 2}
!2 = !{i32 7, !"PIE Level", i32 2}
!3 = !\{i32\ 7, !"uwtable", i32\ 2\}
!4 = !{!"clang version 17.0.6 (git@github.com:fairinternal/CodeGen.git
\hookrightarrow b05db9bbf7a92019267416c1bb9996fe6134e3f1)"}
</code>
```

Listing 2: Prompt used for $IR \to IR$ compiler emulation.

Prompt: [INST] Give the assembly for the following code when optimized using opt -p 'module(default<0z>)': <code>: ModuleID = '<stdin>' source_filename = "-" target datalayout = "e-m:e-p270:32:32-p271:32:32-p272:64:64-i64:64-f80:128-n8:16:32:64-S128" target triple = "x86_64-unknown-linux-gnu" ; Function Attrs: minsize nounwind optsize uwtable define dso_local i32 @add_two(i32 noundef %0, i32 noundef %1) #0 { %3 = alloca i32, align 4 %4 = alloca i32, align 4 store i32 %0, ptr %3, align 4, !tbaa !5 store i32 %1, ptr %4, align 4, !tbaa !5 %5 = load i32, ptr %3, align 4, !tbaa !5 %6 = load i32, ptr %4, align 4, !tbaa !5 %7 = add nsw i32 %5, %6ret i32 %7 } attributes #0 = { minsize nounwind optsize uwtable "min-legal-vector-width"="0" "no-trapping-math"="true" → "stack-protector-buffer-size"="8" "target-cpu"="x86-64" "target-features"="+cmov,+cx8,+fxsr,+mmx,+sse →,+sse2,+x87" "tune-cpu"="generic" } !llvm.module.flags = !{!0, !1, !2, !3} $!llvm.ident = !{!4}$!0 = !{i32 1, !"wchar_size", i32 4} !1 = !{i32 8, !"PIC Level", i32 2} !2 = !{i32 7, !"PIE Level", i32 2} !3 = !{i32 7, !"uwtable", i32 2} !4 = !{!"clang version 17.0.6 (git@github.com:fairinternal/CodeGen.git →b05db9bbf7a92019267416c1bb9996fe6134e3f1)"} $!5 = !\{!6, !6, i64 0\}$ $!6 = !{!"int", !7, i64 0}$!7 = !{!"omnipotent char", !8, i64 0} $!8 = !{!"Simple C/C++ TBAA"}$ </code> The input code has instruction count 8 and binary size 65 bytes. [/INST]

```
The assembly will have instruction count 2 and binary sise 53 bytes:
<code> .text
  .file "-"
                                          # -- Begin function add_two
  .globl add_two
  .type add_two,@function
add_two:
                                        # @add_two
  .cfi_startproc
# %bb.0:
  movl %esi, %eax
  addl %edi, %eax
 retq
.Lfunc_end0:
  .size add_two, .Lfunc_end0-add_two
  .cfi_endproc
                                        # -- End function
  .ident "clang version 17.0.6 (git@github.com:fairinternal/CodeGen.git

→ b05db9bbf7a92019267416c1bb9996fe6134e3f1)"
  .section ".note.GNU-stack", "", @progbits
  .addrsig
</code>
```

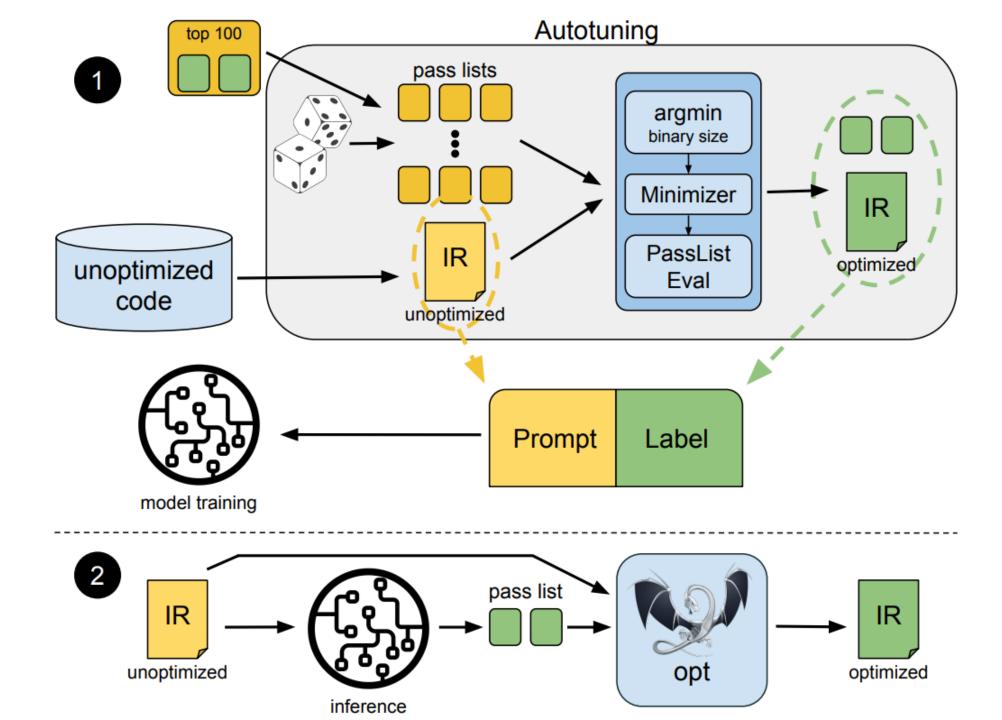
Listing 3: Prompt used for $IR \rightarrow assembly$ compiler emulation.

Flag Tuning

- Goal of a Compiler
 - Size of the final binary
 - Performance of final binary
 - •
- LLM Compiler FTD
 - Unoptimized IR (input)
 - List of opt flags that should be applied (output)
 - *PassListEval was used to identify pass lists that cause compiler failure

How?

- 1. Unoptimized IR is compiled against multiple random pass lists
- 2. Select pass lists that result with minimum binary size
- 3. Evaluate correctness (PassListEval)
- 4. Final Pass list and optimized IR is used as label in training



Prompt:

```
[INST] Tell me how to optimize this LLVM-IR for object file size:
<code>: ModuleID = '<stdin>'
source_filename = "-"
target datalayout = "e-m:e-p270:32:32-p271:32:32-p272:64:64-i64:64-f80:128-n8:16:32:64-S128"
target triple = "x86_64-unknown-linux-gnu"
; Function Attrs: minsize nounwind optsize uwtable
define dso_local i32 @add_two(i32 noundef %0, i32 noundef %1) #0 {
 %3 = alloca i32, align 4
 %4 = alloca i32, align 4
  store i32 %0, ptr %3, align 4, !tbaa !5
  store i32 %1, ptr %4, align 4, !tbaa !5
 %5 = load i32, ptr %3, align 4, !tbaa !5
 %6 = load i32, ptr %4, align 4, !tbaa !5
 %7 = add nsw i32 %5, %6
 ret i32 %7
attributes #0 = { minsize nounwind optsize uwtable "min-legal-vector-width"="0" "no-trapping-math"="true"
→ "stack-protector-buffer-size"="8" "target-cpu"="x86-64" "target-features"="+cmov,+cx8,+fxsr,+mmx,+sse

→ ,+sse2 ,+x87 " "tune-cpu"="generic" }
!llvm.module.flags = !{!0, !1, !2, !3}
!11vm.ident = !{!4}
!0 = !\{i32\ 1, !"wchar_size", i32\ 4\}
!1 = !{i32 8, !"PIC Level", i32 2}
!2 = !{i32 7, !"PIE Level", i32 2}
!3 = !{i32 7, !"uwtable", i32 2}
!4 = !{!"clang version 17.0.6 (git@github.com:fairinternal/CodeGen.git
\hookrightarrow b05db9bbf7a92019267416c1bb9996fe6134e3f1)"}
!5 = !\{!6, !6, i64 0\}
!6 = !{!"int", !7, i64 0}
!7 = !{!"omnipotent char", !8, i64 0}
!8 = !{!"Simple C/C++ TBAA"}</code> [/INST]
```

```
The code has object file size of 65 which can be reduced to 53 by running:

'opt -p 'module(default < 0z > ) '

This will produce code:
```

Disassembly

Assembly -> IR

- Correctness?
 - Verifying equivalence is hard
 - Round tripping: If we generate assembly using the IR and acquire the original assembly (assume correct)
- LLM Compiler FTD
 - Assembly Code (input)
 - Corresponding Disassembled IR (output)

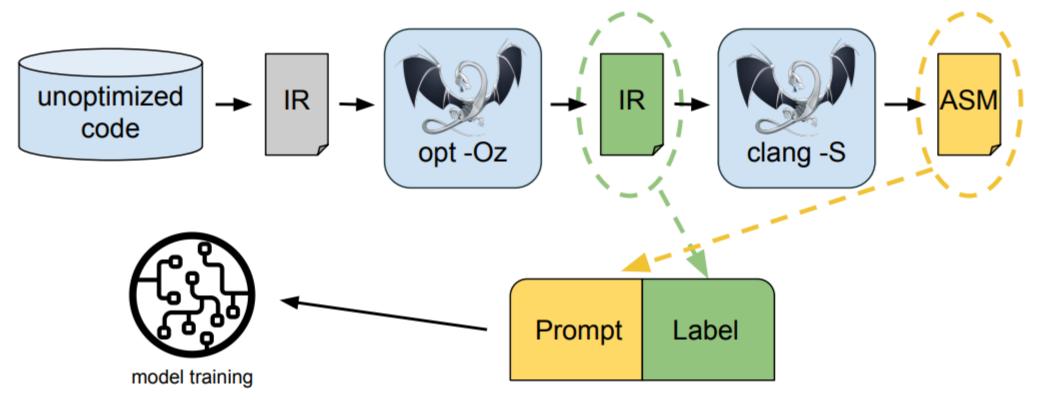


Figure 5: We train the model to understand the relationship between assembly and IR by training it to disassemble a given code sample to its corresponding IR. The IR used to label this training task was generated by optimizing an IR with the -Oz flag.

Prompt:

```
[INST] Disassemble this code to LLVM-IR:
<code> .text
 .file "-"
 .globl add_two
                                          # -- Begin function add_two
 .type add_two,@function
add_two:
                                        # @add_two
  .cfi_startproc
# %bb.0:
 movl %edi, -4(%rsp)
 movl %esi, -8(%rsp)
 movl -4(%rsp), %eax
 addl -8(%rsp), %eax
 retq
.Lfunc_end0:
  .size add_two, .Lfunc_end0-add_two
  .cfi_endproc
                                        # -- End function
  .ident "clang version 17.0.6 (git@github.com:fairinternal/CodeGen.git

→ b05db9bbf7a92019267416c1bb9996fe6134e3f1) "

  .section ".note.GNU-stack", "", @progbits
  .addrsig
</code> [/INST]
```

```
<code>: ModuleID = '<stdin>'
source filename = "-"
target datalayout = "e-m:e-p270:32:32-p271:32:32-p272:64:64-i64:64-f80:128-n8:16:32:64-S128"
target triple = "x86_64-unknown-linux-gnu"
; Function Attrs: minsize nounwind optsize uwtable
define dso_local i32 @add_two(i32 noundef %0, i32 noundef %1) #0 {
 %3 = alloca i32, align 4
 %4 = alloca i32, align 4
 store i32 %0, ptr %3, align 4, !tbaa !5
 store i32 %1, ptr %4, align 4, !tbaa !5
 %5 = load i32, ptr %3, align 4, !tbaa !5
 %6 = load i32, ptr %4, align 4, !tbaa !5
 %7 = add nsw i32 %5, %6
 ret i32 %7
attributes #0 = { minsize nounwind optsize uwtable "min-legal-vector-width"="0" "no-trapping-math"="true"
→ "stack-protector-buffer-size"="8" "target-cpu"="x86-64" "target-features"="+cmov,+cx8,+fxsr,+mmx,+sse

→ ,+sse2 ,+x87 "tune-cpu"="generic" }

!llvm.module.flags = !{!0, !1, !2, !3}
!11vm.ident = !{!4}
!0 = !{i32 1, !"wchar_size", i32 4}
!1 = !{i32 8, !"PIC Level", i32 2}
!2 = !{i32 7, !"PIE Level", i32 2}
!3 = !{i32 7, !"uwtable", i32 2}
!4 = !{!"clang version 17.0.6 (git@github.com:fairinternal/CodeGen.git
→b05db9bbf7a92019267416c1bb9996fe6134e3f1)"}
!5 = !\{!6, !6, i64 0\}
!6 = !{!"int", !7, i64 0}
!7 = !{!"omnipotent char", !8, i64 0}
!8 = !{!"Simple C/C++ TBAA"}
</code>
```

Evaluation: Flag Tuning

• Dataset: MiBench benchmark suite (Guthaus et al. 2001)

- Method
 - Unseen Program (input)
 - Pass List (output)
 - Compare against (-Oz)
- Models
 - GPT-4 Turbo
 - Code Llama Instruct

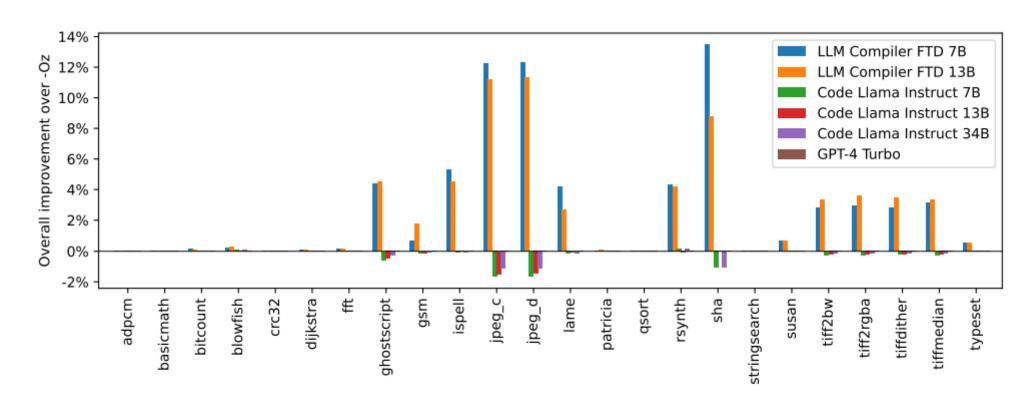


Figure 6: Improvement over -Oz for each of the benchmarks in MiBench.

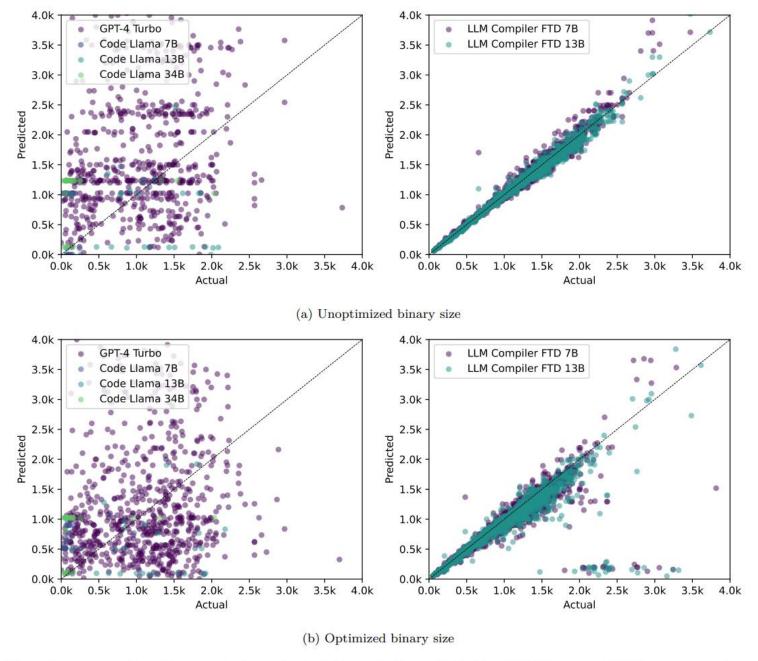


Figure 7: Accuracy of models at predicting code size before and after optimization. LLM COMPILER FTD is most accurate at predicting code size before optimization than after optimization. Code Llama and GPT-4 Turbo, shown left, display little correlation between predicted and actual values.

Disassembly Task

Dataset: MiBench benchmark suite

- Method
 - Assembly Code (input)
 - LLVM IR (output)
- Models
 - GPT-4 Turbo
 - Code Llama Instruct

Table 5: Model performance at disassembling 2,015 assembly codes taken from MiBench. We use *Round trips* to evaluate the capabilities of models, by taking the IR generated by the models and attempting to lower it back to assembly. *Round trips* shows the number of disassembled IRs that can be lowered back, *Round trip BLEU* compares the round-tripped assemblies against the originals, and *Round trip exact match* is the proportion of round-tripped assemblies that are exact character-for-character matches with the input, indicating lossless round-trip from assembly up to IR and back down again.

	Size	Round trips	Round trip BLEU	Round trip exact match
LLM Compiler FTD	7B 13B	936 905	0.951 0.960	12.7% 13.8%
Code Llama - Instruct	7B 13B 34B	30 53 12	0.477 0.615 0.458	$0.0\% \\ 0.0\% \\ 0.0\%$
GPT-4 Turbo (2024-04-09)	-	127	0.429	0.0%

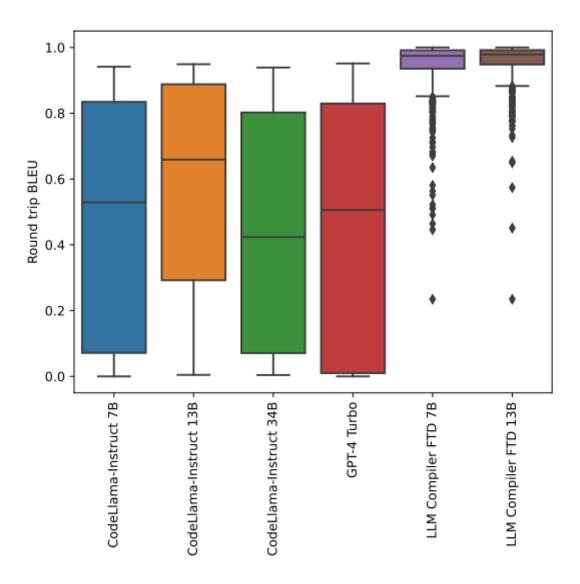


Figure 8: Distribution of round trip BLEU scores on the disassembly task.