The Pixel clock (PCLK) is running all the time without stopping, it is used for entering VS, HS, DE and DB [23:0] states when there is a rising edge of the PCLK. The PCLK can not be used as the internal clock for other functions of the display module.

Vertical synchronization (Vsync) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

Horizontal synchronization (Hsync) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

DE (Data Enable) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the PCLK signal. DB [23:0] are used to tell what is the information of the image that is transferred on the display (When DE= '0' (low) and there is a rising edge of PCLK). DB [23:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the PCLK signal.

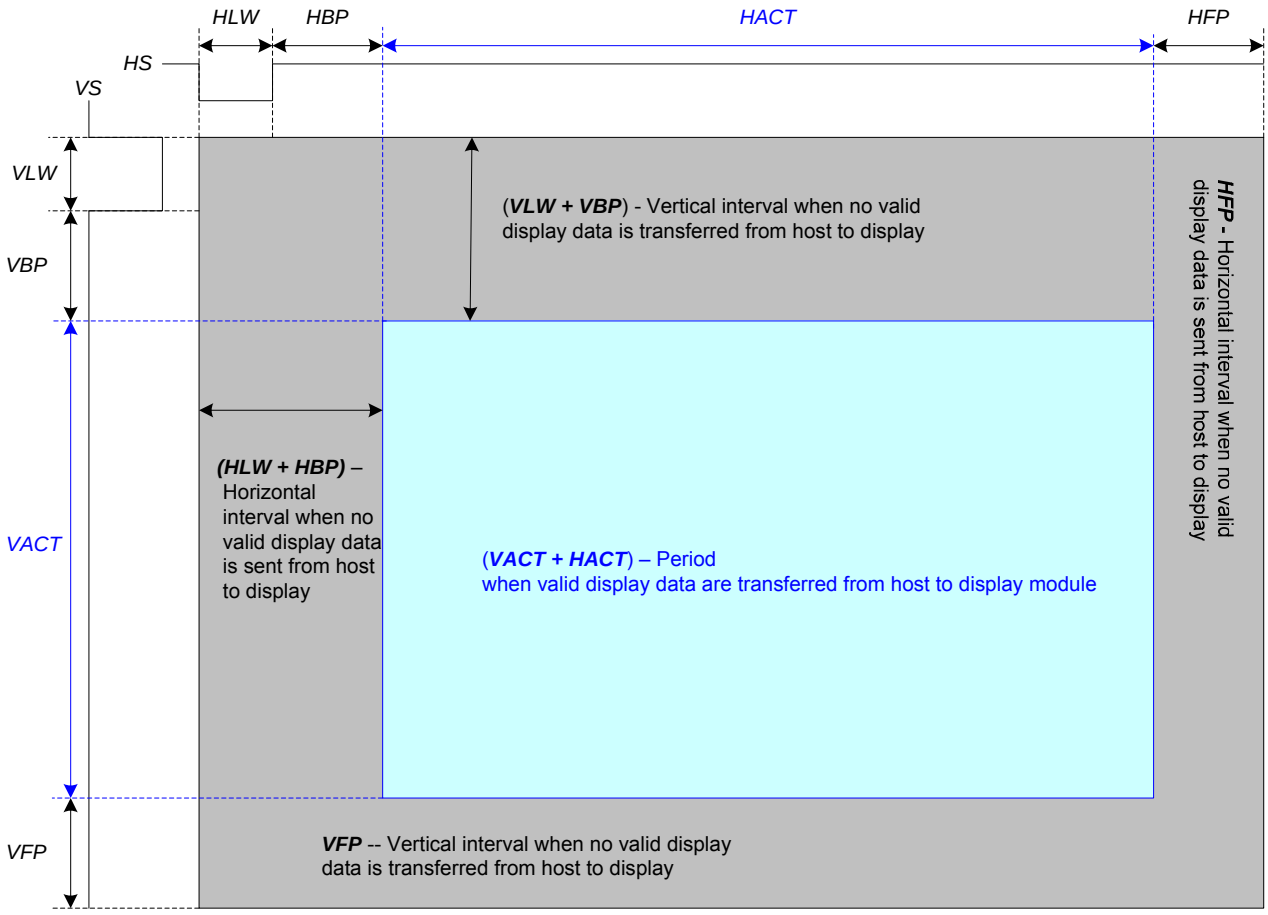
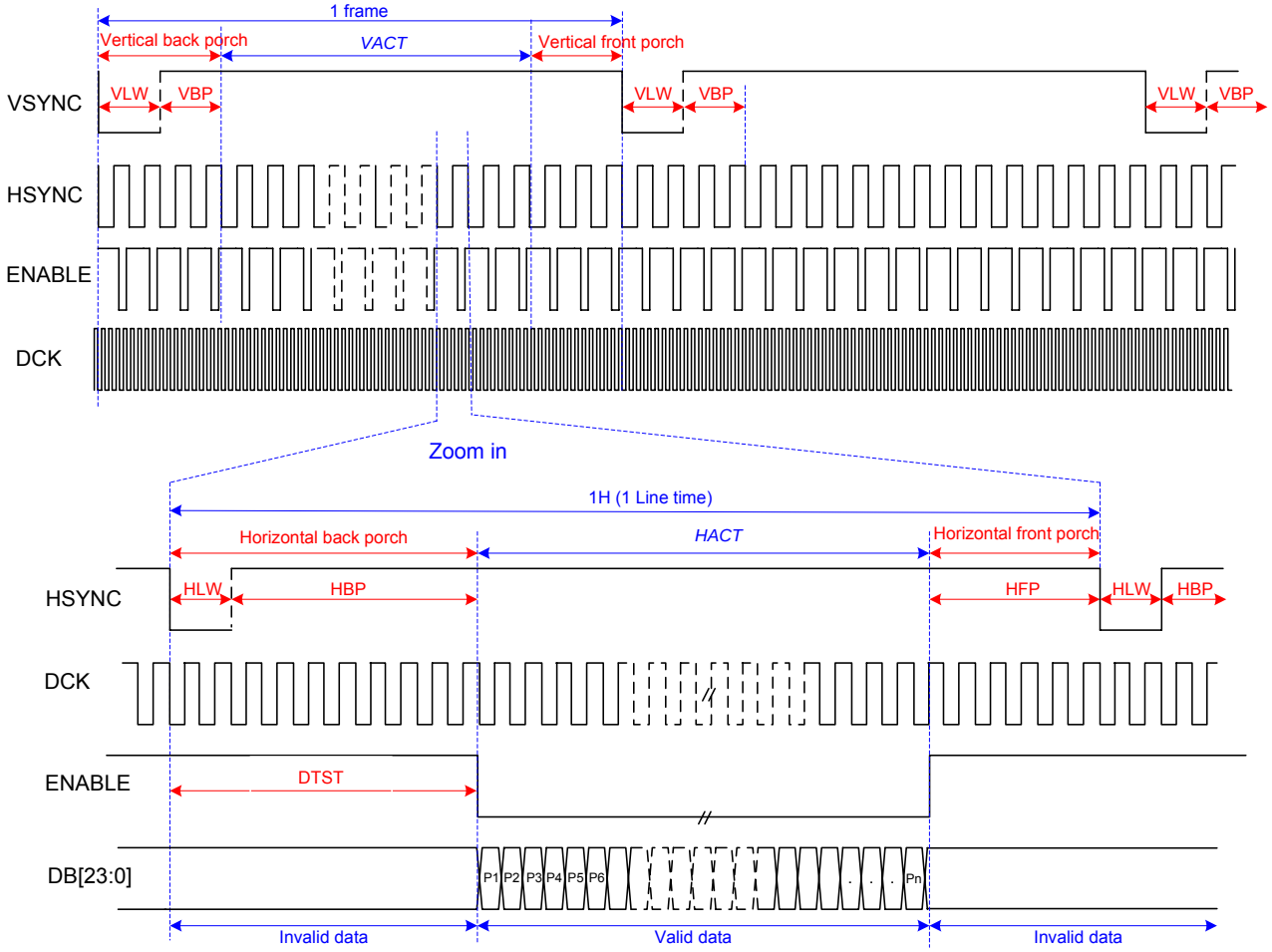


Figure 11 General DPI timing diagram

3.4.2. DPI Interface Timing

The timing chart of 24-/18-/16-bit DPI (RGB) interface mode is illustrated in Figure 12.



VLW : VSYNC Low pulse Width
HLW : HSYNC Low pulse Width
DTST : Data Transfer Startup Time
Pn : pixel 1, pixel 2…, pixel n.

Parameter	Symbols	Condition	Min.	Typ.	Max.	Units
Frame Rate	FR		54		66	fps
Horizontal Low Pulse width	HLW		1		-	DOTCLK
Horizontal Back Porch	HBP		2		126	DOTCLK
Horizontal Address	HACT			480		DOTCLK
Horizontal Front Porch	HFP		2		-	DOTCLK
Vertical Low Pulse width	VLW		1		126	Line
Vertical Back Porch	VBP		1		126	Line
Vertical Address	VACT				864	Line
Vertical Front Porch	VFP		1		255	Line
Data Clock	DCLK		16.6		41.7	MHz

Figure 12 DPI Interface Timing diagram[Note1,Note2]

Note1. HLW+HBP+HFP >= 2us.
Note2. VSPL='0', HSPL='0', DPL='0' and EPL='0' of "(Interface Mode Control 21h of the Page 1)" command.