Custom Asynchronous Binary Protocol

Description:
This is a custom asynchronous protocol focusing on quick resyncs. It uses edge detection to find dropped bits and resync within one frame length.

Structure:
This protocol uses 10 bit frames with two stop bits. The first stop bit is a logic HIGH for a normal bit duration. The second stop bit called the inter-frame bit is a logic LOW for 1.5 bit durations. Then there is a start bit which is a logic HIGH for the normal bit duration. The receiver detects a logic LOW signal that lasts 1.5 bit durations to find the end/start of each frame. Due to this protocol using edge detection to find bits the inter-frame bit has to be wrapped in opposite logic signals.

Bit Type	**Logic Level**	**Duration** (bit durations)
Start Bit	HIGH	1
8 Data Bits	HIGH/LOW	1 per bit (8 total)
Stop Bit	HIGH	1
Inter-Frame Bit	LOW	1.5

Multi-Core:
For precise timing it is best to run the receiver on a multi-core processor. One core detects the value and duration of each pulse while the other core breaks long pulses down into individual bits and decodes the binary and also handles resyncing. The timing core is constantly checking the value of the pulse and once it changes it sends the value adn duration of the pulse to the other core which decodes it. Having any other processes running on the timing core would decrease the precision massively.

Speed Limitations:
The biggest limits to speed are timing precision and decoding speed. Two big modifications that could be made to greatly increase maximum speed are to run the received signal into a comparator to create a digital signal and modify the code to run on an FPGA (field programmable gate array) for parallel processing.