



Laboratory Report

Laboratory Exercise No.:	7	Date Performed:	November 6, 2024
Laboratory Exercise Title:	Hardware Interrupt Interfacing		
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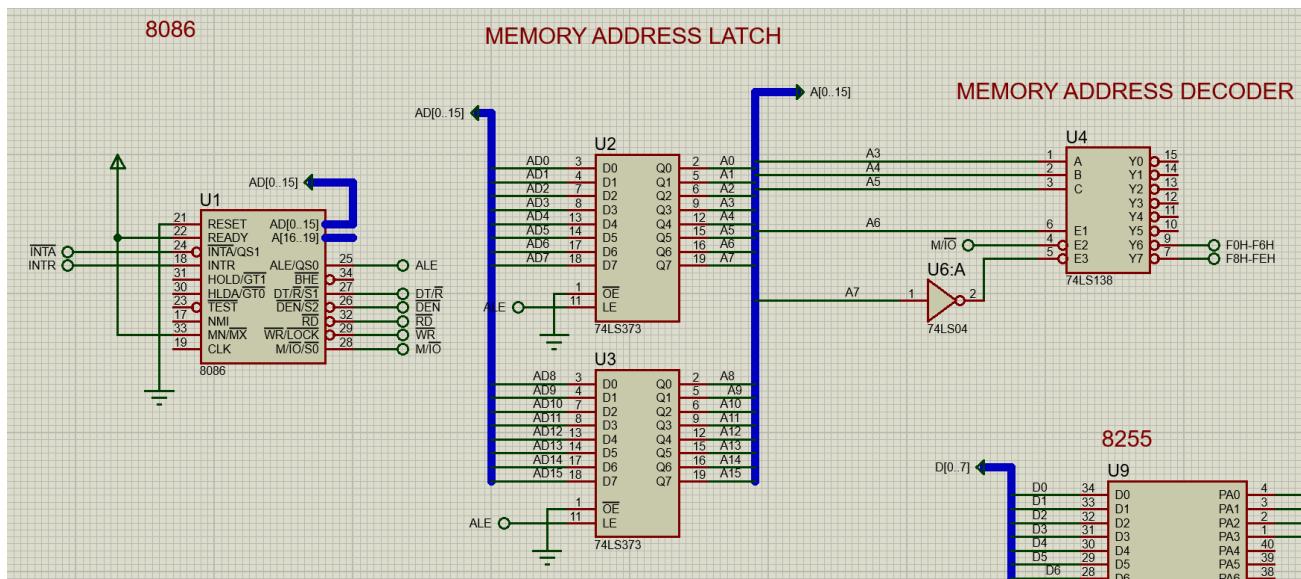
Activity #1

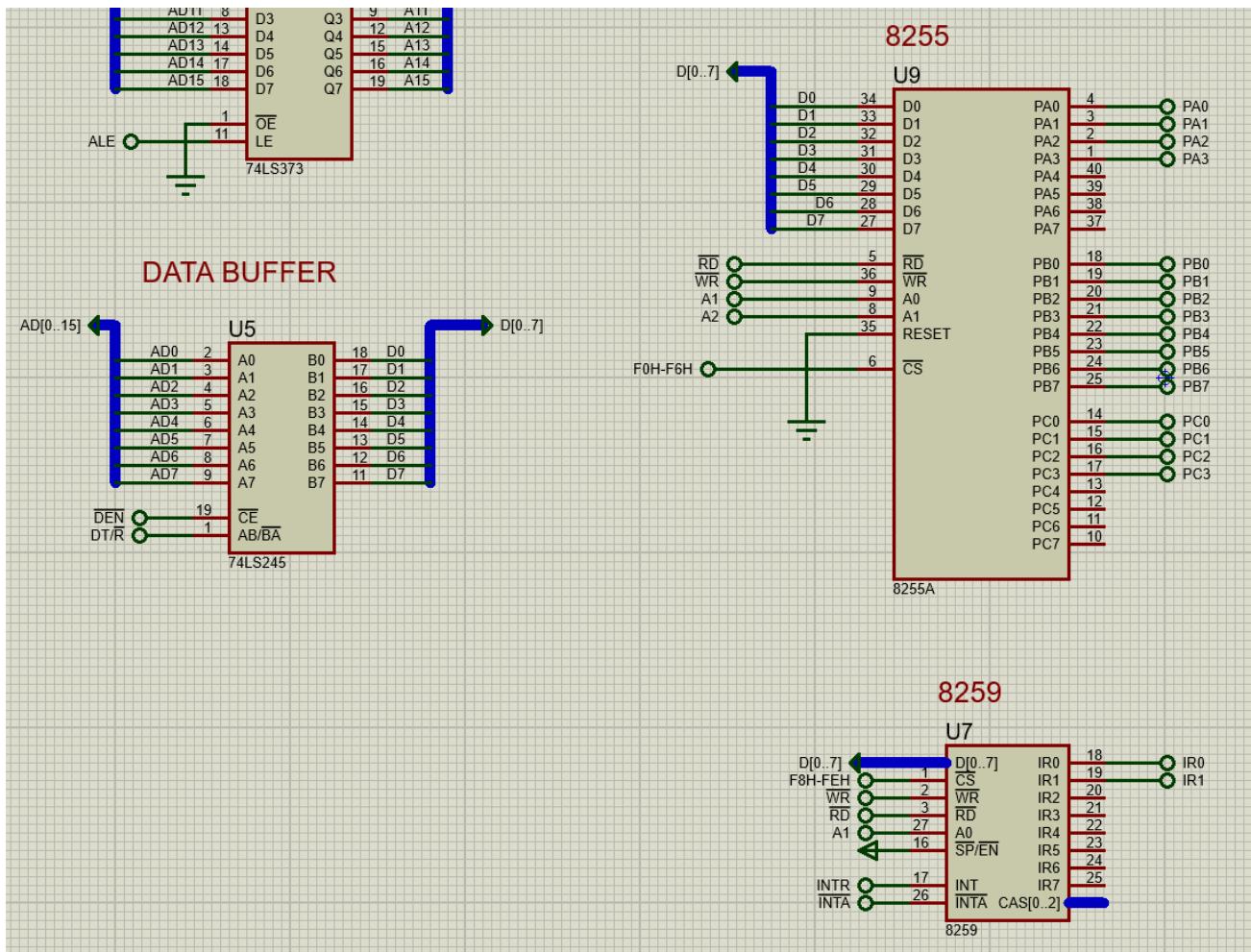
ICW4 needed, Single Mode, Call Address Interval of 8, Edge Triggered ICW1 = 13H

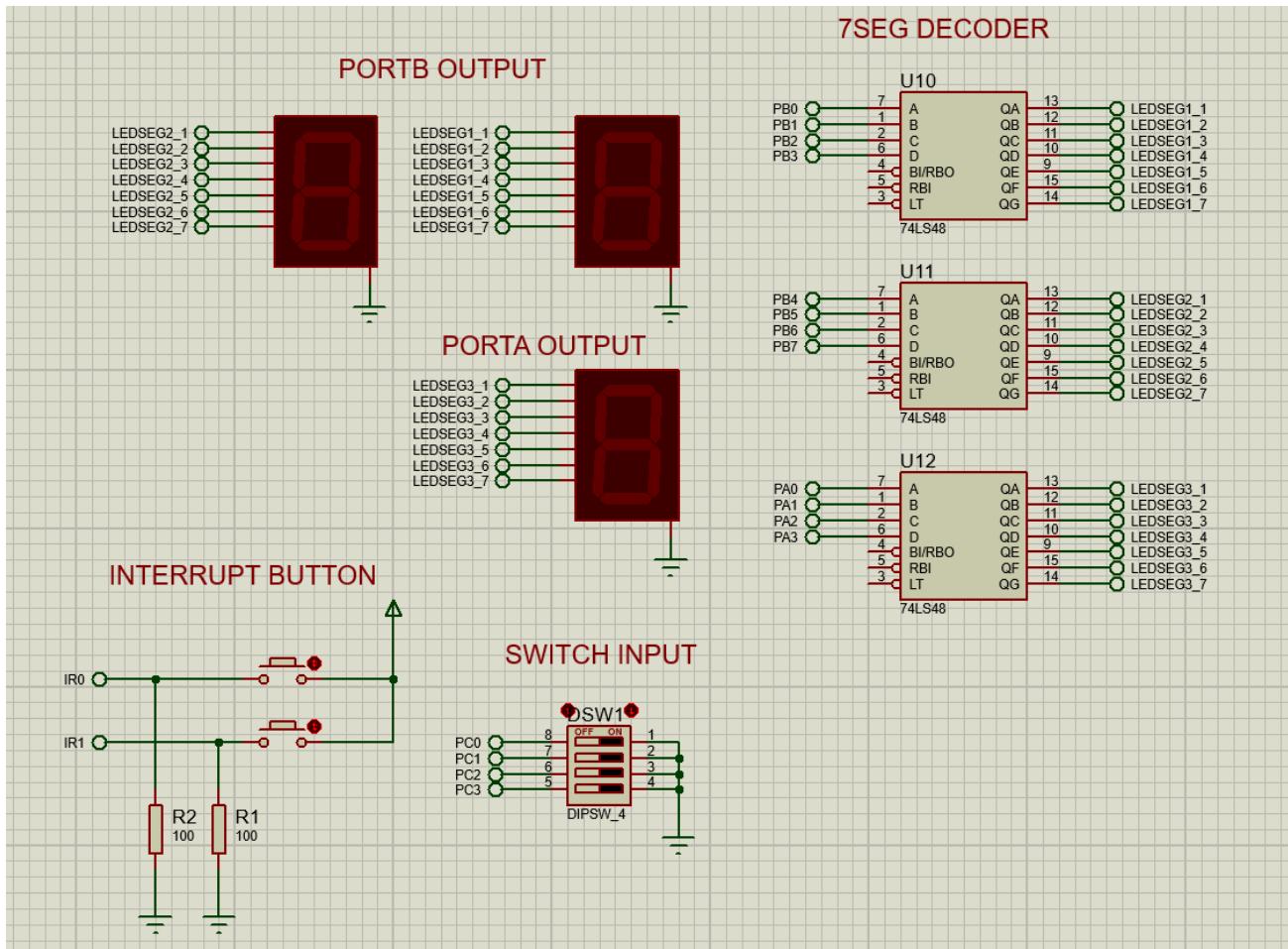
Interrupt Vector Address: 80H-87H ICW2 = 80H

8086 Mode, Auto EOI ICW4 = 03H

only IR0 and IR1 are unmasked OCW11 = 0FCH







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1 PROCED1 SEGMENT
2 ISR1 PROC FAR
3 ASSUME CS:PROCED1, DS:DATA
4 ORG 01000H; write code within below starting at address 08000H
5 PUSHF; push 16-bit operands
6 PUSH AX; save program context
7 PUSH DX
8
9 ;<write the ISR code here>
10 MOV DX, PORTA
11 MOVAL, 09H
12 OUT DX, AL
13
14 POP DX; retrieve program context
15 POPAX
16 POPF; pop 16-bit operands
17 IRET; return from interrupt
18 ISR1 ENDP; end of procedure
19 PROCED1 ENDS

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20
21 PROCED2 SEGMENT
22 ISR2 PROC FAR
23 ASSUME CS:PROCED2, DS:DATA
24 ORG 02000H; write code within below starting at address 09000H
25 PUSHF; push 16-bit operands
26 PUSH AX; save program context
27 PUSH DX
28
29 ;<write the ISR code here>
30 MOV DX, PORTA
31 MOVAL, 00H
32 OUT DX, AL
33
34 POP DX; retrieve program context
35 POPAX
36 POPF; pop 16-bit operands
37 IRET; return from interrupt
38 ISR2 ENDP; end of procedure
39 PROCED2 ENDS
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40
41 DATA SEGMENT
42 ORG 03000H
43 PORTA EQU 0F0H; PORTA address
44 PORTB EQU 0F2H; PORTB address
45 PORTC EQU 0F4H; PORTC address
46 COM_REG EQU 0F6H; Command Register Address
47 PIC1 EQU 0F8H; A1 = 0
48 PIC2 EQU 0FAH; A1 = 1
49 ICW1 EQU 13H; refer to #4
50 ICW2 EQU 80H; refer to #4
51 ICW4 EQU 03H; refer to #4
52 OCW1 EQU 0FCH; refer to #4
53 DATA ENDS
54
55 STK SEGMENT STACK
56 BOS DW 64d DUP(?) stack depth (bottom of stack)
57 TOS LABEL WORD; top of stack
58 STK ENDS
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60  CODE SEGMENT PUBLIC 'CODE'
61  ASSUME CS:CODE, DS:DATA, SS:STK
62  ORG 08000H ; write code within below starting at address 0E000H
63  START:
64      MOV AX, DATA
65      MOV DS, AX ; set the Data Segment address
66      MOV AX, STK
67      MOV SS, AX ; set the Stack Segment address
68      LEA SP, TOS ; set address of SP as top of stack
69      CLI ; clears IF flag
70
71      ;program the 8255
72      MOV DX, COM_REG
73      MOV AL, 89H
74      OUT DX, AL
75
76      ;program the 8259
77      MOV DX, PIC1 ; set I/O address to access ICW1
78      MOVAL, ICW1
79      OUT DX, AL ; send command word
80      MOV DX, PIC2 ; set I/O address to access ICW2,ICW4 and OCW1
81      MOVAL, ICW2
82      OUT DX, AL ; send command word
83      MOVAL, ICW4
84      OUT DX, AL ; send command word
85      MOVAL, OCW1
86      OUT DX, AL ; send command word
87      STI ; enable INTR pin of 8086
88
89      MOV AX, OFFSET ISR1 ; get offset address of ISR1 (IP)
90      MOV [ES:200H], AX ; store offset address to memory at 200H
91      MOVA, SEG ISR1 ; get segment address of ISR1 (CS)
92      MOV [ES:202H], AX ; store segment address to memory at 202H
93      MOVA, OFFSET ISR2 ; get offset address of ISR2 (IP)
94      MOV [ES:204H], AX ; store offset address to memory at 204H
95      MOVA, SEG ISR2 ; get segment address of ISR2 (CS)
96      MOV [ES:206H], AX ; store segment address to memory at 206H
97

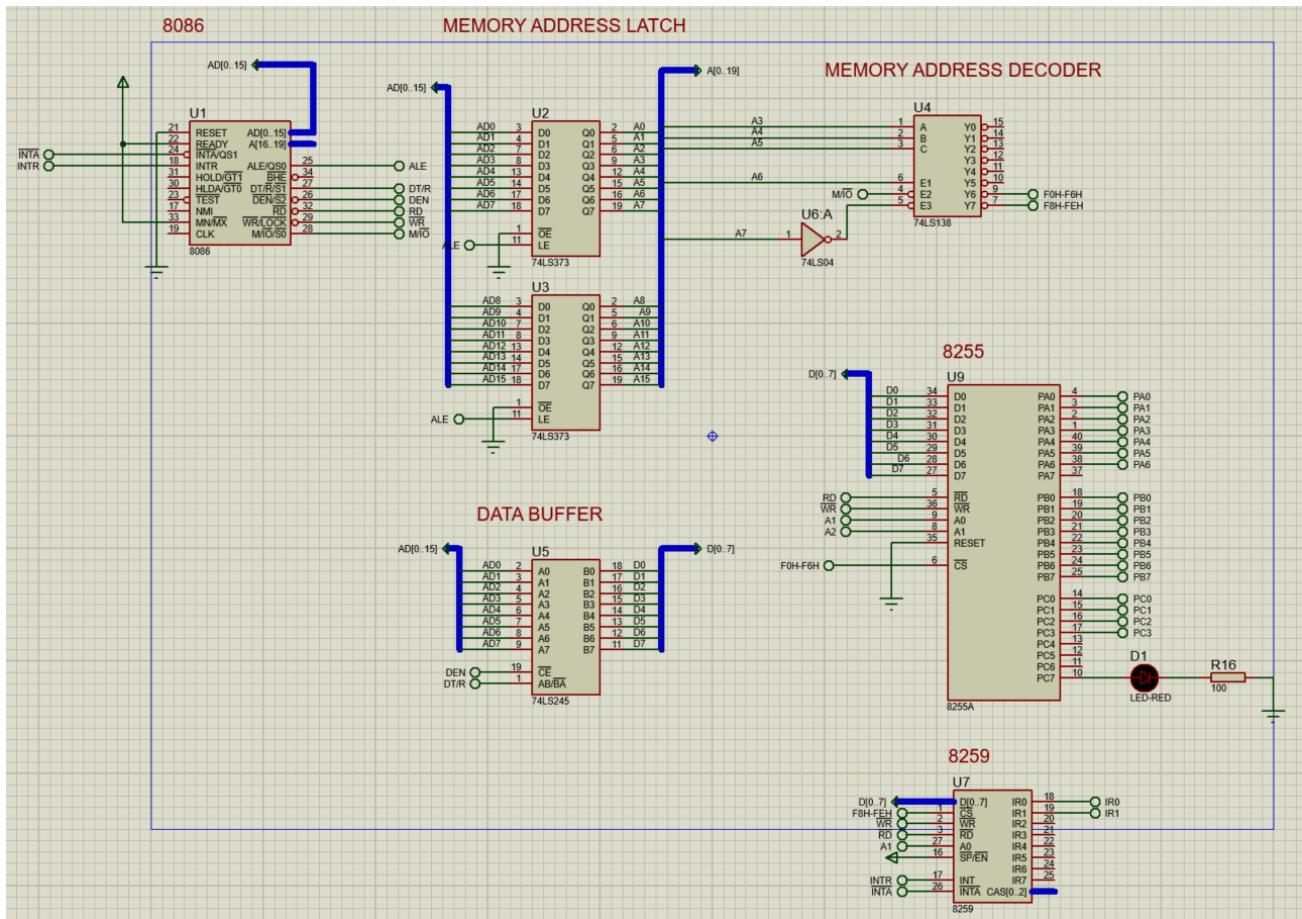
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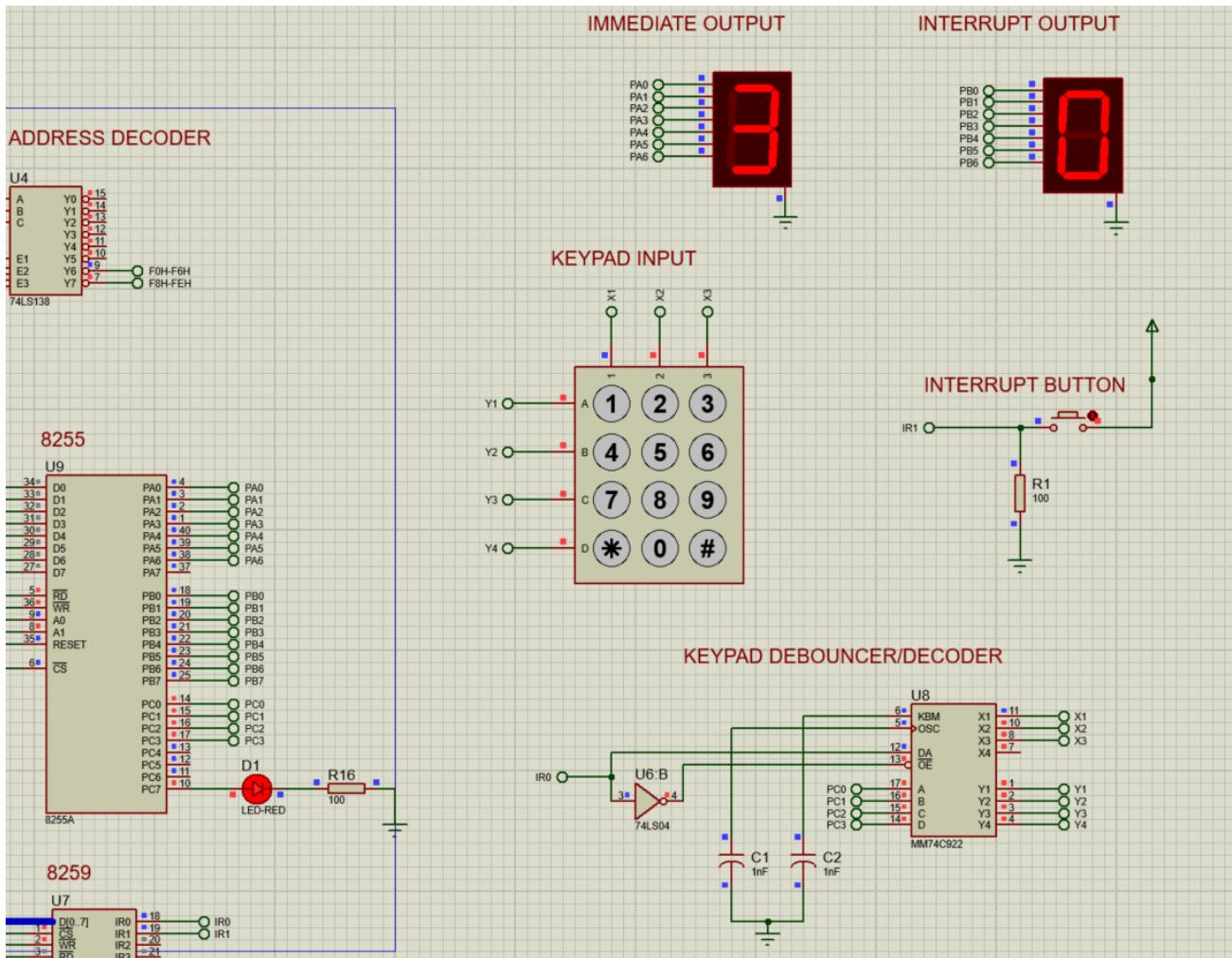
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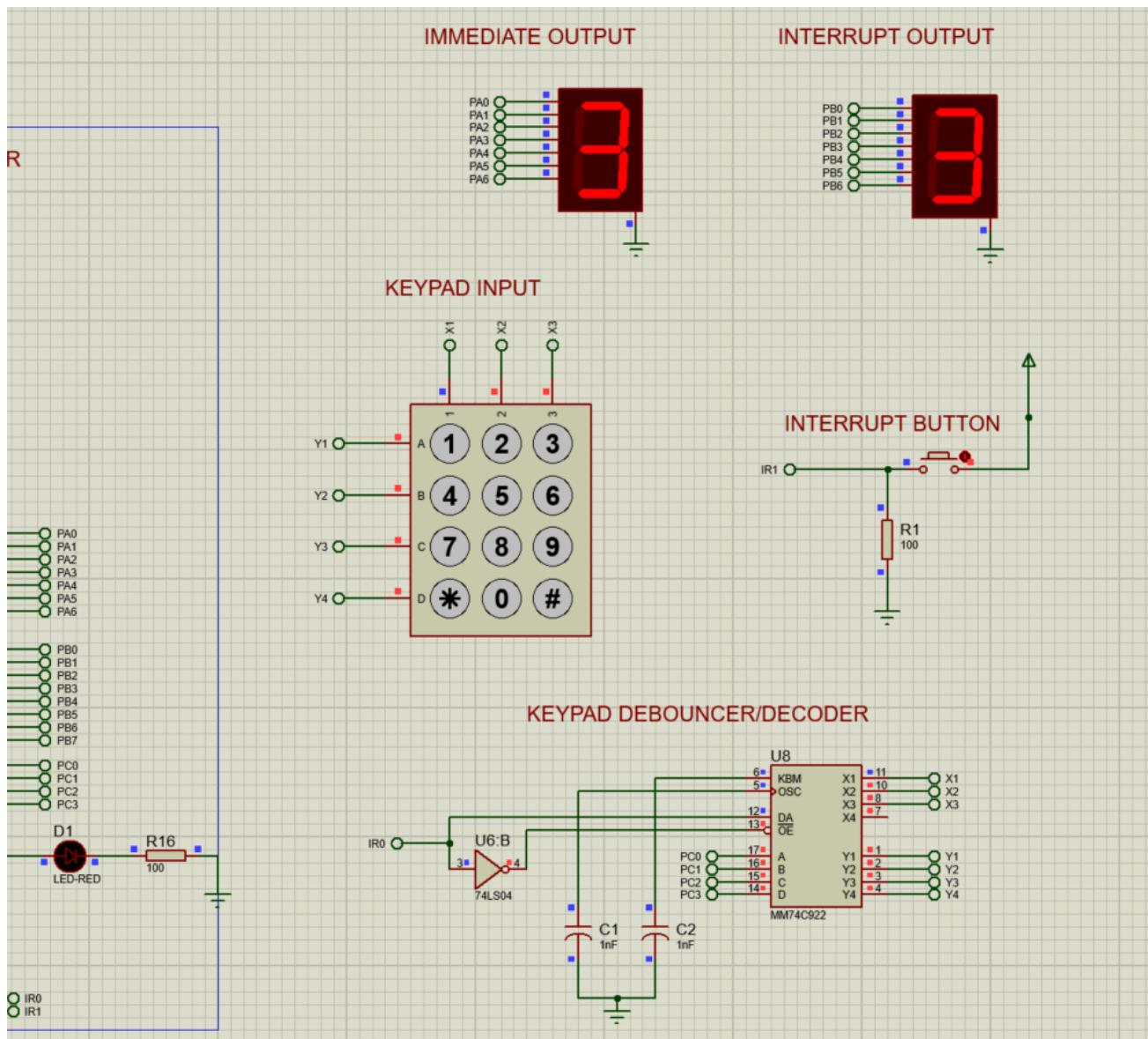
98  ;foreground routine
99  HERE:
100     ;<insert foreground routine code here>
101     _WAIT:
102     MOV DX, PORTC
103     IN AL, DX
104     AND AL, 0FH
105
106     CMP AL, 09H
107     JG GREATER
108
109     MOV DX, PORTB
110     OUT DX, AL
111     JMP _WAIT
112
113     GREATER:
114     MOV DX, PORTB
115     MOV AL, 00H
116     OUT DX, AL
117
118     JMP HERE
119
120     CODE ENDS
121     END START

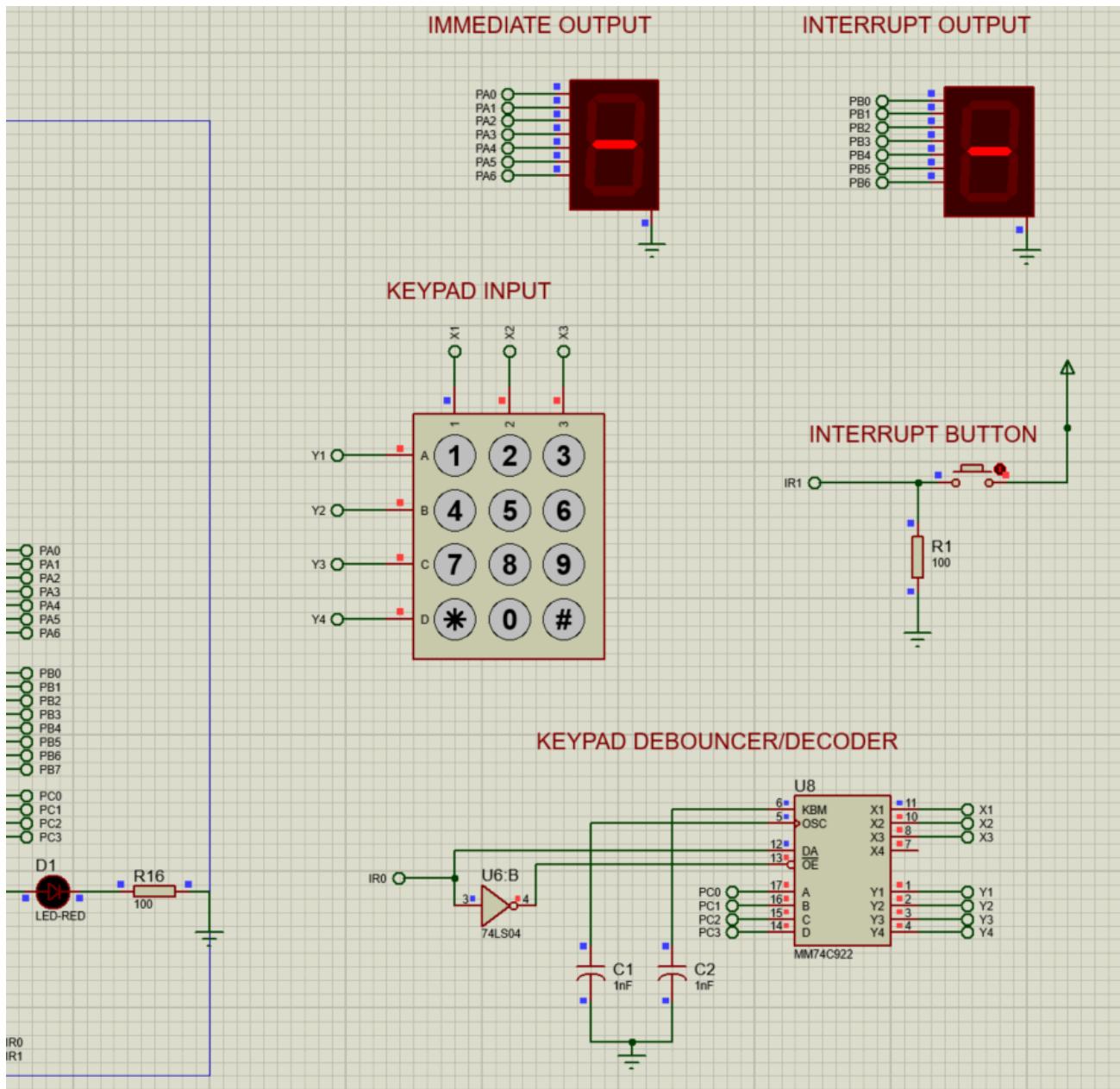
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Activity #2









<pre> 1 PROCED1 SEGMENT 2 ISR1 PROC FAR 3 ASSUME CS:PROCED1, DS:DATA 4 ORG 01000H 5 PUSHF; push 16-bit operands 6 PUSH AX; save program context 7 PUSH DX 8 9 MOVDX, PORTC 10 INAL,DX 11 ANDAL,0FH 12 CMPAL,00H 13 JE _ONE 14 CMPAL,01H 15 JE _TWO 16 CMPAL,02H 17 JE _THREE 18 CMPAL,04H 19 JE _FOUR 20 CMPAL,05H 21 JE _FIVE 22 CMPAL,06H 23 JE _SIX 24 CMPAL,08H 25 JE _SEVEN 26 CMPAL,09H 27 JE _EIGHT 28 CMPAL,0AH 29 JE _NINE 30 CMPAL,0CH 31 JE _DASH 32 CMPAL,0DH 33 JE _ZERO 34 CMPAL,0EH 35 JE _DASH 36 37 _ZERO: 38 MOVCL, AL 39 MOVDX, PORTA 40 MOVAL, NUMB0 41 OUTDX, AL 42 JMPEND_CHECK 43 _ONE: 44 MOVCL, AL 45 MOVDX, PORTA 46 MOVAL, NUMB1 47 OUTDX, AL 48 JMPEND_CHECK 49 _TWO: 50 MOVCL, AL 51 MOVDX, PORTA </pre>	<pre> 51 MOVDX, PORTA 52 MOVAL, NUMB2 53 OUTDX, AL 54 JMPEND_CHECK 55 _THREE: 56 MOVCL, AL 57 MOVDX, PORTA 58 MOVAL, NUMB3 59 OUTDX, AL 60 JMPEND_CHECK 61 _FOUR: 62 MOVCL, AL 63 MOVDX, PORTA 64 MOVAL, NUMB4 65 OUTDX, AL 66 JMPEND_CHECK 67 _FIVE: 68 MOVCL, AL 69 MOVDX, PORTA 70 MOVAL, NUMB5 71 OUTDX, AL 72 JMPEND_CHECK 73 _SIX: 74 MOVCL, AL 75 MOVDX, PORTA 76 MOVAL, NUMB6 77 OUTDX, AL 78 JMPEND_CHECK 79 _SEVEN: 80 MOVCL, AL 81 MOVDX, PORTA 82 MOVAL, NUMB7 83 OUTDX, AL 84 JMPEND_CHECK 85 _EIGHT: 86 MOVCL, AL 87 MOVDX, PORTA 88 MOVAL, NUMB8 89 OUTDX, AL 90 JMPEND_CHECK 91 _NINE: 92 MOVCL, AL 93 MOVDX, PORTA 94 MOVAL, NUMB9 95 OUTDX, AL 96 JMPEND_CHECK 97 _DASH: 98 MOVCL, AL 99 MOVDX, PORTA 100 MOVAL, NUMBN 101 OUTDX, AL </pre>
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<pre> 102 JMP END_CHECK 103 104 END_CHECK: 105 POPDX; retrieve program context 106 POPAX 107 POPF; pop 16-bit operands 108 IRET; return from interrupt 109 ISR1 ENDP, end of procedure 110 PROCED1 ENDS 111 112 PROCED2 SEGMENT 113 ISR2 PROC FAR 114 ASSUME CS:PROCED2, DS:DATA 115 ORG 02000H 116 PUSHF; push 16-bit operands 117 PUSHAX; save program context 118 PUSH DX 119 120 CMP CL,00H 121 JE _ONE 122 CMP CL,01H 123 JE _TWO 124 CMP CL,02H 125 JE _THREE 126 CMP CL,04H 127 JE _FOUR 128 CMP CL,05H 129 JE _FIVE 130 CMP CL,06H 131 JE _SIX 132 CMP CL,08H 133 JE _SEVEN 134 CMP CL,09H 135 JE _EIGHT 136 CMP CL,0AH 137 JE _NINE 138 CMP CL,0CH 139 JE _DASH 140 CMP CL,0DH 141 JE _ZERO 142 CMP CL,0EH 143 JE _DASH 144 145 _ZERO: 146 MOVDX, PORTB 147 MOVAL, NUMB0 148 OUTDX, AL 149 JMP END_CHECK 150 _ONE: 151 MOVDX, PORTB 152 MOVAL, NUMB1 </pre>	<pre> 153 OUTDX, AL 154 JMP END_CHECK 155 _TWO: 156 MOVDX, PORTB 157 MOVAL, NUMB2 158 OUTDX, AL 159 JMP END_CHECK 160 _THREE: 161 MOVDX, PORTB 162 MOVAL, NUMB3 163 OUTDX, AL 164 JMP END_CHECK 165 _FOUR: 166 MOVDX, PORTB 167 MOVAL, NUMB4 168 OUTDX, AL 169 JMP END_CHECK 170 _FIVE: 171 MOVDX, PORTB 172 MOVAL, NUMB5 173 OUTDX, AL 174 JMP END_CHECK 175 _SIX: 176 MOVDX, PORTB 177 MOVAL, NUMB6 178 OUTDX, AL 179 JMP END_CHECK 180 _SEVEN: 181 MOVDX, PORTB 182 MOVAL, NUMB7 183 OUTDX, AL 184 JMP END_CHECK 185 _EIGHT: 186 MOVDX, PORTB 187 MOVAL, NUMB8 188 OUTDX, AL 189 JMP END_CHECK 190 _NINE: 191 MOVDX, PORTB 192 MOVAL, NUMB9 193 OUTDX, AL 194 JMP END_CHECK 195 _DASH: 196 MOVDX, PORTB 197 MOVAL, NUMBN 198 OUTDX, AL 199 JMP END_CHECK 200 201 END_CHECK: 202 POPDX; retrieve program context 203 POPAX </pre>
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<pre> 204 POPF; pop 16-bit operands 205 IRET; return from interrupt 206 ISR2 ENDP, end of procedure 207 PROCED2 ENDS 208 DATA SEGMENT 209 ORG 03000H 210 PORTA EQU 0F0H; PORTA address 211 PORTB EQU 0F2H; PORTB address 212 PORTC EQU 0F4H; PORTC address 213 COM_REG EQU 0F6H; Command Register Address 214 PIC1 EQU 0F8H A1 = 0 215 PIC2 EQU 0FAH A1 = 1 216 ICW1 EQU 13H 217 ICW2 EQU 80H 218 ICW4 EQU 03H 219 OCW1 EQU 0FCFH 220 NUMB0 EQU 0011111B; 0 221 NUMB1 EQU 00000110B; 1 222 NUMB2 EQU 0101101B; 2 223 NUMB3 EQU 0100111B; 3 224 NUMB4 EQU 01100110B; 4 225 NUMB5 EQU 01101101B; 5 226 NUMB6 EQU 01111101B; 6 227 NUMB7 EQU 00000111B; 7 228 NUMB8 EQU 01111111B; 8 229 NUMB9 EQU 01101111B; 9 230 NUMBN EQU 01000000B; 231 DATA ENDS 232 233 STK SEGMENT STACK 234 BOS DW 64d DUP(?) stack depth (bottom of stack) 235 TOS LABEL WORD top of stack 236 STK ENDS 237 238 CODE SEGMENT PUBLIC CODE' 239 ASSUME CS:CODE, DS:DATA, SS:STK 240 ORG 03000H 241 242 START: 243 MOVAX, DATA 244 MOVDS, AX; set the Data Segment address 245 MOVAX, STK 246 MOVSS, AX; set the Stack Segment address 247 LEA SP, TOS ; set address of SP as top of stack 248 CLI; clears IF flag 249 250 251 ;program the 8255 252 MOVDX, COM_REG 253 MOVAL, 81H 254 OUTDX, AL </pre>	<pre> 255 ;program the 8259 256 MOVDX, PIC1; set I/O address to access ICW1 257 MOVAL, ICW1 258 OUTDX, AL; send command word 259 MOVDX, PIC2; set I/O address to access ICW2,ICW4 and OCW1 260 MOVAL, ICW2 261 OUTDX, AL; send command word 262 MOVAL, ICW4 263 OUTDX, AL; send command word 264 MOVAL, OCW1 265 OUTDX, AL; send command word 266 STI, enable INTR pin of 8086 267 268 ;storing interrupt vector to interrupt vector table in memory 269 MOVAX, OFFSET ISR1 get offset address of ISR1 (IP) 270 MOV[ES:200H], AX; store offset address to memory at 200H 271 MOVAZ, SEG ISR1; get segment address of ISR1 (CS) 272 MOV[ES:202H], AX; store segment address to memory at 202H 273 MOVAZ, OFFSET ISR2 get offset address of ISR2 (IP) 274 MOV[ES:204H], AX; store offset address to memory at 204H 275 MOVAZ, SEG ISR2; get segment address of ISR2 (CS) 276 MOV[ES:206H], AX; store segment address to memory at 206H 277 278 ;foreground routine 279 MOVDX, PORTA; set port address of PORTA 280 MOVAL, NUMB0 281 OUTDX, AL; 282 283 MOVDX, PORTB; set port address of PORTB 284 MOVAL, NUMB0 285 OUTDX, AL 286 287 HERE: 288 CALL DELAY_5MS 289 CALL DELAY_5MS 290 MOVDX, PORTC 291 MOVAL, 80H 292 OUTDX, AL 293 CALL DELAY_5MS 294 CALL DELAY_5MS 295 MOVAL, 00H 296 OUTDX, AL 297 JMP HERE 298 299 DELAY_5MS: 300 MOV BX, 0DF2H 301 302 L1: 303 DECBX 304 NOP 305 JNZ L1 </pre>
306 RET 307 308 CODE ENDS 309 END START	

Why do you think the LED is blinking steadily while other activities are going on?

In the 8086 system, the LED blinks steadily while other activities are going on because the interrupt service routine (ISR) for the LED is being triggered at regular intervals, independent of other ongoing processes. Hardware interrupts allow the CPU to momentarily pause its current task to execute the ISR, which toggles the LED state. Once the ISR completes, the CPU resumes the interrupted task seamlessly. This ability to manage multiple tasks concurrently via interrupts enables the LED to blink consistently, even while other processes are handled in the background.

What do you think is the ultimate advantage of using interrupts especially involving I/O devices?

The ultimate advantage of using interrupts, especially with I/O devices, is that they allow the 8086 to work efficiently by eliminating the need for constant polling. Instead of the 8086 actively waiting for an I/O device to complete an operation, it can continue executing other tasks until the device signals completion by triggering an interrupt. This reduces idle time, optimizes 8086 usage, and improves the overall responsiveness and performance of the system, particularly in environments requiring real-time or high-speed processing.

References