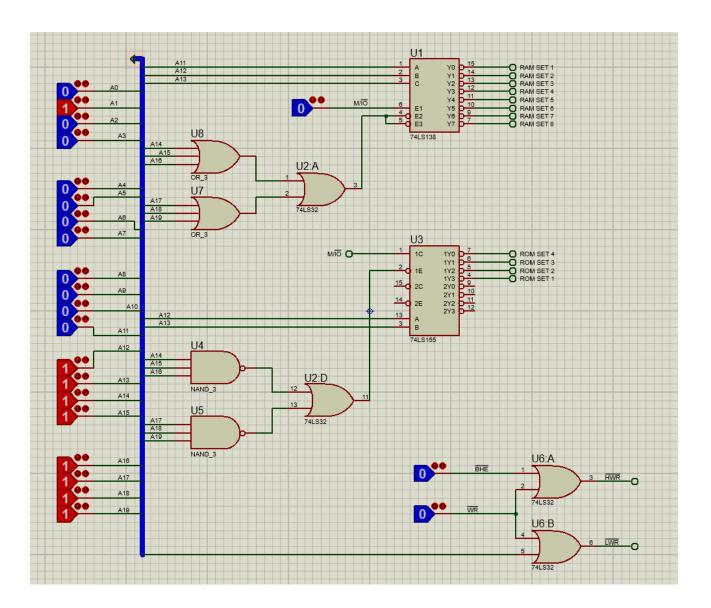


Laboratory Report

Laboratory Exercise No.:	4	Date Performed:	October 14, 2024		
Laboratory Exercise Title:	Memory Interfacing (with Addressing Decoding)				
Name of Student:	Ivor Louisetyne Canque May G. Ochia	Document Version:	1.0		

Activity #1

ADDRESS (A ₁₉ A ₀	,)	M/IO	\overline{WR}	BHE	Memory Set Enabled	HWR	LWR	Observations
0000 0000 1111 0000 0001	00F01H	1	0	0	RAM Set 2	0	1	high bank 8-bit transfer (write)
1111 1100 0110 1000 0010	FC680H	1	0	1	ROM Set 4	1	0	low bank 8-bit transfer (write)
0000 0101 1010 0111 1100	05A7CH	1	1	0	none	1	1	address out of range
1111 1111 0000 0000 0010	FF002H	0	0	0	none	0	1	Accessing isolated
0000 0001 1111 1111 1111	01FFFH	1	1	1	RAM Set 4	1	1	No bank selected
0000 0000 0000 0000 0001	00001H	1	1	0	RAM Set 1	1	1	No bank selected
1111 1011 1111 0000 0011	FBF03H	1	0	0	none	0	1	address out of range
0000 0000 1111 1100 1110	00FCEH	0	1	1	none	1	1	Accessing isolated
0000 0100 0000 0000 0000	04000H	1	0	0	none	0	1	address out of range
0000 0010 0110 0101 1001	02659H	1	0	1	RAM Set 5	1	1	No bank selected



a. How many RAM and ROM chips are used?

There are 16 RAM chips and 8 ROM chips.

b. What is the chip size of the RAM and ROM?

2K x 8 is the chip size of the RAM, and 4K x 8 is the chip size of the ROM.

c. Determine the address range of the RAM and ROM

RAM Address Range

SET	Address Range	
1	00000H - 007FFH	
2	00800H - 00FFFH	
3	01000H - 017FFH	

4	01800H - 01FFFH	
5	02000H - 027FFH	
6	02800H - 02FFFH	
7	03000H - 037FFH	
8	03800H - 03FFFH	

ROM Address Range

SET	Address Range	
1 FF000H - FFFFFH		
2	FE000H - FEFFFH	
3	FD000H - FDFFFH	
4	FC000H - FCFFFH	

d. Based on the number of chips and chip size, calculate and determine the address range (start and end) of each chip sets for both RAM and ROM..

RAM

chip size: 2K = 007FFH

SET	Start Address	End Address	Address Range
1	00000H	00000H + 007FFH = 007FFH	00000H - 007FFH
2	007FFH + 1H = 00800H	00800H + 007FFH = 00FFFH	00800H - 00FFFH
3	00FFFH +1H = 01000H	01000H + 007FFH = 017FFH	01000H - 017FFH
4	017FFH + 1H = 01800H	01800H + 007FFH = 01FFFH	01800H - 01FFFH
5	01FFFH + 1H = 02000H	02000H + 007FFH = 027FFH	02000H - 027FFH
6	027FFH + 1H = 02800H	02800H + 007FFH = 02FFFH	02800H - 02FFFH
7	02FFFH + 1H = 03000H	03000H + 007FFH = 037FFH	03000H - 037FFH
8	037FFH + 1H = 03800H	03800H + 007FFH = 03FFFH	03800H - 03FFFH

ROM

chip size: 4K = 00FFFH

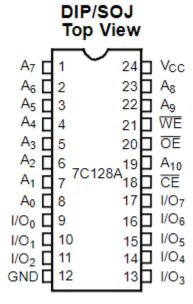
SET	Start Address	End Address	Address Range
1	FFFFFH - 00FFFH = FF000H	FFFFFH	FF000H - FFFFFH
2	FEFFFH - 00FFFH = FE000H	FF000H - 1H = FEFFFH	FE000H - FEFFFH
3	FDFFFH - 00FFFH = FD000H	FE000H - 1H = FDFFFH	FD000H - FDFFFH
4	FCFFFH - 00FFFH = FC000H	FD000H - 1H = FCFFFH	FC000H - FCFFFH

e. Suggest an actual RAM (static RAM) and ROM (EPROM) integrated circuit (IC) with the same size as determined in (b).

RAM CY7C128A pdf, CY7C128A Description, CY7C128A Datasheet, CY7C128A view ::: ALLDATASHEET :::

CY7C128A (2K x 8 Static RAM)

Pin Configurations



C128A-2

M2732A pdf, M2732A Description, M2732A Datasheet, M2732A view ::: ALLDATASHEET :::

M2732A (4K x 8)

24 D VCC A7 🛭 1 A6 🛮 2 23 A8 A5 🛚 3 22 ll A9 A4 🛮 4 21 A11 A3 [5 20 GVPP A2 6 M2732A 19 A10 A1 [7 18 h E 8 D 0A 17 DQ7 16 DQ6 Q0 [9 Q1 [10 15 Q5 14 DQ4 Q2 [11 13 DQ3

Figure 2. DIP Pin Connections

Activity #2

Solution:

RAM: RAM Size: 16K x 16 using 8K x 8

$$no.of\ chips = \frac{RAM\ size}{chip\ size} \times 2\ banks = \frac{16K}{8K} \times 2\ banks = 4\ chips$$

$$no.of\ sets = \frac{no.of\ chips}{2\ banks} = \frac{4}{2} = 2\ sets$$

ROM: ROM Size: 16K x 16 using 8K x 8

$$no. of chips = \frac{ROM \, size}{chip \, size} \times 2 \, banks = \frac{16K}{8K} \times 2 \, banks = 4 \, chips$$

$$no. of \, sets = \frac{no. of \, chips}{2 \, banks} = \frac{4}{2} = 2 \, sets$$

Address Decoding for Memory Banks:

Address Decoding for RAM

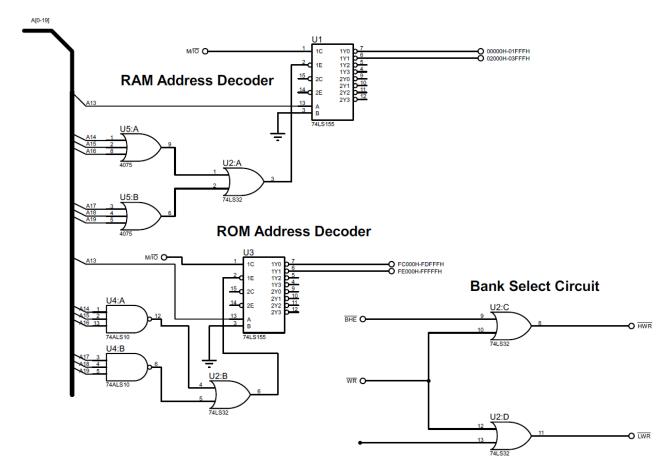
Chip Size: 8K = 01FFFH

SET	Start Address	End Address	Address Range
1	00000H	00000H + 01FFFH = 01FFFH	00000H - 01FFFH
2	01FFFH + 1H = 02000H	02000H + 01FFFH = 03FFFH	02000H - 03FFFH

Address Decoding for ROM

Chip Size: 8K = 01FFFH

SET	Start Address	End Address	Address Range
1	FFFFFH - 01FFFH = FE000H	FFFFFH	FE000H - FFFFFH
2	FDFFFH + 01FFFH = FC000H	FE000H - 1H = FDFFFH	FC000H - FDFFFH



RAM and ROM Address Decoder

References