Shidong Shen

WeChat: seddon2001 | shensd@ios.ac.cn | Homepage | Github

Education

University of Chinese Academy of Sciences (UCAS) Sep 2023 – Jul 2026 (expected)
Institute of Software, Chinese Academy of Sciences (ISCAS) Beijing, China
Master of Computer Science and Technology (CS), Advisor: Prof. Zhilin Wu
Research Focus: LLM4SE, Hardware Formal Verification and Fuzzing

Northwestern Polytechnical University (NWPU) Sep 2019 – Jun 2023
Bachelor of Computer Science and Technology (CS) (Honors Class) | GPA: 3.83/4.10 Xi'an, China
Courses: Computer Architecture: 100 Data Structures: 94 Algorithm Design and Analysis: 95 Compiler Principles: 93

Publication

Formal Verification of RISC-V Processor Chisel Designs [code][paper] SETTA 2024, Hong Kong SAR, China
10th Dependable Software Engineering. Theories, Tools, and Applications
Shidong Shen, Yicheng Liu, Lijun Zhang, Fu Song, Zhilin Wu

- Proposed the first end-to-end approach for formally verifying RISC-V processor designs fully at the Chisel high-level, leveraging Chisel's object-oriented and functional programming constructs.
- Developed a modular and parameterized reference model of RISC-V instructions in Chisel, enabling the generation of customized RISC-V ISA reference model.
- Introduced a novel queue-based synchronization mechanism to reduce correctness verification to a model-checking problem, enabling the use of serval model-checkers.
- Validated the approach on two open-source RISC-V processor designs, discovering 7 real-world unknown bugs and demonstrating three-orders-of-magnitude efficiency improvement over state-of-the-art methods.

Research Experiences

Instruction Set Consistency Formal Verification for RISC-V Processor Sep 2022 – Present

- Conducted in-depth analysis of microarchitecture designs for multiple open-source RISC-V processors, including Rocket, BOOM, XiangShan, and NutShell.
- Employed model checking and symbolic execution to identify discrepancies between processor implementations and the ISA specification.
- Addressed the challenges of formal verification for out-of-order and multi-issue processors using techniques such as pipeline follower and arbitrary multiplexer selection.
- Optimized the verification tool by incorporating design insights from existing tools like riscv-formal and ChiselVerify.
- Interim results published at SETTA 2024

Hybrid Verification of Processors by Synergistic Integration of BMC and Fuzzing [code] Oct 2024 – Apr 2025

- Designed the **BMCFuzz**, a novel two-way hybrid verification approach that synergistically integrates BMC and Fuzzing.
- Implemented a snapshot mechanism to capture processor states, expanding BMC state space exploration.
- Developed an algorithm to select snapshots, improving coverage and bug detection.
- Validated on three RISC-V processors, uncovering new vulnerabilities; manuscript under reviewing.

First-Person Hand Action Recognition Based on Multi-Source Data Fusion Network Dec 2021 – Apr 2022

- Advisor: Assoc. Prof. Guoqing Zhou at Computer Vision and Computational Photography Laboratory, NWPU
- Researched first-person hand action recognition using a multi-source data fusion network.
- Integrated and analyzed data from RGB, optical flow, and depth images to enhance recognition accuracy.
- Designed and implemented a multi-stream Bi-LSTM network using PyTorch to model temporal dependencies across different data modalities.

Projects

LLVM-based Interpreter and Analysis Tools Oct 2023 – Jan 2024
Stack: C/C++, LLVM, Clang

- Developed as part of the Advanced Compilation Principles and Software Analysis and Testing courses.
- Implemented a basic interpreter based on Clang, supporting a subset of C language constructs.

- Developing custom Clang-Tidy checkers for automated rule checking.
- Implementing instrumentation for analyzing and debugging concurrent programs.
- Applied serval flow analysis algorithms to optimize program performance.

GenshinCPU - Seven-Stage Pipelined MIPS Architecture Processor [code][report] Sep 2020 – Aug 2021

Stack: Verilog/SystemVerilog, C/C++, FPGA

- A seven-stage single-issue processor based on the MIPS32 instruction set architecture.
- Contains instruction and data cache, with a frequency of 145MHz, and can run PMON, Ucore, and Linux systems normally
- Responsible for CPU micro-architecture design and Linux kernel adaptation.
- Built CI (Continuous Integration) and Verilator (Accelerated Compilation) infrastructure, saving 300 hours of local debugging time, designed and completed differential testing framework.
- Booted the Linux 2.6 kernel in 3 days, earning the National First Prize in the 5th Loongson Cup.

SQL-OJ Database Online Evaluation System [code] Jan 2022 – Apr 2022

Stack: SQL, HTML, CSS, JavaScript and Python (Django)

- Developed an online SQL assessment platform for teaching, supporting exams, exercises, and student management.
- Designed and implemented front-end (Bootstrap) and back-end (Django) systems with answer analysis.
- Optimized system performance for high concurrency using Redis, Celery, and message queue mechanisms.
- Awarded National Second Prize in the Chinese Collegiate Computing Competition; adopted as the official evaluation system for "Database Principles" at NWPU since 2022.

Intelligent Training Management Platform for Museum Volunteers Apr 2020 – Sep 2020

Stack: HTML, CSS, JavaScript and PHP

- Combined with my personal experience of volunteering at Shaanxi History Museum, I developed a one-stop platform for recruitment, training, management, communication, and guarantee for the museum volunteer groups.
- Currently, it has been used in Shaanxi History Museum with a total of 2,000 users.
- Won the National Second Prize of China Collegiate Computer Computing Contest(WeChat Mini Program Track).

Honors & Awards

Scholarships

- Academic Scholarship, University of Chinese Academy of Sciences 2023, 2024
- AVIC First Class Scholarship, Northwestern Polytechnical University 2022
- Top Student Award, Northwestern Polytechnical University (Top 20 undergraduate) 2021
- China National Scholarship 2020, 2021
- Tencent Grand Prize Scholarship (Top 1 in School of Computer Science, NWPU) 2021

Competitions

- National Second Prize, Chinese Collegiate Computing Competition 2022
- National First Prize, National Student Computer System Capability Challenge (Loongson Cup) 2021
- Meritorious Winner (First Prize), Mathematical Modeling Competition for American Students 2020, 2021
- National Second Prize, China Collegiate Computing Contest 2020, 2021

Leadership & Recognition

- Merit Student, University of Chinese Academy of Sciences 2024
- Outstanding Graduate, Northwestern Polytechnical University 2023
- Top 10 Class Monitors, Northwestern Polytechnical University 2022

Skills

- **Programming Languages**: C/C++, Verilog/SystemVerilog, Chisel, Java/TypeScript, Python, LLVM, PHP, Assembly
- **Tools & Frameworks**: LangChain, Docker, Pytorch, CUDA, Vivado, Git, Vue, React, K8s, FPGA, Django, Chipyard